Development of a Smart Thyristor Valve for HVDC Transmission

Gianluca De Bonis, BSc, MSc



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Abstract

In HVDC transmission schemes, two converters are needed: a rectifier at the sending point and an inverter at the receiving point. Depending on voltage and current ratings, many types of converters can be chosen. For voltages of hundreds of kV and currents of a few kA, thyristor converters are one of the best solutions, because they have the highest voltage withstanding capability and the highest efficiency, compared to other power semiconductor devices.

A thyristor converter is realized by many valve sections, whose volume is approximately occupied for only the 10% by thyristors and for the 10% by the gate drivers. The remaining 80% is taken by passive auxiliary circuits, needed to protect thyristors during turn-on and turn-off commutations.

Aim of this project is the reduction of the auxiliary circuit size, to reduce costs, volume and weight of the overall valve, through the investigation of active, instead of passive solutions.

The project starts from a theoretical investigation, including literature review, and proceeds with simulations of the proposed control methods. The last step is an experimental work, using a reduced scale test circuit.

The proposed active control circuits are successfully validated. Experimental results match simulation results, therefore, the investigated active configurations can be used for improving the actual thyristor valves.

Future directions are high voltage experimental tests and the realisation of a real scale prototype, to verify the effective costs, volume and weight reduction of the updated valve, compared to the current state of the art.

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1. Introduction

Nowadays HVDC (High Voltage DC) transmission represents the most suitable technical solution to transmit electrical power over long distances, generally above 800 km for overhead lines and above 50 km for submarine cables. To connect a HVDC line to the rest of the AC grid, electrical power is converted from AC to DC, transmitted as DC and then converted back to AC, employing two converters overall. The higher is the electrical power to be transmitted, the higher is the voltage level. For voltage levels of 500 kV and beyond and currents of a few kA, thyristor valve converters are still the best technical solution compared to more modern IGBT or SiC MOSFET topologies, thanks to their higher voltage and current ratings, higher efficiency and lower gate power required for the control. The main drawbacks of thyristor valves are that they are bulky, heavy and expensive. The aim of this project it to investigate innovative technical solutions for thyristor valve design, to reduce their cost and their size in terms of volume and weight.

1.1. Background of the research project

Transmission and distribution of electric energy is dominated by the AC technology, because of the ease of transforming AC voltage from one level to another one. Despite this, there are several applications for which DC transmission is more convenient than AC.

Due to its mechanical structure, a cable has a much higher capacitance than an overhead line. When an alternating voltage is imposed on a cable, the total current is the sum of the load current and a capacitive charging current. The latter charges and discharges the cable every half cycle and, even for a cable of a moderate length, it can utilize a major part of the total current carrying capability, severely limiting the amount of useful real power that can be transmitted. In the case of HVDC transmission, apart from the initial transient, the cable draws no capacitive charging current in steady state. Therefore, power transmission is limited only by the resistive losses incurred.

Considering the total cost of lines and stations and comparing AC with DC, a break-even distance can be defined, after which DC results more convenient. As represented in Fig. 1-1, the break-even distance is 800 km for overhead lines and 50 km for submarine cables [1].

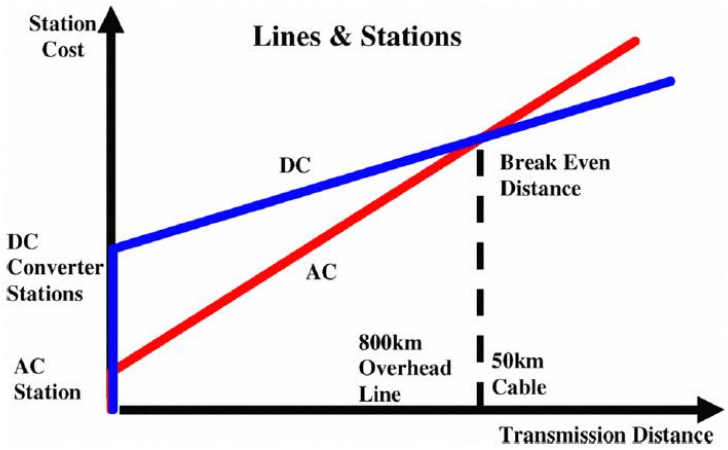


Figure 1-1: DC versus AC transmission – Line and Station Cost [1]

In some situations, DC may be the only feasible method of power transmission, for example when two AC systems operate at different frequencies or when the distance is too long for stable and/or economic AC transmission. In general, HVDC transmission applications can be classified in four broad categories:

1. Transmission of electrical power where AC would be uneconomical, impracticable or subject to environmental restrictions.
2. Interconnection between systems that operate at different frequencies, or between systems which, although they have the same nominal frequency, cannot be operated reliably in synchronism.
3. Electrical power augmentation without significant increase of the short circuit level of the receiving AC system.
4. Improvement of AC system performance by the fast and accurate control of HVDC power.

Any scheme usually involves a combination of two or more of these categories.

When HVDC transmission is chosen, the connection to the rest of the AC grid needs an AC to DC converter, called rectifier, and a DC to AC converter, named inverter.

Depending on the power to be transmitted and on the voltage rating, many types of converters can be chosen. For voltages of hundreds of kV and currents of a few kA, thyristor converters are the best technology as, compared to other power semiconductor devices, they have the highest voltage withstanding capability and the highest efficiency.

Despite the fact that the employment of thyristors is a mature and very reliable technology, it has some important drawbacks. To operate a thyristor safely, bulky and heavy auxiliary circuits are necessary to protect it during turn-on and turn-off commutations. The assembly of thyristors in series and all the relevant auxiliary circuits is called a "valve section": the volume percentage of thyristors, over the overall volume of the valve section, is about 20%, including the gate drivers. To reach the DC transmission voltage, many valve sections need to be connected in series, realising a "thyristor valve". Thyristor valves are very expensive, and the cost of the overall converter is further increased because of its weight, which requires substantial mechanical structures to suspend valves from the roof, to provide seismic protection.

The detailed structure of a thyristor valve is explained in Chap. 4. The typical cross section surface of a valve section is about 8 m^2, and the characteristic weight is 1100 kg. A potential size reduction in terms of volume and weight and an associated cost reduction of thyristor valves represent the challenge of this research project.

1.2. Project Objectives

In terms of volume, only the 20% of a thyristor valve section participates in the voltage conversion, and the remaining 80% is needed for thyristor protection during turn-on and turn-off commutations. This fact leads to a research project aimed to reduce volume and weight of protective auxiliary circuits and, eventually, to decrease costs.

A cost reduction of converters needed for HVDC transmission would make HVDC more competitive, compared to AC, reducing the break-even distance after which DC results more convenient, as shown in Fig. 1-2.

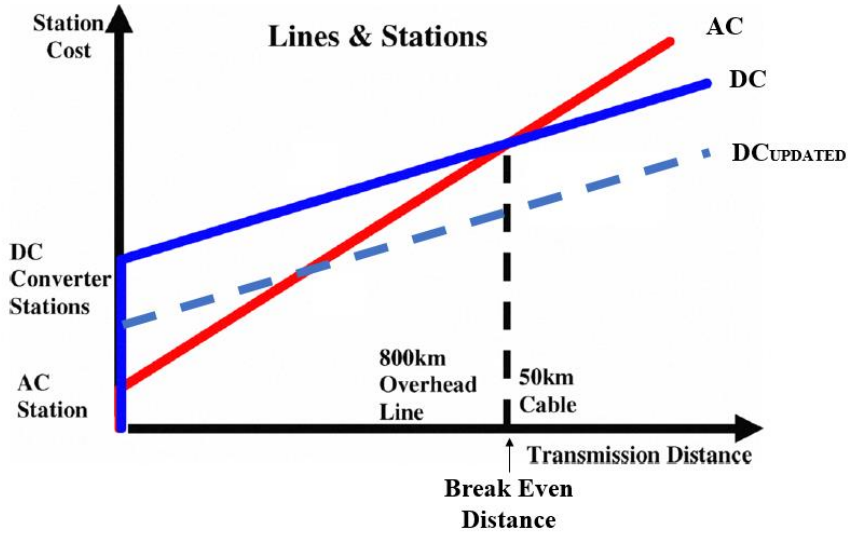


Figure 1-2: DC-AC break-even distance updated for DC cost reduction

Lower break-even distance means that HVDC could be considered for shorter transmission distances, increasing the number of applications.

The proposed solution is based on the design of an active system, able to do what is usually done by passive components, such as di/dt and dv/dt limiting. The replacement of the actual passive remedial components with active circuits can lead to a smarter design of thyristor valves, making them smaller, lighter and cheaper.

Until the 1990s, most of the research was about thyristor improvement, rather than overall valve enhancement. Indeed, in 1987, M. L. Woodhouse wrote a paper about voltage and current stresses implications on valve design, in which appears this

statement: “the considerations that lead to a specific valve design remain a mystery” [2].

The main ideas about active solutions to compensate voltage and current stresses are contained in two Alstom Grid patents of 2014 [3][4]. Investigations of these ideas represent a fundamental part of this research project.

It is reasonable to examine active solutions nowadays and it was not a few decades ago, when the first thyristor valves were set up, because power semiconductor device technology was not mature enough to be used in critical applications. For instance, IGBTs and MOSFETs have much higher current and voltage ratings today and they have a considerably higher reliability. Furthermore, every semiconductor switch needs a gate signal and, depending on the application, a voltage or current sensor for feedback control, which increases the control complexity. In addition, years ago, the computational capacity of microcontrollers and PCs was not high, so it was not possible to manage high complexity control but, nowadays, it is quite straightforward. In the end, both the hardware to be used in the aimed auxiliary active circuits and the control needed, have recently reached the necessary technological level to be employed in the considered application.

The specific objectives of the project are a theoretical investigation of the proposed actively controlled auxiliary circuits, their analysis in a simulation environment, the set up of an experimental rig and the experimental validation of simulation results.

1.3. Thesis Structure and Content

The project is developed in three main parts:

1. A theoretical investigation
2. Simulations
3. Experimental tests

The purpose of chapter two is to introduce the context of application and the state of the art, illustrating the history of HVDC, from the early mercury-arc valves to the actual thyristor valves. Furthermore, the main HVDC configurations are described and some important examples of application are discussed.

Chapter three concerns the physical theory of thyristors, which are the key element of a converter station, starting from a description of the silicon structure and of the V-I characteristics. Subsequently, turn-on and turn-off commutations are examined, relating the limitations to the internal physical phenomena. In addition, a list of models for electrical circuit simulation environment is provided, with a discussion about advantages and disadvantages of each modelling technique. The selected model for simulations is explained in detail, along with choice criteria, and sample simulations are provided.

Chapter four shows the structure of an actual thyristor valve, explaining in detail the function of every single auxiliary component. Afterwards, the purpose of auxiliary active circuits is issued, discussing under which conditions they can replace the actual passive auxiliary components, realizing the same function.

Chapter five contains the simulations done to investigate the innovative ideas. Both turn-on and turn-off control method are illustrated in detail and simulations of real scale operation are provided.

In chapter six, a link between real scale and a reduced scale, to be used in experimental tests, is defined. The purpose and the design of a test circuit are discussed and, afterwards, its operation is illustrated. Doing reduced scale experiments is fundamental, as real scale tests would not be feasible in the university lab, because of the cost, the time required, and safety issues related to high voltage. Aim of the experimental test is to cycle a device under test through the on-state, the turn-off

commutation, the reverse blocking state, the forward blocking state, the turn-on commutation and the on-state again. Commutations can be examined using an oscilloscope and all the active control circuits of interest can be tested.

Chapter seven contains all the relevant experimental results, for both turn-on and turn-off tests. All the pictures from the oscilloscope are represented beside the associated simulation result.

In the end, Chapter eight contains the conclusions and future directions.

2. HVDC Transmission

Although AC is the dominant technique for electrical power transmission, there are certain applications for which DC is preferable to minimize conduction losses of interconnection lines or connecting electricity networks with different frequencies. The standard configuration of a HVDC transmission system is a DC line connected to the rest of the AC grid through an AC to DC converter (sending end) and a DC to AC converter (receiving end). These converters are the core of HVDC transmission and their service began in the 1950s, when mercury arc valves went into operation. Subsequently, thyristor valves replaced mercury arc valves and devices like BJTs, IGBTs and MOSFETs became available so, nowadays, AC to DC converters and DC to AC converters can be designed in many ways, depending on the electrical power to be transmitted and on the voltage level.

In this project, only thyristor valves operating in Line Commutated Converters (LCC) are considered. This is the best technical solution to build a converter with very high voltage and current ratings (hundreds of kV, a few kA), because thyristors are amongst the largest semiconductors of any type produced for any industry, with very high efficiency.

A brief history of the process that conducted from the earliest mercury-arc valves to the actual thyristor valves is described below. Subsequently, different HVDC configurations are considered and the main important features and concepts of operation of 6-pulse and 12-pulse LCC converters are explained. Finally, important applications like the Konti-Skan HVDC line, the Sino-Russia Back to Back, the Three Gorges-Shanghai and the Champa-Kurukshetra schemes are illustrated.

2.1. A Historical Perspective

Although the earliest electrical power systems used DC for generation, transmission and loads, AC transmission replaced DC transmission during the early part of the 20th century, mainly because of the ease of changing voltage levels using transformers.

Nevertheless, DC transmission was still perceived as having advantages over AC transmission in many applications.

Early research efforts were done in the 1930s, when mercury arc rectifiers were invented, but they could not withstand high voltage. The development of high voltage mercury arc valves in the early 1950s made it possible for the first time to economically convert AC power to DC power, and to transmit it as DC. But, in those years, it was a risk to employ a technology that was not mature and, most of the times, the well-developed AC was chosen. With the development of thyristor valves, in the 1970s, solid state thyristors completely replaced mercury-arc valves, and the realization of HVDC transmission lines grew steadily in the last fifty years, as shown in Fig. 2-1 [5].

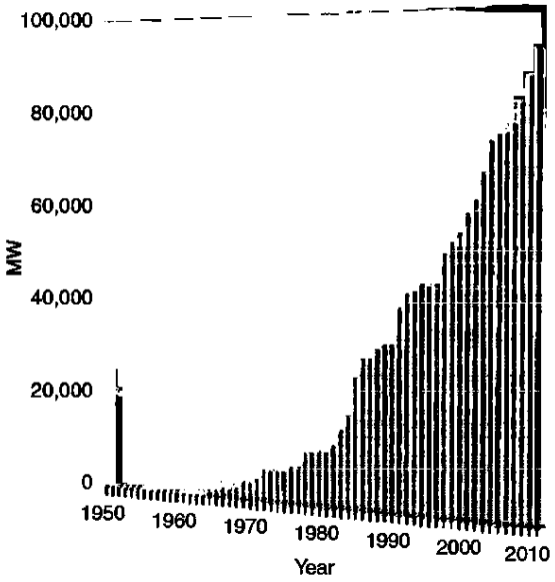


Figure 2-1: Development of HVDC between 1950 and 2010 [5]

The cost of HVDC systems is much higher than the cost of AC systems, except if cables are needed for the transmission link. This is the case of undersea cables, because of the length-dependent reactive power consumption of AC cables. In addition, HVDC results more convenient than AC where AC systems are not developed enough to maintain stable operation of the electrical grid. For example, in countries where population centers are huge and scattered, it is difficult to economically build a strong, integrated AC transmission system, and HVDC is a feasible option for high-power long-distance transmission [5].

An example of replacement of mercury-arc valves by thyristor valves is the Gotland converter station, on the Swedish east coast. It went into service in 1954 and it was the first fully commercial static plant for HVDC, using mercury-arc valves. In the original configuration, it could transfer 20 MW over 98 km, with a voltage of 100 kV. The first thyristor module for HVDC application was employed in Gotland as well, in 1970, increasing the transmitted power to 30 MW and the voltage to 150 kV. The system was further upgraded in 1983 and in 1987. A picture of the Gotland converter station while employing mercury-arc valves and thyristors at the same time is illustrated in Fig. 2-2 [5].



Figure 2-2: Gotland Converter Station with mercury-arc valves and thyristor valves [5]

Between 1980 and 1995 most of the research on valve size reduction was focused on thyristors, rather than other valve components, and the volume of a thyristor valve was reduced to about one-third, while power losses to about one-half. In 1995 the development of thyristors was under way of further increase in withstand voltage and current, even though the size reduction was already reaching the saturation level [6].

A research on how to improve the tradeoff relationship between the increase of the dielectric strength of a thyristor and the reduction of conduction losses, through the ion-irradiation technology, is illustrated in [6]. Trends between the late 1970s and 1995 are depicted in Fig. 2-3.

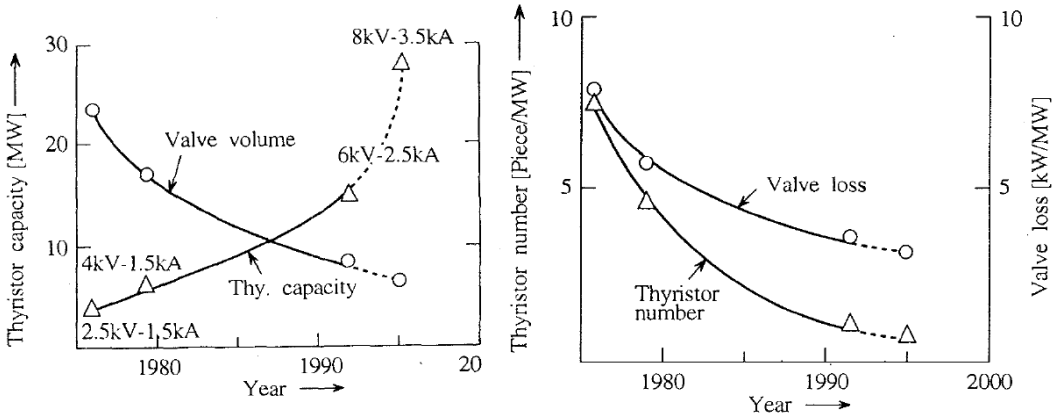


Figure 2-3: Thyristor Capacity and Valve Volume (left) – Number of Thyristors and Valve Loss (right) [6]

In the late 1990s, research was still focused on increasing voltage and current rating of thyristors, to reduce the number of auxiliary components and to make the gating system simpler. The technological level of thyristor valves in 1998 is described in [7].

The complete historical process of thyristor valves from the 1930s until 2007, including further examples of application, is illustrated in detail in [5].

Today, the global electricity power demand is growing in terms of both throughput and efficiency. The economical and technical advantages of HVDC are carefully considered by power system planners, who have to meet also the environmental concerns of the 21st century. In addition, the increasing use of renewable energy sources is contributing to the growth of HVDC applications. Not only the standard HVDC is expanding, but also the UHVDC (Ultra High Voltage DC, for voltages above 600 kVdc) and MVDC (Medium Voltage DC, for voltages below 100 kVdc, in which IGBTs are mostly used).

2.2.HVDC Configurations and Line Commutated Converters

One of the typical structures of a HVDC interconnection is shown in Fig. 2-4. AC power is converted into DC power through a rectifier, transmitted across the DC line, which is either an overhead line or a cable, and converted back into AC through an inverter. The rectifier and the inverter have the same electrical structure, but they work in a different way: the inverter operation is called “inverse operation mode”. Thanks to their structure, two important features of HVDC lines are that they make it possible to connect electricity networks with different frequencies, and they are able to isolate two grids of high-power capabilities under fault conditions.

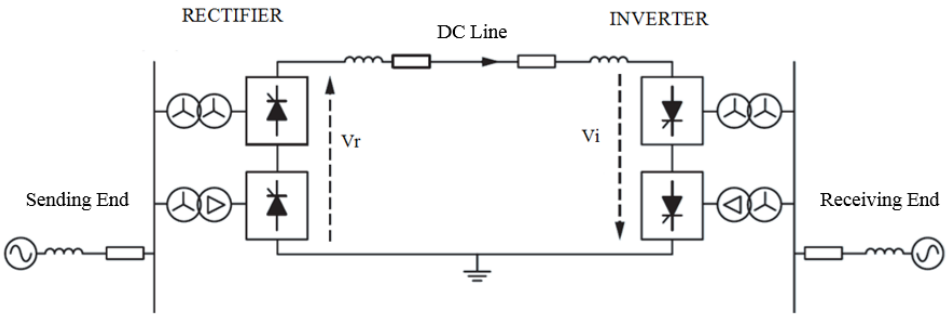


Figure 2-4: Basic HVDC Transmission

The main HVDC configurations are:

- Monopolar with ground return
- Monopolar with metallic return
- Bipolar
- Back to back

A monopolar HVDC system with ground return consists of one or more converter units in series or in parallel at each end, a single conductor and return through the earth or sea, as shown in Fig. 2-5. It can be a cost-effective solution for a HVDC cable transmission and/or the first stage of a bipolar scheme. At each end of the line it requires an electrode line and a ground or sea electrode built for continuous operation.

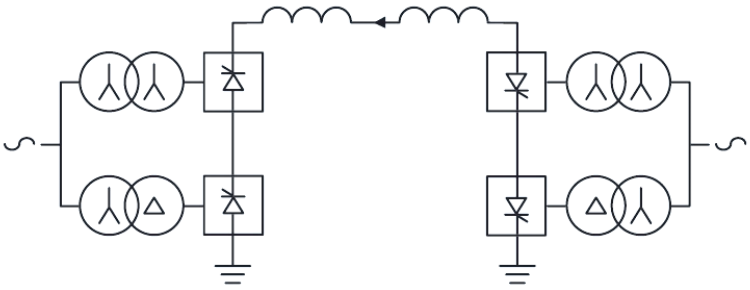


Figure 2-5: Monopolar HVDC system with ground return

A monopolar HVDC system with metallic return usually consists of one high voltage and one medium voltage conductor as shown in Fig. 2-6. Such a configuration is used either as the first stage of a bipolar scheme, avoiding ground currents, or when construction of electrode lines and ground electrodes results in an uneconomical solution, due to a short distance or a high value of earth resistivity [8].

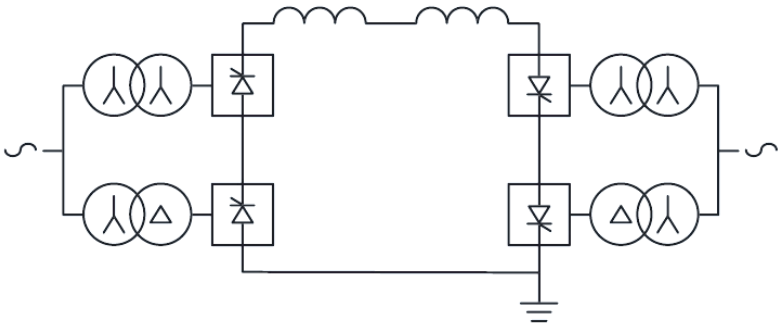


Figure 2-6: Monopolar HVDC system with metallic return

A bipolar HVDC system consists of two poles, each of which includes one or more converter units, in series or in parallel. There are two conductors, one with positive and the other with negative polarity to ground for power flow in one direction. For power flow in the other direction, the two conductors reverse their polarities. The overall electric circuit is a combination of two monopolar schemes with ground return, as shown in Fig. 2-7. With both poles in operation, the imbalance current flow in the ground path can be held to a very low value [8].

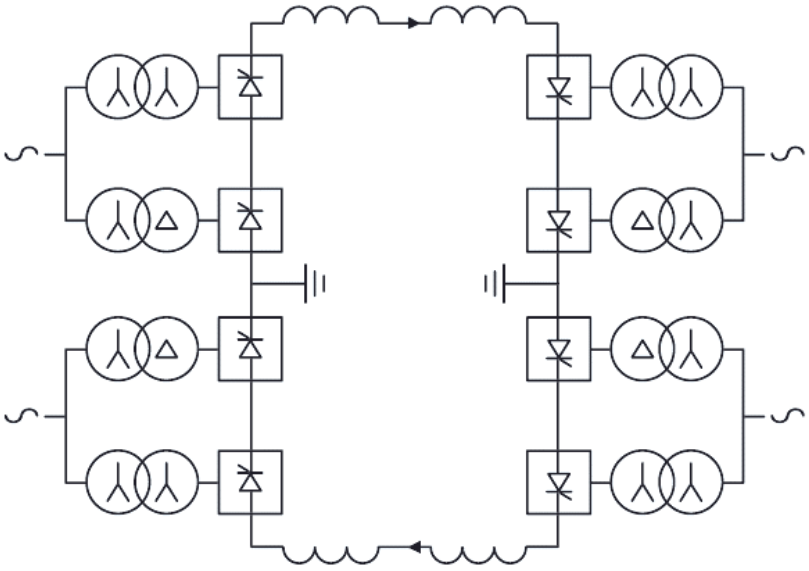


Figure 2-7: Bipolar HVDC system

The bipolar arrangement is very common and provides the following operational capabilities:

- During the outage of one pole, the other one can be operated continuously with ground return.
- When one pole cannot be operated with full load current, the two poles of the bipolar scheme can be operated with different currents, as long as both ground electrodes are connected.
- In case of partial damage to DC line insulation, one or both poles can be continuously operated at a reduced voltage.
- In place of ground return, a third conductor can be added end-to-end. This conductor carries unbalanced currents during bipolar operation and serves as the return path when a pole is out of service.
- For a pole outage, in case long-term ground current flow is undesirable, the bipolar system can be operated in monopolar metallic return mode, if appropriate DC arrangements are provided, as shown in Fig. 2-8.

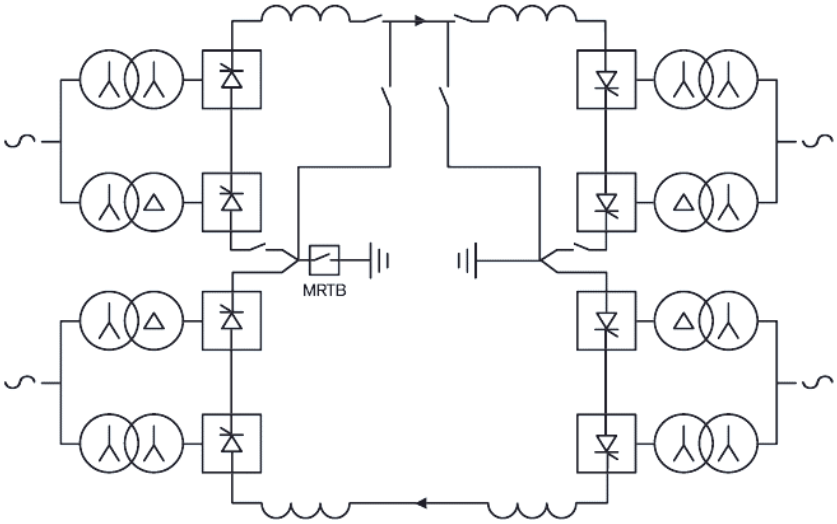


Figure 2-8: Bipolar system with monopolar metallic return for pole outage

Transfer of the current to the metallic path and back without interruption requires a Metallic Return Transfer Breaker (MRTB) and other special purpose switchgear in the ground path of the terminal. If a short interruption of power flow is permitted, the MRTB is not necessary.

Back to back HVDC links are special cases of monopolar HVDC interconnections, for which there is no DC transmission line and both converters are located at the same site. For economic reasons, the valves of both converters may be located in one valve hall. Fig. 2-9 shows two different circuit configurations: smoothing inductors on the DC links might not be required. Generally, for a back-to-back HVDC link, the DC voltage rating is lower and the current rating is higher, compared with HVDC interconnections via overhead lines or cables. The reason is that valve costs are much more voltage-dependent, as the higher is the voltage, the greater the number of thyristors.

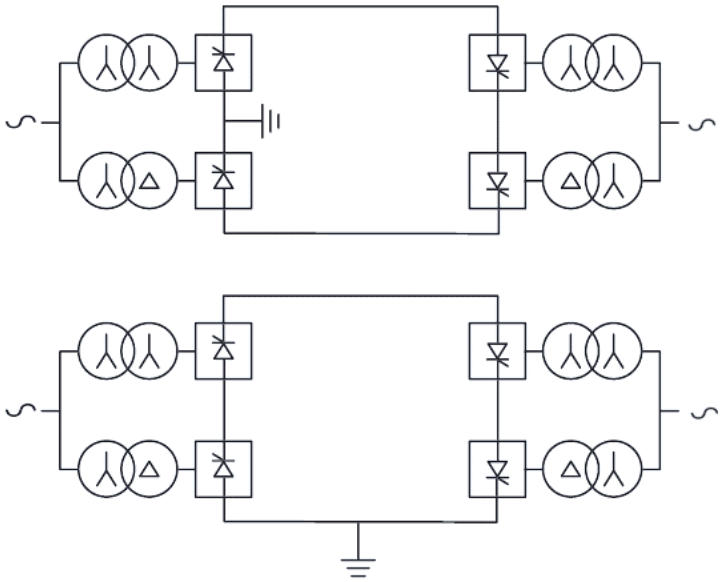


Figure 2-9: Back to Back HVDC interconnection

In the previous pictures of configurations (from Fig. 2-4 to Fig. 2-9), all the converters represented as a single thyristor are a standard six-pulse structure. If two six-pulse converters are connected in series, with a phase-shift of 30 electrical degrees, they realize a twelve-pulse converter, which is one of the most used converter structures for HVDC applications. The detailed electrical scheme of a twelve-pulse converter for a 800 kV application is represented in Fig. 2-10 [9].

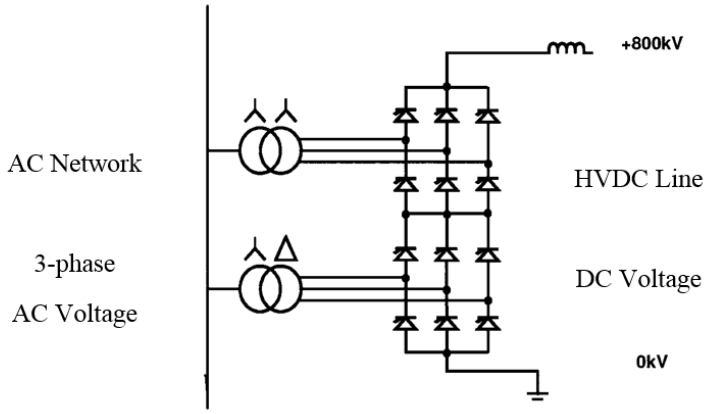


Figure 2-10: Twelve-pulse bridge arrangement

The name of these converters comes from the ripple frequency at the DC side, being six or twelve times the supply frequency. The difference between the DC voltage obtained with a six-pulse and the DC voltage obtained with a twelve-pulse is shown in Fig. 2-11. It is clear how the ripple has a lower amplitude in the case of the twelve-pulse.

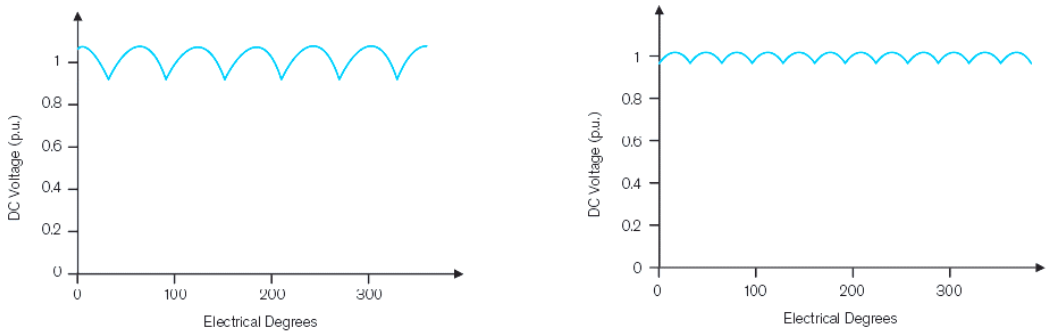


Figure 2-11: DC voltage using six-pulse converters (left) and twelve-pulse converters (right)

Both the six-pulse and the twelve-pulse are called "phase-controlled, line-commutated" converters. The reason why they are addressed as "phase-controlled" is related to the fact that they make use of devices that can be turned on, but not off, by a control action. The "firing angle" of the rectifier and the "extinction angle" of the inverter can be varied to control the DC link. Both the rectifier voltage and the inverter voltage are independently controlled and the DC line current results from the voltage difference across DC line the resistance, according to:

$$I_{DC} = \frac{V_{Rectifier} - V_{Inverter}}{R_{DC}}$$

A "commutation" is the process of transferring current from a switching device to another one. During a commutation, the device that stops conducting "turns-off", while the device that gets into the conduction state "turns-on". The label "line-commutated" (or "naturally commutated") indicates that the commutation process relies on the line voltage of the AC system: the incoming thyristor automatically applies the line voltage, in reverse, to the outgoing one.

The key element of these converters is the thyristor valve (Chap. 4). What is commonly showed as a single thyristor, is in practice a series of thyristor valves, much more

complicated than an individual thyristor. Voltages waveforms on a thyristor valve, for both a rectifier and an inverter, are depicted in Fig. 2-12. Such voltages are shared amongst the valves of the series.

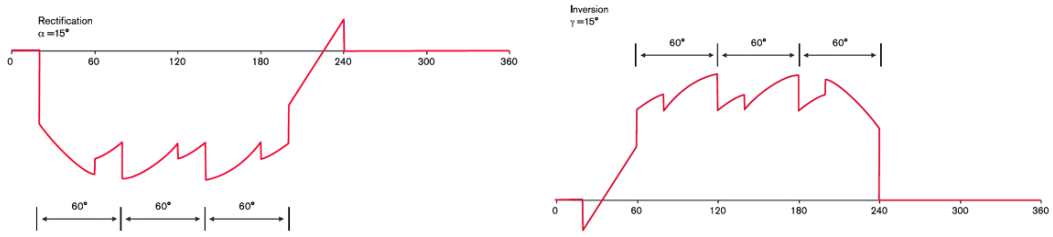


Figure 2-12: Rectifier (left) and Inverter (right) valve voltage waveform excluding commutation overshoots

2.3. Examples of Application

Four examples of existing applications are discussed, in order to highlight some practical issues of interest when operating a converter for several tens of years.

1) The Konti-Skan HVDC link connects Sweden and Denmark and was built in the early 1960s using mercury arc valves [10]. The first pole was rated 250 MW, with a voltage of 250 kV and a rated current of 1 kA, implemented with a single HV conductor and using sea electrodes in both countries to realize the return path through ground and sea. In the 1990s, a second pole was installed, and cables of Pole 1 were replaced with cables of the same ratings as Pole 2, to allow its future upgrade. Pole 2 is rated at 350 MW, operating at a DC voltage of 285 kV and at a rated current of 1230 A. This scheme also had a single HV conductor and shared the existing sea electrode return with Pole 1. In the late 1990s, a full replacement of Pole 1 converters was decided, employing the AREVA (subsequently Alstom Grid) H400 valves for the first time. The main reasons of the decision were that mercury arc valves required significant maintenance activity, with the associated cost of personnel and outages of power, plus they were an environmental issue. When the two poles had different power ratings, they were operated in parallel, with manual control to balance their operation and to minimize current through the sea electrodes. After the Pole 1 update, both poles have the same rating and can be operated as a true bipole, at ±285 kV, reducing the sea electrode current to zero.

Further refurbishment projects, like the Nelson river pole 1, the Mc Neill back to back, the UK-France cable link, and the Haenam-Jeju HVDC link, are discussed in [11]. The main factors that affect refurbishment strategies are: control system obsolescence and cost of control system replacement, compared to cost of valves replacement and cost of both valves and control replacement. The main commercial and operational issues are budget, outage duration, risk strategy, and power contract commitments. There is no single refurbishment strategy that fits all HVDC systems: early installations had many individual design features and constraints, that require the refurbishment process to be addressed paying attention to the specific design. New technologies in control

hardware and software and converter power electronics give the possibility of not only extending the life, but also enhancing the functionality of existing HVDC systems.

2) The Sino-Russia back-to-back HVDC scheme, delivered at the end of 2011 and located at the border between China and Russia, is rated 750 MW and operates at ±125 kV, 3 kA. It employs the H400 electrically-triggered thyristor valves, the same used for the Konti-Skan Pole 1 refurbishment, which design is explained in detail in [12]. The Russian side is normally operated in rectifier mode, with a nominal firing angle of 15°, and the Chinese side in inverter mode, with a nominal extinction angle of 17°. During the ice storm season, the valves could be re-configured into two parallel-connected rectifier bridges to melt the ice on the high voltage transmission lines, by passing high dc current through them. A single line circuit diagram for the converter unit, that is installed on the Chinese side of the border, is depicted in Fig. 2-13. The normal operation voltage for both sides of the AC system ranges from 500 kV to 550kV, with a nominal frequency of 50 Hz. Details of a valve section and of the cooling system are depicted in Fig. 2-14. For this application, the choice of a thyristor converter, represents the optimum compromise between the scheme's low cost and high efficiency requirements.

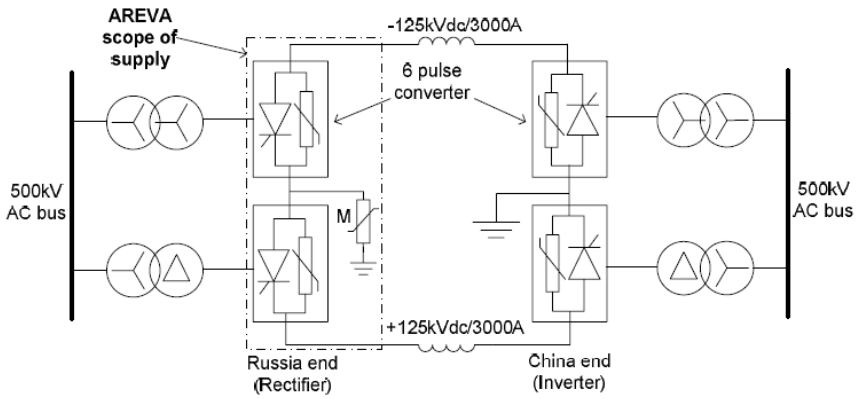


Figure 2-13: Sino-Russia back-to-back HVDC scheme [12]

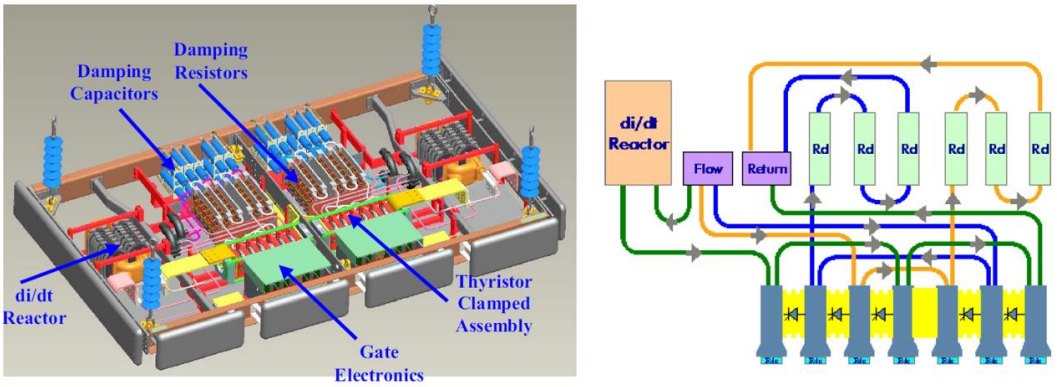


Figure 2-14: Details of the Valve Section (left) and of the Cooling System (right) [12]

3) The Three Gorges Dam, located in the Hubei province, in China, is the second biggest dam in the world, after the Itaipù (located on the border between Brazil and Paraguay). The related hydroelectric power plant is the world's largest power station in terms of installed capacity, with its 22.5 GW, and it is fully functional from 2012. In 2014 it generated 98.8 TWh, setting the world record, surpassed by the Itaipù in 2016, with its 103.1 TWh. Part of the total power is transmitted in AC and part of it in HVDC, depending on the distance of the load centre from the power plant. One of the HVDC transmission lines is the Three Gorges-Shanghai, a 3GW, ±500 kV, 3 kA system [13]. The single line circuit diagram is illustrated in Fig. 2-15 and it is conceptually the same of the Sino-Russia back-to-back. Differences are represented by voltage and current ratings and by the fact that the two converters are not located under the same roof, but 890 km far from each other and connected by an overhead DC line. Thyristor valves used for converters are, also in this case, the AREVA H400, installed for the first time at this voltage rating. The valve assembly uses a double-valve structure and it is suspended from the roof of the valve hall to ensure earthquake withstanding capability.

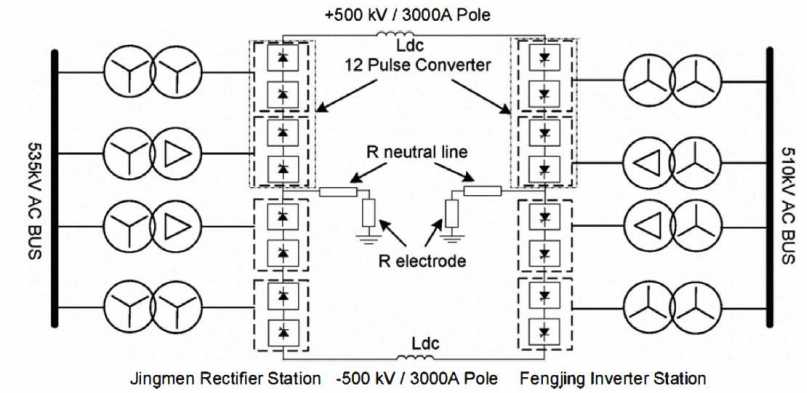


Figure 2-15: One of the HVDC transmission lines of the Three Gorges-Shanghai [13]

4) The Champa-Kurukshetra HVDC scheme is one of the projects scheduled by the India POWERGRID Corporation to reinforce the electricity grid in that region [14]. It is a 3 GW project, rated ±800 kV, 1875 A. The project started in 2012: the first pole was completed in March 2017, while pole 2 was commissioned in September 2017 and it is expected to be completed by December 2018. This HVDC line represents the first application of the H400 valves at such a high voltage: the development process of suitable valves for ±800 kV applications is described in [9]. The project was originally commissioned to Alstom Grid, that combined with GE Digital Energy in 2015, to form GE Grid Solutions. Therefore, the pole 2 was commissioned to the latter. A single line circuit diagram is provided in Fig. 2-16.

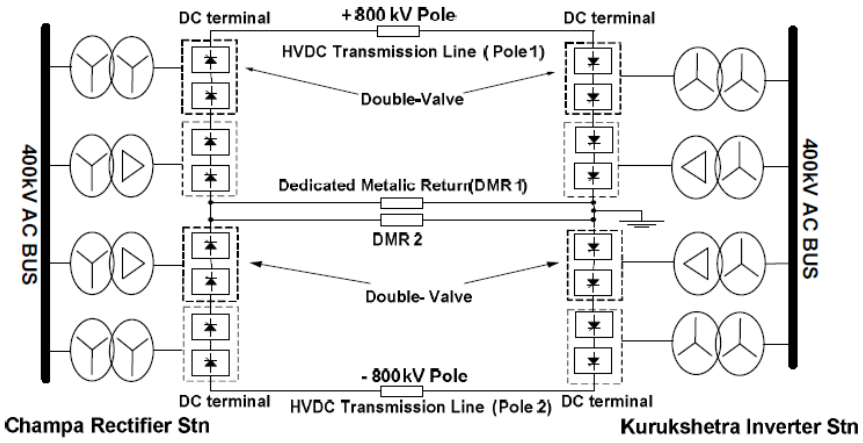


Figure 2-16: Champa-Kurukshetra HVDC Scheme – Pole 1 [14]

The complete scheme comprises four 12-pulse LCC converters. The Champa station is normally operated in rectifier mode and the Kurukshetra station in inverter mode. An unusual feature of the ±800 kV transmission scheme is a Dedicated Metallic Return (DMR) which is firmly earthed at the Kurukshetra converter station abandoning the requirement of grounding electrodes. This method has the main advantage of eliminating corrosion of buried pipelines.

The system will be further upgraded with another 3 GW bi-pole, reaching a total transmitted power up to 6 GW. In detail, since the DC conductors have a significant loading capability, an additional bi-pole of comparable rating will be connected in parallel with the first one, realizing a parallel bi-pole operation.

2.4. Summary

In this chapter, DC lines and AC lines are compared, examining the reasons that lead to the decision of installing a DC interconnection line, rather than an AC one.

The historical path of HVDC is illustrated, starting from the first installations of mercury-arc valves in the 1950s and proceeding with the development of thyristor valves in the 1970s, that led to a complete replacement of mercury-arc valves. The continuous growth of HVDC applications is described, considering also research trends, which always aimed to reduce valve losses and volume, through the augmentation of thyristor voltage and current ratings until the 1990s and through the improvement of the valve auxiliary circuits subsequently.

The main configurations of a HVDC line are described, which are: monopolar with ground return, monopolar with metallic return, bipolar and back-to-back. The most common converter technologies are the 6-pulse and the 12-pulse: the voltage ripple in the two cases is shown, along with the DC link current expression and voltage waveforms on a thyristor valve, in both rectifier and inverter mode.

Four important examples of existing lines are examined, including some considerations on refurbishment strategies.

In the next chapter, the thyristor physical structure is represented, and the V-I static and dynamic characteristics are examined. A classification of the different models to be used in electrical circuit simulation software is provided and the most suitable model for this research project is chosen.

Once the model is chosen, it is inserted into a monopolar 6-pulse converter to run real scale simulations (for convenience, not to slow down simulations) given that, for the proposed scope, there is no need to reach ultra-high voltages and to limit the ripple below a certain threshold. Ground return or metallic return does not make a difference in simulations, while it depends on the specific application in practice.

3. Thyristor Physical Theory and Model Representation

Thyristors used for HVDC valves are amongst the largest semiconductor devices and, compared to GTOs, IGBTs and MOSFETs, have the highest voltage and current ratings, as shown in Fig. 3-1. Very first thyristors, produced in the late fifties, could only block a few hundred volts in their off state and conduct a few amps when turned on. Nowadays, thyristors used in HVDC can withstand voltages greater than 8 kV and conduct currents up to 4 kA [15].

In a thyristor valve for a HVDC converter, thyristors are the most critical components They are expensive devices and there may be many thousands of them in a whole HVDC converter, depending on the power rating. Moreover, they are quite vulnerable during turn-on and turn-off transitions and require many additional components to control and protect them, as explained in Chap. 4.

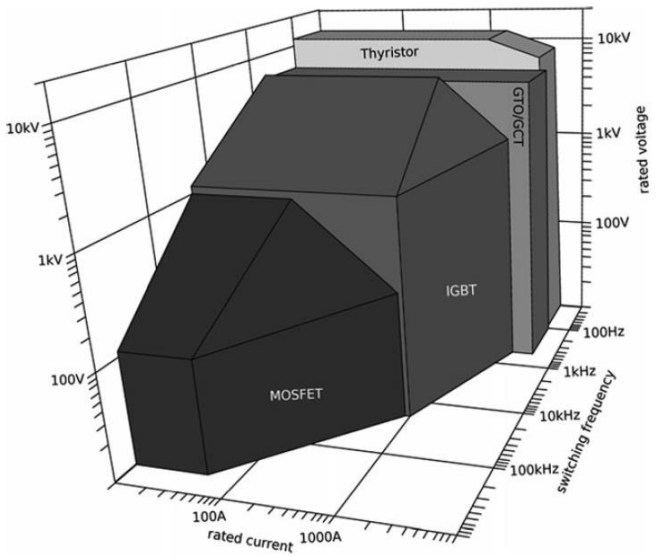


Figure 3-1: Voltage and current ratings of different semiconductor power devices versus switching frequency [15]

Thyristors have three terminals and a unique four-layer construction. They behave as a latching switch, that can be turned on by the control terminal, addressed as gate, but they cannot be turned off by the gate. Current can only flow between the anode and the cathode and, without any gate signal, a high voltage can be supported between the

anode and the cathode with only a small leakage current flow. These properties, plus a very high efficiency, make the thyristor a very suitable component for line-commutated converters, “LCC”, for HVDC.

3.1. Basic Structure and V-I Characteristics

A thyristor is a bipolar switching semiconductor device which behaves like a controllable diode. It has two main terminals, the anode and the cathode, and a smaller control terminal, the gate. Current is normally conducted from anode to cathode.

When anode is negative respect to the cathode, “reverse” voltage is applied, current is not allowed to pass, and voltage is “blocked”. When anode is positive with respect to the cathode, “forward” voltage is applied and the thyristor blocks voltage until a current signal is injected into its gate terminal. Thereafter, the device conducts current until it drops to zero, at which point a reset occurs and the thyristor turns off again.

Plan views of two different gate and cathode layouts are shown in Fig. 3-2. The distributed gate electrode structure is for large-diameter thyristors (10 cm), while the localized structure is for smaller diameter ones. In general, gate and cathode layouts vary greatly depending on the diameter of the device, the intended di/dt capability, and the designed range of switching speed. The circuit symbol for the thyristor is shown in the same picture: it is essentially the symbol of a diode, with the gate control terminal added to it. Voltage and current conventions are pointed out on the symbol.

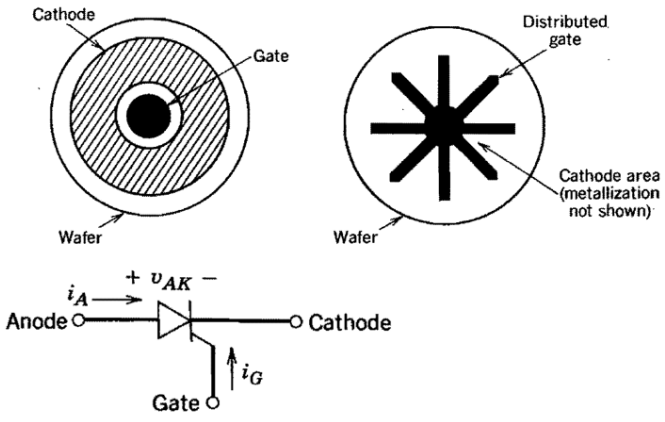


Figure 3-2: Vertical cross section of two different structural layouts and circuit symbol [16]

A distributed gate thyristor, with an 8.5 kV voltage rating, is shown in Fig. 3-3. It has an active silicon diameter of 115 mm, which is built from a silicon ingot of 125 mm diameter, and consequently it is often referred to as “125 mm”, or “5 inch” thyristor. The specific device represented is the Infineon T2871N [17], which main characteristics from the data sheet are contained in Appendix A.

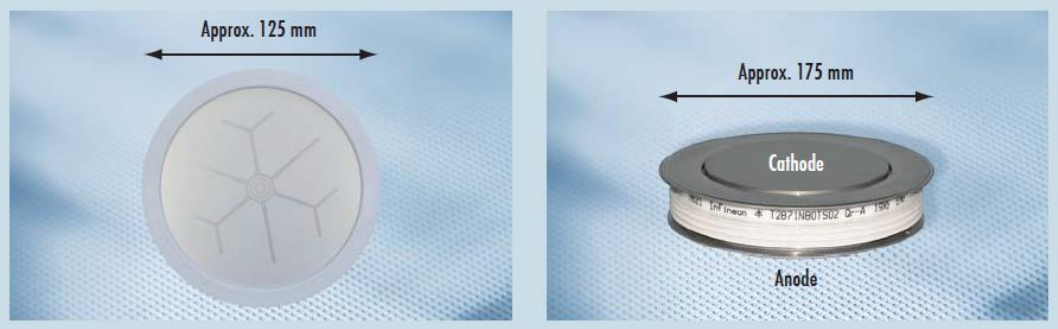


Figure 3-3: Modern 8.5 kV 125 mm thyristor: silicon wafer (left) and complete capsule (right) © Infineon Technology AG

Thyristors can be Electrically Triggered (ETT) or Light Triggered (LTT). This chapter is focussed only on the first type, which is more common. A brief explanation of the basic physics is given, followed by a discussion of the two stable states (ON and OFF) and the two transitional states (turn-on and turn-off).

The thyristor belongs to the “bipolar” family of semiconductor devices as it operates with charge carriers of both polarities (holes and electrons). It has a four-layer structure of alternating p-type and n-type silicon as shown in Fig. 3-4. The n-layer used to form the cathode connection is usually more highly doped than the other layers and is referred to as “n+” layer. On the other hand, the n-layer between the two p-layers is a low doped region and represents the main technological difference between low power devices and high-power devices. The reason why such a region is low doped is related to both the forward and reverse blocking capability. As the length of the n-region is increased, the blocking capability increases at the expense of a higher on-state resistance so, if the length of the n-region is too high, the on-state resistance could become too large. Consequently, the effective length of the n-region is a compromise between satisfactory blocking capability and low on-state voltage.

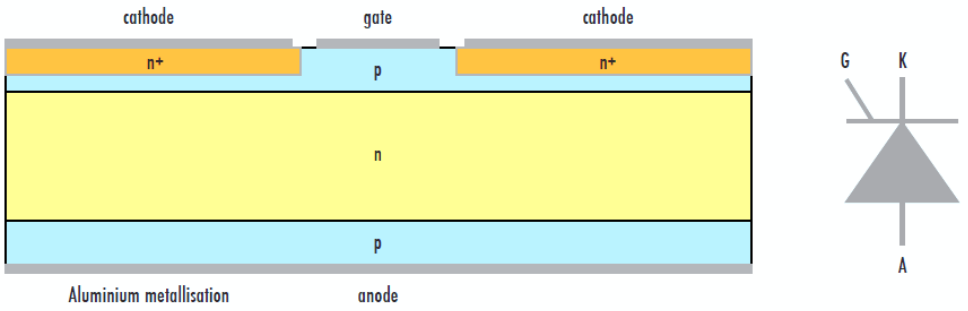


Figure 3-4: Simple thyristor structure

The operation can be understood by examining the "two transistor model" represented in Fig. 3-5. The four layers are associated to two BJTs, a PNP and an NPN, connected in the following way: the collector of the PNP is connected to the base of the NPN, and the base of the PNP to the collector of the NPN.

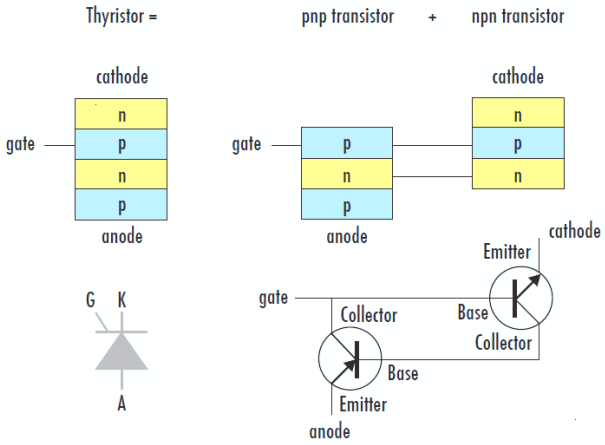


Figure 3-5:The two-transistor model of a thyristor

For the thyristor to be turned on, it needs a pulse of current to be injected into the gate terminal when voltage across it is positive. The effect of this is to introduce current into the base of the NPN and to pass a larger current from collector to emitter. The collector current into the NPN results in base current of the PNP, that causes the PNP to pass more current from its collector to emitter. The PNP collector current feeds back into the NPN base, causing more current from its collector to its emitter and more current in the PNP base and so on. A positive feedback mechanism is created and the

thyristor “latches” into the conducting state. Once turned on, the thyristor remains on until the external circuit reduces current below a critical level, called “holding current”.

Concerning off-state properties, an ideal thyristor would pass no current and block any voltage applied to it in either direction. Real thyristors fall short of this ideal in several respects, allowing small amounts of current to pass, and being sensitive to the rate of change of voltage (dv/dt) applied.

When the device is not turned on, it blocks voltages of both polarities because there is always at least one reverse-biased p-n junction in each direction. If a forward voltage is applied, it is supported by the junction between the upper p layer and lower n layer, in the same way of a reverse biased diode. For a short distance on either side of the junction, charge carriers are cancelled out and a “depletion region”, also known as space-charge-region, is created, where the semiconductor behaves like an electrical insulator. Like any thin insulating layer, the depletion region behaves as a capacitance and, consequently, an off-state thyristor has a measurable capacitance, known as its “junction capacitance”. Because the width of the depletion region increases with the applied voltage, the junction capacitance is non linear, reducing as voltage is increased.

When the thyristor is reverse biased, two depletion regions are formed: one at the junction between the gate and the cathode and one at the junction between the anode and the lower n region, so called “n-base”. The gate-cathode junction is capable of withstanding only quite a low voltage, while the anode-n-base takes up most of the voltage across the thyristor.

Depletion regions for both reverse and forward voltage are depicted in Fig. 3-6.

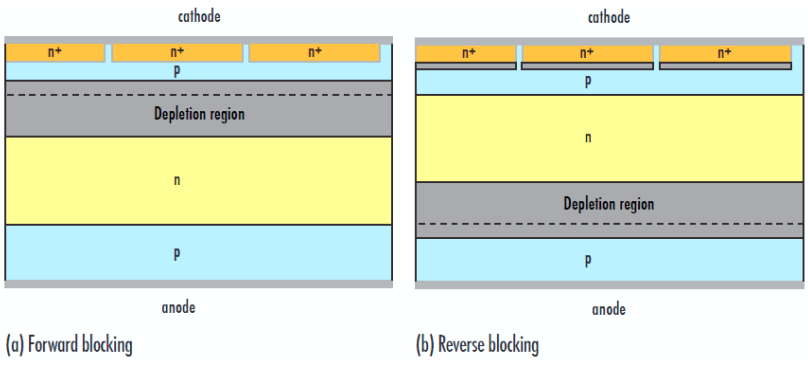


Figure 3-6: Depletion regions during forward blocking state (a) or reverse blocking state (b)

An ideal thyristor in the off-state does not carry any current at all, while blocking very high voltage, but a real thyristor does not achieve this ideal. During the off-state, there is always a small current that flows through the thyristor, which value depends on temperature and voltage. Moreover, different thyristors from the same production batch can have different off-state current values, presenting some challenges in the design of HVDC valves.

The three main effects that contribute to the total off-state current through a thyristor are listed below.

- Leakage current: it is present for any dv/dt, including the static case of a DC voltage, and it arises from charge carriers that are thermally excited. This effect follows an Arrhenius-type sensitivity to temperature, with current increasing exponentially with temperature and varying very little with voltage.
- Avalanche current: a thyristor subjected to off-state voltage experiences a high electric field in its depletion region, which causes charge carriers to be accelerated and to collide with atoms in the crystal structure, causing further generation of holes and electrons and creating a positive feedback "avalanche" mechanism. This causes rapid multiplication of current that can be damaging if energy is not limited. Unlike leakage current, avalanche current depends much more strongly on voltage than on temperature. In detail, it increases with voltage and, for a given voltage, it decreases with temperature.
- Displacement current: it depends on the dv/dt, since it arises from the junction capacitance "C" of an off-state thyristor. An applied dv/dt causes a current to flow in the thyristor, defined by:

$$i = C\frac{dv}{dt}$$

Displacement current is superimposed on top of leakage and avalanche currents that may already be present. If the sum of leakage, avalanche and displacement current exceeds a certain threshold, it becomes enough for self-triggering, which is usually a destructive event. Therefore, a dv/dt capability is defined for any thyristor.

Up to around 70% of the nominal voltage rating of the thyristor, leakage current is the dominant source and off-state current increases rapidly with temperature, while for voltages approaching the nominal rating, avalanche current becomes the dominant source. Fig. 3-7 shows the V-I characteristics of a real thyristor, pointing out when the off-state current is dominated by the leakage current and when the off-state current is dominated by the avalanche current.

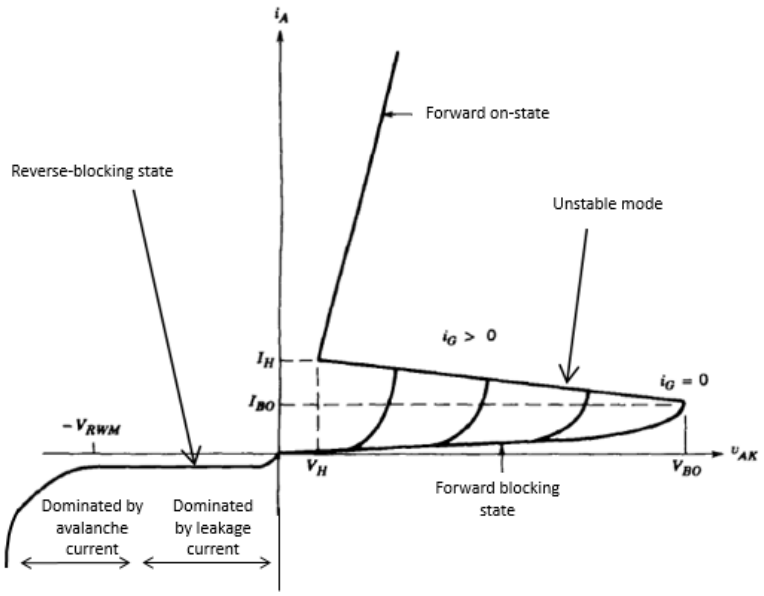


Figure 3-7: V-I Characteristic of a real thyristor [16]

When the off-state current flows in the reverse direction, the limiting factor is essentially thermal: power dissipation is voltage multiplied by current and, since voltage can be quite high, it does not require much current to result in high power dissipation. When the off-state current flows in the forward direction, the limit is generally reached at a lower voltage and occurs when current becomes high enough to cause spontaneous turn-on, which is usually a destructive event that must be avoided at all costs. For all these reasons, thyristors capable of withstanding very high dv/dt without self-triggering are needed and some form of dv/dt protection is needed as well.

Another issue to be considered is how voltage ratings change at high temperature. Values provided by manufacturers are usually valid between room temperature and 125°C. During some fault conditions, high temperatures are reached: leakage current,

that increases exponentially with temperature, becomes the dominant source of off-state current, and the voltage withstand capability starts to fall off very quickly. Generally, the forward voltage rating falls off at a lower temperature than the reverse voltage rating, as illustrated in Fig 3-8.

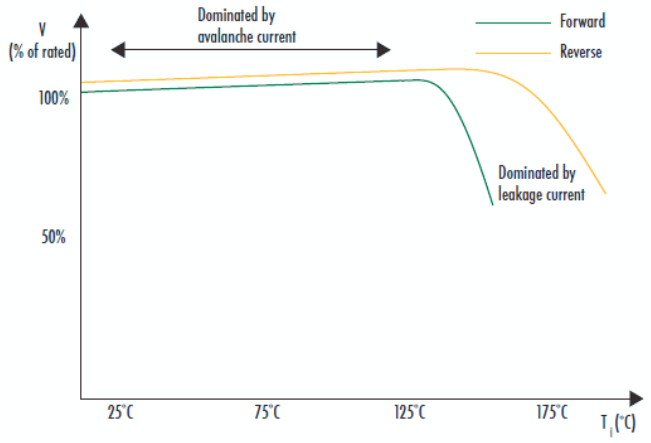


Figure 3-8: Forward and reverse voltage rating versus temperature

Concerning on-state properties, once it is fully turned on, a thyristor behaves as a very efficient switch, presenting an on-state voltage drop of a few volts. Such a voltage drop is very important because it gives rise to most of the power losses, so-called conduction loss, and equal to current multiplied by voltage. The on-state voltage is not constant but increases with current and depends on temperature. The simplest approximation of the voltage variation with current is a “straight-line approximation”, i.e. a fixed voltage threshold and a slope resistance. The threshold varies little between different thyristors and is generally about 1.2 V, while the slope resistance is a function of the silicon thickness and area. As the temperature increases, the threshold voltage tends to reduce, and the slope resistance increases. Typically, at the rated current at which a power thyristor operates, the on-state voltage drop is relatively insensitive to temperature, so temperature effects can be generally neglected.

3.2. Switching Characteristics and Limitations

Once static properties of a thyristor are examined, it is fundamental to investigate also dynamic characteristics, i.e. properties and limitations of turn-on and turn-off transitions. In the following discussion it is assumed that a large area high voltage device (e.g. 125 mm, 8.5 kV) is being considered.

Concerning turn-on properties, a thyristor is turned on by passing a short pulse of current of a few amps into the gate terminal for a few microseconds, when it is forward biased, causing a positive feedback mechanism and the "latch" into the conducting state.

The turn-on phase is the most dangerous for a HVDC thyristor because, initially, a current of several thousand amps starts to be conducted within just a few microseconds through a tiny area of the silicon, close to the gate terminal, while it takes much longer for the whole conducting area of the silicon to spread and cover the full area available. The whole process can be examined splitting it in two parts: the initial phase and the "spreading" phase.

The initial phase generally takes around 1 μs from the appearance of the gate current to the conduction of a significant amount of current, while the complete turn-on process takes about 1 ms. For a few hundred nanoseconds, the anode-cathode current is not large enough to have any appreciable effect on the external circuit, but after a turn-on delay time of typically 500 ns, the turn-on process finally starts to have a tangible effect and voltage across the thyristor falls during the following 100-200 ns, as shown in Fig. 3-9.

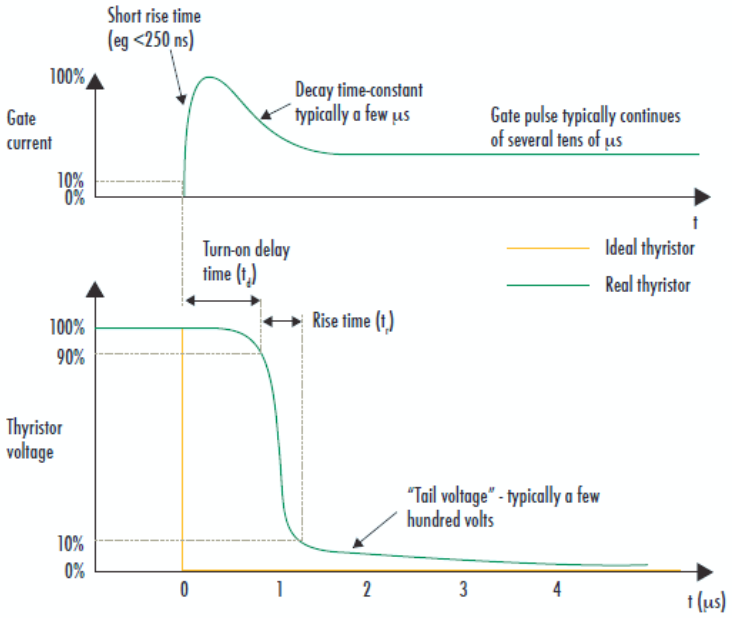


Figure 3-9: Initial turn-on process

Once the anode-cathode voltage starts to fall, current in the thyristor rises very quickly and the most dangerous situation for the thyristor begins. To ensure that the rate of rise of current is not excessive, it is necessary to include a di/dt saturable inductor (addressed also as limiting reactor), in series with the thyristor. During the first few microseconds after turn-on, the load current in the thyristor is negligible and current mainly arises from three sources:

- External stray capacitances of the converter transformer windings and bushings
- Damping capacitor (see Chap. 4)
- Any undamped capacitances

The first one is limited by the di/dt saturable inductor, the second one by the damping resistor (see Chap. 4) and the third one by the turn-on speed of the thyristor itself. Undamped capacitances obviously need to be kept to a minimum.

Considering all the factors, the total current that flows in the thyristor in the first few microseconds after turn-on looks like the one in Fig. 3-10.

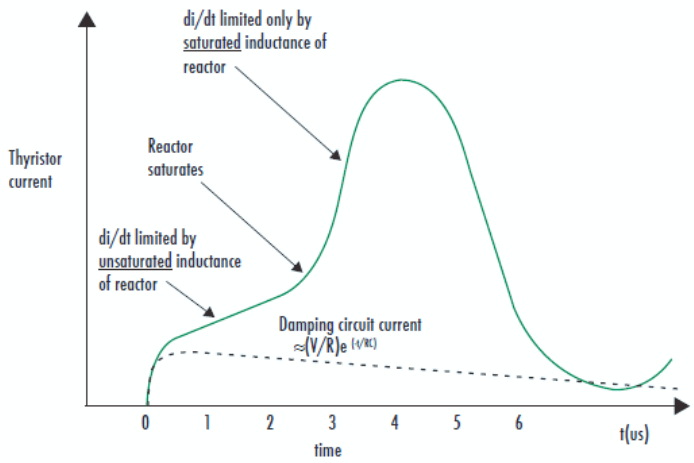


Figure 3-10: Total thyristor inrush current in the first few microseconds after turn-on

Typically, for turn-on from the full rated voltage of the thyristor, it takes 3-5 µs for the saturable inductor to saturate. During the unsaturated phase, current only rises by a few hundred amps per microsecond but, after saturation, the rate of rise of current is much greater. For a typical repetitive condition, the reached current peak might be around 1000-1500 A, at 6-8 µs after turn-on, concentrated in a tiny area of the silicon and, therefore, with the device under great stress. Subsequently, the conducting area starts to spread, at a speed of the order of tens of meter/second, addressed as spreading velocity, which depends on the current density in the turned-on area. It can take more than a millisecond for the conducting area to cover the whole silicon: during this time, a smaller conduction area means a higher on-state voltage, than it would normally be for a fully turned-on thyristor. This gives rise to spreading losses, additional to conduction losses examined above, but not particularly important to the overall losses of a thyristor. Both conduction losses and spreading losses are summarized in Fig. 3-11.

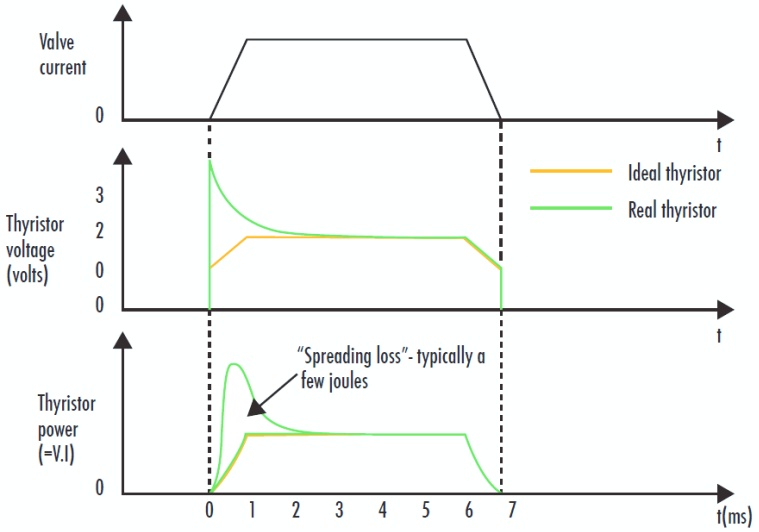


Figure 3-11: Conduction losses and spreading losses during the spreading phase of a thyristor

Concerning turn-off properties, an ideal thyristor should cease conduction exactly at the instant where current drops below the holding current and instantly recover its full ability to block voltages and dv/dt of either polarity. Real thyristors fall short of this ideal in two important respects:

- Conduction continues for a short period after current zero, resulting in a period of reverse current and "reverse recovered charge" Qrr
- After reverse current decays, the device remains vulnerable for some time to excessive positive voltage or dv/dt and hence has a defined turn-off time, tq, during which voltage must remain negative

As depicted in Fig. 3-12, the period of reverse current flow in the thyristor comprises two phases:

- Up to trr, current increases linearly in the negative direction at a typical rate of a few amps per microsecond (that depends on the total inductance of the commutating loop), reaching a peak value Irr
- After trr, current decreases (becomes less negative) following approximately an exponential relationship

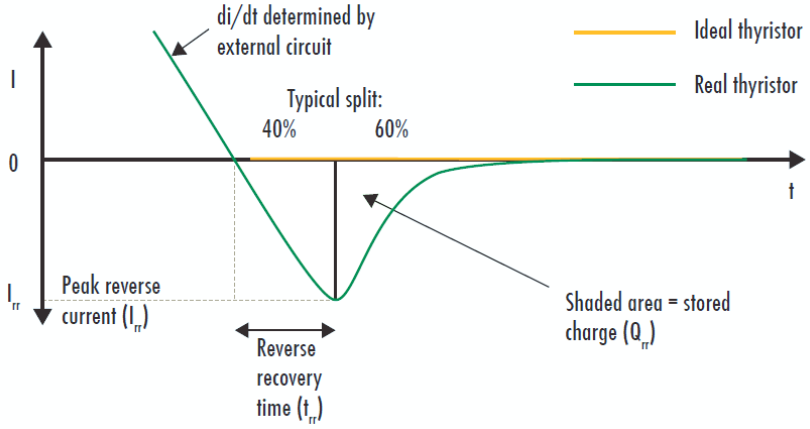


Figure 3-12: Thyristor reverse current at turn-off

The total area under the reverse current represents the stored charge Qrr of the thyristor. Typically, depending on the specific thyristor, about 40% of Qrr occurs before the peak of reverse current and 60% after it. Qrr and Irr are very important parameters to be considered for both modelling and valve design, for two main reasons:

- Irr determines the voltage commutation overshoot that occurs after the device turns off
- The spread tolerance of Qrr, referred to as ΔQrr, amongst different thyristors has a strong adverse effect on voltage sharing after turn-off that can persist until thyristors are next to be turned on again

An ideal thyristor withstands any positive voltage with any dv/dt immediately after turn-off, but a real thyristor cannot do this as it needs a recovery period of some hundreds of microseconds, i.e. the turn-off time tq mentioned above. During this time interval, voltage has to stay negative, before it is safe to apply any positive voltage and, subsequently, a further time interval needs to elapse before the thyristor is safely capable of withstanding high dv/dt.

If voltage becomes positive too soon or has too high dv/dt after the thyristor turns off, the device spontaneously turns itself back on again, in a process known as forward recovery failure, that can destroy the thyristor, unless self-triggering takes place at sufficiently low voltage or dv/dt. The most dangerous zone is where the thyristor struggles to withstand the re-applied voltage.

From a physical point of view, when voltage across the thyristor changes from negative to positive, any charge carrier in the silicon from previous conduction gives rise to a short pulse of forward recovery current. The more time elapses after turn-off, the more charge carriers recombine and, hence, the smaller forward recovery current becomes. Above a certain threshold, forward recovery current is high enough to cause spontaneous self-triggering via a similar regenerative process to that seen during normal turn-on, but without involving the gate terminal. At high dv/dt, the forward recovery current is superimposed on a displacement current flowing through the junction capacitance, hence making the device more sensitive. Similarly, at high temperatures the forward recovery current is superimposed on the leakage current. For these reasons, turn-off time increases with both dv/dt and temperature. Fig. 3-13 shows voltage and current for a thyristor when subjected to an event which causes voltage to become positive at various times after current zero. For the blue, green and orange traces, voltage becomes positive after the turn-off time has elapsed and the thyristor safely withstands the re-applied voltage. For the red trace, voltage is re-applied within the turn-off time and the thyristor spontaneously re-conducts.

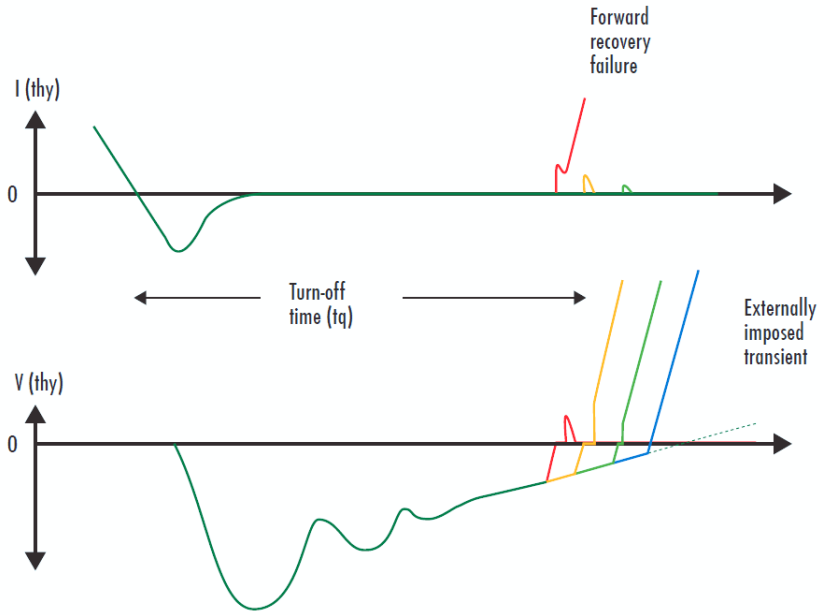


Figure 3-13:Voltage and current across a thyristor with re-applied forward voltage

Because forward recovery failure can destroy the thyristor, it is important to provide protection, turning the device on as a precautionary measure if voltage appears likely to become positive within the turn-off time.

3.3. Modelling for Electrical Circuit Simulation Environment

The main difficulty in designing models for bipolar power devices is in the distributed nature of the charge transport in the semiconductor, which is governed by the ambipolar diffusion equation (ADE) [18] [19]:

$$D\frac{\partial^2 p}{\partial x^2} = \frac{p}{\tau} + \frac{\partial p}{\partial t}$$

Where *p(x,t)* is the carrier concentration (holes or electrons in nearly equal concentration), *D* is the ambipolar diffusion constant and τ the carrier lifetime.

Before choosing the best model for the specific application, different models need to be compared and the final choice results from a compromise between convenience, accuracy and numerical efficiency in implementing physical effects.

Fundamental aspects that distinguish different power device models are model formulation technique and concept employed. Very broadly, all models can be classified either as macromodels, or as micromodels, as shown in Fig. 3-14.

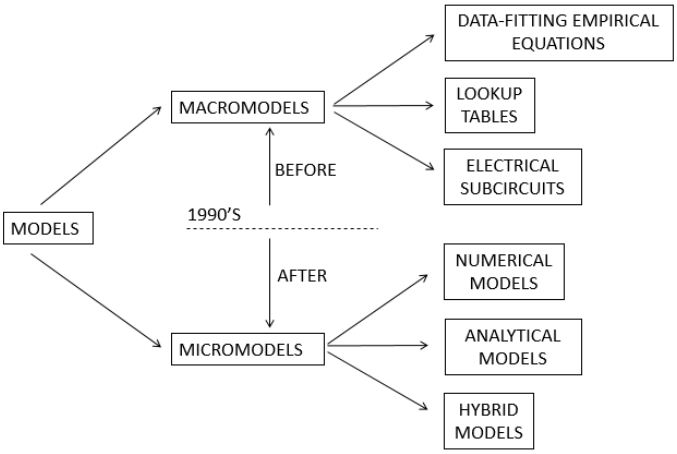


Figure 3-14: Models Classification

Macromodels reproduce the external behaviour of the device by using empirical techniques, without considering its geometrical nature and its internal physical

processes. This external behaviour is usually modelled by means of simple data-fitting empirical equations, lookup tables or electrical subcircuits of common components to emulate known experimental data. Because of the latter reason, macromodels are often labelled as subcircuit models, but many so called subcircuit models are actually micromodels, because they use subcircuits to simulate fairly complex physics-based mathematical equations. The main disadvantages of macromodels are limitations in terms of flexibility and accuracy.

Micromodels are closely based on the internal device physics and, if properly formulated, should yield good accuracy over a wide range of operating conditions. Because device physics unavoidably require mathematical equations, micromodels are also known as mathematical models and they are generally classified as numerical models, analytical models and hybrid models. Compared to macromodels, they are more computationally efficient, more accurate and more related to the device structure and to the fabrication process. For these reasons, most of the models proposed from the 1990's are micromodels, therefore an accurate description of micromodels is reported below.

Numerical models are based on numerical solutions of the partial differential equation set of semiconductor physics, that has no closed mathematical solution. Physical phenomena involved are carrier drift and diffusion components, carrier generation and recombination effects, and the relationship between space charge and electric field. Numerical solutions are obtained inserting a geometric mesh and solving equations step by step by, using either the finite-element or the finite-difference method, without simplifications. This sort of modelling provides a rigorous picture of the device behaviour but, owing to its numerical intensity, convergence properties and CPU times, it is limited to the analysis of simplified test circuits, that in practice involve only a single semiconductor. Although this may suffice during the device design and at technological development stages, such techniques are unable to cope with the simulation of realistic power circuits and are therefore of little use in their design, for which simplified models are employed. From an engineering point of view, the degree of accuracy achieved using an exact numerical model is not always necessary or even justified, especially if the input data, such as the doping profile, is known with a limited accuracy. In such cases, more compact models, obtained through some assumptions and simplifications in the semiconductor physics, are satisfactory.

Analytical models rely on a set of mathematical functions to describe the device's terminal characteristics without resorting to numerical methods. An example is the standard diode model in PSpice, designed for microelectronic devices, that is not suitable for simulating the dynamic and static behaviour of power devices, because it does not take into account conductivity modulation and charge storage in the low doped region. Both effects can be considered once the carrier concentration in the low doped region is determined, which is a function of time and position and its variation is determined by the ADE. An exact analytical solution of the ADE is not possible in the general case, but there are different approximated analytical approaches to solve it. The computational load of analytical models is far lower than those of numerical models and several simulators, such as PSpice and Saber, are available.

Hybrid models are a combination of numerical and analytical models and their origin is from the fact that certain physical phenomena in power devices are very difficult to simulate realistically using only analytical equations, especially charge storage effects in the low doped region. The basic idea of this method is to use a fast numerical algorithm that solves semiconductor equations in the low doped region only, while analytical equations are applied to the rest of the device structure. This procedure has the advantage that a high accuracy of the charge carrier behaviour can be simulated without the long execution time associated with fully numerical models.

For this research project a numerical model is not necessary, nor justified, so only the choice amongst hybrid and analytical models is of interest and a summary of the more relevant ones is listed below.

Some of the hybrid methods are proposed by Kraus [20] and Goebel [21]. As explained above, they are based on a hybrid algorithm that solves physical equations partly numerically and partly analytically. The basic idea is shown schematically in Fig. 3-15. In detail, a fast numerical algorithm, which is usually the finite element method or the finite difference method, solves the ADE and calculates the charge carrier distribution in the lightly doped region. The voltage across the low doped zone, that depends on the carrier distribution, is subsequently calculated with analytical equations.

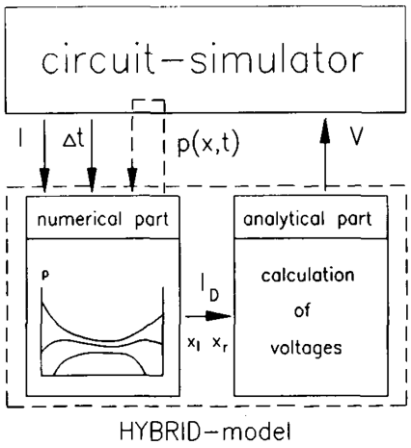


Figure 3-15: Principle of the hybrid method

Analytical models proposed by different authors are quite different from each other. A PSpice equivalent circuit representation for the base region, obtained by rational approximation of Laplace transform solution of the ADE, is proposed by Strollo [22] and is showed in Fig. 3-16.

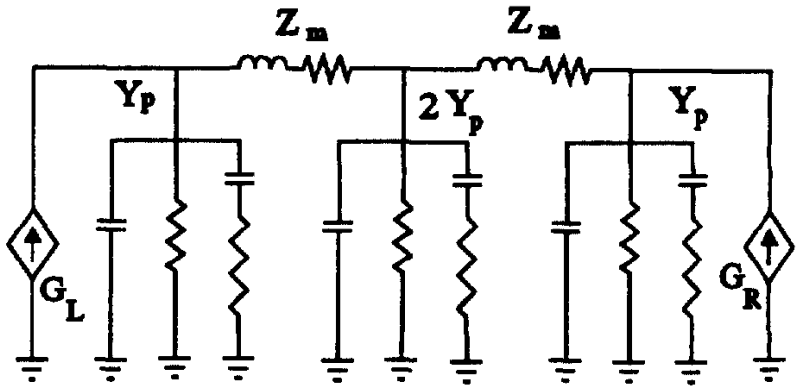


Figure 3-16: Network representation of the base region - Strollo

A Lumped-Charge modelling technique is proposed by Ma and Lauritzen [23] [24] and the base concept is represented in Fig. 3-17. A lumped charge model can be constructed if

- The device model is discretized into several critical regions, each of which contains one charge storage node and up to two connection nodes
- Hole and electron charge values at each node are obtained by multiplying the carrier concentration and its critical volume

- Charge nodes are linked using the following six equations from device physics and circuit theory: current density equations, current continuity equations, charge neutrality equations, Boltzmann's relation (P-N junction equation), Poisson's equations and the KCL and KVL laws.

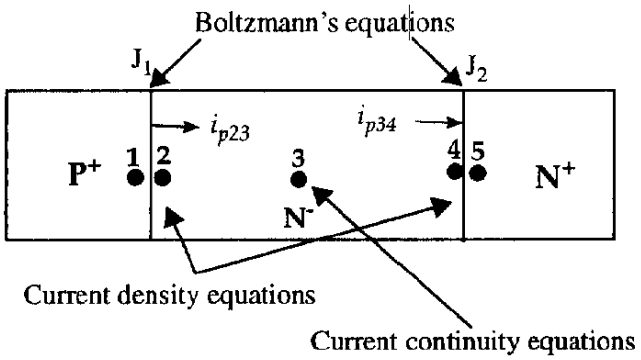


Figure 3-17: Lumped charge nodes and device equations for a one dimensional power diode structure – Ma and Lauritzen

A mathematical model based on conventional power diode equations plus a few more equations is proposed by Tseng [25]. In detail, equations of PN junction capacitance, dynamic stored charge in the mid-region, avalanche breakdown across the PN junction under influence of a high reverse voltage and mid-region conductivity modulation are added to the conventional equations and the network depicted in Fig. 3-18 results.

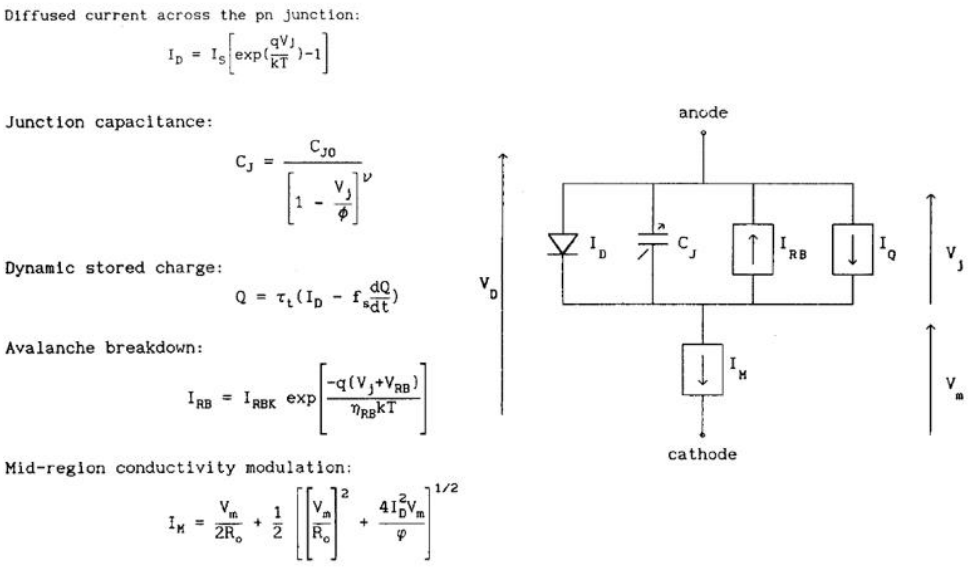


Figure 3-18: Network representation of power diode model - Tseng

A broad classification of micro-models available until the end of 1990's is summarized by Tseng [26] [27]

Furthermore, a model based on a Fourier solution of the ADE is developed by Leturcq [28]. The diffusion equation is converted into a system of an infinite number of first order linear differential equations, which is further represented in terms of circuit elements in the form of equivalent RC lines, as shown in Fig. 3-19, where voltages across the successive cells represent the Fourier series coefficients.

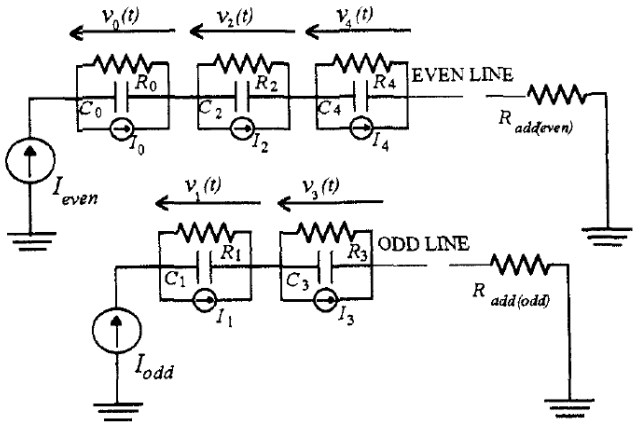


Figure 3-19: RC-line representation of the generic solution of the diffusion equation - Leturcq

Equations are handled by a computational block in the form of the one represented in Fig. 3-20, beside the carrier concentration profile in the carrier storage region.

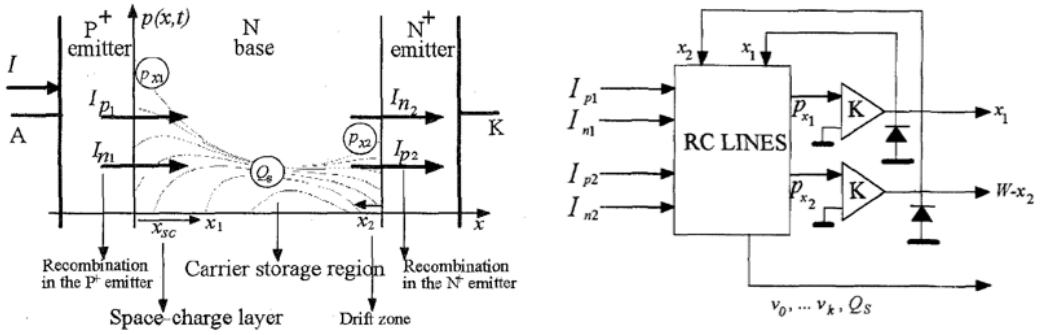


Figure 3-20: Carrier concentration profile and block-diagram for the analogue solution of the ambipolar diffusion equation with fixed or mobile boundaries - Leturcq

A power diode model based on the Fourier solution of the ADE is also presented by the same author [29], plus model for other bipolar power devices [30], [31]. The concept developed by Leturcq is based on a regional approach to modelling, defining a unified range of circuit-oriented models for power bipolar semiconductor switches and replacing the concept of «one device, one model» with an adaptable assembly of a small number of submodels, associated with clearly identified regions of the device structure.

A more recent model, suitable for the implementation in MATLAB and Simulink, is presented by Bryant [32] [33]. It is still based on a Fourier solution of the ADE and adaptable to different devices and an example of a block diagram is depicted in Fig. 3-21.

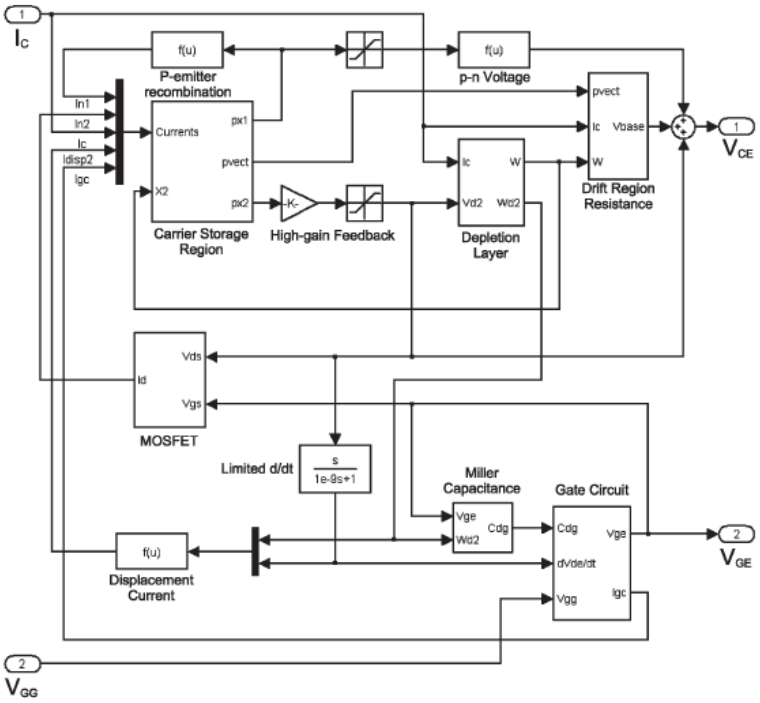


Figure 3-21: Fourier based Simulink model of an IGBT - Bryant

3.4. Model choice for the Specific Application

For this research project, it is not required to reproduce the physical behaviour of thyristors in an extremely detailed way. In particular, it is not needed to show the carrier concentration profile in the low doped region, so it is definitely not necessary to use a numerical model. Simulations need to investigate mainly the interaction between the thyristor and the external electrical circuit. Therefore, the chosen model is the PLECS "Dynamic thyristor (SCR) model with reverse recovery", originally developed by Courtay [34] in MAST, the Saber simulator modelling language. Such a model uses directly available data-sheet parameters and automatically converts them into the physical constants needed in model equations, with a procedure called "automatic parameter extraction", in order to include internal effects, such as forward and reverse recovery. In first place, a diode model is realised with an on-resistance Ron in series with an ideal diode, that represents the junction voltage by an exponential law. The thyristor model is derived from the diode model, by replacing the on-resistance with a module that realizes the thyristor static properties. This module is basically a binary resistance Ron/Roff controlled by a digital gate. When the thyristor is in the off-state under positive voltage, Roff blocks the current that would flow through the diode. In the on-state, Ron is the on-resistance as in the diode model. The transition Roff to Ron occurs when Vak is positive and the gate active, or if Vak exceeds the breakover voltage Vbo: ON or OFF state are determined by the conduction state of the internal switch. The turn-on time tf is the parameter to be adjusted in order to reproduce accurately turn-on transients and switching losses. The thyristor remains in the on-state until it gets reverse biased for a time interval long enough to have most of its excess charge removed from the light-doped region. The parameter tq is the minimum time interval for which Vak must be maintained negative to guarantee thyristor turn-off.

Table 1 contains a summary of input parameters and the associated thyristor model is represented in Fig. 3-22.

Features	Parameters
I-V Characteristics	Ron, Von, Is, init_state
Reverse Recovery	Ifo, dIr/dt, Irrm, trr, Qrr
Junction Capacitance	C
Turn-on Transient	tf
Critical Turn-on	tq, Vbo

Table 1: Input parameters for the thyristor model

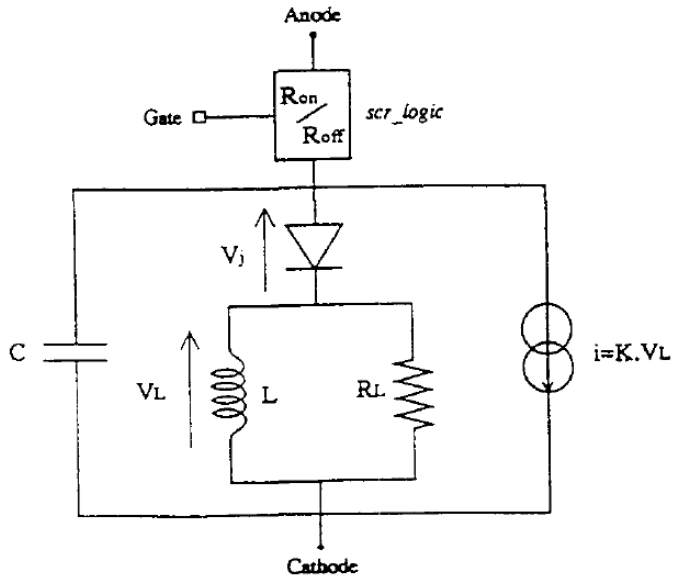


Figure 3-22: Thyristor model - Courtay

Current turn-off waveform, including reverse recovery effect, is depicted in Fig. 3-23.

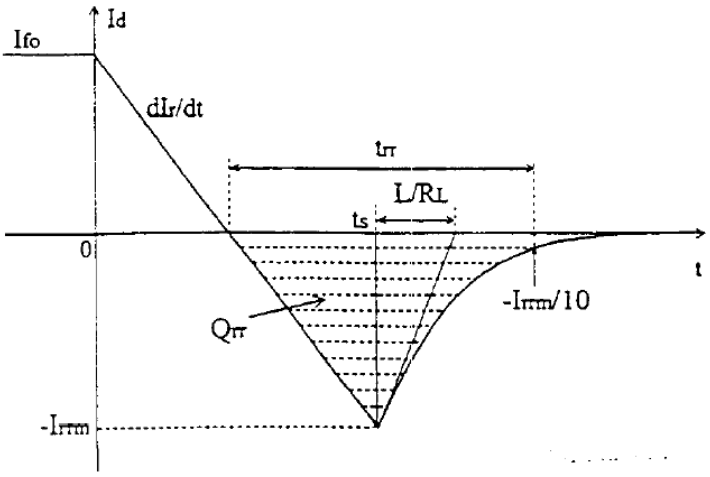


Figure 3-23: Thyristor current turn-off waveform

The description provided in PLECS for the mentioned model is: «This component is a behavioural model of a thyristor which reproduces the effect of reverse recovery. The effect can be observed when a forward biased thyristor is rapidly turned off. It takes some time until the excess charge stored in the thyristor during conduction is removed. During this time the thyristor represents a short circuit instead of an open circuit, and a negative current can flow through the thyristor. The thyristor finally turns off when the charge is swept out by the reverse current and lost by internal recombination. The same effect is modelled in the Diode with Reverse Recovery and described there in detail».

Two notes are provided for the user in the "help" tab:

- Due to the small time-constant introduced by the turn-off transient a stiff solver is recommended for this device model,
- If multiple thyristors are connected in series the off-resistance may not be infinite (which means not to set "inf" in the Roff box).

The window to let the user include model parameters is the one illustrated in Fig. 3-24.

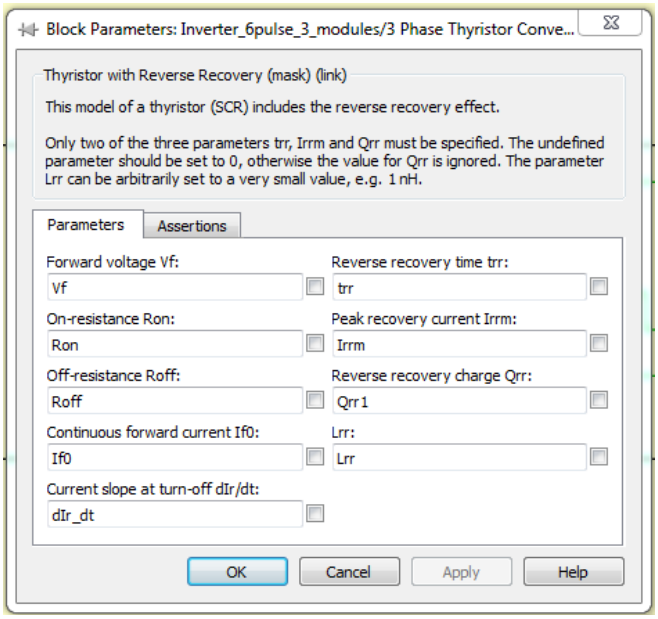


Figure 3-24: Mask of the thyristor with reverse recovery component in PLECS

Input parameters required to run the model are, in detail:

- Forward voltage “Vf” (voltage between anode and cathode when the thyristor is conducting)
- On-resistance “Ron” (resistance of the conducting device)
- Off-resistance “Roff” (resistance of the blocking device)
- Continuous forward current “If0” (under test conditions)
- Current slope at turn-off “dIr/dt” (under test conditions)
- Reverse recovery time “trr” (turn-off time under test conditions)
- Peak recovery current “Irrm” (absolute peak value of the reverse current under test conditions)
- Reverse recovery charge “Qrr” (under test conditions)
- Lrr (inductance that acts as a probe measuring the di/dt)

Only two of the three parameters trr, Irrm and Qrr must be specified. The undefined parameter must be set to 0, otherwise the value for Qrr is ignored. The parameter Lrr can be arbitrarily set to a very small value, e.g. 1nH. Probe Signals are thyristor voltage, thyristor current and thyristor conductivity. The latter is the conduction state of the internal switch, which is 0 when the thyristor is blocking, and 1 when it is conducting.

The ultimate PLECS model is depicted in Fig. 3-25.

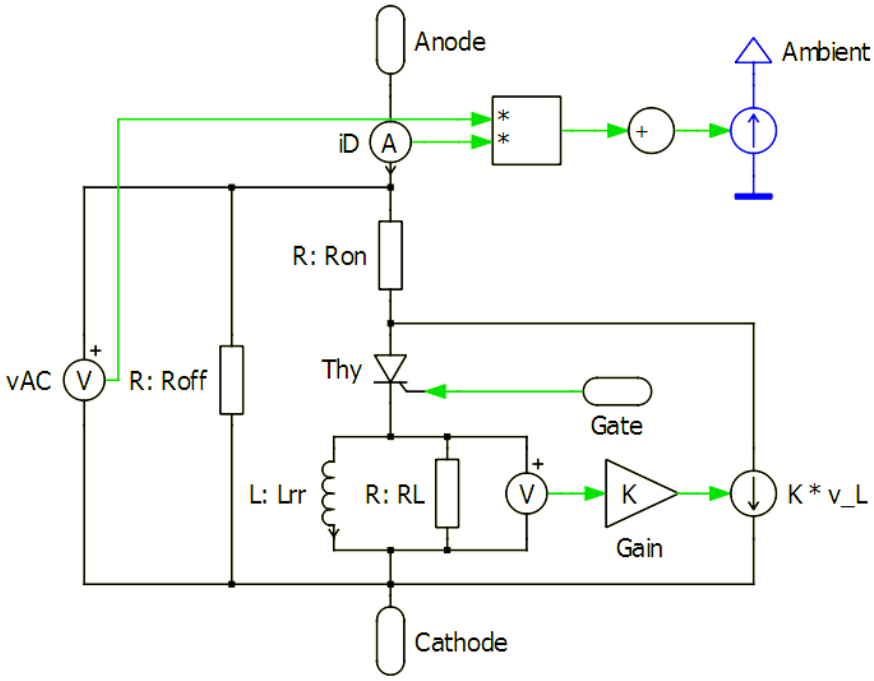


Figure 3-25: Model of the thyristor with reverse recovery - PLECS

3.5. Sample Simulation and Effect Representation

Once the power thyristor model is chosen, a sample simulation is conducted for the Dynex DCR 3030V42. Current and voltage ratings are 3 kA and 4 kV respectively and model parameters are listed in Table 2 (see Appendix B for the data sheet). The 6-pulse inverter in Fig. 3-26 is considered and voltage and current waveforms of one of the six thyristors are illustrated in Fig. 3-27. Damping branches are included, but the saturable inductor is not, because the external stray capacitance discharge is not considered at this stage (see details in Chap. 4). The DC grading resistor is not considered either, because only a single device is simulated, instead of a series.

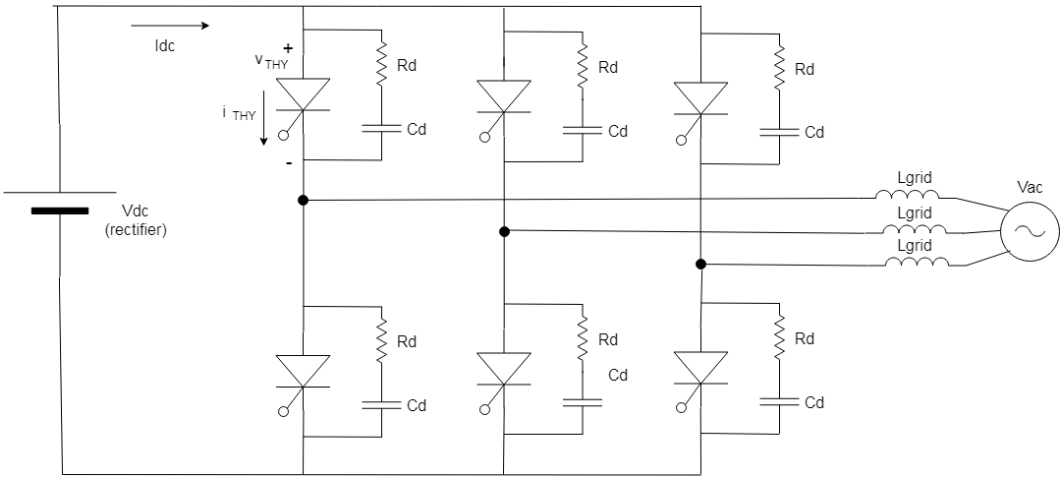


Figure 3-26: Electrical circuit of the 6-pulse inverter

Forward Voltage “Vf”	0.9 V
On- State Resistance “Ron”	0.3 mΩ
Off-State Resistance “Roff”	1 MΩ
Continuous forward current “If0”	3 kA
Current slope at turn-off “dIr/dt”	200 MA/s
Reverse recovery time “trr”	400 µs
Peak recovery current “Irrm”	0 A
Reverse recovery charge “Qrr”	37.5 mC
Lrr “Lrr”	1 nH

Table 2: Thyristor parameters for the sample simulation

Turn-on and turn-off details are show in Fig. 3-28 and Fig. 3-29 respectively.

Details of the reverse recovery effect are depicted in Fig. 3-30. Reverse voltage clearly starts to become established (to become negative) after the reverse current peak.

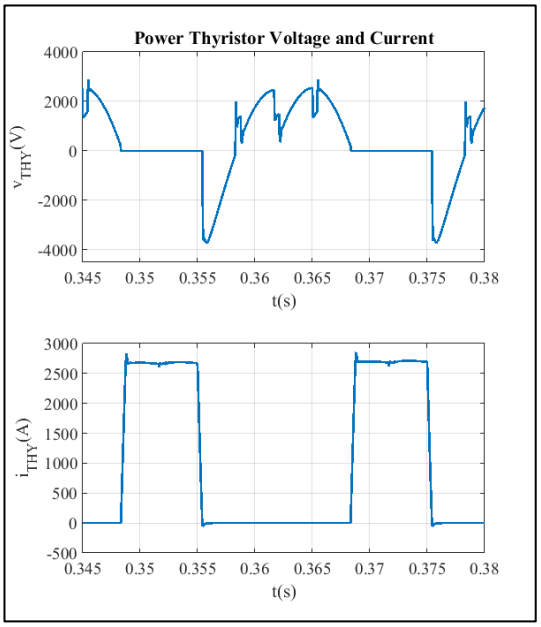


Figure 3-27: Power thyristor voltage and current waveforms; 6-pulse inverter

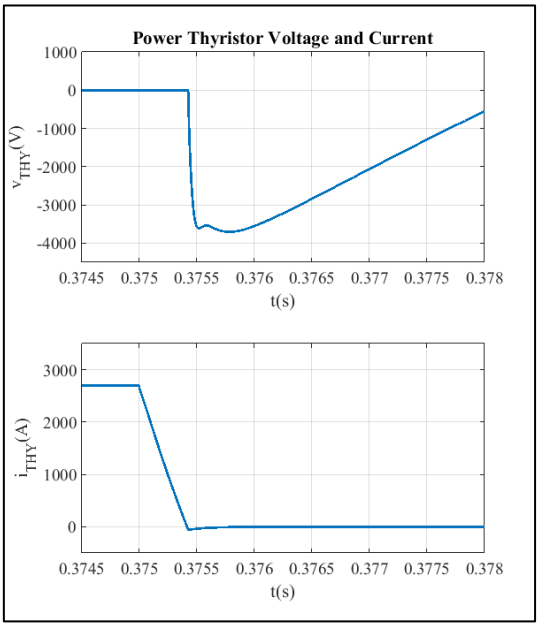


Figure 3-29: Power thyristor turn-off; 6-pulse inverter

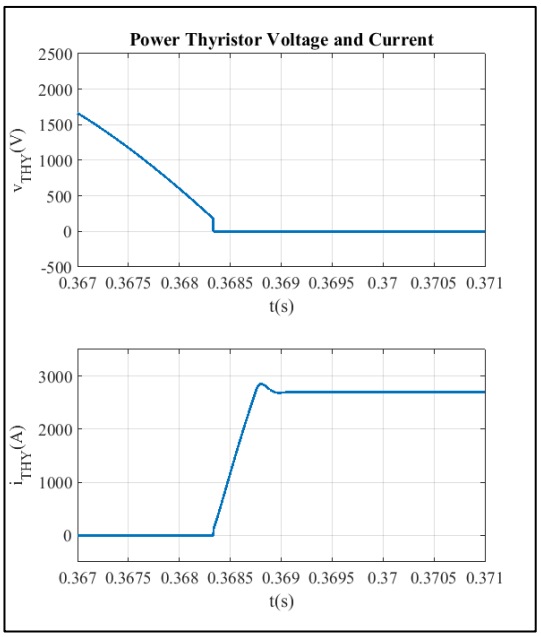


Figure 3-28: Power thyristor turn-on; 6-pulse inverter

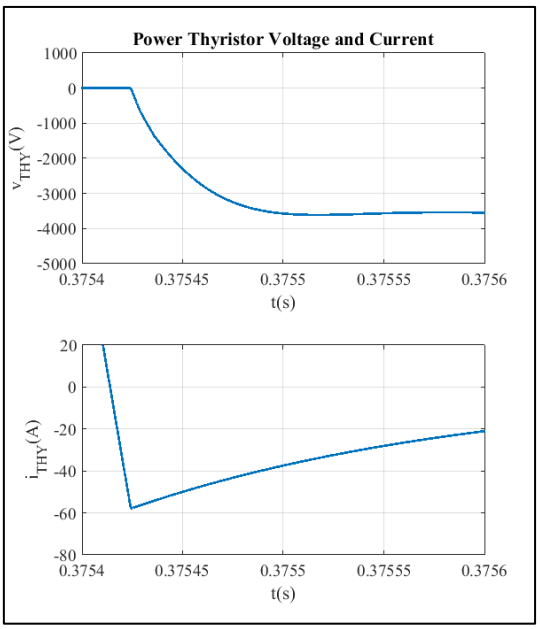


Figure 3-30: Power thyristor reverse recovery; 6-pulse inverter.

3.6. Summary

In this chapter, the basic structure of a power thyristor and the static V-I characteristic are illustrated. Switching transitions are investigated, with particular attention to dv/dt and di/dt limitations. Different models for electrical circuit simulation environment are classified and the most appropriate one for this research project is chosen, providing a sample simulation that represents the effects of interest.

The chosen model is the “Dynamic thyristor (SCR) model with reverse recovery” available in PLECS, which is analytical and addressed as behavioural, because equations are inserted in an electrical sub-circuit, ready to be used in the simulation circuit. From the sample simulation results, forward and reverse recovery are reproduced satisfactorily.

In the next chapter, the thyristor valve converter is presented, providing a detail description of the auxiliary passive components needed to operate a thyristor series safely. Afterwards, the ideas behind the auxiliary active circuits employment and the conditions to be respected to replace passive branches with active ones are explained.

4. Thyristor Valve Converters

Thyristor valves are amongst the most important items of equipment in a HVDC converter station. Typically, they are second only to the transformer in terms of cost.

A thyristor valve is essentially a switch that exhibits unidirectional, diode-like, conduction when turned on by the control system, and that is turned off when the external circuit forces the current to zero, which happens naturally each cycle in line-commutated HVDC installations.

The term "valve" is a throwback to the earlier days of HVDC, when mercury arc valves were used for this function. They operated in a totally different way (being essentially vacuum tubes, hence the name "valve") but did essentially the same job.

When thyristors were introduced, the name valve was retained. A thyristor valve can be eventually defined as «an assembly of series/parallel thyristors that behaves like a single, very large thyristor».

Thyristor valves typically need to be able to withstand hundreds of kilovolts in their off-state. Since thyristors from which they are constructed are only capable of withstanding a few kV each, thyristor valves need to contain many thyristors in series. Ensuring that these series-connected thyristors share the applied voltage evenly is a significant challenge.

Many early designs of thyristor valve used parallel connections of thyristors to increase the effective current rating. However, using the very large thyristors now available, with diameters of up to 150 mm, this is no longer necessary.

In general, the correct design of a thyristor valve is a complex, multi-disciplinary process involving a range of engineering disciplines including power engineering, power electronics, analogue electronics, semiconductor physics, high-voltage corona, materials science, heat transfer, fluid mechanics, mechanical and structural engineering.

4.1. Thyristor Valve Structure

The smallest building block of a thyristor valve is the composition of a thyristor, a gate unit, an RC damping circuit, a DC grading resistor and a heat sink and is termed thyristor level. The electrical circuit of a thyristor level is shown in Fig. 4-1, in which “Cd” is the damping capacitance, “Rd” is the damping resistor and “Rdc” is the DC grading resistor. A valve section is the series of several thyristor levels, typically between five and fifteen, and a single di/dt limiting reactor. A series of valve sections, the number of which depends on the voltage of the application, realizes a complete valve (Fig. 4-2).

The gate unit issues the turn-on current pulse to the gate terminal of the thyristor when instructed to do so by the control system. The RC damping circuit controls the magnitude of the blocking voltage overshoot and, together with the DC grading circuit, it ensures uniform voltage distribution between series-connected thyristor levels. These two grading circuits cover different areas of the frequency domain: the damping circuit covers frequencies from fundamental, 50 Hz or 60 Hz, up to a few kHz, and the DC grading circuit deals with 0 Hz.

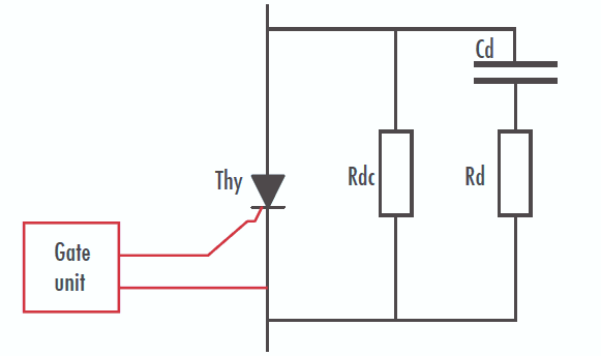


Figure 4-1: Thyristor Level

An additional component is needed to complete the thyristor valve section: a di/dt limiting reactor to control stresses on the thyristor during the early stages of conduction. The type based on lumped di/dt reactors is considered, in which the di/dt reactor is not unique to each thyristor level but shared between several thyristor levels.

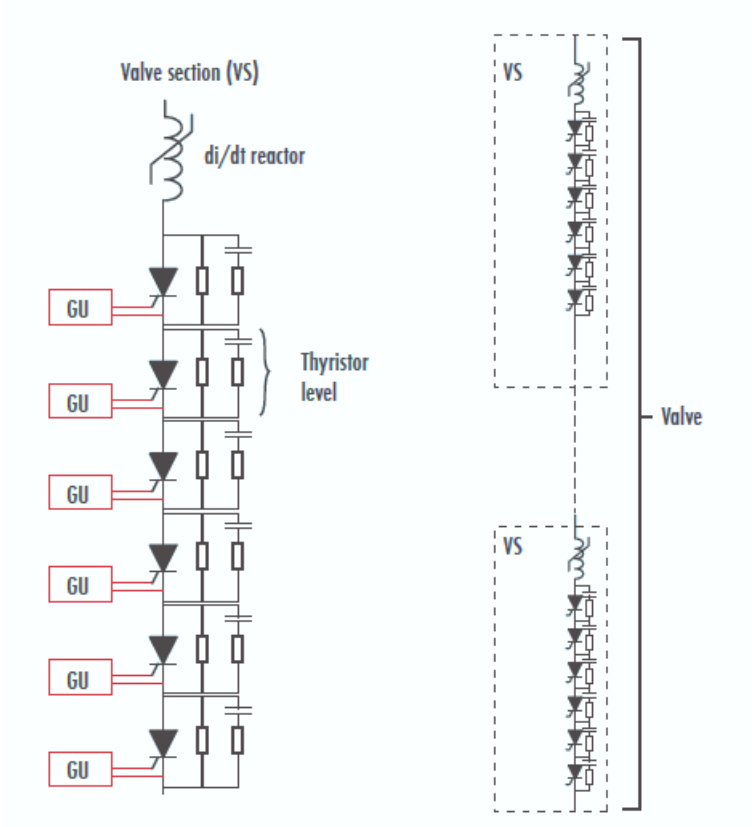


Figure 4-2: Thyristor Valve Section (left) and Thyristor Valve (right)

Voltage distribution amongst thyristor levels during the off-state is an important issue, which has not a straightforward solution. With perfect voltage distribution, the number of thyristors required in a valve could be calculated dividing the voltage rating required for the valve by the voltage rating of each thyristor but, voltage distribution in a valve is never perfect and unbalanced voltage distribution needs to be considered in the design. As a consequence, a valve always needs more thyristors in series than would be predicted by the simple division mentioned above. Since there is a clear economic incentive to use as few thyristors as possible, one of the main objectives of valve design is to make voltage distribution as good as reasonably possible, without incurring excessive costs for other components.

The main mechanism for achieving good voltage distribution is to fit voltage grading circuits, which aim to provide a well-controlled parallel impedance across each thyristor level, so that voltage distribution is as good as it reasonably can be at all relevant frequency ranges. The most important grading circuit is the Rd-Cd combination, often referred to as the “snubber” circuit by analogy with the RC circuit

used on some other lower-power converters, but better described by the term “damping” because of its role in attenuating oscillatory voltage overshoot that occurs during turn-off. The damping circuit is very effective at controlling voltage distribution at fundamental frequency and for moderately fast impulse waveforms, but it becomes less effective at very high frequencies (MHz) and is completely ineffective at zero frequency (DC). To deal with these frequency regimes, all thyristor valves include a plain resistive DC grading resistor and many designs also include some form of plain capacitive fast grading capacitor.

The valve is connected to the AC system via series inductance, mainly arising from the leakage inductance of the converter transformer. During the on-state, the load current flows through this series inductance and the thyristor. The thyristor provides a very low impedance path, which almost completely prevents any voltage from appearing across the damping circuit. However, at turn-off, the thyristor ceases to conduct current shortly after current zero, and at this time the damping circuit becomes connected in series with the external inductance of the converter, forming a series LC circuit.

Any LC circuit subjected to a step-change of voltage tends to oscillate. In a HVDC valve, this oscillation results in a peak voltage across thyristor valves, much higher than the instantaneous value at fundamental frequency voltage, as supplied by the converter transformer. The commutation overshoot is exacerbated by the presence of reverse recovery charge (Qrr). With an ideal thyristor (Qrr = 0) it would be possible to choose damping circuit components to give nearly critical damping and achieve an overshoot of 10% or less but, with real ones, overshoots of 50% or more are common. Unless the commutation overshoot can be damped sufficiently, the number of thyristor levels in the valve need to be increased. Therefore, it is essential that the damping circuit provides enough damping during the turn-off voltage transient (Fig. 4-3).

Reverse recovery charge differences (ΔQrr) amongst different thyristors in the valve, have an adverse effect on voltage sharing after turn-off. If two thyristors connected in series have different values of Qrr, the thyristor with lower Qrr initially sees a higher negative voltage than the other thyristor, but a lower positive voltage after the voltage changes polarity (Fig. 4-4). The voltage offset error amongst thyristors is equal to $\Delta V = \Delta Qrr/Cd$.

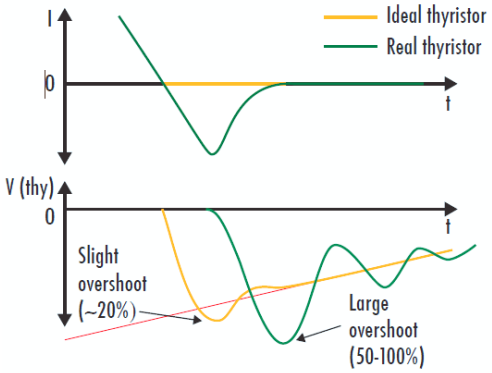


Figure 4-3: Turn-off transient showing effect of thyristor stored charge

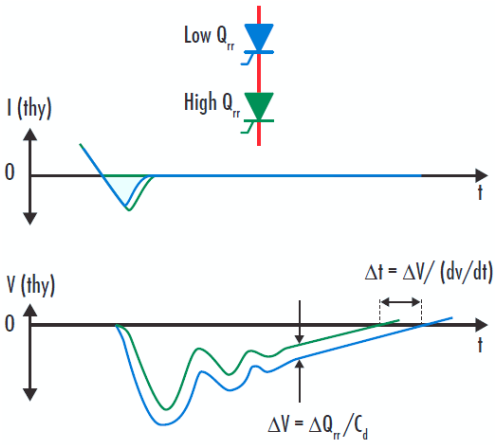


Figure 4-4: Effect of variations of stored charge on voltage sharing

Some consideration about the design of each auxiliary component are listed below.

- damping capacitor design

The main role of the damping capacitor is to enforce uniform voltage sharing. With typical component values of 1.0 – 1.5 µF for Cd and 40 – 60 Ω for Rd, the damping circuit is overwhelmingly capacitive at fundamental frequency, and the effect of the resistor becomes significant at frequencies of several kHz.

The capacitance value is chosen on an economic basis. Larger values of capacitance result in better suppression of the recovery overshoot transient and better limitation of voltage imbalances, caused by variations of stored charge amongst thyristors. Nevertheless, power losses of the damping circuit increase more than proportionally with capacitance, with two effects: increase of capitalized losses of the station and need of a damping resistor rated for higher power dissipation. These two effects, which can each be of comparable importance, provide a powerful motivation to use the smallest possible capacitance that does not result in excessive recovery overshoot. With 8.5 kV, 125 mm thyristors, according to Alstom Grid/GE Grid Solutions experience, the economical optimum value of the damping capacitor is generally in the range 1.0 – 1.5 µF per level.

- damping resistor design

The damping resistor performs two main functions:

- Damping of the turn-off voltage overshoot
- Limitation of the step current at turn-on

Concerning the first function, if commutating inductance and damping capacitance are known, it is straightforward to calculate the damping resistance needed to give critical damping. But, in practice, the stray capacitance of the transformer cannot be damped, and the stored charge causes the voltage overshoot to be much larger than in a conventional critically damped system. It is therefore necessary to perform quite detailed simulations, including accurate models of the turn-off behavior, in order to achieve damping resistor optimum choice.

Regarding the second function, when the thyristor turns on, the damping capacitor is pre-charged to approximately the same voltage of the thyristor. In the absence of a damping resistor, this capacitor would discharge extremely quickly (< 1µs) into the thyristor, giving a very short and extremely large current pulse, which would destroy the thyristor. Therefore, the damping resistor has to provide enough series resistance in the circuit to limit this discharge current to a safe value. On the other hand, resistance has not to be too large, to not incur in excessive dv/dt experienced by the thyristor under certain abnormal operating conditions.

Taking these requirements into account, according to Alstom Grid/GE Grid Solutions experience, the optimum value of damping resistor for a 125 mm, 8.5 kV thyristor is typically 40-60 Ω.

- DC grading resistor design

The fact that the damping circuit contains a capacitor, makes it completely ineffective for any condition when the valve is subjected to a DC voltage. To deal with voltage grading under these conditions, a resistive circuit is needed. This is normally provided by fitting a resistor across each thyristor. There are two principal effects which can lead to voltage imbalance under DC conditions that need to be corrected by the DC grading resistor:

- Tolerances of the off-state and reverse leakage current amongst series-connected thyristors
- DC grading errors resulting from the cooling pipework within the valve

In a water-cooled valve, water resistance inside coolant pipes has an important effect on voltage sharing under DC conditions. With a good design, it is possible to size coolant pipes to give equal resistances across each valve module but, this is not what is usually required. What the valve needs is equal resistance across each thyristor level. When all modules contain the same number of thyristors, this occurs naturally, but there are several reasons why different modules that make up a valve may have unequal numbers of thyristors.

The main function of the DC grading resistor is to correct these effects and ensure that the resulting voltage distribution under DC conditions is adequate to prevent any individual thyristor experiencing a voltage exceeding its DC voltage rating.

A secondary function of the DC grading resistor can be to act as the top end of a voltage divider, so that the Gate Unit can measure voltage across thyristors for control and protection purposes.

The choice of the resistor value is an economic compromise between a high value, which generates little losses, and a low value, which is more effective at controlling voltage distribution and hence permits fewer thyristor levels for a given application. Modern HVDC valves typically use values of the order of 100 kΩ per level.

- Saturable inductor design

Thyristors are very vulnerable in the first few µs after turn-on and require the rate of rise of current to be limited to a few hundred amps per µs. This is accomplished by connecting a di/dt limiting inductor in series.

In order not to increase the reactive power consumption of the converter, it is undesirable (and too expensive) to use a linear inductor, so the magnetic material is deliberately allowed to saturate each cycle. Hence, the inductor is frequently called “saturable”. This component also plays a useful role in limiting the rate of rise of voltage (dv/dt) experienced by thyristors in the off-state, as a result of certain fault events.

The design of the saturable inductor is complex [35], because of compromises between its ability to limit di/dt in the very early stages of turn-on (which favour using low-loss magnetic material) and the need to provide damping of the turn-on transient (for which a certain, known mount of core loss is desirable). After the thyristor, the di/dt inductor is probably the most complex and important component in the valve, with characteristics that influence almost every other aspect of the valve design.

Therefore, the two main functions performed by the inductor are:

- Reduction of turn-on di/dt stresses (hence the name)
- Reduction of fast transient voltage stresses applied to the thyristor

Regarding the first function, although modern thyristors have an active silicon diameter of up to 150 mm, the complete thyristor does not turn on simultaneously. In the first few µs after turn-on, only a very small area, within a millimetre or so of the edge of the gate terminal, initially conducts. Therefore, if current rises too rapidly after turn-on, this localized area may overheat and the thyristor would be destroyed. For this reason, the rate of rise of current, di/dt, must be limited during these first few µs.

The main current source in this time interval is the stray capacitance of the converter transformer. If not limited by a di/dt inductor, the discharge of these stray capacitance would result in a theoretically infinite current in the thyristor, which would not be withstood.

The main function of the di/dt inductor is, therefore, to slow down the discharge of this stray capacitance, so that it occurs slowly enough (Fig. 4-5).

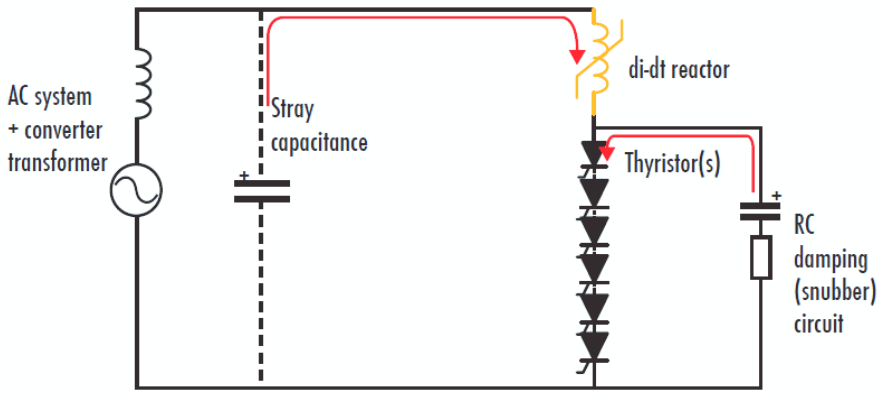


Figure 4-5: Discharge of external stray capacitance when valve turns on

In addition to limiting the rate of rise of initial current, and thereby peak current, the inductor must also provide damping to prevent thyristor current from becoming too oscillatory. In particular, it is vital to ensure that current in the thyristor does not drop below zero after turn-on, otherwise the thyristor could be destroyed (Fig. 4-6).

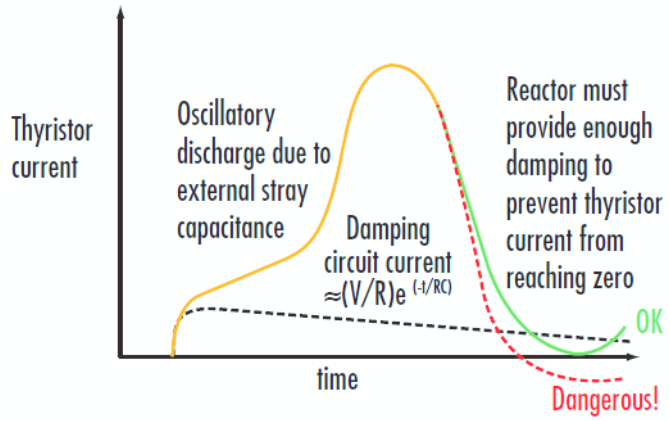


Figure 4-6: Effect of di/dt limiting inductor on valve current in first 10-20 µs

Concerning the second function, the saturable inductor is in series with thyristors and their associated damping circuits and the combination of inductor and damping circuits forms a low pass filter, which attenuates fast voltage transients, as shown in Fig. 4-7, reducing both the amplitude (peak) and the steepness (dv/dt) of the voltage experienced by thyristors. Obviously, this is only effective at low current values, where the inductor is not saturated.

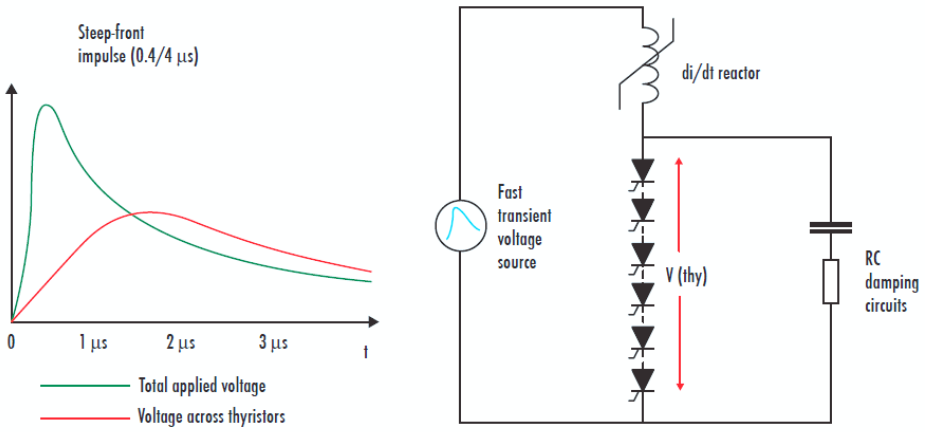


Figure 4-7: Beneficial effect of di/dt limiting inductor for suppressing dv/dt on thyristor

To fulfil its primary requirement of limiting di/dt at turn-on, the inductor needs to have a high inductance at low values of current (a few hundred amps). However, in order to avoid unnecessary increase of reactive power consumption of the converter, it is undesirable for this inductance to be present at normal load current. Hence, the di/dt inductor is nearly always of the saturable type, for which the magnetic material is deliberately allowed to saturate every time that the valve is turned on. This also allows the inductor to be much smaller than a linear one of the same unsaturated inductance.

The saturation current is normally a few hundred amps, which is high enough to deal with the initial inrush from stray capacitances when the valve turns on (and to act as a buffer for fast voltage transients). The transition from unsaturated to saturated must be progressive and not exhibit an abrupt “knee”, as this can result in excessively fast voltage collapse between the valve section terminals and consequent dv/dt induced in the other valve sections of the series stack. Conduction and hysteresis losses should be as low as possible, since this gives no benefit to the valve design. However, it may be advantageous for the core material to have some eddy current losses, since this is a quite effective method of providing damping of the turn-on current.

In Fig. 4-8 is represented the saturable inductor of the Alstom H400 valve, which is a multi-turn type and weighs about 250 kg.

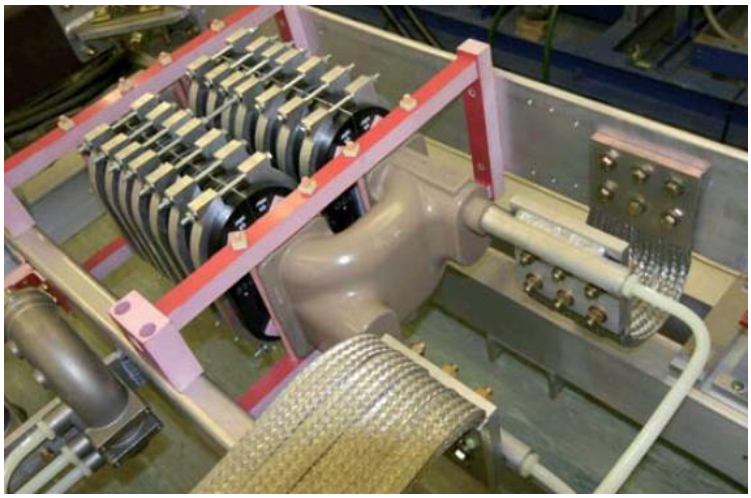


Figure 4-8: Multi-turn saturable inductor ALSTOM H400 HVDC valve

The complete Alstom H400 valve is shown in Fig. 4-9, which weight is about 1100 kg.

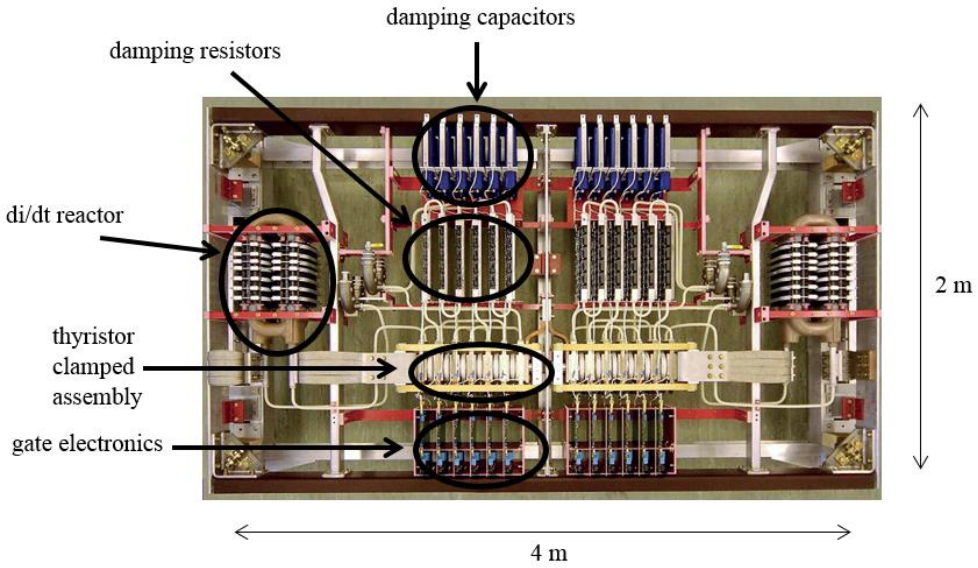


Figure 4-9: Complete ALSTOM H400 HVDC valve

4.2. Purpose of Auxiliary Active Circuits Employment

Auxiliary active circuits have two main purposes: replacement of the saturable reactor with a specific active branch for turn-on compensation and reduction of damping capacitors size through a properly controlled turn-off branch. In addition, power losses reduction with consequent cooling system size reduction. Detailed investigation of both active circuits is presented in chapters 5 and 7. Real scale simulations are issued in Chap. 5, while reduced scale simulations and experimental tests are presented in Chap. 7. The specific configuration chosen for the active circuits is targeted to investigate the Alstom Grid patents [3][4].

- Active Current Control

The stray capacitance of the external circuit causes a high rate of change of current in the main thyristor immediately after the switch on and a saturable reactor is typically adopted to protect the device. An alternative current path between terminals of the thyristor (Fig.4-10) permits a safe discharge of any current arising from external stray capacitances and either size reduction or elimination of the saturable inductor. For the realization of the alternative path, different configurations can be applied. One possibility is to employ a transistor in series with a limiting resistor. The transistor could be a silicon carbide device, with high voltage performance characteristic, high current pulse rating (a few kA) and modest average current ratings (a few amps).

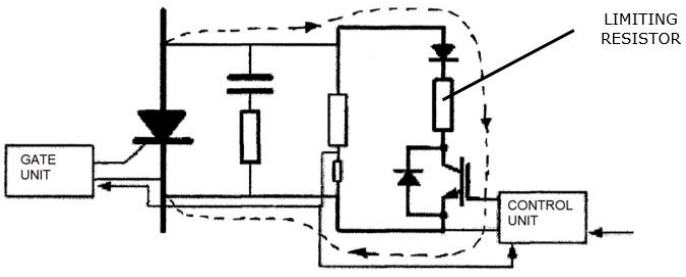


Figure 4-10: Turn-on active control circuit [3]

If the auxiliary transistor is switched on about 10 to 20 μs before the switch on of the main thyristor (Fig. 4-11), any stray capacitance discharge current is diverted to flow

through the alternative path and the stray capacitance is largely or completely discharged through the limiting element. It is necessary to find a trade-off between selecting the value of the current limiting resistor and choosing the time delay before the main thyristor is switched on.

The auxiliary element could additionally switch-on when the rate of change of voltage across the main thyristor exceeds a predetermined threshold.

Another possibility is the use of a fast-auxiliary thyristor instead of the transistor, as showed in Fig. 4-12, with a turn-on delay time smaller than the one of the main thyristor.

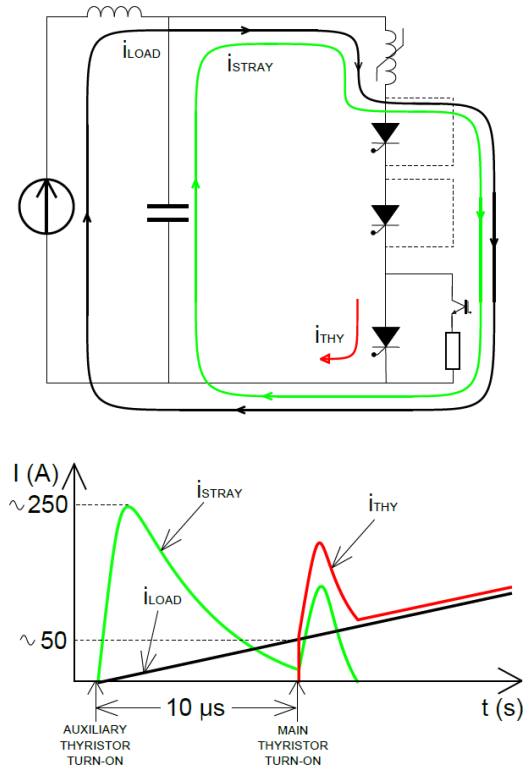


Figure 4-11: Active Current Control purpose [3]

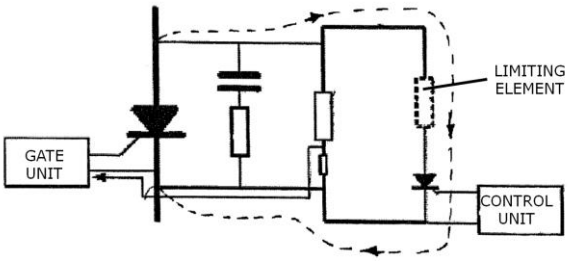


Figure 4-12: Alternative turn-on active circuit configuration [3]

Further discussion about which device can be chosen as the auxiliary device is given in Sec. 7.3. For this research purpose, in simulations it is treated as an ideal switch.

In order to achieve the same functionality of the case in which the saturable inductor is employed, the active branch has to divert the current spike that arises from transformer stray capacitance, in the initial turn-on stage. The auxiliary branch that replaces the saturable inductor is not connected in the same way: while the inductor is in series with the main thyristor, the auxiliary branch is in parallel.

- Active Damping Circuit

Thyristors from the same batch exhibit different characteristics, such as different reverse recovery charge, and have inherent limitations in their performance. The idea to overcome these limitations is to connect an auxiliary branch in parallel to the main thyristor and to create an alternative current path, which makes it possible to reduce the voltage across the main thyristor and to follow a certain voltage reference. Compensation of voltage variations in the turn-off performance gives the possibility to mix and match thyristors from different batches and suppliers and to reduce the size of the associated damping circuit. A complete valve configuration, including voltage measurement across the DC grading resistor and the relevant feedback to the control unit, is showed in Fig. 4-13, beside the compensation process.

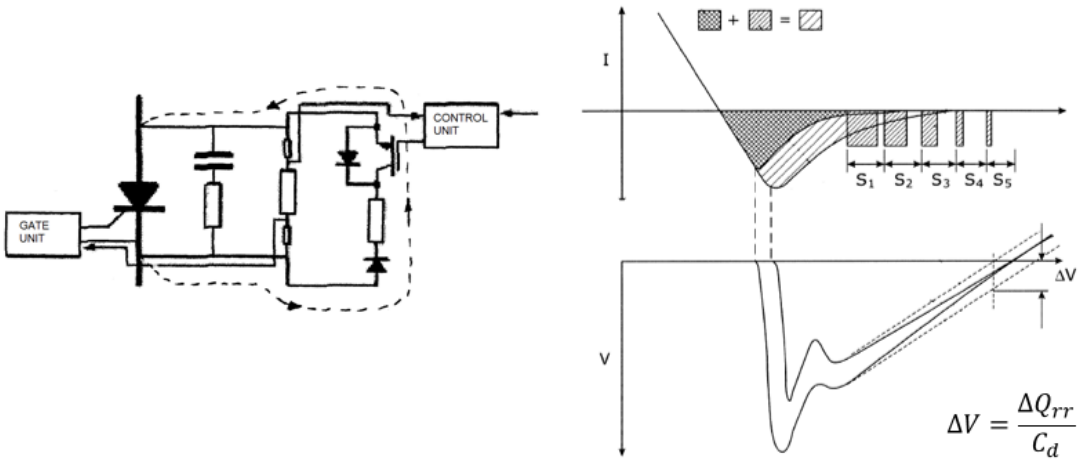


Figure 4-13: Active Damping Circuit configuration and purpose [4]

The aim of the auxiliary branch active control is to pass an amount of charge approximately equal to the difference of Qrr and bring the voltage across the main thyristors closer to the average voltage of the series. Another task of the active damping circuit is the control of reapplied dv/dt, experienced by the thyristor when it is switched off. The control of the static forward voltage in the off-state is still carried out by the DC grading resistor.

It is possible to include both the parallel and the inverse parallel auxiliary switching elements in a full bridge arrangement (Fig. 4-14), or by direct use of a bidirectional switch to obtain bidirectional functionality. In this configuration, voltage balance in both forward and reverse recovery can carried out by the same circuit, using a single control unit for all the tasks.

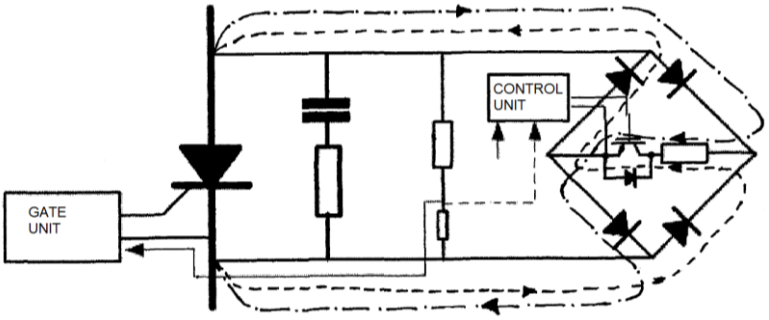


Figure 4-14: Full bridge arrangement of active circuits [4]

4.3. Summary

In this chapter, the thyristor valve configuration currently used for HVDC applications is presented, describing the function of all the auxiliary components needed to limit the magnitude and the rate of change of voltage and current transients. Such auxiliary components are: the damping resistor, the damping capacitor, the DC grading resistor and the saturable inductor. A cooling system, which size is related to power losses, is also present.

The main effects to be compensated during turn-off commutations are: voltage overshoots, due to the reverse recovery charge, and voltage imbalances, due to reverse recovery charge differences among many devices in series. The effect to be managed during turn-on commutations is the current spike caused by the external stray capacitance discharge. The function of every single auxiliary component in compensating these effects is examined, and issues related to the design of the actual passive auxiliary components are faced. Definitions of thyristor level, valve section and valve are provided as well.

The two active solutions proposed to replace the actual passive components, in order to reduce cost, volume and weight of the valves, are described. The Active Current Control aims to divert current from the external stray capacitance into an auxiliary branch, limiting the rate of rise of current in the main thyristor, during turn-on. The Active Damping Circuit goal is to provide uniform voltage sharing during turn-off, through the management of auxiliary active branches connected in parallel to each thyristor.

In the next chapter, an investigation of the proposed active solutions is conducted, through simulations in Matlab-Simulink environment.

5. Proposal for the Active Current Control and for the Active Damping Circuit

This chapter includes the theory and simulations in Matlab-Simulink environment of two methods to control turn-on and turn-off transitions, in real scale. These two methods are called Active Current Control and Active Damping Circuit. The aim of the first one is to divert the initial current spike from external stray capacitances, during turn-on, while purpose of the second one is to provide voltage equalization, compensating reverse recovery charge differences, immediately after turn-off. Current spike diversion during turn-on is fundamental to limit the rate of rise of current and to avoid failure, caused by overtemperature in a tiny area of the thyristor, while voltage equalisation immediately after turn-off is essential to protect thyristors from overvoltage.

Even though the hardware configuration of both auxiliary circuits is conceptually the same, two different auxiliary branches are installed, due to different electrical ratings required for auxiliary devices and to different values needed for auxiliary resistances. The updated thyristor valve configuration is shown in Fig. 5-1 and its control is based on the block diagram in Fig. 5-2.

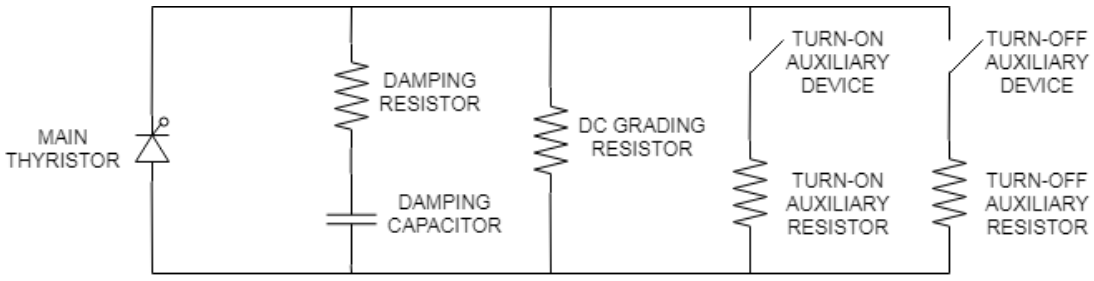


Figure 5-1: Thyristor valve updated with actively controlled branches

The saturable reactor is replaced by the turn-on active branch, while the DC grading resistor is maintained for static voltage control, as explained in Sec. 4.1.

Concerning the main thyristor, if not specified, real scale simulations are always referred to the DYNEX DCR 3980H85 [36], whose ratings are 8.5 kV and 3.98 kA (see Appendix C).

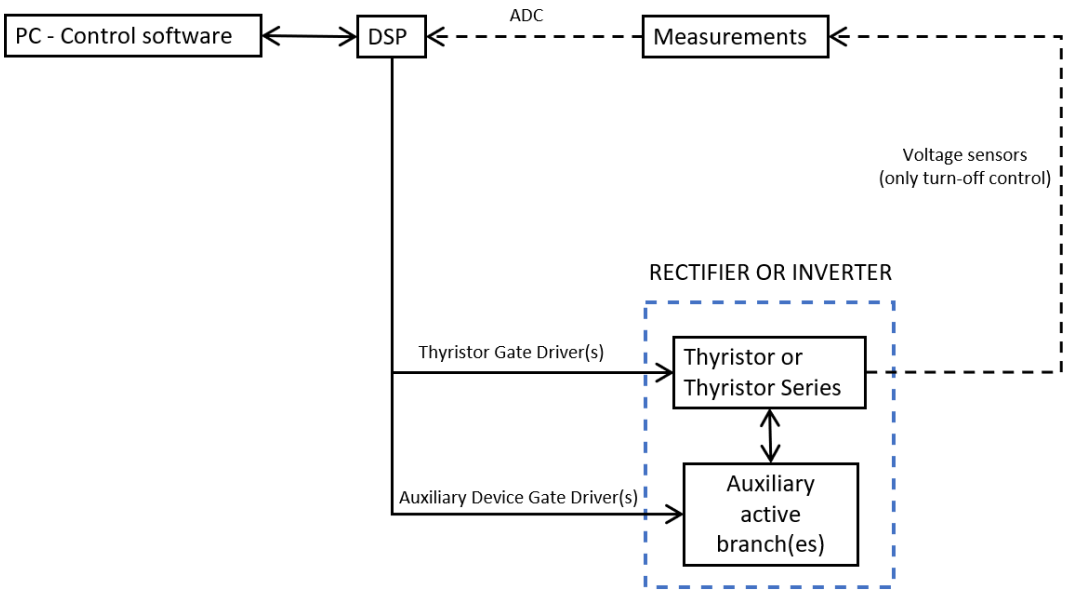


Figure 5-2: Block diagram of the active control methods

Turn-on control method simulations are referred to the 6-pulse inverter in Fig. 5-3, in which the thyristor symbol contains the complete valve illustrated in Fig. 5-1. For turn-off control method simulations, three valves in series are considered, as shown in Fig. 5-4.

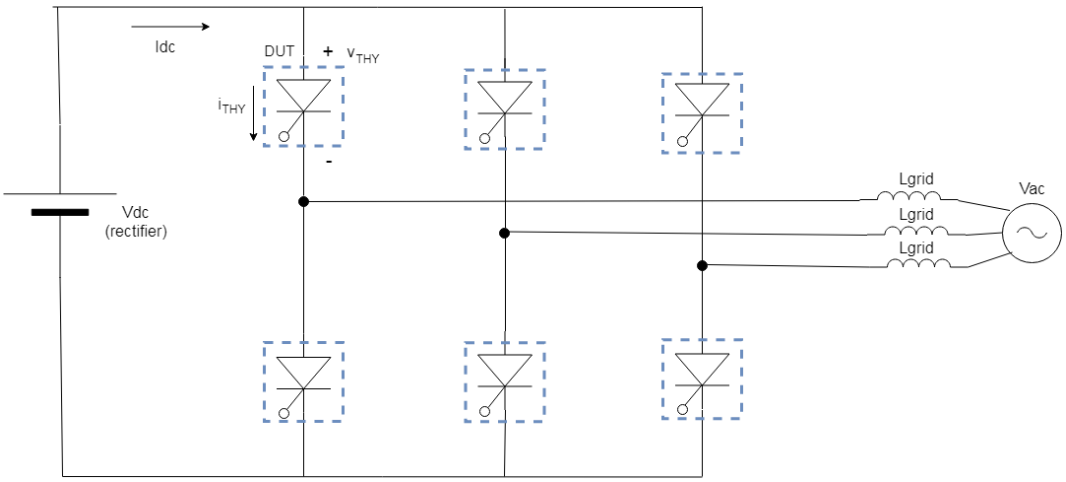


Figure 5-3: Six-pulse inverter for turn-on control simulations in real scale

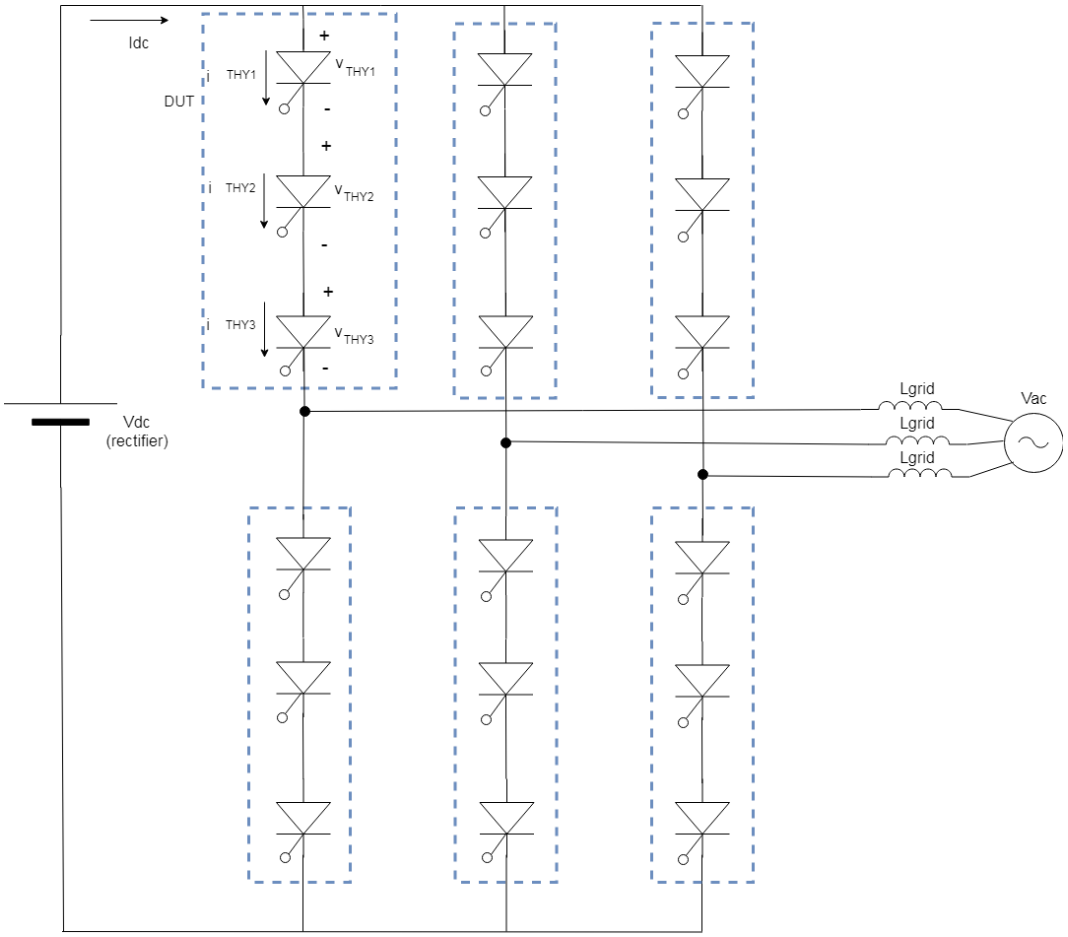


Figure 5-4: Six-pulse inverter for turn-off control simulations in real scale

5.1. Turn-on Control Method

The turn-on control method consists of diverting current from the external stray capacitance into the auxiliary branch, turning the auxiliary device on for a proper time interval (Δt) and delaying the main thyristor turn-on by the same Δt. Auxiliary resistance (R_{AUX}) and Δt values are carefully chosen, through a comparison between different simulation results. In addition, a power losses comparison, based on simulation results, and a discussion about R_{AUX} power rating are provided.

The external stray capacitance depends on the converter transformer and its discharge current is of the type represented in Fig. 4-11. Values of the current peak and of the discharge time interval depend on the specific application: in general, according to the

Alstom Grid/GE Grid Solutions experience, it takes approximately 10 µs for the current to reach the peak, whose value is between 50% and 100% of the on-state current. The transformer model is not known, so it is not straightforward to set a proper external stray capacitance and to reproduce the exact discharge current wave shape in simulation.

Turn-on and turn-off tests are conducted separately. While it is important to use the right Cd-Rd combination for turn-off compensation purposes (as explained in Sec. 4.1), it is not necessary for turn-on tests. Therefore, for turn-on simulations, the damping capacitor can be exploited to provide, approximately, the discharge current that would be provided by the external stray capacitance of the transformer and, consequently, even without a transformer model, the transformer terminal characteristic can be reproduced by the Rd-Cd series combination.

The aim of the turn-on control method is to divert the external capacitance discharge current, in a reliable way. For simulations below, a 2 kA on-state current is considered. Parameters assumed for the current peak and for the discharge time interval are respectively 100% of the on-state current and 20 µs. The Cd-Rd adjustment process is based on the targeted current discharge waveshape: the damping capacitance needs to be large enough to contain all the electric charge to be delivered, while the damping resistance must be the right value to limit the current peak to 2 kA.

The electric charge is the area under the initial turn-on current, which can be calculated considering the current shape approximately as a triangle:

$$Q \cong \frac{I_{PEAK} \cdot \Delta t}{2} = \frac{2\ kA\ \cdot 20\ \mu s}{2} = 20\ mC$$

If the forward voltage before turn-on is 4 kV, the required Cd results:

$$Cd = \frac{Q}{V} = \frac{20\ mC}{4\ kV} = 5\ \mu F$$

Voltage and current wave shapes for Cd = 5µF and different Rd values are illustrated in Fig. 5-5. Maintaining the same capacitance, the area below the initial spike does not change but, reducing the resistance, the current peak value increases.

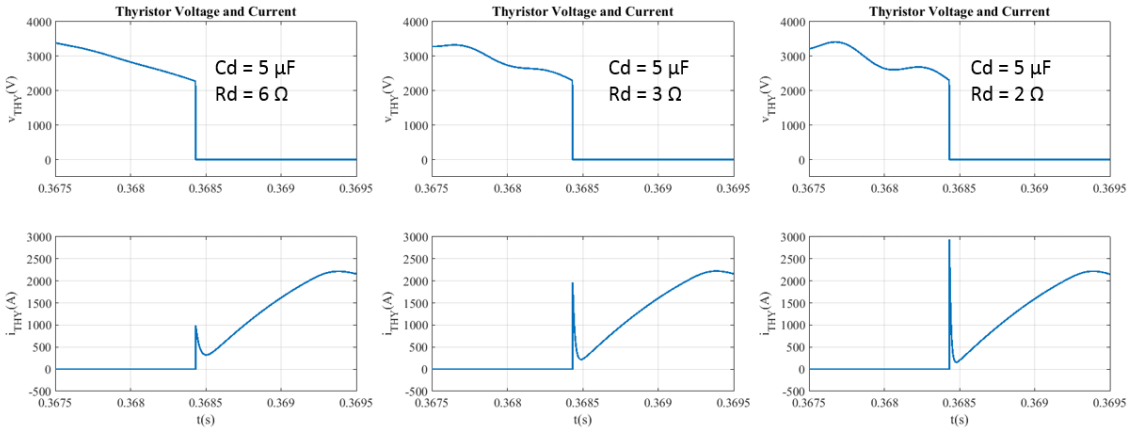


Figure 5-5: Effect of different Rd values on turn-on simulations

Voltage and current wave shapes for Rd = 3 Ω and different Cd values are illustrated in Fig. 5-6. Increasing the capacitance and maintaining the same resistance and the same forward voltage before turn-on, a longer discharge time interval arises.

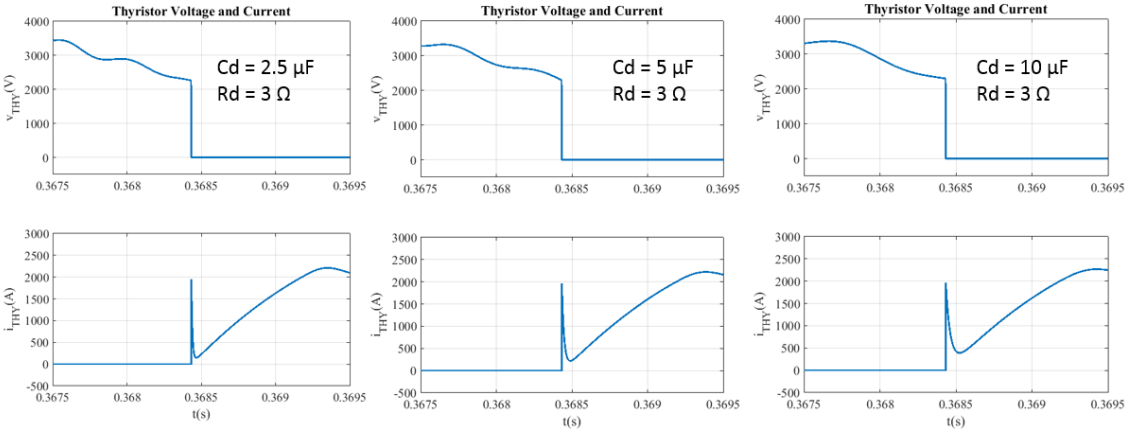


Figure 5-6: Effect of different Cd values on turn-on simulations

To test the robustness of the proposed turn-on control method, the capacitance used in the following simulations is 10 µF, i.e. double than the necessary one: if the auxiliary branch can divert a higher charge than the one of normal operation, it is capable of diverting any lower one. Concerning the damping resistance, after a careful adjustment process, the chosen value is 3 Ω, in order to obtain a 2 kA discharge current peak.

In detail, the discharge process for Cd = 10 µF and Rd = 3 Ω, pointing out the delivered charge into the thyristor in the case of no compensation, is illustrated in Fig. 5-7. In a time interval of about 100 µs, the charge is about 70 mC, which is an overestimated value because it takes into account also the contribute of to the load current: after this time interval, the current rise only depends on the load current.

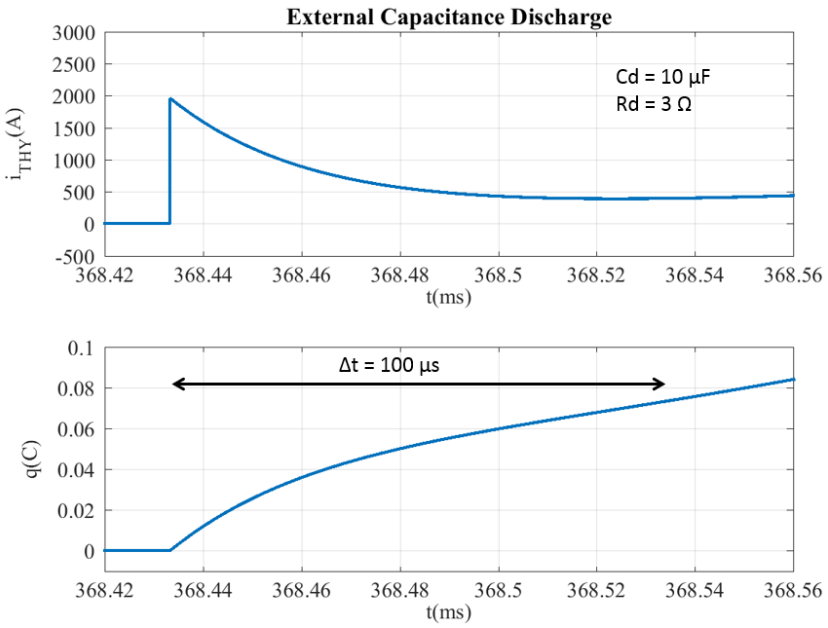


Figure 5-7: External capacitance discharge process and detail of the delivered charge

Subsequently to the external capacitance discharge, the current slope is 2 A/µs, that arises from a voltage of 2 kV at the turn-on time instant and a grid inductance (L_{GRID}) of 1 mH:

$$v = L\frac{di}{dt} \quad \rightarrow \quad \frac{di}{dt} = \frac{v}{L} \quad \rightarrow \quad 2\,A/\mu s = 2\,kV/mH$$

At first, simulation results with no compensation are shown and, subsequently, results for different R_{AUX}, Δt patterns, listed in Table 3, are compared.

Note: In captions, "real scale" becomes "REAL", the main thyristors is addressed as "THY" and "auxiliary branch" becomes just "AUX".

Concerning the auxiliary device, it has to withstand high currents for a short time interval and it can be a SiC device or a pulsed power thyristor, an example of which is the DYNEX PT85QWx45 [37], which main features from its data sheet are listed in Appendix D.

If there is no compensation, the turn-on auxiliary device is never turned-on and the initial current spike to be diverted is highlighted in Fig 5-8. This current spike depends only on the external stray capacitance, which cannot be reduced or eliminated. Therefore, to protect the main thyristor, the electrical charge stored in the stray capacitance can be safely and completely discharged through a dedicated path.

The current spike width does not change in different operating conditions, so it is only required to find the most appropriate R_{AUX}, Δt pattern with no need to implement a closed loop control method. In simulation, once Δt is decided, the main thyristor turn-on is delayed by the same time interval, during which only the auxiliary device is turned on. In the real case, if thyristor turn-on is delayed, there may again be a di/dt limitation immediately after turn-on: keeping the auxiliary branch on for a short time after initial turn on will help to clamp the voltage across the thyristor during the spreading phase.

Simulation results for different R_{AUX} and Δt patterns are compared from Fig. 5-9 to Fig. 5-14 and a general criterion to choose the best compromise is discussed. For each pattern, it happens that the sum of the auxiliary current and the main thyristor current is equal to the not compensated main thyristor current.

Increasing R_{AUX}, the auxiliary branch current peak is reduced, its width is increased, and corresponding power losses are larger. Power losses affect both the converter efficiency and the cooling system size. For a six-pulse converter, the instantaneous and average power losses in a period are:

$$p_{LOSS}(t) = 6 \cdot R_{AUX} {i_{AUX}}^2(t)$$

$$P_{LOSS_MEAN} = \frac{1}{T}\int_0^T p_{LOSS}(t)dt = = \frac{1}{T}\int_0^T R_{AUX} {i_{AUX}}^2(t)dt$$

This power corresponds to the thermal power to be carried by the cooling system and its percentage of the transmitted power through the HVDC line is:

$$P_{LOSS_MEAN}\% = \frac{P_{LOSS_MEAN}}{P_{TRANSMITTED_MEAN}} \cdot 100$$

The mean transmitted power would be the same value as the instantaneous one, if there was no ripple. For considered simulations: $P_{TRANSMITTED_MEAN}$ = 28 MW (2kA; 14kV)

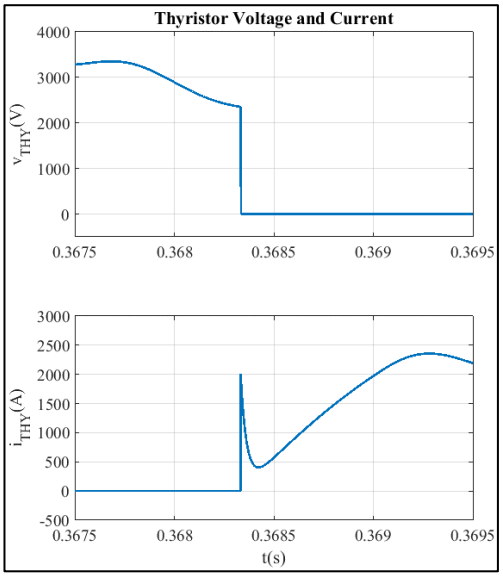


Figure 5-8: Turn-on REAL - no compensation – THY waveforms

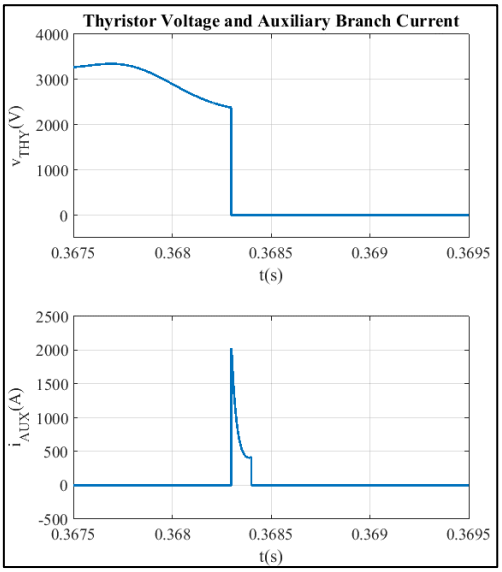


Figure 5-9: Turn-on REAL – Pattern 1– AUX waveforms

Pattern	R_{AUX}	Δt
1	0.03 Ω	100 µs
2	0.3 Ω	120 µs
3	3 Ω	160 µs

Table 3: R_{AUX}, Δt patterns for turn-on compensation

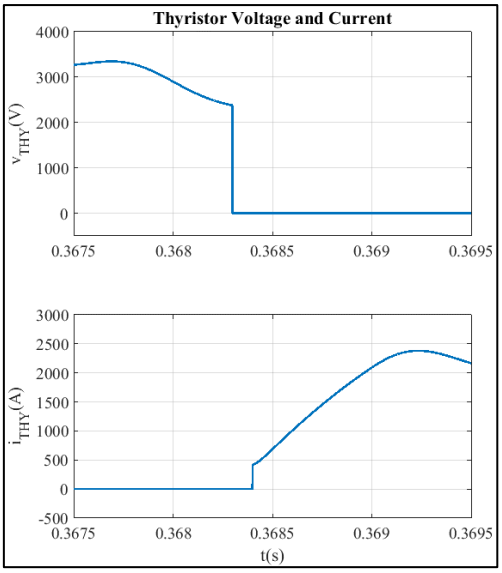


Figure 5-10: Turn-on REAL - Pattern 1– THY waveforms

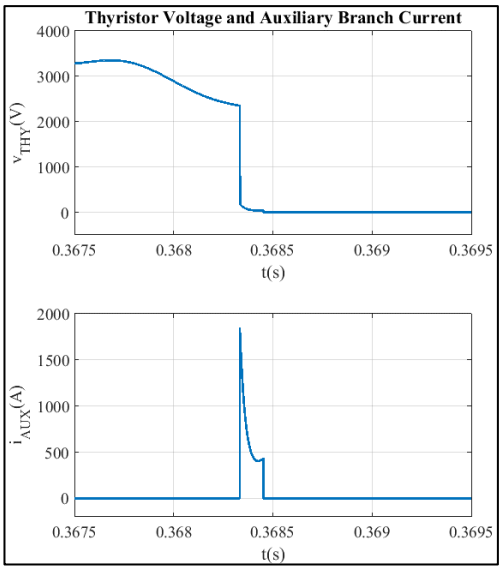


Figure 5-11: Turn-on REAL - Pattern 2– AUX waveforms

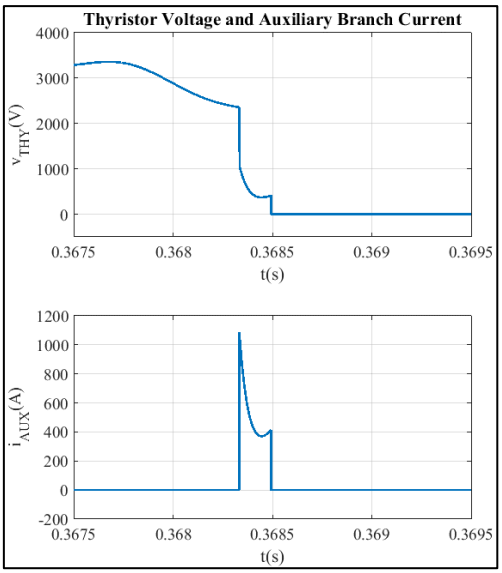


Figure 5-13: Turn-on REAL - Pattern 3 – AUX waveforms

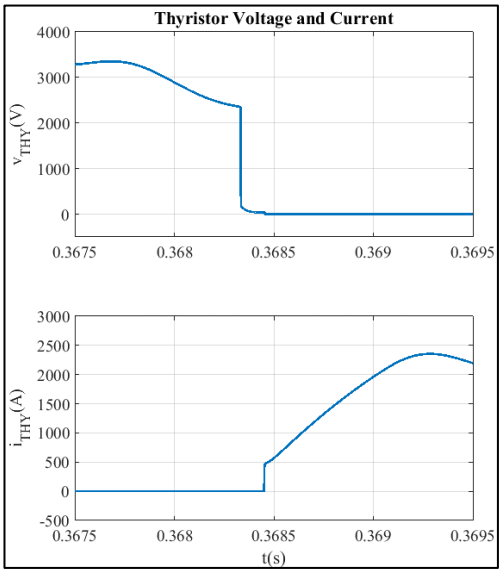


Figure 5-12: Turn-on REAL - Pattern 2 – THY waveforms

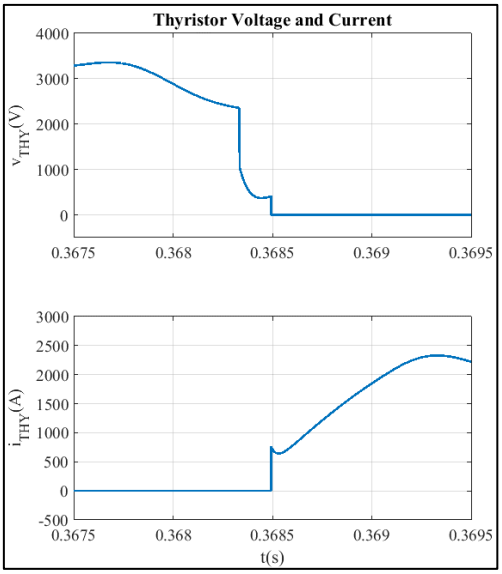


Figure 5-14: Turn-on REAL - Pattern 3– THY waveforms

In detail, simulation results for R_{AUX} =0.03 Ω, Δt =100 μs are shown in Fig. 5-9 and Fig. 5-10, results for R_{AUX} =0.3 Ω, Δt =120 μs in Fig. 5-11 and Fig. 5-12 and results for R_{AUX} =3 Ω, Δt =160 μs in Fig. 5-13 and Fig. 5-14.

Instantaneous power losses and mean power losses for each pattern are shown from Fig. 5-15 to Fig. 5-17.

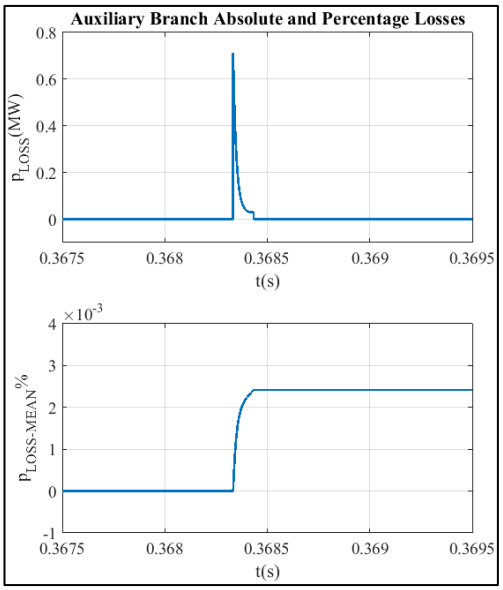


Figure 5-15: Power losses for Pattern 1

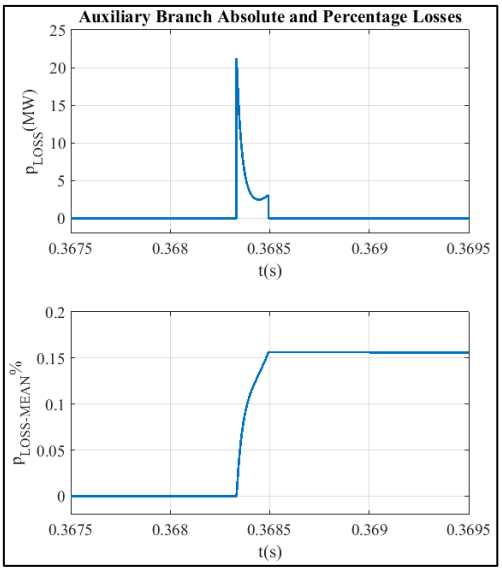


Figure 5-17: Power losses for Pattern 3

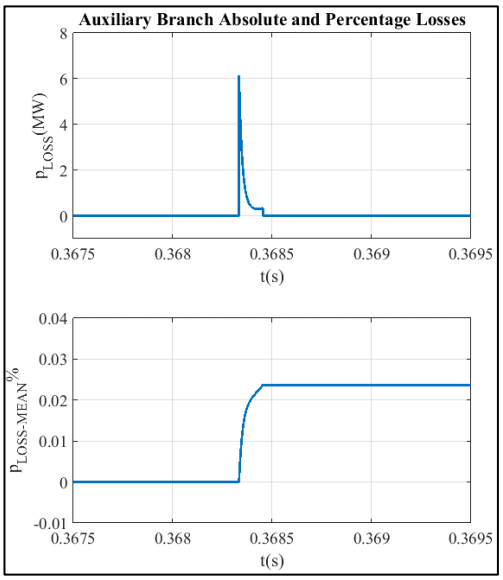


Figure 5-16: Power losses for Pattern 2

From pictures, power losses values corresponding to each R_{AUX} are:

R_{AUX} = 0.03 Ω → P_{LOSS_MEAN} = 700W

R_{AUX} = 0.3 Ω → P_{LOSS_MEAN} = 6.2 kW

R_{AUX} = 3 Ω → P_{LOSS_MEAN} = 42 kW

This power represents the cooling system thermal power portion that depends on turn-on compensation.

In these simulations, the particular way of providing the initial current spike results in power losses in the damping resistor. However, this is not a realistic spike source, but only a method for simulation and experimental purposes, so it does not affect considerations about R_{AUX} power rating.

In conclusion, assuming a certain stray capacitance value, its stored charge must be completely released in every period, regardless of the R_{AUX} value. The stored charge is about the same as the area below the i_{AUX} waveform, which becomes lower and wider with increasing R_{AUX}. For this reason, when increasing R_{AUX} it is necessary to increase also Δt, to maintain the same area. But the slower is the process, the larger are power losses, so, at the end, R_{AUX} must be chosen as small as possible to achieve the quickest compensation process and the smallest power loss. The minimum value of R_{AUX} is limited by the peak current, which depends also on the converter transformer: for a real transformer, a detailed model would need to be considered, including all the relevant impedances. Once R_{AUX} is defined, the corresponding Δt can be determined as well, and the control system turns out to be completely designed.

If the real scale final design of the active configuration shows smaller power losses than the case in which the saturable reactor is employed, the cooling system size can be reduced. If cost, volume and weight of the valve that uses the turn-on auxiliary active branch are smaller than the ones of the saturable reactor employment case, the active option results more convenient.

Aim of this work is to demonstrate that the physical principle of current diversion through an auxiliary active branch works correctly. Therefore, in addition to real scale simulations illustrated above, reduced scale simulations and experimental verification have been done and results are summarized in Sec. 7.1.

5.2. Turn-off Control

In a thyristor valve without any actively controlled compensation system, the damping capacitance (Cd) is designed to address two tasks: provide enough damping and limit voltage differences during turn-off. If a turn-off auxiliary active branch compensates voltage differences, Cd can be designed only to limit oscillations, which leads to choosing a smaller capacitance value and to reducing the associated cost, volume and weight. Once Cd is reduced, it is necessary to choose a proper damping resistance (Rd) value to achieve an acceptable damping. In this chapter, both Cd and Rd are maintained to the realistic values of 1 μF and 40 Ω respectively and the discussion is focussed on how to compensate voltage differences, regardless of Cd and Rd variations. A detailed discussion about Cd reduction and consequent Rd choice is given in Sec. 7.2, where both simulations and experimental tests with different Cd-Rd combinations are compared, in a reduced scale.

Voltage differences depend on non-uniform reverse recovery charge (Qrr) and reverse recovery time (trr) of thyristors from the same batch. Thyristors with smaller Qrr are called “faster” because they take a shorter time to turn-off than the ones with bigger Qrr, addressed as “slower”. If no active branches are connected, the turn-off process for two thyristors in series, with different Qrr, is described below and referred to the electrical circuit in Fig. 5-18.

Until the faster thyristor starts to recover, reverse recovery currents (I_{RR1} and I_{RR2}) flow across the devices and voltage across both thyristors is zero. When the faster thyristor starts to recover, voltage builds across Cd for faster device. However, no change in voltage across the slower thyristor occurs until some time later, due to reverse recovery charge differences (ΔQrr). When also the slower device starts to recover, voltage increases across both capacitors but, at the end of the process, voltage across Cd for faster device is always higher (more negative).

The bigger is Cd, the more uniform is voltage sharing (voltage differences are approximately: $\Delta V=\Delta Qrr/Cd$), but the employment of bigger Cd has many drawbacks in terms of cost, volume, weight and losses. This fact leads to investigate different solutions for uniform voltage sharing than increasing Cd.

The concept of active voltage balancing is based to the connection of an auxiliary resistance (R_{AUX}), in parallel to each thyristor for proper time intervals, slowing down voltages that tend to establish quicker that the other ones. Time interval amounts depend on the specific control method. The dynamics followed by the compensation process is described below and referred to the electrical circuit in Fig. 5-19.

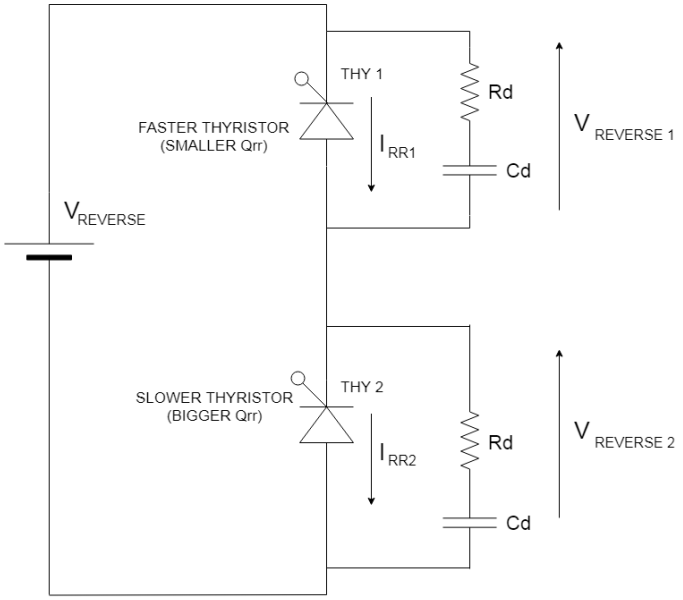


Figure 5-18: Turn-off process for two thyristors in series with different Qrr and no compensation

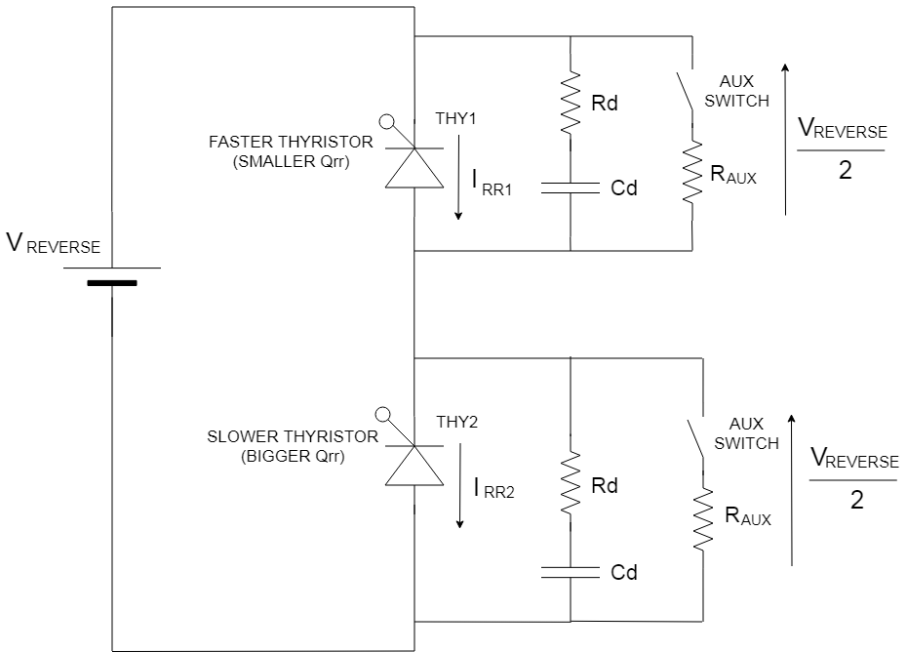


Figure 5-19: Turn-off process for two thyristors in series with active compensation

When the auxiliary switch connected in parallel to the faster thyristor is turned on, it is not possible for that thyristor to start establishing the reverse voltage, so it has to "wait for the slower thyristor" to start getting into the reverse blocking state. This mechanism makes it possible to choose the Cd value only for damping purpose and not for voltage sharing anymore.

Regardless the control method, the physics of the compensation process does not change from one technique to another. R_{AUX} remains connected in parallel to the faster thyristor for the necessary compensation time interval (Δt). To look for the best R_{AUX} value it is necessary to test different values and to choose the one that gives the preferable response in terms of compensation speed, voltage steps (dv/dt) and losses. To determine Δt in advance, it would be necessary to know ΔQrr in advance, but this is not practical and not possible with a reasonable precision. For this reason, a closed loop, real time control is necessary. Two control methods have been investigated: hysteresis and "turn-off delay". The first one is explained in detail in the following section, while the second one is examined in the subsequent section. In both cases, current in the auxiliary branch flows in the opposite way than in the turn-on compensation process, therefore, both R_{AUX} and the auxiliary switch have different features than in the turn-on case.

Most of the studies concern two or three devices in series, but all the concepts can be extended to any number of devices in series just referring each ΔV to the average voltage.

5.3. Hysteresis Method

The hysteresis method, summarised in Fig. 5-20, consists of measuring thyristor voltages continuously, at a proper sampling frequency (with the actual microcontrollers, there is no problem to take voltage measurements at a relatively high sampling frequency, compared to the industrial one) and calculating the average value. Voltage differences (ΔVs) are subsequently calculated through the differences between each voltage and the average one and compared to the hysteresis thresholds, (V_{UP} and V_{DOWN}), according to Fig. 5-21. In detail, if the voltage difference between a thyristor voltage and the average voltage is above V_{UP} or below V_{DOWN}, the auxiliary switch in the auxiliary branch of the considered thyristor is turned ON or OFF respectively. When the voltage difference is between V_{DOWN} and V_{UP}, the switch state depends on its previous state, before crossing the threshold.

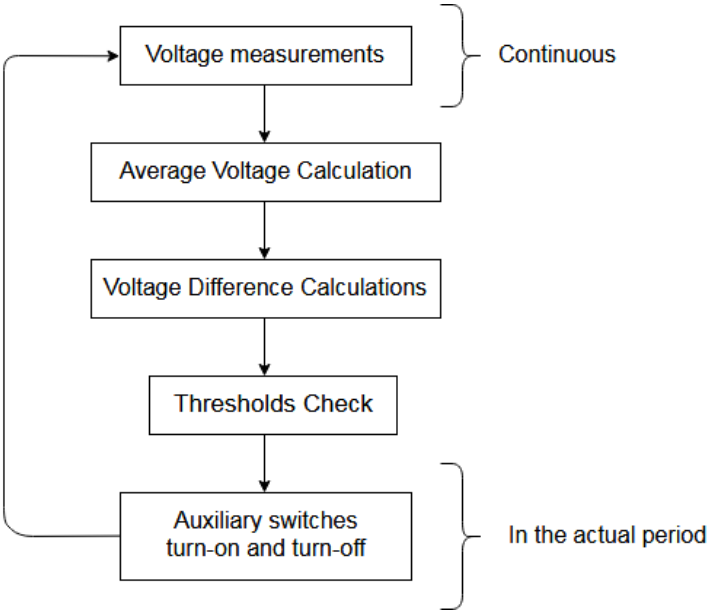


Figure 5-20: Functional chart of hysteresis method for turn-off compensation

The considered R_{AUX}, V_{UP} and V_{DOWN} patterns are listed in Table 4.

Pattern	R_{AUX}	V_{UP}	V_{DOWN}
1	1 kΩ	100	-20
2	500 Ω	100	-20
3	1 kΩ	50	-10
4	500 Ω	50	-10

Table 4: R_{AUX}, V_{UP}, V_{DOWN}, Patterns for turn-off compensation – Hysteresis method

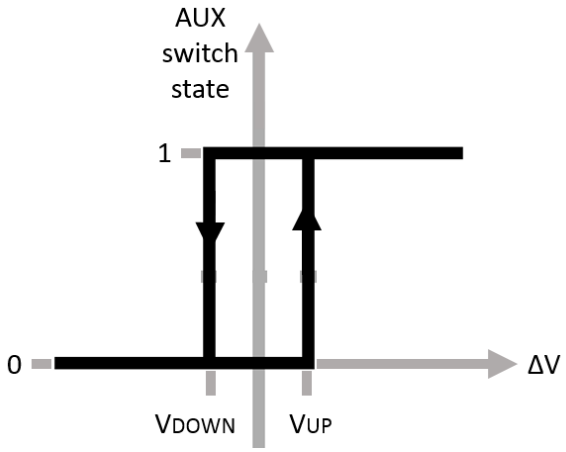


Figure 5-21: Graphical description of hysteresis method for turn-off compensation

Advantages of the hysteresis method are that it has no transient to reach the steady state and it is easy to be implemented. Only three parameters in total are required: R_{AUX}, V_{UP} and V_{DOWN}.

Simulation results for three modules in series, are reported below. Given that Cd is maintained to the realistic value of 1 μF (no active compensation case), ΔQrr is exaggerated to ± 20%, to get significant ΔV to be compensated. Results of no compensation are shown in Fig. 5-22 and 5-23, while results of compensation with Pattern 1 are represented in Figures 5-24 and 5-25.

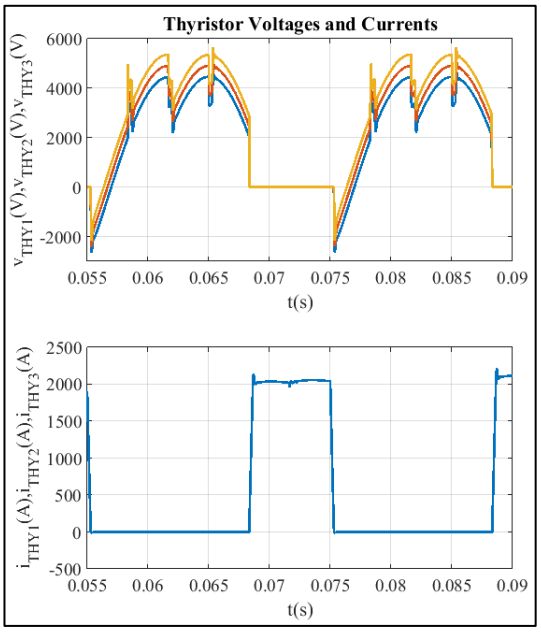


Figure 5-22: Hysteresis REAL - no compensation – THY waveforms

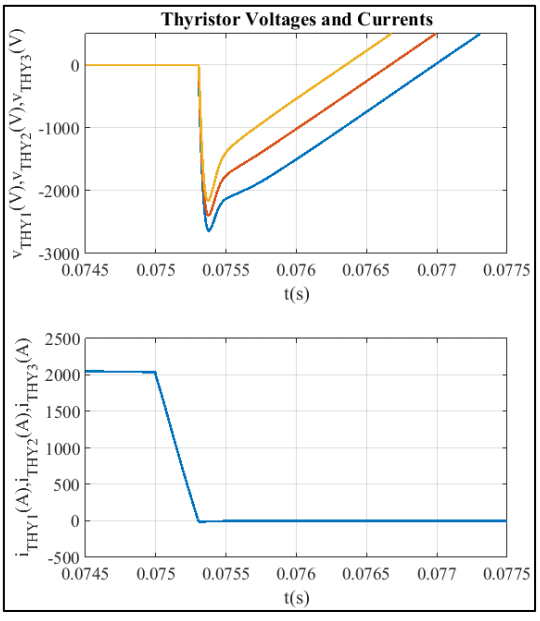


Figure 5-23: Hysteresis REAL - no compensation – THY waveforms – zoom

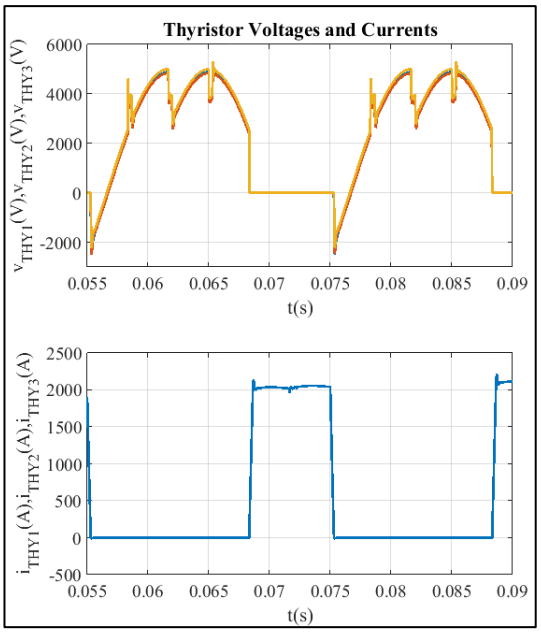


Figure 5-24: Hysteresis REAL – Pattern 1 – THY waveforms

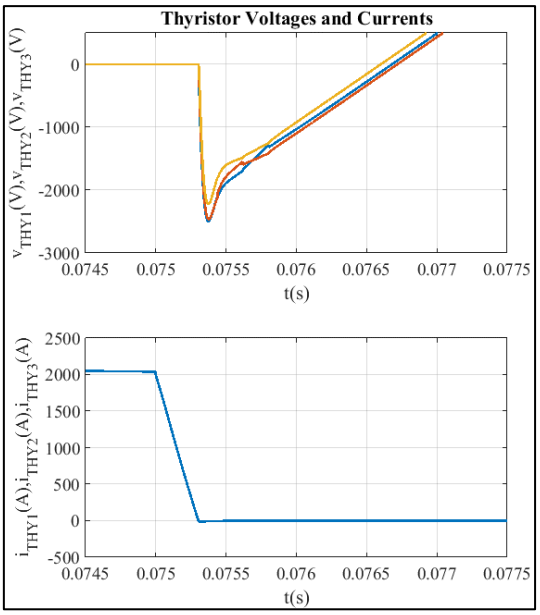


Figure 5-25: Hysteresis REAL – Pattern 1 – THY waveforms – zoom

Different patterns of R_{AUX}, V_{UP} and V_{DOWN} are analysed in terms of ΔV and auxiliary switch gate signals. Waveforms for R_{AUX}=1kΩ, V_{UP}=100V and V_{DOWN}= -20V, in Fig. 5-26 and Fig. 5-27, are compared with waveforms for R_{AUX}=500Ω, in Fig. 5-28 and Fig. 5-29 (same V_{UP} and V_{DOWN}).

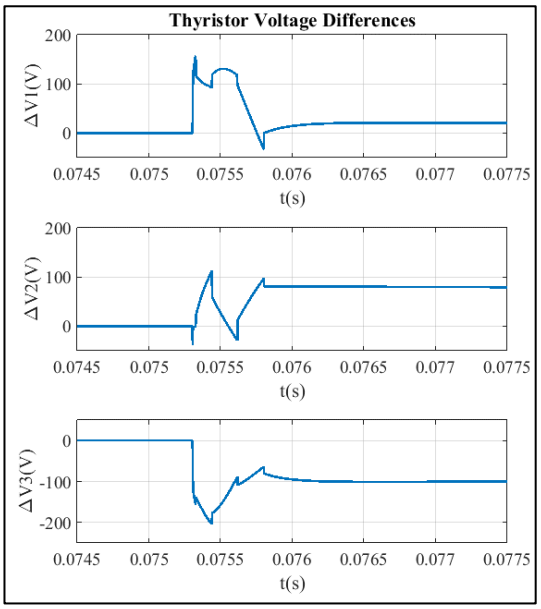


Figure 5-26: Hysteresis REAL – Pattern 1 – voltage differences

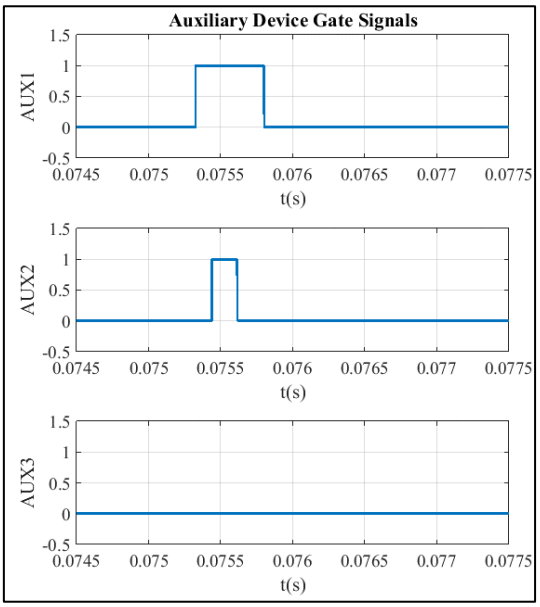


Figure 5-27: Hysteresis REAL - Pattern 1 – aux gate signals

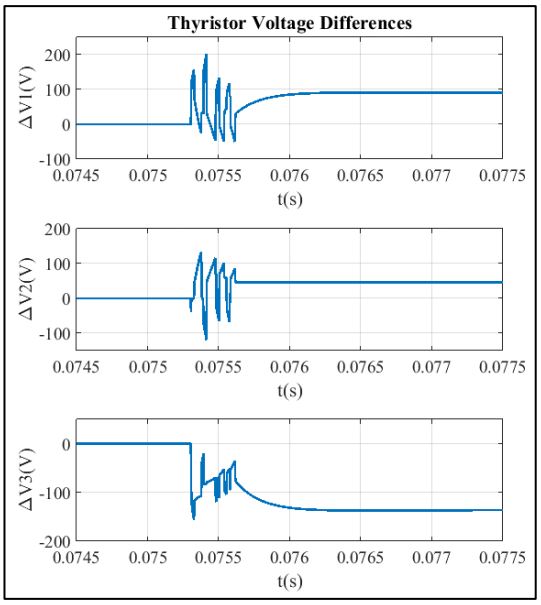


Figure 5-28: Hysteresis REAL – Pattern2 – voltage differences

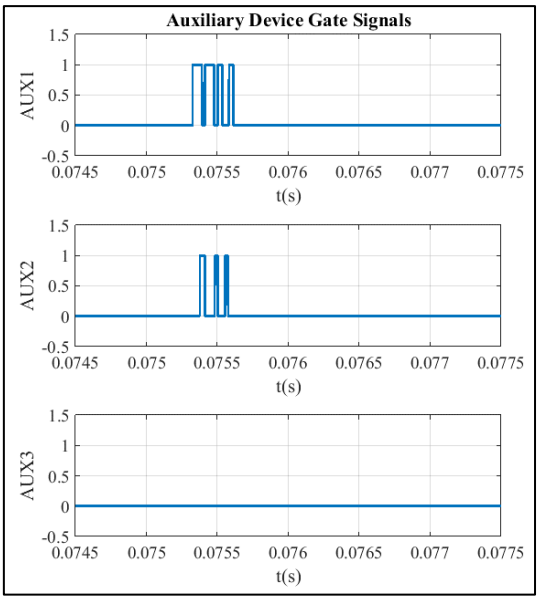


Figure 5-29: Hysteresis REAL – Pattern 2 – aux gate signals

Reducing R_{AUX}, the control becomes more tends to become unstable: ΔV is more oscillating and auxiliary switch gate signals jump between 0 and 1 more than once during the compensation process. Similar results are obtained maintaining R_{AUX}=1kΩ and setting V_{UP}= 50V, V_{DOWN}= -10V (Fig. 5-30, 5-31). Reducing both R_{AUX} and voltage thresholds to the pattern R_{AUX}=500Ω, V_{UP}=50V, V_{DOWN}= -10V, the control gets even more prone to instability (Fig. 5-32, 5-33).

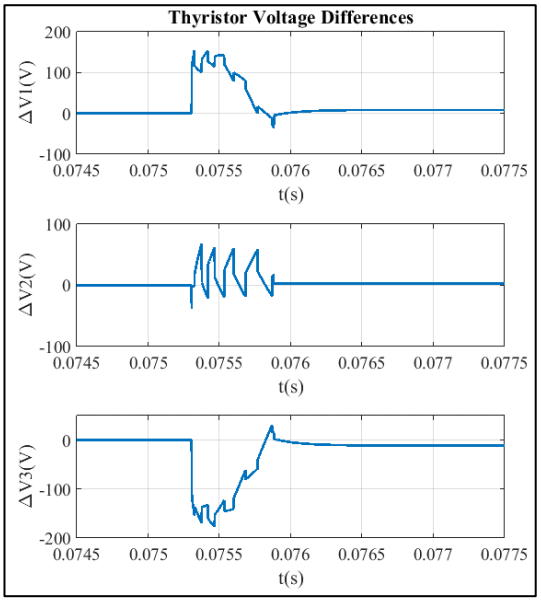


Figure 5-30: Turn-off REAL – Pattern 3 – voltage differences

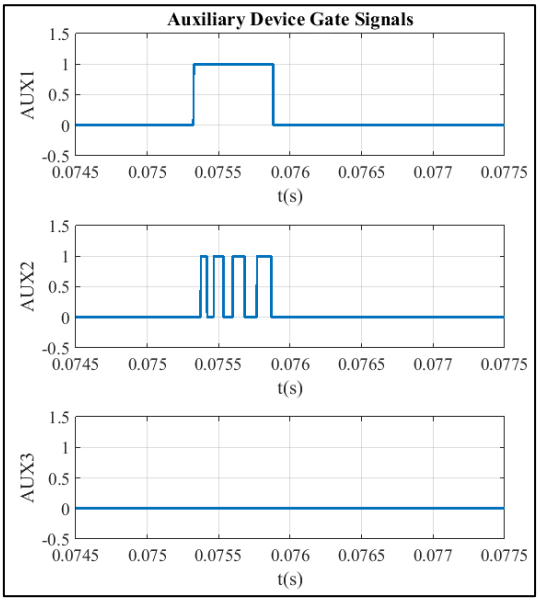


Figure 5-31: Turn-off REAL – Pattern 3 – auxiliary gate signals

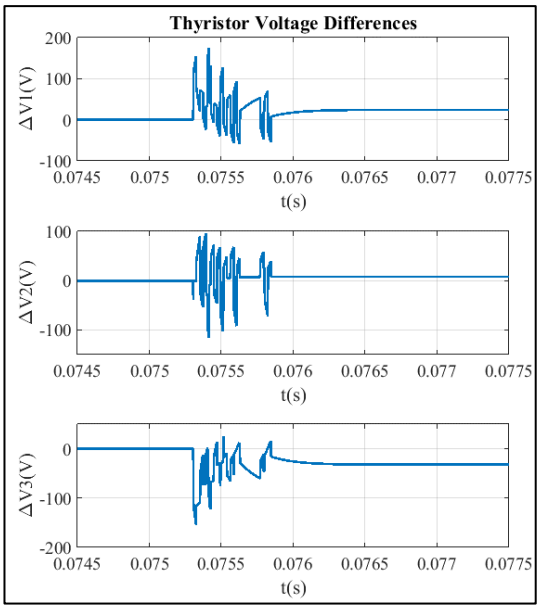


Figure 5-32: Turn-off REAL – Pattern 4 – voltage differences

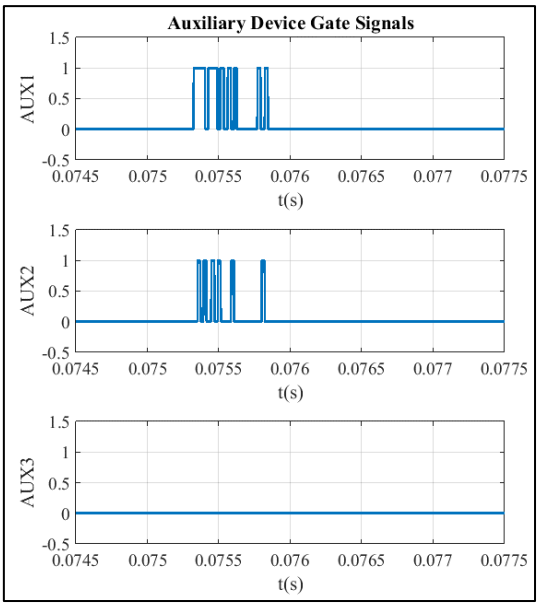


Figure 5-33: Turn-off REAL – Pattern 4 – auxiliary gate signals

Losses in the auxiliary branch for all the considered patterns of parameters are shown in Figures 5-35, 5-37, 5-39 and 5-41, beside zooms of voltage compensation (Fig. 5-34, 5-36, 5-38, 5-40). Instantaneous and average power losses are referred to a six-pulse converter, in the same way of turn-on compensation losses (Sec. 5.1). Mean transmitted power is still 28 MW.

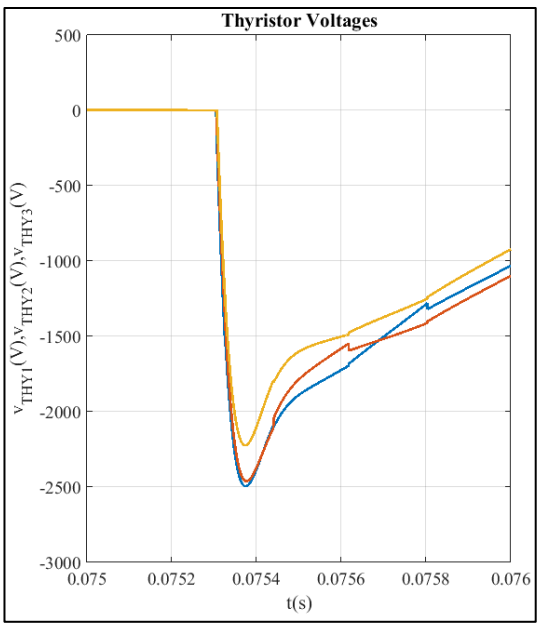


Figure 5-34: Turn-off REAL – Pattern 1 – voltages – zoom

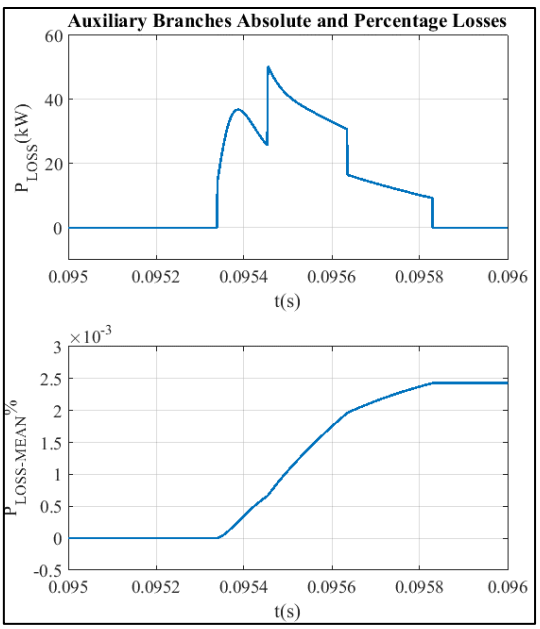


Figure 5-35: Power losses for Pattern 1

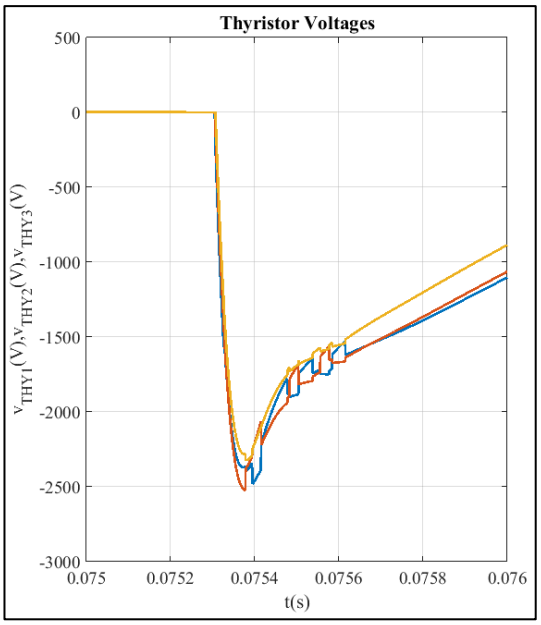


Figure 5-36: Turn-off REAL – Pattern 2 – voltages – zoom

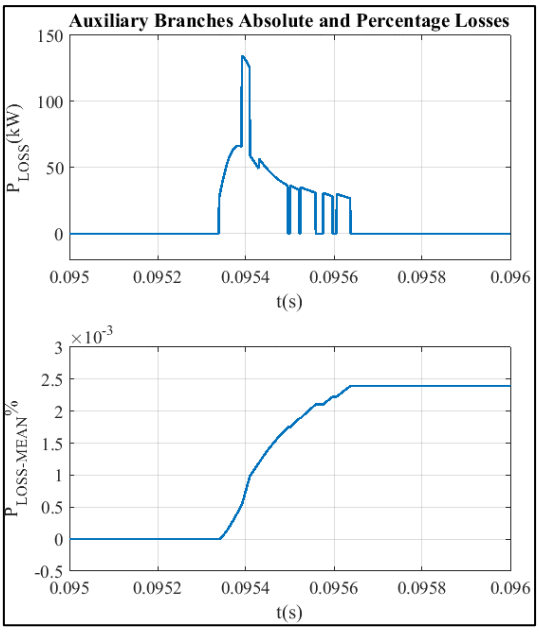


Figure 5-37: Power losses for Pattern 2

Power losses are between 650 W and 800W for all the four patterns considered, over a transmitted power of 28 MW. Therefore, percentage losses are between 0.0025% and 0.003%, in general much smaller than the ones of turn-on compensation.

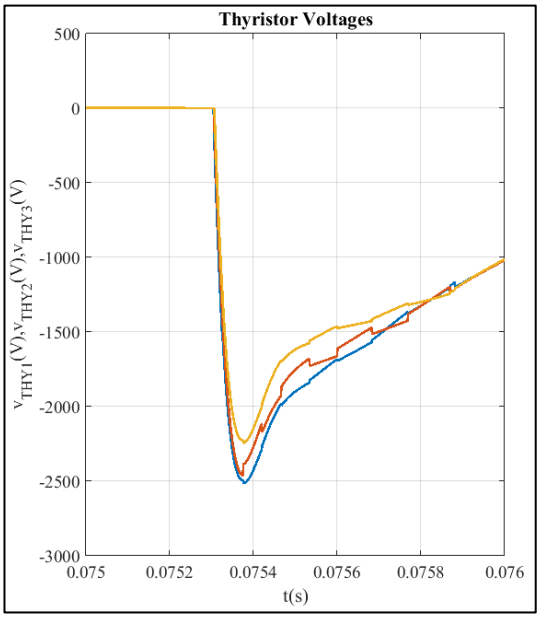


Figure 5-38: Turn-off REAL – Pattern 3 – voltages - zoom

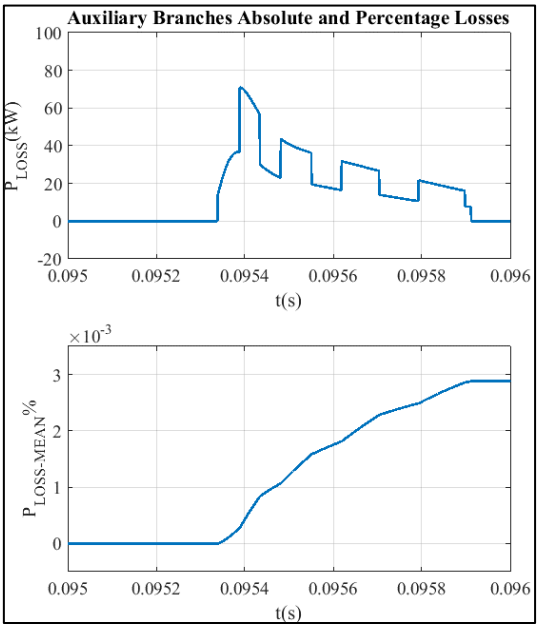


Figure 5-39: Power losses for Pattern 3

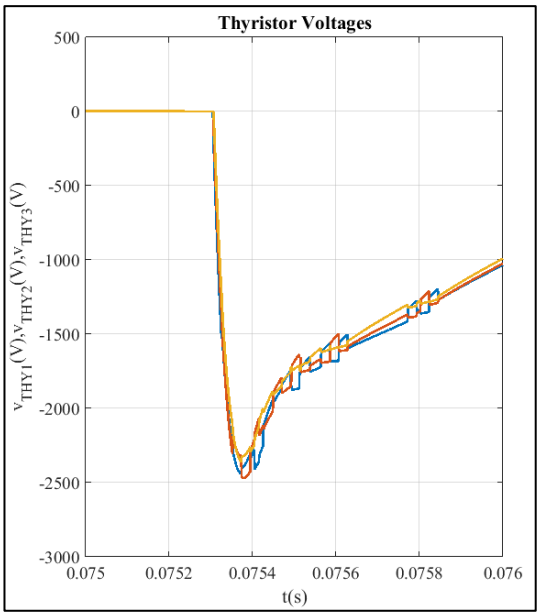


Figure 5-40: Turn-off REAL – Pattern 4 – voltages - zoom

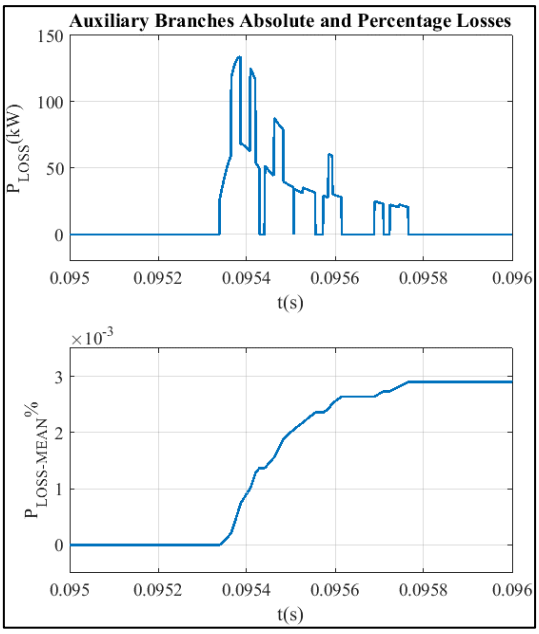


Figure 5-41: Power losses for Pattern 4

The hysteresis method has two main disadvantages. The first one is that compensation cannot start immediately at the beginning of the turn-off process, but only when the first ΔV exceeds one threshold, while the second one is that, at the end of compensation, ΔV cannot be zero, but only a value within hysteresis thresholds. There is a limit to thresholds reduction, as represented in comparisons above: if they are too small, the compensation process tends to instability and the auxiliary switch commutates too many times during compensation. The same consequence occurs reducing R_{AUX} too much, but with the adantage of reducing the compensation process duration.

Power losses of the auxiliary branch must be taken into account into the design of the overall valve cooling system.

Both limitations of the hysteresis method are overcome by the “turn-off delay” method, investigated in the following section.

5.4. Faster Device "Turn-off Delay" Method

The faster device "turn-off delay" method, summarized in Fig. 5-42, consists of measuring thyristor voltages in a discrete way, once every period, calculating the average voltage and voltage differences (ΔVs), and eventually deciding the compensation time interval, addressed as "turn-off delay" (or just "delay") value. Voltages are measured at a point between the end of the turn-off transient and the subsequent voltage zero crossing with positive slope. ΔVs are calculated through differences between each voltage and the average one, and once ΔV is available for each thyristor, it is elaborated in a PI closed loop, which decides the "delay". The compensation process is based on the same physics as the hysteresis method, previously described. The "delay" is the time interval that the auxiliary switch remains on and the one calculated in a certain period is applied in the subsequent one, as soon as current zero crossing occurs.

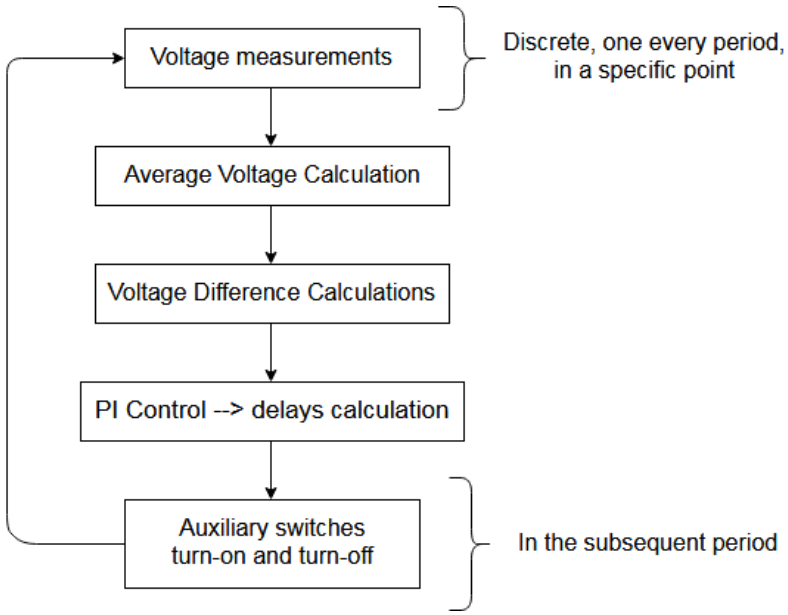


Figure 5-42: Functional chart of "turn-off delay" method for turn-off compensation

During the PI control transient, voltage sharing is not uniform, but once the steady state is reached, the "delay" for each thyristor depends only on their ΔQrr. Like the hysteresis method, only three parameters in total are required: R_{AUX} and the two PI control constants, K_P and K_I. Three R_{AUX} values are considered: 10 Ω, 100 Ω and 500 Ω. When R_{AUX} is 10 Ω and 100 Ω, K_P and K_I are $5 \cdot 10^{-9}$ and $2 \cdot 10^{-6}$ respectively, while

when R_{AUX} is 500 Ω, K_P and K_I are $10 \cdot 10^{-9}$ and $8 \cdot 10^{-6}$ respectively. The choice of the K_I values is related to the relationship between voltage differences and compensation time intervals, while the determination of K_P depends on the dynamic of the compensation process. The three considered patterns are summarized in Table 5.

Pattern	R_{AUX}	K_P	K_I
1	100 Ω	$5 \cdot 10^{-9}$	$2 \cdot 10^{-6}$
2	10 Ω	$5 \cdot 10^{-9}$	$2 \cdot 10^{-6}$
3	500 Ω	$10 \cdot 10^{-9}$	$8 \cdot 10^{-6}$

Table 5: R_{AUX}, K_P, K_I, Patterns for turn-off compensation – "Turn-off Delay" Method

Simulation results for three modules in series, are reported below. Given that Cd is maintained to the realistic value of 1 μF (no active compensation case), ΔQrr is exaggerated to ± 20%, to get significant ΔV to be compensated. Results of no compensation are shown in Fig. 5-43 and Fig. 5-44, while results of compensation with R_{AUX}=100Ω, $K_P=5 \cdot 10^{-9}$, $K_I=2 \cdot 10^{-6}$ are represented in Fig. 5-45 and Fig. 5-46.

Concerning Pattern1 (R_{AUX}=100Ω, $K_P=5 \cdot 10^{-9}$, $K_I=2 \cdot 10^{-6}$), simulation results for ΔVs, auxiliary switch gate signals, dv/dt stresses and losses are shown in Figures 5-47, 5-48, 5-49 and 5-50 respectively.

Two additional patterns are investigated in terms of compensation speed and ΔV. Waveforms for R_{AUX} = 10 Ω, in Figures 5-51 and 5-52, are compared with waveforms for R_{AUX} = 500 Ω, in Figures 5-53 and 5-54.

A comparison is done also in terms of auxiliary switch gate signals and dv/dt stresses. Waveforms for R_{AUX} = 10 Ω, in Figures 5-55 and 5-56, are compared with waveforms for R_{AUX} = 500 Ω, in Figures 5-57 and 5-58.

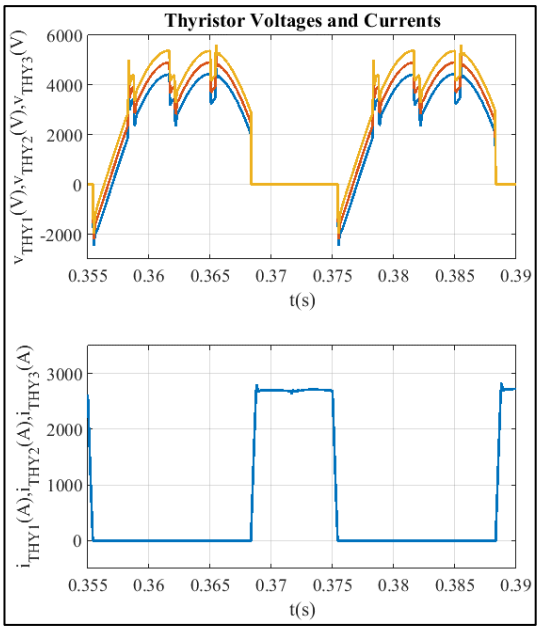


Figure 5-43: Turn-off REAL - no compensation - THY waveforms

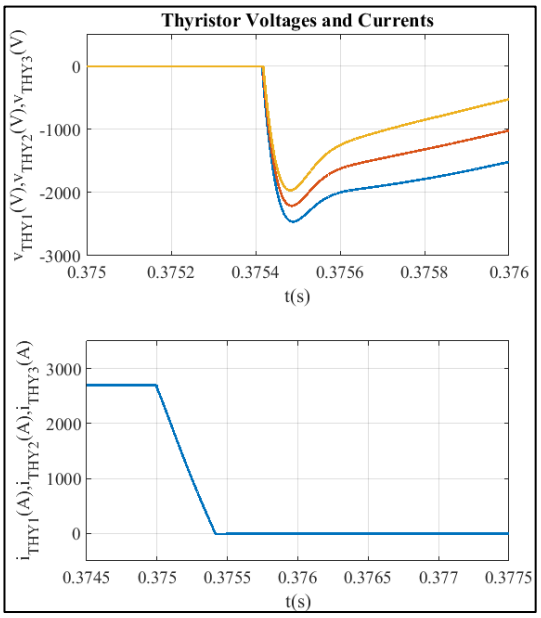


Figure 5-44: Turn-off REAL - no compensation - THY waveforms – zoom

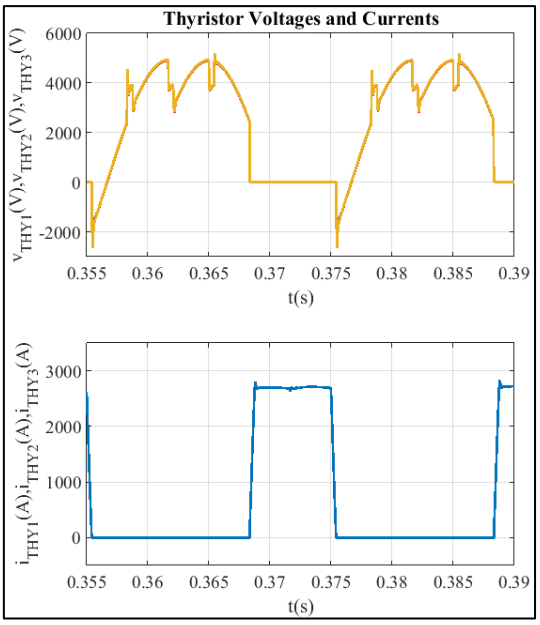


Figure 5-45: Turn-off REAL – Pattern 1 - THY waveforms

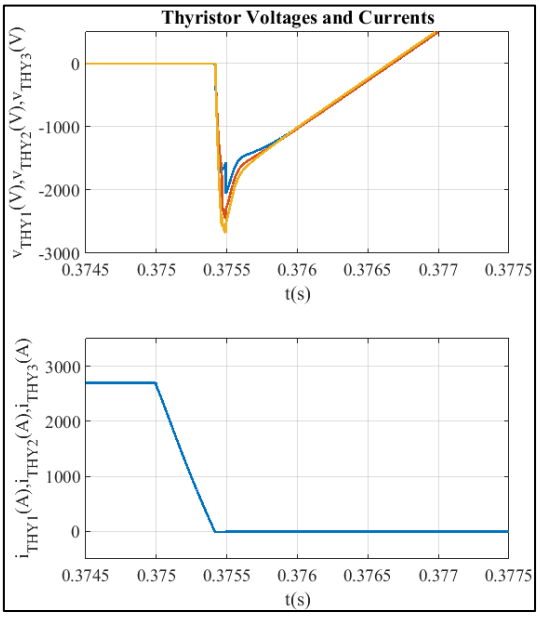


Figure 5-46: Turn-off REAL - Pattern 1 – THY waveforms– zoom

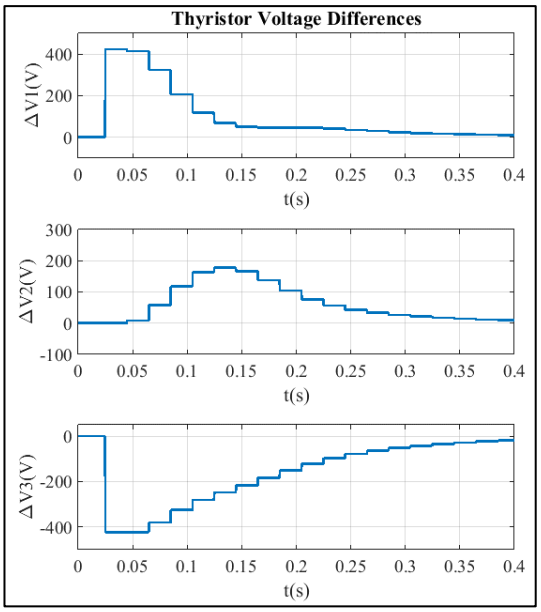


Figure 5-47: Turn-off REAL – Pattern 1 – voltage differences

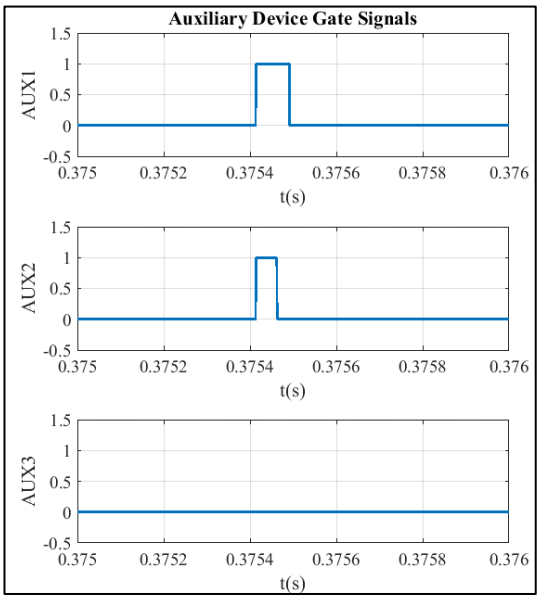


Figure 5-48: Turn-off REAL – Pattern 1 – auxiliary gate signals

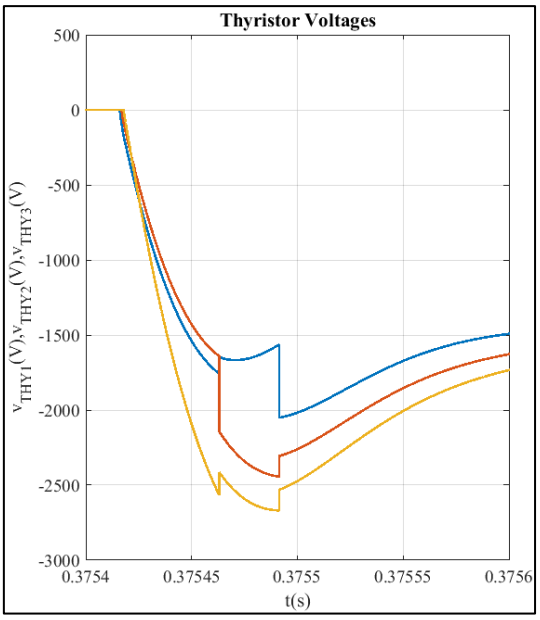


Figure 5-49: Turn-off REAL – Pattern 1 – THY voltages – zoom

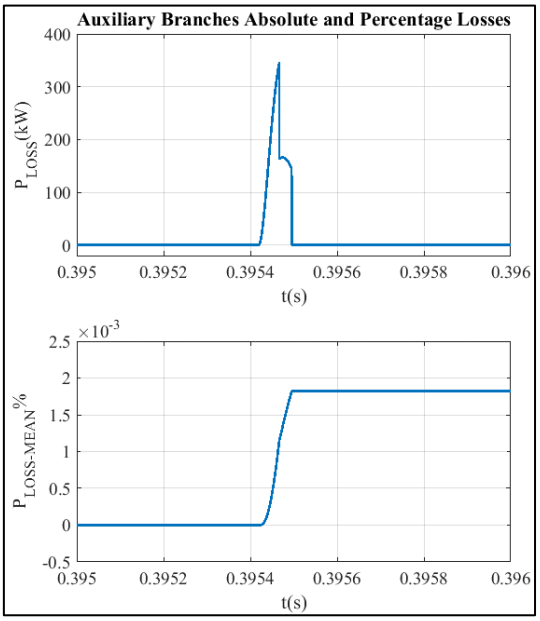


Figure 5-50: Power losses for Pattern 1

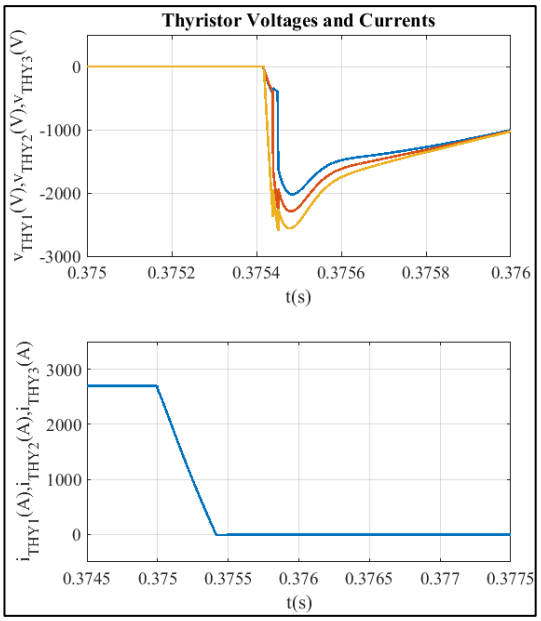


Figure 5-51: Turn-off REAL – Pattern 2 – THY waveforms– zoom

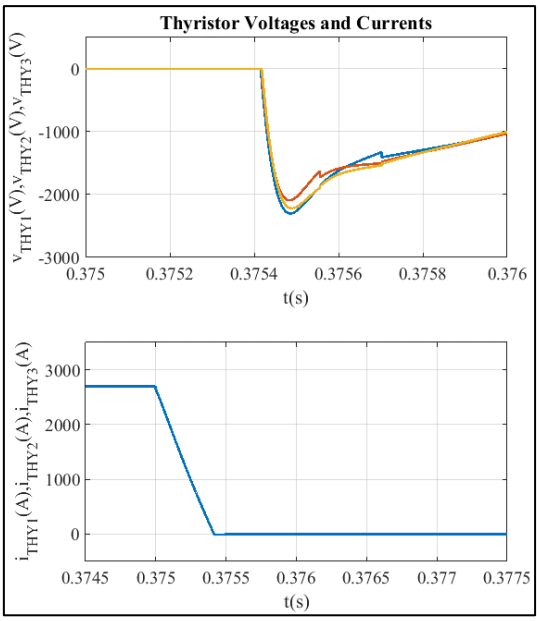


Figure 5-53: Turn-off REAL – Pattern 3 – THY waveforms– zoom

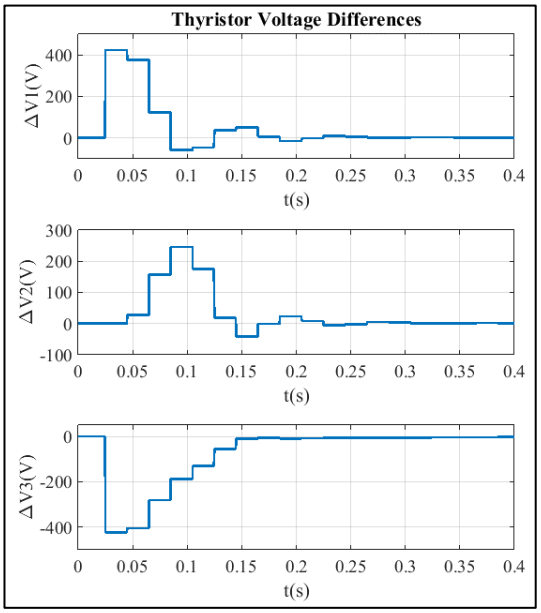


Figure 5-52: Turn-off REAL – Pattern 2 – voltage differences

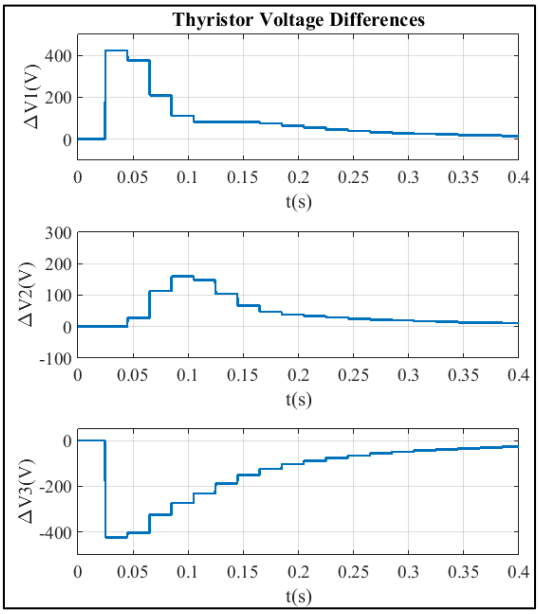


Figure 5-54: Turn-off REAL – Pattern 3 – voltage differences

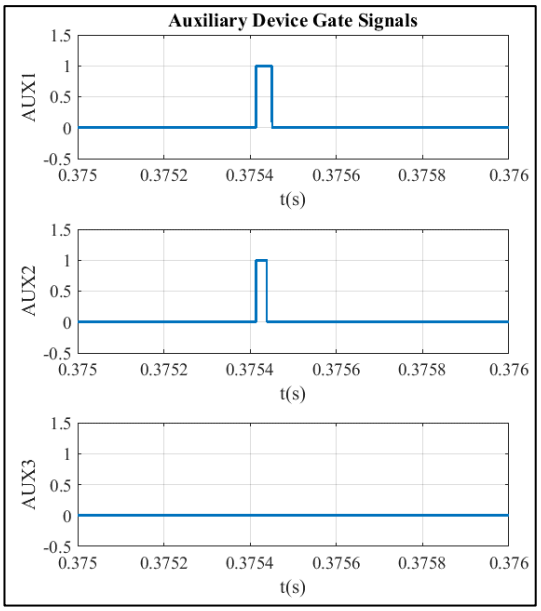


Figure 5-55: Turn-off REAL – Pattern 2 – auxiliary gate signals

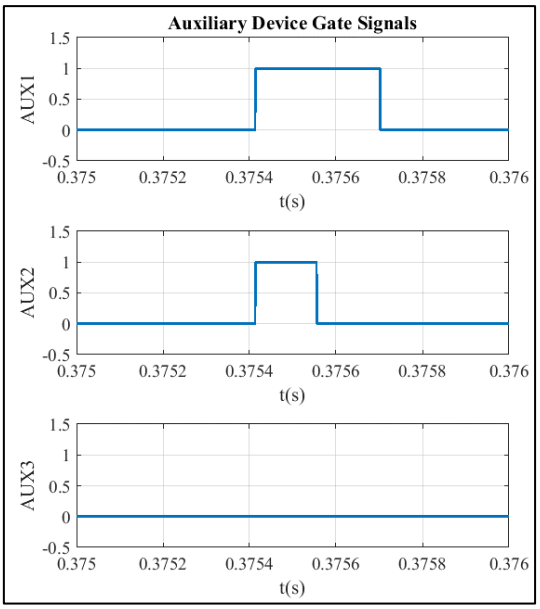


Figure 5-57: Turn-off REAL - Pattern 3 – auxiliary gate signals

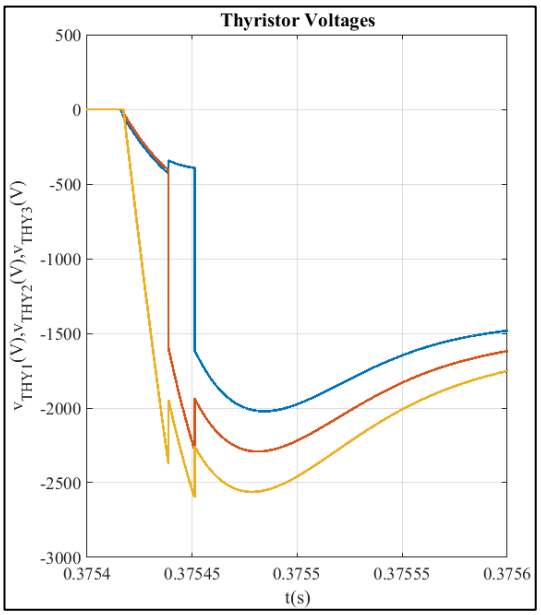


Figure 5-56: Turn-off REAL – Pattern 2 – THY voltages – zoom

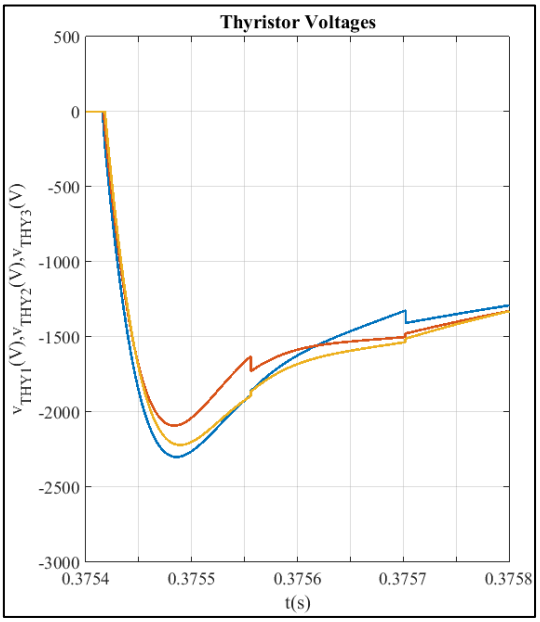


Figure 5-58: Turn-off REAL – Pattern 3 - THY voltages – zoom

Losses for R_{AUX} = 10Ω and for R_{AUX} = 500Ω are represented in Figures 5-59 and 5-60 respectively.

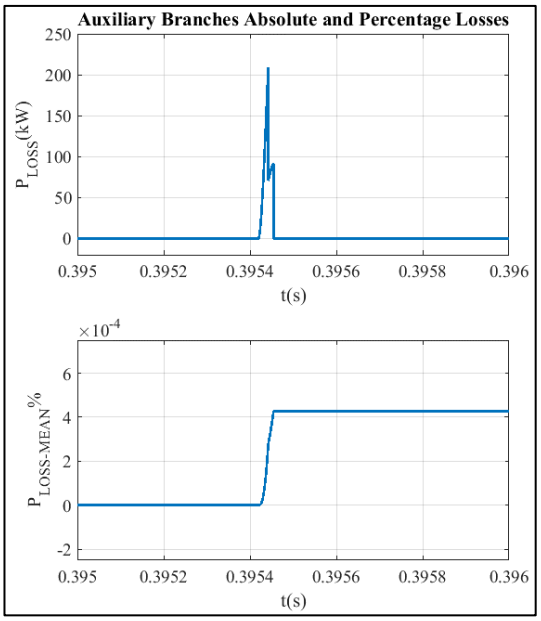


Figure 5-59: Power losses for Pattern 2

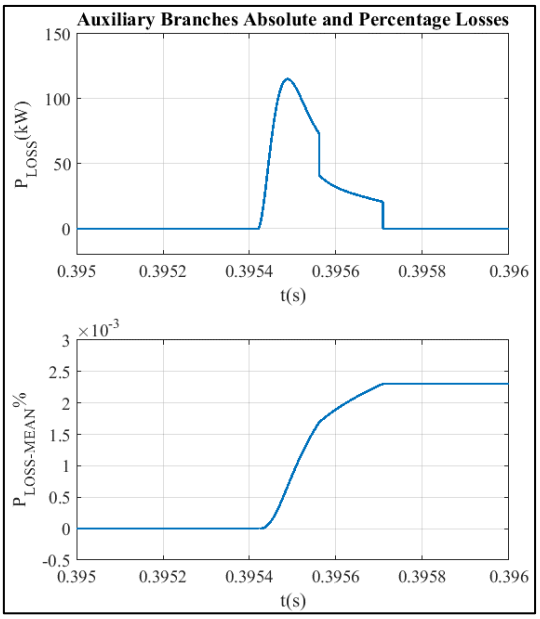


Figure 5-60: Power Losses for Pattern 3

The transmitted power is 35 MW and losses for the three R_{AUX} values are:

R_{AUX} = 10 Ω → P_{LOSS_MEAN} = 150 W

R_{AUX} = 100 Ω → P_{LOSS_MEAN} = 630 W

R_{AUX} = 500 Ω → P_{LOSS_MEAN} = 800 W

The smaller is R_{AUX}, the faster is the compensation process and the more serious are dv/dt stresses, which means that R_{AUX} cannot be chosen below a certain limit. On the contrary, the bigger is R_{AUX}, the slower is the balancing process, the smoother are voltages in terms of dv/dt and the more significant are losses. Ultimately, R_{AUX} must be chosen as a compromise to obtain compensation with reasonable dv/dt stress and acceptable losses.

5.5. Summary

In this chapter, real scale simulations of turn-on and turn-off control methods have been performed.

Concerning the turn-on control method, two main parameters related to each other need to be set correctly, in order to achieve a proper compensation: the diversion time interval and the auxiliary resistance value. Three different patterns are compared and power losses, corresponding to each pattern, are investigated. The main result is that the auxiliary resistance should be chosen as small as possible, compatibly with the current peak, to achieve the quickest compensation process and the smallest power losses.

Concerning the turn-off control method, two different techniques, based on the same physical concept and on the same hardware, are simulated: the “hysteresis” and the “faster device turn-off delay”. Both of them ensure uniform voltage sharing successfully.

The main limit of the “hysteresis” control method is that the steady state error, which depends on voltage thresholds, cannot be eliminated. Four different patterns of auxiliary resistance and voltage thresholds are compared, and the best pattern is the compromise that provide satisfactory steady state error, not causing too many switching events during the compensation process.

The “faster device turn-off delay” method employs a PI controller and it is more complicated than the hysteresis, but more precise. Three different patterns of auxiliary resistance and PI parameters are compared: the best one is the compromise to obtain compensation with reasonable dv/dt stress and acceptable losses.

Simulations in Matlab-Simulink environment give satisfactory results and the chosen model is a valid tool, recommended for further research.

In the next chapter, the experimental test circuit used to validate the proposed control methods, in a reduced scale, is presented.

6. Experimental Test Circuit

To demonstrate the concept on which a compensation method is based, it is possible to make reduced scale experiments, instead of real scale ones, with advantages in terms of safety, cost, speed and flexibility. Reducing the scale, concepts remain the same and numbers change. In general, it is not always possible to establish a rigorous link between real and reduced scale: it depends on the specific experiment. Concerning thyristor valves, a detailed discussion about scaling issues is presented in Sec. 6.1.

An experimental test circuit is set up, to analyse turn-on and turn-off commutations of a thyristor, or a thyristor series, under test. In detail, a single thyristor turn-on commutation is examined to investigate a turn-on active control method, while a thyristor series turn-off commutation is analysed to investigate a turn-off active control method. The realised circuit can be used to test a generic device, not necessarily a thyristor, either doing a double pulse test or turning the device on and off periodically. Details about the two possible operation modes are discussed in Sec. 6.2.

6.1. Link between Real Scale and Experimental Scale

Reduced scale experiments represent the real scale operation rigorously, if there is a link between the two scales.

In real scale, the thyristor valve includes the saturable inductor and the DC grading resistor. In the experimental circuit, the saturable inductor is eliminated, thanks to the turn-on active control employment, while the DC grading resistor is maintained for static voltage control, with no need to be scaled, keeping the real value of 100 kΩ.

The remaining parameters that need to be scaled are the damping capacitance (Cd) and the damping resistance (Rd), which can be scaled depending on the relationship between the real scale and the reduced scale thyristor reverse recovery time.

According to the Alstom Grid experience, if the time constant is about a tenth of the reverse recovery time, the Cd-Rd series combination is properly designed for voltage sharing purpose. The reverse recovery time of the real scale thyristor (DYNEX DCR

3980H85) is, on average, trr = 500 μs: to obtain a time constant τ = 50 μs, the real scale damping parameters commonly chosen are Cd = 1 μF and Rd = 50 Ω.

The reverse recovery time of the reduced scale thyristor (Vishay VS-50RIA80) is, on average, trr = 50 μs: to obtain a time constant τ = 5 μs, one possibility is to reduce Cd ten times and to leave Rd to the same value, according to the need of reducing Cd to shrink the real scale valve. In this case, the reduced scale parameters become:

Cd = 100 nF; Rd = 50 Ω.

To test the effectiveness of the active balancing method and to achieve a further real scale valve size reduction a second pattern is considered, with half Cd and double Rd, maintaining the same τ.

Experimental turn-off tests are ultimately conducted using the following two patterns for the damping parameters with the same time constant, τ = 5 μs.:

- Cd = 100 nF and Rd = 50 Ω;
- Cd = 50 nF and Rd = 100 Ω.

In both real scale and reduced scale, the effective value of the reverse recovery time depends on the forward conduction current, which determines the amount of reverse recovery charge, and on the turn-off current slope (di/dt).

Concerning turn-on tests, it is not necessary to choose a Cd-Rd combination suitable for voltage sharing purposes, especially if turn-on compensation is examined separately from turn-off compensation. Given the need of a current source for the initial current spike to be diverted by the active control system, the pattern Rd = 12 Ω and Cd = 2 μF is chosen. Further discussion follows in Sec. 7.1.

The last parameter that need to be chosen for the experimental test circuit is the commutation inductance (L_{COM}) that, together with the applied voltage, determines the current slope during turn-on and turn-off transitions. In real scale, the commutation inductance depends on the supply inductance (power supply, line and transformer) of the specific application. Three different values are considered for the experiments: one for turn-on tests and two for turn-off tests.

Realistic values for the real scale turn-on are a current slope of 5 A/μs and a time interval of 400 μs to reach 2 kA, while the initial current spike peak is between 1 kA

and 3 kA, with an approximate duration of 10 μs. In reduced scale, the L_{COM} considered for turn-on tests is 4.7 mH, so a forward voltage of 200 V gives a current slope (di/dt) of 35 A/ms and a conduction current of 7 A after 200 μs. According to the Cd-Rd choice for turn-on tests, both the initial peak and its duration are exaggerated (14 A peak and 40 μs duration) to stress the control system as much as possible and to test its robustness.

The two inductances used for turn-off tests are L_{COM} = 0.73 mH and L_{COM} = 9 mH and they are both combined with the two Cd-Rd patterns, giving four possible combinations, as discussed in Sec. 7.2. L_{COM} = 0.73 mH makes the turn-off negative current slope (di/dt) as large as possible, to obtain a turn-off as quick as possible and voltage differences as large as possible. L_{COM} = 9 mH makes current slope about ten times smaller than in the other case, but introduces strong oscillations to test the robustness of the turn-off control system.

The overall aim is to demonstrate that the control methods work regardless of the Cd, Rd, L_{COM} scaling method, i.e. concepts of operation remain valid and developed control systems stay stable in different conditions.

6.2. Experimental Test Circuit Purpose

The experimental test circuit illustrated in Fig. 6-1 is designed to turn the Device Under Test (DUT) on and off and to measure its voltage (and current, if needed) during the on-state, the reverse blocking state, the forward blocking state and during transitions between states. The employment of active control methods to control transitions is investigated according to the block diagram in Fig. 6-2.

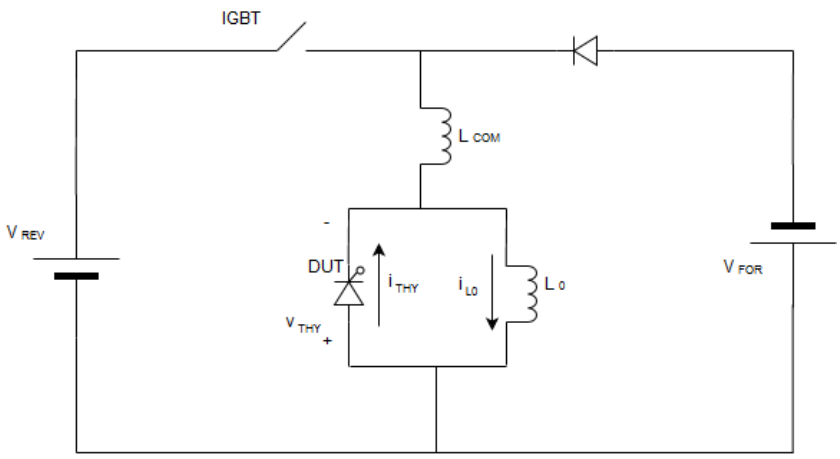


Figure 6-1: Experimental circuit for double pulse test operation

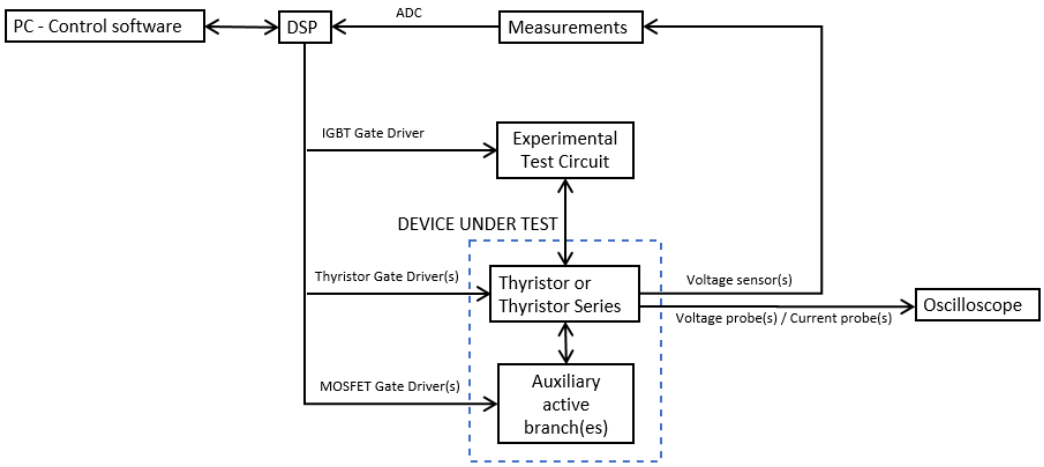


Figure 6-2: Block diagram of experimental test circuit operation

The block diagram illustrated is the most general version: voltage measurements might not be necessary, depending on the active control method to be validated. The presence of auxiliary active branches is considered only in Chap. 7. In the rest of this chapter, the design and operation of the experimental circuit without any active branch will be examined.

Components that realise the experimental test circuit are the following:

- DUT = Device Under Test – single thyristor or thyristor series (plus auxiliary branches)
- V_{REV} = Reverse voltage power supply
- V_{FOR} = Forward voltage power supply
- IGBT = Switch that decides to apply V_{REV} or V_{FOR} on the device
- L_{COM} = Commutation inductance
- L_0 = Inductance to maintain current in the DUT during the forward conduction state

Considering a double pulse test, the operation of the circuit takes place through the following five steps:

1. The IGBT is turned on and current flows through the V_{REV} - L_{COM} - L_0 path until the desired current value for the forward conduction state of the DUT is reached. During this time interval, the equations of interest are:

$$\frac{di_{L0}}{dt} = \frac{V_{REV}}{L_{COM} + L_0} \quad ; \quad v_{THY} = V_{REV} \quad ; \quad i_{THY} = 0 \quad ;$$

2. When the aimed current value for the forward conduction state is obtained, the IGBT is turned off and current flows through the V_{FOR}-L_{COM}-L_0 loop until the DUT is turned on. At this stage, the main equations are:

$$\frac{di_{L0}}{dt} = \frac{-V_{FOR}}{L_{COM} + L_0} \quad ; \quad v_{THY} = V_{FOR} \quad ; \quad i_{THY} = 0 \quad ;$$

3. When the DUT is turned on, the current loop becomes the DUT - L_0 and L_0 behaves as a current source. The time interval between the IGBT turn-off and

the DUT turn-on is as short as possible, to maintain current as close as possible to the value reached at the IGBT turn-off instant. During the DUT conduction, its current decreases according to the DUT on-state voltage, usually negligible compared to the reverse and forward voltage of the test circuit:

$$\frac{di_{L0}}{dt} \cong 0\ (slightly\ negative)\ ;\quad v_{THY} \cong 0\ \ ;\quad i_{THY} = i_{L0}\ \ ;$$

4. The IGBT is turned on again to turn the DUT off and to measure the reverse recovery effect on current and voltage. Equations of interest are the same as step 1.

5. The IGBT is turned off, to extinguish inductors residual current in the V_{FOR} - L_{COM} - L_0 loop. The main equations are the same of step 2, until the current becomes zero and is blocked by the diode.

Depending on the experiment, a double pulse test might be a limit. For example, it cannot show the dynamic of the "turn-off delay" control method, which takes a certain number of cycles before reaching the steady state. This limit can be overcome replacing V_{FOR} power supply with a RC parallel, as in Fig. 6-3, and repeating steps 1, 2 and 3 periodically. Once the period and the IGBT duty cycle are fixed, the circuit behaves like a buck-boost converter, except for the presence of the DUT branch.

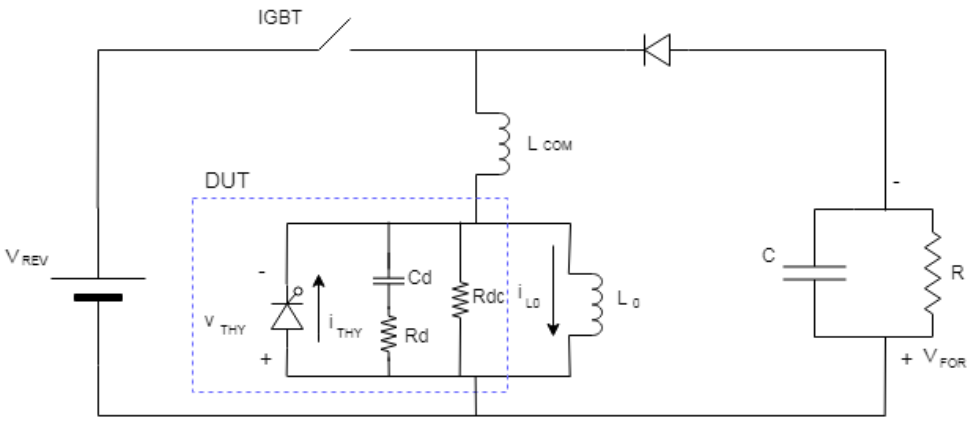


Figure 6-3: Experimental test circuit for periodic operation

The voltage gain V_{FOR} /V_{REV} depends on the load resistance "R" and on the IGBT duty cycle. In both simulations and experiments, there are no specific requirements to use different values for V_{FOR} and V_{REV} so, for convenience, the gain is maintained around 1.

Results of a simulation in Matlab-Simulink environment, using parameters below, are illustrated in Fig 6.4.

- V_{REV} = 100 V
- L_{COM} = 0.18 mH, with a parasitic resistance of 0.1 Ω
- L_0 = 4.7 mH, with a parasitic resistance of 0.3 Ω
- C = 7.5 mF
- R = 250 Ω
- Rd = 50 Ω, Cd = 1 μF
- T = 3 ms – f = 333 Hz
- IGBT duty cycle = 13%
- Phase delay between IGBT turn-off and DUT turn-on = 0.6 ms

The described experimental circuit is operated periodically, at a 3 ms period, which corresponds to a 333 Hz frequency, for both turn-on and turn-off tests. The reason behind the choice is referred to the case of the maximum reverse voltage applied of 600 V: with an IGBT duty cycle of 13% and a commutation inductance is 4.7 mH, the IGBT stays on for 0.39 ms and the reached current is 50 A in the V_{REV} – IGBT - L_{COM} - L_0 loop, while the device is in the reverse blocking state. Then, with a phase delay of the DUT of 0.6 ms before turn-on, the device stays in the forward blocking state for 0.21 ms, while current passes through the L_{COM}-L_0-V_{FOR}-diode loop. For the remaining part of the period, which duration is is 2.4 ms, the device remains in the on-state, conducting the current in the DUT - L_0 loop.

Experimental results are discussed in Sec. 6.4. Discrepancies between simulation results and experiments are related to the estimation of inductor parasitic resistances, which is not straightforward. If simulations do not consider inductors parasitic resistances, the simulation voltage gain is higher than the experimental one. Nevertheless, for our purposes, tolerance on V_{FOR} /V_{REV} ratio is not very strict, so tolerances on "R" and IGBT duty cycle are not severe. In addition, if duty cycles are chosen using a DSP, their variation is very quick and V_{FOR} /V_{REV} ratio adjustments do not require many simulations.

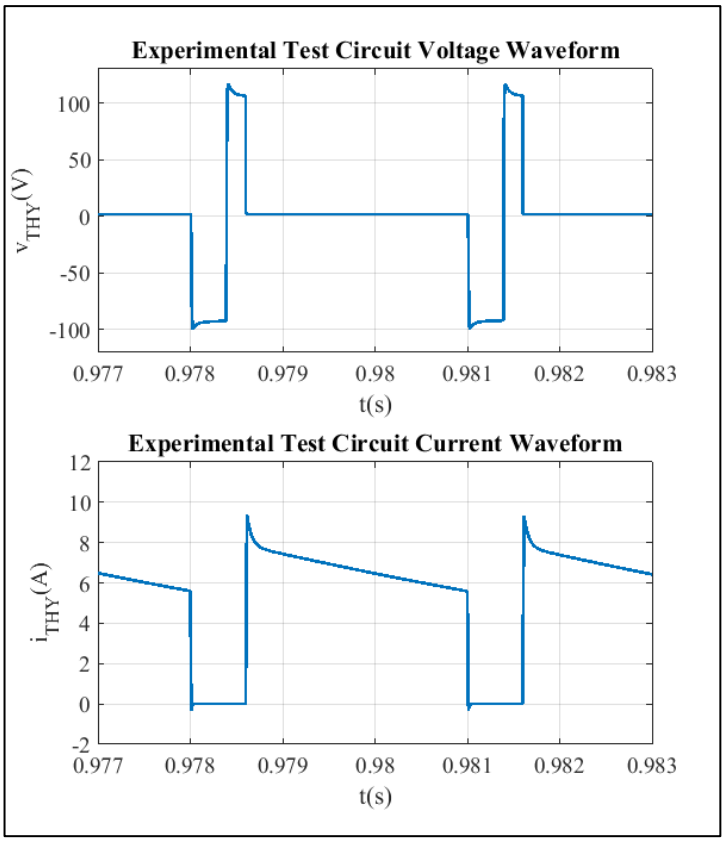


Figure 6-4: Simulation results for the experimental test circuit

In conclusion, the main advantage of operating the experimental test circuit periodically instead of in double pulse test mode, is the possibility of testing active control methods that present a certain dynamic before reaching the steady state. Other advantages are the need of only one power supply, instead of two, and the possibility of varying the relationship between V_{FOR} and V_{REV} by just modifying the IGBT duty cycle in the DSP code.

6.3. Experimental Test Circuit Design

V_{REV} power supply is realised according to the electrical scheme in Fig. 6-5, employing the components in Fig. 6-6.

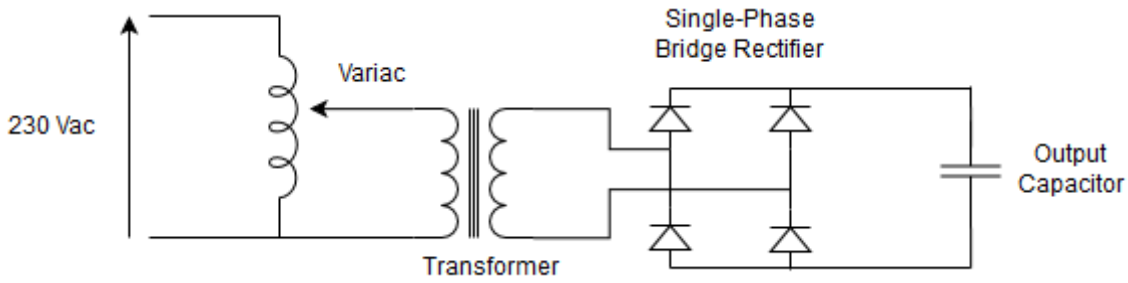


Figure 6-5: Power supply - Electrical scheme

The Variac output can reach 270 V_{RMS} (380 V_{MAX}) and it is connected to the transformer low voltage terminals, to increase the bridge rectifier input voltage by a factor 400/230 ≈ 1.7. Therefore, the power supply output voltage can be varied between a minimum of 0 V and a maximum of 650 V. The maximum voltage is reduced to about 600 V in practice, due to resistive losses, not considered in the ideal case.

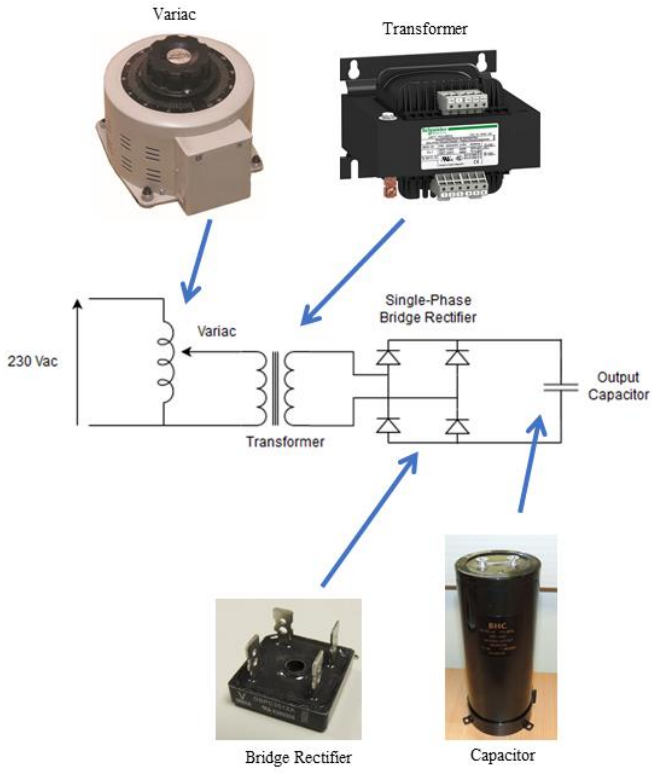


Figure 6-6: Power supply - Components

Components that realise the power supply are the following:

- Variac: Carroll & Meynell CMV 20E, 20 A, 4.8 kVA, 0 → 270 Vac
- Transformer: Schneider Electric ABT7 PDU250G, 230/400V ±15V, 2.5 kVA
- Bridge Rectifier: Vishay VS-GBPC 3512A, 35 A, 1200 V
- Output Capacitor: BHC 15 mF, 450 VDC, two in series

If double pulse tests need be done, two identical and independent power supplies are necessary. The two output voltages are independent only if there is no interaction, i.e. if the circuit does not behave as a buck-boost, in which one of the two output voltages is controlled by the circuit instead of the Variac. On the contrary, operating the experimental test circuit as a buck-boost, it is not necessary to duplicate the V_{REV} power supply structure and V_{FOR} power supply can be realised using the output capacitor and a load resistor in parallel. The periodic operation is the one of interest for the experimental tests conducted and the overall experimental test circuit for this case is realised using the components in Fig. 6-7.

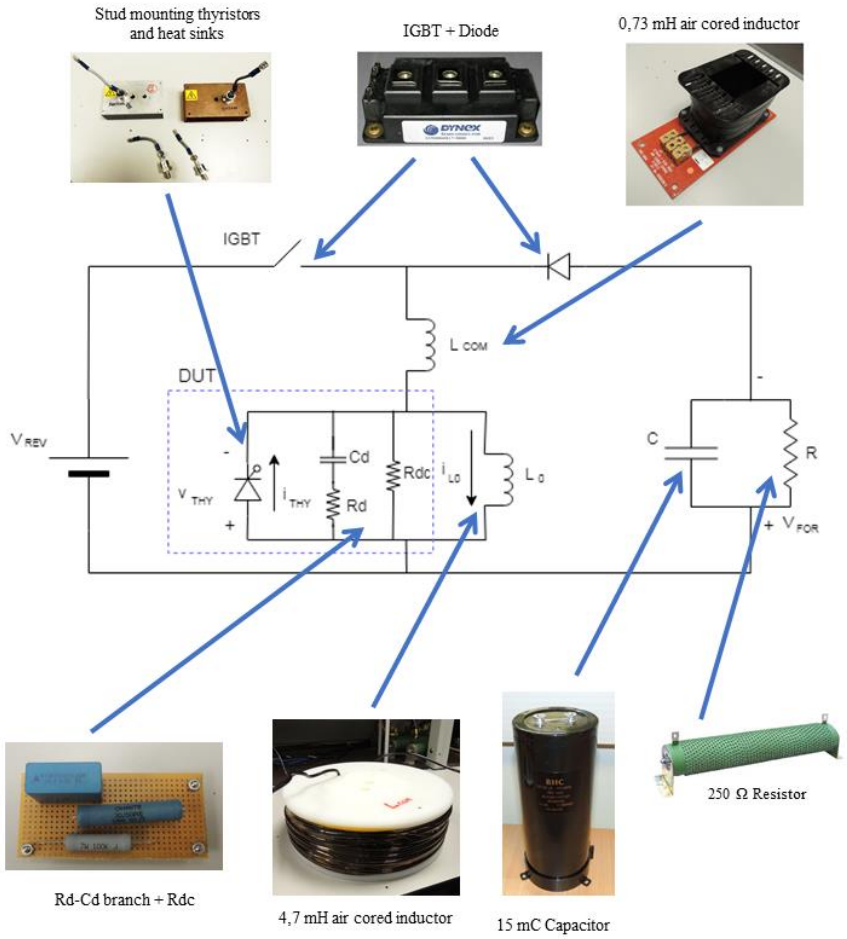


Figure 6-7: Experimental test circuit for periodic operation- Components

The chosen load resistor has a resistance of 250 Ω and it is realised by a parallel of four 1 kΩ resistors, 200W each, for a total power of 800 W and a maximum voltage of 450 V. A higher voltage can be applied for tests that do not run for a long time.

The IGBT and the diode are included in a half bridge module: the selected one is the Dynex DIM200WHS17-A000, 1.7 kV, 200 A.

In order to avoid saturation issues, air cored inductors are used. For L_0, a 4.7mH value is always used, whereas for L_{COM}, a 0.73 mH, a 4.7 mH or a 9 mH value is selected, depending on the test. The employed 9 mH is obtained connecting one 4.7 mH inductor in series to six 0.73 mH inductors. The 4.7mH, 80A, air cored inductor design is described in Appendix E.

The DUT, that is a single thyristor or a thyristor series string, depending on the test, is chosen from the pattern of stud mounting thyristors in Table 6.

Model	Voltage Rating (V)	Current Rating (A)
Multicomp 2N690	600	25
Semikron SKT50/16 E	1600	50
IXYS CS35-12IO4	1200	69
Vishay VS-50RIA20	200	50
Vishay VS-50RIA60	600	50
Vishay VS-50RIA80	800	50
Vishay VS-50RIA120	1200	50

Table 6: Pattern of stud mounting thyristors used for experimental tests

Finally, the damping capacitor, the damping resistor and the DC grading resistor are through-hole components mounted on a stripboard.

6.4. Experimental Test Circuit Operation

Turn-on and turn-off test results when no active circuits are employed, are illustrated for the Vishay VS-50RIA80, 800V, 50A.

A turn-on test of a single thyristor is shown in Fig. 6-8. The active control aim will be to divert the initial current spike, as discussed in Sec. 5.1 (real scale simulations) and 7.1 (reduced scale experiments and simulations).

Turn-off tests of a single thyristor and of two thyristors in series are depicted in Fig. 6-9 and Fig. 6-10 respectively. When testing two thyristors in series, the electrical circuit is the one showed in Fig. 6-11.

Different Qrr of two Vishay VS-50RIA80 from the same batch results in non-uniform voltage sharing after turn-off. The active control objective will be to obtain voltage balancing, as discussed in detail in Sec. 5.2, 5.3 (real scale simulations) and 7.2 (reduced scale experiments and simulations).

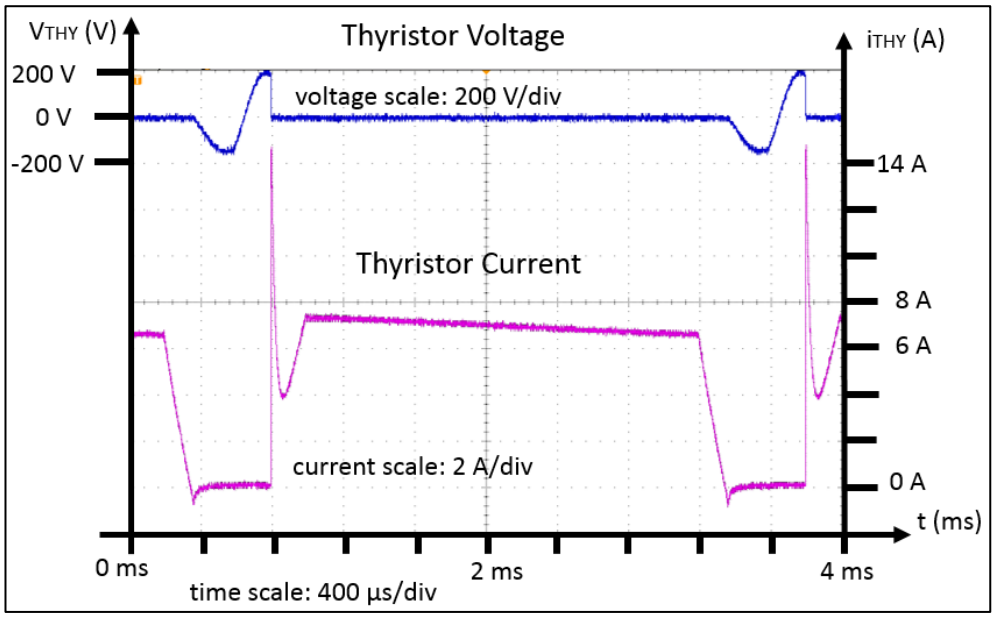


Figure 6-8: Reduced scale Turn-on test

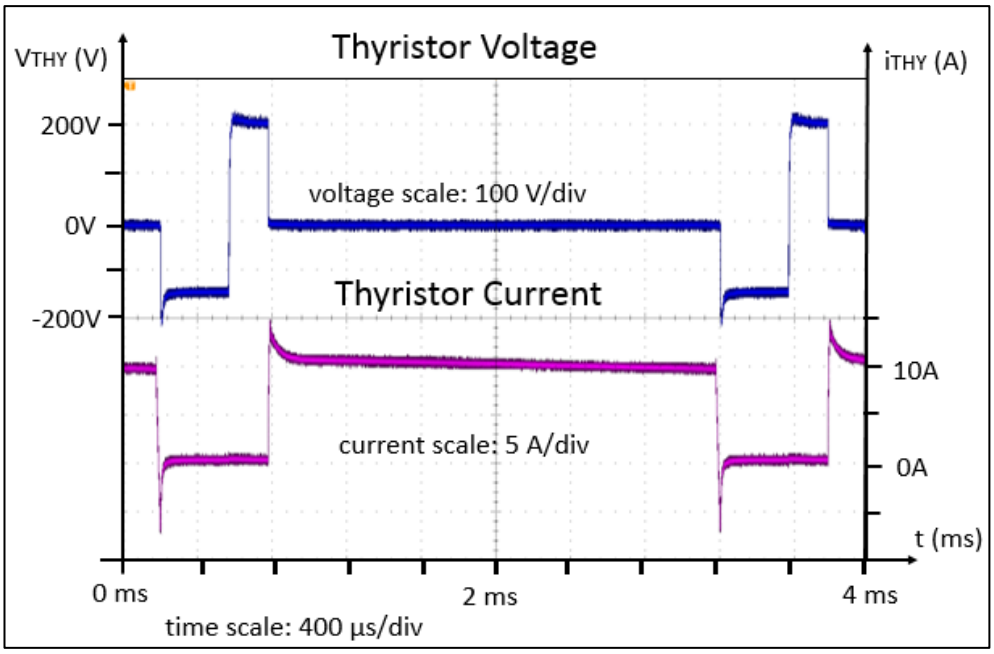


Figure 6-9: Reduced scale Turn-off test – single thyristor

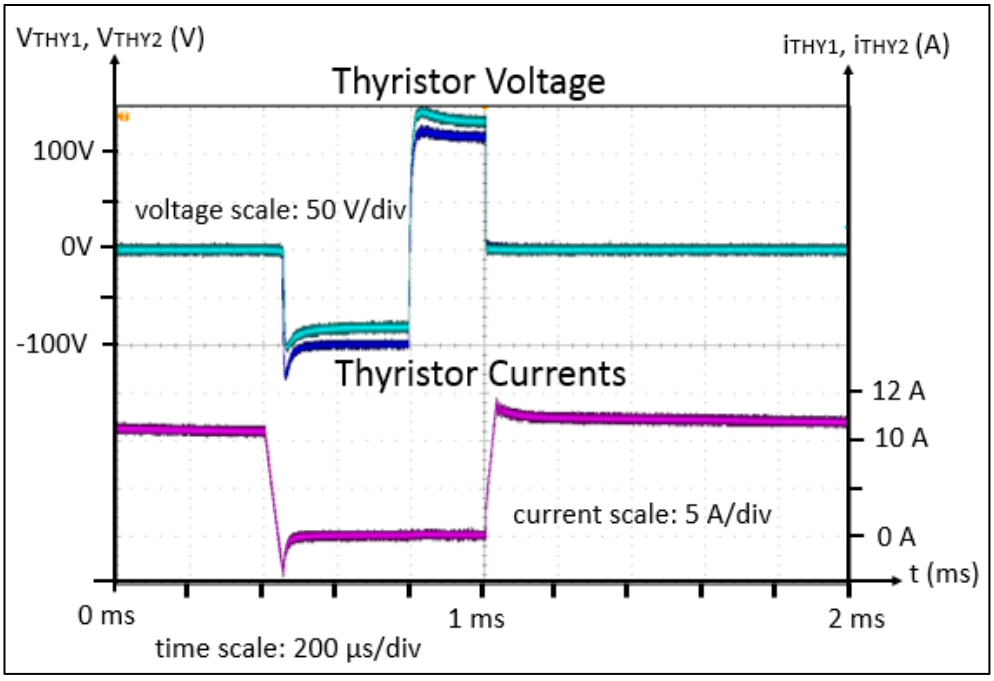


Figure 6-10: Reduced scale Turn-off test – two thyristors in series

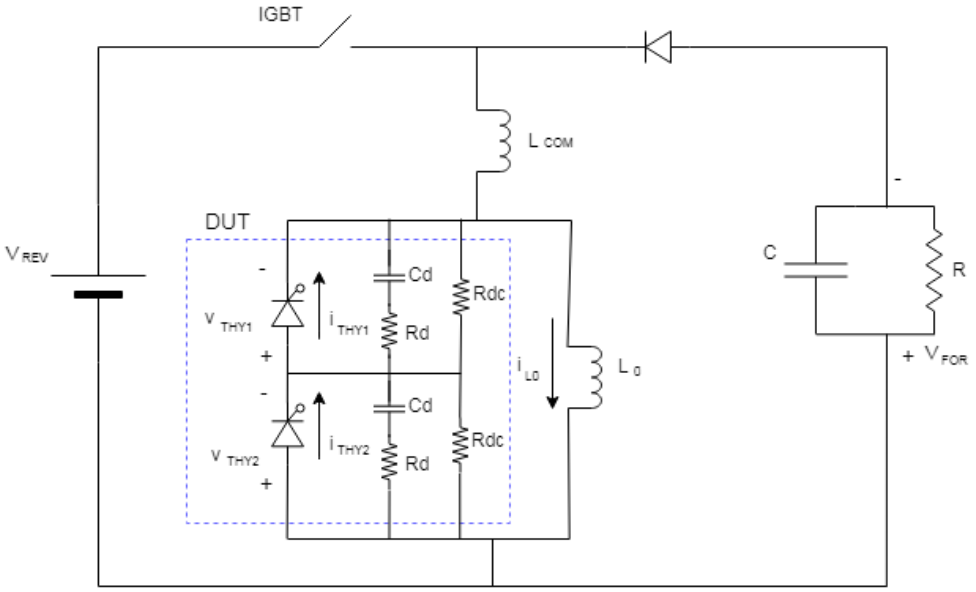


Figure 6-11: Experimental test circuit for testing two devices in series

6.5. Summary

In this chapter, the purpose, the design and the operation of an experimental test circuit are discussed. Such a circuit is realised in a reduced scale, for flexibility and cost reasons.

At first, the link between the real scale and the experimental scale is examined. The considered system is not perfectly scalable, because it is not possible to scale all the parameters at the same time but, the control methods of interest can be tested even without total scaling.

The purpose of the reduced scale test circuit is to turn the Device Under Test (DUT) on and off periodically, to demonstrate the effectiveness of the investigated auxiliary active circuits, during turn-on and turn-off transitions. A sample simulation has been performed.

The design of the experimental circuit has been explained in detail, providing also a list of the stud-mounting thyristors employed in the DUT.

The operation of the designed circuit is correct, as experimental results match the sample simulation. Experimental waveforms show a current spike to be diverted during turn-on and a voltage imbalance after turn-off for devices in series with different reverse recovery charge.

In the next chapter, experimental results for turn-on and turn-off active control methods are presented and scaling-up issues are discussed as well.

7. Experimental Results

Experimental results for turn-on and turn-off tests, are discussed in Sec. 7.1 and Sec. 7.2 respectively. For each test, experimental waveforms are represented beside simulation waveforms, to show that experiments confirm the theory and that every time a parameter needs to be modified, quick and reliable results can be obtained from simulations, before setting up a new experiment.

7.1. Turn-on Control Method

The turn-on active control method is tested using the experimental circuit shown in Fig. 6-3 and considering the DUT represented in Fig. 7-1. The device used as the auxiliary switch is a MOSFET.

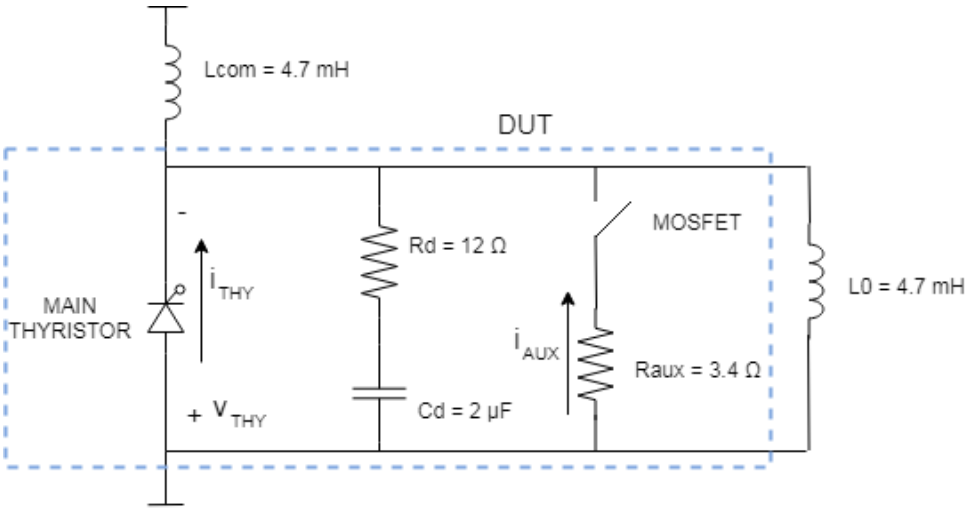


Figure 7-1: Device Under Test used for turn-on control experiments

The current spike in the first part of the turn-on transient is obtained using the following damping parameters: Rd = 12 Ω; Cd = 2 µF. This pattern does not provide enough damping during turn-off, which is not an issue as experiments are focussed on turn-on. For the auxiliary resistance, the chosen value is R_{AUX} = 3.4 Ω.

The commutation inductance is L_{COM} = 4.7 mH so, if forward voltage is 200 V, current slope is about 40 A/ms. As discussed in Sec. 6.1, it is not possible to rigorously scale all parameters of a thyristor valve. Each parameter is scaled depending on the specific test: for turn-on test, the L_{COM} chosen value is correctly scaled, but Cd and Rd are not.

The spike shape achieved with the listed parameters is slightly different from the real scale case but, in percentage terms, it has approximately the same time duration and the same overshoot, which are the most important features to be represented in the reduced scale. It is actually not important to demonstrate that the exact current shape of the real scale can be diverted using the actively controlled branch, but it is essential to prove that, using the proposed method, any current shape at the initial stage of the turn-on process can be carried by an auxiliary component, instead of the main thyristor.

If there is no compensation, i.e. if the auxiliary branch is never turned on and the initial current spike is not diverted, experimental results and simulations are represented in Fig.7-2 and 7-4 respectively.

If compensation is introduced, waveforms are displayed in Fig. 7-3 and 7-5. The thyristor turn-on gate signal is delayed by the same amount of the auxiliary device turn-on time interval, which is 80 μs, so the thyristor turn-on occurs 80 μs later than in the no-compensation case. As said for the case of a large thyristor, the auxiliary branch should be kept on for a time interval slightly longer than the delay, to help to clamp the voltage across the thyristor during the spreading phase, even though di/dt limitations are unlikely to affect the small thyristors used in the experiments.

Current in the auxiliary active branch is shown in Fig. 7-6 and Fig. 7-7 and it is approximately the current spike of the first part of the turn-on transient, successfully diverted.

Both simulations and experimental results show the same waveforms, i.e. experiments confirm simulation results previously found and demonstrate that the investigated method can be used in the real valve.

Note: In captions, “reduced scale” becomes “REDUCED”, experimental is “EXP”, simulation is “SIM”, main thyristors are addressed as “THY” and the words “auxiliary branch” become just “AUX”.

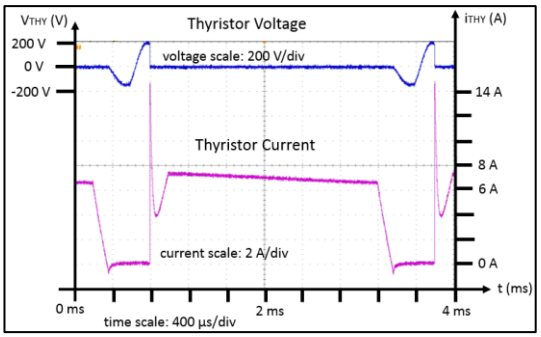


Figure 7-2: Turn-on REDUCED – no compensation – EXP results

Consequently to the chosen parameters, the current peak to be diverted is more than 100% bigger than the on-state current.

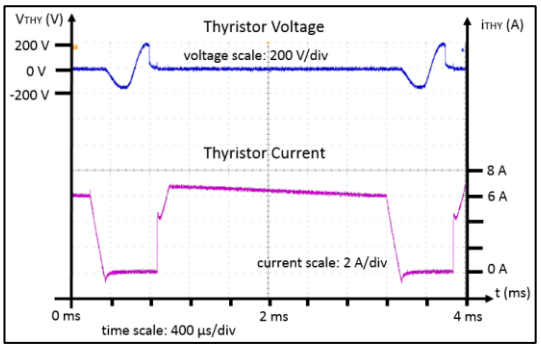


Figure 7-3: Turn-on EXP - RAUX=3.4 Ω, Δt=80 µs – THY waveforms

Once the initial peak is cut off, the rest of the current wave shape is not affected by the compensation process.

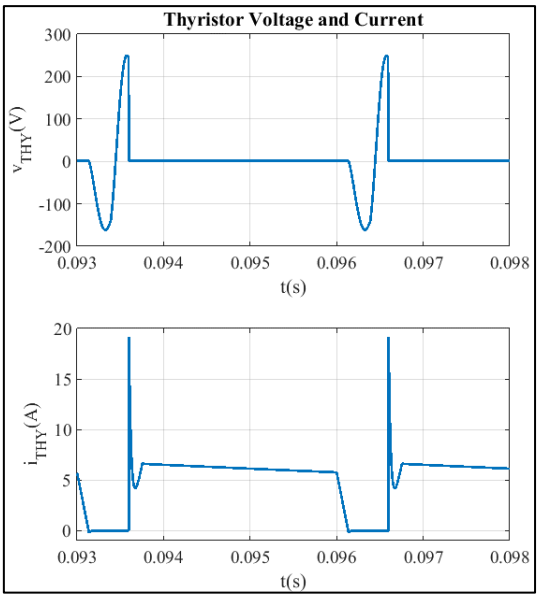


Figure 7-4: Turn-on REDUCED – no compensation – SIM results

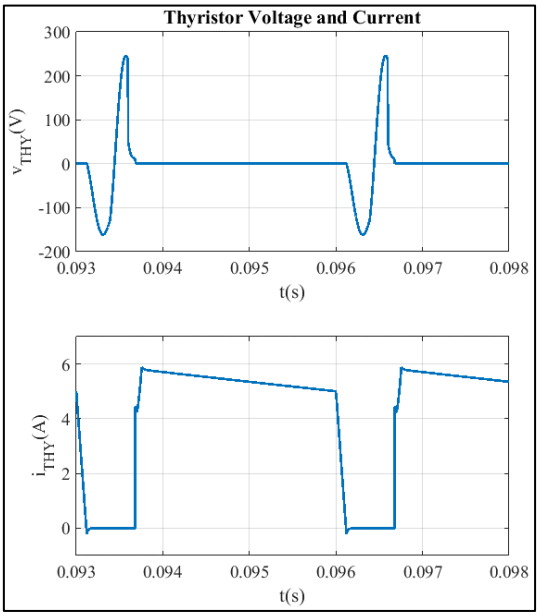


Figure 7-5: Turn-on SIM - R_{AUX}=3.4 Ω, Δt=80 µs – THY waveforms

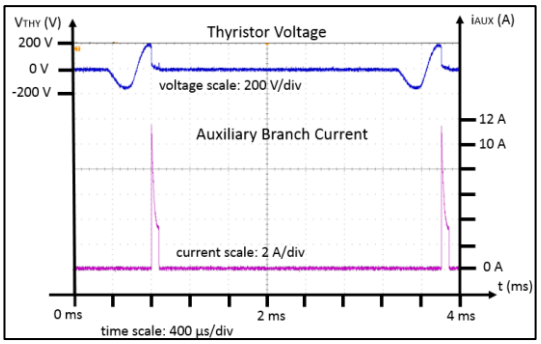


Figure 7-6: Turn-on EXP - RAUX=3.4 Ω, Δt=80 µs – AUX waveforms

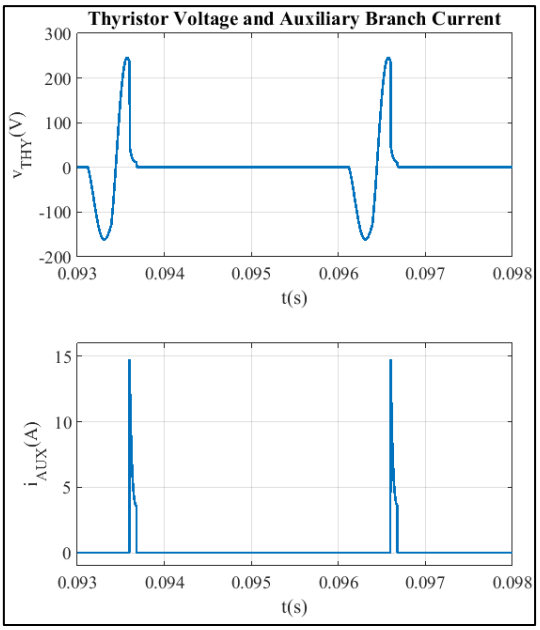


Figure 7-7: Turn-on SIM - RAUX=3.4 Ω, Δt=80 µs – AUX waveforms

The diverted current peak maintains the wave shape that it had before diversion.

The turn-on compensation can be examined setting a smaller time scale, in order to get more detailed graphs of current peak diversion. Waveforms in Fig. 7-8 and 7-9 show the case without compensation, as in Fig. 7-2 and Fig.7-4, but zoomed. Fig. 7-10 and 7-12 show the case with compensation and, finally, Fig. 7-11 and 7-13 show the auxiliary branch waveforms.

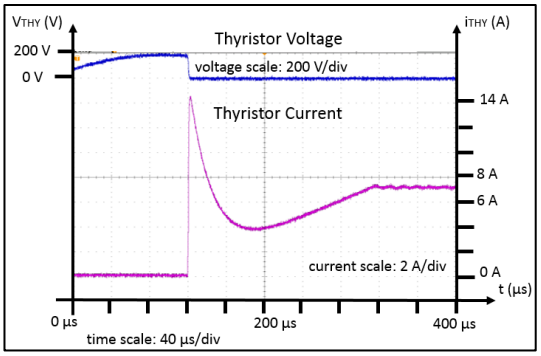


Figure 7-8: Turn-on REDUCED – no compensation – EXP results - zoom

The rate of rise of current is much lower after the Rd-Cd branch discharge.

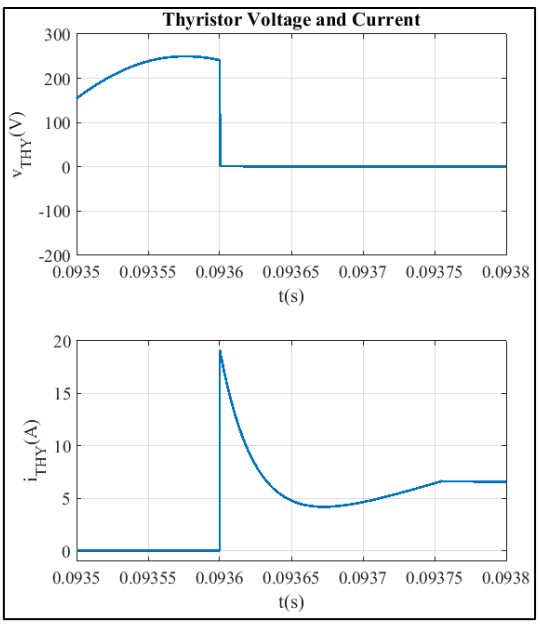


Figure 7-9: Turn-on REDUCED – no compensation – SIM results - zoom

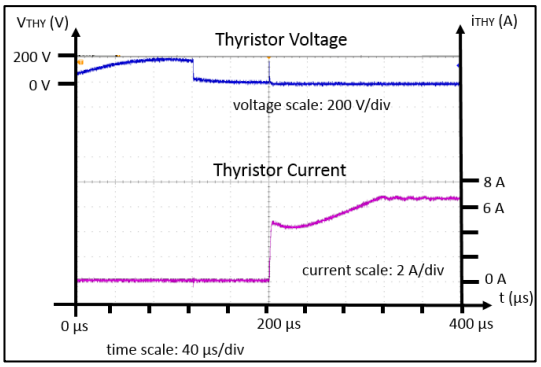


Figure 7-10: Turn-on EXP - RAUX=3.4 Ω, Δt=80 µs – THY waveforms – zoom

The compensation time interval has to be long enough to avoid having any residual part of the initial current peak, that might damage the main thyristor.

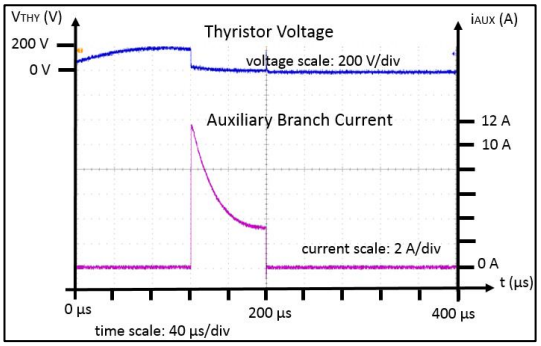


Figure 7-11: Turn-on EXP - RAUX=3.4 Ω, Δt=80 µs – AUX waveforms – zoom

The current peak value in the auxiliary branch is slightly lower than the not diverted one, because of the auxiliary resistance. The lower is R_{AUX}, the smaller is the difference.

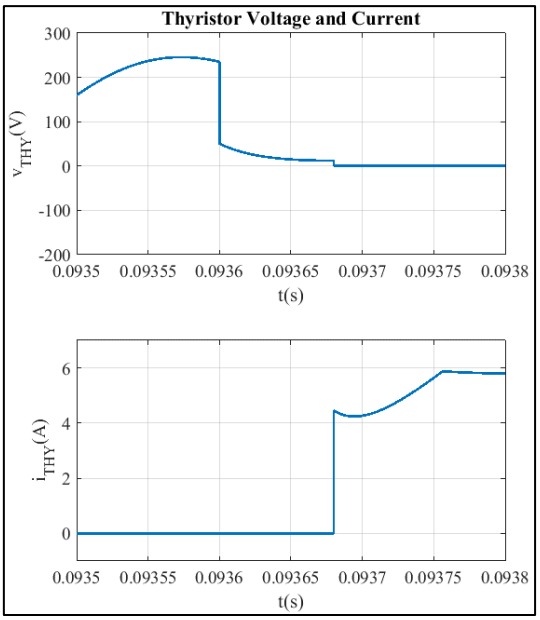


Figure 7-12: Turn-on SIM - R_{AUX}=3.4 Ω, Δt=80 µs – THY waveforms – zoom

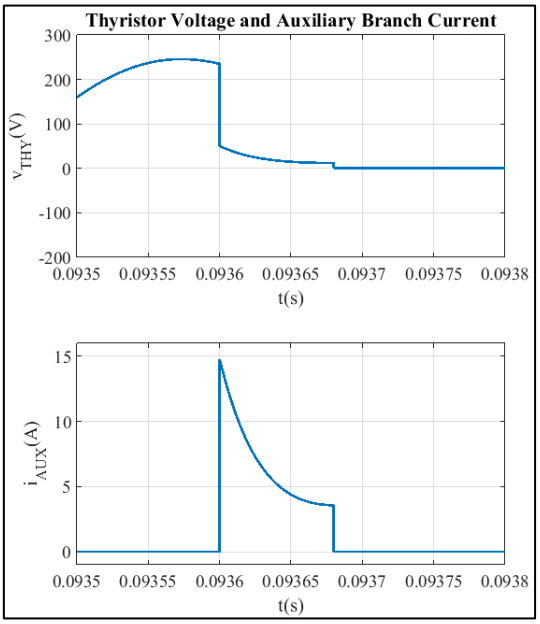


Figure 7-13: Turn-on SIM - R_{AUX}=3.4 Ω, Δt=80 µs – AUX waveforms – zoom

7.2. Turn-off Control Method – "Faster Device Turn-off Delay"

Experimental tests are only about the "Faster Device Turn-off Delay" because the Hysteresis one is easier to be implemented and it is based on the same physical principle, so if the "Turn-off Delay" works, also the hysteresis does. The synchronisation of the "Turn-off Delay" with the current zero crossing is ideal. In the experiments the compensation process is synchronised with the reverse voltage application, but this is possible only because the DSP signal, that decides to apply the blocking voltage, is available and it can be used also to start applying the "Delay". This is not possible in the real converter, for which reverse voltage is externally applied, and frequency is not exactly 50 Hz: for this reason, it is necessary to employ a Rogowski probe (see more detailed discussion in Sec. 7.3) which detects negative di/dt as soon as reverse voltage is applied. The time interval between di/dt starts being negative and negative current zero crossing (beginning of the reverse recovery process) is the offset of the control system and it makes the PI transient longer. From an electrical point of view, there is no problem if the auxiliary switch is turned on when the main thyristor is still conducting. It has no effect until the reverse recovery process starts, because R_{AUX} is connected in parallel to a short circuit until current becomes negative.

The DUT used to validate the turn-off control method with the experimental test circuit in Fig. 6-2, is shown in Fig. 7.14. Once the faster device is identified, only one auxiliary branch is connected, because the other one would never be activated by the control system. Therefore, i_{AUX} in the waveforms below is always the current in the auxiliary device in parallel to the faster thyristor. In a real application, with a generic number of devices in series, none of the auxiliary devices can be disconnected, to achieve effective voltage balancing.

The only parameter that does not change for all the experiments is the L_0 inductance, which is always 4.7 mH. On the other hand, the pattern L_{COM}, Cd, Rd, R_{AUX}, is varied to investigate the control method operation in different conditions, in terms of compensation speed, overshoot and voltage steps (dv/dt). All the investigated patterns are listed in Table 7.

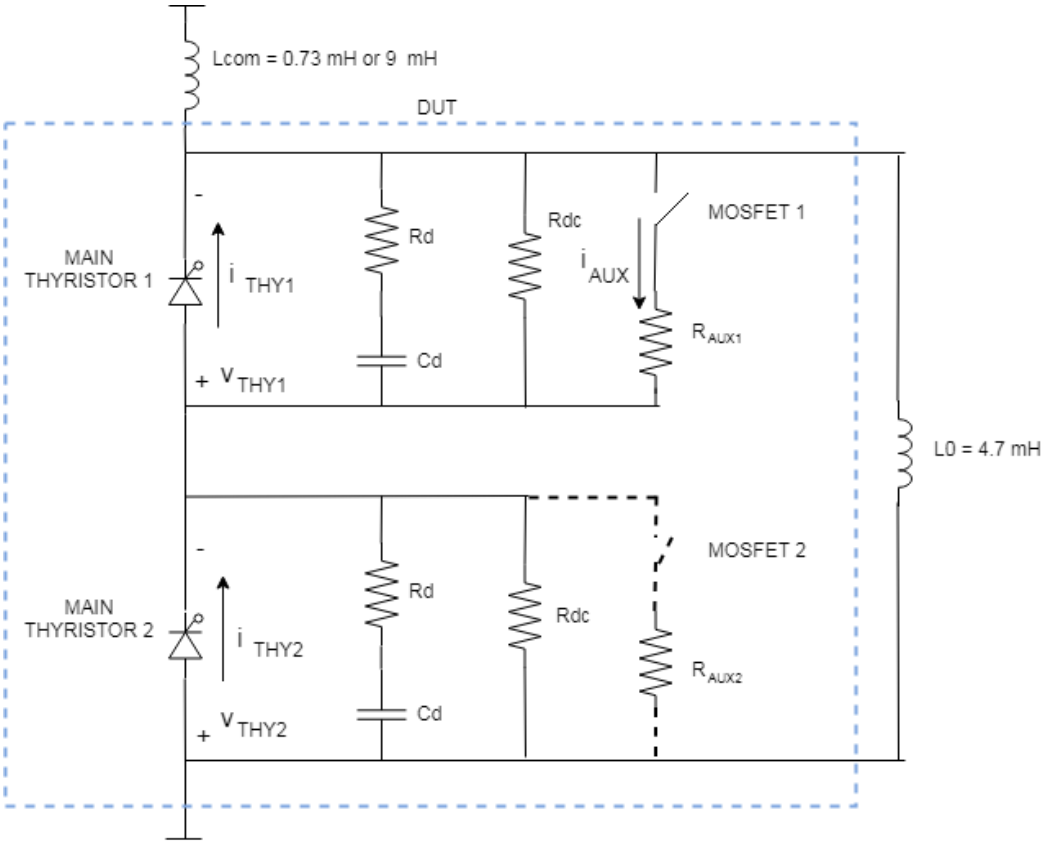


Figure 7-14: Device Under Test used for turn-off control experiments

PATTERN	L_{COM}	Cd	Rd
1	0.73 mH	100 nF	50 Ω
2	0.73 mH	50 nF	100 Ω
3	9 mH	100 nF	50 Ω
4	9 mH	50 nF	100 Ω

Table 7: Parameter patterns for reduced scale turn-off experiments and simulations

Voltage and current experimental waveforms for L_{COM} = 0.73 mH, Cd = 100 nF, Rd = 50 Ω (Pattern 1) and no compensation are displayed in Fig. 7-15, while simulation results for the same pattern are shown in Fig. 7-17.

Reverse recovery charge values set in simulations are:

Qrr1 = 290 µC, Qrr2 = 330 µC → ΔQrr = 40 µC

Note: In captions, "reduced scale" becomes "REDUCED", experimental is "EXP", simulation is "SIM", main thyristors are addressed as "THY" and the words "auxiliary branch" becomes just "AUX".

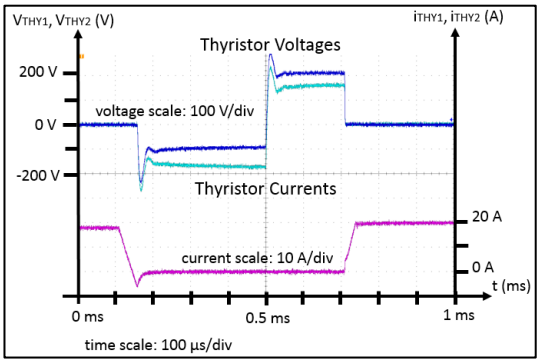


Figure 7-15: Turn-off REDUCED – no compensation – EXP results – Pattern 1

A zoom on the turn-off time interval is depicted in Fig. 7-16, while the relevant simulation is shown in Fig. 7-18.

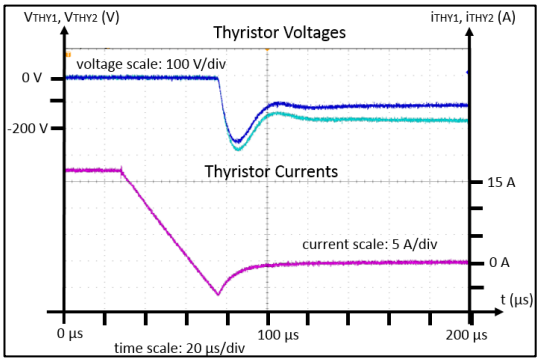


Figure 7-16: Turn-off REDUCED – no compensation – EXP results – Pattern 1 – zoom

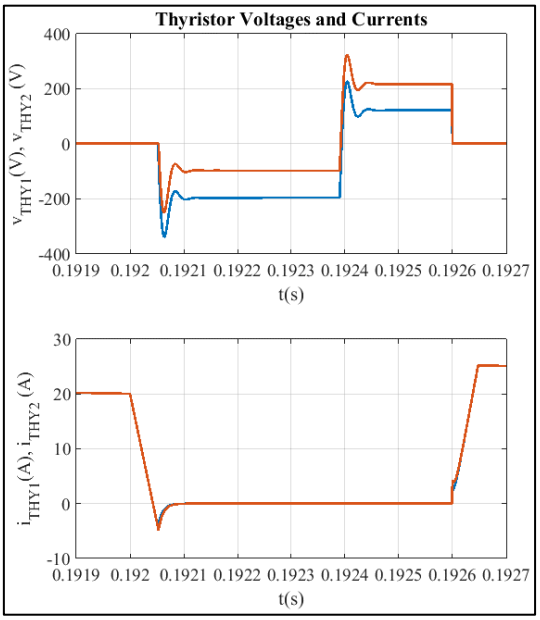


Figure 7-17: Turn-off REDUCED – no compensation – SIM results – Pattern 1

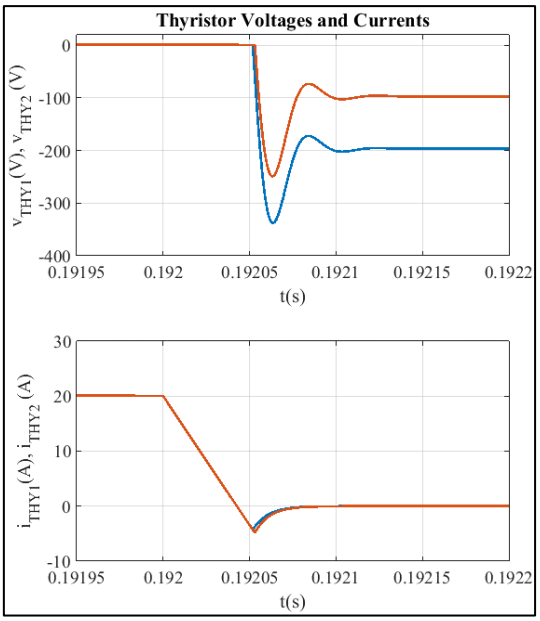


Figure 7-18: Turn-off REDUCED – no compensation – SIM results – Pattern 1 – zoom

Experimental waveforms for compensation with a 10 Ω R_{AUX} are illustrated in Fig. 7-19, while simulation ones in Fig. 7-21. Zooms on the turn-off time interval for experiment and simulation are shown in Fig. 7-20 and 7-22 respectively.

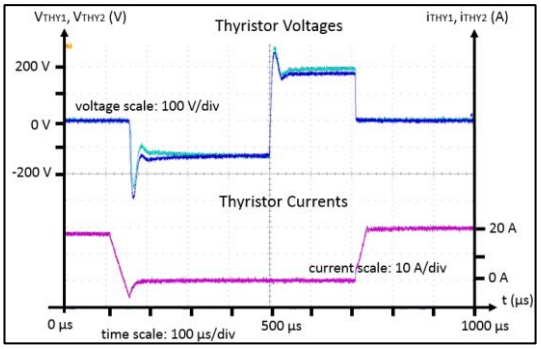


Figure 7-19: Turn-off REDUCED – RAUX = 10 Ω – EXP results – Pattern 1

The experimental results confirm the simulations. This makes simulation a very useful tool to investigate different patterns, without the need of making a new experiment every time that a parameter is modified.

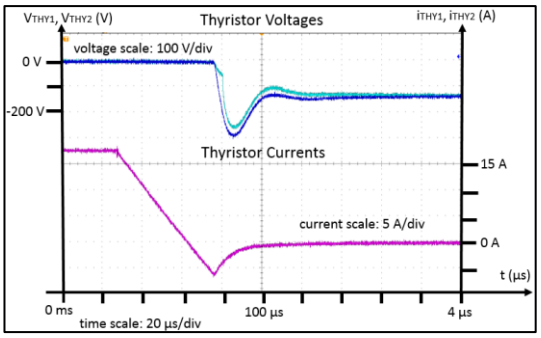


Figure 7-20: Turn-off REDUCED – RAUX = 10 Ω – EXP results – Pattern 1 – zoom

The faster thyristor voltage waveform, affected by the compensation, shows a dangerous step, i.e. a high dv/dt, as soon as compensation terminates.

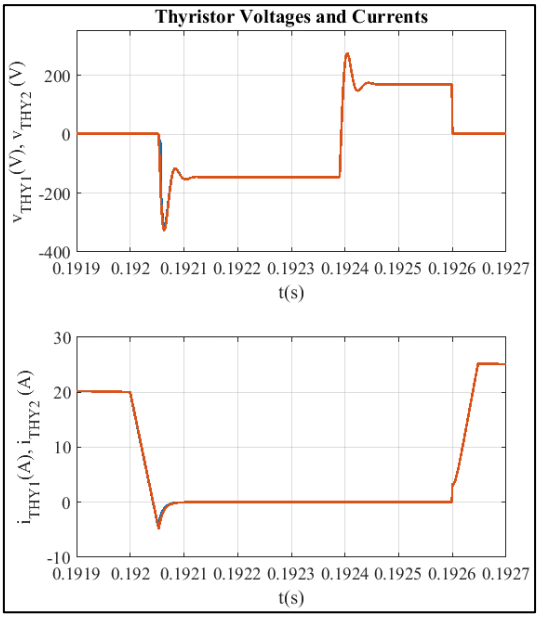


Figure 7-21: Turn-off REDUCED – R_{AUX} = 10 Ω – SIM results – Pattern 1

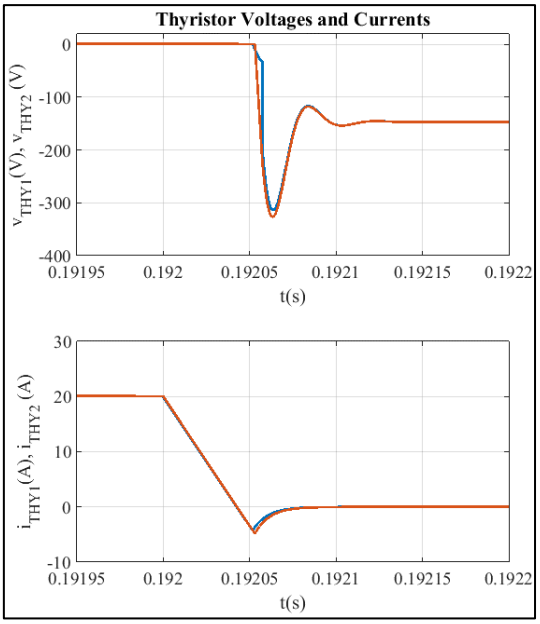


Figure 7-22: Turn-off REDUCED – R_{AUX} = 10 Ω – SIM results – Pattern 1 – zoom

Voltage balance and auxiliary current are represented in Fig. 7-23 (experiment) and Fig. 7-24 (simulation). Only one auxiliary current is shown, because the one in the branch in parallel to the slower device is zero. The auxiliary current peak is 4 A and the compensation time interval is about 5 µs. The area below the auxiliary current is 18 µC, about half of ΔQrr. The other half of ΔQrr is balanced by the damping capacitor.

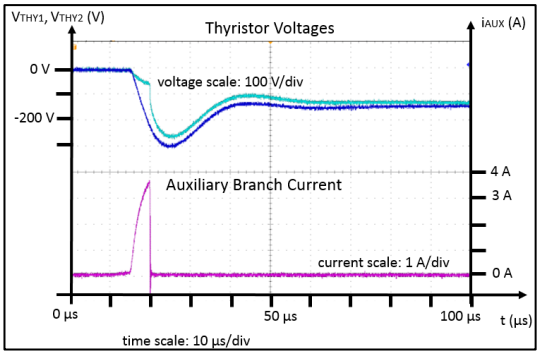


Figure 7-23: Turn-off REDUCED – RAUX = 10 Ω – EXP results – Pattern 1 – AUX current

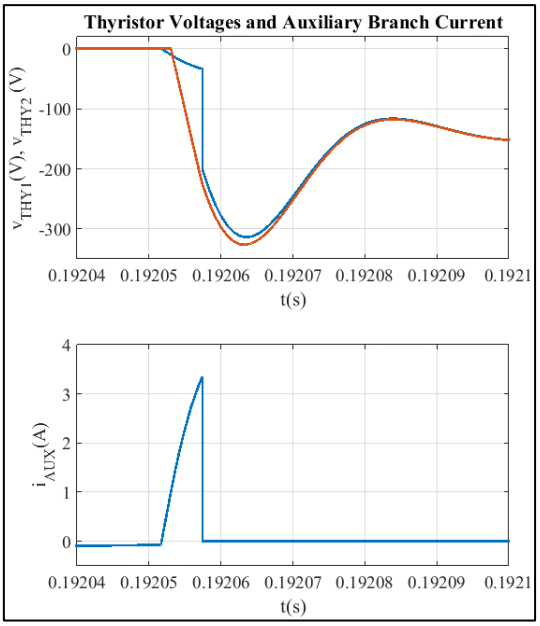


Figure 7-24: Turn-off REDUCED – R_{AUX} = 10 Ω – SIM results – Pattern 1 – AUX current

Different values of the auxiliary resistance are examined, to find the best one in terms of compensation speed and voltage stress (dv/dt) on thyristors. In detail, the two additional R_{AUX} values, tested for the same L_{COM}, Cd, Rd pattern, are 100 Ω and 500 Ω.

Waveforms for compensation with a 100 Ω R_{AUX} are illustrated from Fig. 7-25 to Fig. 7-28. The comparison between Fig. 7-25 and Fig. 7-20 shows that, increasing R_{AUX}, the compensation time interval turns out to be longer. Again, like the R_{AUX}=10 Ω case, the faster thyristor shows a dangerous voltage step. Experimental waveforms are illustrated in Fig. 7-25 and 7-26, while simulation ones in Fig. 7-27 and 7-28.

The auxiliary current peak is 2 A and the compensation time interval is about 10 µs. The area below the auxiliary current is about 15 µC, a little smaller than in the 10 Ω R_{AUX} case.

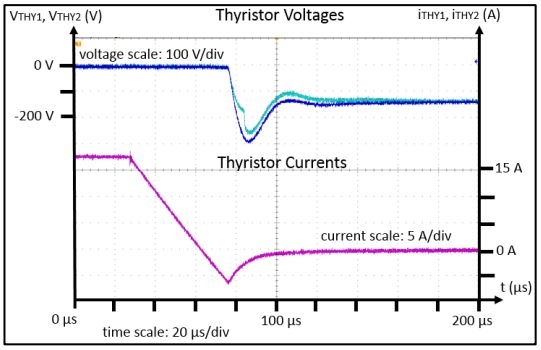


Figure 7-25: Turn-off REDUCED – RAUX = 100 Ω – EXP results – Pattern 1

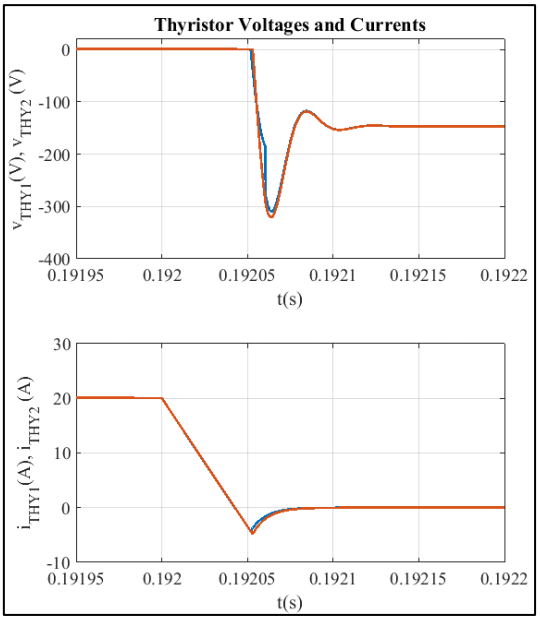


Figure 7-27: Turn-off REDUCED – R_{AUX} = 100 Ω SIM results – Pattern 1

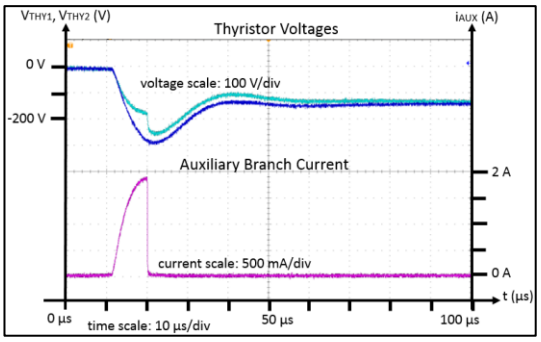


Figure 7-26: Turn-off REDUCED – RAUX = 100 Ω – EXP results – Pattern 1 – AUX current

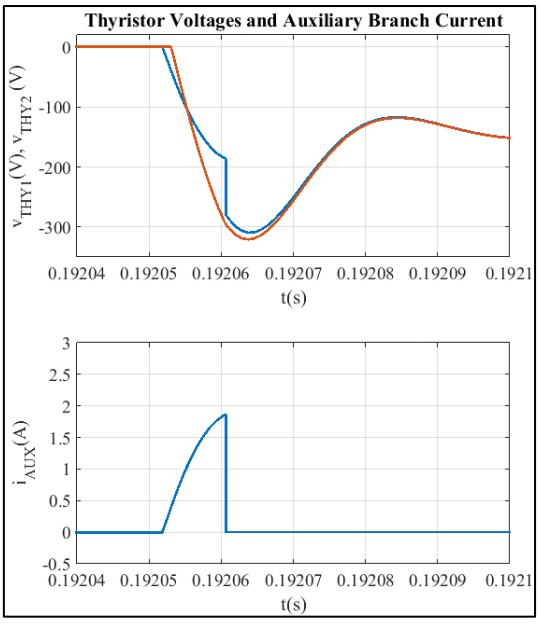


Figure 7-28: Turn-off REDUCED – R_{AUX} = 100 Ω – SIM results – Pattern 1 – AUX current

Waveforms for compensation with a 500 Ω R_{AUX} are illustrated from Fig. 7-29 to Fig. 7-32. The comparison between Fig. 7-29 and Fig. 7-25 shows that a further increase of R_{AUX} results in a longer compensation time interval but, in this case, the faster

thyristor voltage waveform, affected by the compensation, does not show any dangerous voltage step after compensation.

From a thyristor voltages point of view, the compensation process does not show excessive voltage steps, like in the two previous R_{AUX} cases. Experimental waveforms are illustrated in Fig. 7-29 and 7-30, while simulation ones in Fig. 7-31 and 7-32.

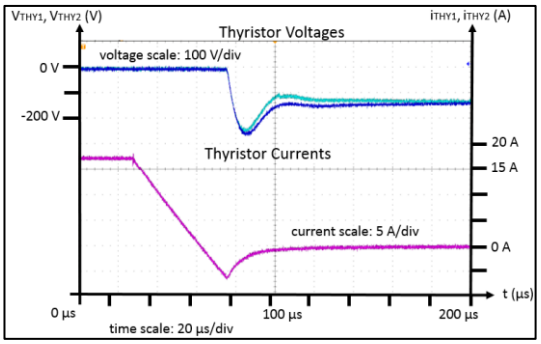


Figure 7-29: Turn-off REDUCED – RAUX = 500 Ω – EXP results – Pattern 1

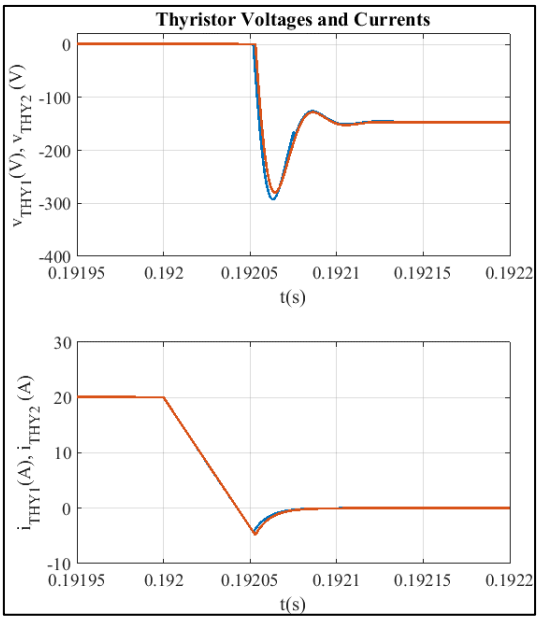


Figure 7-31: Turn-off REDUCED – RAUX = 500 Ω – SIM results – Pattern 1

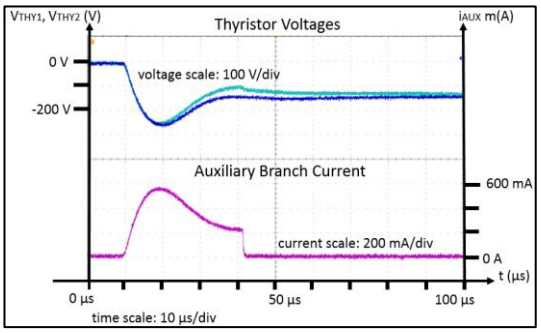


Figure 7-30: Turn-off REDUCED – RAUX = 500 Ω – EXP results – Pattern 1 – AUX current

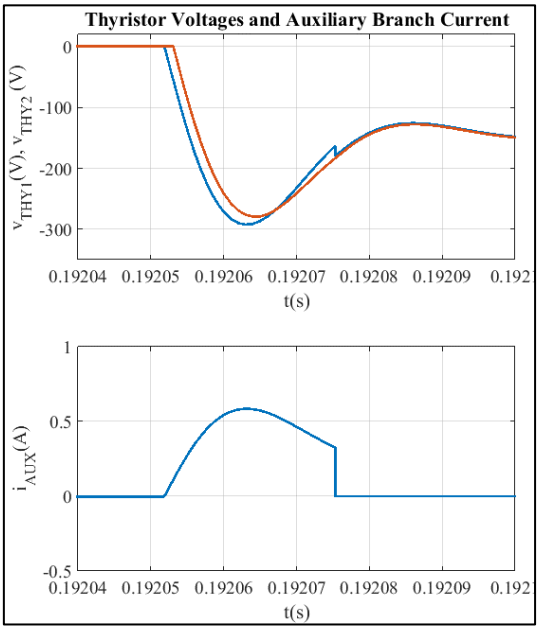


Figure 7-32: Turn-off REDUCED – R_{AUX} = 500 Ω – SIM results – Pattern 1 – AUX current

The area below the auxiliary current is about 12 µC, smaller than the previous two cases, because the balancing process takes longer, and the recombination effect is more important.

Once Pattern 1 is tested, the correct operation of the control system is investigated on Pattern 2: L_{COM} = 0.73 mH, Cd = 50 nF, Rd = 100 Ω, i.e. half Cd and double Rd, in order to reduce volume and losses related to the damping capacitance and to maintain the same time constant of the Cd-Rd series.

Voltage and current experimental waveforms for Pattern 2 and no compensation are displayed form Fig. 7-33 to Fig. 7-36. Fig. 7-33 and 7-35 are experimental results, while Fig. 7-34 and 7-36 are simulation results.

Fig. 7-35 and 7-36 are a zoom of the turn-off time interval, in which the active voltage balance provides compensation, when it is in operation.

Reverse recovery charge values set in simulations are the same of the previous pattern, so ΔQrr is 40 µC.

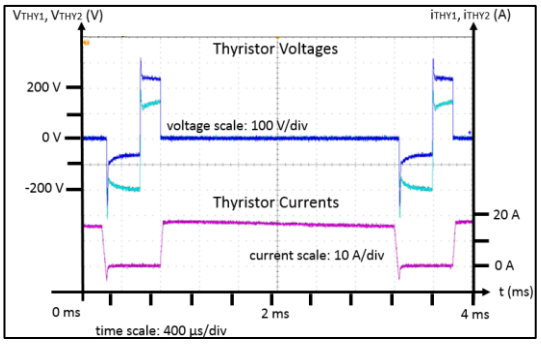


Figure 7-33: Turn-off REDUCED – no compensation – EXP results – Pattern 2

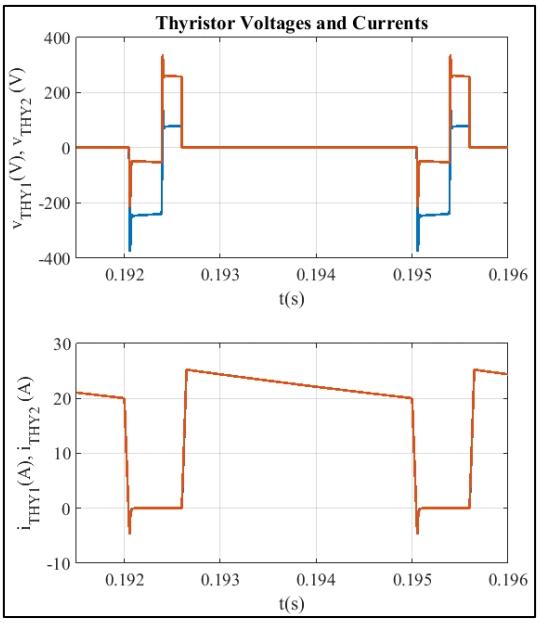


Figure 7-34: Turn-off REDUCED – no compensation – SIM results – Pattern 2

Comparing not compensated waveforms of pattern 2 with not compensated waveforms of pattern 1, they show about the same ΔV, due to the same ΔQrr, but bigger overshoot because of Cd reduction. In detail, overshoot for Cd = 50 nF is about 10% larger than the one for Cd = 100 nF.

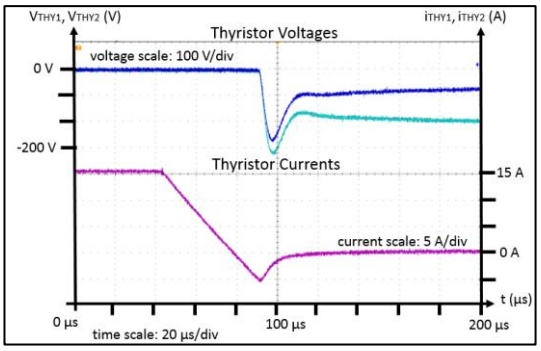


Figure 7-35: Turn-off REDUCED – no compensation – EXP results – Pattern 2 - zoom

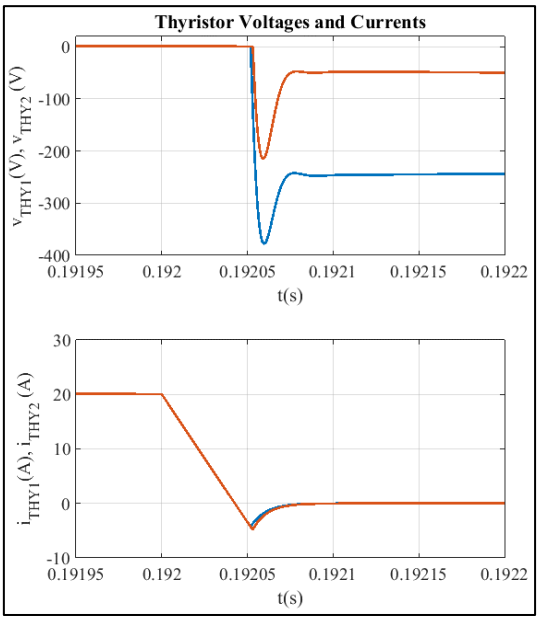


Figure 7-36: Turn-off REDUCED – no compensation – SIM results – Pattern 2 - zoom

Given that the best R_{AUX} value turned out to be 500 Ω, only this value is considered for compensation. Experimental results for L_{COM} = 0.73 mH, Cd = 50 nF, Rd = 100 Ω (Pattern 2) and R_{AUX} = 500Ω are shown in Fig. 7-37, while Fig. 7-39 represents a zoom of the turn-off compensation process. Figures 7-38 and 7-40 show simulation results for the same pattern.

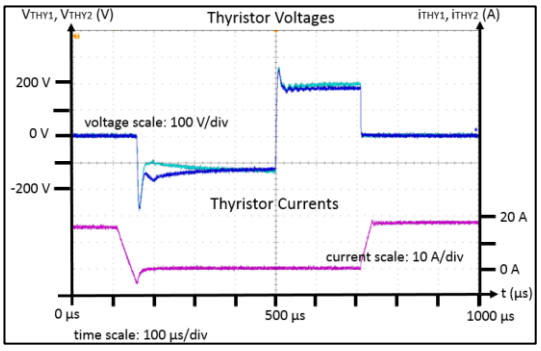


Figure 7-37: Turn-off REDUCED – R_{AUX} = 500 Ω – EXP results – Pattern 2

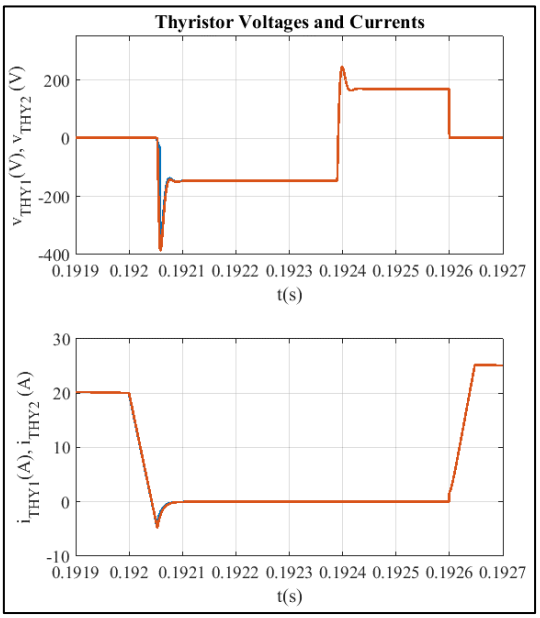


Figure 7-38: Turn-off REDUCED – R_{AUX} = 500 Ω – SIM results – Pattern 2

Even though there is a larger overshoot and a slightly bigger ΔV than pattern 1 case, the active compensation system keeps working correctly and it balances voltages also

during the overshoot time interval. Therefore, the investigated control system shows robustness to parameter changes.

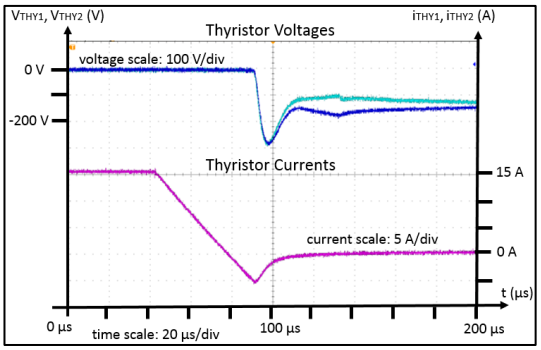


Figure 7-39: Turn-off REDUCED – R_{AUX} = 500 Ω – EXP results – Pattern 2 - zoom

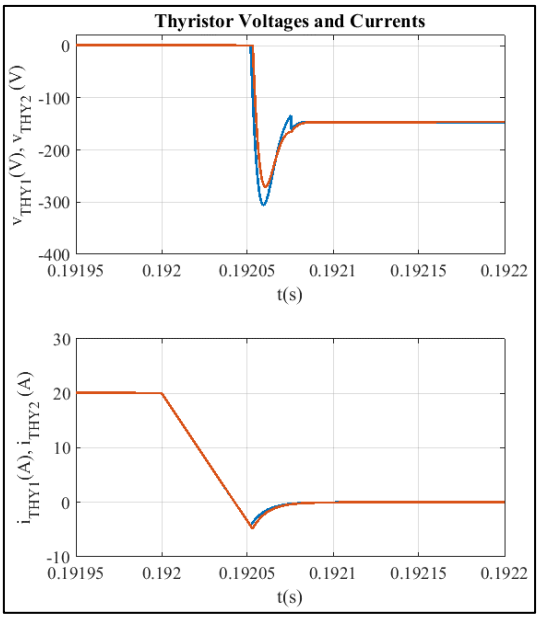


Figure 7-40: Turn-off REDUCED – R_{AUX} = 500 Ω – SIM results – Pattern 2 - zoom

Voltage balance and auxiliary current are represented in Fig. 7-41 (experiment) and Fig. 7-42 (simulation). The balancing time interval is longer than the one of the 100 µF case and the area below the auxiliary current is about 8 µC, due to a more significant recombination effect.

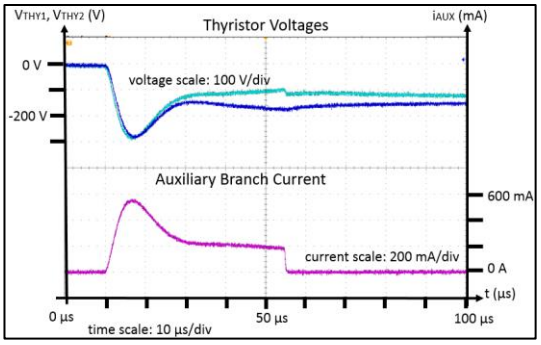


Figure 7-41: Turn-off REDUCED – RAUX = 500 Ω – EXP results – Pattern 2 – AUX current

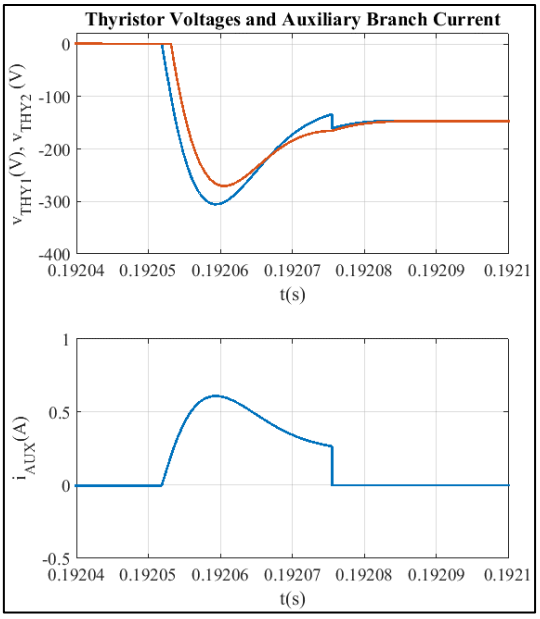


Figure 7-42: Turn-off REDUCED – R_{AUX} = 500 Ω – SIM results – Pattern 2 – AUX current

As mentioned in Sec. 6.1, experiments with a bigger L_{COM} value are conducted to test stability and robustness of the control system for different current slopes during turn-off. Increasing L_{COM}, smaller ΔVs correspond to the same ΔQrr, because the turn-off process takes longer, and carrier recombination tends to dominate.

Voltage and current waveforms for L_{COM} = 9 mH, Cd = 100 nF, Rd = 50 Ω (Pattern 3) and no compensation are displayed in Fig. 7-43 (experiment) and 7-44 (simulation). Only a zoom on the turn-off time interval is shown.

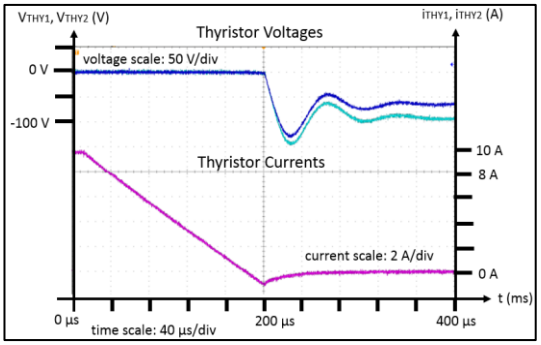


Figure 7-43: Turn-off REDUCED – no compensation – EXP results – Pattern 3

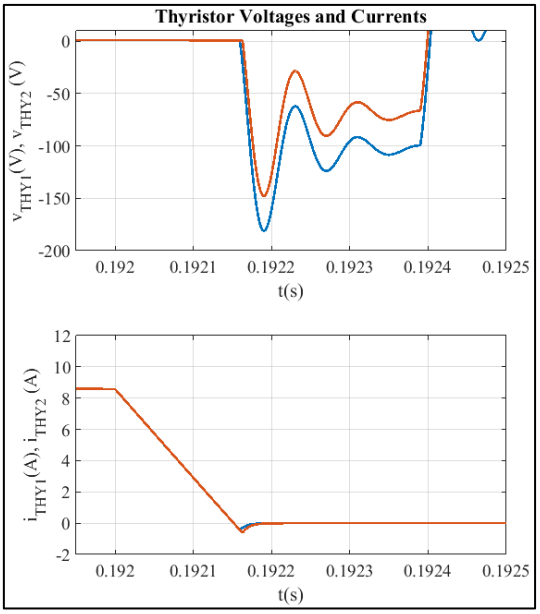


Figure 7-44: Turn-off REDUCED – no compensation – SIM results – Pattern 3

Concerning compensation, only the case of R_{AUX} = 500 Ω is considered. Voltage and current waveforms for Pattern 3 and compensation with R_{AUX} = 500 Ω are depicted in Fig. 7-45 (experiment) and 7-46 (simulation), in which the compensation process does not present severe voltage steps. Therefore, 500 Ω turns out to be the most appropriate R_{AUX} choice also for different L_{COM} values.

The active control system keeps working for L_{COM}, Cd, Rd pattern variations, showing stability and robustness to parameter variations.

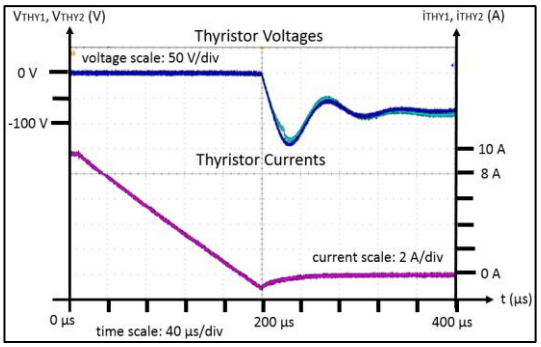


Figure 7-45: Turn-off REDUCED – RAUX = 500 Ω – EXP results – Pattern 3

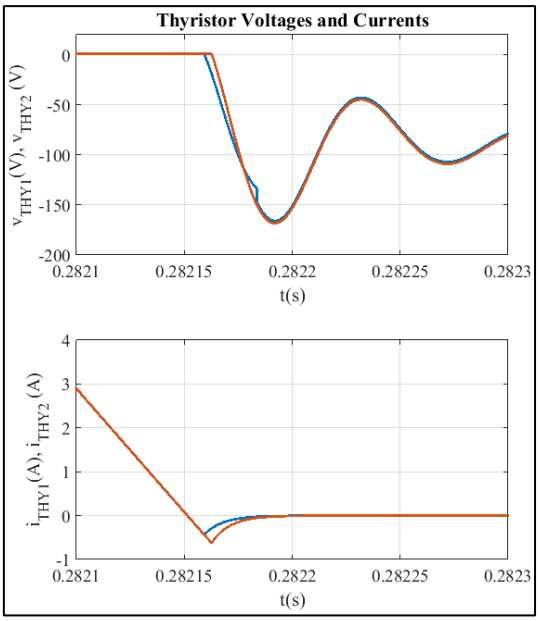


Figure 7-46: Turn-off REDUCED – R_{AUX} = 500 Ω – SIM results – Pattern 3

Voltage balance and auxiliary current are represented in Fig. 7-47 (experiment) and Fig. 7-48 (simulation). The area below the auxiliary current is about 8 µC.

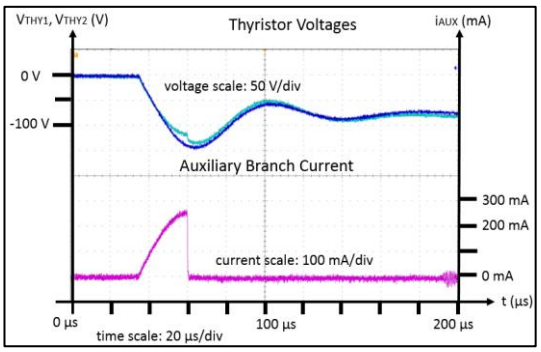


Figure 7-47: Turn-off REDUCED – RAUX = 500 Ω – EXP results – Pattern 3 – AUX current

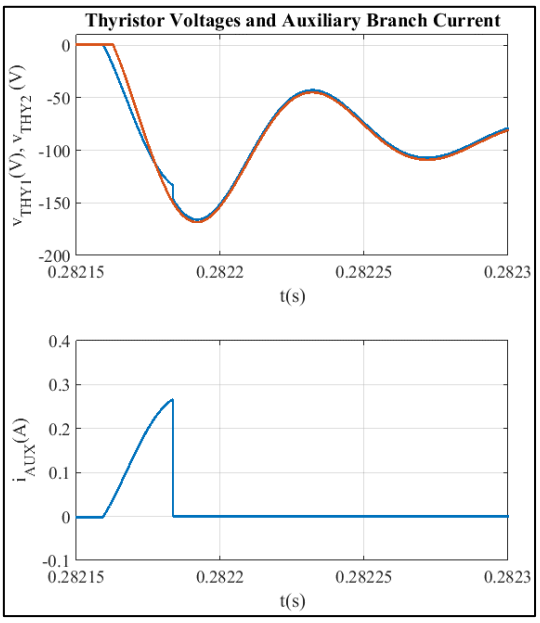


Figure 7-48: Turn-off REDUCED – R_{AUX} = 500 Ω – SIM results – Pattern 3 – AUX current

In the same way of the L_{COM} = 0.73 mH case, after testing Cd = 100 nF, Rd = 50 Ω, the combination Cd = 50 nF, Rd = 100 Ω is investigated. The reasons for Cd reduction do not change if a different L_{COM} is considered: they remain volume and losses reduction. After Cd choice, Rd value is the one that maintains the desired time constant.

Voltage and current waveforms for L_{COM} = 9 mH, Cd = 50 nF, Rd = 100 Ω (Pattern 4) and no compensation are displayed in Fig. 7-49 (experiment) and 7-50 (simulation). Comparing these pictures to the ones of Pattern 3, a slight overshoot increase is shown, due to Cd reduction. Pattern 4 waveforms, compensated with R_{AUX} = 500 Ω, are illustrated in Fig. 7-51 (experimental) and 7-52 (simulation). The compensation is not affected by dangerous voltage steps.

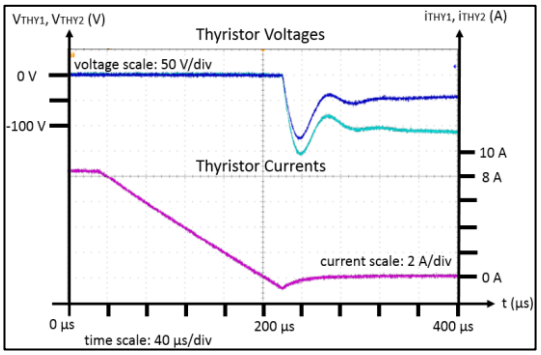


Figure 7-49: Turn-off REDUCED – no compensation – EXP results – Pattern 4

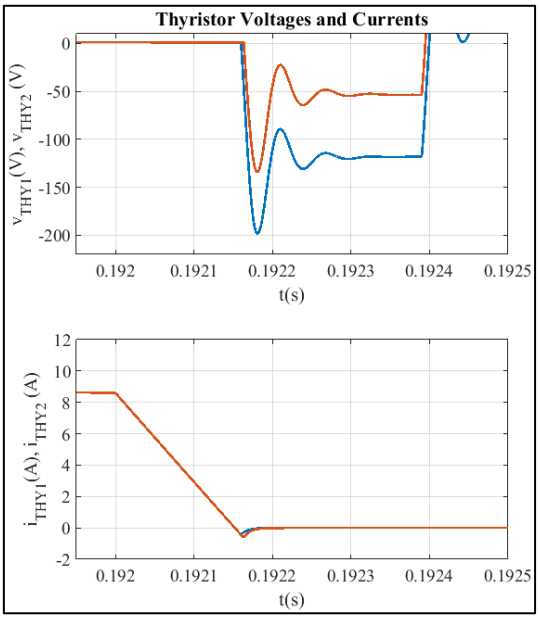


Figure 7-50: Turn-off REDUCED – no compensation – SIM results – Pattern 4

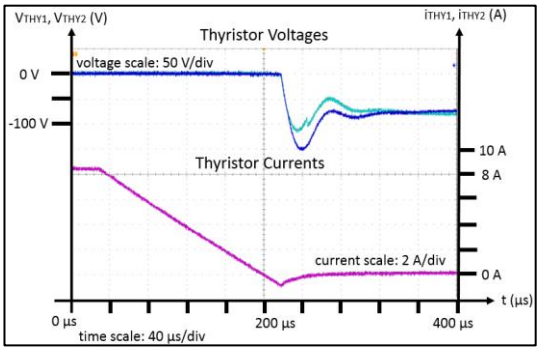


Figure 7-51: Turn-off REDUCED – RAUX = 500 Ω – EXP results – Pattern 4

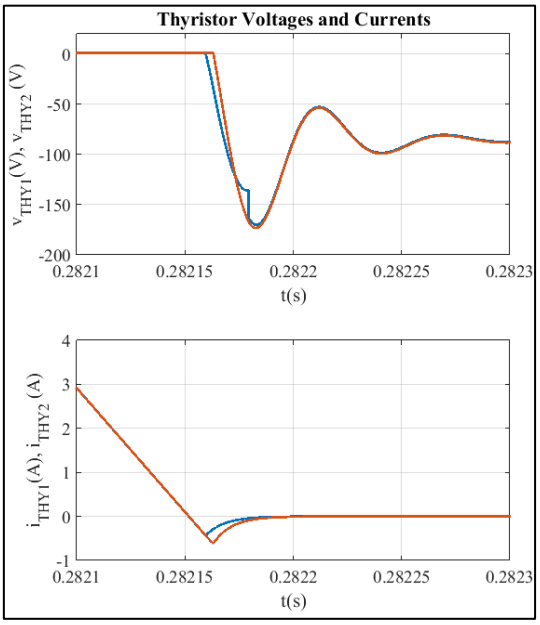


Figure 7-52: Turn-off REDUCED – R_{AUX} = 500 Ω – SIM results – Pattern 4

Voltage balance and auxiliary current are represented in Fig. 7-53 (experiment) and Fig. 7-54 (simulation). The area below the auxiliary current is about 6 µC.

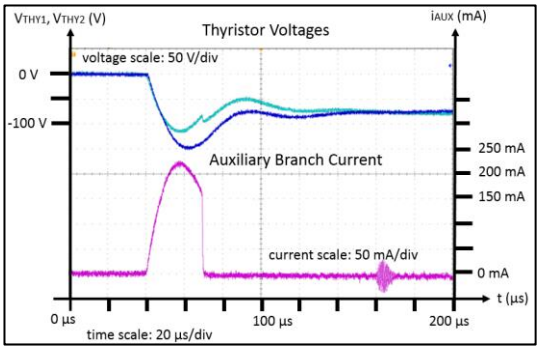


Figure 7-53: Turn-off REDUCED – RAUX = 500 Ω – EXP results – Pattern 4 – AUX current

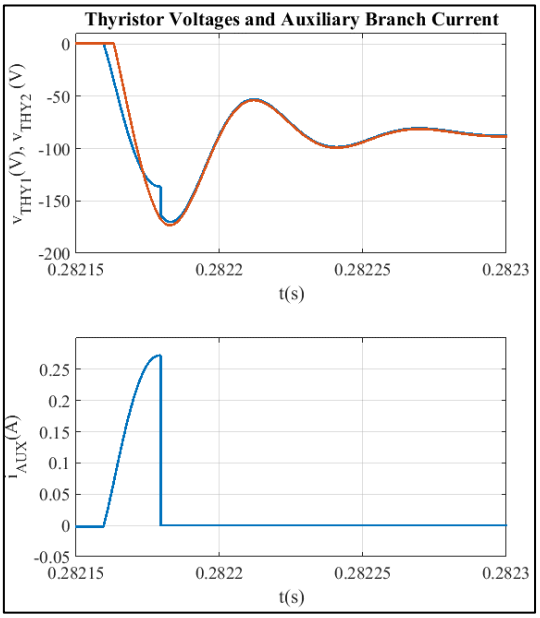


Figure 7-54: Turn-off REDUCED – R_{AUX} = 500 Ω – SIM results – Pattern 4 – AUX current

Comparing all the auxiliary current waveforms, the general feature is that the longer the compensation time interval, the more significant the recombination effect and the smaller the electrical charge that passes through the auxiliary branch.

7.3. Scaling-up issues

Once the active control methods are developed at a reduced scale, it is important to know how to apply them back in the real scale. The turn-on control method can be applied in the same way as the reduced scale, as it is directly synchronised with the main thyristor gate signal. On the other hand, a synchronisation issue needs to be addressed to apply the "Faster Device Turn-off Delay" method.

As discussed in Sec. 7.2, a Rogowski probe is necessary in real scale to synchronise "turn-off delays" with the actual turn-off, to maintain the active control internal to the valve, not dependent on external measurements (firing angle variation, frequency etc.).

The synchronisation of the "turn-off delay" with negative current zero crossing is not possible in the real valve, because the sampling time to measure the zero crossing is of the same order of magnitude of the compensation time interval. In the experiments (Sec. 7.2), the compensation process is synchronised with the reverse voltage application, because the DSP signal that applies the blocking voltage is available and it is used also to start applying the "delay". This is not possible in the real converter, for which the reverse voltage is externally applied, and the frequency is not exactly 50 Hz. A Rogowski probe, detects negative di/dt when reverse voltage is applied, before the zero crossing. The time interval between di/dt starts being negative and current zero crossing (beginning of the reverse recovery) is the offset of the "turn-off delay". The consequence of the offset is a longer transient for the PI control to reach the steady state than in the ideal case of no offset. From an electrical point of view, the auxiliary switch is turned on when the main thyristor is still conducting, i.e. when di/dt is negative but the current has not crossed the zero yet. This has no effect until the reverse recovery process starts, because R_{AUX} is connected in parallel to a short circuit before the negative current peak is reached.

Concerning the hardware, to update the actual thyristor valve, including the Active Current Control and the Active Damping Circuit, three main changes need to be done:

1) Saturable reactor replacement with the Active Current Control system
2) Damping capacitors size reduction thanks to Active Damping Circuit inclusion
3) Cooling system size modification

1) The saturable reactor removal in the real scale thyristor valve is possible only if the turn-on control method works perfectly, i.e. any di/dt above thyristor rating is carried by the auxiliary active branch. In this case, the saturable reactor can be taken off and, in the updated configuration, its volume and weight shares are replaced by the ones of the turn-on active branch. In detail, the saturable reactor is replaced by a number of auxiliary switch-auxiliary resistance branches, equal to the number of thyristors in series.
2) Damping capacitance reduction determines damping capacitors volume and weight reduction, thanks to the use of a turn-off active control system. Therefore, capacitors size reduction is accompanied by an auxiliary switch-auxiliary resistance series inclusion, for each thyristor of the series.
3) The cooling system thermal power size depends on thyristors losses, damping branches (Cd-Rd series) losses, turn-on and turn-off active branches losses. If total losses of the updated valve are lower than the ones of the actual valve, the cooling system size can be reduced in terms of both thermal power and volume, with related benefits.

Once all the updates are set up to realise the new thyristor valve version, revised total volume and total weight are compared with the previous version ones. In addition, the updated version cost is compared with the previous configuration cost: the comparison should include also the revised operating cost, due to a different efficiency. If there is no advantage in terms of initial cost, but the actively controlled valve shows a higher efficiency, this may still provide an attractive solution once capitalised losses over operational life have been considered.

7.4. Summary

In this chapter, both turn-on and turn-off control methods are successfully tested, using a reduced scale experimental circuit.

Concerning turn-on experiments, a high value of commutation inductance (L_{COM}) is used, in order to reduce the di/dt and to obtain an initial current spike separated from the on-state current rise. A specific damping resistance-damping capacitance (Rd-Cd) combination is chosen to get an appropriate wave shape of the initial current spike and a 3.4 Ω auxiliary resistance (R_{AUX}) is employed to achieve a satisfactory current diversion. No feedback control is needed because once the external circuit is defined, the relevant stray capacitance does not change significantly during the operation and the diversion time interval does not need to be adjusted. A diversion time interval of 80 μs resulted a satisfactory choice for the conducted experiments.

Regarding turn-off experiments, the "faster device turn-off delay" method is validated. Four different patterns of L_{COM}, Cd, Rd have been tested and three different values of R_{AUX} have been compared. The best R_{AUX} value in terms of compensation speed, overshoot and voltage steps (dv/dt) turned out to be 500 Ω.

Scaling-up issues, concerning saturable inductor replacement, damping capacitors size reduction and cooling system size modification are finally discussed.

The next chapter contains the conclusions of this research project.

8. Conclusions

The research presented in this thesis has investigated the development of a smart thyristor valve for HVDC transmission, to reduce the auxiliary circuits volume and weight, through the employment of active, instead of passive solutions. Such a reduction can lead to a cost reduction of the overall valve and, thanks to a lower weight, also to a cost reduction of the mechanical structure needed to sustain the valve from the roof, for seismic protection.

The thesis starts with a description of the historical path of HVDC transmission and of the main configurations of HVDC schemes, including some examples of application.

In order to perform simulations of the actual thyristor valves and of different configurations, a precise model of the devices of interest is needed. A detailed discussion about the physics of thyristors and about the different models available is provided, and a sample simulation of the model chosen for this project is performed.

The actual valve configuration is discussed, describing the function of each passive component, especially the saturable inductor and the damping branch. The saturable inductor provides di/dt limiting during turn-on commutations, to protect the thyristor from the external stray capacitance discharge, while the damping branch provides both damping and voltage sharing during turn-off transients.

Turn-on and turn-off active control methods make use of one auxiliary branch each, realised by an auxiliary switch and an auxiliary resistance in series. It is not possible to implement both methods in the same branch, because two different values of auxiliary resistance are required, with two different power ratings.

The turn-on active control method diverts the current spike from the external stray capacitance into the auxiliary branch during the initial part of the turn-on transient, while the turn-off active control method connects the auxiliary resistances in parallel to each thyristor for proper time intervals during the turn-off transient, providing uniform voltage sharing.

Real scale simulations of a thyristor valve operating into a six-pulse inverter validate both the proposed actively controlled solutions.

A reduced scale experimental rig has been designed and built in order to validate the active control methods also experimentally. The design of the experimental rig is explained in detail, including the link between real scale and reduced scale.

Turn-on and turn-off active control systems are investigated independently, and the associated experimental test are conducted separately. From an electrical point of view, they are two electrical branches to be connected in parallel to the device under test, which control should be integrated in the same software.

Concerning turn-on control, the two parameters to be adjusted to achieve a correct operation are the auxiliary resistance (R_{AUX}) and the diversion time interval (Δt). The power rating of R_{AUX} has to be established according to power losses during current diversion.

The turn-off control system goal is to balance voltage differences, due to different reverse recovery charge of thyristors in series, during turn-off. Two methods have been tested, based on a different control concept, but on the same electrical circuit: the "hysteresis" and the "faster device turn-off delay". The first one has been only simulated, while the second one has been also tested experimentally.

Advantages of the "hysteresis" method are that it is easy to be implemented and that it reaches the steady state immediately, while the main disadvantage is that the steady state error cannot be compensated. Three parameters need to be adjusted for correct operation: R_{AUX} and the two hysteresis voltage thresholds.

The "faster device turn-off delay" has a more complex implementation than the "hysteresis", as it requires a PI control, but it has the advantage of compensating the steady state error very effectively. The main disadvantage is that it requires a certain time interval before reaching the steady state. Three parameters have to be calibrated: the two PI constants and the R_{AUX} value. The PI constants have been adjusted depending on R_{AUX}, while the R_{AUX} value has been chosen from a comparison between different numbers: the best choice is a compromise to obtain a compensation process fast enough, with no dangerous voltage steps. In both simulations and experimental tests, different combinations of the damping parameters have been compared, to reduce the damping capacitance value as much as possible, without losing uniform voltage sharing, thanks to the active control.

Experimental results are successful and match simulations for both the control methods, therefore, the investigated active configurations can be considered for effective improvements of the actual thyristor valves.

To apply the examined control methods in the real scale it is necessary to scale-up the reduced scale prototype. One issue that need to be carefully considered while scaling-up the turn-off control method is the current zero-crossing detection. The employment of a Rogowski probe to overcome this problem has been discussed. Once a real scale smart thyristor valve prototype will be available, cost, volume and weight reduction will be definitely verified.

The research contributions of the work presented in this thesis are a theoretical knowledge of active control of thyristor turn-on and turn-off commutations, successful simulation results of an active turn-on control method for initial current spike diversion, successful simulation results of an active turn-off control method for uniform voltage sharing, design and realisation of a test circuit for experimental tests, successful experimental results that match simulation results and validation of the ideas contained in the two reference patents.

Future directions are related to the development of a fully commercial product. The necessary steps are high voltage experimental tests on a real scale prototype, the comparison between different hardware solutions in terms of auxiliary devices and the verification of the effective costs, volume and weight reduction of the updated valve, compared to the actual one.

9. References

Not many researchers work on the investigated topic because most of the research is focussed on the development of innovative high-frequency modulation converters (either multilevel or not), rather than the innovation of traditional thyristor valves. For this reason, there are no significant recent publications.

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10. Appendix A – Infineon T2871N Data Sheet

	Technische Information / technical information	
Netz-Thyristor Phase Control Thyristor	**T2871N**	Infineon Technologies Bipolar GmbH & Co. KG

Key Parameters

V_{DRM} / V_{RRM}	7500V … 8000V
I_{TAVM}	2620A (T_C=85°C)
I_{TSM}	93000A
v_{T0}	1,267V
r_T	0,336mΩ
R_{thJC}	4,3K/kW
Clamping Force	90 … 130kN
Max. Diameter	172,5mm
Contact Diameter	115mm
Height	35mm

Features

- Full blocking 50/60Hz over a wide range temperature range
- High DC blocking stability
- High surge current capability
- High case non-rupture current
- High di/dt capability

Typical Applications

- High Voltage Direct Current Transmission HVDC
- Static Var Compensation SVC
- Rectifier for Drives Applications
- Medium Voltage Drives
- Load Commutating Inverter

Elektrische Eigenschaften / electrical properties
Höchstzulässige Werte / maximum rated values

Periodische Vorwärts- und Rückwärts-Spitzensperrspannung repetitive peak forward off-state and reverse voltage	T_{vj} = -40°C… $T_{vj\,max}$	V_{DRM},V_{RRM}	7500 8000	V V
Durchlaßstrom-Grenzeffektivwert maximum RMS on-state current	T_C = 85 °C	I_{TRMSM}	4120	A
Dauergrenzstrom average on-state current	T_C = 85 °C T_C = 70 °C T_C = 55 °C	I_{TAVM}	2620 3170 3660	A A A
Stoßstrom-Grenzwert surge current	T_{vj} = 25 °C, t_P = 10 ms T_{vj} = $T_{vj\,max}$, t_P = 10 ms	I_{TSM}	93000 90000	A A
Grenzlastintegral I²t-value	T_{vj} = 25 °C, t_P = 10 ms T_{vj} = $T_{vj\,max}$, t_P = 10 ms	I²t	43250 40500	10^3 A²s 10^3 A²s
Kritische Stromsteilheit critical rate of rise of on-state current	DIN IEC 60747-6 f = 50 Hz, i_{GM} = 3 A, di_G/dt = 6 A/µs	$(di_T/dt)_{cr}$	300	A/µs
Kritische Spannungssteilheit critical rate of rise of off-state voltage	T_{vj} = $T_{vj\,max}$, v_D = 0,67 V_{DRM} 5.Kennbuchstabe / 5th letter H	$(dv_D/dt)_{cr}$	2000	V/µs

Elektrische Eigenschaften / electrical properties

Charakteristische Werte / characteristic values

Durchlaßspannung on-state voltage	$T_{vj} = T_{vj\,max}$, i_T = 5000A	v_T	typ. Max.	2,45 2,95	V V
Schleusenspannung threshold voltage	$T_{vj} = T_{vj\,max}$	$V_{(TO)}$	typ. max.	1,083 1,267	V V
Ersatzwiderstand slope resistance	$T_{vj} = T_{vj\,max}$	r_T	typ. Max.	0,274 0,336	mΩ mΩ
Durchlaßkennlinie 500A ≤ i_F ≤ 6000A on-state characteristic $v_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$	$T_{vj} = T_{vj\,max}$	typ.	A B C D	0,6702 0,000075 -0,02702 0,023126	
		max.	A B C D	0,72998 0,000111 -0,01889 0,02575	
Zündstrom gate trigger current	T_{vj} = 25°C, v_D = 12 V	I_{GT}	max.	350	mA
Zündspannung gate trigger voltage	T_{vj} = 25°C, v_D = 12 V	V_{GT}	max.	2,5	V
Nicht zündender Steuerstrom gate non-trigger current	$T_{vj} = T_{vj\,max}$, v_D = 12 V $T_{vj} = T_{vj\,max}$, v_D = 0,5 V_{DRM}	I_{GD}	max. max.	20 10	mA mA
Nicht zündende Steuerspannung gate non-trigger voltage	$T_{vj} = T_{vj\,max}$, v_D = 0,5 V_{DRM}	V_{GD}	max.	0,4	V
Haltestrom holding current	T_{vj} = 25°C, v_D = 12 V	I_H	max.	350	mA
Einraststrom latching current	T_{vj} = 25°C, v_D = 12 V, R_{GK} ≥ 10 Ω i_{GM} = 3 A, di_G/dt = 6 A/µs, t_g = 20 µs	I_L	max.	3	A
Vorwärts- und Rückwärts-Sperrstrom forward off-state and reverse current	$T_{vj} = T_{vj\,max}$ $v_D = V_{DRM}$, $v_R = V_{RRM}$	i_D, i_R	max.	900	mA
Zündverzug gate controlled delay time	DIN IEC 60747-6 T_{vj} = 25 °C,i_{GM} = 3 A, di_G/dt = 6 A/µs	t_{gd}	max.	2	µs

Elektrische Eigenschaften / electrical properties

Charakteristische Werte / characteristic values

Freiwerdezeit circuit commutated turn-off time	$T_{vj} = T_{vj\,max}$, $i_{TM} = I_{TAVM}$ v_{RM} = 100 V, v_{DM} = 0,67 V_{DRM} dv_D/dt = 20 V/µs, $-di_T/dt$ = 10 A/µs 4.Kennbuchstabe / 4th letter O	t_q	typ.	550	µs
Sperrverzögerungsladung recovered charge	$T_{vj} = T_{vj\,max}$ $i_{TM} = I_{TAVM}$, $-di_T/dt$ = 10 A/µs V_R = 0,5V_{RRM}, V_{RM} = 0,8V_{RRM}	Q_r	max.	22	mAs
Rückstromspitze peak reverse recovery current	$T_{vj} = T_{vj\,max}$ $i_{TM} = I_{TAVM}$, $-di_T/dt$ = 10 A/µs V_R = 0,5V_{RRM}, V_{RM} = 0,8V_{RRM}	I_{RM}	max.	400	A

Thermische Eigenschaften / thermal properties

Innerer Wärmewiderstand thermal resistance, junction to case	Kühlfläche / cooling surface beidseitig / two-sided, θ = 180°sin beidseitig / two-sided, DC Anode / anode, DC Kathode / cathode, DC	R_{thJC}	max. max. max. max.	4,5 4,3 7,8 9,6	K/kW K/kW K/kW K/kW
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	Kühlfläche / cooling surface beidseitig / two-sided einseitig / single-sided	R_{thCH}	max. max.	1,0 2,0	K/kW K/kW
Höchstzulässige Sperrschichttemperatur maximum junction temperature		$T_{vj\,max}$		125	°C
Betriebstemperatur operating temperature		$T_{c\,op}$		-40...+125	°C
Lagertemperatur storage temperature		T_{stg}		-40...+150	°C

Mechanische Eigenschaften / mechanical properties

Anpresskraft clamping force		F	90...130	kN
Steueranschlüsse control terminals	DIN 46244 Gate Kathode /Cathode		A 4,8x0,8 A 6,3x0,8	
Gewicht weight		G	typ. 4000	g
Kriechstrecke creepage distance			49	mm
Schwingfestigkeit vibration resistance	f = 50 Hz		50	m/s²

11. Appendix B – Dynex DCR 3030V42 Data Sheet

Dependable Power through Innovation

DCR3030V42

Phase Control Thyristor

DS5810-3 January 2014 (LN31245)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

KEY PARAMETERS

V_{DRM}	4200V
$I_{T(AV)}$	3030A
I_{TSM}	40600A
dV/dt*	1500V/µs
dI/dt	400A/µs

* **Higher dV/dt selections available**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR3030V42 DCR3030V40 DCR3030V35 DCR3030V30	4200 4000 3500 3000	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 200mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3030	A
$I_{T(RMS)}$	RMS value	-	4760	A
I_T	Continuous (direct) on-state current	-	4550	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	40.6	kA
I^2t	I^2t for fusing	V_R = 0	8.24	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00746	°C/W
		Single side cooled	Anode DC	-	0.0130	°C/W
			Cathode DC	-	0.0178	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 54kN	Double side	-	0.002	°C/W
		(with mounting compound)	Single side	-	0.004	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / $_{VRRM}$		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			48.0	59.0	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	400	A/µs
$V_{T(TO)}$	Threshold voltage – Low level	200A to 1700A at T_{case} = 125°C		-	0.82	V
	Threshold voltage – High level	1700A to 7000A at T_{case} = 125°C		-	0.98	V
r_T	On-state slope resistance – Low level	200A to 1700A at T_{case} = 125°C		-	0.292	mΩ
	On-state slope resistance – High level	1700A to 7000A at T_{case} = 125°C		-	0.198	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		TBD	TBD	µs
t_q	Turn-off time	T_j = 125°C, V_R = 200V, dI/dt = 1A/µs, dV_{DR}/dt = 20V/µs linear		250	500	µs
Q_S	Stored charge	T_j = 125°C, dI/dt – 1A/µs, $V_{R\,pk}$ =3000V, V_{RM}= 1700V		1600	3500	µC
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At V_{DRM}, T_{case} = 125°C	TBD	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	350	mA
I_{GD}	Gate non-trigger current	V_{DRM} = 5V, T_{case} = 25°C	TBD	mA

12. Appendix C – Dynex DCR 3980H85 Data Sheet

Dependable Power through Innovation

DCR3980H85

Phase Control Thyristor

DS6139-2 January 2015 (LN32245)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- Bridge Rectifiers
- High Voltage Power Supplies
- Motor Drives

KEY PARAMETERS

V_{DRM}	8500V
$I_{T(AV)}$	3980A
I_{TSM}	59580A
dV/dt*	2000V/µs
dI/dt	200A/µs

* **Higher dV/dt selections available**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR3980H85* DCR3980H80 DCR3980H75	8500 8000 7500	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 600mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.
*8200V @ -40^0 C, 8500V @ 0^0 C

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3980	A
$I_{T(RMS)}$	RMS value	-	6247	A
I_T	Continuous (direct) on-state current	-	5767	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	59.58	kA
I^2t	I^2t for fusing	V_R = 0	17.75	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.004255	°C/W
		Single side cooled	Anode DC	-	0.008	°C/W
			Cathode DC	-	0.0093	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 135.0kN	Double side	-	0.0009	°C/W
		(with mounting compound)	Single side	-	0.0018	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			120	155	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	600	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	2000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	500	A/µs
$V_{T(TO)}$	Threshold voltage – Low level	500 to 4000A at T_{case} = 125°C		-	1.0	V
	Threshold voltage – High level	4000 to 8000A at T_{case} = 125°C		-	1.2933	V
r_T	On-state slope resistance – Low level	500A to 4000A at T_{case} = 125°C		-	0.31	mΩ
	On-state slope resistance – High level	4000A to 8000A at T_{case} = 125°C		-	0.2333	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	I_T = 3000A, T_j = 125°C, V_R = 200V, dI/dt = 1A/µs, dV_{DR}/dt = 20V/µs linear			1000	µs
Q_S	Stored charge	I_T = 3000A, T_j = 125°C, dI/dt – 1A/µs, V_{Rpeak} ~5100V, V_R ~ 3400V		4900	10600	µC
I_{RR}	Reverse recovery current			54	87	A
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	350	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	10	mA

13. Appendix D – Dynex PT85QWx45 Data Sheet

Dependable Power through Innovation

PT85QWx45

Pulse Power Thyristor Switch

DS5334-2 July 2012 (LN29644)

FEATURES

- Double Side Cooling
- Fast turn-on
- Low Turn-on Losses

APPLICATIONS

- Pulse Power
- Crowbars
- Ignitron replacement

KEY PARAMETERS

V_{DRM}	4500V
$I_{T(AV)}$	1670A
I_{TSM}	37000A
dI/dt	22000A/µs

* **Higher dV/dt selections available**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
PT85QWx45	4500/16	T_{vj} = 0°C to 125°C, I_{DRM} = I_{RRM} = 250mA, V_{DRM}, V_{RRM} t_p = 10ms,

Lower voltage grades available.

CURRENT RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load, T_{case} = 80°C	1670	A
$I_{T(RMS)}$	RMS value	-	2622	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	29.6	kA
I^2t	I^2t for fusing	V_R = 50% V_{RRM}	4.38	MA^2s
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	37	kA
I^2t	I^2t for fusing	V_R = 0	6.85	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.01	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 36kN	Double side	-	0.001	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
		On-state (conducting)		-	135	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			36	44	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	250	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, R_{gk}≤ 1.5Ω		-	200	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 20kA Gate source 30A t_r < 1.5µs, T_j = 125°C	Non-repetitive	-	22	kA/µs
$V_{T(TO)}$	Threshold voltage	T_{vj} = 125°C		-	1.45	V
r_T	On-state slope resistance – Low level	T_{case} = 125°C		-	0.3	mΩ

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.0	4.0	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	-	1.5	A

14. Appendix E – Air Cored Inductor Design for the Experimental Test Circuit

In order to avoid saturation and consequent non-linear behaviour of inductors, two air cored inductors have been realised, which design is based on the Brooks inductor [35].

Air cored inductors are usually wound with circular turns, so that the wires build up to give a rectangular cross-section, as shown in Fig. 10-1.

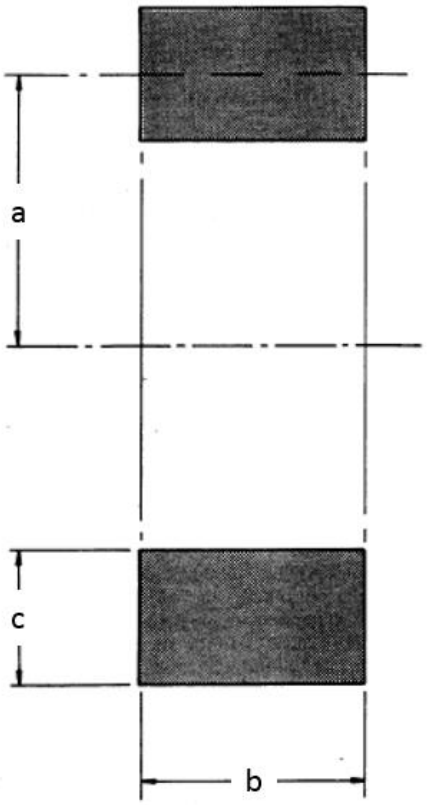


Figure 14-1: Circular inductor with rectangular section

For the Brooks inductor b=c, a=1.5c and it can be easily remembered as "four squares". For a desired L_B inductance with a maximum current rating I_m and a fixed current density J_m, the "c" dimension and the number of turns "N" can be calculated as follows.

$$c = \sqrt[5]{\frac{L_B I_m^2}{2.029 \mu_0 J_m^2}}$$

$$N = \sqrt[5]{\frac{L_B^2 J_m}{4.117 \mu_0^2 I_m}}$$

For a speedy approximate solution, the universal design graph in Fig.10-2 can be used.

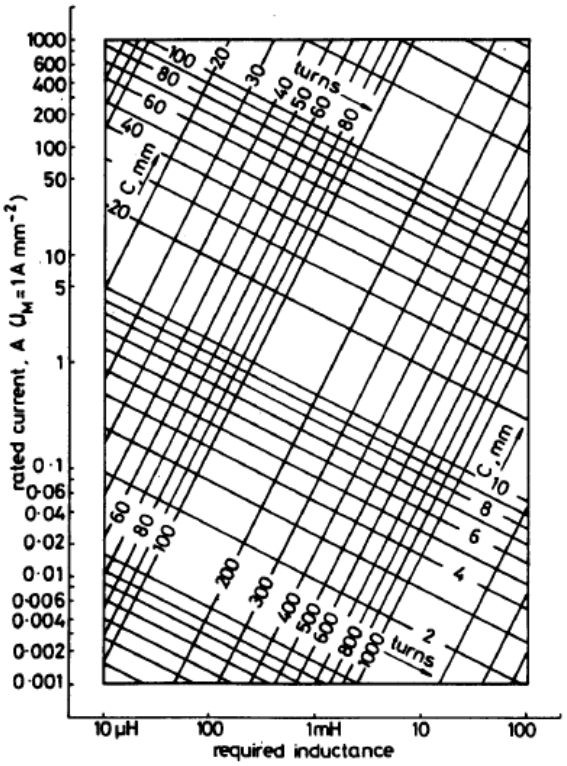


Figure 14-2: Design graph for Brooks inductors based on current density J_M = 1 A/mm^2

The proposed solution for the realisation of the 4.8 mH inductor is depicted in Fig. 10-3: the effective inductance of this design is 4.9 mH and the current density corresponding to the maximum current rating of 50 A is 3.86 A/mm^2 (single turn cross section of 13 mm^2). If a double pulse test is considered, it is not important to maintain the current density below a specific value, because the forward conduction state of the DUT is only a few ms long in experimental tests. On the contrary, if a periodic test is contemplated, current density cannot be higher than the maximum admitted value for the chosen design.

It is very expensive to build a custom cross section for a relatively short winding and, for this reason, a round wire has to be chosen. In particular, the closest round wire is the 5.00 mm diameter and the closest solution to the one in Fig. 10-3 is the following:

n = 13

c = 5·13 = 65 mm

N = 13·13 = 169

Effective inductance = L_B = 4.7 mH

Rint = 65 mm (Internal Diameter = 130 mm)

Rmean = 97.5 mm (Mean Turn Diameter = 195 mm)

Rext = 130 mm (External Diameter = 260 mm)

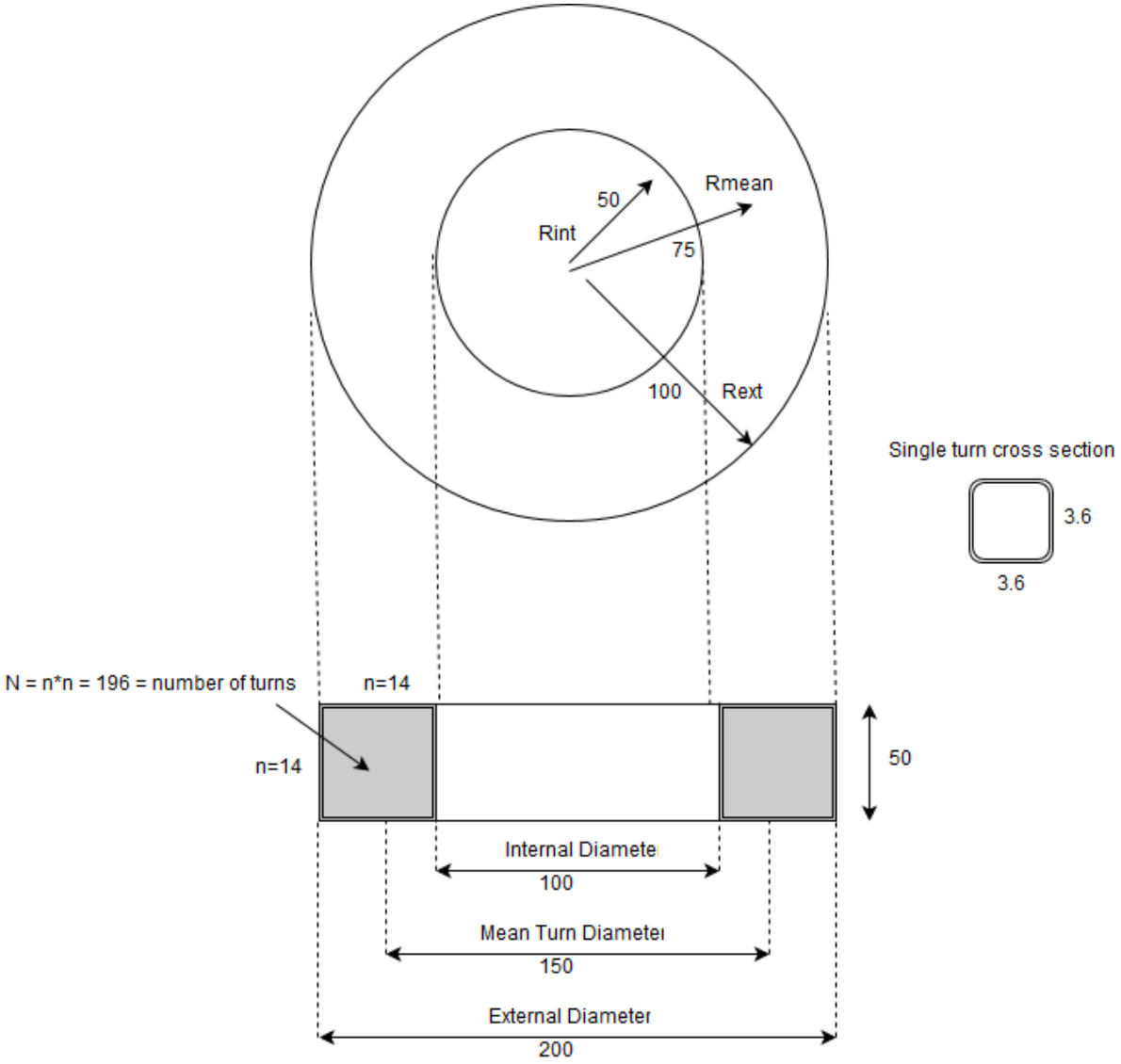


Figure 14-3: 4.9 mH 50 A air cored inductor

In general, it might be very expensive to build two inductors respecting this design, due to the necessity of building a specific winding mandrel. Depending on the budget, it might be decided to change the design using an existing standard mandrel, which main drawback is the rectangular section and the necessity to adapt and approximate all the Brooks inductor calculations for that geometry.

For this project, two custom mandrels have been designed by the Electrical and Electronic Engineering workshop of the University of Nottingham.