



Triangular/Trapezoidal Current Mode for High Step Ratio Modular Multilevel dc-dc Converter

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To Nayeth, my parents, teachers, colleagues and friends.
Thank you for all of your support along the way.

Abstract

Recent developments in dc powered technologies have increased interest in highly efficient dc-dc converters, especially at high voltage and high-step voltage ratios. Modular multilevel converters (MMCs) are an attractive alternative approach to this demand because they can manage medium and high dc voltages while using standard semiconductor devices with high efficiency if they employ soft-switching techniques. However, the latest soft-switching techniques proposed to MMCs require resonant circuits, limiting their operation.

This thesis proposes a new zero-current switching modulation technique for a high-step-ratio MMC dc-dc converter without resonant circuits. The proposed modulation generates trapezoidal or triangular current as result of a rms current minimization problem. The proposal enables the soft-switching operation of the converter over a wide output voltage and power range, using a simple control scheme to regulate the output voltage and the voltage balance among the floating cell capacitors.

The effectiveness of the proposed control strategy is validated through simulations and experimental results. Simulation results are obtained for a 1MW, 10kV to 1kV converter model developed in PLECS software. Additionally, a 1 kVA downscale prototype has been designed and constructed during this Ph.D.

Simulation and experimental results for steady-state, bidirectional power-flow, and input voltage and load disturbances have confirmed the successful operation of the triangular/trapezoidal current mode. In all the experiments, the proposed control systems ensure proper capacitor voltage balancing, proving that the converter has satisfactory dynamic response and cell voltage balance over a wide output voltage and power range.

List of Publications

I. Journal Papers

i. **C. Pineda**, J. Pereda, F. Rojas, G. Droguett, C. Burgos-Mellado and A. J. Watson, "Optimal ZCS Modulation for Bidirectional High-Step-Ratio Modular Multilevel dc-dc Converter," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2021.3078235. Q1

ii. **C. Pineda**, J. Pereda, F. Rojas, C. Cerda, X. Zhang and A. J. Watson, "Asymmetrical Triangular Current Mode (ATCM) for Bidirectional High Step Ratio Modular Multilevel Dc–Dc Converter," in IEEE Transactions on Power Electronics, vol. 35, no. 7, pp. 6906-6915, July 2020. Q1

II. Conference Papers

i. **C. Pineda**, J. Pereda, C. Burgos-Mellado, A. Watson and F. Rojas, "Zero-Current Switching (ZCS) for a High Step Ratio Modular Multilevel dc-dc Converter with wide voltage range operation," 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), 2020, pp. 1-8.

ii. C. Cerda, F. Rojas, **C. Pineda**, J. Pereda, M. Diaz and G. Gatica, "Grid Forming Operation for a High Step Ratio Modular Multilevel DC-DC Converter," 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2020, pp. 494-498.

iii. C. Cerda, F. Rojas, **C. Pineda**, J. Pereda, M.Diaz, J. Salgado and G. Droguett, "Inductor design for a High performance DC-DC Modular Multilevel Converter," 2019 IEEE CHILEAN Conference on Electrical, Electronics Engineering, Information and Communication Technologies (CHILECON), Valparaiso, Chile, 2019, pp. 1-7.

iv. **C. Pineda**, J. Pereda, S. Neira, P. Bravo, J. Rodríguez and C. García, "Trapezoidal Current Mode for Bidirectional High Step Ratio Modular Multilevel dc-dc Converter," 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), Santos, Brazil, 2019, pp. 1-6.

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Chapter 1

Introduction

The modern electrical infrastructure is the result of a continuous technical-economical discussion along its history. At the ending of the 19th century, during the early development of electric power systems there was much discussion about whether the direct current (dc) or alternating current (ac) should dominate systems used for the generation, transmission and distribution of electrical energy. This dispute, historically knew as "the battle of the currents", ended in favor of the use of ac, mainly for three reasons: (i) the ability to efficiently step voltage up and down due to the development of the ac transformer, (ii) high power generation capability resulting from advances in the development of turbines and ac generators and (iii) efficient power consumption in industrial processes resulting from the poly-phase ac motors [1]. Since then the electric transmission and distribution networks have been predominately ac.

The transmission of electricity using High voltage direct current (HVDC) systems are the exception. HVDC transmission has been demonstrated to be an economically and technically attractive option, mostly in specific point-to-point transmission systems such as those required for offshore wind farms and long transmission lines [2]. Over long distances as well for submarine lines, dc power transmission has significant advantages over ac, including lower power losses, reduced cabling requirements and the absence of reactive power.

Compared to ac transmission, however, there is a requirement for conversion stations which are used to link the HVDC system with the existent ac infrastructure. Nevertheless, for short and medium distances, this alternative has been economically unattractive. Thus, the dc based transmission or distribution power systems were mainly viewed as niche.

However, in recent years this situation has begun to change. The high penetration of renewable energy sources and the development of efficient power electronics systems in the grid is changing how power systems are constructed and operated. This change is also driven by the fast incorporation of (i) solar photovoltaic (PV) and wind power sources, (ii) energy storage systems, (iii) electric vehicle (EV) chargers, (iv) big data centres and (v) new HVDC grids. The growth of renewable energy has been continuous in recent years, reaching over 25 % of the total world energy generation in 2019 [3]. Among all renewable energy sources, wind and solar PV energy represent the biggest and fastest growth. Furthermore, this growth is expected to continue to develop in the future. According to the International Energy Agency, wind and PV sources will provide more than half of the additional electricity generation by 2040 [4]. Thus, the global generation matrix is rapidly changing from fossil combustibles to the wind and solar PV power.

The intermittent nature of these renewable power has a significant influence on the stability of power systems. Thus, battery energy storage systems (BESS) have begun to appear on electrical networks for short-term peak power and as a frequency-response reserve, in order to stabilise these new unpredictable energy sources. It is expected that the use of BESS and other energy storage technologies will increase in the grids of the future, as the penetration of renewable energy also increases.

The nature of loads of our grids has also changed significantly in recent years. One of the biggest challenges that the electrical infrastructure is likely to face will be the rise of electro-mobility. The global stock of electric vehicles (EV) was 5 million in 2018, an increase of 63% from the previous year [4]. Fur-

thermore, EV sales are forecasted to surpass 3.5 million per year by 2030 [5]. Following this, the number of EV charging points worldwide will increase dramatically to supply this enormous demand for electrical energy. Therefore, the electricity infrastructure at the distribution level is expected to have to adapt to this new scenario quickly.

Another trend is the need for more and bigger data centres. As the world becomes increasingly digitalised, data centres are emerging as an important source of energy demand. The global data centre electricity demand is estimated to account for around 1% of the worldwide electricity usage, and it is expected to growth continuously [4]. As a result of advances in storage-drive density and data centre power usage effectiveness, the recent trend has been to build large data centres [6]. Thus, how these new data centres are supplied with energy is a matter under discussion.

Finally, the HVDC systems are starting to be proposed beyond the point-to-point transmission systems. The development of the voltage source converter (VSC) has enabled the potential for multi-terminal connection of various HVDC stations, allowing the production of large meshed and radial HVDC networks [7, 8]. Thus, it is predictable that a new family of large HVDC grids will develop, potentially allowing wide sharing of the total power resources in large regions and continents [9].

These advances have enabled the resurgence of dc power systems due to the native usage of dc current in all these new technologies. Dc grids have been widely discussed for solar PV energy [10], offshore wind farms [11], EV fast chargers [12], BESS [13], data centers [14] and HVDC multiport systems [15, 16]. Thus, the future networks could increasingly utilize dc, as is shown in Fig. 1.1, to reduce the number of ac/dc converters in the grid and to bring the advantages of dc power transmission into the medium and low voltage range [17]. In fact, recent dc distribution network market forecasts predict over a 7 % of compound annual growth rate for the period 2020-2025 [18, 19].

However, the massive penetration of dc power networks will take time because

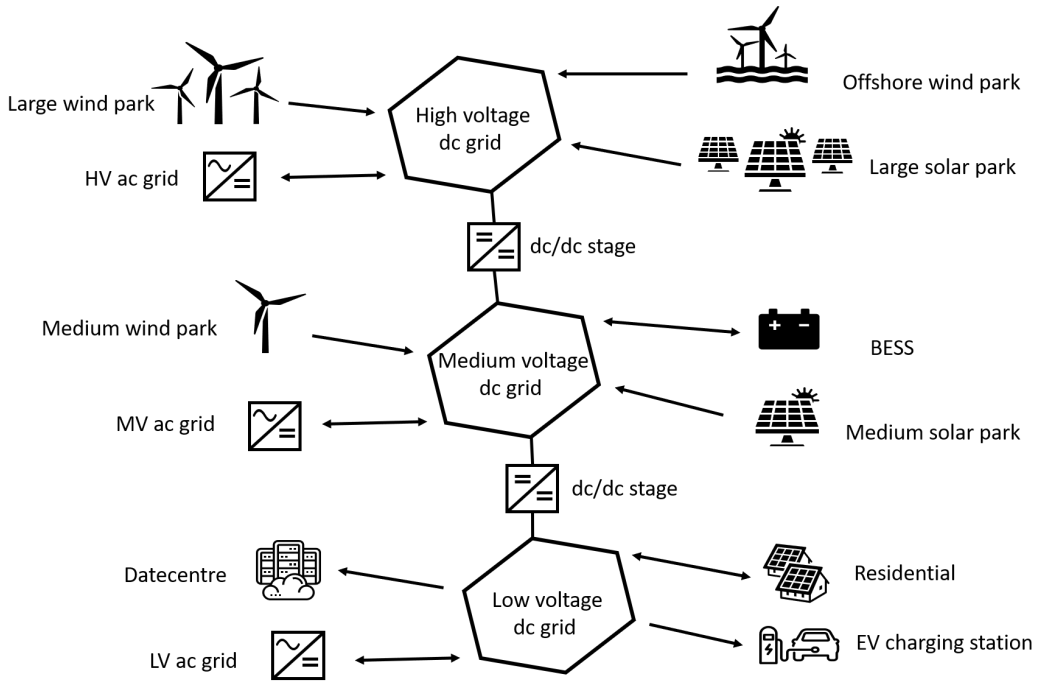


Figure 1.1: *Dc grids of different voltage levels.*

it must displace the actual ac infrastructure and there is still a competitiveness gap between the dc conversion technology and the mature ac transformer, especially for high and medium voltage range [20, 21]. Since dc-dc converters are constructed with expensive solid-state devices, the major concern is their economic feasibility. Furthermore, there is still room to improve their reliability and efficiency [22].

Therefore, the next generation of high efficiency dc-dc power converters is the enabling technology for the development of the new electrical infrastructure and the establishment of dc meshed grids. For this, the dc transformer should provide bidirectional power flow, voltage control, black-start functionality and high step voltage ratio for the links between different voltage level dc buses.

For high and medium voltage, several dc-dc converter topologies have been proposed, but there are two proposals that stand out for their high reliability, modularity and flexibility: the input-series output-parallel (ISOP) converters, based on dc-dc building blocks [23–29]; and the front-to-front modular multilevel (FTF-MMC) converter [30–35].

The FTF-MMC comprises two MMCs connected via an ac medium-frequency

transformer link in an effort to reduce the size of the transformer and other passive elements of the converter [36]. This solution provides full bidirectional power flow control, galvanic isolation and the voltage level can be easily scaled using standard power device technology. However, the hard-switching operation increases the power losses, and one MMC is not necessary when it is connected to a low voltage port. Thus, the FTF-MMC is not suitable for the interconnection between low and medium voltage dc grids with a high voltage ratio.

Resonant MMC dc-dc topologies have been proposed for high step voltage ratio to address these problems [37–45]. In these proposals, one MMC is replaced for a standard two-level converter for better voltage utilization at the low voltage port. Furthermore, this approach enables soft-switching operation to decrease power losses. In order to achieve the soft-switching in the semiconductor devices, these proposals used a resonant tank formed of the capacitors of the MMC cells, which is excited by a square wave voltage at the resonant frequency. Thus, the voltage control through the variation of the operating frequency [46, 47] and of the width of the voltage pulse [48] have been the most employed control techniques. However, operation at a frequency different to the resonant frequency is more complex to model, and the soft-switching capability may be lost, limiting the power range in which the converter is highly efficient. Furthermore, the resonant operation is highly sensitive to the parameters of the resonant tank, requires a design that carefully considers parasitic elements, and generates high peak current in the ac link. This high peak current may cause high conduction losses and a reduced efficiency despite its soft-switching capability [46, 48].

An alternative to the resonant operation are the triangular and trapezoidal current mode (TCM) schemes that have been proposed for dual active bridge (DAB) dc-dc converters [49–51]. TCM achieves zero-current switching (ZCS) in the semiconductor devices without resonance; therefore, the design process and control scheme is simpler than that utilizing resonance. Furthermore,

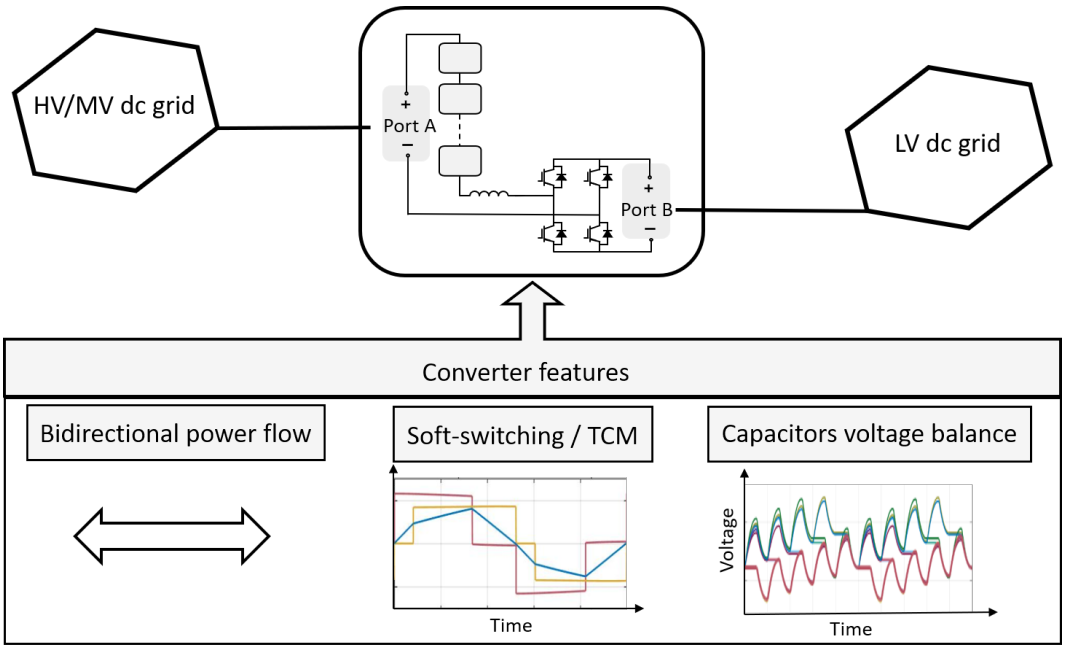


Figure 1.2: *High step ratio MMC dc-dc for the interface between dc grids.*

TCM enables the soft-switching over a wide operating range, extending the high-efficiency performance over the full power range. However, TCM has been barely researched in MMC dc-dc topologies [52–54].

This PhD project aimed to investigate the application of the TCM technique in a high step ratio MMC dc-dc converter for the interconnection between low and medium voltage dc networks (Fig. 1.2). In order to achieve this, the converter should provide high efficiency and bidirectional power flow whilst ensuring the energy storage in the converter is maintained and balanced across the cells..

1.1 Hypotheses

The following hypotheses are stated for this research project:

1. The MMC is suitable for the high voltage step ratio dc-dc stage required for the link between low and medium voltage dc grids.

2. It is possible to achieve soft-switching operation in the MMC dc-dc converter through new control schemes and without the need of a resonant tank.

3. TCM can be implemented in MMC dc-dc converter to provide zero-current switching, high dc-dc voltage step ratio and bidirectional power flow.

4. A control scheme can be developed and optimized to ensure proper capacitor voltage balancing for a wide voltage and power output.

1.2 Objectives

This PhD research project aims to contribute to the state of the art of MMC dc-dc converters for the interconnection of medium and low voltage dc grids. Thus, the following objectives are defined:

1. To develop of a general model of the MMC dc-dc converter with non resonance operation.

2. To optimise of the TCM scheme to the MMC dc-dc converter in order to achieve a bidirectional power flow, cell voltage balancing and zero-current switching in a wide power and voltage operating range.

3. To develop of a control strategy which enables grid forming and typically required operational functionality.

4. To design of a scaled-down prototype to validate the performance, capacitors voltage balancing and soft-switching operation of the TCM control scheme applied in the MMc dc-dc.

1.3 Thesis outline

The thesis structure is divided into seven chapters, as follows:

- Chapter 2: A summary of power converters and control strategies for dc-dc conversion in the medium voltage range is presented. Additionally,

an overview of multi-cell topologies with an emphasis on the MMC dc-dc converter topology is addressed in this Chapter.

- Chapter 3: The presentation of the high-step ratio MMC dc-dc and a model avoiding resonant operation is made in this Chapter. The asymmetrical triangular and trapezoidal current modes are proposed for steady-state operation under the assumption of having fixed voltages at input and output ports. For the trapezoidal case, the steady-state solution defines a set of general solutions which have two degrees of freedom. Thus, an optimisation problem is defined and solved to find a suitable solution. In this Chapter, the current stress is minimized to optimize the utilization and sizing of the switches and passive components. The trapezoidal optimisation problem is solved for a wide voltage and power range, showing that trapezoidal and triangular current modes are complementary modes for an optimised modulation.

- Chapter 4: The control system for the dynamic regulation of the MMC dc-dc output voltage is discussed, considering the low voltage port as a load. Thus, the operation is extended to a variable output voltage and flexible cells stack modulation. Also, two different cell stack modulation strategies are proposed to generate a three-level voltage controlled by transitions times. In the first modulation proposal, the cells are modulated with the same waveform using a phase shift to reduce the resultant switching-frequency. The second modulation proposal is implemented with a sorting algorithm for energy control of the converter cells.

- Chapter 5: The simulation results of the proposed converter are presented in this Chapter. The full-scale converter is simulated for the interconnection between a 10kV and a 1.1 kV dc grid. A set of simulation tests for bidirectional operation, cell capacitor voltage balancing, voltage transient response, and grid forming capability are presented.

- Chapter 6: This Chapter discusses the design and construction of a scaled-down prototype which will be used to validate the work in the previous chapters. The characteristics of the converter, magnetic components, control platform and dc power sources are detailed.

- Chapter 7: The experimental results of the proposed converter are presented in this Chapter. A set of tests for bidirectional operation, capacitor voltage balancing, voltage perturbations and grid forming are discussed.

- Chapter 8: The conclusions, main contributions and a perspective for further improvements are presented in this Chapter.

Chapter 2

State of the art of high and medium voltage dc-dc converters

2.1 Introduction

In this Chapter an extensive review of the state of the art of high and medium voltage dc-dc converters is presented. Based on recent literature, a vast amount of topologies are classified into three categories according to their structure. Also, a discussion of the features, advantages and limitations of each family is carried out, considering isolation, optimal voltage step ratio, bidirectionality, modularity and control complexity.

This Chapter also provides an overview of existing control strategies for dc-dc converters. Finally, a discussion of current modulation techniques at an ac-link stage is presented. A particular emphasis is made on those alternatives that provide soft-switching.

2.2 Topologies

Although several techniques to achieve dc-dc conversion are widely known for low voltage ratio [55, 56], the adaptation of these techniques to medium and high voltage is not straightforward. The main issue is the voltage limitation of the current semiconductor devices. Therefore, high voltage converters require the interconnection of several low voltage devices or sub-converters, restricting the use of the traditional conversion strategies.
Several methods have been proposed to address this problem, which can be classified according the utilization of an intermediate ac stage. Thus, they can categorized into three topology families:

1. Centralised ac-link.

2. Distributed ac-link.

3. Direct dc-dc.

The centralised ac-link type rely on a dc-ac-dc conversion scheme (Fig. 2.1 (a)), the distributed ac-link category modularize the ac stage by using several low voltage ac-links (Fig. 2.1 (b)), and the direct dc-dc topologies lack an intermediate ac stage (Fig. 2.1 (c)),

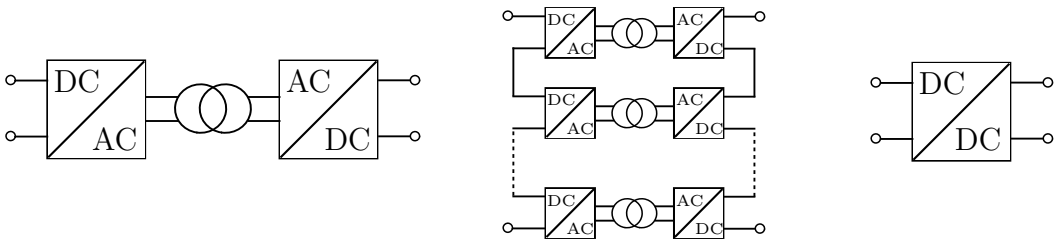


Figure 2.1: *Possible structures for dc-dc conversion: (a) Centralised ac-link type , (b) Distributed ac-link type, and (c) Direct dc-dc type.*

The proposed classification of the literature review using those categories is summarized in Fig. 2.2 and a brief description of each of them is presented in following subsections. Similar classifications are presented in [57, 58].

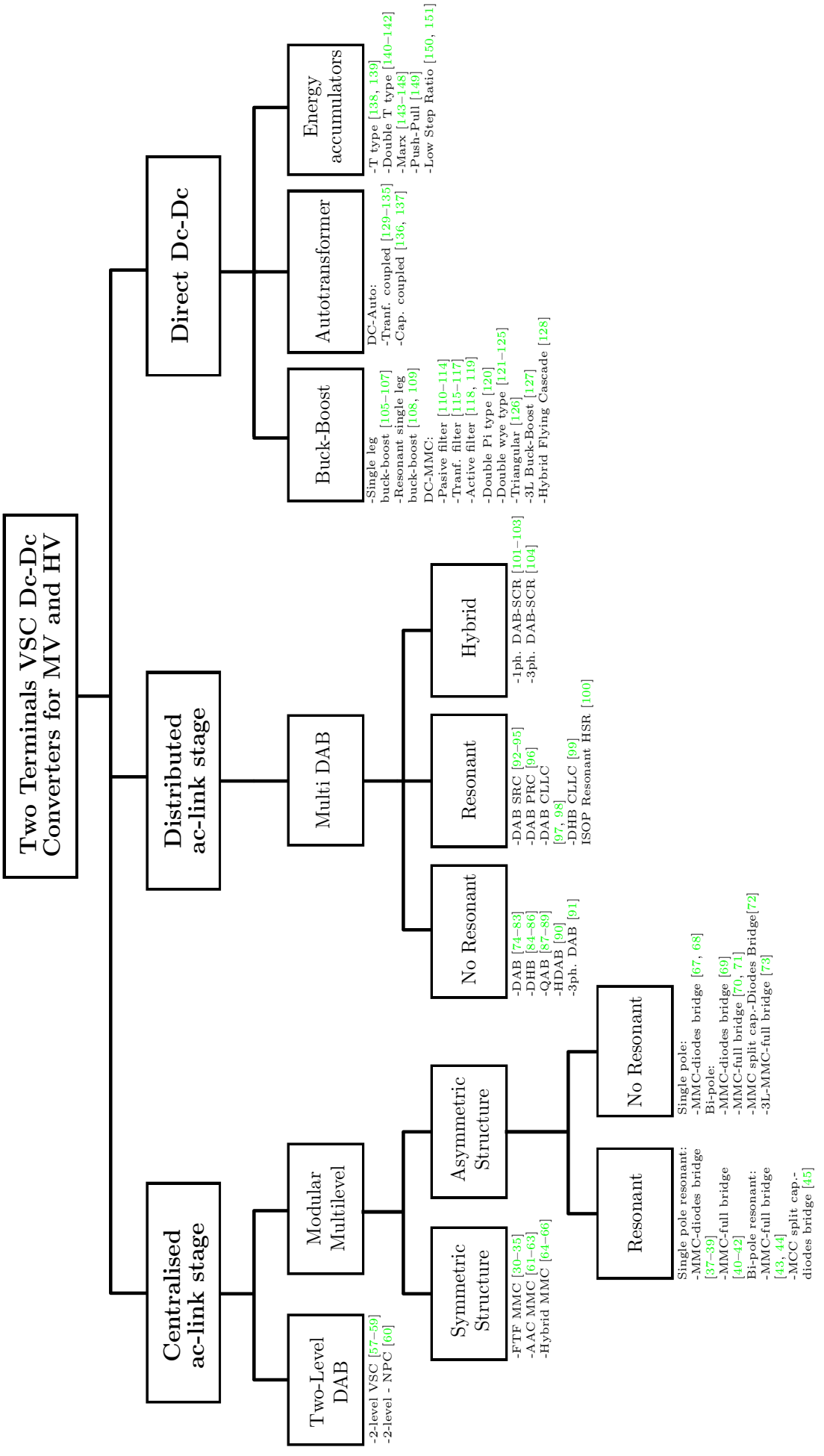


Figure 2.2: *Classification of two terminals VSC Dc-Dc converters for MV and HV.*

2.2.1 Centralised ac-link

The topologies with a centralised ac-link stage rely on a dc-ac-dc conversion scheme with two ac-dc conversion stages. These two ac-dc converters are connected through an ac-link, commonly formed using a single transformer, which is designed for high or medium-frequency operation to reduce the size and weight of the passive components. The transformer also provides galvanic isolation and voltage scaling between ports. The isolation capability is commonly demanded for safety and, in case of failure, to prevent the presence of dangerous voltages at low voltage port. Also, it allows separated grounding systems of both dc ports. Furthermore, the turns ratio of the transformer can be adjusted to meet the voltage requirements of the dc ports, providing an additional scaling to the voltage step ratio if it is needed. Thus, these topologies can achieve higher voltage step ratios than the direct dc-dc alternatives.
Because of the voltage rating limitations of modern semiconductor devices, three strategies have been proposed to adapt the centralised ac-link topologies to MV/HV:

1. Two level dual active bridge using series switches.

2. Symmetric modular multilevel dc-ac-dc converters.

3. Asymmetric modular multilevel dc-ac-dc converters.

Two level dual active bridge using series switches

The dual active bridge (DAB) is one of the most popular topologies which relies on a dc-ac-dc chain conversion structure [152]. Each dc-ac conversion stage is implemented using a H-bridge, which are then connected together using a medium-frequency transformer. Thus, this solution can provide galvanic isolation, high voltage step ratio and bidirectional power flow if the H-bridges are actively controlled. However, the voltage rating of standard semiconductor devices limit their use in HV applications.

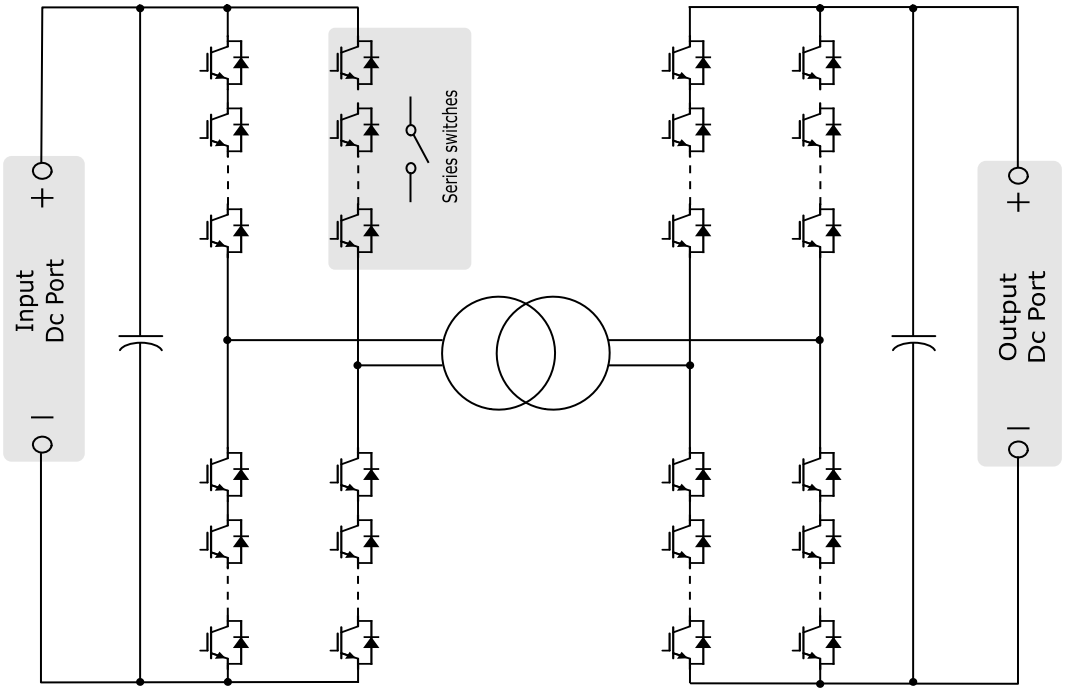


Figure 2.3: *Two level dual active bridge using series switches*

To reach higher voltage ratings, the semiconductor devices of the traditional H-bridge can be replaced by a series connection of several low voltage devices [58], as is shown in Fig. 2.3. Thus, this structure allows scale-up the voltage rating to MV/HV.

If the series switches in each arm are controlled simultaneously, their operation is equivalent to a two level DAB. Thus, each converter can impose a two-level square voltage at the ac-link. The power flow control between ports is achieved by manipulating the duty-cycle and phase-shift of these two square voltages.

Some modifications of this structure have been studied in recent literature. The two-level version of the DAB (using single or series connected semiconductor devices) can be extended to operate with a three-phase ac-link by adding an extra leg in each H-bridge [57]. This can improve the total power density and the design of the ac-link transformer [152]. Furthermore, when a low voltage dc port is present, a combination of single or series switch H-bridges can be used on the two sides of the converter. The lower voltage side can also be replaced with an NPC converter for MV links [59, 60].

The series switches DAB structure presents several issues for a reliable oper-

ation at high voltage. The main drawback is the need for additional control methods or external circuits to ensure the voltage balance among the devices both during static (on or off) and the dynamic transient states [153]. Usually, complex gate-drive methods or additional snubber circuits are needed. Also, the high dv/dt of the ac-link may result in premature failure of transformer insulation and produce high levels of electromagnetic interference (EMI) [154]. Therefore, the series connection of devices is generally avoided.

Symmetric modular multilevel dc-ac-dc converters

In recent years, modular multilivel converters (MMCs) have risen as an attractive solution for power transformation in the MV/HV range due to their high performance, good transient response and reliability [155–157]. MMCs can be used to interface ac and/or dc networks, and they have been proposed for several applications, such as: offshore wind farm [158, 159], photovoltaic power plants [160–162], solid state transformers [163–165], electrical drives [166, 167], and HVDC transmission systems [168, 169].

For dc-dc conversion, the dc-ac-dc front to front modular multilevel (FTF-MMC) converter is one of the most studied topologies at MV/HV range [30–35]. The FTF-MMC uses two MMCs connected through a medium frequency transformer, as is shown in Fig. 2.4 (a). This structure can be seen as a DAB with series switches where the semiconductor devices are replaced by controllable voltage source cells, using half-bridge (Fig. 2.4 (b)) or full-bridge (Fig. 2.4 (c)) cells. For this reason, the topology is also known as a modular multilevel DAB. The cell stacks composed of half-bridges can generate only positives voltages while the full-bridges can generate bipolar voltages. Additionally, the full-bridge alternative add dc fault blocking capability.

In contrast with the series switch DAB, each cell of the FTF-MMC is independently controlled and handles only a fraction of the dc port voltage, allowing a multilevel voltage at the ac link. This structure dramatically reduces the dv/dt in the ac waveform in comparison with the series switch based DAB.

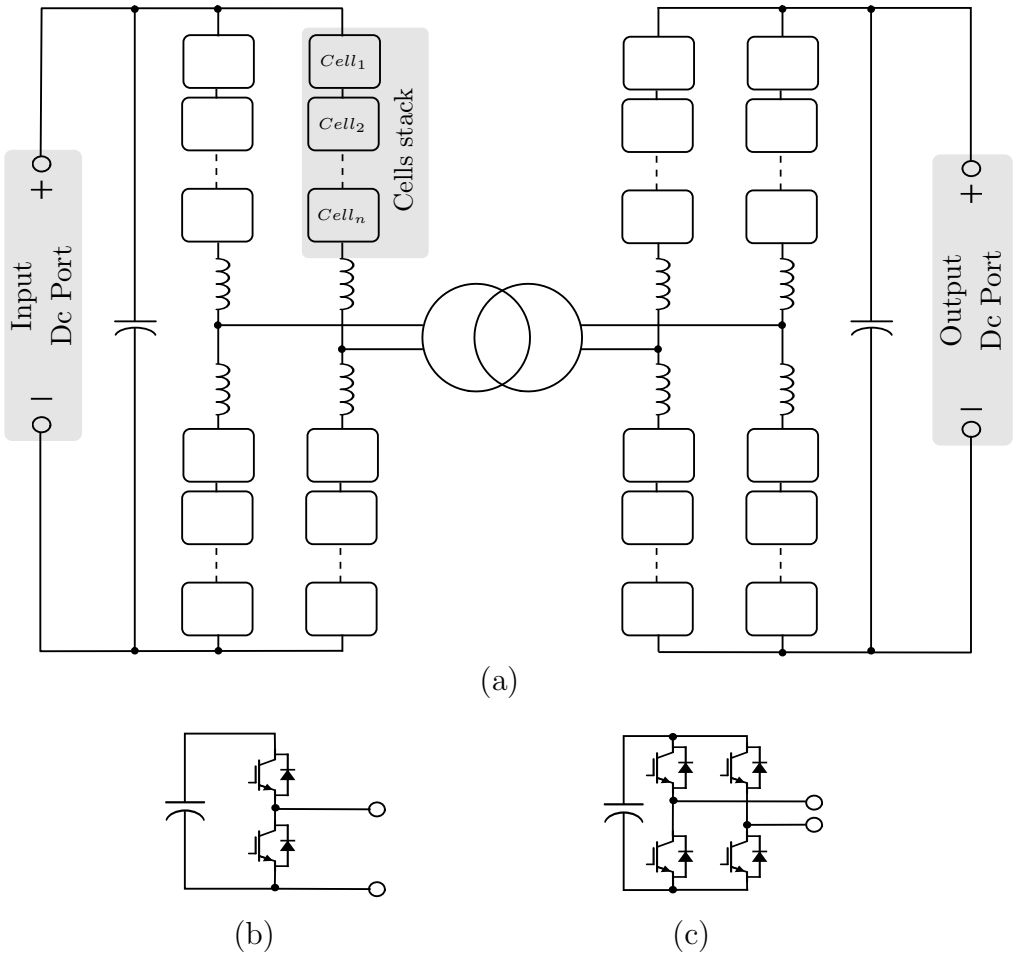


Figure 2.4: *(a) FTF-MMC topology*

Furthermore, this topology provides full bidirectional power flow control and galvanic isolation. Unfortunately, the cost of this flexibility is that the topology requires dedicated control strategies to maintain the capacitor voltage balance of the cells and their hard-switching operation reduces efficiency, especially when used to produce a high step ratio voltage transformation.

Some modifications of the FTF-MMC have been proposed. The FTF-MMC can be extended to a three-phase ac-link by adding an extra leg to each MMC [32–34], or the structure of the cell stacks can be modified by replacing some cells with director switches (Fig. 2.5) [61–65]. The latter, which are part of a family of converters known as hybrid MMCs, can reduce the size and cost of the converter and improve their efficiency [63].

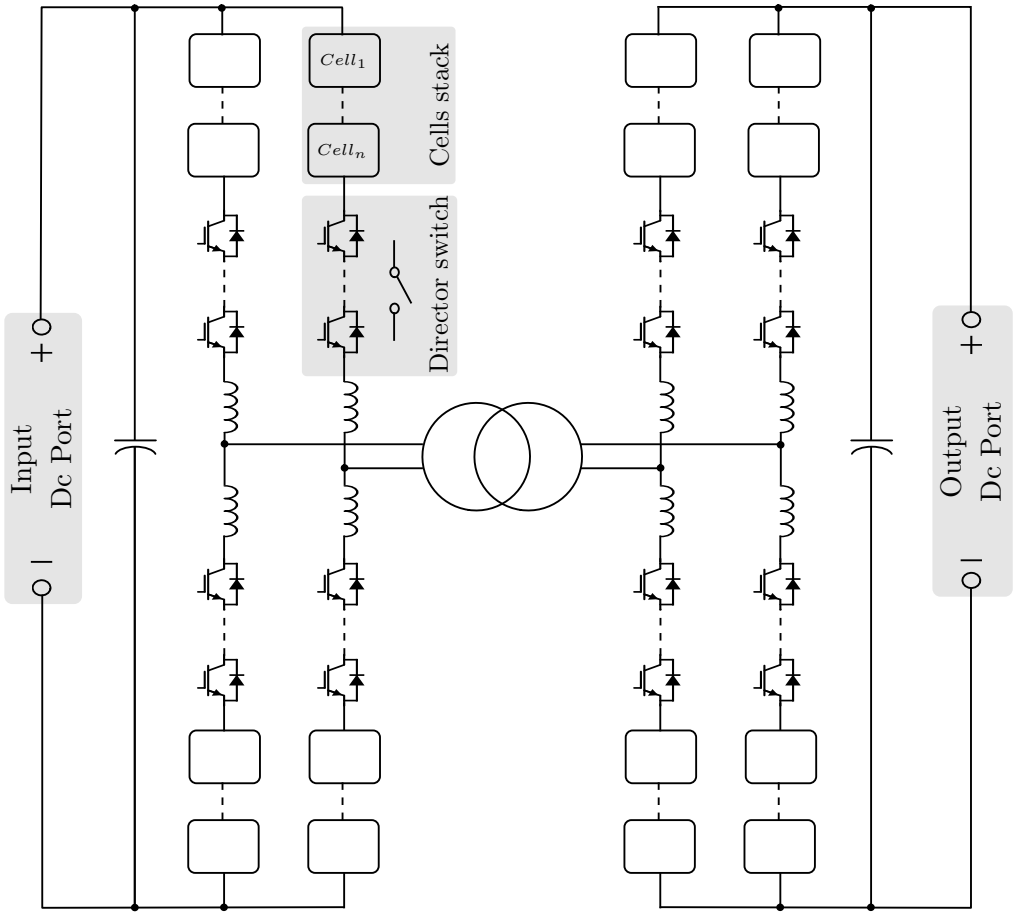


Figure 2.5: *Hybrid MMC topology.*

Asymmetric modular multilevel dc-ac-dc converters

When a low voltage port is present, an asymmetrical structure may provide better voltage transformation whilst using standard rated semiconductor devices [38]. The asymmetrical structures replace one MMC with a two-level low voltage ac-dc converter, whilst keeping the MMC at the high voltage port. The first asymmetrical proposals use a single diodes bridge as low voltage ac-dc converter, simplify the MMC to a single stack of cells, and add a resonant network at the ac-link, as is shown in Fig. 2.6 (a) [37–39]. This resonant tank can be configured using various networks such as the series LC (Fig. 2.6 (c)), LLC (Fig. 2.6 (d)), etc [170]. Furthermore, the capacitor cells can be used to form part of an equivalent series capacitance in the resonant tank [37–42]. Since the single stack configuration and their restriction of connection to a monopole dc

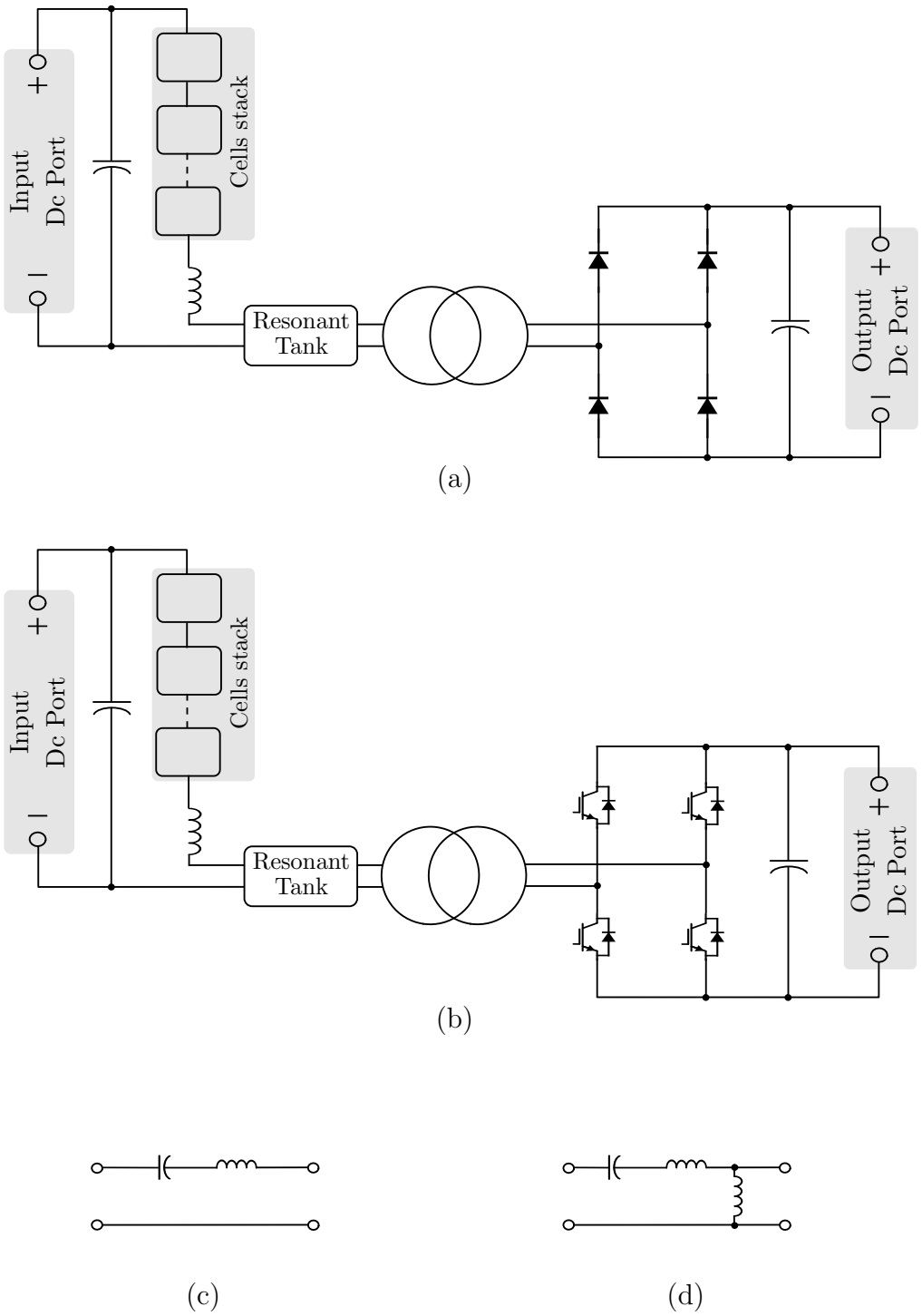


Figure 2.6: *Monopole asymmetrical dc-ad-dc resonant MMC: (a) diodes bridge as low voltage ac-dc converter, (b) full-bridge as low voltage ac-dc converter, (c) series LC resonant tank, (d) LLC resonant tank.*

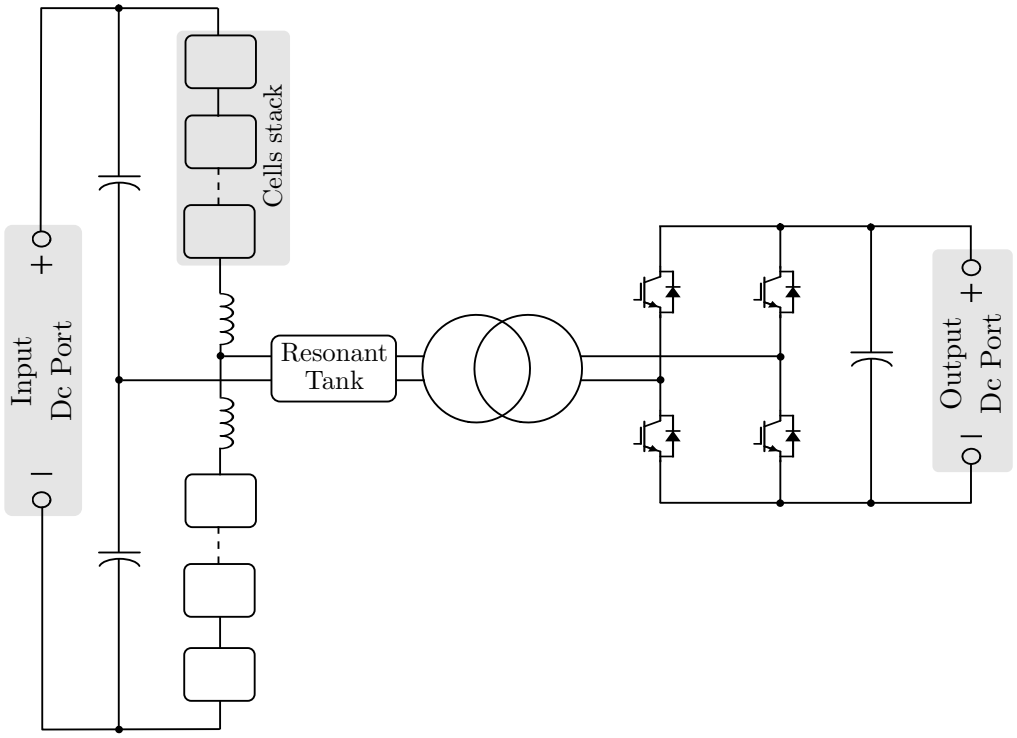


Figure 2.7: *Bipole asymmetrical dc-ad-dc resonant MMC using a full-bridge as low voltage ac-dc converter.*

grid, this topology is also know as monopole asymmetrical dc-ac-dc resonant MMC.

In contrast to the multilevel ac-link voltage of the FTF-MMC, the modulation of a single stack of the monopole asymmetrical dc-ac-dc resonant MMC produces a two-level low voltage at the ac-link. Thus, it is possible to achieve higher voltage ratio between dc ports, because both the cells stack and transformer contribute to the voltage transformation [37]. Furthermore, if the application does not require galvanic isolation, the converter can still link dc ports of different voltages without the need for a transformer [37, 38].

To generate the output dc voltage, the square ac-link low voltage at the secondary of the transformer is then rectified by the diodes bridge. However, it allows power-flow in one direction due to the unidirectional nature of the diodes. To enable bidirectional power-flow, a full-bridge converter can be used instead, as is shown in Fig. 2.6 (b) [40, 41]. Furthermore, the topology can be extended to a bipole type configuration if it include a complete leg and there

is access to the midpoint of the HV dc link, as is shown Fig. 2.7 [43–45].

To reduce the switching losses, all these topologies utilise a resonant operation. For this, the resonant tank is excited by a square wave voltage at the resonant frequency, achieving zero-current-switching (ZCS) in the semiconductor devices. Thus, it is possible provide precise control of the power flow and dc output voltage by manipulating the operating frequency of this square wave voltage [46, 47].

However, the resonant operation has several issues. The main problem is that high efficiency is only achieved for a limited operational range, due to the restricted output voltage and power zones where ZCS is achieved [171]. Thus, these topologies can achieve high efficiency in applications with constant electrical variables because the converter always works near the optimum operating point for which it was designed, however, it loses effectiveness for applications with high variation in their demand curves, such as electrical distribution networks [172]. Furthermore, the design of a resonant converter is considerably more difficult. Since the resonant frequency is usually in the medium/high frequency range, the resonant tank operation can be strongly affected by parasitic and stray components. Thus, the electrical elements and their corresponding printed circuit boards (PCBs) require a design that carefully considers their frequency response [173]. Finally, these resonant converters generate high peak currents and voltages in the passive elements. This high peak current require significant oversizing of these elements and it increases the total conduction losses, leading to low performance despite its soft-switching capability [37].

Therefore, others asymmetrical structures have been proposed which avoid the need for the resonant operation (the resonant tank is therefore omitted) [67–73, 174–176]. These structures are similar to the previous configurations, and are therefore categorised similarly i.e. monopole asymmetrical MMC - diode bridge (Fig. 2.8 (a)) [67, 68], monopole asymmetrical MMC - full-bridge (Fig. 2.8 (b)) [52, 53], bipole asymmetrical MMC - diode bridge (Fig. 2.9 (a)) [69, 72], and bipole asymmetrical MMC - full-bridge (Fig. 2.9 (b)) [174, 175].

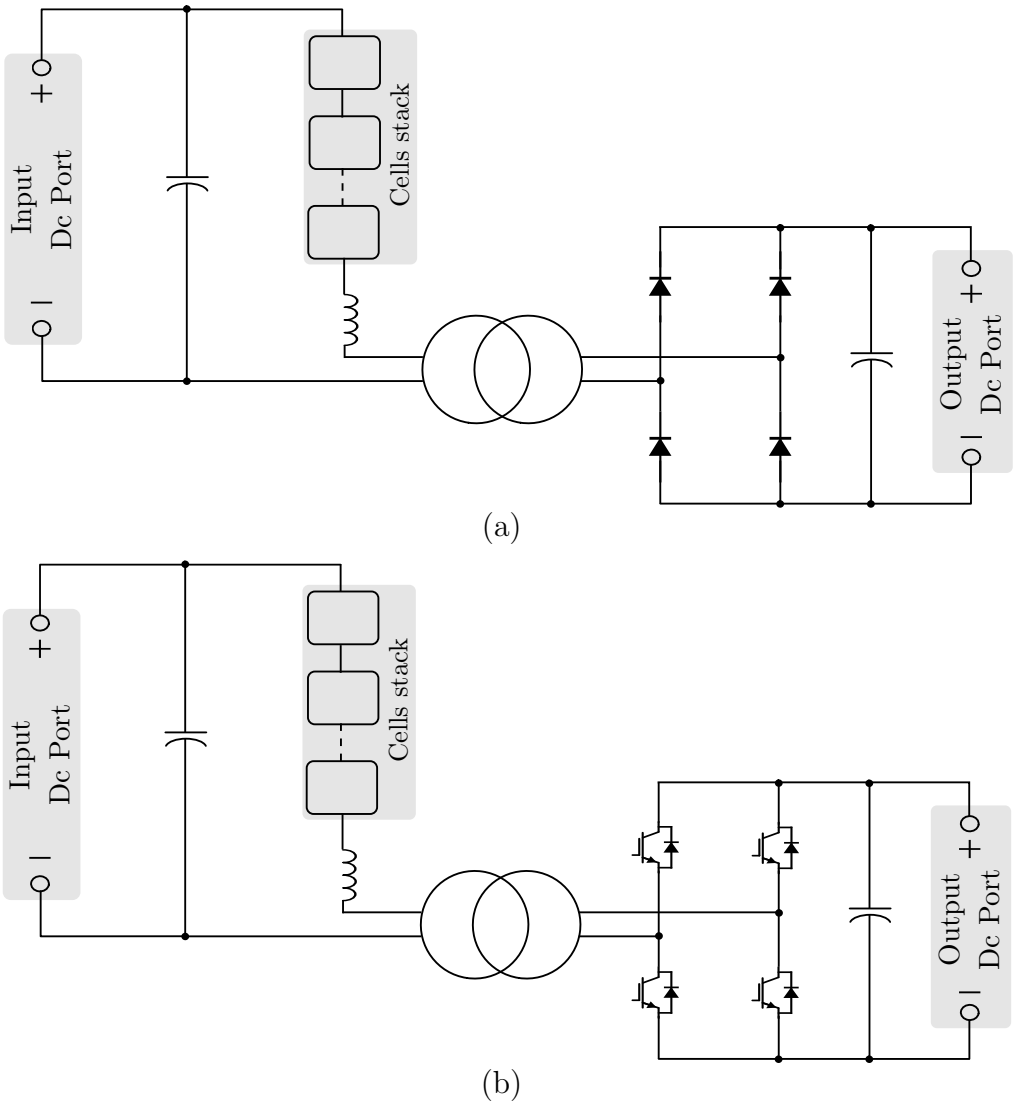
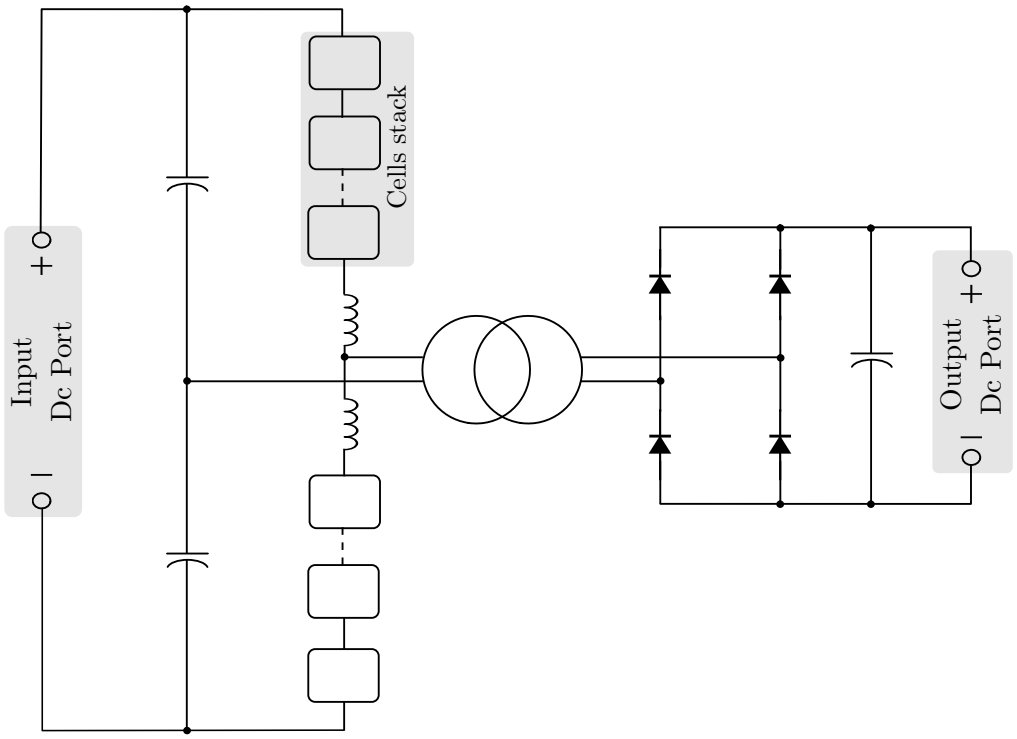
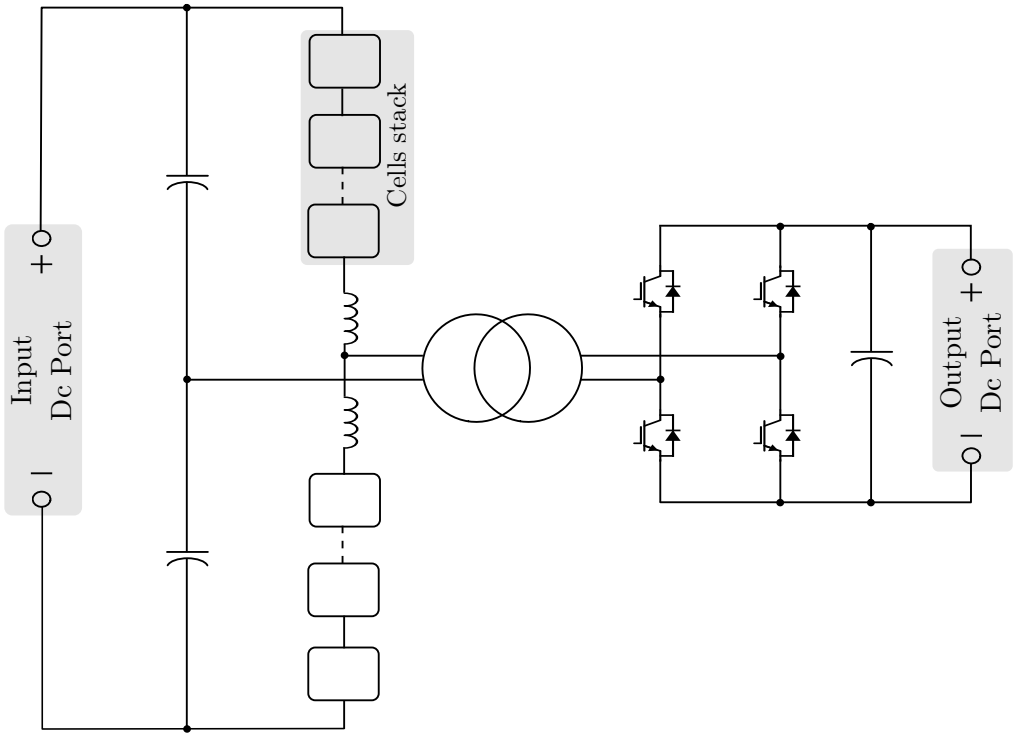


Figure 2.8: *Monopole asymmetrical dc-ad-dc MMC: (a) diodes bridge as low voltage ac-dc converter, (b) full-bridge as low voltage ac-dc converter.*



(a)



(b)

Figure 2.9: *Bipole asymmetrical dc-ad-dc MMC: (a) diodes bridge as low voltage ac-dc converter, (b) full-bridge as low voltage ac-dc converter.*

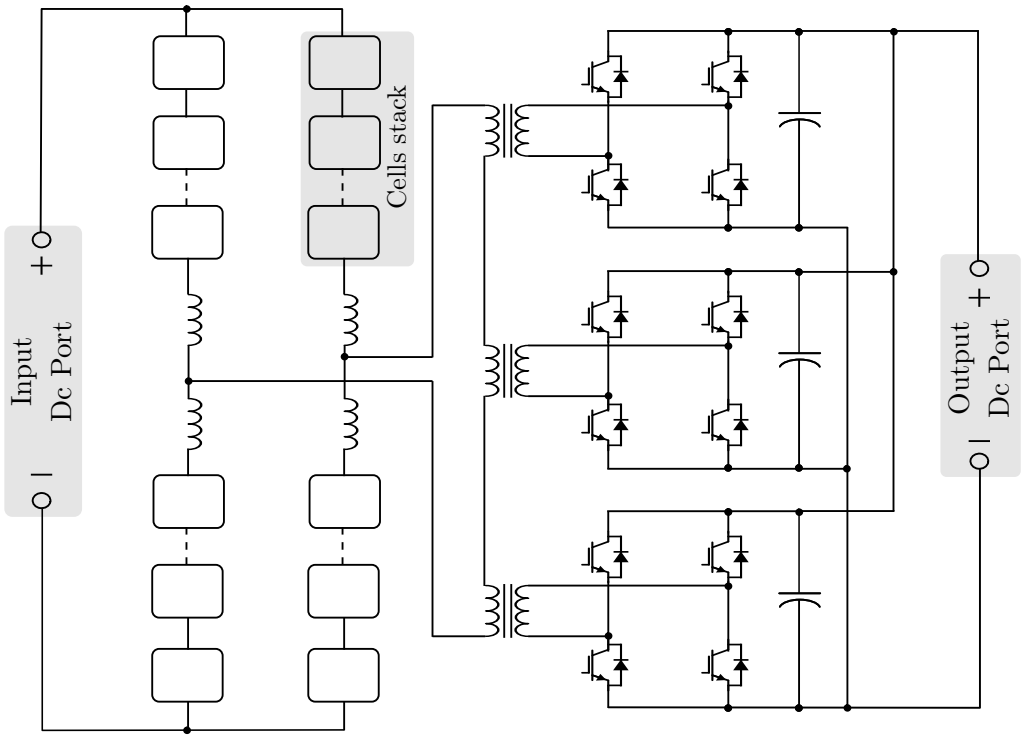


Figure 2.10: *Asymmetrical dc-ad-dc MMC with muti-winding transformer.*

Because of their non-resonant operation, these topologies can extend the high-efficiency performance over the whole power and voltage range, whilst avoiding the issues related with the design of resonant converters. Furthermore, the low voltage ac/dc converter can be implemented with several transformers and low voltage converters in parallel to increase the current capability of the low voltage dc port, as is shown in Fig 2.10 [70, 71, 73, 176]. The primary side of these transformers are connected in series to create the centralised ac-link, whilst the secondary sides are connected to each low voltage converter. Since there is a parallel connection of these converters, it is necessary to implement a control strategy to avoid circulating currents amongst them, which may occur due to inevitable constructive differences in the transformers.

2.2.2 Distributed dc-ac-dc

The distributed ac-link topologies create multiple ac-links using the interconnection of several dc-ac-dc converters. Thus, it is possible to scale these up to

higher power applications, using the traditional low power dc-ac-dc converters as building blocks or cells. Since each dc-ac-dc cell has its own ac-link, this extends the modularity to the ac-link stage, enabling a full modular solution whilst keeping the advantages of the previous family i.e. galvanic isolation, voltage scaling and reduced size and weight of the transformers resulting from the high-frequency operation.

The cells can be interconnected in different configurations to meet the needs of each dc port [177–180]. If the cells are connected in series, the dc current is shared and the voltage is split among all the converters, allowing a higher voltage rating at this dc port. If they are connected in parallel, the dc current is distributed among all the converters, increasing the total current rating on this side of the converters. Since each cell terminal can be independently connected, there are four alternative configurations: i) Input Series - Output Series (ISOS), ii) Input Series - Output Parallel (ISOP), iii) Input Parallel - Output Series (IPOS), and iv) Input Parallel - Output Parallel (IPOP). These four different configurations are illustrated in Fig. 2.11 (a)-(d).

The most common dc-ac-dc cell topology is the dual active bridge (DAB), which has been extensively analyzed in the literature [181]. Each DAB is composed by two low voltage H-bridges, which are linked through a medium-frequency transformer, as is shown in Fig. 2.11 (e). The ac-link inductor, which may be formed from the leakage inductance of a transformer, is used to control power flow through the converter, whilst the input and output capacitors work as filters for the dc ports.

The ISOP and IPOS configurations of DAB cells are one of the most popular topologies to link two dc grids of different voltage levels [74–82]. As a result of their structure, these topologies provide flexibility, modularity, galvanic isolation, high voltage step ratio, and bidirectional power flow. Thus, these multi-DAB converters are considered as a promising technology to interface dc grids. However, these topologies are not suitable for high voltage rating. The main issue is the high insulation requirement of the transformers, despite their

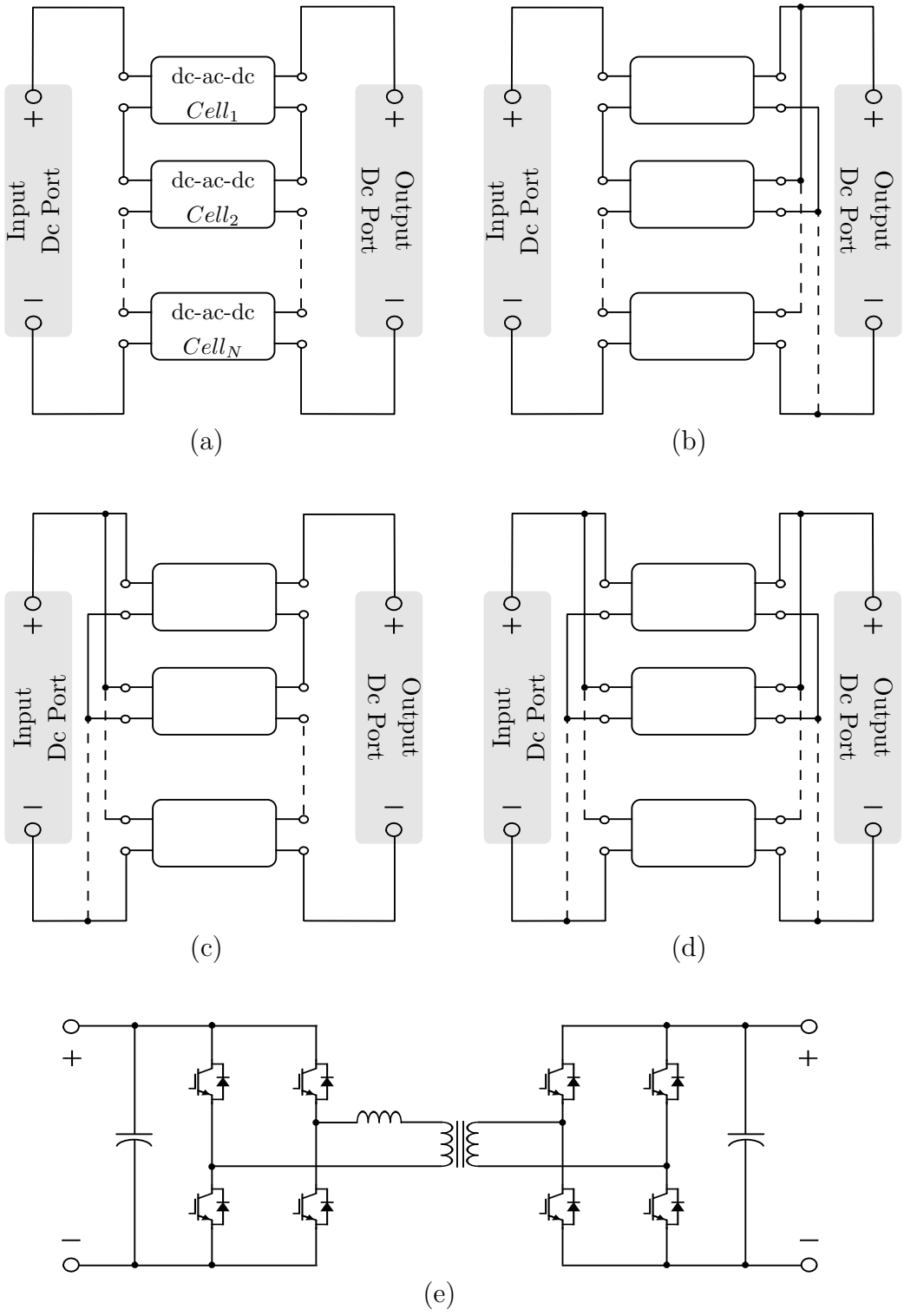


Figure 2.11: *Distributed dc-ac-dc converters: (a) ISOS configuration, (b) ISOP configuration, (c) IPOS configuration , (d) IPOP configuration, (e) DAB cell*

reduced local voltage rating [182]. Resultingly, these topologies are limited to medium voltage range. Also, the parallel connection of DABs requires an additional control loop in order to balance the current among the DABs and avoid undesirable circulating currents [177–180].

Some modifications of the traditional multi-DAB structure have been suggested. Most of these ideas propose changes in the structure of the dc-ac-dc cell. In [84–86], the full-bridges are replaced by half-bridges and split capacitors, as is shown in Fig. 2.12 (a). This reduces the number of devices required per cell, thus lowering cost, but it requires a voltage balance control for the split capacitors to ensure a symmetric ac link. An alternative and more complex cell was proposed in [90]. This dc-ac-dc cell replaces the upper switches of the full-bridges with half-bridges, as is shown in Fig. 2.12 (b). This maintains the advantages of conventional DAB, whilst adding more flexibility to the control [90]. Furthermore, it is possible to use a three-phase link if the H-bridges are replaced by standard converters [91], as is shown in Fig. 2.12 (c). As mentioned above, a three-phase transformer is generally considered to be a more efficient solution than a single-phase transformer.

An important variant of the traditional DAB cell are the resonant DABs. Since the traditional DAB efficiency decreases rapidly when the voltage amplitudes at each side of transformer are different [183], the resonant alternatives have been considered in order to the increase the soft-switching range, and therefore, enhance the converter efficiency. The resonant DABs incorporate a resonant network at the ac-link, which is excited at its resonant frequency [92–99]. This resonant network can be composed of different configurations for the resonant tank [170], the most common being the series LC (Fig. 2.12 (d)), the LLC (Fig. 2.12 (e)) and the CLLC resonant tank (Fig. 2.12 (f)). The LC resonant tank require only an additional capacitor, but it offers a narrow soft-switching range [92–96]. The LLC alternative extends the soft-switching range, and can be formed with only inductor and additional capacitor if the magnetizing inductance of the transformer is used for the parallel inductor component [171].

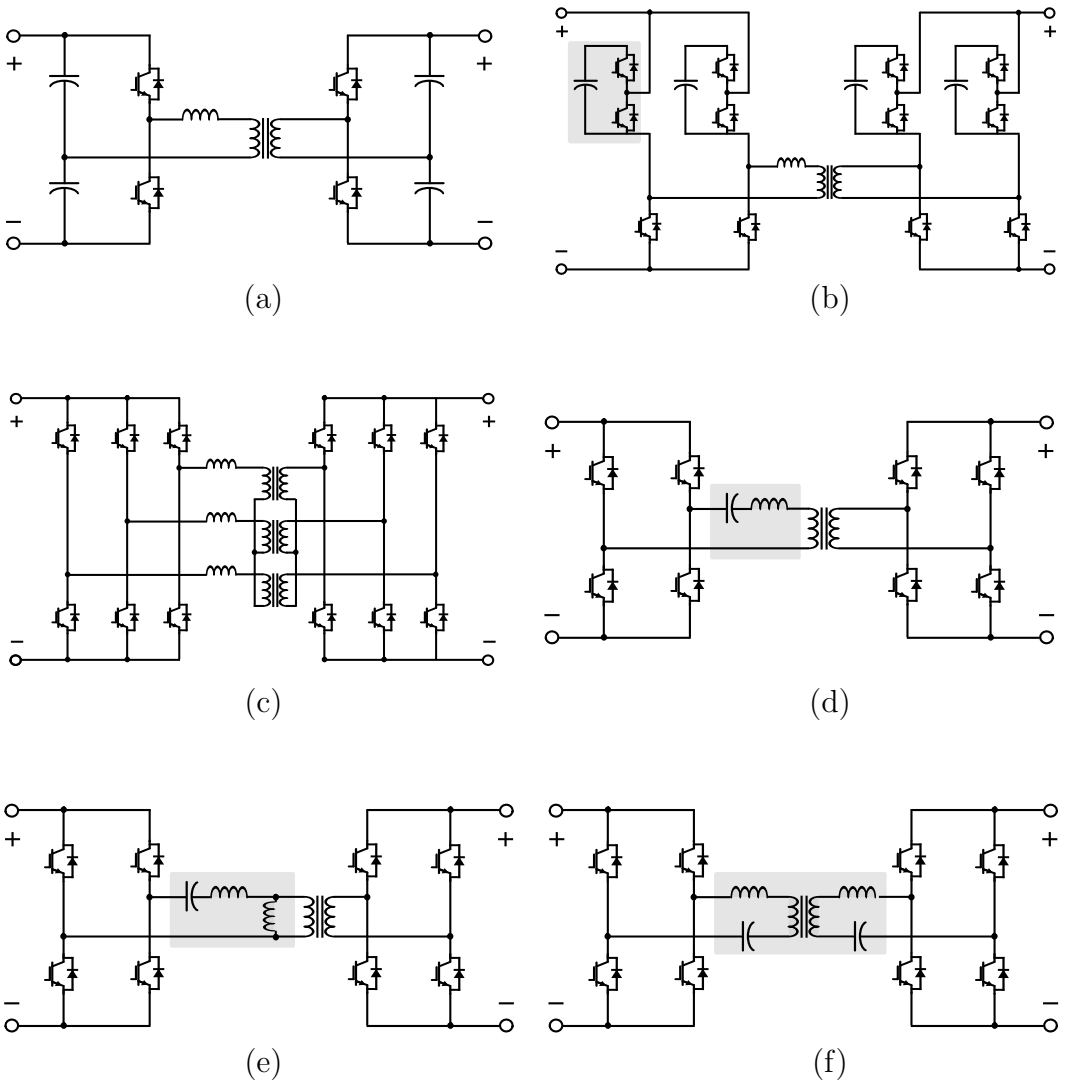


Figure 2.12: *Alternatives DAB cells: (a) Dual half-bridge cell, (b) Hybrid-DAB cell, (c) Three-phase DAB cell, (d) LC series resonant DAB cell, (e) LLC resonant DAB, and (f) CLLC resonant DAB.*

However, the asymmetry of the LLC structure leads to a different operation between when the power flow is reversed. Finally, the CLLC resonant tank has a wide soft-switching range and symmetrical operation for both directions of power flow, but it requires two additional capacitors and an extra inductor [97–99]. Resultingly, the choice of resonant tank depends of the voltage and power operation range of the application.

Finally, recent papers have proposed the hybrid utilisation of cells [101–104]. These proposals use both resonant and traditional cells in an ISOP configuration (Fig. 2.13), benefiting from the high efficiency of the resonant DABs, and

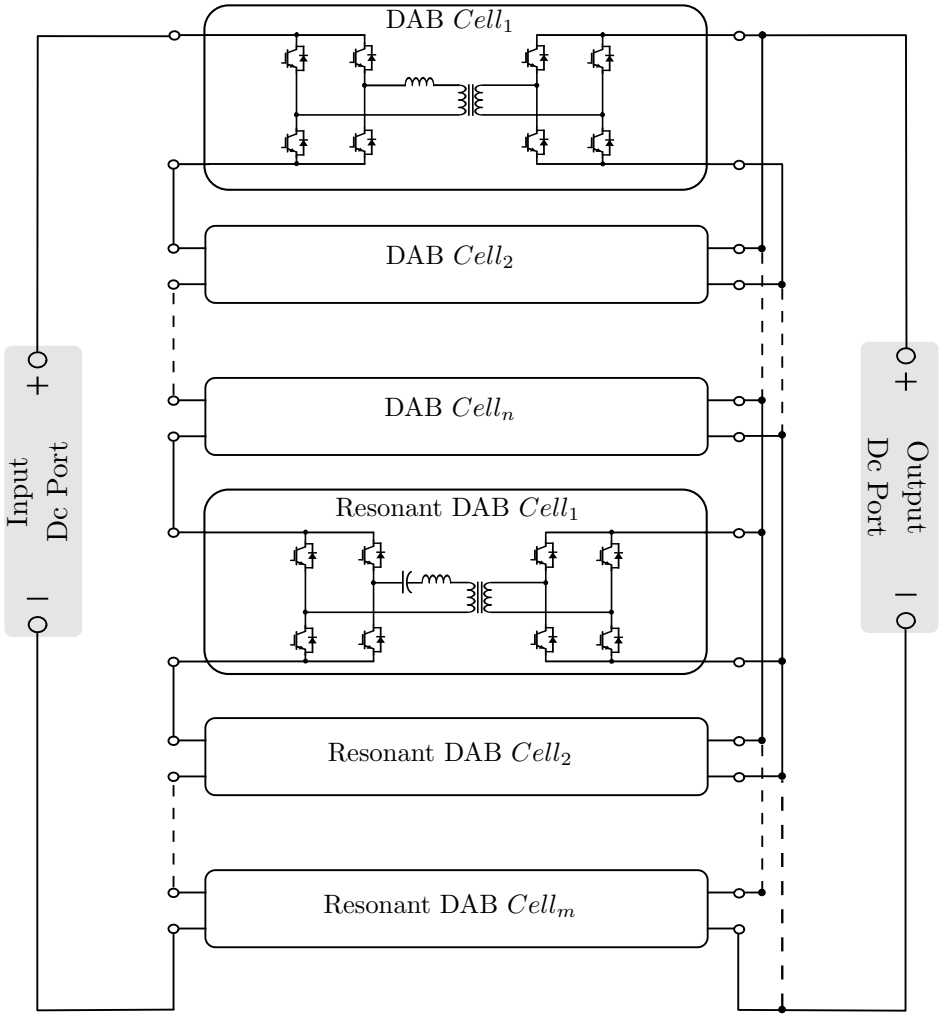


Figure 2.13: *Hybrid Multi-DAB converter*

the voltage and power regulating capability of the traditional DABs. Thus, the required number for each type of DAB can be optimised to fulfill the voltage and power regulating demand of the application, and to maximise the converter efficiency [101].

2.2.3 Direct dc-dc

The direct dc-dc topologies are defined by a single-stage conversion, avoiding an intermediate ac stage. This family can be divided into three subcategories:

1. Buck-Boost structures.

2. Autotransformer structures.

3. Energy accumulators.

A good overview of the the direct dc-dc family is presented in [184].

Buck-Boost structures

The buck-boost configuration is one of the most common structures used to build a direct dc-dc converter [105–119]. The buck-boost leg is constructed of two stacks of low voltage cells as is shown in Fig. 2.14 (a). The cells are commonly formed using half-bridges (Fig. 2.14 (b)) or full-bridges (Fig. 2.14 (c)). However, other topologies have also been considered in the literature [185]. This arrangement requires filters to eliminate the ac component of the output current, which can be implemented using a passive filter. The operating principle of the buck-boost structure is to generate overlapped ac and dc current loops; the dc component is used to transfer power between dc ports, whilst the ac loop maintains the energy balance among the cell stacks. To generate these current loops, the upper and lower stacks impose sinusoidal voltage waveforms with different ac and dc components [105]. Thus, through the control of the stack voltages, it is possible achieve bidirectional power flow between dc ports, whilst maintaining the voltage balance in the capacitors of the stacks.

The buck-boost single leg converter [105–107] can be modified to operate with a resonant tank [108, 109, 149] or with multiple legs if more buck-boost structures are connected in parallel [110–119]. This multi-leg configuration is also called DC-MMC converter. The DC-MMC generates more current loops due to the extra legs (Fig. 2.15) (a)), adding flexibility to the control. Thus, the added ac current loop allows the removal of the input dc port filter. The parallel connection of the output enables the uses of various filter configurations, which can be implemented using passive filters (Fig. 2.15) (b))[110–114] or coupled inductors (Fig. 2.15) (c)) [115–117].

Some modifications of the DC-MMC have been proposed to add symmetry and access to a neutral point. In [115, 117], the DC-MMC is extended for a

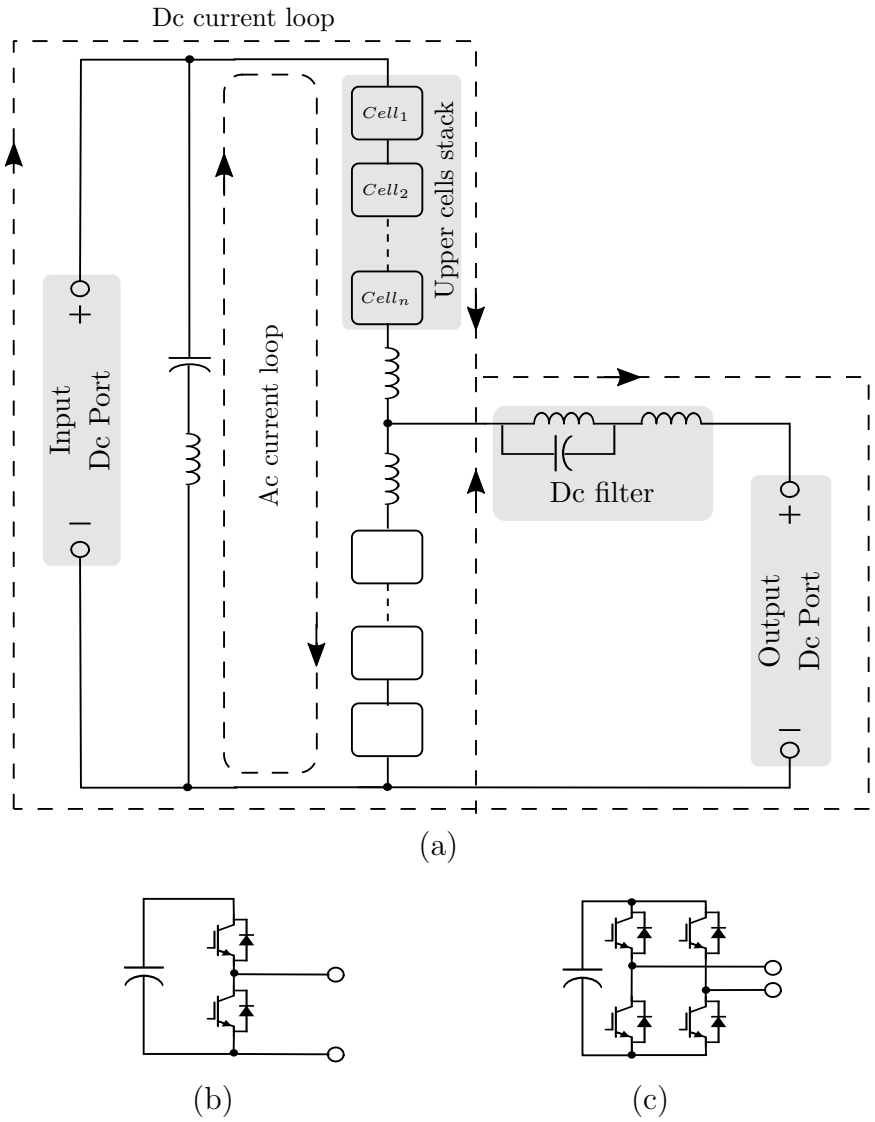


Figure 2.14: *Single-leg Buck-Boost structure :(a) Converter topology (b) Half-Bridge cell , and (c) Full-Bridge cell*

symmetric monopole configuration, as is shown Fig. 2.16 (a). In [121, 122], the output filters are replaced by cell stacks, forming a double star structure (DWye) (Fig. 2.16 (b)). This configuration can also be extended to a symmetrical structure [140–142]. Finally, a double Π structure [120] is proposed to build the direct dc-dc converter (Fig. 2.16 (c)).

Owing to their modular structure, the buck-boost family have the advantages of high reliability and flexibility. In fact, the converter voltage rating can be easily expanded by increasing the number of cells per stack. However, these topologies are only suitable for applications that do not require galvanic

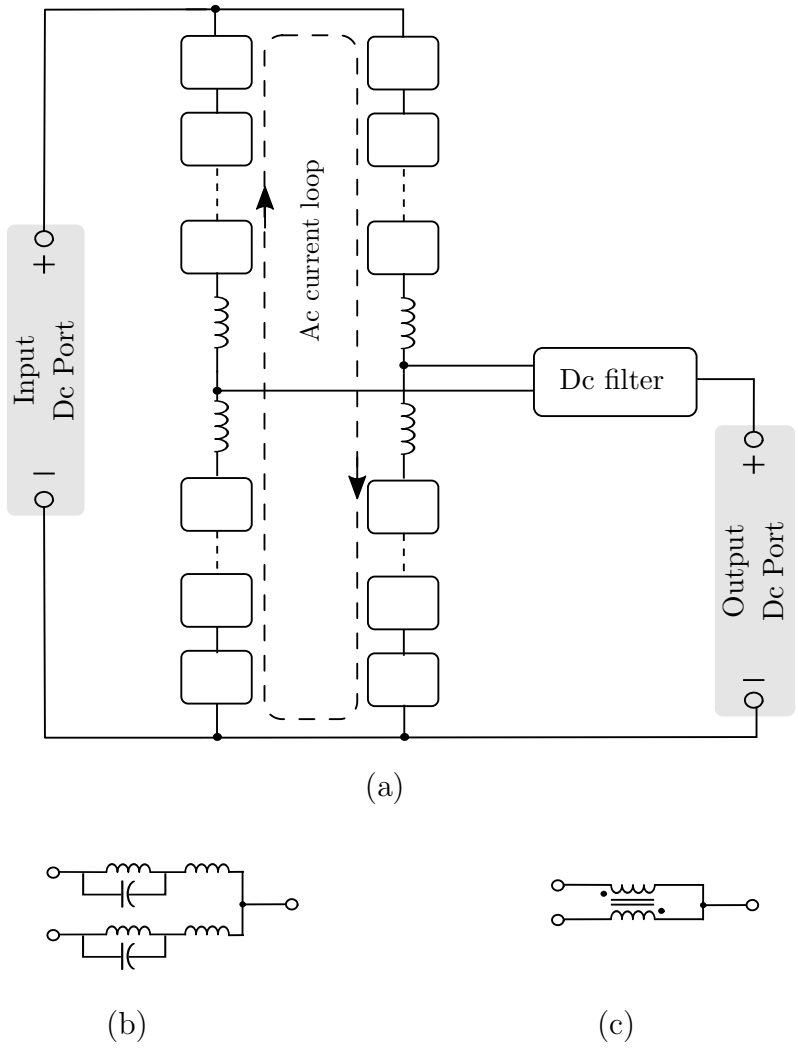
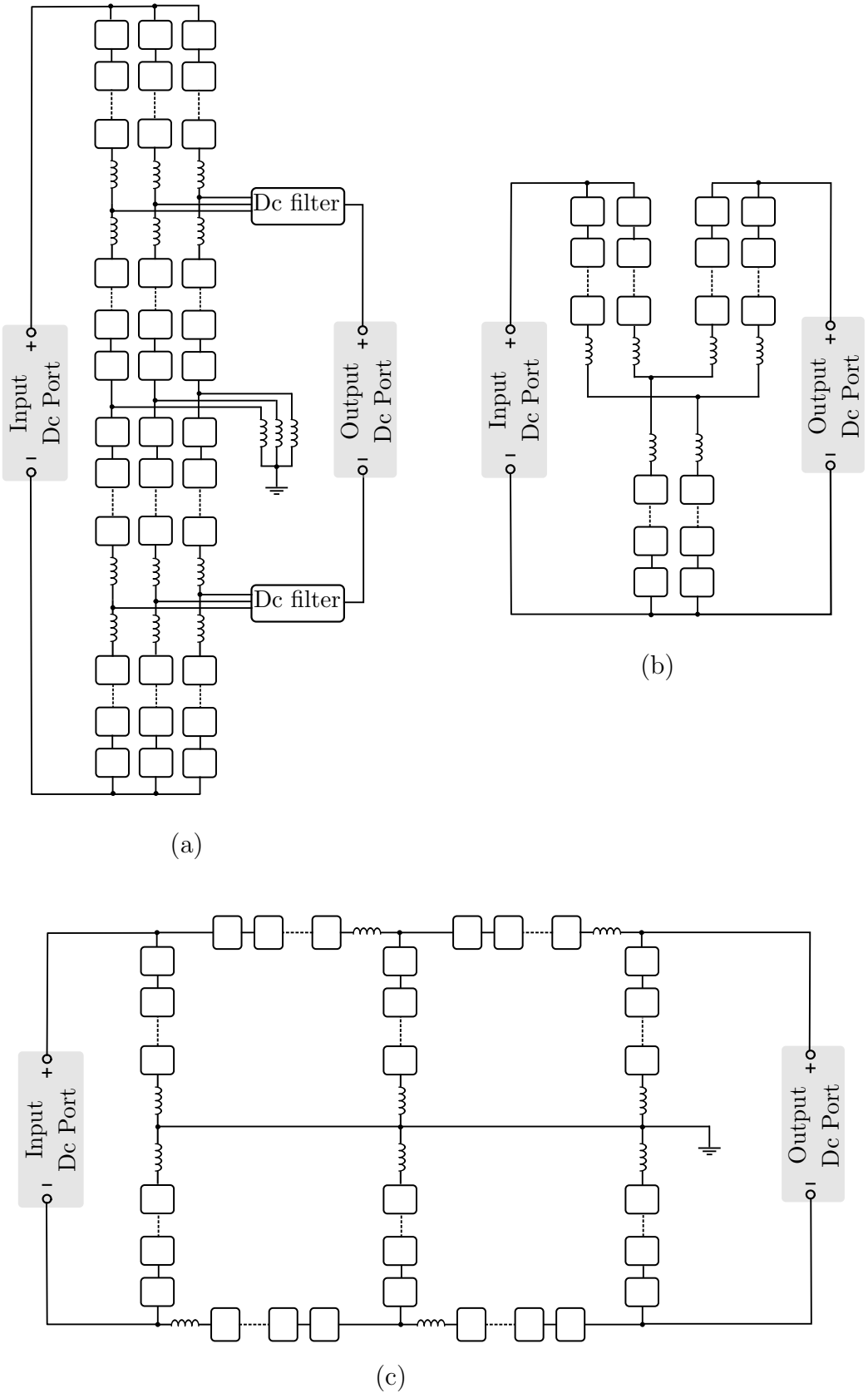


Figure 2.15: *Buck-Boost interleaved structure :(a) DC-MMC using two legs (b) Dc filter: passive solution, and (c) Dc filter: coupled inductors*

isolation due to their transformerless structure. Other drawbacks are the need for large output filters, when they are needed, and high circulating currents. This circulating currents are the main factor that limit the efficient operation in systems needing low voltage step ratios [184]. The DC-MMC has interested ABB for its potential commercial application [186].

Autotransformer structure

The DC-Auto is another of the most studied direct dc-dc topologies [129–135]. Their structure can be seen as the series connection of two MMCs by their



(a)

(b)

(c)

Figure 2.16: *DC-MMC derivations :(a) DC-MMC symmetrical monopole configuration (b) Double Wye structure, and (c) Double* Π *structure*

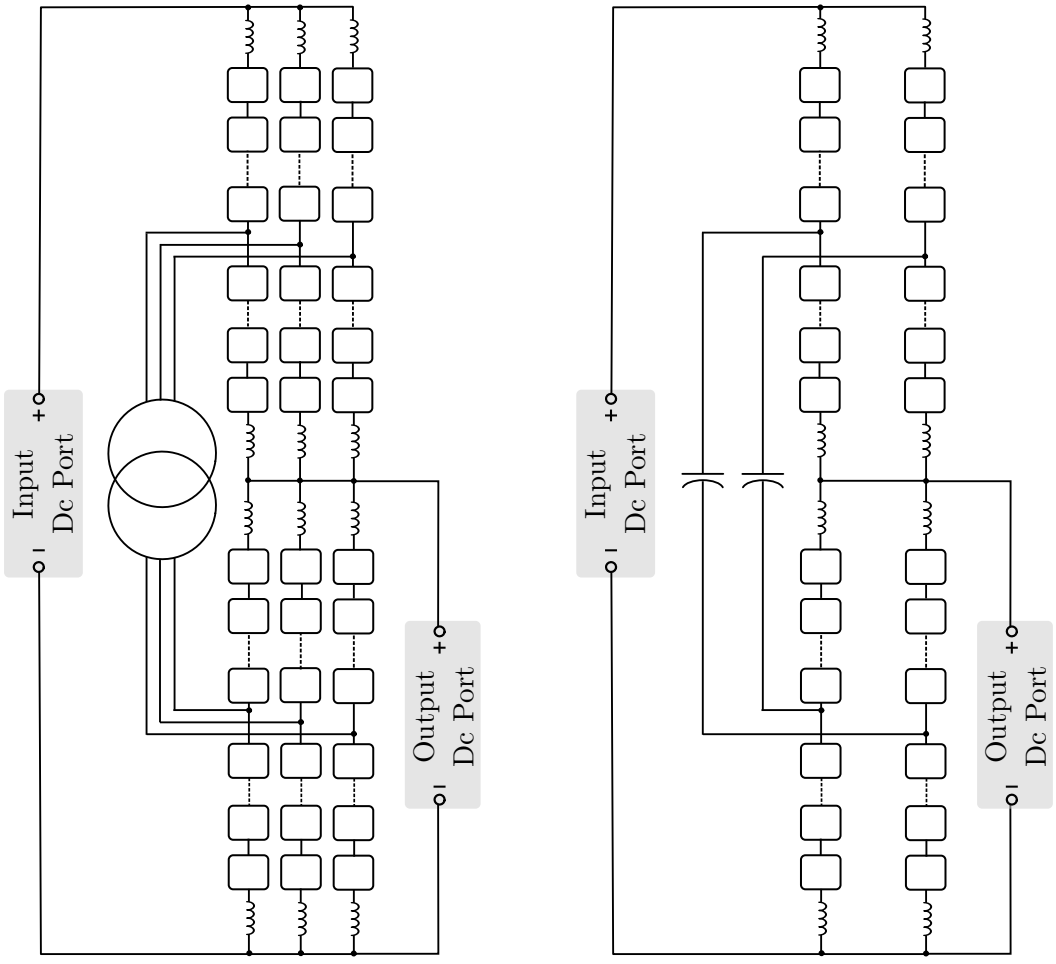


Figure 2.17: *Autotransformers structures: (a) 3-Legs DC-Auto, (b) 2-Legs DC-Auto with capacitors for ac coupling.*

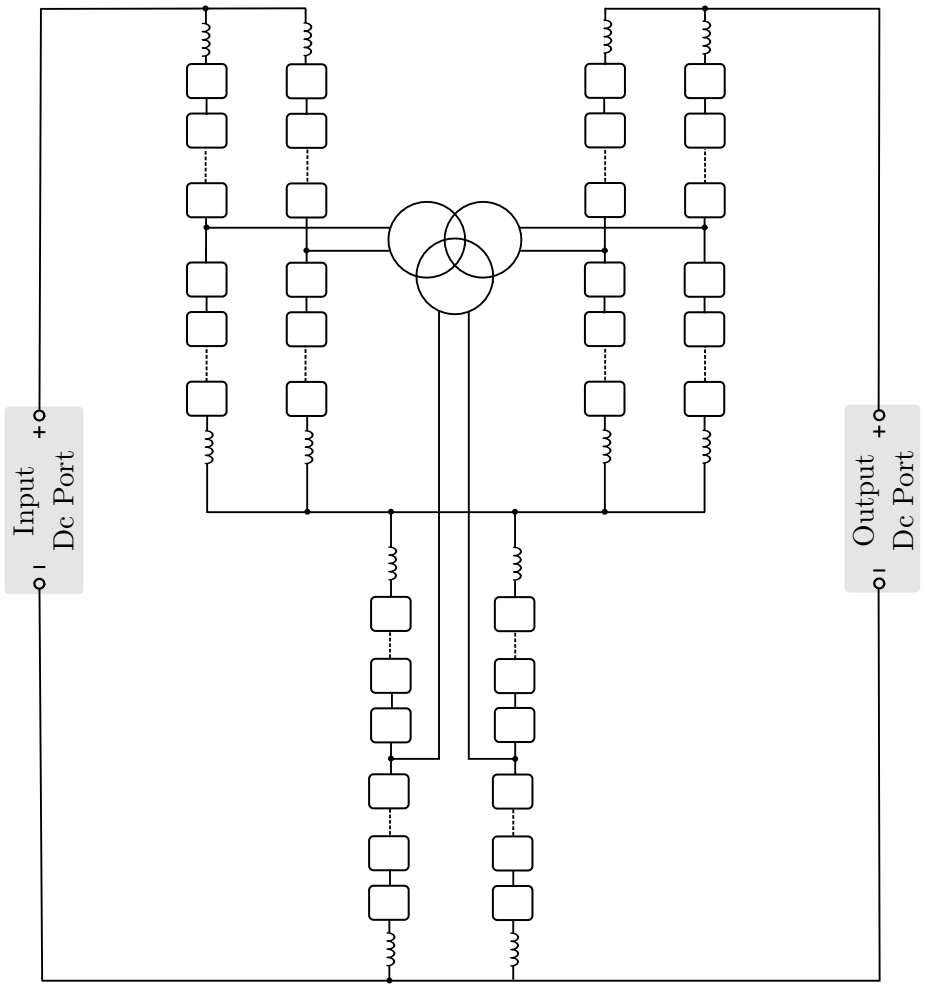


Figure 2.18: *Double Wye structure with transformer*

dc ports, and linked through an ac transformer (Fig. 2.17 (a)). Thus, only a fraction of the power flows through the ac link, allowing a better utilisation of the cells in comparison with the F2F-MMC. An extensive analysis of the capital cost and efficiency of both topologies is presented in [131, 135].

Derivations of this structure have been analysed in the literature. In [136, 137], the transformer is replaced with capacitors (Fig. 2.17 (b)) for an even greater cost and weight reduction, and in [123–125], the auto-transformer concept is applied to the DWye converter to share the ac power flow among the stacks (Fig. 2.18).

The DC-Auto presents the same advantages that the DC-MMC in terms of high reliability and flexibility. Furthermore, the DC-Auto has a higher efficiency and a smaller passive component size in most scenarios, since both MMCs

can be designed to work with an optimal modulation index [135]. However, like the DC-MMC, the high efficiency operation begins to diminish for high voltage step ratios [184]. Thus, this topology is more suitable for low voltage step ratio. Also, regardless the use of a transformer, this family does not provide galvanic isolation due to the transformer only process a portion of the power. For an industrial application, the DC-Auto has attracted the interest of Siemens [187].

Energy accumulators

Energy accumulators are proposed as the final subcategory of direct dc-dc converters for the medium and high voltage range. Energy accumulators are based on the succession of a state of charge and discharge of energy storage elements. The T structure and multi-stage resonant converters are examples of this concept.

The T structure is shown in Fig. 2.19 (a). It is built of one or multiple cell stacks used as energy storage elements, and two series switches for each cell stack [128, 138, 139]. Also, the cells are composed by half-bridges (Fig. 2.19 (b)) or full-bridges (Fig. 2.19 (c)). When one arrangement of series switches at the input dc port is closed, the associated capacitor cell stack begins charging. The discharging stage begins when the corresponding series switches at the output port are switched on. Thus, the series switches control the charge and discharge state of the cell stack, whilst the number of inserted cells in each state is adapted to the input and output dc voltage levels. Therefore, the transition between charge and discharge states requires a dead time in the series switches to accommodate the differing number of cells inserted.

The advantages of these converters are their flexibility, scalability, and high voltage ratio capability. However, the large energy rating of energy storage elements limits their operation to low power applications. Also, the problems of series connection of semiconductor devices needs to be addressed.

The multi-stage resonant converter is another example of an energy accumu-

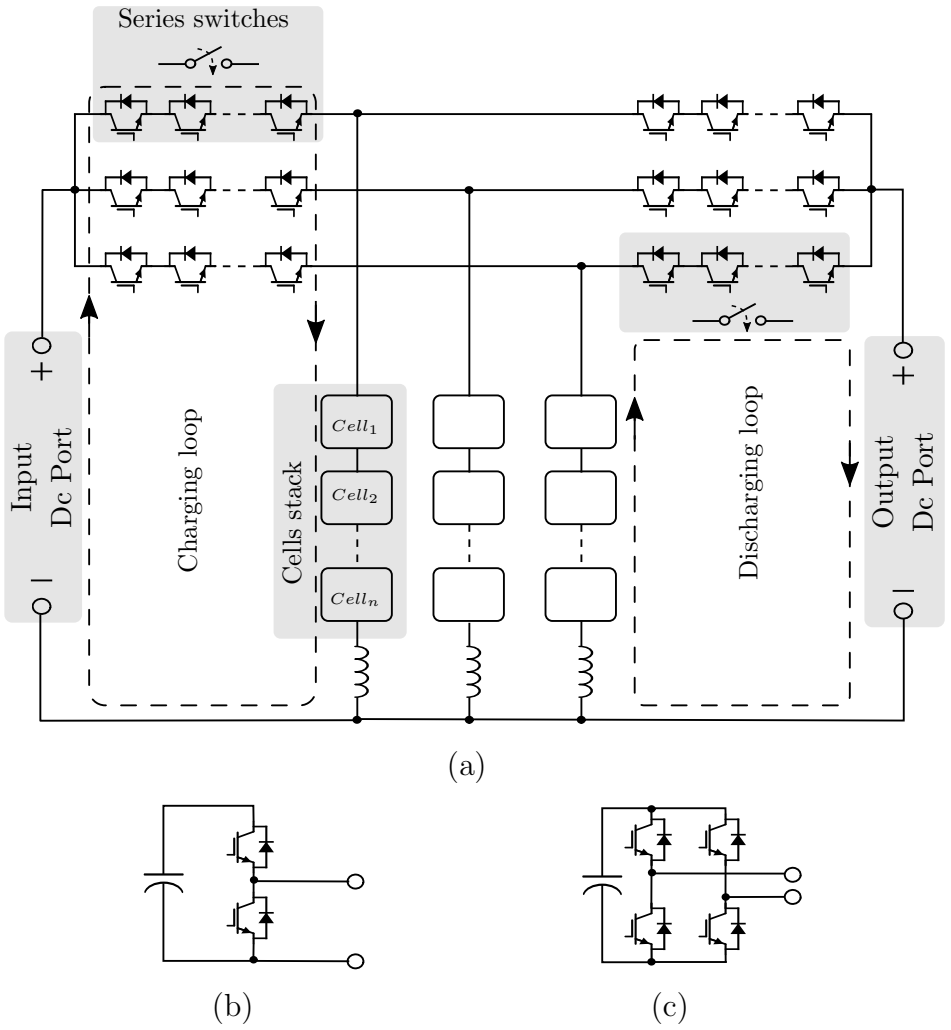


Figure 2.19: *Energy accumulator using 3-leg T structure: (a) Topology, (b) Half-brige cell, (c) Full-bridge cell.*

lator structure. It is constructed of an interconnection of multiple resonant stages as is in shown Fig. 2.20. The operation of these converters are based on repeated charging and discharging process of distributed capacitors through a resonant circuit [143–146]. In the boost mode, the capacitors are charged in parallel when the switches S_c are turned on, and then discharged in series into the high voltage dc bus when the switches S_d are closed. For the buck mode, the inverse action takes place. Different cell topologies have been proposed to exploit the same concept [147, 148].

The multiple-stage resonant converters also present modularity and flexibility. They can provide a high voltage step ratio with lower electrical stress on the resonant components in comparison with the single-stage resonant circuits.

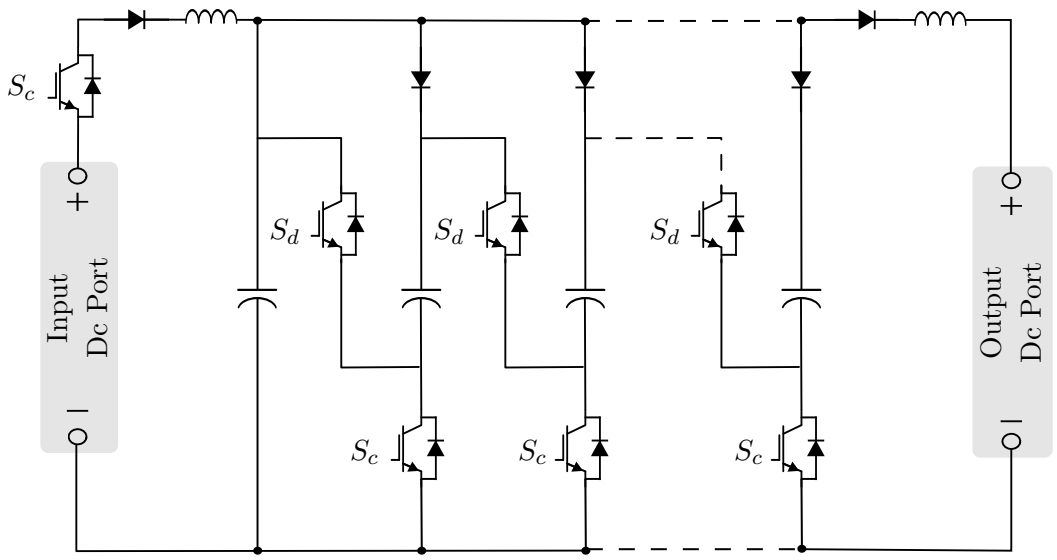


Figure 2.20: *Energy accumulator using 3-leg T structure: (a) Topology, (b) Half-brige cell, (c) Full-bridge cell.*

Furthermore, the resonant operation allows soft-switching in the semiconductor devices. The disadvantages of these proposals are the unbalanced current distribution among the cells, and the demand of bidirectional switches for reversal power flow.

2.2.4 Potential applications

In this subsection, a comparison of the previous topologies is presented. For all the topologies, the features considered are the suitable input/output voltage range, transformation ratio, bidirectional power flow capability, galvanic isolation, dc fault blocking and modularity. Furthermore, the possible applications in dc grids are identified for each topology considering these features.

The main features of the proposed classification topologies and the potential application are summarised in Table 2.1. The possible applications of dc-dc converters in dc grids can be classified in: (a) HVdc grid interconnection, (b) Dc collectors, (c) Dc feeders, and (d) High step ratio link. The first application is needed for the configuration of a meshed HVdc grid. A meshed HVdc grid is formed by the interconnection of different HVdc grids, which generally have different types of grounding and voltage level. Therefore, an intermediate dc-

dc converter would be necessary for their interconnection. This application requires a low transformation ratio, bidirectional power flow capability and galvanic isolation is desirable. Since a possible failure will have an important impact on the electrical grid, the fault blocking capability and a high reliability for the converter are critical. Thus, the modularity is a recommended feature to increase the reliability of the converter. The Dc collectors are the second possible application. They are used to interconnect a high/medium voltage dc bus with several dc sources such as solar photovoltaic arrays and offshore windfarms. This application requires a medium transformation ratio to elevate the voltage of the sources to the dc bus voltage, unidirectional operation and galvanic isolation is highly recommended for safety reasons. The fault blocking capability and a high reliability in the converter are desirable, but less critical than the HVdc grid interconnection case. Dc feeders are another possible application. These are required to interconnect a medium voltage dc bus to dc loads such as EV chargers, data centres, or BESS. This application requires a medium transformation ratio to elevate the voltage of the loads to the dc bus voltage and usually a bidirectional capability is necessary because of the nature of the loads. Commonly, galvanic isolation is required as standard for this application. A modular structure is also highly desirable to provide easy scaling if more loads are needed in the future. Finally, the high step ratio link is the last possible application. They are used to interconnect dc grids of different voltage ratings, as are required for HVdc tapping or for the link of MV dc grids with LV dc grids. This application requires high transformation ratio to adapt the voltages of the two dc grids and the bidirectional operation is also desirable due to the massification of energy sources at low and medium voltage. Galvanic isolation is needed to protect the low voltage grid, but it can be added in an additional stage.

Table 2.1: Main features of dc-dc topologies

Topology structure	Features							Application
	Input Voltage	Output Voltage	Transf. Ratio	Bidirectionally	Galvanic Isolation	Fault Blocking	Modularity	
Two level DAB	MV/LV	MV/LV	Medium	Yes	Yes	Yes	No	Dc collector/feeder
Symmetrical dc-ac-dc MMC	HV/MV	HV/MV	Medium	Yes	Yes	Yes	High	HVdc grid inter. Dc collector/feeder
Asymmetrical dc-ac-dc MMC	HV/MV	MV/LV	High	Yes	Yes	Yes	High	High step ratio link
Multi DAB	MV/LV	MV/LV	High	Yes	Yes	Yes	High	High step ratio link Dc collector/feeder
Buck-boost direct dc-dc	HV/MV	HV/MV	Low	Yes	No	Yes	High	HVdc grid inter.
Autotransformer MMC	HV/MV	HV/MV	Low	Yes	No	Yes	High	HVdc grid inter.
Energy accumulators	HV/MV	MV/LV	Medium	No	No	Yes	Medium	High step ratio link Dc collector

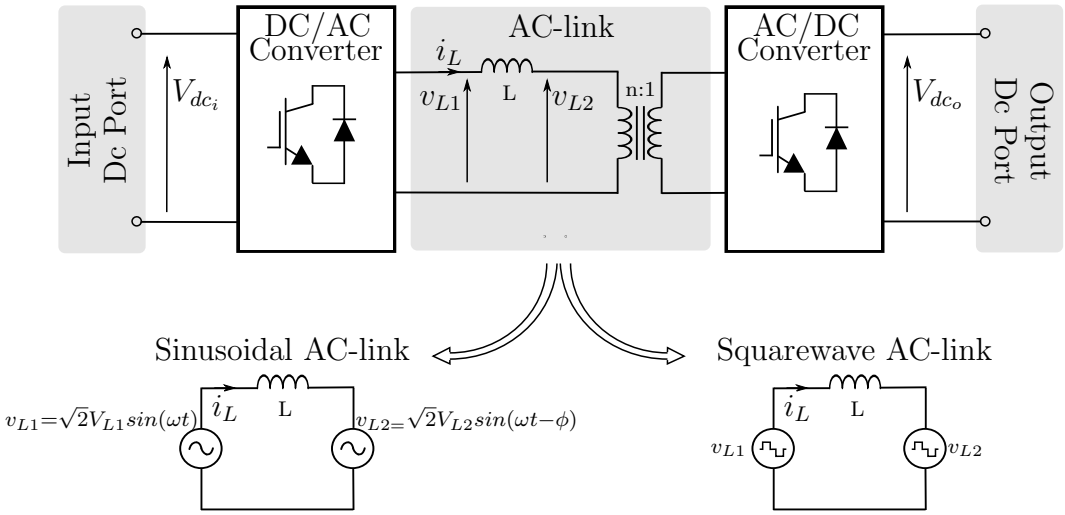


Figure 2.21: *General structure of Dc-Dc Converter with AC-link*

2.3 Ac-link power control strategies

The control strategies used in the different topologies vary according to their structure and application. Since most of the previously presented topologies are formed of ac links in both their centralised and distributed versions, the ac-link power control is the core element of the control scheme. The most utilised ac-link type is formed by an inductor and/or a transformer, therefore, this subsection will analyse the main power flow control strategies for this type of ac-link available in the literature [181, 188].

An ac-link formed by an inductor and a transformer is illustrated in Fig. 2.21. Since the voltages at input V_{dc_i} and output V_{dc_o} port remain stable in steady state, the power flow can be controlled by adjusting the magnitude and direction of the inductor current i_L. For the case of sinusoidal voltages at ac-link, the classical model of power transmission in ac power systems can be applied [189]. Therefore, it is possible express the apparent power S as in (2.1), considering V_{L1} and V_{L2} as the rms values of the voltages at the ac-link v_{L1} and v_{L2} respectively, ω the frequency of these voltages and L the inductance of the ac-link inductor.

$$S = \frac{V_{L1} \cdot V_{L2}}{\omega L} sin(\phi) + j\left(\frac{V_{L1} \cdot V_{L2}}{\omega L} cos(\phi) - \frac{V_{L2}^2}{\omega L}\right). \tag{2.1}$$

Thus, the power flow can be controlled by the phase-shift ϕ between the ac link voltages. This model can directly be applied when the dc/ac converters can generate good approximations of sinusoidal voltages, as is the case of the symmetric modular multilevel dc-ac-dc converters.

The same phase-shift principle can be used for the case of dc/ac converter topologies that generate a low number of voltage levels at the ac-link, such as standard DAB topologies. The usage of PWM methods to modulate the ac voltages with low level voltages could be an alternative, however, this limits the operation to ac voltages with low fundamental frequency at the ac-link. Therefore, square-wave voltages operation is the most common for medium and high frequency ac-link. In this case, both converters generate high frequency square-waves in the v_{L1} and v_{L2} voltages, which are phase-shifted in order to control the power flow. The most important power control schemes using square-waveforms are: (a) Single-phase-shift control (SPS), (b) Extended-phase-shift control (EPS), (c) Dual-phase-shift (DPS), (e) Triple-phase-shift (TPS) and (f) Triangular/Trapezoidal current mode (TCM).

2.3.1 Single phase-shift control (SPS)

The most widely used control method using square-waveform is the SPS control [190–194]. The typical waveforms of this modulation scheme are shown in Fig. 2.22 (a). In this scheme, each converter is modulated in order to generate the v_{L1} and v_{L2} voltages with a two-level waveform and 50% fixed duty-cycle, and amplitudes V_{L1} and V_{L2} respectively. If H-bridges are used as the AC/DC and DC/AC converters, these voltage amplitudes are directly related with the Dc port voltages ($V_{L1} = V_{dc_i}$ and $V_{L2} = n \cdot V_{dc_o}$), but other converter topologies can be incorporated if this relation is known. Thus, the i_L current through the inductor L can be modelled as a part-function with four different zones, allowing the power to be expressed as (2.2). Therefore, the power flow direction and magnitude can be straightforwardly controlled though the phase-shift ϕ

between v_{L1} and v_{L2}.

$$P_{SPS} = \frac{1}{2\pi} \int_0^{2\pi} v_{L1} \cdot i_L \, d\omega t = \frac{V_{L1} \cdot V_{L2}}{\pi \omega L} \phi(\pi - \phi) \tag{2.2}$$

The advantages of SPS control is its simplicity and fast dynamic response [181]. However, the main issue of this strategy is the reduced efficiency due to the restricted soft-switching zone and the high circulating current requirements [188].

2.3.2 Extended phase-shift control (EPS)

In order to reduce the drawbacks of the SPS control, the EPS method has been proposed [195–199]. The EPS control can improve the traditional SPS behavior due to the incorporation an additional control variable, which is added if one converter changes it's modulation to generate a three-level voltage waveform, whilst the other one keeps the two-level waveform and 50% fixed duty-cycle (Fig. 2.22 (b)). Because the addition of the zero voltage state, the backflow power is null during this zero voltage state interval, decreasing the circulating current and current stress [197].

The power flow direction and magnitude can be straightforwardly controlled using (2.3), through the control of the phase-shift ϕ and the length of the zero voltage state δ.

$$P_{EPS} = \frac{V_{L1} \cdot V_{L2}}{\pi \omega L} \left((\phi - \delta)(\pi - \phi + \delta) + \frac{1}{2}\delta(\pi - 2\phi + \delta) \right) \tag{2.3}$$

Therefore, the EPS control enhances regulating power control range and flexibility due to the incorporation of the additional control variable δ. Also, the reduction of the reactive power reduces the conduction losses and consequently, it improves the efficiency of the converter. However, the main drawback of the EPS scheme is their need of use different modulation schemes for each converter, which generates an uneven operation between the converters

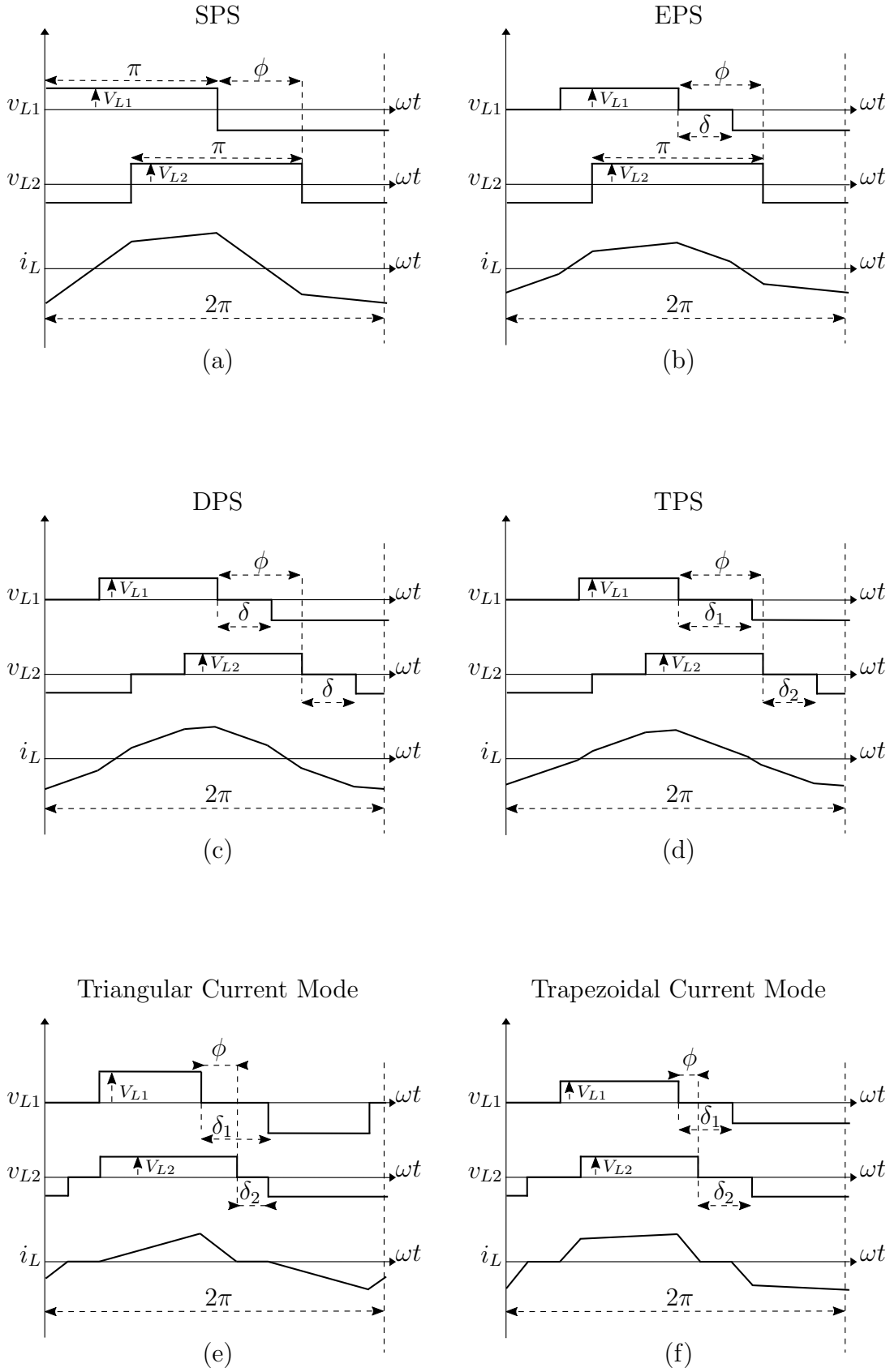


Figure 2.22: *Ac link power control strategies: (a) Single phase-shift control (SPS), (b) Extended phase-shift control (EPS), (c) Dual-phase-shift control (DPS), (d) Triple Phase-Shift control (TPS), (e) Triangular Current Mode and (f) Trapezoidal Current Mode*

and requires the exchange of the modulation strategy between them for their bidirectional operation [199].

2.3.3 Dual phase-shift control (DPS)

In order to standardise the modulation of both converters, the dual-phase-shift control (DPS) has been proposed [193, 200–205]. The DPS scheme generate two three-level voltage waveform at both sides of the ac-link inductor. In this case, both converters share a common time window for the zero voltage state δ, which together with the phase-shift ϕ, controls the tracking of power flow demand (2.4). The general waveforms of the DPS control are shown in Fig. 2.22 (c).

$$P_{_{DPS}} = \begin{cases} \dfrac{V_{L1} \cdot V_{L2}}{\pi \omega L} \left(\phi(\pi - \phi) - \dfrac{1}{2}\delta^2 \right) & 0 \leq \delta \leq \phi \leq \pi \\ \\ \dfrac{V_{L1} \cdot V_{L2}}{\pi \omega L} \phi \left(\pi - \delta - \dfrac{1}{2}\phi \right) & 0 \leq \phi \leq \delta \leq \pi \end{cases} \tag{2.4}$$

The DPS control keeps the advantages of the EPS scheme in terms of reduced circulating current and current stress, improved efficiency and, a wider range and flexibility for the power control [181].

2.3.4 Triple Phase-Shift control (TPS)

The triple-phase-shift control (TPS) is the latest square voltage waveform scheme based in phase-shift [206–213], and it can be seen as the generalisation of the DPS scheme for the case of unequal zero voltage time at both converters. Thus, it adds and extra degree of freedom, δ_2, in the modulation scheme, as is shown in Fig. 2.22 (d). This general approach can be used to implement all of the previously described approaches, i.e. SPS, EPS and DPS control. The DPS operation can be derived if the restriction $\delta_1 = \delta_2$ is imposed; the EPS scheme if $\delta_2 = 0$ and finally the SPS control if $\delta_1 = \delta_2 = 0$.

The addition of the extra degree of freedom enables the definition of an optimization problem to find the best solution from all feasible solutions, with the objective of minimise the conduction losses [207, 208, 211], minimise the current stress [210, 212], maximise the power range [206], or others multi-objective goals [213]. Thus, the TPS presents different implementations depending on the objective pursued, making the TPS the most flexible scheme of the phase-shifted control family.

2.3.5 Triangular/Trapezoidal Current Mode (TCM)

One case of the TPS, aimed to extend the soft-switching range, is the triangular/trapezoidal current mode (TCM) [49–51]. This approach uses one or two degrees of freedom of the general TPS control to obtain several zero-current transitions (ZCS) at both converters. Thus, the current at the ac-link draw a triangular or trapezoidal waveform, as is shown in Fig. 2.22 (e)-(f). The ZCS conditions can be deducted as

$$\frac{\pi - \delta_2}{\pi - \delta_1} = \frac{V_{L1}}{V_{L2}} \tag{2.5}$$

and, also the relation (2.6) is achieved for the triangular current case.

$$\phi + \delta_2 = \delta_1 \tag{2.6}$$

Therefore, this allows the expression of power transfer through (2.7), reducing the TPS optimization problem to a single control variable, whilst achieving ZCS in all power range.

$$P_{_{Tri}} = \begin{cases} \dfrac{2V_{L1} \cdot V_{L2}^2}{\pi\omega L(V_{L1} - V_{L2})}\phi^2 & V_{L2} < V_{L1} \\ \\ \dfrac{2V_{L1}^2 \cdot V_{L2}}{\pi\omega L(V_{L2} - V_{L1})}\phi^2 & V_{L1} < V_{L2} \end{cases} \tag{2.7}$$

For the trapezoidal current mode, the condition (2.6) is released losing two transitions at ZCS, but increasing the power range in comparison with the triangular case. The advantages of the TCM scheme are the simplification of the power expression and the absence of an optimisation problem to solve. Therefore, the implementation complexity of the TPS control scheme is significantly reduced, whilst keeping a high efficiency over the full power range, due to the ZCS operation. Also, TCM can effectively limit the peak current present in the converter [51]. Finally, the triangular current mode is suitable where the difference between V_{L1} and V_{L2} is considerable, while the trapezoidal can be applied when that difference is low. Thus, both schemes are complementary for an operation with wide voltage range in the dc ports.

Chapter 3

High step ratio dc-dc MMC

3.1 Introduction

In this Chapter an extensive model for the High step ratio dc-dc MMC is presented. The MMC modulation proposal is presented based on the previous research works that propose the use of MMC for high step ratio. Also, the application of the TCM scheme for the ac-link of this asymmetrical structure is detailed in their triangular and trapezoidal versions. For the second alternative, an optimisation problem is defined considering the objective to minimise the current stress in the semiconductor devices. Also, the conditions to achieve ZCS and MMC capacitor voltage balance are analysed for both cases.
Thus, it is possible find a simple model for the converter that yields ZCS in the devices for a wide voltage range, avoiding the resonant operation of the previous high step ratio MMC research works.

3.2 Topology and lossless model

The topology of the high step ratio dc-dc MMC is shown in Fig. 3.1, which was classified previously in terms of its structure as a monopole asymmetrical MMC-full-bridge. It is formed by a stack of N half-bridge cells which support the high-voltage port V_{HV}, while an active full-bridge converter connects the

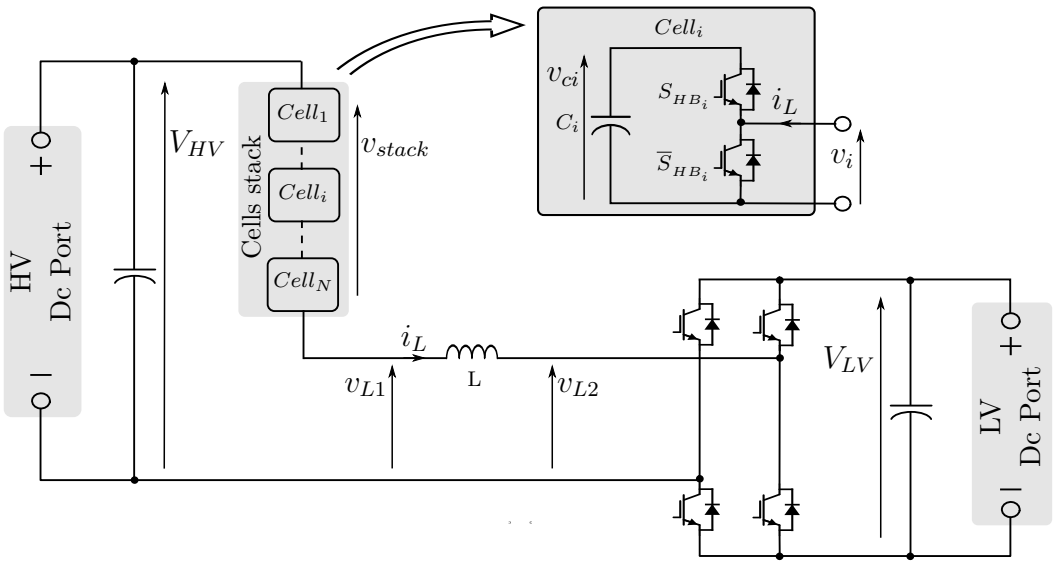


Figure 3.1: *High step ratio dc-dc MMC topology*

low-voltage port V_{LV}. Both subsystems are connected through an inductor L generating an ac low-voltage link, which is designed for high or medium-frequency operation to reduce the size and weight of the passive components. Furthermore, filters are placed at both sides of the converter to decrease voltage and currents ripple, but these are not considered in the following work since they have no impact on the modulation analysis.

The lossless dynamic equations that describe the general operation of the converter can be found as follows. The current through the inductor can be expressed in terms of the voltages at both sides v_{L1} and v_{L2} following (3.1).

$$L\frac{di_L}{dt} = v_{L1} - v_{L2} \tag{3.1}$$

Since the voltage v_{L1} is the difference between the high-voltage V_{HV} and the total voltage in the stack v_{stack}, this voltage v_{stack} defines the voltage v_{L1} through (3.2). Also, it is noticeable that the voltage v_{stack} is given by the sum of the half-bridges output voltages v_i, therefore, v_{stack} is dependent directly on the switching states of each cell $S_{HB_i} \in \{1, 0\}$ and its capacitor voltage v_{ci}, as is described in (3.3).

$$v_{L1} = V_{HV} - v_{stack} \tag{3.2}$$

$$v_{stack} = \sum_{i=1}^{N} v_i = \sum_{i=1}^{N} v_{ci} \cdot S_{HB_i} \tag{3.3}$$

On the other hand, the voltage v_{L2} is determined by the full-bridge commutation state $S_{FB} \in \{1, 0, -1\}$ and the dc voltage V_{LV} at the low voltage dc port following (3.4).

$$v_{L2} = V_{LV} \cdot S_{FB} \tag{3.4}$$

Therefore, the dynamic equation for the inductor current i_L resulting from the substitution of (3.2),(3.3) and (3.4) in (3.1), and the dynamic equation for the voltages in the cell capacitors are summarised in (3.5).

$$\begin{aligned} L\frac{di_L}{dt} &= V_{HV} - \sum_{i=1}^{N} v_{ci} \cdot S_{HB_i} - V_{LV} \cdot S_{FB} \\ C_i\frac{dv_{ci}}{dt} &= i_L S_{HB_i} \end{aligned} \tag{3.5}$$

If it is assumed that all cells have equal capacitance C, that their capacitor voltages are controlled to the desired value v_c^* and neglecting internal losses, the relationship between the capacitor voltages and the total stack power P_{stack} is:

$$C\frac{d}{dt}\sum_{i=1}^{N} v_{ci} \approx \frac{P_{stack}}{v_c^*}. \tag{3.6}$$

3.3 Three-level Cells stack operation

As was discussed in the previous Chapter, the trapezoidal/triangular control mode needs a coordinated three-level voltage at both terminals of the ac-link inductor. Therefore, the application of this control scheme to this topology requires special attention in the generation of the voltages v_{stack} and v_{L2}. The full-bridge can straightforwardly generates three-levels in v_{L2} by using unipolar modulation, but the cell stack requires a special operation to get a three-level

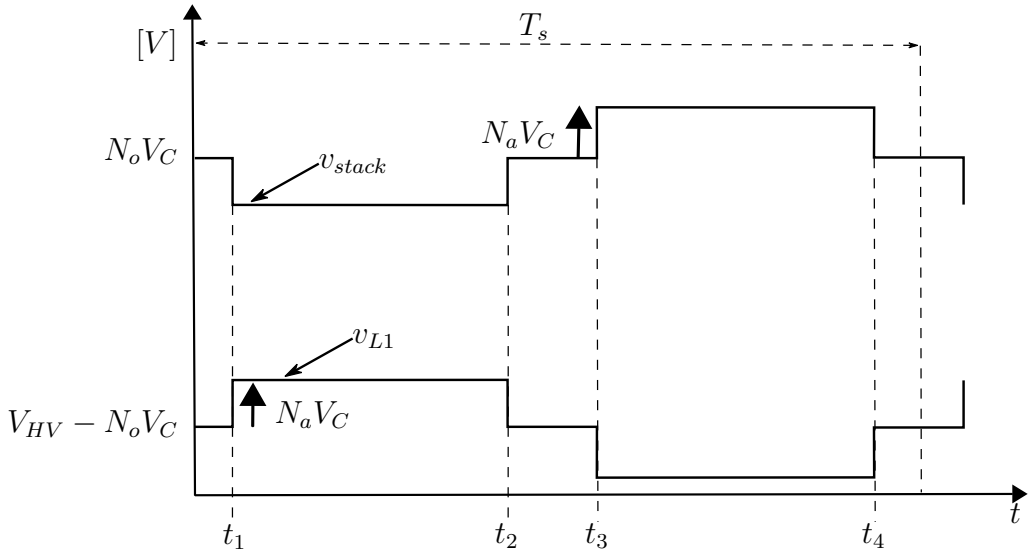


Figure 3.2: *General three-level square-waveform stack operation*

square-waveform in v_{L1}. This subsection presents the conditions in order to achieve this.

From (3.2), it is clear that v_{stack} must be a three-level voltage in order to generate a three-level voltage in v_{L1}. A general expression of a three-level voltage for v_{stack} is shown in (3.7), considering that the stack operation is centered on N_o cells, the voltage amplitude is generated by N_a cells and all the capacitor voltages in the cells are balanced and equal to V_C. Also, the v_{stack} commutation times (t_1, t_2, t_3, t_4) in one cycle T_s are considered as is shown in Fig, 3.2.

$$v_{stack}(t) = \begin{cases} (N_o - N_a)V_C & \text{if } t \in [t_1, t_2] \\ (N_o + N_a)V_C & \text{if } t \in [t_3, t_4] \\ N_o \cdot V_C & Otherwise \end{cases} \tag{3.7}$$

Thus, replacing (3.7) in (3.2), the voltage v_{L1} can be expressed as

$$v_{L1}(t) = \begin{cases} V_{HV} - (N_o - N_a)V_C & \text{if } t \in [t_1, t_2] \\ V_{HV} - (N_o + N_a)V_C & \text{if } t \in [t_3, t_4] \\ V_{HV} - N_o \cdot V_C & \textit{Otherwise} \end{cases} \tag{3.8}$$

Analysing (3.8), the condition to generate a square wave voltage, centered on zero in v_{L1} can easily deduced as (3.9),

$$V_C = \frac{V_{HV}}{N_o} \tag{3.9}$$

Therefore, v_{L1} is a three-level voltage, centered on zero, as shown in (3.10), if (3.9) holds .

$$v_{L1}(t) = \begin{cases} V_{HV}\dfrac{N_a}{N_o} & \text{if } t \in [t_1, t_2] \\ -V_{HV}\dfrac{N_a}{N_o} & \text{if } t \in [t_3, t_4] \\ 0 & \textit{Otherwise} \end{cases} \tag{3.10}$$

Thus, the stack modulation defines the step-down voltage ratio r_S (3.11) between the amplitude of the ac-link voltage $\hat{v}_{L1}$ and the high-voltage V_{HV}, as is shown in (3.2). With this equation, it is possible to adjust the voltage ratio r_s through N_a and N_o in order to enable voltage reconfiguration or redundant operation for the case of failure in any cell.

$$r_S = \frac{\hat{v}_{L1}}{V_{HV}} = \frac{N_a}{N_o} \tag{3.11}$$

The feasible range for N_a and N_o can be found considering two restrictions: i)

the voltage stack can be only positive since half-bridges are used in the cells and ii) the maximum number N of cells available in the stack. These two restrictions define the feasible range for N_a and N_o in (3.12), which can be derived if these restrictions are analysed in (3.7).

$$\begin{aligned} 0 &\leq N_o - N_a \\ N_a + N_o &\leq N. \end{aligned} \tag{3.12}$$

Therefore, the discrete nature of N_a and N_o and their operational range limited by (3.12) defines a finite number of combinations to generate the voltage ratio r_S. The range for r_S can be deduced noticing that the lowest value is achieved with $N_a = 1$ and $N_o = N - 1$, whilst the highest value is achieved with $N_a = N_o$. Thus, the operational limits under these restrictions are shown in (3.13).

$$\frac{1}{N-1} \leq r_S \leq 1 \tag{3.13}$$

The case $N_a = 1$ and $N_o = N - 1$ is the more attractive option for a high step voltage application. This is because this choice generates the biggest difference between the dc high voltage port V_{HV} and the ac-link voltage amplitude $\hat{v}_{L1}$ ($r_s = \frac{1}{N-1}$), whilst yielding the lowest voltage magnitude in the cell. Thus, the voltage blocking requirement of the cells is reduced . Furthermore, the voltage transformation ratio linearly increases as the number of cells in the stack is incremented, making this option attractive for high voltage operation where the number of cells required is naturally high in order to block the high voltage V_{HV} with standard low voltage devices.

The approach given above is not the only one that can generate a three-level voltage for v_{L1}, centered on zero, whilst also meeting the restrictions of (3.12) and there are other possible alternative choices for N_a and N_o. These other alternative selections could be suitable for a flexible control of r_s or for redundant operation. However, for controlling r_s this strategy would provide

Table 3.1: Possible N_a and N_o choices for a stack formed by five half-bridge cells.

Choice	N_a	N_o	V_C	r_S
a	1	4	$\frac{V_{HV}}{4}$	$\frac{1}{4}$
b	1	3	$\frac{V_{HV}}{3}$	$\frac{1}{3}$
c	1	2	$\frac{V_{HV}}{2}$	$\frac{1}{2}$
d	1	1	V_{HV}	1
e	2	3	$\frac{V_{HV}}{3}$	$\frac{2}{3}$
f	2	2	$\frac{V_{HV}}{2}$	1

poor voltage resolution due to the discrete nature of N_a and N_o. Thus, the manipulation of N_a and N_o is more suitable for voltage reconfiguration rather than voltage control [41].

Redundant operation can be configured by leaving one or more cells in stand-by, which can be achieved if $N_a + N_o < N$. In this case the converter has enhanced reliability because it can use any stand-by cell to replace a malfunctioning cell.

It should be noticed that the condition (3.9) must be assured in all cases, therefore, the mean voltage of the cell capacitors must be adjusted if N_o is changed. To exemplify this, for the case of a fixed high voltage V_{HV} and a stack with 5 half-bridges, Table 3.1 and Figure 3.3 show all the possible choices for N_a and N_o, and the corresponding switching patterns.

Since the highest voltage step-down conversion is achieved with the choice a (see Fig. 3.3 (a)), this case is the more attractive operation for a high step voltage application. In this choice, the stack voltage step ratio is $rs = \frac{1}{4}$, reaching the highest voltage transformation for a stack with five cells. The

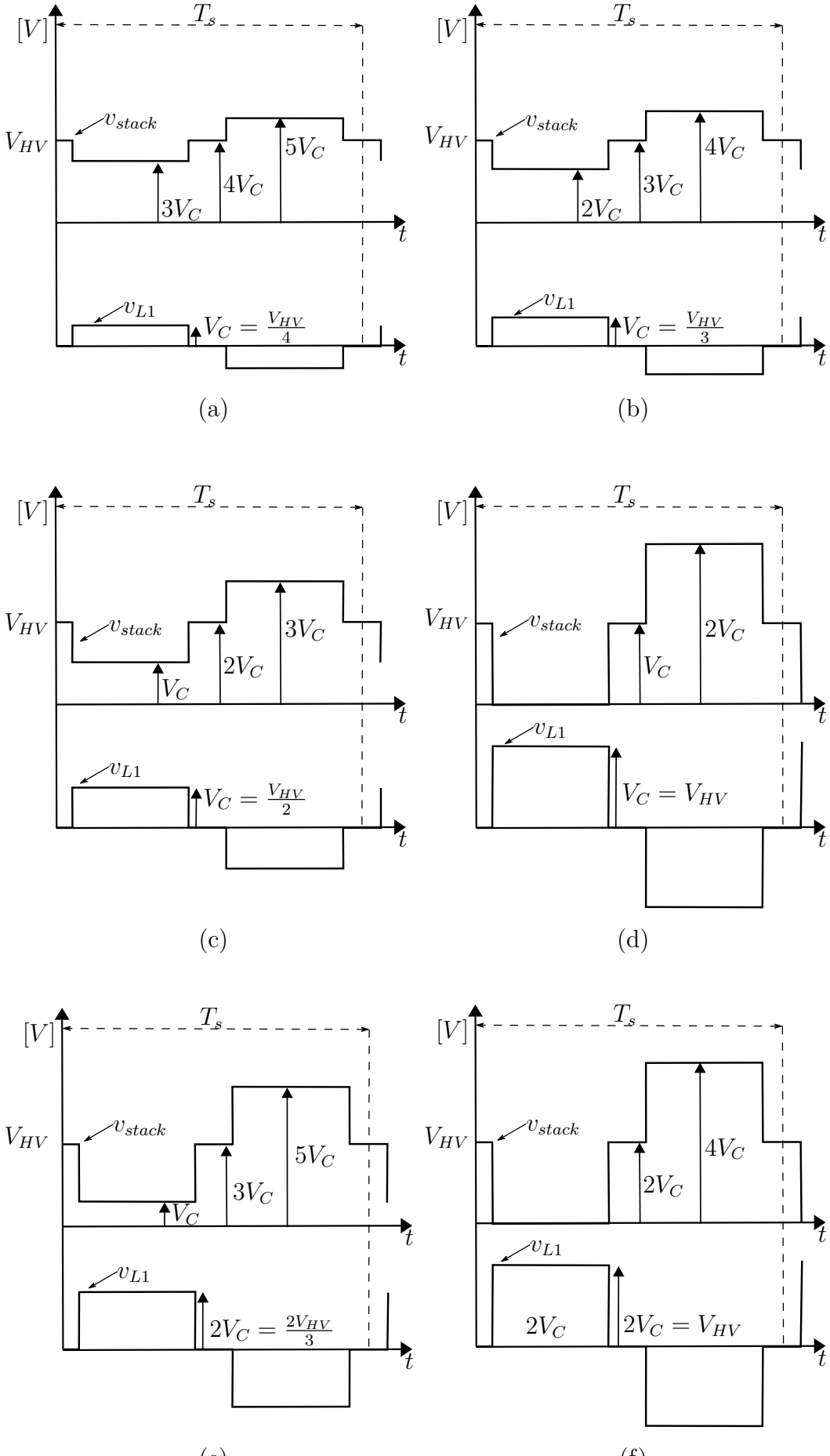


Figure 3.3: *Possible switching patterns for a stack formed by five half-bridge cells. (a) choice a, (b) choice b, (c) choice c, (d) choice d, (e) choice and (f) choice f.*

choices b,c,d and f present an alternative operation with one (state b and f), two (state c) or three (state d) redundant cells, as is shown in Fig. 3.3(b)-(f). Under this operation the converter can handle any faulty cell if it is by-passed and the rest of cells are adapted to the new operation. Thus, the converter has increased reliability, but at cost of a lower voltage step ratio in comparison with the choice a. The choices e and f are special (see Fig. 3.3 (e)(f)) because they require the simultaneous operation of two cells at all times due to the $N_a = 2$ configuration. Although these states are theoretically possible, their practical implementation have several drawbacks. The main issue is the difficulty in obtaining a completely synchronized operation of the cells due to the parameter variations of the devices, even if they are from the same batch. These variations usually leads to slight differences in the turn-on and turn-off times, resulting in one cell blocking the double nominal voltage while the other cell is still in transition. For this reason, the $N_a = 1$ states are the most economical and attractive choices for steady-state at nominal power, whilst leaving the $N_a > 1$ states for specials cases such as black-start, capacitors pre-charge stage or to face a big voltage dip at the HV port.

3.4 Asymmetrical Triangular Current Mode

Considering the stack operation previously presented which generates a voltage square-waveform centered on zero in v_{L1}, it is possible to apply any of the power control strategies for square-waveform voltages in the ac link. In this subsection, the application of the triangular current mode (TCM) to the High step ratio dc-dc MMC is studied.

TCM controls the power flow through the transition times of the voltages on both sides of the inductor. Therefore, the slope of the inductor current i_L is defined by the inductance L and its voltage, which is imposed by the difference between the voltages controlled by the stack v_{L1} and the full-bridge v_{L2} according to (3.1). Conventional TCM generates a symmetric current in

the inductor, which is desired for DAB converters, but it is a problem for the proposed topology. The issue is that a symmetric current would generate zero power flow from the high-voltage side because this current flows in series in the high-voltage dc-link. To solve this problem, an asymmetric triangular current mode (ATCM) scheme is proposed to create a dc current component without loosing their ZCS capability.

If the ac link voltage ratio r_V represents the ratio between the amplitude of the voltages at both sides of the inductor as

$$r_V = \frac{\hat{v}_{L2}}{\hat{v}_{L1}} = \frac{V_{LV}}{r_S V_{HV}} \tag{3.14}$$

it is possible find the total voltage transformation r_T ratio between dc ports in (3.15). It is noticeable that the total voltage ratio r_T can reach very low values due to the multiplicative effect of the stack voltage ratio r_S and r_V.

$$r_T = \frac{V_{LV}}{V_{HV}} = r_S \cdot r_V \tag{3.15}$$

Like the traditional TCM scheme, the case of $r_V = 1$ is unable to generate a triangular current, therefore TCM will be analyzed below for the following two different cases: i) $r_V > 1$ and ii) $r_V < 1$.

Case i) $\mathbf{r_V > 1}$

The general waveforms under the proposed ATCM scheme when $r_V > 1$ is illustrated in Fig. 3.4. During the intervals $[t_0, t_1]$, $[t_3, t_4]$ and $[t_6, t_0 + T_s]$, the voltages v_{L1} and v_{L2} are zero to keep the current i_L constant at I_0, I_1 and I_3 values respectively in each interval. In t_1, the cell stack imposes the $r_S V_{HV}$ voltage in v_{L1} whilst the full-bridge is kept in zero state. The voltage $r_S V_{HV}$ is therefore applied to the inductor, causing the current i_L to increase linearly. In t_2, the full-bridge imposes the low-voltage $n_T V_{LV}$ in v_{L2}, so the inductor voltage is defined by the difference of the voltages applied by both converters $(r_S V_{HV} - V_{LV})$. Because the voltage V_{LV} is greater than $r_S V_{HV}$ when $r_V > 1$,

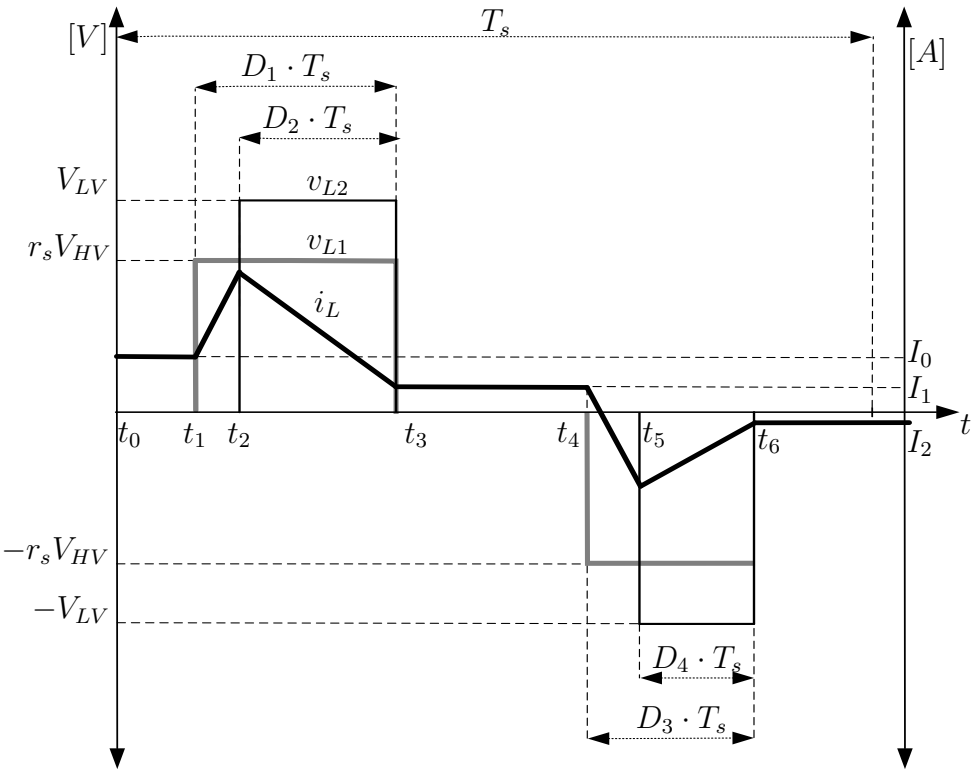


Figure 3.4: *General ac-link waveforms for positive power-flow under asymmetrical triangular current mode and $r_V > 1$.*

this generates a negative slope in the inductor current until time t_3. At this time, the stack and full-bridge simultaneously generate zero voltage in v_{L1} and v_{L2} to maintain the current constant until the time t_4. The same behaviour can be described in the second semi-cycle for negative values of v_{L1} and v_{L2}. Thus, the general equations for current i_L in positive power flow are show in (3.16).

$$i_L(t) = \begin{cases} I_0 & \text{if } t \in [t_0, t_1] \\ I_0 + \frac{r_S V_{HV}}{L}(t – t_1) & \text{if } t \in [t_1, t_2] \\ I_0 + \frac{r_S V_{HV}}{L}(t_2 – t_1) - \frac{V_{LV} – r_S V_{HV}}{L}(t – t_2) & \text{if } t \in [t_2, t_3] \\ I_1 & \text{if } t \in [t_3, t_4] \\ I_1 - \frac{r_S V_{HV}}{L}(t – t_4) & \text{if } t \in [t_4, t_5] \\ I_1 - \frac{r_S V_{HV}}{L}(t_5 – t_4) + \frac{V_{LV} – r_S V_{HV}}{L}(t – t_5) & \text{if } t \in [t_5, t_6] \\ I_2 & \text{if } t \in [t_6, t_0 + T_s] \end{cases} \tag{3.16}$$

In order to obtain ZCS transitions at t_1, t_3, t_4 and t_6 times, the currents of the zero voltage states I_0, I_1, I_2 must remains null. This can be achieved if the duty cycles D_i defined as in Fig. 3.4 satisfy the ZCS conditions described in (3.17).

$$\begin{aligned} D_2 &= \frac{D_1}{r_V} + \frac{I_0 L}{V_{LV} T_s} \\ D_4 &= \frac{D_3}{r_V} - \frac{I_1 L}{V_{LV} T_s} \end{aligned} \tag{3.17}$$

Thus, the steady-state waveforms with ZCS operation are shown in Fig. 3.5 (a). Under this scheme, the peak currents in the inductor i_L^{p1} and i_L^{p2} can be found in (3.18).

$$\begin{aligned} i_L^{pk_1} &= i_L(t_2) = \frac{r_S V_{HV}}{L}\left(1 - \frac{1}{r_V}\right) D_1 T_s \\ i_L^{pk_2} &= i_L(t_5) = -\frac{r_S V_{HV}}{L}\left(1 - \frac{1}{r_V}\right) D_3 T_s \end{aligned} \tag{3.18}$$

In order to calculate the power transferred between the high-voltage port, the low-voltage port and the interchange of power with the cells, the areas $A_{\triangle 1}$ and $A_{\triangle 2}$ are defined in (A.3) and illustrated in Fig. 3.5(a). These areas can be expressed as a function of the peak currents in the inductor i_L^{pk1} and i_L^{pk2} using the proposed ATCM, however this analysis could consider a generalized inductor current waveform at this point.

$$\begin{aligned} A_{\triangle 1} &= \int_{t_1}^{t_3} i_L \cdot dt = \frac{i_L^{pk_1} D_1 T_s}{2} \\ A_{\triangle 2} &= \int_{t_4}^{t_6} i_L \cdot dt = \frac{i_L^{pk_2} D_3 T_s}{2} \end{aligned} \tag{3.19}$$

Thus, the average power delivered by the high voltage port P_{HV} in one switching cycle T_s can be defined by the sum of these areas if the high volage V_{HV}

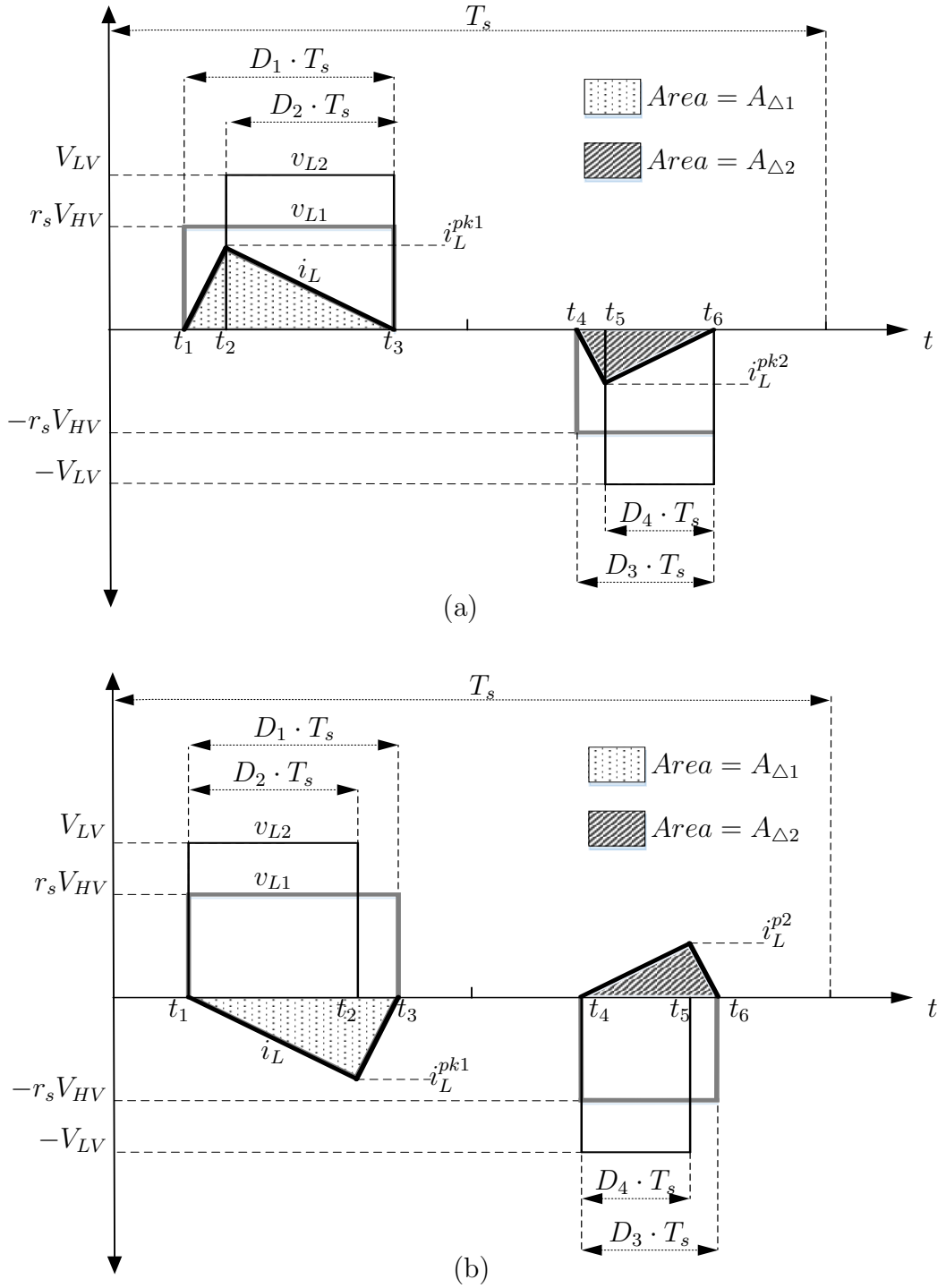


Figure 3.5: *Ac-link waveforms under ZCS-ATCM and $r_V > 1$ (a) HV to LV power-flow and (b) LV to HV power-flow.*

remains constant, as is shown in (A.2).

$$P_{HV} = \frac{1}{T_s} \int_{t_0}^{t_0+T_s} V_{HV} \cdot i_L \cdot dt = \frac{V_{HV}}{T_s}(A_{\triangle 1} + A_{\triangle 2}) \tag{3.20}$$

From (A.2), the high-voltage average power P_{HV} is null with symmetric operation ($A_{\triangle 1} = -A_{\triangle 2}$), which leads to a non-feasible operationg condition. Therefore, asymmetrical operation is a requirement to achieve a power balance between ports.

On the other hand, the average power for the low voltage port P_{LV} expression is found in (A.15), neglecting the power losses and the capacitors voltage ripple.

$$P_{LV} = \frac{1}{T_s} \int_{t_0}^{t_0+T_s} v_{L1} \cdot i_L \cdot dt = \frac{r_S V_{HV}}{T_s}(A_{\triangle 1} - A_{\triangle 2}) \tag{3.21}$$

Therefore, these two equations can be expressed in matrix form as (3.22), allowing control the power transfer through the modulation of the areas $A_{\triangle 1}$ an $A_{\triangle 2}$.

$$\begin{bmatrix} P_{HV} \\ \\ P_{LV} \end{bmatrix} = \frac{V_{HV}}{T_s} \begin{bmatrix} 1 & 1 \\ \\ r_S & -r_S \end{bmatrix} \begin{bmatrix} A_{\triangle 1} \\ \\ A_{\triangle 2} \end{bmatrix} \tag{3.22}$$

Alternatively, this matrix equation can be expressed as a function of the average power for the stack P_{stack} in (3.23), since it is the difference of these two average powers ($P_{stack} = P_{HV} - P_{LV}$) if the cell power losses are neglected.

$$\begin{bmatrix} P_{HV} \\ \\ P_{stack} \end{bmatrix} = \frac{V_{HV}}{T_s} \begin{bmatrix} 1 & 1 \\ \\ 1 - r_S & 1 + r_S \end{bmatrix} \begin{bmatrix} A_{\triangle 1} \\ \\ A_{\triangle 2} \end{bmatrix} \tag{3.23}$$

In order to achieve a steady state balance in the converter, the capacitor voltages must remain constant at the desired value v_c^*. This is achieved analysing

(3.6) and noticing that in the steady-state the stack power P_{stack} is null. Therefore, the voltage balance condition in steady-state under ATCM can derived from (3.23) imposing $P_{stack} = 0$. Thus, this condition can be expressed as in (3.24).

$$D_3 = D_1\sqrt{\frac{1 - r_S}{1 + r_S}} \tag{3.24}$$

The ratio $\frac{D_3}{D_1}$ also represents the level of asymmetry of the current in the inductor i_L needed to keep the capacitor voltages balances at steady-state. Thus, for a high voltage step ratio (high r_S) a low asymmetry is required.

Finally, the power transfer $P_{\triangle\, r_V>1}$ under ATCM at steady-state can be derived in (3.25), considering the ZCS and power balance conditions. This equation is useful to design the converter for a defined power rate and provide a good approximation of the steady-state operation for all power range through the control of D_1. Also, the feasible range for D_1 is limited by the time window of the switching cycle f_s, therefore, the sum of the external duty-cycles must fulfill the inequation $D_1 + D_3 \leq 1$.

$$P_{\triangle\, r_V>1} = \pm\frac{V_{HV}^2 \cdot r_S^2 \cdot (r_V - 1)}{f_s L \cdot r_V(r_S + 1)} D_1^2 \qquad \text{with } 0 < D_1 \leq \frac{1}{1 + \sqrt{\frac{1-r_S}{1+r_S}}} \tag{3.25}$$

A similar analysis can be performed for negative power flow inverting the phase shift of voltages v_{L1} and v_{L2} as is illustrated in Fig 3.5(b). Thus, these relationships allow full bidirectional control of the power flow whilst maintaining the ZCS and voltage balance in the converter.

Although the converter is designed to operate at a nominal voltage level and therefore for a fixed r_V parameter, any voltage disturbance in the ports will affect r_V proportionately. Therefore, an analysis of the impact of r_V on the power is needed in order to operate in a wide voltage range and for disturbed operation. Thus, the impact on the maximum power delivery per-unit in term

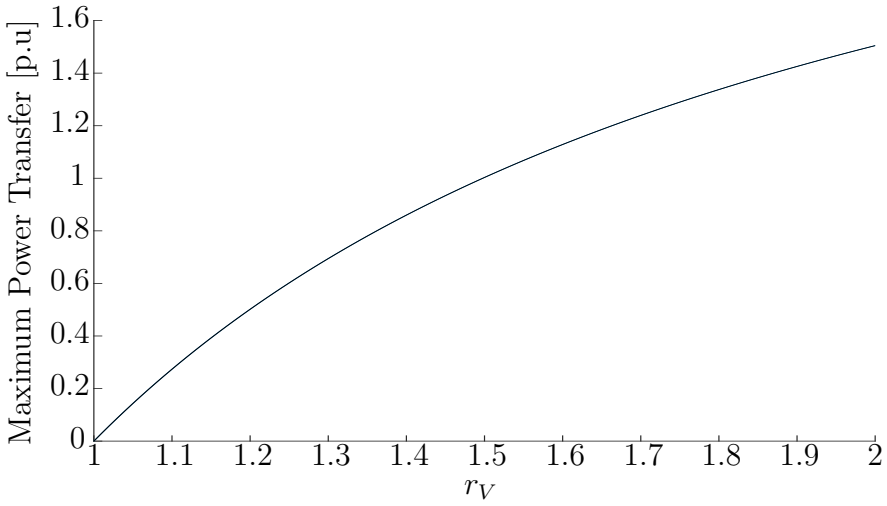


Figure 3.6: *Power range of $P_{\triangle\, r_V>1}$ with $r_S = \frac{1}{9}$.*

of r_V is shown in Fig. 3.6, considering $r_S = \frac{1}{9}$ as example and the power base as

$$P_{base} = \frac{V_{HV}^2 \cdot r_S^2}{12 f_s L}. \tag{3.26}$$

This power range provides suitable operation if r_V is much greater than one, but is highly limited if $r_V \approx 1$, as is shown in Fig. 3.6. Therefore, the converter design under this modulation must consider this limitation to ensure the ability to deliver power at a wide voltage operation. The latter should also consider the total voltage transformation requirement, since for a high voltage transformation ratio application, r_V should ideally be as low as possible.

Case ii) $\mathbf{r_V < 1}$

Other alternative operation of ATCM is the $r_V < 1$ case, which is illustrated in Fig. 3.7. In the same way as in the case $r_V > 1$, during the intervals $[t_0, t_1]$, $[t_3, t_4]$ and $[t_6, t_0 + T_s]$, the voltages v_{L1} and v_{L2} are zero to keep the current i_L constant. At t_1, the cell stack impose the $r_s V_{HV}$ voltage in v_{L1} and the full-bridge imposes the low-voltage V_{LV} in v_{L2}. Since the voltage $r_S V_{HV}$ is greater than V_{LV} when $r_V < 1$, this generates a positive slope in the inductor current, causing the current i_L to increase linearly. At t_2, the v_{L1} voltage

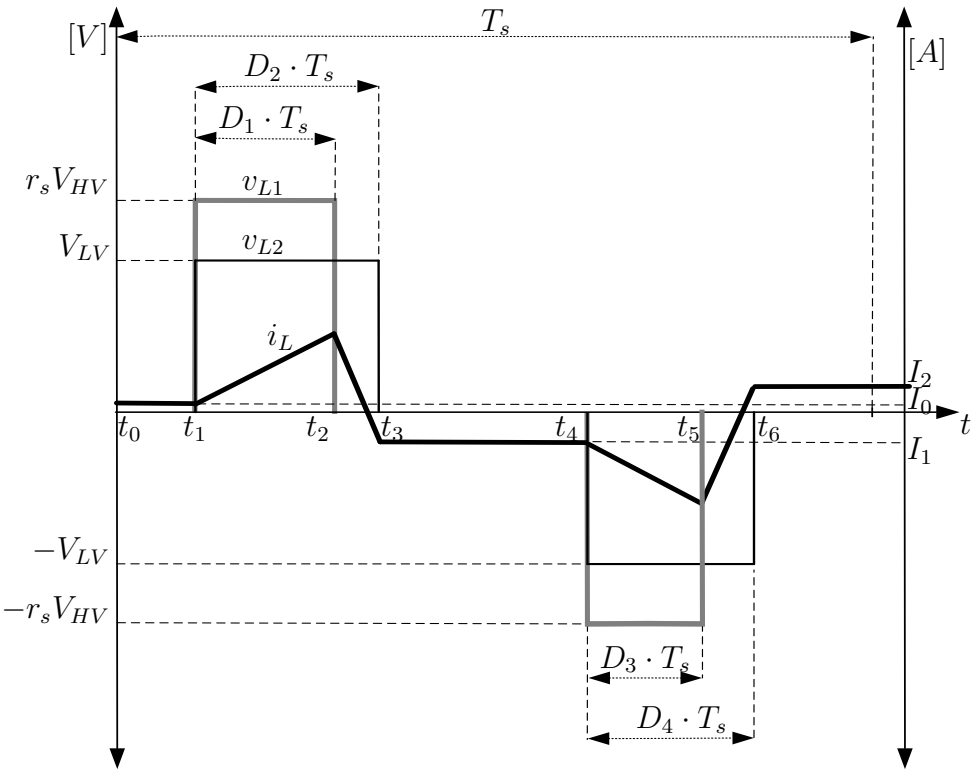


Figure 3.7: *General ac-link waveforms for positive power-flow under asymmetrical triangular current mode and $r_V < 1$.*

change to zero while the full-bridge continue imposing the low-voltage V_{LV} in v_{L2}. Since $r_V < 1$, this generates a negative voltage at the inductor, yielding a negative slope of the inductor current until time t_3. At this time, the full-bridge generate zero voltage in v_{L2} to maintain the current constant until time t_4. The same behaviour can be described in the second semi-cycle for negative values of v_{L1} and v_{L2}. Thus, the general equations for current i_L in positive power flow are shown in (3.27).

$$i_L(t) = \begin{cases} I_0 & \text{if } t \in [t_0, t_1] \\ I_0 + \frac{(r_S V_{HV} - V_{LV})}{L}(t - t_1) & \text{if } t \in [t_1, t_2] \\ I_0 + \frac{(r_S V_{HV} - V_{LV})}{L}(t_2 - t_1) - \frac{V_{LV}}{L}(t - t_2) & \text{if } t \in [t_2, t_3] \\ I_1 & \text{if } t \in [t_3, t_4] \\ I_1 - \frac{(r_S V_{HV} - V_{LV})}{L}(t - t_4) & \text{if } t \in [t_4, t_5] \\ I_1 - \frac{(r_S V_{HV} - V_{LV})}{L}(t_5 - t_4) + \frac{V_{LV}}{L}(t - t_5) & \text{if } t \in [t_5, t_6] \\ I_2 & \text{if } t \in [t_6, t_0 + T_s] \end{cases} \tag{3.27}$$

In order to obtain ZCS transitions at t_1, t_3, t_4 and t_6 times, the currents of the zero voltage states I_0, I_1, I_2 must remains null. In the same way as in the case $r_V > 1$, this can be achieved if the the duty cycles D_i satisfy the ZCS conditions founded in (3.17).

Thus, the steady-state waveforms with ZCS operation are shown in Fig. 3.8 (a). Under this scheme, the peak currents in the inductor i_L^{p1} and i_L^{p2} are shown in (3.28)), which are slightly different of the expressions found in (3.18)) for the case $r_V > 1$.

$$\begin{aligned} i_L^{pk_1} &= i_L(t_2) = \frac{r_S V_{HV} \cdot r_V(1 - r_V)}{L} D_2 T_s \\ i_L^{pk_2} &= i_L(t_5) = -\frac{r_S V_{HV} \cdot r_V(1 - r_V)}{L} D_4 T_s \end{aligned} \tag{3.28}$$

Since the externals duty-cycles are D_2 and D_4 for the case $r_V < 1$, the areas $A_{\triangle 1}$ and $A_{\triangle 2}$ are updated in (3.29).

$$\begin{aligned} A_{\triangle 1} &= \int_{t_1}^{t_3} i_L \cdot dt = \frac{i_L^{pk_1} D_2 T_s}{2} \\ A_{\triangle 2} &= \int_{t_4}^{t_6} i_L \cdot dt = \frac{i_L^{pk_2} D_4 T_s}{2} \end{aligned} \tag{3.29}$$

Therefore, the matrix form of the power equations is shown in (3.30) if P_{stack} is used instead of P_{LV}.

$$\begin{bmatrix} P_{HV} \\ \\ P_{stack} \end{bmatrix} = \frac{V_{HV}}{T_s} \begin{bmatrix} 1 & 1 \\ \\ 1 - r_S r_V & 1 + r_S r_V \end{bmatrix} \begin{bmatrix} A_{\triangle 1} \\ \\ A_{\triangle 2} \end{bmatrix} \tag{3.30}$$

Therefore, the voltage balance condition in steady-state under ATCM with

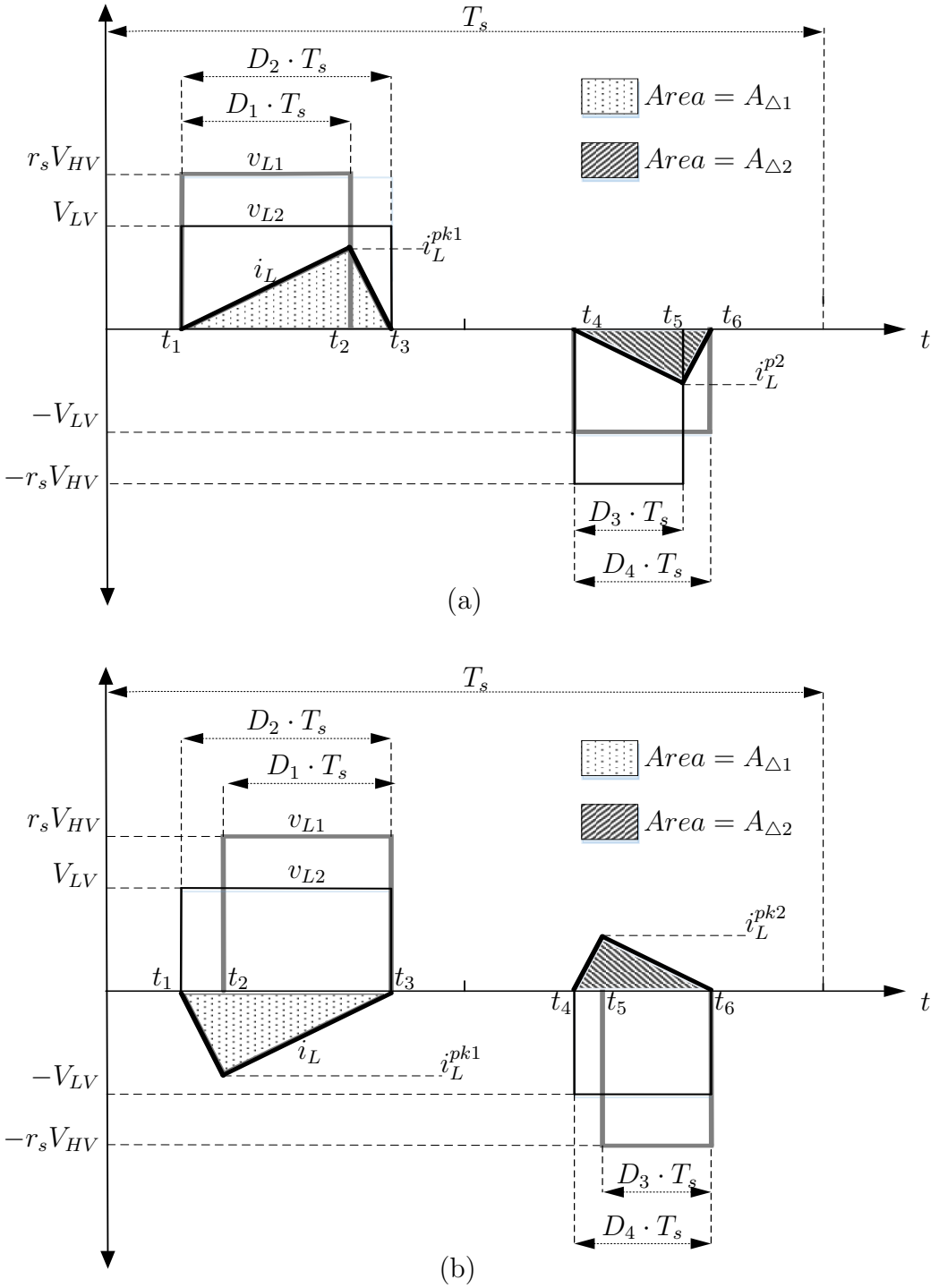


Figure 3.8: *Ac-link waveforms under ZCS-ATCM and $r_V < 1$ (a) HV to LV power-flow and (b) LV to HV power-flow.*

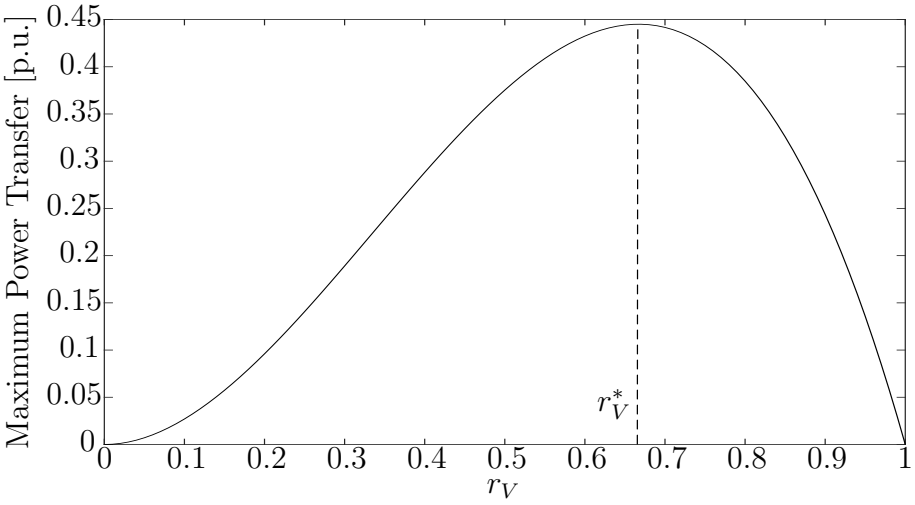


Figure 3.9: *Power range limit of $P_{\triangle\, r_V<1}$ with $r_S = \frac{1}{9}$.*

$r_V > 1$ is found (3.31), using the same procedure realised for the case $r_V < 1$.

$$D_4 = D_2\sqrt{\frac{1 - r_S r_V}{1 + r_S r_V}} \tag{3.31}$$

Finally, the power transfer $P_{\triangle\, r_V<1}$ under ATCM with $r_V > 1$ at steady-state is derived in (3.32), considering the feasible range for D_2 ($D_2 + D_4 \leq 1$). If the phase-shift of the voltages v_{L1} and v_{L2} is inverted, the converter is able to generate negative power flow, as is shown in Fig 3.8(b).

$$P_{\triangle\, r_V<1} = \pm\frac{V_{HV}^2 \cdot r_S^2 \cdot r_V^2 \cdot (1 - r_V)}{f_s L(r_S r_V + 1)} D_2^2 \qquad \text{with } 0 < D_2 \leq \frac{1}{1 + \sqrt{\frac{1-r_S r_V}{1+r_S r_V}}} \tag{3.32}$$

The influence of r_V on the maximum power delivery per-unit under this scheme is shown in Fig. 3.9, considering the same power base P_{base} and r_S as the previously presented case for $r > 1$. The maximum power under this modulation is achieved at r_V^*, but it is highly limited if $r_V \approx 1$ or $r_V \approx 0$. Therefore, it is recommended to design the operation around r_V^* to have a wider power range.

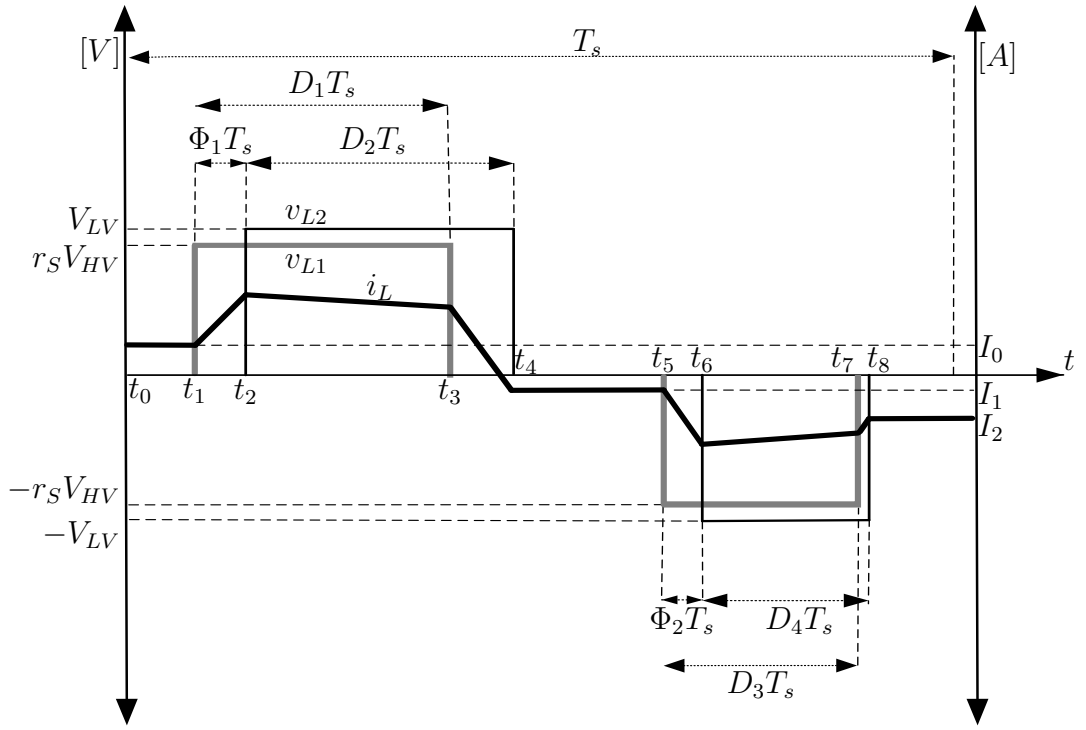


Figure 3.10: *General ac-link waveforms for positive power-flow under asymmetrical trapezoidal current mode.*

3.5 Trapezoidal Current Mode

As an alternative to the triangular current mode, the trapezoidal current mode is an attractive option to modulate the current at the ac-link. The trapezoidal current operation extends the power range for the cases $r_V \approx 1$, where the ATCM power range is limited or even not feasible.

The inductor current i_L has a trapezoidal shape if the commutation times t_i are arranged as shown in Fig. 3.10. This scheme adds two additional commutation times in a switching cycle, which are controlled by the phase-shifts Φ_1 and Φ_2.

Thus, the resultant generalised trapezoidal waveform is defined as the piece-

wise function (3.33).

$$i_L(t) = \begin{cases} I_0 & \text{if } t \in [t_0, t_1] \\ I_0 + \frac{r_S V_{HV}}{L}(t–t_1) & \text{if } t \in [t_1, t_2] \\ I_0 + \frac{r_S V_{HV}}{L}(t_2–t_1) + \frac{(r_S V_{HV} - V_{LV})}{L}(t–t_2) & \text{if } t \in [t_2, t_3] \\ I_0 + \frac{r_S V_{HV}}{L}(t_2–t_1) + \frac{(r_S V_{HV} - V_{LV})}{L}(t_3–t_2) - \frac{V_{LV}}{L}(t–t_3) & \text{if } t \in [t_3, t_4] \\ I_1 & \text{if } t \in [t_4, t_5] \\ I_1 - \frac{r_S V_{HV}}{L}(t–t_5) & \text{if } t \in [t_5, t_6] \\ I_1 - \frac{r_S V_{HV}}{L}(t_6–t_5) - \frac{(r_S V_{HV} - V_{LV})}{L}(t–t_6) & \text{if } t \in [t_6, t_7] \\ I_1 - \frac{r_S V_{HV}}{L}(t_6–t_5) - \frac{(r_S V_{HV} - V_{LV})}{L}(t_7–t_6) + \frac{V_{LV}}{L}(t–t_7) & \text{if } t \in [t_7, t_8] \\ I_2 & \text{if } t \in [t_8, t_0 + T_s] \end{cases} \quad (3.33)$$

As in the ATCM cases, the i_L current yields ZCS for half of the commutations (t_1,t_4,t_5 and t_8) if (3.17) holds. Accordingly, ZCS operation of the trapezoidal current mode is shown in Fig. 3.11(a) with corresponding piece-wise function results in (3.34).

$$i_L(t) = \begin{cases} 0 & \text{if } t \in [t_0, t_1] \\ \frac{r_S V_{HV}}{L}(t–t_1) & \text{if } t \in [t_1, t_2] \\ \frac{r_S V_{HV}}{L}\Phi_1 T_s + \frac{r_S \cdot V_{HV} \cdot (1–r_V)}{L}(t–t_2) & \text{if } t \in [t_2, t_3] \\ \frac{r_S V_{HV}}{L}\Phi_1 T_s + \frac{r_S \cdot V_{HV} \cdot (1–r_V)}{L}(D_1 - \Phi_1)T_s - \frac{r_S \cdot V_{HV} \cdot r_V}{L}(t–t_3) & \text{if } t \in [t_3, t_4] \\ 0 & \text{if } t \in [t_4, t_5] \\ -\frac{r_S V_{HV}}{L}(t–t_5) & \text{if } t \in [t_5, t_6] \\ -\frac{r_S V_{HV}}{L}\Phi_2 T_s - \frac{r_S \cdot V_{HV} \cdot (1–r_V)}{L}(t–t_6) & \text{if } t \in [t_6, t_7] \\ -\frac{r_S V_{HV}}{L}\Phi_2 T_s - \frac{r_S \cdot V_{HV} \cdot (1–r_V)}{L}(D_3 - \Phi_2)T_s + \frac{r_S \cdot V_{HV} \cdot r_V}{L}(t–t_7) & \text{if } t \in [t_7, t_8] \\ 0 & \text{if } t \in [t_8, t_0 + T_s] \end{cases} \quad (3.34)$$

Furthermore, a perfect trapezoidal current can be generated with $r_V = 1$, however, in the following analysis r_V is considered as a parameter for generality. To model the exchange of power between the high-voltage port, the low-voltage

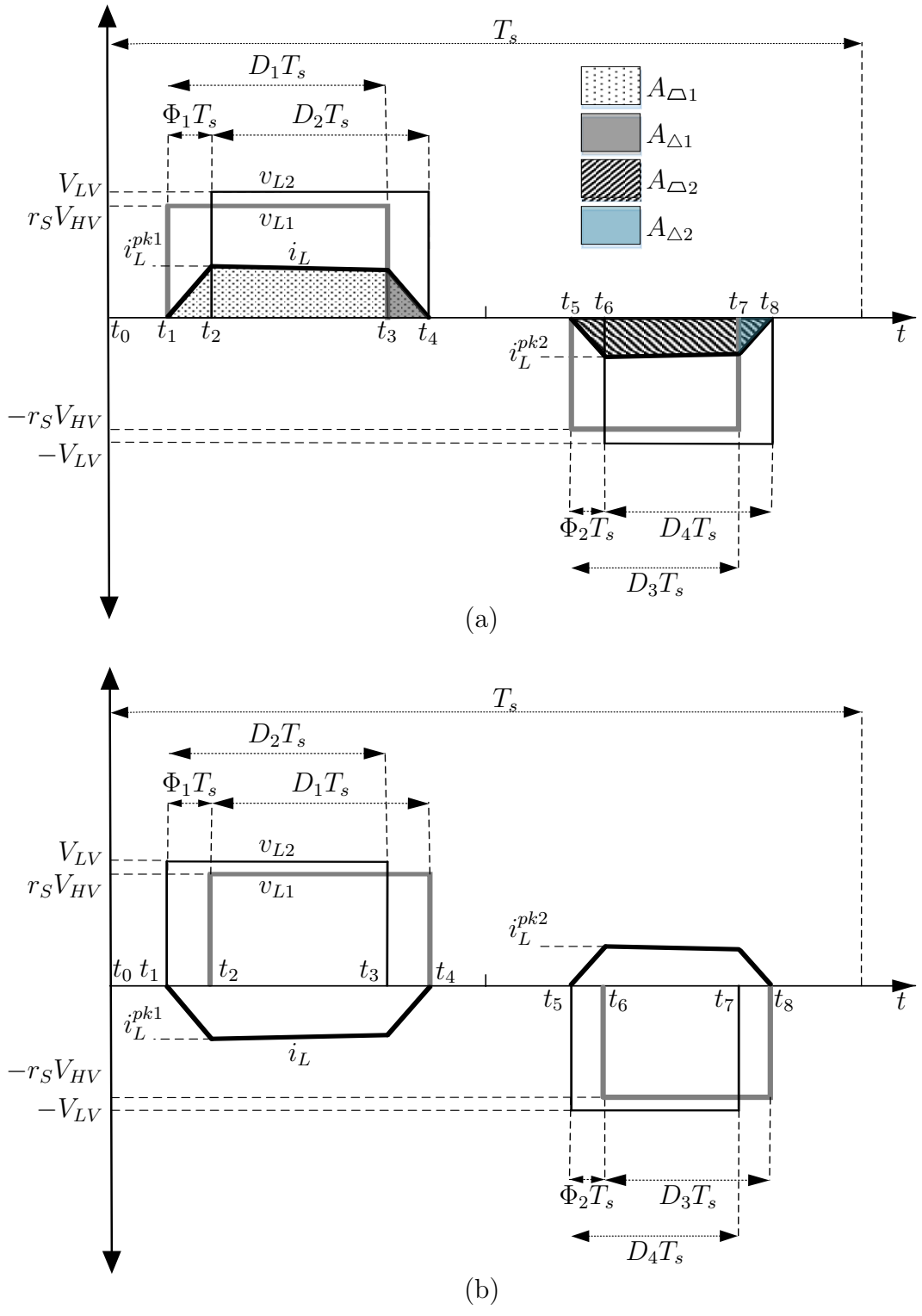


Figure 3.11: *Current and voltage waveforms for converter under ZCS trapezoidal modulations: (a) power flow from high-voltage side to low voltage side. (b) power flow from low-voltage side to high-voltage side.*

port and the cell stack, the areas covered for the inductor current in the positive ($A_{\triangle 1}$) and negative ($A_{\triangle 2}$) cycles of the switching cycle f_s are defined in (3.35) and illustrated in Fig. 3.10 (a). Thus, these areas can be expressed as a function of the phase-shifts Φ_i and the duty-cycles D_i if the ZCS condition (3.17) holds.

$$\begin{aligned} A_{\triangle 1} &= \int_{t_1}^{t_4} i_L \cdot dt = \frac{V_{HV} \cdot r_S}{2Lf_s^2} \left(2D_1\Phi_1 + D_1^2(\frac{1}{r_V} - 1) \right) \\ A_{\triangle 2} &= \int_{t_5}^{t_8} i_L \cdot dt = -\frac{V_{HV} \cdot r_S}{2Lf_s^2} \left(2D_3\Phi_2 + D_3^2(\frac{1}{r_V} - 1) \right) \end{aligned} \tag{3.35}$$

If the ZCS operation of the trapezoidal current mode is achieved, the average power delivered by the high-voltage port in one switching cycle P_{HV} is determined by the high voltage V_{HV} and the sum of the areas $A_{\triangle 1}$ and $A_{\triangle 2}$ as is shown in (3.36).

$$P_{HV} = \frac{1}{T_s} \int_{t_0}^{t_0+T_s} V_{HV} \cdot i_L \cdot dt = \frac{V_{HV}}{T_s}(A_{\triangle 1} + A_{\triangle 2}) \tag{3.36}$$

Therefore, the final expression for the high-voltage power P_{HV} as function of of the phase-shifts Φ_i and the duty-cycles D_i is found in (3.37). Its per-unit expression $P_{HV,pu}$ is obtained considering the power base as $P_{base} = \frac{V_{HV}^2 \cdot r_S^2}{12 f_s L}$. This power-base corresponds to the maximum power transfer for the case $r_V = 1$, as will be shown further through (3.43). Also, a detailed derivation of P_{HV} is included in Appendix A.

From (3.37) and like the previous current modulations, the high voltage average power P_{HV} is null with symmetric operation ($D_1 = D_3$ and $\Phi_1 = \Phi_2$), which leads to a non-feasible operation. Hence, asymmetrical operation is a requirement to achieve steady-state operation.

$$
\begin{aligned}
P_{HV} &= \frac{V_{HV}^2 \cdot r_S}{2 f_s L}\left(2D_1\Phi_1 - 2D_3\Phi_2 + (D_1^2 - D_3^2)(\frac{1}{r_V} - 1)\right) \\
P_{HV,_{pu}} &= \frac{6}{r_S}\left(2D_1\Phi_1 - 2D_3\Phi_2 + (D_1^2 - D_3^2)(\frac{1}{r_V} - 1)\right)
\end{aligned}
\tag{3.37}
$$

On the other hand, the average power in the low-voltage port at one switching cycle P_{LV} can be determined using the same method. For this case, the areas $A_{\triangle 1}$ and $A_{\triangle 2}$ covered for the inductor current in the intervals (t_3,t_4) and (t_7,t_8) are defined in (3.38) and illustrated in Fig. 3.10 (a).

$$
\begin{aligned}
A_{\triangle 1} &= \int_{t_3}^{t_4} i_L \cdot dt = \frac{V_{HV} \cdot r_S \cdot r_V}{2 L f_s^2}\left(\Phi_1 + D_1(\frac{1}{r_V} - 1)\right)^2 \\
A_{\triangle 2} &= \int_{t_7}^{t_8} i_L \cdot dt = -\frac{V_{HV} \cdot r_S \cdot r_V}{2 L f_s^2}\left(\Phi_2 + D_3(\frac{1}{r_V} - 1)\right)^2
\end{aligned}
\tag{3.38}
$$

These two areas allow express the low-voltage port power as

$$
P_{LV} = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} v_{L1} \cdot i_L \cdot dt = \frac{V_{HV} \cdot r_S}{T_s}\left((A_{\square 1} - A_{\triangle 1}) - (A_{\square 2} - A_{\triangle 2})\right) \tag{3.39}
$$

leading to define the low-voltage power P_{LV} as function of of the phase-shifts Φ_i and the duty-cycles D_i in (3.40). A detailed derivation of P_{LV} is included in Appendix A.

$$
\begin{aligned}
P_{LV} &= \frac{V_{HV}^2 \cdot r_S^2 \cdot r_V}{2 f_s L}\left(2D_1\Phi_1 + 2D_3\Phi_2 + (D_1^2 + D_3^2)(\frac{1}{r_V} - 1) - \Phi_1^2 - \Phi_2^2\right) \\
P_{LV,pu} &= 6 r_V\left(2D_1\Phi_1 + 2D_3\Phi_2 + (D_1^2 + D_3^2)(\frac{1}{r_V} - 1) - \Phi_1^2 - \Phi_2^2\right)
\end{aligned}
\tag{3.40}
$$

Thus, it is possible to control the power transfer between the high-voltage and low-voltage ports through (3.37) and (3.40), maintaining the voltage balance in the capacitors. The difference between these powers allows to charge or dis-

charge the capacitors in one cycle T_s, and the steady state balance is achieved when both powers remain identical at both sides of the converter ($P_{HV} = P_{LV}$) if the power losses are neglected. A similar analysis can be performed for negative power flow inverting the phase-shift of voltages v_{L1} and v_{L2} (Φ_1 and Φ_2) as is illustrated in Fig. 3.10 (b). Therefore, these relationships allow full bidirectional control of the power flow maintaining ZCS and voltage balance in the converter.

Differently from the triangular case, where the steady-state power is controlled by only one duty-cycle, the trapezoidal current mode provides a set of general solutions (Φ_1, Φ_2, D_1, D_3) for a specific power transfer, which has two degrees of freedom due to the incorporation of the additional variables Φ_1 and Φ_2. Thus, an optimisation problem can be defined for a given state to find the best solution from all feasible alternatives.

3.5.1 Optimisation problem

In this subsection, the trapezoidal current mode optimisation problem is discussed and solved numerically. Also, an analytical approach is employed to help understand the problem and their results.

Because the soft-switching operation of the trapezoidal current mode naturally leads to reduced switching losses, the minimisation of the conduction losses rises as an attractive objective of the optimisation problem in order to reduce the total power losses and to achieve more efficient operation. Thus, the optimization problem is set to minimise the square of the rms inductor current per-unit $i_{L,pu}^{rms}$, since to the conduction losses of the passive elements and devices are highly dependent of this rms current. The derivation of this rms inductor current per-unit as function of ($\Phi_1, \Phi_2, D_1, D_3, r_V$) is found in Appendix B.1.

Since the rms inductor current $i_{L,pu}^{rms}$ is nonlinear, a nonlinear optimisation problem (NLP) is defined in (3.41) to find the optimal solution $(\Phi_1, \Phi_2, D_1, D_3)^{op}$

which produce the minimal rms current. The constraints of this optimisation problem are the power conditions and the feasible range of the solution. The power constraints are defined by the power references $P^*_{HV,pu}$ and $P^*_{LV,pu}$ required for the power balance between ports, whilst the set of possible solutions are restricted to positive solutions and fitted to the maximum time-window T_s.

$$\begin{aligned} \min_{\Phi_1,\Phi_2,D_1,D_3} \quad & J = (i^{rms}_{L,pu})^2 \\ \text{subject to} \quad & P_{HV,pu} = P^*_{HV,pu} \\ & P_{LV,pu} = P^*_{LV,pu} \\ & \Phi_1 + \Phi_2 + \tfrac{D_1}{r_V} + \tfrac{D_3}{r_V} \leq 1 \\ & \Phi_1, \Phi_2, D_1, D_3 \geq 0 \end{aligned} \tag{3.41}$$

This NLP is numerically solved in MATLAB using an interior point algorithm [214] for a wide range of the parameters (r_V, r_S) and power references. Thus, a lookup table can store the optimised results for future utilization and comparison.

Analytical approach at steady-state with $r_V \approx 1$

A significant analysis of the NLP problem is required to explain their results due to the solution of the problem is highly dependent on r_V. Thus, an analytic approach to the NLP problem is subsequently made for some representative cases.

For the case $r_V \approx 1$, the problem of minimising $(i^{rms}_{L,pu})^2$ is equivalent to the minimisation of $\Phi_1 + \Phi_2$ or the maximisation of $D_1 + D_2$, as demonstrated in Appendix B.2. This can be interpreted as saying that the minimisation problem for $(i^{rms}_{L,pu})^2$ is equivalent to maximising the current utilisation in the time-window T_s. If the current does not fit the entire time-window (Fig. 3.10 (a)), this pulsating current generates higher rms inductor current than an equivalent current which utilise the full time-window (Fig. 3.12 (c)). Therefore, the solution of the NLP is allocated in the superior limit of the inequality constriction for D_1 and D_3. Thus, it is possible to find the optimized solution if

this constraint is considered as an equality. Hence, the per-unit power function P_{pu} can be found as a function of Φ_1 and Φ_2, solving the system of equations (3.42) which considers the steady-state constraint ($P^*_{HV,pu} = P^*_{LV,pu} = P_{pu}$) and the time-window maximisation.

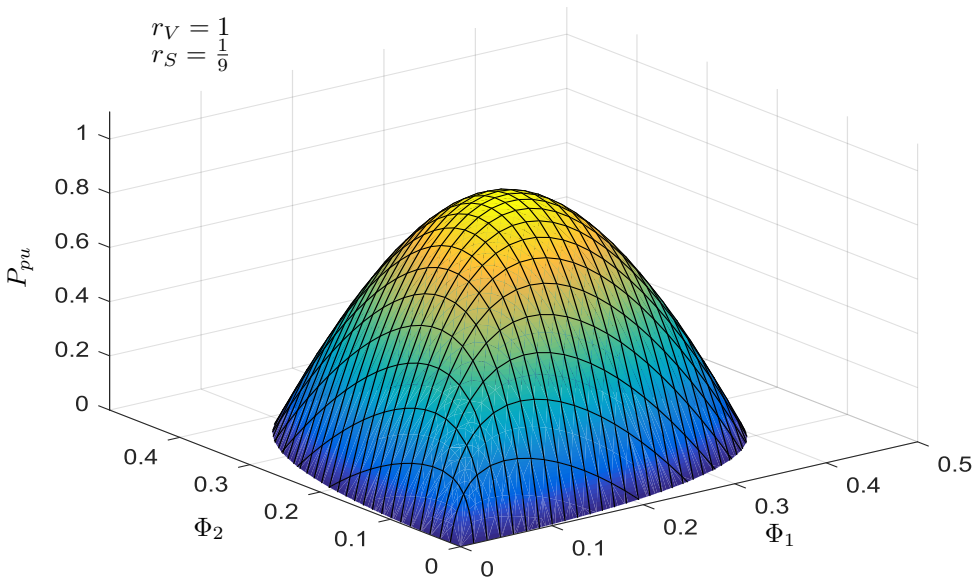
$$\begin{aligned} P_{HV,pu} &= P_{pu} \\ P_{LV,pu} &= P_{pu} \\ \Phi_1 + \Phi_2 + \frac{D_1}{r_V} + \frac{D_3}{r_V} &= 1 \end{aligned} \tag{3.42}$$

The power function P_{pu} which solves (3.42) is illustrated in Fig. 3.12 (a) considering the more straightforward case to analyze ($r_V = 1$) and $r_S = 1/9$ as an example. The contours lines of this surface and the numeric solutions of the NLP for different power references P^*_{pu} are shown in Fig. 3.12 (b), confirming that the optimal solution is allocated in these contours lines. The comparison of three feasible solutions for a reference of power $P^*_{pu} = 0.8$ is shown in Fig. 3.12 (c) to illustrate the negative impact on the inductor current of the non-optimal solutions (cases 1 and 2). From Fig. 3.12 (b), the NLP numerical solutions are allocated near the curve $\Phi_1 = \Phi_2$. Thus, if the approximation $\Phi_1 = \Phi_2$ is imposed, the optimal power function can be simplified to

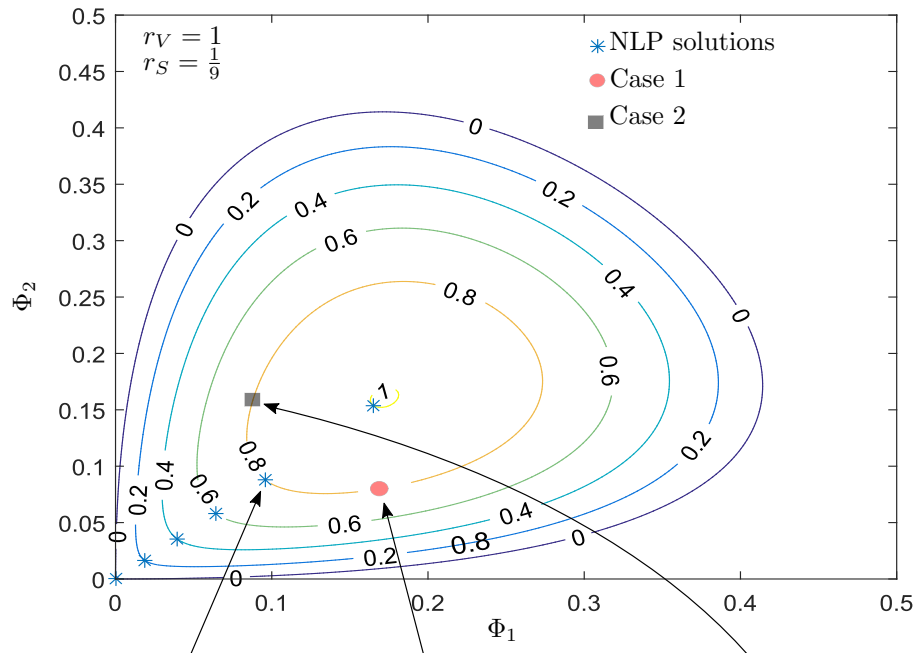
$$P_{pu,\Phi_2=\Phi_1} = 12 \cdot \Phi_1(1 - 3\Phi_1). \tag{3.43}$$

The maximum power transfer for this case is obtained at $\Phi_1 = 1/6$, resulting in a power per-unit equal to unity.

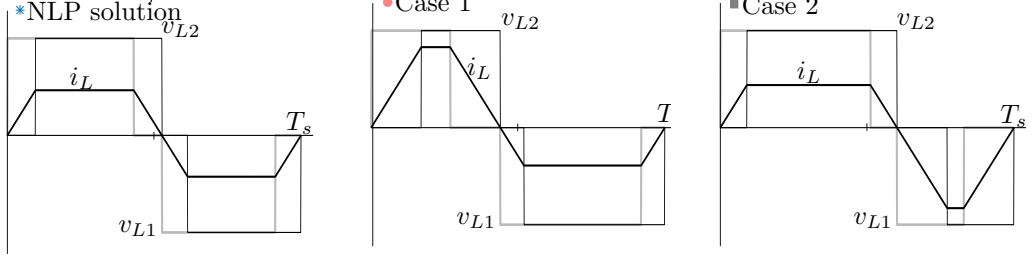
A similar analysis can be performed for the case $r_V < 1$. Following the same idea, it is possible to find a power function dependant on Φ_1 and Φ_2. The power function P_{pu} and the contour lines of the power function per-unit surface together with the numeric solutions of the NLP for different power references P^*_{pu} are shown in Fig. 3.13 (a)(b) for the case $r_V = 0.85$. As in the previous case, the NLP numerical solutions are allocated near the curve $\Phi_1 = \Phi_2$,



(a)



(b)



(c)

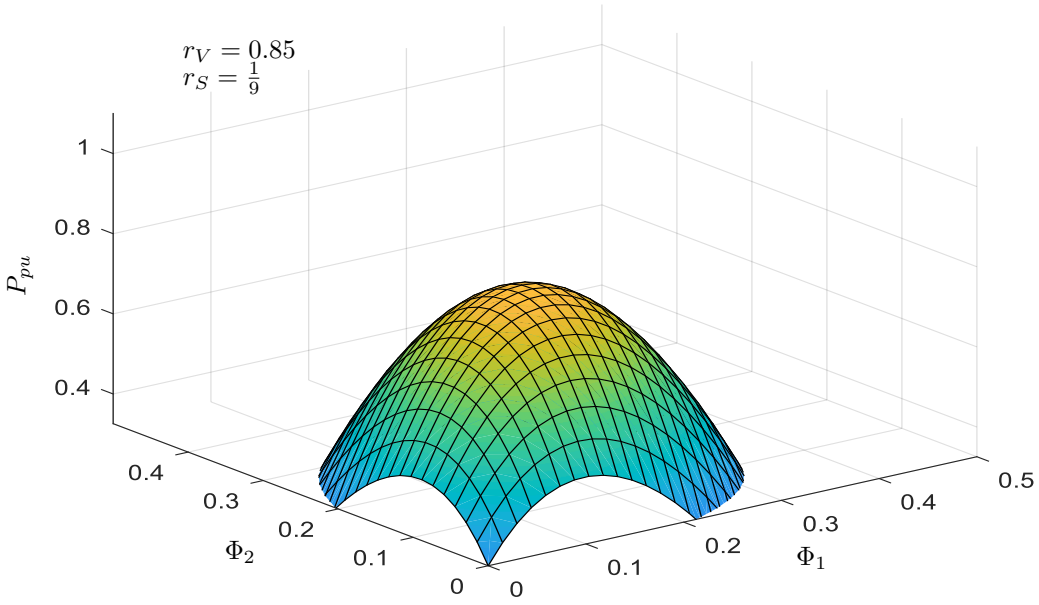
Figure 3.12: *Power curves with* $r_V = 1$ *and* $r_S = \frac{1}{9}$. *(a) Power function. (b) Power contour lines. (c) Waveforms of feasible solutions for* $P^* = 0.8$.

allowing simplification of the problem.

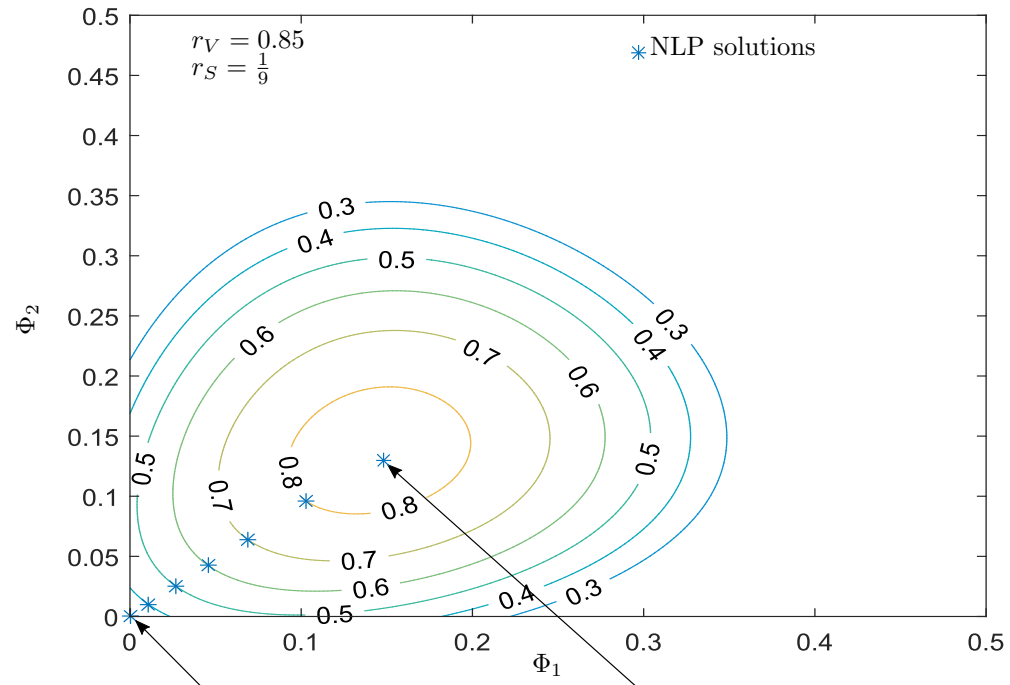
However, there is a limit for the power range where it is possible to find feasible solutions using the contour lines. The new superior limit of this power range is determined by the limitation of the parameter r_V since the power is almost proportional to r_V, as can be seen in (A.15). This limit case is illustrated in Fig. 3.13 (d) considering $r_V = 0.85$ and $r_S = \frac{1}{9}$ as an example, generating a maximum power transfer of $P^* = 0.844$. On the other hand, the inferior limit is achieved when the current is no longer trapezoidal at $\Phi_1 = 0$ and $P^* = 0.326$. At this limit case (Fig. 3.13 (c)) the current starts to be triangular, enabling the asymmetric triangular current mode (ATCM) with $r_V < 1$ for power references lower than the inferior limit. Thus, ATMC is able to modulate through the duty cycle beyond this limit if the time-window restriction (3.42) is released. Furthermore, the ATCM is also the solution of the NLP problem, achieving the minimal rms inductor current in this power range.

The analysis for the case $r_V > 1$ is similar. The contour lines of the power function per-unit surface and the numerical solutions of the NLP for different power references P^*_{pu} are shown in Fig. 3.14 (a)(b) for the case $r_V = 1.15$. As in the previous case, the NLP numerical solutions are allocated near the curve $\Phi_1 = \Phi_2$ (Fig. 3.14 (b)), and the limit cases are illustrated in Fig. 3.13 (c)(d). The inferior limit for the power P_{pu} is achieved when the current is no longer trapezoidal at $P^* = 0.392$. At this limit case (Fig. 3.14 (c)) the current starts to be triangular, enabling the asymmetric triangular current mode (ATCM) with $r_V > 1$ for power references lower than this limit.

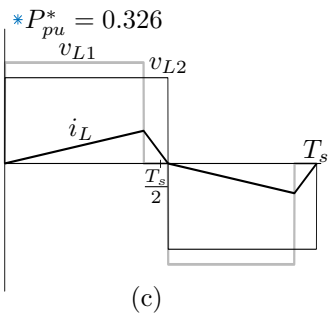
Therefore, the trapezoidal and triangular current modes are complementary modes for an optimized modulation. This general approach allows incorporation of ATCM in the analysis, noticing that the ATCM is a particular case of the trapezoidal current mode when some conditions are achieved. The conditions to obtain ATCM from trapezoidal current mode are summarised in Table 3.2 for any r_V and for both positive negative power-flow.



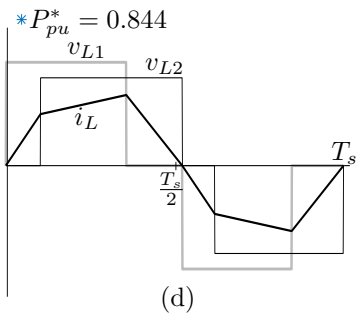
(a)



(b)

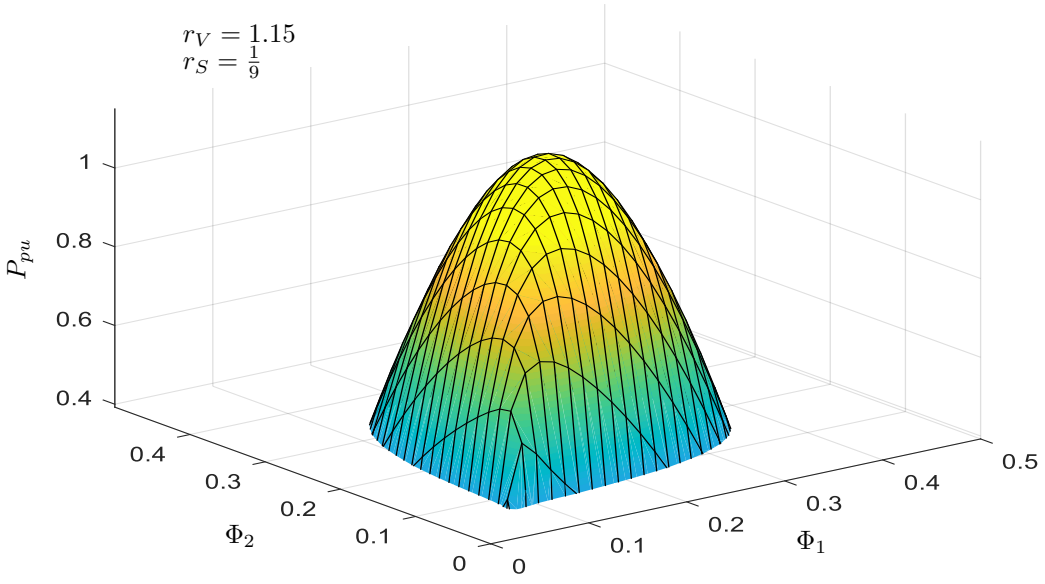


(c)

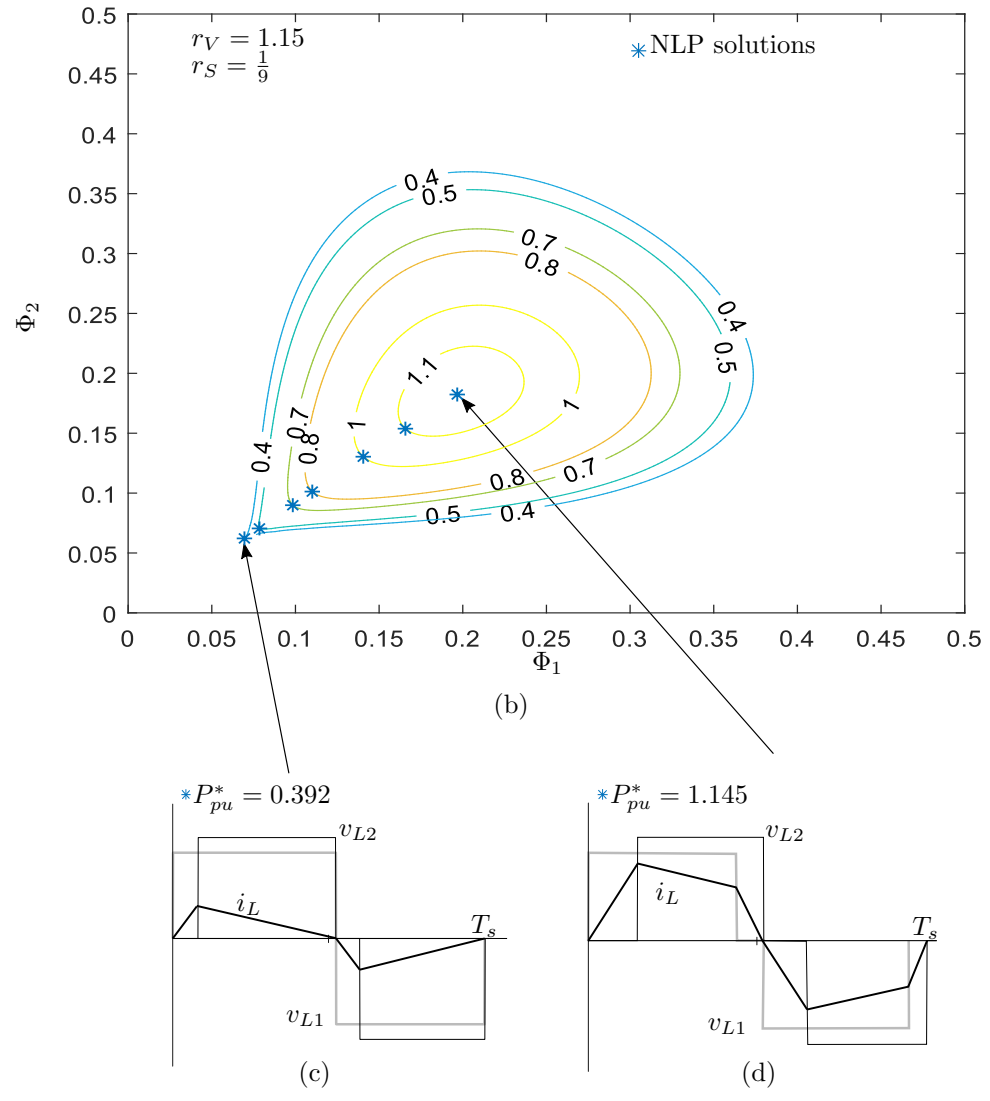


(d)

Figure 3.13: *Power contour lines with $r_V = 0.85$ and $r_S = \frac{1}{9}$. Waverforms for limit cases using trapezoidal mode.*



(a)



(b)

(c)

(d)

Figure 3.14: *Power contour lines with* $r_V = 1.15$ *and* $r_S = \frac{1}{9}$. *Waverforms for limit cases using trapezoidal mode.*

Table 3.2: Conditions to obtain triangular current mode from trapezoidal current mode.

Operation	$r_V < 1$	$r_V > 1$
ATCM Positive power-flow	$\Phi_1 = \Phi_2 = 0$	$\Phi_1 = D_1 - D_2$ $\Phi_2 = D_3 - D_4$
ATCM Negative power-flow	$\Phi_1 = D_2 - D_1$ $\Phi_2 = D_4 - D_3$	$\Phi_1 = \Phi_2 = 0$

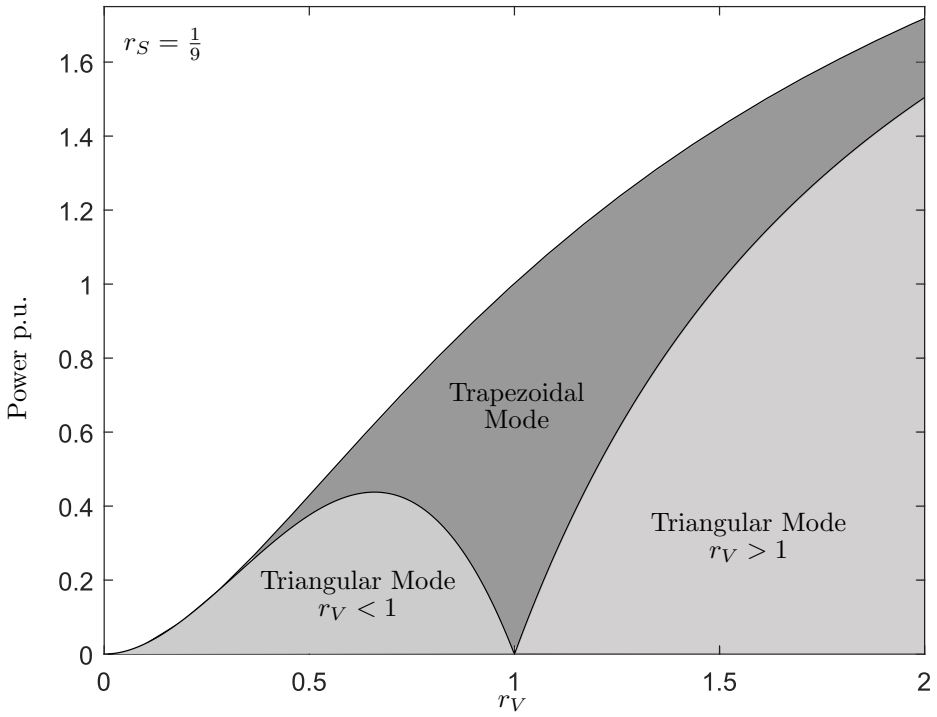


Figure 3.15: *Control map for $r_S = \frac{1}{9}$ in the interval $r_V = (0, 2)$*

According to the observations above, it is possible to create a control map (Fig. 3.15) for a wide r_V range. This map defines three complementary modes: trapezoidal, triangular $r_V < 1$ and triangular $r_V > 1$ if the previous analysis of the power range in terms of r_V is extended to the interval (0,2). This control map allows the optimized operation point $(\Phi_1, \Phi_2, D_1, D_3)$ to be obtained for each power reference P^*_{pu}, using a set of steady-state equations. Details of the control map will be found in next Chapter.

Although the converter is designed to operate at a nominal voltage level and therefore for a fixed r_V parameter, any voltage disturbance in the ports will affect r_V proportionately (3.14). In particular, for a black start operation, this value will be close to zero. Therefore, the previous analysis of the impact of r_V on the power is useful to operate over a wide voltage range at the ports.

Chapter 4

Control scheme

4.1 Introduction

In this Chapter the proposed control scheme for the High step ratio dc-dc MMC is presented. The proposed control strategy enables operation of the converter while providing a wide-range of output voltage control at the LV dc port, several commutations in the semiconductor devices with ZCS, and good steady state and transient regulation of the capacitor voltages.
In order to analyse a variable output voltage operation, the LV output port it assumed to have a capacitive filter and a resistive load, as is shown in Fig. 4.1(a). An overview of the overall control structure is illustrated in Fig. 4.1(b), considering a hierarchical structure of the following sub-control loops:

1. Output voltage loop
2. Trapezoidal current optimiser
3. Single-cell balancing and stack modulation
4. H-bridge modulation

Two different modulations are proposed for the cell stack: (i) time-controlled phase-shift modulation and (ii) time-controlled sorting modulation. The first proposal generates an equal utilization of the cells in an extended time-window

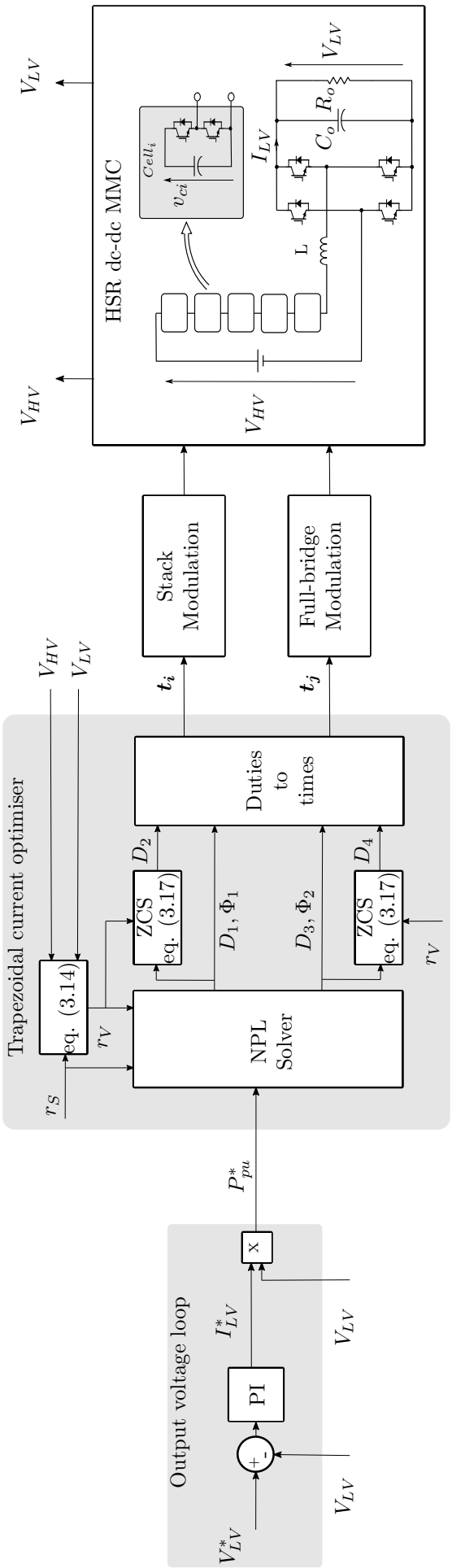


Figure 4.1: *HSR dc-dc MMC proposed control scheme to regulate output voltage with the LV port as load.*

based on a phase-shift strategy, achieving natural voltage balance in the capacitors.

The second stack modulation proposal performs an active control of the single-cell capacitor balancing thanks to the incorporation of capacitor voltage feedback and a sorting modulator.

The details and considerations for each sub-control loop are discussed in the following subsections.

4.2 Output voltage loop

To regulate the voltage at the LV dc port, an output voltage control loop is implemented based on a PI controller. When a capacitive filter is connected at the port (see Fig. 4.1 (a)), the open loop transfer function $G_{LV}(s)$ which describes the output voltage behavior in terms of the current at LV dc port I_{LV} is

$$G_{LV}(s) = \frac{V_{LV}(s)}{I_{LV}(s)} = \frac{R_o}{1 + R_o \cdot C_o \cdot s}. \tag{4.1}$$

This linearty transfer function between the current I_{LV} and the output voltage V_{LV} given by the output voltage filter facilitates the incorporation of a PI controller, which regulates the output voltage through the dc current I_{LV}. Since the modulator is implemented as a power modulator, the current reference is adapted to a power reference P^*_{LV} by multiplying it by the output voltage V_{LV}.

4.3 Trapezoidal current optimiser

The trapezoidal current optimiser is the core of the proposed control scheme where the trapezoidal current mode is implemented. It delivers the transition times $\boldsymbol{t_i} = (t_1, t_3, t_5, t_7)$ required for the stack modulation, and the times $\boldsymbol{t_j} = (t_2, t_4, t_6, t_8)$ corresponding to the H-bridge operation, in order to modulate the power references P^*_{HV} and P^*_{LV} under the trapezoidal current mode. Since

the triangular current mode is a particular case of the trapezoidal model, this approach includes both current modulations.

As is illustrated in Fig. 4.1, the power modulator is composed of three main blocks in cascade: (i) NLP solver, (ii) Zero-current switching and (iii) Duties to times, which are described below.

4.3.1 NLP Solver

The power reference generated by the external control-loops define the NLP problem to minimise the rms current of the trapezoidal wave-form described in (3.41), which is solved by the NLP solver block. Since the power modeling employs the parameters r_V and r_S, r_V is calculated using equation (3.14) with the measured values of the voltages at both ports V_{HV} and V_{LV}, whilst r_S is determined by the selected stack modulation (3.11).

An online implementation of the NLP solver would be unable to solve the optimisation problem within the time-step of the controller if the converter is working at medium or high frequency, therefore, an offline implementation or a simplified analytic solver is recommended. Thus, the NLP solver block could be implemented as a look-up table that stores the results of the optimisation problem previously solved offline or as a control map which select the operating mode with its corresponding set of equations at steady-state (Table 4.1). In this thesis, the latter one is implemented.

The control map method provides an approximation of the NLP solution using a control map and a set of steady-state equations. The control map defines three complementary operating modes: trapezoidal, triangular $rV < 1$ and triangular $rV > 1$. The boundaries of these zones which define each operating mode are identified as $P^{max}_{\sqcap}$, $P^{max}_{\triangle\, r_V<1}$, $P^{max}_{\triangle\, r_V>1}$, defining the triangular zone $rV < 1$ as the area below the curve $P^{max}_{\triangle\, r_V<1}$, the triangular zone $rV > 1$ as the area below the curve $P^{max}_{\triangle\, r_V>1}$, and the trapezoidal zone as the area below the function $P^{max}_{\sqcap}$ and over the triangular boundary curves, as is shown in Fig.

4.2(a).

The per-unit expressions for the upper boundaries of the triangular modes are found in (4.2), evaluating (3.32) and (3.25) in the upper limit of D_2 and D_1 respectively.

$$\begin{aligned} P^{max}_{\triangle\, r_V<1} &= \frac{12r_V^2 \cdot (1-r_V)}{(r_S r_V+1)(1+\sqrt{\frac{1-r_S r_V}{1+r_S r_V}})^2} \\ P^{max}_{\triangle\, r_V>1} &= \frac{12 \cdot (r_V-1)}{r_V(r_S+1)(1+\sqrt{\frac{1-r_S}{1+r_S}})^2} \end{aligned} \tag{4.2}$$

The upper limit of the trapezoidal mode can be also found as a function of r_V, analysing the limits where the results of the NLP problem delivers feasible solutions. Thus, for the case $r_S = \frac{1}{4}$, this boundary is fitted by the polynomial function (4.3).

$$P^{max}_{\square} = 0.063 \cdot r_V^6 - 0.47 \cdot r_V^5 + 1.57 \cdot r_V^4 - 3 \cdot r_V^3 + 2.78 \cdot r_V^2 + 0.05 \cdot r_V. \tag{4.3}$$

Zone identification and selection using the above criteria is made by the block mode selector (see Fig. 4.2(b)), whilst the block solver calculates the output duty cycles considering these three different modes and the steady-state equations, which are summarized in Table 4.1.

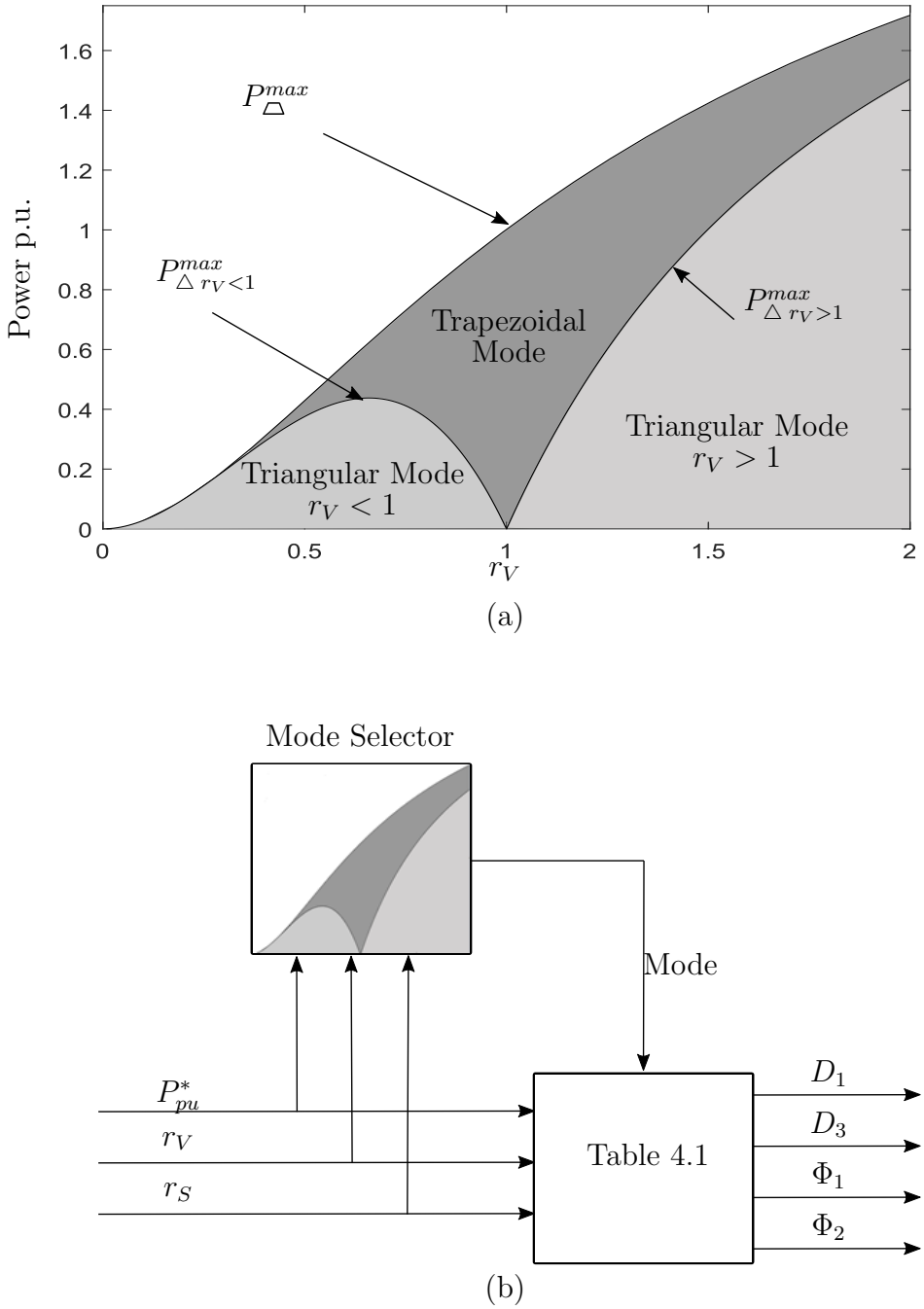


Figure 4.2: *Control map implementation: (a) Operating zones and (b) Control blocks.*

Table 4.1: Optimized Current Modes at steady-state

	Trapezoidal	Triangular	
		$r_V < 1$	$r_V > 1$
Minimum $(i_L^{rms})^2$	$\Phi_2 = \Phi_1$ $D_1 + D_3 = r_V(1 - \Phi_1 - \Phi_2)$	$\Phi_1 = \Phi_2 = 0$	$\Phi_1 = D_1 - D_2$ $\Phi_2 = D_3 - D_4$
Power balance	$D_3 = \frac{1-\sigma_1}{2} - \frac{r_S \cdot P_{pu}}{12 \cdot \sigma_1}$ [1]	$D_3 = D_1\sqrt{\frac{1 - r_S \cdot r_V}{1 + r_S \cdot r_V}}$	$D_3 = D_1\sqrt{\frac{1 - r_S}{1 + r_S}}$
Power P_{pu}	$\pm\frac{6 \cdot \sigma_1 \cdot (\sigma_1 - \sigma_2)}{r_S^2 \cdot (1 - r_V)}$ [1] with $r_V \neq 1$ $\pm 12 \cdot \Phi_1 \cdot (1 - 3\Phi_1)$ with $r_V = 1$	$\pm\frac{12 \cdot r_V^2 \cdot (1 - r_V)}{(1 + r_S \cdot r_V)} D_2^2$	$\pm\frac{12 \cdot (r_V - 1)}{r_V \cdot (r_S + 1)} D_1^2$

[1] $\sigma_1 = 2\Phi_1 r_V + 1 - r_V, \quad \sigma_2 = (\sigma_1^2(1 - r_S^2 r_V^2) + 4\Phi_1^2 r_S^2 r_V)^{0.5}$.

Thus, the NLP solver block delivers the optimal solution $(\Phi_1, \Phi_2, D_1, D_3)$ which generates the minimum rms inductor current with good precision.

4.3.2 ZCS blocks

The current modeling using the trapezoidal and triangular current mode relies on a ZCS operation, therefore, the ZCS blocks regulates the duties (D_2, D_4) to achieve this. These duties are calculated from (3.17), using the NLP solver output $(\Phi_1, \Phi_2, D_1, D_3)$. This open-loop approach provides a good approximation to achieve ZCS, but it highly dependent on the parameter r_V and the inductance L.

Thus, any significant error on the estimation of these parameters leads to a hard-switching operation. To solve this, the ZCS block could be implemented as a closed-loop with current feed-back, however, this would require a high-resolution measurement of the current and a controller with smaller sampling times than the rest of the control scheme. Hence, its practical implementation is limited to the use of high-performance controllers, such as field-programmable gate arrays (FPGAs) or SoC FPGAs. Therefore, the open-loop alternative is chosen as the ZCS block due to its simplicity and ease of implementation on a standard CPU controller.

4.3.3 Duties to times block

Finally, the Duties to times block wraps the duty-cycles $(\Phi_1, \Phi_2, D_1, D_2, D_3, D_4)$ defined by the NPL solver and ZCS blocks, into two time vectors: $\boldsymbol{t_i} = (t_1, t_3, t_5, t_7)$ and $\boldsymbol{t_j} = (t_2, t_4, t_6, t_8)$.

The relation between the duty-cycles and the times can easily derived as (4.4) using Fig. 3.10. The times t_1 and t_5 can be freely adjusted as long as the positive and negative semi-cycles do not overlap and hey fit in the time-window T_s, which is achieved if the restrictions $t_4 \leq t_5$ and $t_8 \leq T_s$ are kept.

$$
\begin{aligned}
t_2 &= t_1 + \Phi_1 T_s \\
t_3 &= t_1 + D_1 T_s \\
t_4 &= t_2 + D_2 T_s \\
t_6 &= t_5 + \Phi_2 T_s \\
t_7 &= t_5 + D_3 T_s \\
t_8 &= t_6 + D_4 T_s
\end{aligned}
\tag{4.4}
$$

Thus, the times $\boldsymbol{t_i}$ associated with the voltage v_{L1} feed the half-bridge stack modulation block, whilst the times $\boldsymbol{t_j}$ corresponding to the voltage v_{L2} are used by the modulation block of the H-bridge.

4.4 Single-cell balancing and stack modulation

For proper operation of the converter, the voltages of the stack capacitors must be maintained constant and equal. Thus, there are two types of voltage regulation that must be achieved: (i) capacitor mean voltage regulation and (ii) equalized voltage among capacitors.

The capacitor mean voltage balance is achieved thanks to an intrinsic characteristic of the topology. Due to the the series connection of the stack in the topology, a natural negative capacitor voltage feedback is generated i.e when the capacitor mean voltage drops, the voltage at the ac-link v_{L1} increases following (3.2). Thus, the current flowing through the capacitors increases, charging the capacitor voltages. A similar behaviour is observable when the capacitor mean voltage rises, decreasing the voltage at the ac-link and consequently discharging the capacitors. Thus, the voltage balance is naturally achieved at steady state if the power reference P^*_{stack} is set to zero. This topology feature is exploited in [37–41], completely avoiding a dedicated control-loop.

Despite the natural regulation of capacitor mean voltage, the individual capaci-

tor voltages $\boldsymbol{v_c}$ could be unbalanced due to parameter differences, diverse initial voltage values or unequal utilization. Therefore, the stack modulation should incorporate a voltage balance strategy among the cells to avoid problems in the current modulation created by these unbalances. Also, the modulation in the half-bridge stack requires generation of a three-level voltage v_{L1} precisely controlled by the transitions times $\boldsymbol{t_i} = (t_1, t_3, t_5, t_7)$. Hence, traditional PWM methods are discarded because of lack of control of the transition times.

In the following subsections two stack modulations are presented to address this issue: (i) time-controlled phase-shift modulation and (ii) time-controlled sorting modulation. Also, the practical implementation using finite state machines (FSMs) is detailed in C.1.

4.4.1 Time-controlled phase-shift stack modulation

The first modulation proposed relies on a phase-shift strategy, where the cells are modulated with the same waveform using a phase-shift to reduce the resultant switching-frequency and to achieve balanced use of the cells. For this, the time modulation presented in [48] is used as base and modified to an asymmetric operation. Details of its practical implementation are included in Appendix C.1.1.

For the case $r_S = \frac{1}{N-1}$, the voltages v_i of the half-bridge cells are considered as a periodic signal of period $N \cdot T_s$ and are defined by transition times and the parameter j. The commutation state S_1^j of the first cell is described by (4.5), and this can be used for the derivation for the rest of cells by including a phase-shift of T_s. The parameter j defines a set of different cell wave-forms in the half-bridge cell that create the same voltage in the stack.

$$S_{HB_1}^j(t) = \begin{cases} 0 & if \text{ if } t \in [t_1, t_5] \cup [t_7 + j \cdot T_s, t_3 + (j+1)T_s] \\ 1 & else \end{cases} \tag{4.5}$$

The modulation wave-forms of each cell are illustrated in Fig. 4.3(a)(b) for

$j = 0$ and $j = 2$ respectively, taking $N = 5$ cells and a stack voltage ratio $r_S = \frac{1}{4}$ as an example. As the voltage in the stack v_{stack} is the sum of all cell voltages, v_{stack} is identical for all $j \in \mathbb{N} \mid (0 \leq j < N-1)$. Thus, the stack voltage v_{stack} is a three-level voltage of amplitude V_C, period T_s and controlled by its transition times, as is required in the high step voltage ratio operation detailed in Section 3.3. Furthermore, this stack modulation scheme produces an equal utilization of the cells in period $N \cdot T_s$, thus, this modulation provides a natural voltage balance among the capacitor cells at steady-state even if the capacitors have different capacitance values [53]. The charge and discharge process of the capacitor v_{c1} for positive power-flow can be observed in Fig. 4.3 with the coloured arrows, noticing that the ratio $\frac{1-r_S}{1+r_S}$ found for the voltage balance condition at steady-state under triangular current mode (3.24) can be deduced as the number of charging states (blue arrows) over the number of discharging states (red arrows) in the cell while it is inserted ($v_1 = V_C$).
Even though the v_{stack} is identical for all $j \in \mathbb{N} \mid (0 \leq j < N-1)$, the selection of the parameter j has an important impact in the capacitor voltage ripple. If $j = N$-1 or $j = 0$ (Fig. 4.3 (a)), the commutations in the cell are concentrated in a small time-window. This produces several consecutive discharging states in the capacitor cell, which generates higher voltage ripple than a distributed operation ($j = 2$) where the consecutive discharging states are minimised. To illustrate this, the voltage ripple is derived below for the cases $j = 0$ and $j = 2$.

The voltage behavior in each cell capacitor is determined by (4.6), where the current flowing through it is defined by the inductor current i_L and the cell state S_{HB_i}.

$$C_i \frac{dv_{ci}}{dt} = i_L \cdot S_{HB_i} \tag{4.6}$$

Taking the first cell of the phase-shift modulation with $j = 0$ (Fig. 4.3 (a)), the minimum capacitor voltage $v_{c1_{j=0}}^{pk-}$ is found in (4.7), integrating (4.6) up to

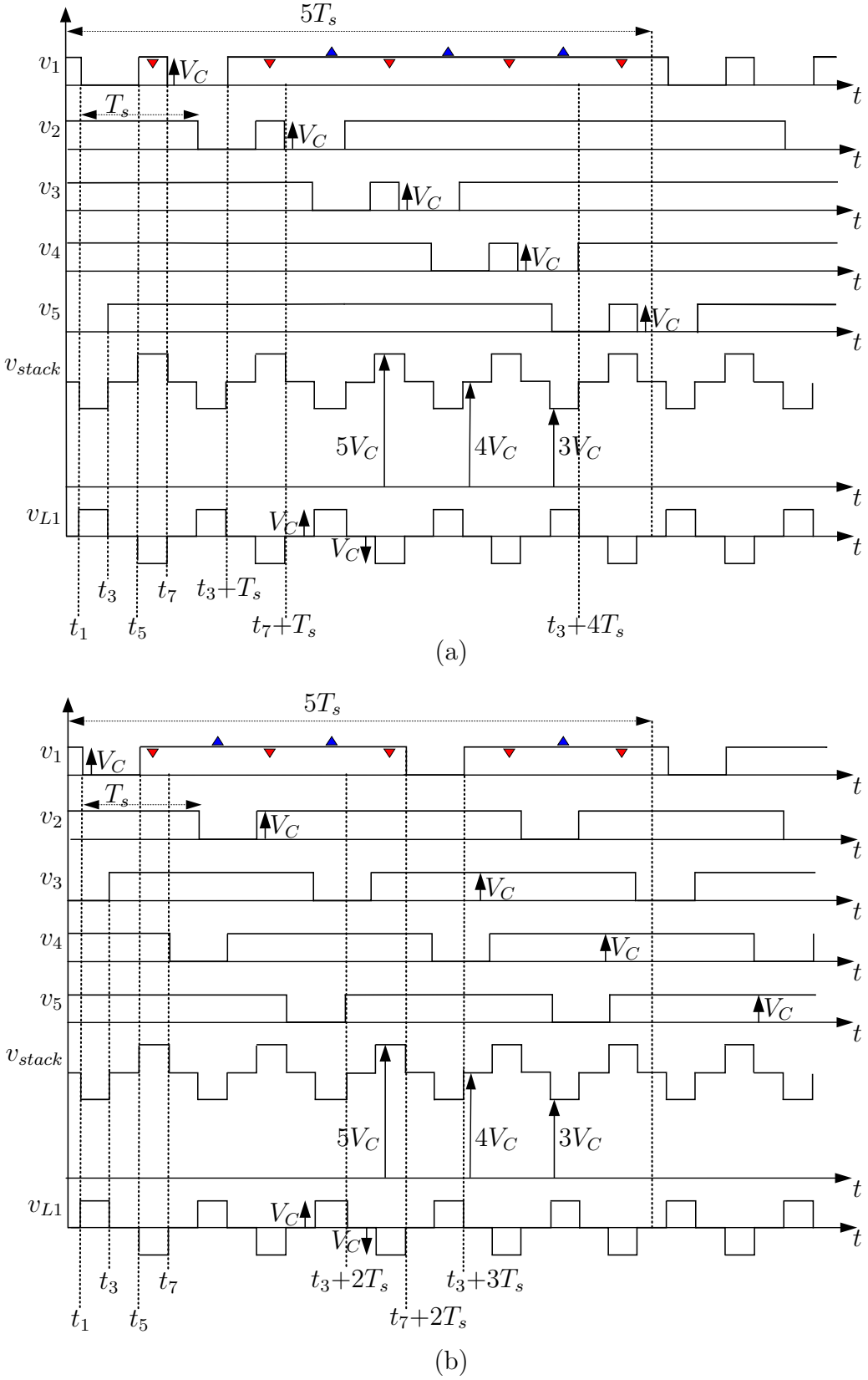


Figure 4.3: *Modulation wave-forms in the stack of five cells in the period $5T_s$: (a) case $j = 0$ and (b) case $j = 2$*

the end of the two consecutive discharging states at the time t_7+T_s.

$$v_{c1_{j=0}}^{pk-} = v_{c1}(t_0) + \frac{1}{C_1} \int_{t_0}^{t_7+T_s} i_L \cdot S_{_{HB_1}} dt \tag{4.7}$$

In the same way, the maximum capacitor voltage $v_{c1_{j=0}}^{pk+}$ is found in (4.8), integrating (4.6) until the end of the third charging state at time t_3+(N-1) $\cdot$ T_s.

$$v_{c1_{j=0}}^{pk+} = v_{c1}(t_0) + \frac{1}{C_1} \int_{t_0}^{t_3+(N-1)\cdot T_s} i_L \cdot S_{_{HB_1}} dt \tag{4.8}$$

Therefore, the peak-to-peak voltage ripple $v_{c1_{j=0}}^{pk}$ in the cell capacitor is expressed in (4.9) as the difference between the extreme values $v_{c1_{j=0}}^{pk+}$ and $v_{c1_{j=0}}^{pk-}$. Furthermore, this peak-to-peak voltage can be expressed in terms of the areas defined in (3.35) and (3.38), if the trapezoidal current modulation is used. For the case of triangular current mode, these areas can be simplified according to (3.29).

$$v_{c1_{j=0}}^{pk} = v_{c1_{j=0}}^{pk+} - v_{c1_{j=0}}^{pk-} = \frac{1}{C_1} \int_{t_7+T_s}^{t_3+4\cdot T_s} i_L \cdot S_{_{HB_1}} dt = \frac{3(A_{\sqsupset 1} - A_{\triangle 1}) + 2(A_{\sqsupset 2} - A_{\triangle 2})}{C_1} \tag{4.9}$$

A similar process is performed to find the peak-to-peak voltage ripple $v_{c1_{j=2}}^{pk}$ of the first cell under this phase-shift modulation with $j = 2$ (Fig. 4.3 (b)). In this case the minimum capacitor voltage occurs at time t_7, whilst the maximum voltage occurs at the end of the second charging state at time t_3+$2T_s$.
Therefore, the peak-to-peak voltage ripple $v_{c1_{j=2}}^{pk}$ in the cell capacitor is found in (4.10).

$$v_{c1_{j=2}}^{pk} = \frac{1}{C_1} \int_{t_7}^{t_3+2\cdot T_s} i_L \cdot S_{_{HB_1}} dt = \frac{2(A_{\sqsupset 1} - A_{\triangle 1}) + (A_{\sqsupset 2} - A_{\triangle 2})}{C_1} \tag{4.10}$$

From (4.10) and (4.9), it is noticeable that a distributed modulation of the commutation states over the period $N \cdot T_s$ (case $j = 2$) produces a lower

voltage ripple in the capacitor than the concentrated case ($j = 0$). Therefore, it is advantageous to choose a modulation with j as close to $0.5N$ as possible. In this way, the switching states of each cell are distributed over the whole period $N \cdot T_s$, resulting in minimised voltage ripple. Furthermore, (4.10) allows the cell capacitance value to be chosen for a desired voltage ripple.

The main drawback of this phase-shift modulation is its lack of a feedback loop. This means that the balance is only achieved after a long period of time if the initial voltages are very different or under significant voltage disturbances. If the imbalance of the capacitor voltages is significant, it leads to problems in the current modulation which relies on balanced operation. Therefore, it is desired to have a modulation strategy which considers the individual capacitor voltages to reduce the convergence time.

4.4.2 Time-controlled sorting stack modulation

In order to provide capacitor voltage feedback into the phase-shift the modulation presented above, an alternative stack modulation is implemented based on a sorting modulation [215]. The sorting algorithm performs voltage balance among the cells because the cells with the lowest capacitor voltages are periodically charged, whilst the cells with the highest voltages are discharged. To illustrate the sorting operation in the stack and the capacitor voltage charging state in each cell, Fig. 4.4 shows the wave-forms for the period T_s with $N = 5$ cells and a stack voltage ratio $r_S = \frac{1}{4}$ as an example. At the bottom of this figure, the inductor current i_L wave-form is included assuming trapezoidal current mode. It should be noted that this current is the same current through the cells, and consequently, the current that flows through its capacitor when the cell is inserted.

As a modulation example, cells one (v_1), two (v_2) and three (v_3) are fully inserted for the whole period T_s, whilst cells four (v_4) and five (v_5) are used to modulate the three-level voltage. When the power-flow is positive (Fig.

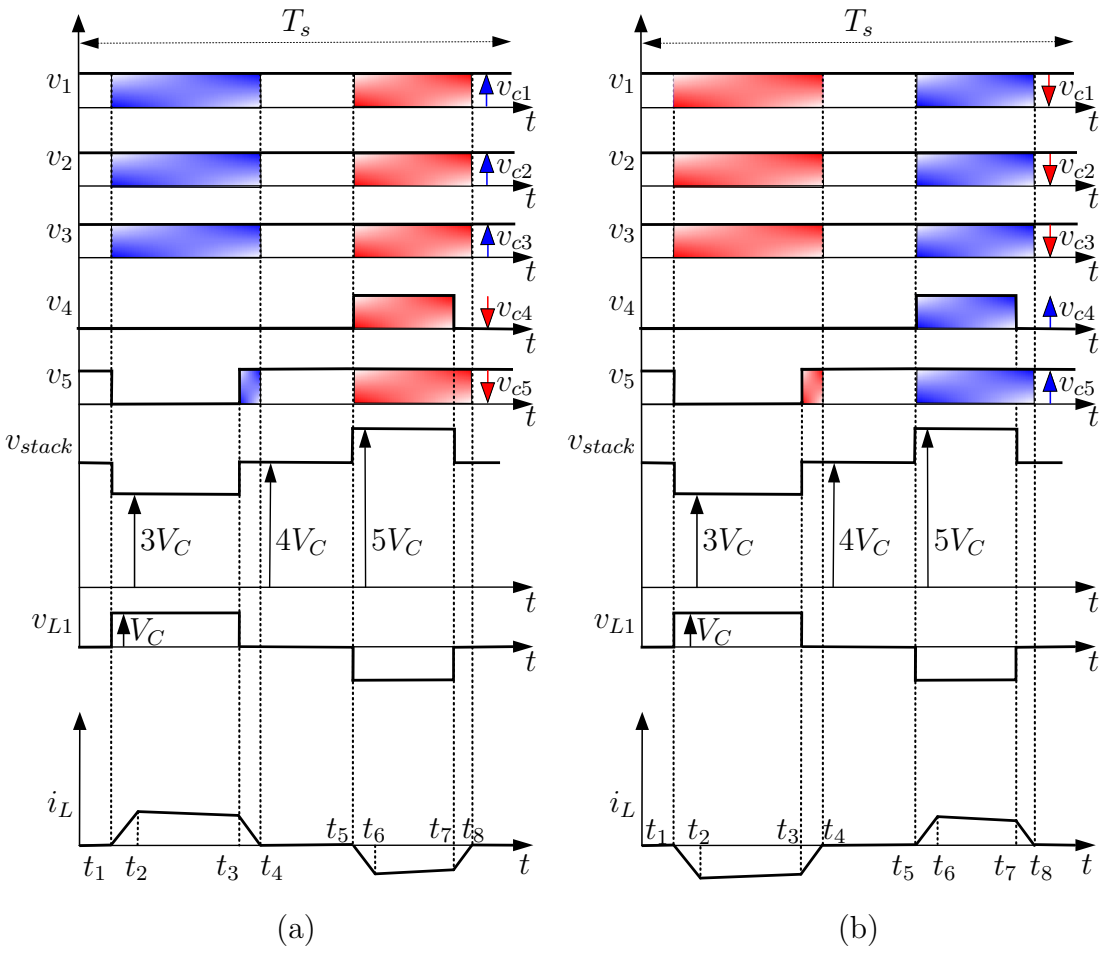


Figure 4.4: *Wave-forms in the stack in the period T_s: (a) Positive power-flow and (b) Negative power-flow.*

4.4 (a)), the capacitors of the fully inserted cells (v_{c1}, v_{c2} and v_{c3}) increase their charge level at the end of the period T_s (blue arrow) because the time-window where the capacitor is charging (blue zone) predominates over the discharging time-window (red zone). This predominance of the charging over the discharging state is assured because the mean value over the period T_s of the current through these capacitors is positive when the power-flow is from the HV to LV port. On the other hand, the capacitors of the cells four and five are in discharging state (red arrow) at the end of the period since the mean value of the current is negative while they are inserted. Hence, in order to balance the capacitor voltages among the cells, the capacitor voltages can be periodically measured to identify the two most charged cells to be used as modulating cells (and thus reduce their capacitor voltage), whilst the remaining cells are

selected as fully inserted cells to increase their voltage.

An analogous behavior occurs when the power-flow is negative, as is shown in Fig. 4.4 (b). In this case, the capacitors of the fully inserted cells are in a discharging state (v_{c1}, v_{c2} and v_{c3}), whilst the modulating cells (v_{c4} and v_{c5}) are in charging state because the inversion of the current waveform. Therefore, a reduction in the capacitor voltage imbalance among the cells is achieved when the two less charged cells are used as modulating cells, whilst the rest are fully inserted to increase their voltage.

The above charge analysis allows a sorting algorithm to be implemented (see Fig. 4.5) to sort in ascending order (if the power-flow is positive) or descending order (if the power-flow is negative) the capacitor voltage measurements created in the list $\boldsymbol{L}[\boldsymbol{N}]$, and thus, to select the cells used as modulating and fully inserted cells. After this selection, the gate signal are generated using finite state machines (FSMs), which are described in Appendix C.1.2.

The capacitor voltage ripple with this modulation depends on the frequency of the capacitor voltage sampling and sort algorithm, which can be executed after a defined number of switching cycles or triggered if any cell exceeds the desired voltage ripple. The latter method provides a way of controlling the capacitor voltage ripple.

4.5 H-bridge modulation

The H-bridge modulation block generates the gate signals for the full-bridge connected at the LVdc port. The modulation is defined by the times $\boldsymbol{t_j} = (t_2, t_4, t_6, t_8)$ associated with the voltage v_{L2}, and it is implemented using a finite state machine (FSM) to provide high precision on the commutation times. Details of the FSM implementation can be found in Appendix C.1.3.

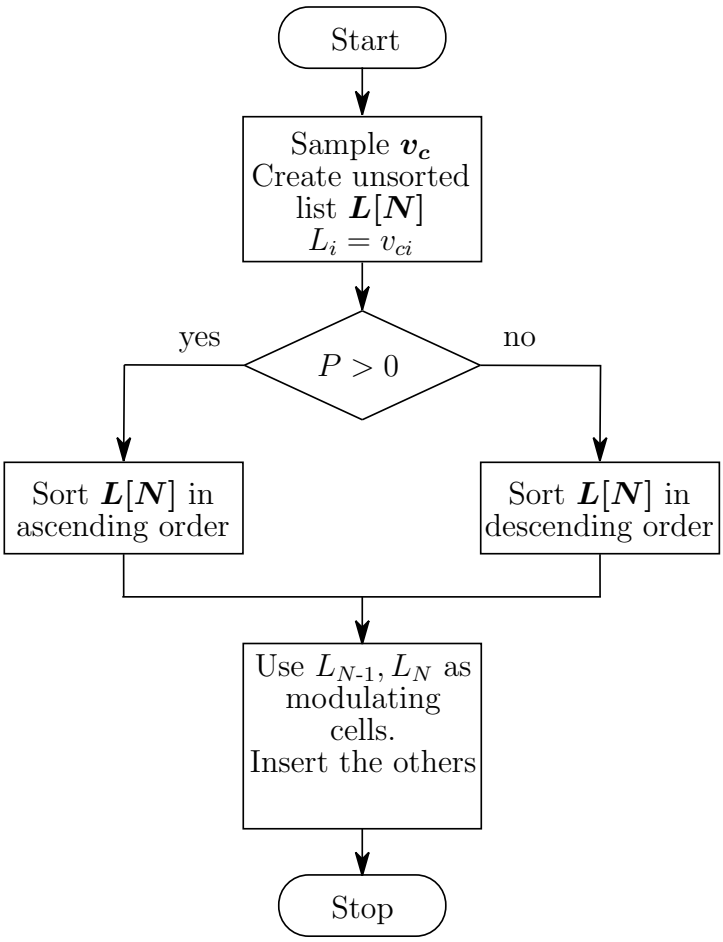


Figure 4.5: *Sorting algorithm*

Chapter 5

Full-scale simulations

5.1 Introduction

The high step ratio MMC dc-dc converter has been simulated in PLECS to verify the theoretical analysis presented in previous chapters. The parameters used for all simulations are detailed in Table 5.1, considering a 1 MW converter that interconnects 10 kV and 1.1 kV networks. The design process of the simulated converter working with $r_V \approx 1$, can be summarised as:

1. To define the number of cells and operating voltage in the cells using 3.11, and adjusting the nominal stack voltage ratio r_S as close as possible to the voltage step ratio needed ($\frac{V_{LV}}{V_{HV}}$). Thus, the converter will operate with $r_V \approx 1$.

2. To define the switching frequency f_s and the inductance L in order to provide enough power transfer at nominal operation. As $r_V \approx 1$, $P_{base} = \frac{V_{HV}^2 \cdot r_S^2}{12 f_s L}$ can be used as an approximation of the maximum power transfer.

3. To calculate the capacitance of the cells capacitor using 4.6 and the voltage ripple requirement.

Table 5.1: Parameters of the Simulated System

Description	Parameter	Value
Power rate	P_{base}	1 MW
HV side Voltage	V_{HV}	10 kV
LV side Voltage	V_{LV}	1.1 kV
Mean capacitor cell voltages	V_C	1.111 kV
Number of cells	N	10
Nominal stack voltage ratio	r_S	1/9
Nominal ac-link voltage ratio	r_V	≈ 1
Inductor inductance	L	102 μH
Capacitance of cell capacitors	C_i	50 mF $\pm$ 20%
Output capacitor	C_o	10 mF
Output load	R_o	1.3 Ω
Switching frequency	f_s	1 kHz
IGBTs ABB 5SNA3600E17000	V / I	1.7 kV / 3.6 kA

The following scenarios have been simulated to validate the modulation and control strategies for a full-scale converter:

1. Simulation at steady-state.

2. Simulation of output voltage step response.

The steady-state simulation predicts the voltage and current waveforms in the devices and passive components, such as the ac-link inductor and cell capacitors. Also, a power loss analysis is performed at different power levels. Finally, a simulation of the output voltage step response with a fixed load allows the evaluation of the dynamic behaviour of the converter under different load voltage levels.

Different capacitance values ($\pm$ 20% margin) are considered for each capacitor in the cells to evaluate the voltage balancing under realistic conditions. The stack modulation is set to the highest stack voltage ratio possible for ten cells ($r_S = \frac{1}{9}$) and the nominal ac-link voltage ratio is set close to 1.

The modulation and control strategies proposed in Chapters 3 and 4 were implemented using the PLECS library.

5.2 Simulation at steady-state

The first set of simulation results considers the steady-state operation of the proposed full-scale high step ratio MMC dc-dc converter at nominal power.

Fig. 5.1 shows waveforms for the operation of the converter in a complete phase-shift switching cycle, i.e. a period of $10 \cdot T_s$, where ten is the number of cells that form the stack. The output cell voltages follow the same switching patter using the phase-shift modulation, as is illustrated in Fig. 5.1 (a). The resulting three-level stack voltage (Fig. 5.1 (b)) is the sum of the ten cell voltages, and it has an amplitude of V_{LV} and a voltage offset of V_{HV} in order to produce the required waveform for v_{L1}. Thus, it achieves the highest stack voltage ratio possible for ten cells ($r_S = \frac{1}{9}$), generating a three-level low voltage at the ac-link (v_{L1} in Fig 5.1 (d)).

The voltages of each cell capacitor in the modulation cycle are shown in Fig. 5.1 (c). The mean voltage value in the capacitors remains constant at 1.111 kV, verifying the correct power balance of the converter and cells even when different capacitance values are used for the capacitors of each cell.

Since the amplitude of v_{L1} and v_{L2} are equivalent ($r_V \approx 1$), the operation generates a perfect trapezoidal current waveform at the ac-link, as is shown in Fig. 5.1 (d).

Fig. 5.2 shows the detailed waveforms for the half-bridge cell and the full-bridge. Since the series connection of the cells stack with the ac-link, the current flowing through the cells is identical to the inductor current i_L. Voltage and cell current for one cell are shown in Fig. 5.2 (a), verifying the reduction of the effective switching frequency of the cell. Furthermore, half of the cell transitions are performed under soft-switching conditions, whilst the other half hard switch.

The charge and discharge process of the cell capacitor voltage v_{c1} can be observed in the zoomed capture Fig. 5.2 (b), where the voltage remains balanced over the switching cycle. The capacitor voltage ripple was designed to be be-

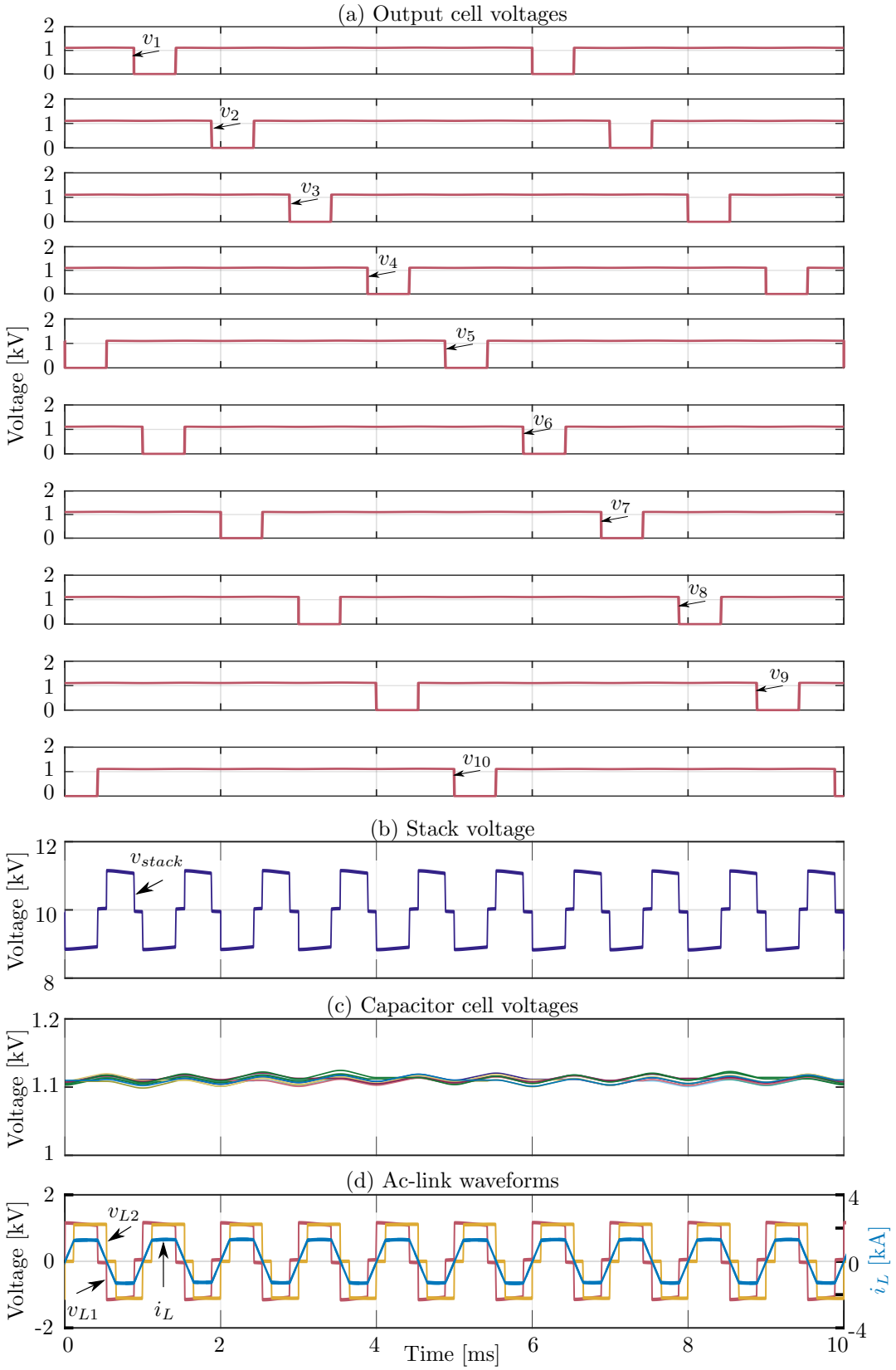


Figure 5.1: *Simulation results at full-scale, typical waveforms: (a) Output cell voltages for ten cells using phase-shift modulation. (b) Resulting total stack voltage. (c) MMC capacitor voltages, ten cells. (d) Ac-link inductor voltages and current.*

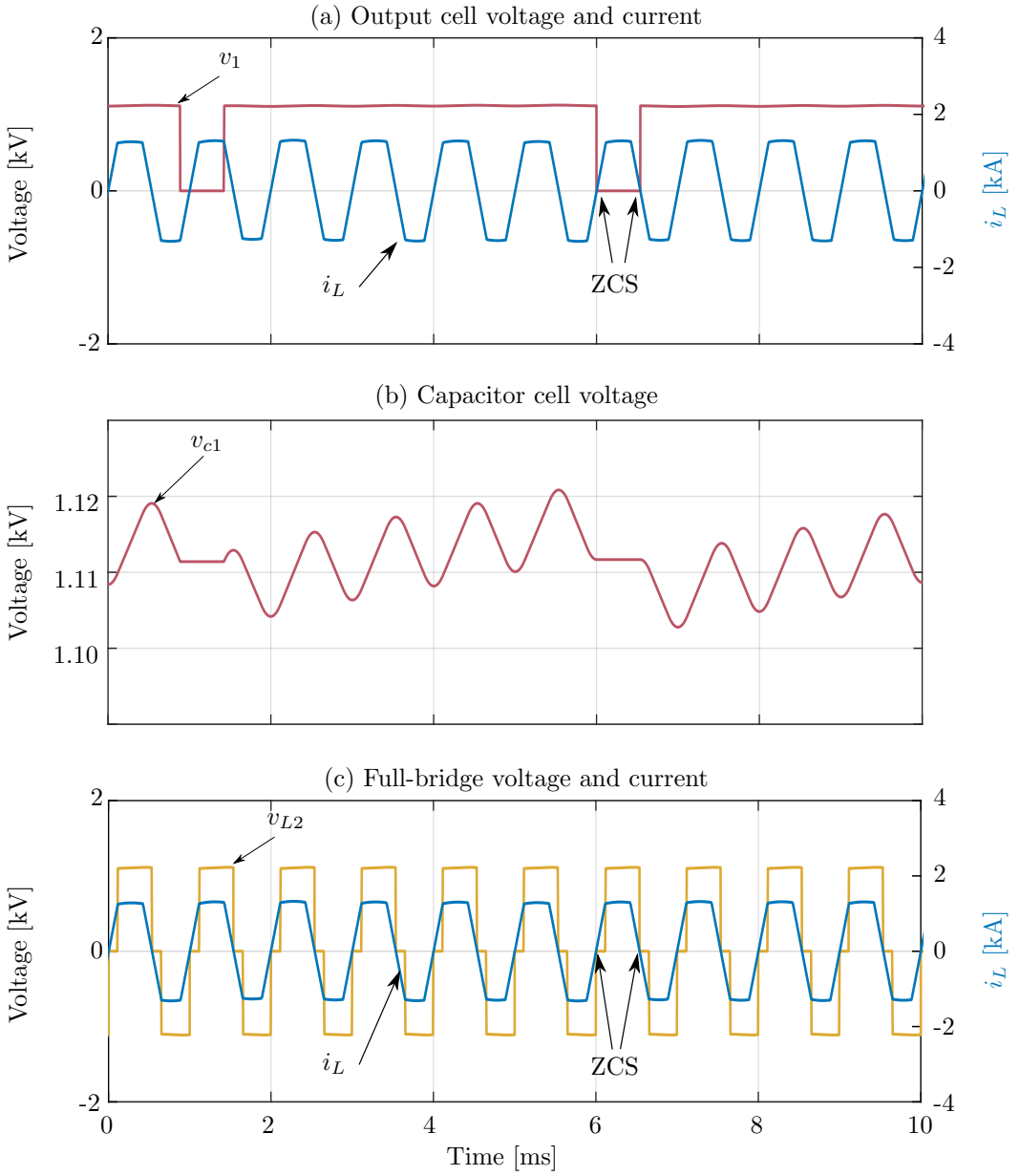


Figure 5.2: *Simulation results at full-scale, typical waveforms:(a) Output cell voltage and current. (b) Zoomed capacitor cell voltage. (c) Output full-bridge voltage and current.*

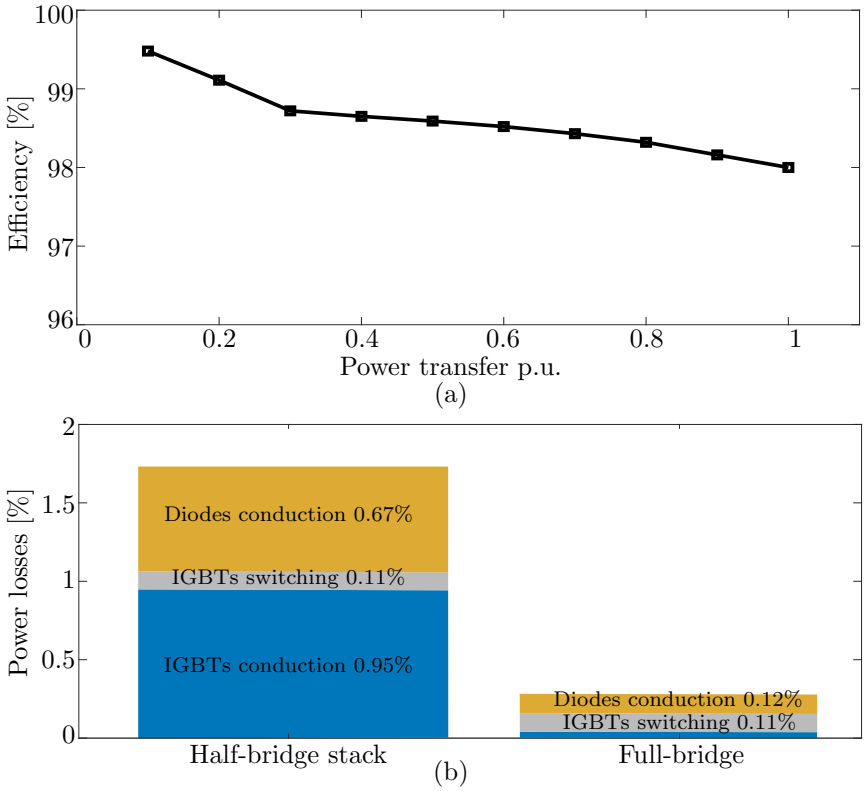


Figure 5.3: *Efficiency of simulated converter with $r_V = 1$. (a) Efficiency curve vs power transfer and (b) Power losses distribution at full power.*

low 3% in order to ensure a square waveform, therefore, the capacitance requirement for the converter is quite high when compared to traditional MMC converters.

Finally, the voltage and current flowing through the full-bridge is illustrated in Fig. 5.2 (c). In the same way as for the half-bridge cell, half of the full-bridge transitions are performed with ZCS, however, the effective switching frequency of the full-bridge is equal to the ac-link frequency f_s.

5.2.1 Power losses

In order to evaluate the impact of the ZCS modulation on the efficiency of the full-scale converter, a PLECS model of the IGBTs was added to estimate the switching and conduction losses in the semiconductor devices.

The overall simulated efficiency of the proposed full-scale converter is at least 98% over the whole power range, as is shown in Fig. 5.3 (a). The following power losses were considered: (i) IGBT conduction losses; (ii) IGBT turn-on

and turn-off switching losses; (iii) diode reverse recovery losses; and (iv) diode conduction losses.

The power losses breakdown at nominal power is illustrated in Fig. 5.3 (b). The power losses in the cell stack represents 86.1% of the total losses and comprise mostly of conduction losses (93%). The power losses in the low voltage full-bridge at full power represent the other 13.9% of total losses and are distributed more evenly between conduction (59%) and switching losses (41%). The dominance of the total conduction losses over total switching losses is due both to soft-switching capability and to the serial connection of the cells in the stack, which multiplies its conduction losses several times. Therefore, the total number of cells could limit the total efficiency in cases where a high number of cells are required.

Finally, at this power and voltage range, the converter is near of the power limit using commercial IGBTs due to the number of cells and its high current rating. For higher current ratings, multiples AC/DC stages [73] or parallel devices would need to be used. However, these alternatives make the design more complex, requiring more control loops in order to achieve balance among parallel converters. They may also require sophisticated control techniques in order to to use devices in parallel [216].

5.3 Simulation of output voltage step response.

The second set of simulation results show the output voltage step response for the proposed full-scale high step ratio MMC dc-dc converter with the LV port as fixed load. This scenario enables the evaluation of the dynamic response of the converter and the proposed modulation under different output voltage levels. Thus, the optimal modulation works on both triangular and trapezoidal current modes.

Fig. 5.4 illustrates the output voltage step response of the converter emulating a black start operation. Fig. 5.4 (a) shows the V_{LV} output voltage from an ini-

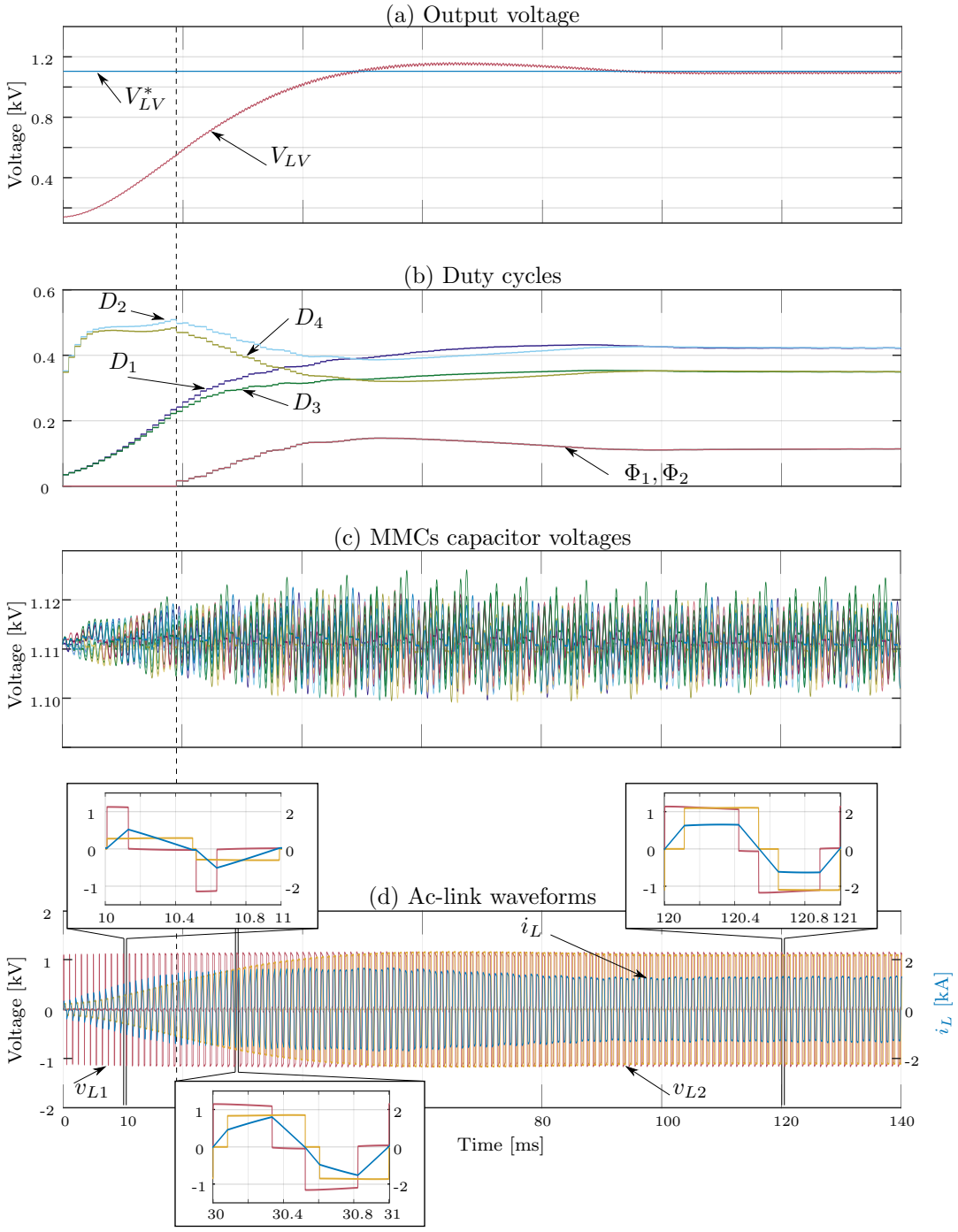


Figure 5.4: *Simulation results at full-scale, output voltage step response: (a) Output voltage. (b) Duty cycles. (c) MMC capacitor voltages. (d) Ac-link inductor waveforms.*

tial low voltage state until reach its reference V_{LV}^{*}. The dynamic behaviour of the waveform duty cycles (Fig. 5.4 (b)) is well damped throughout the simulation period, even during the triangular-trapezoidal transition. This transition occurs when Φ_i starts to become non-zero at 19 [ms] (dashed-line), where the triangular zone corresponds to a low value of r_V, and the trapezoidal zone is apparent for greater values of r_V. At the end of the time-window the duty-cycles D_1, D_2 and D_3, D_4 converge as is predicted by (3.17), since the parameter r_V is close to unity under these conditions. The MMC capacitor voltages remain balanced around the desired mean value (1.111 kV), as is shown in Fig. 5.4 (c). Finally, the ac-link inductor current and voltage waveforms show the current modulation method, which is result of the rms current minimisation problem (Fig. 5.4 (d)). The zoomed waveform captures confirm the soft-switching operation of the converter regardless of the value of the output voltage V_{LV} or whether it has a triangular or trapezoidal current waveform.

Chapter 6

Scaled-down prototype

6.1 Introduction

This Chapter presents the design of the experimental prototype used to validate the theoretical analysis and simulation results.

The first section shows an overview of the lab setup, describing the main components used in the experimental work. The second section details the half-bridge cell and full-bridge cell designs used in the converter. The third section explains the ac-link inductor design process, and the requirements of inductance derived of the theoretical analysis. Finally, the last section describes the control platform where the proposed modulation and control scheme were implemented.

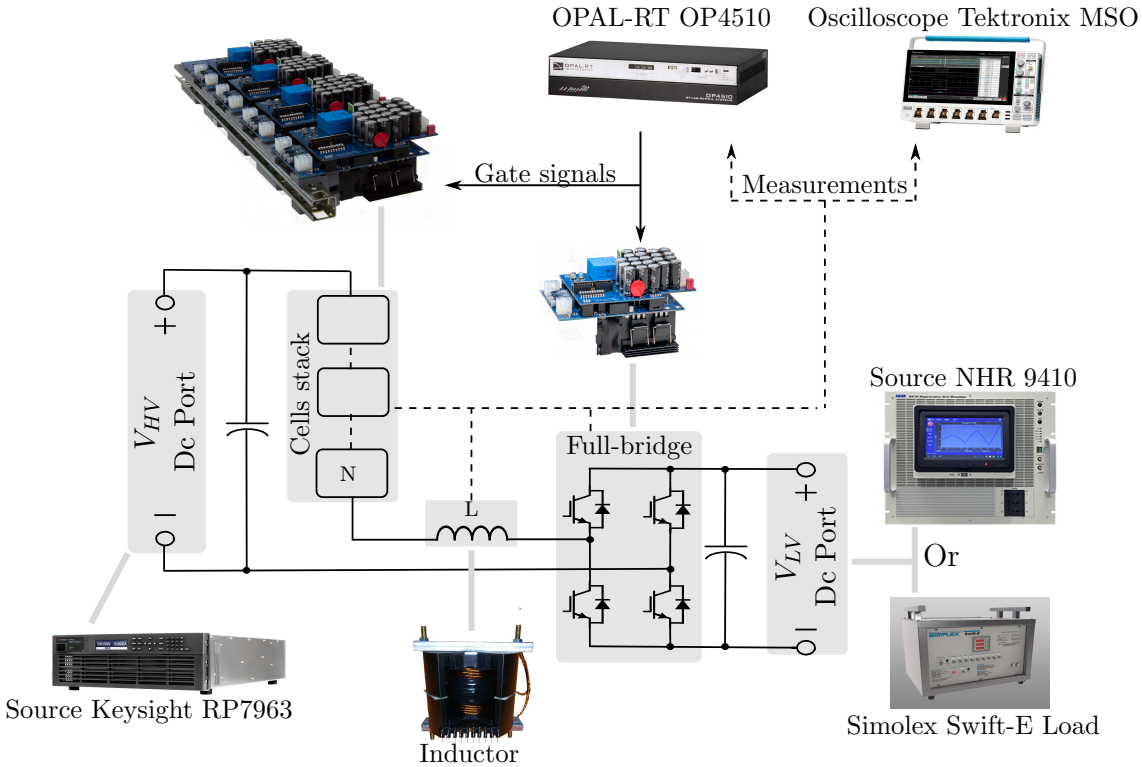
6.2 Overview of the experimental setup

An overview of the experimental setup is shown in 6.1, with the main components labelled including the converter (cells stack, ac-link inductor and full-bridge), power sources, load, control platform and measurement equipment. The main electrical parameters of the scaled-down prototype are listed in Table 6.1.

The converter cells were previously designed for the work in [217] and use using



(a)



(b)

Figure 6.1: *Experimental prototype: (a) Lab setup. (b) Schematic overview.*

Table 6.1: Parameters of Experimental Prototype

Description	Parameter	Value
Nominal power	P_{base}	725 W
HV side nominal voltage	V_{HV}	750 V
LV side nominal voltage	V_{LV}	187.5 V
Mean capacitor cell nominal voltage	V_C	187.5 V
Number of cells	N	5
Stack voltage ratio	r_S	1/4
Nominal ac-link voltage ratio	r_V	1
Capacitance of cell capacitors	C_i	987 μF
Inductor inductance	L	811 μH
Output capacitance	C_o	987 μF
Output load	R_o	50-100 Ω
Switching frequency	f_s	5 kHz
MOSFETs Infineon IPW65R041CFD	V / I	650 V / 80 A
Output voltage PI controller	K_p / K_i	0.0698 / 3.8965

MOSFETs 650V-15A MOSFETs. More details about the cells are provided in subsection 6.3.

The ac-link inductor was realised using a ferrite core and its detailed design procedure is included in subsection 6.4.

A DC Keysight RP7963 regenerative power source (950V, 20A, 10kW) is used as high-voltage dc port, enabling a bidirecctional power flow operation. This power supply can also be controlled and monitored remotely, allowing transients to be programmed to test the prototype converter.

For low-voltage dc port, two connections are considered: (a) a Regenerative Grid Simulator NHR 9410-4 (200V,30A,4kW) and (b) a Simolex Swift-E 10KW Resistive load bank. The first enables a test platform for a bidirectional power-flow to be realised, while the second is used to validate the controlled output voltage operation with different loads.

An OPAL-RT OP4510 system was used as the control platform for the prototype converter. This is based on a Intel Xeon E3 v5 CPU and a Kintex-7 FPGA. The control platform is used to implement the control scheme develped in Chapter 4 using Matlab Simulink. It can also be sued to sample and record

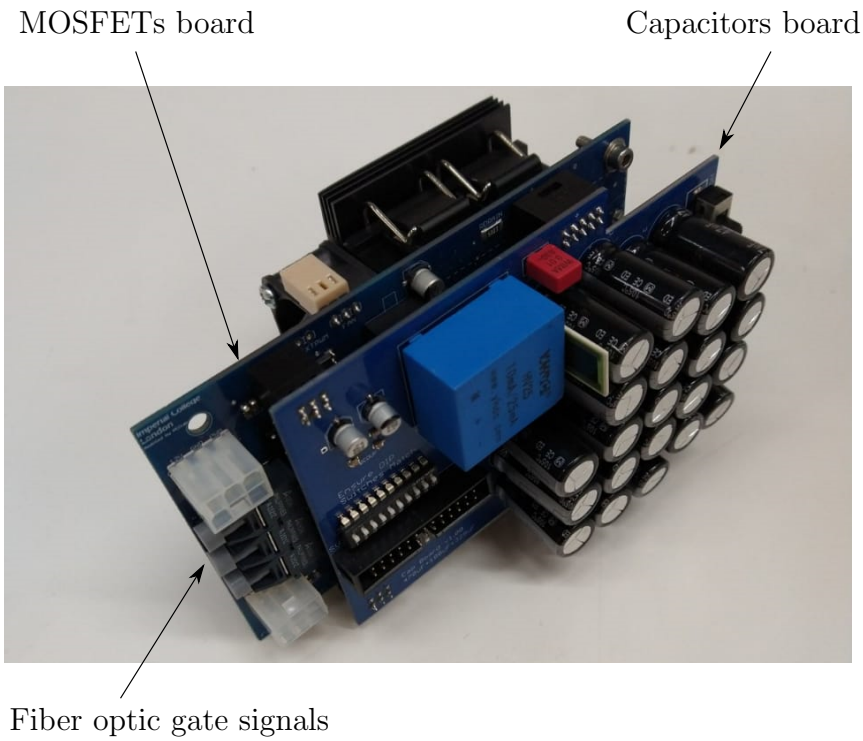


Figure 6.2: *Half-bridge cell and full-bridge*

the various control variables. Details of the Simulink model and control platform are presented in subsection 6.5.

Finally, a high-performance six channel oscilloscope ,the Tektronix MSO46 4-BW-200, was used to save the data of the electrical variables of the converter.

6.3 Half-bridge cell and full-bridge design

Identical full-bridge cells were used for the full-bridge and the half-bridge cells since they operate with similar voltage and current requirements. In the case of the half-bridge cells, only one leg was populated and controlled.

The cell is formed from two different boards, as is shown in Fig. 6.2. The first board consists of the gate signal fiber-optic receivers, the gate driver circuit, and the MOSFET full-bridge. The second board includes the dc-link capacitor, the voltage measurement stage, and the output communication connector. Both boards are coupled through the dc-link via various headers.

The main design parameters of the cells are included in Table 6.2. Each full-

Table 6.2: Parameters of Power Cells

Parameter	Value
Semiconductor devices	4x MOSFETs Infineon IPW65R041CFD
MOSFETs Heatsink	2x C40-058-AE
Total dc-link capacitance	987 μF
Gate drivers IC	2x Analog Devices ADUM4223BRWZ
Gate driver power supplies	2x TRACOPOWER TMV 2415S 15V
Voltage sensor	YHDC HV25 $\pm 5V$
Output communication bus	Serial

bridge cell utilises four Infineon MOSFET modules IPW65R041CFD rated for a nominal voltage of 650V and a nominal current of 15A, which provides adequate overrating for a lab test environment. The design considers a dedicated integrated circuit (IC) for the gate drivers in boost-strap configuration. Furthermore, an isolated 15V power supply is used to achieve the required isolation in each half-bridge boost-strap gate circuit. Zener diodes are used to prevent transient over-voltage of the MOSFETs gate signals and a pull-down resistor connected between gate and emitter of the MOSFET ensures that the semiconductor remains off during the power-up sequence of the gate driver.

Each cell has a dc-link capacitance of 987 μF formed from 21x47 μF capacitors. The required capacitance of the cells is defined by the stack modulation and the maximum capacitor voltage ripple. Since the ac-link current modelling assumes fixed voltages in the cells, it is desirable to ensure that the voltage ripple in its capacitors is low. Thus, the capacitance of the cell capacitors are selected to keep the voltage ripple below 2%, using expression (4.10).

Moreover, each cells include a 5V voltage transductor which is used to measure the capacitor voltage. This measured voltage is communicated over the main control hardware using a serial communication bus. Finally, a DIN mount adapter was designed and built using a 3d printer.

6.4 Ac-link inductor design

The ac-link inductor was specially designed for the application in order to avoid saturation and provide good performance at 5kHz. The design procedure is detailed in [218], considering the guidelines of [219].

The inputs of the design process are: i) inductance required (L_{req}), ii) the maximum peak current in the winding (I_{peak}), and iii) the characteristics of the core such as effective magnetic cross section (A_e), the effective magnetic path length (l_e), the relative effective permeability (μ_e), and the maximum operational point of the magnetic flux density (B_{op}).

Since the prototype is designed to transfer the nominal power as the maximum power at $r_V = 1$, the inductance required L_{req} can be deducted from the P_{base} expression (A.13).

$$L_{req} = \frac{V_{HV}^2 r_S^2}{12 f_s P_{base}} \tag{6.1}$$

Therefore, the required inductance L_{req} is 808.2 μH, considering the prototype parameters of Table 6.1. The maximum peak current I_{peak} considered in the design is 10A to provide over a 20% of margin of safety.

Fig. 6.3 illustrates the ferrite core PM87/70 (material N87) used in the design, and its main parameters are summarised in Table 6.3. The operational point of the magnetic flux density B_{op} was selected to ensure the operation in the linear zone of hysteresis loop.

Table 6.3: Core Parameters

Description	Parameter	Value
Effective magnetic cross section	A_e	910 mm^2
Effective magnetic path length	l_e	146 mm
Relative effective permeability	μ_e	1530
Saturation magnetic flux density	B_{sat}	390 mT
Operating magnetic flux density	B_{op}	200 mT

According to [218], the outputs of the design process are: i) the number of



Figure 6.3: *EPCOS Core PM87/70.*

turns (n) and ii) the total air-gap (s). Thus, considering the values of the core parameters, the inductance required (L_{req}), and the maximum peak current in the winding (I_{peak}), the output of the design process is summarised in Table 6.4 and the resulting inductor is shown in Fig 6.4.

Table 6.4: Output of the inductor design process

Description	Parameter	Value
Number of turns	n	44
Total air gap	s	2.69 mm

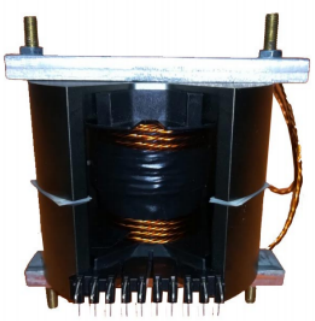


Figure 6.4: *Designed ac-link inductor with 44 turns, 3 mm air-gap, and EPCOS Core PM87/70. Resulting inductance of* $811\mu H$.

The inductor designed was experimentally tested, and an inductance of 811 μH at 5 kHz is achieved, after adjusting the total air gap to 3 mm. This represents a 0.35% error with respect to the required inductance value.

6.5 Control Platform

The OPAL-RT OP4510 system is used as the converter control platform. This hardware is based on an Intel Xeon E3 v5 CPU and a Kintex-7 FPGA. The OPAL-RT unit provides a flexible architecture configuration for the I/O cards, as is shown in Fig. 6.5. These I/O cards interface to the FPGA, allowing fast and accurate signal generation and processing. A fast PCI-express bus links the FPGA and CPU, enabling the exchanging of data and signals between processors. Thus, the CPU is able to carry out the high-level control, whilst the FPGA implements the modulation and signals processing.

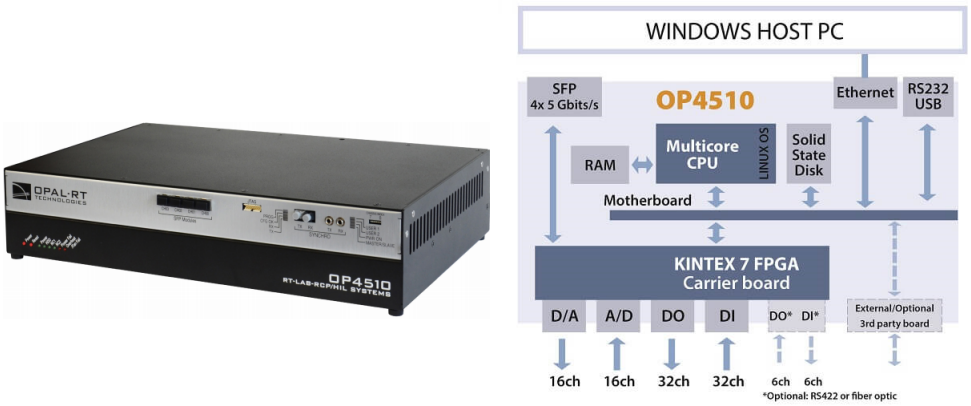


Figure 6.5: *Opal-RT 4510 hardware architecture.*

The specifications of the OPAL-RT4510 unit used in the PhD project are summarized in Table 6.5.

Table 6.5: OP4510 Hardware Configuration

Description	Specification
CPU	Intel Xeon CPU 4cores 3.5GHz
FPGA	Kintex7 325T
Digital output card	2xOP5360 (32 channels, push-pull, 5-15V, 50ns)
Analog input card	2xOP5340 (16 channels, 2MS/s, 16bits)
Programming environment	Matlab Simulink/ RT-Lab

This unit has two digital output cards OP5360, offering a total of 64 output channels suitable for high-frequency (up to 500 kHz) and a voltage output from 5V to 15V. Each digital card provides 32 isolated channels divided in two

DB37 output connectors.

The digital output cards generate the gate signals for the power electronic devices. However, an intermediate card has been designed to adapt the digital outputs (DO) to fiber-optic signals (FO), since the cells were designed with a fiber-optic interface receiver. The adapting card DO/FO is shown in Fig 6.6.

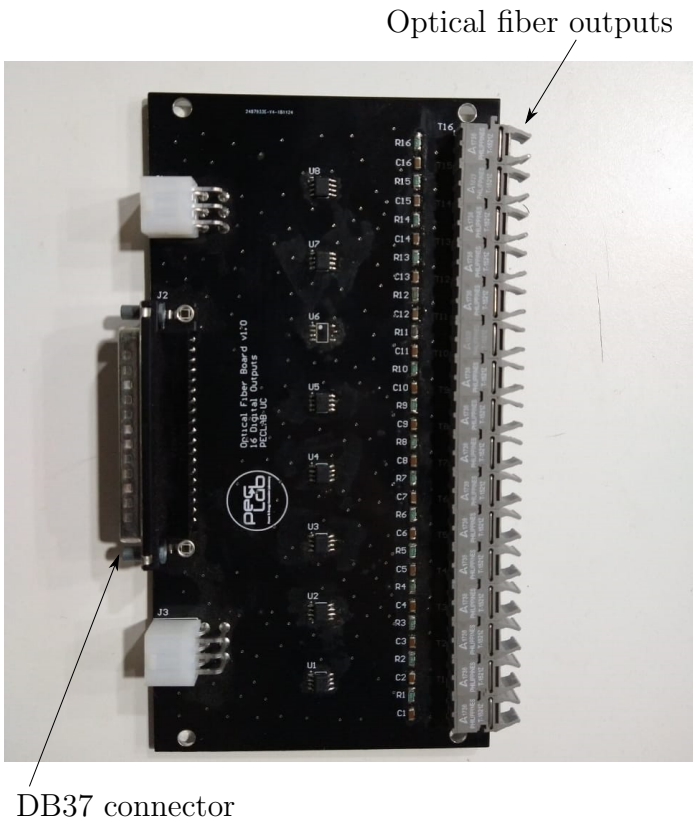


Figure 6.6: *Optical fiber board*

The OPAL-RT unit also has two analog input cards OP5340, which are used to receive the measurements from the power converter. These input cards provide up to 16 input channels ±20V each, using DB37 connectors as input interface. The OP5340 cards convert the analog signals to digital using a 16-bit resolution analog-to-digital converter (ADC). Each ADC can sample up to 125 kS/s, giving a total throughput of 2 MS/s, and all channels are simultaneously sampled.

The control platform is sued to implement the control scheme in a Matlab Simulink model, which is then adapted and transferred to the CPU and FPGA through the software RT-Lab. An overview of the Matlab Simulink model is

shown in Fig. 6.7 and its main parameters are listed in Table 6.6

Table 6.6: Parameters of Control Platform

Description	Parameter	Value
CPU sample time	$T_{sample-CPU}$	200 μs
FPGA sample time	$T_{sample-FPGA}$	50 ns
Output voltage PI controller	K_p / K_i	0.0698 / 3.8965
Sorting frequency	f_{sort}	5kHz

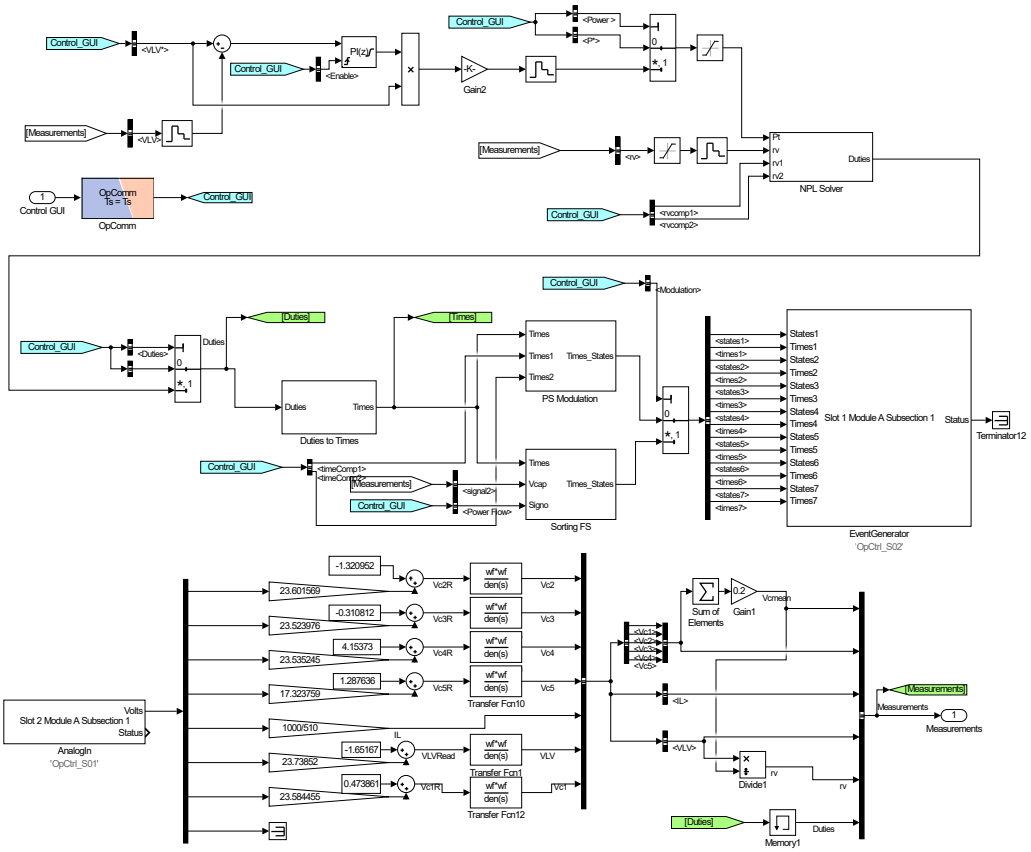


Figure 6.7: *Matlab implementation of modulation and control scheme.*

The output voltage PI controller was implemented with an anti-winding continuous PI block, and it is discretised using the Fordward Euler integration method. The PI controller parameters is adjusted for a natural frequency of $\omega_n = 20\pi$ with a damping factor of $\xi = 0.707$, considering the close-loop transfer function associated to 4.1.

Chapter 7

Experimental Validation

7.1 Introduction

The experimental setup described in Chapter 6 has been implemented to verify the theoretical and simulation work proposed in this thesis. This Chapter presents experimental results of the modulation and control strategies proposed in Chapters 3 and 4. Thus, the following tests have been performed to validate proper capacitor voltage balancing, bidirectional power-flow and ZCS operation:

1. Controlled power-flow with fixed dc voltages.

2. Controlled output voltage operation with LV dc port operated as a load.

The parameters considered for all test are detailed in Table 6.1. Results are saved using the OPAL-RT platform and a Tektronix MSO46 oscilloscope with differential voltage and current probes. The sample time used for the Opal-RT and oscilloscope variables is $1ms$ and $0.8\mu s$ respectively.
For all further results, the stack modulation is performed to achieve the higher stack voltage ratio possible for five cells ($r_S = \frac{1}{4}$) using phase-shift modulation. Similar results were obtained using the sorting modulation scheme, which are detailed in Section 7.4.

7.2 Controlled power-flow at fixed dc voltages.

The first set of experimental results considers both dc ports connected to bi-directional dc voltage sources. Thus, this configuration allows the evaluation of the power control-loop. Both stack modulation proposals and the bi-directional operation are validated.

A subset of experimental results obtained under this configuration are:

1. Steady-state operation.
2. Maximum power-flow reversal.

7.2.1 Steady-state operation.

The first subset of experimental results consists of steady-state operation under different power references and output voltage levels in order to validate the power modelling over a wide voltage range. The steady-state operating points tested are obtained combining the following parameters:

1. Adjusted LV dc voltage to evaluate three scenarios: $r_V \approx 0.8$, $r_V \approx 1$ and $r_V \approx 1.2$.
2. Maximum power ($P_{pu} \approx r_V$) and low power operation ($P_{pu} = 0.2$).
3. Positive and negative power-flow.

Fig. 7.1 shows the ac-link waveforms at maximum power and power-flow from HV to LV port for three different output voltage levels: $V_{LV} = 150V$ ($r_V \approx 0.8$), (b) $V_{LV} = 187.5V$ ($r_V \approx 1$) and (c) $V_{LV} = 225V$ ($r_V \approx 1.2$). As it is deducted from the control diagram (Fig. 3.15), at these voltage levels and power, the converter is operating within the trapezoidal current mode, therefore, four ZCS transitions are generated in a switching period T_s. In all cases, the asymmetry of the voltage is noticeable at the ac-link (v_{L1} and v_{L2}) and the inductor current i_L between the positive and negative half-cycles,

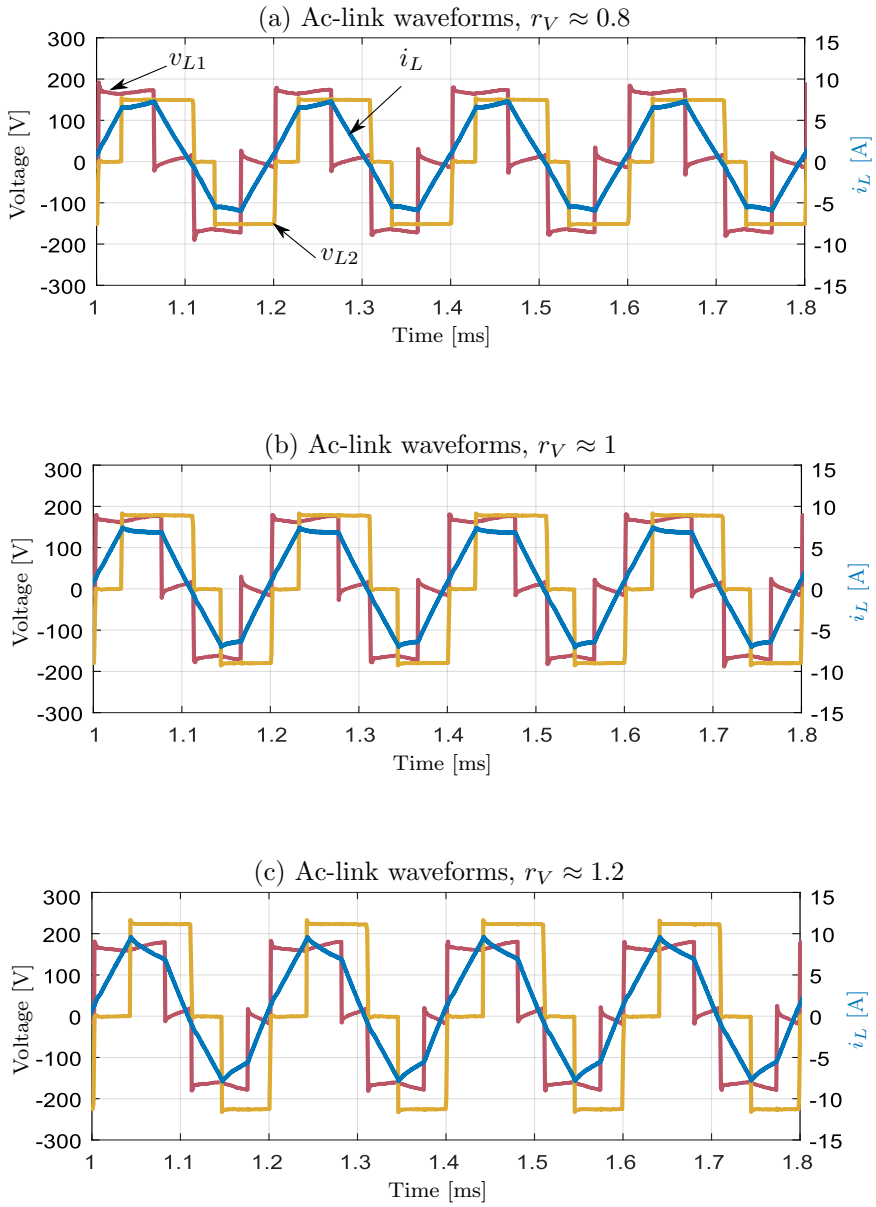


Figure 7.1: *Experimental results at steady-state, positive power-flow and maximum power: (a) Output voltage $V_{LV} = 150V$ ($r_V \approx 0.8$), (b) Output voltage $V_{LV} = 187.5V$ ($r_V \approx 1$) and (c) Output voltage $V_{LV} = 225V$ ($r_V \approx 1.2$)*

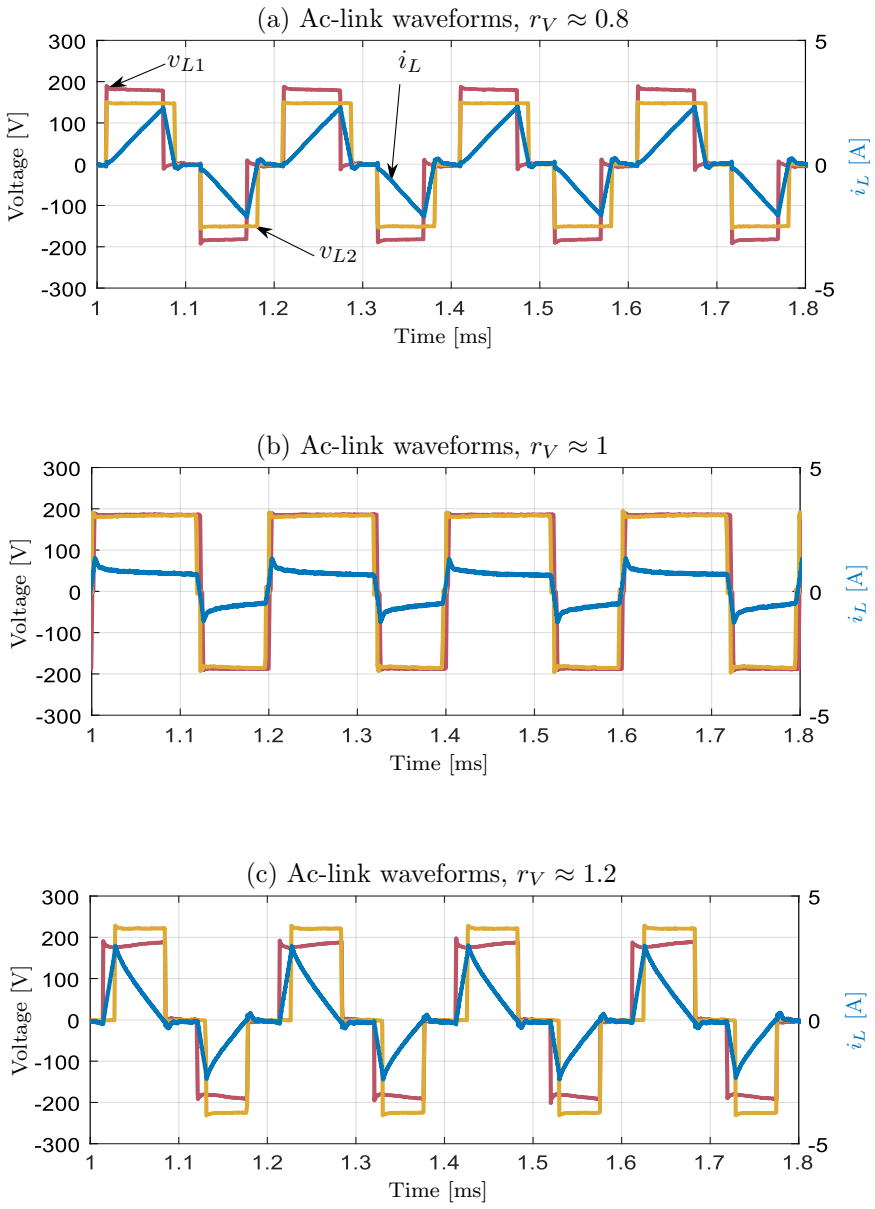


Figure 7.2: *Experimental results at steady-state, positive power-flow and low power ($P_{pu} = 0.2$): (a) Output voltage $V_{LV} = 150V$ ($r_V \approx 0.8$), (b) Output voltage $V_{LV} = 187.5V$ ($r_V \approx 1$) and (c) Output voltage $V_{LV} = 225V$ ($r_V \approx 1.2$)*

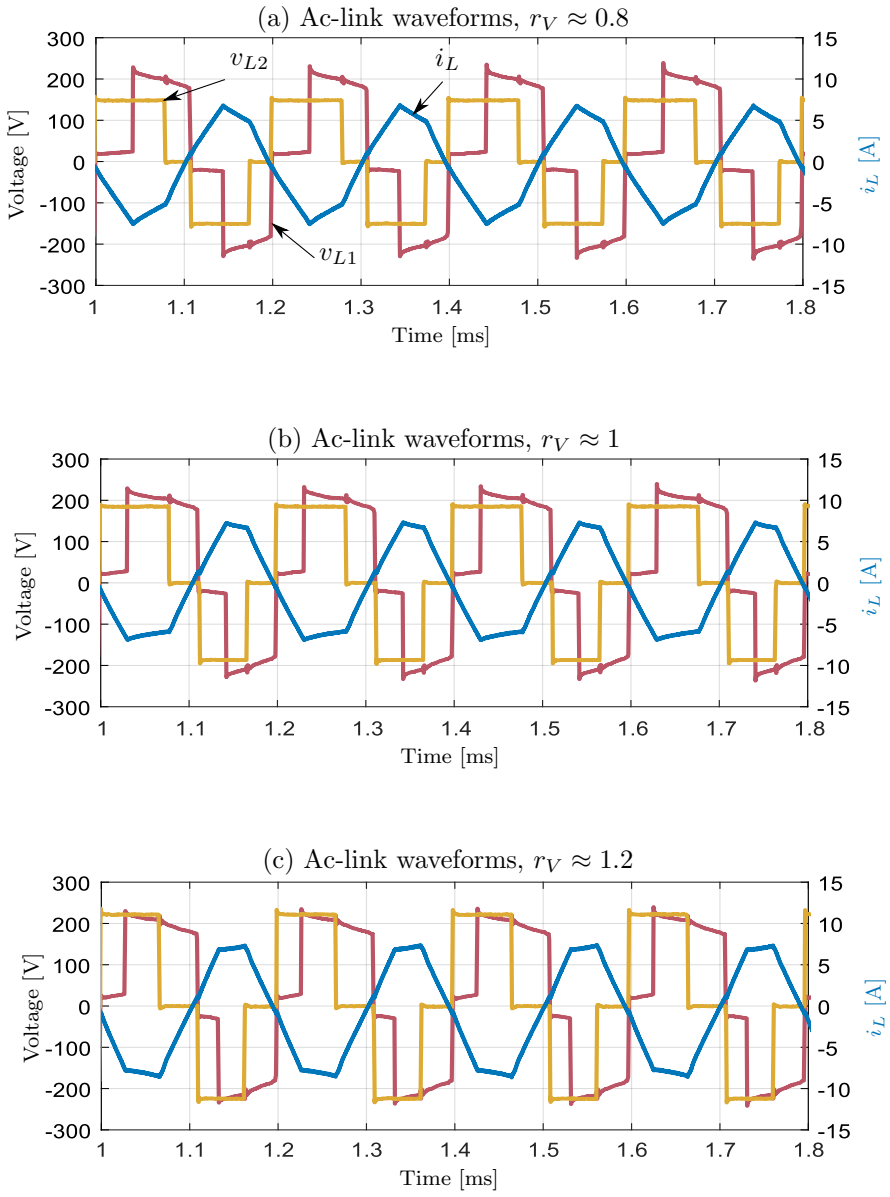


Figure 7.3: *Experimental results at steady-state, negative power-flow and maximum power: (a) Output voltage* $V_{LV} = 150V$ *(*$r_V \approx 0.8$*), (b) Output voltage* $V_{LV} = 187.5V$ *(*$r_V \approx 1$*) and (c) Output voltage* $V_{LV} = 225V$ *(*$r_V \approx 1.2$*)*

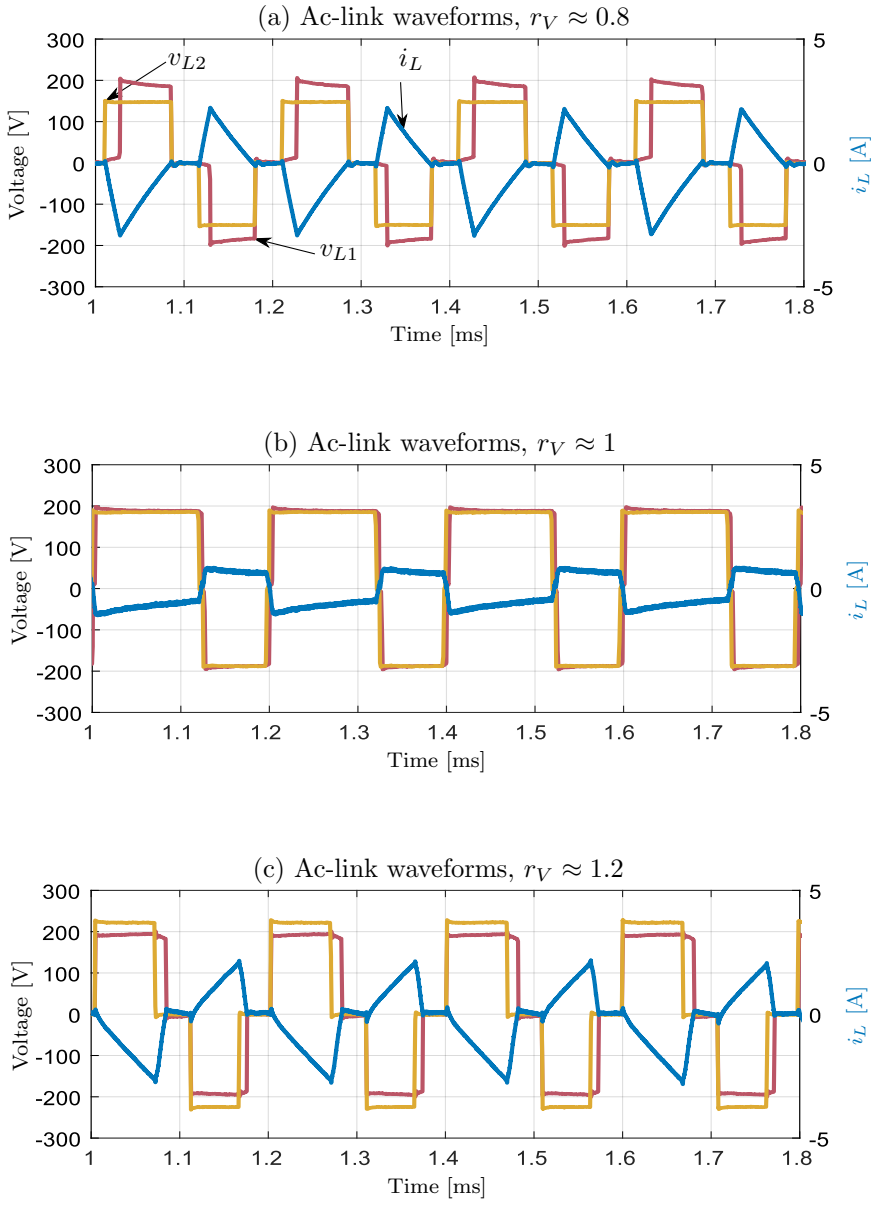


Figure 7.4: *Experimental results at steady-state, negative power-flow and low power ($P_{pu} = 0.2$): (a) Output voltage $V_{LV} = 150V$ ($r_V \approx 0.8$), (b) Output voltage $V_{LV} = 187.5V$ ($r_V \approx 1$) and (c) Output voltage $V_{LV} = 225V$ ($r_V \approx 1.2$)*

which is required to generate the dc current component. Furthermore, the current fits across the entire switching cycle T_s, avoiding prolonged states at zero current in order to minimise the rms current.

The ac-link waveforms at reduced power transfer ($P_{pu} = 0.2$) for the same output voltages values are illustrated in Fig 7.2. Where the parameter r_V is on-unity (7.2 (a)(c)), the current modulation requires the triangular operation, whilst if $r_V \approx 1$ the trapezoidal current mode is still able to modulate the power reference, as was deducted in the control diagram. When the converter is operating within the triangular current mode, six ZCS transitions are generated in a switching period T_s and prolonged states at zero current are needed it to achieve the lower power transfer. Nevertheless, the $r_V \approx 1$ case can deliver low power reducing the phase-shift between v_{L1} and v_{L2}, as is shown in 7.2 (b).

The bidirectional operation of the converter is illustrated for the same power and voltage levels in Fig. 7.3 and 7.4, showing symmetrical operation for both the positive and negative power-flow conditions.

7.2.2 Maximum power reversal.

The final subset of lab testing at fixed dc voltages shows the dynamic behaviour of the converter under maximum power reversal.

Fig. 7.5 illustrates the converter step response for an instantaneous change of direction in the power-flow at maximum power, starting from positive power-flow (HV to LV direction) and ending in negative power-flow (LV to HV direction) (see Fig. 7.5 (a)).

Since the magnitude of the reference power remains constant, the absolute value of all duty cycles remain invariant throughout the test, only the sign of the phase-shifts Φ_1 and Φ_2 is changed (see Fig. 7.5 (b)).

The MMC capacitors maintain voltage balance during all of the tests, regardless of the instantaneous change in the direction of power-flow, as is illustrated

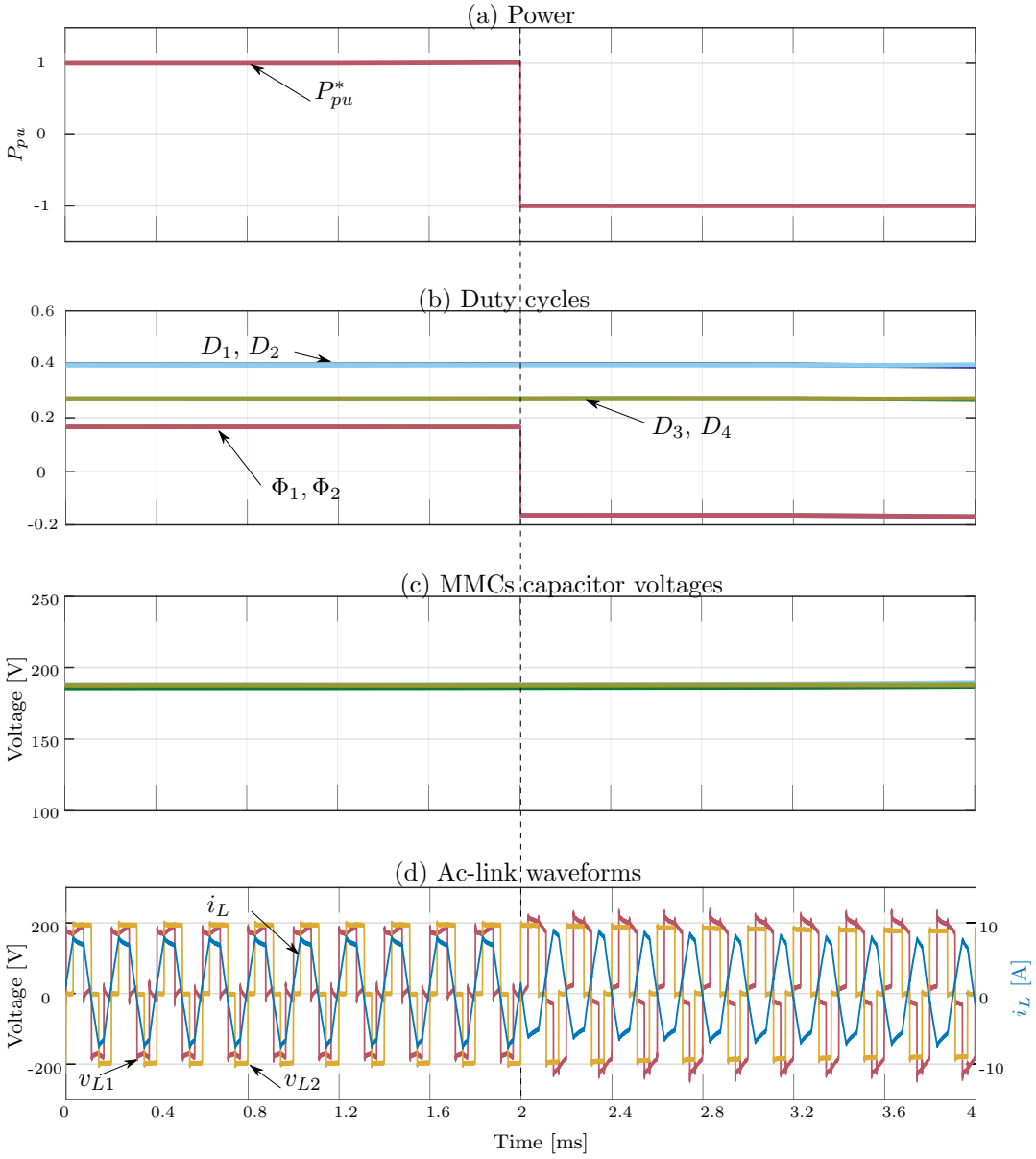


Figure 7.5: *Experimental results for maximum power reversal : (a) Output voltage, (b) Duty cycles, (c) MMC capacitor voltages and (d) Ac-link waveforms.*

in 7.5 (c)).

Finally, the waveforms of the current and the voltages at the ac-link confirms that the trapezoidal current operation is used over the whole test period (7.5 (d)). Furthermore, the zoomed captures confirm the soft-switching transitions in the semiconductor devices under both operating modes.

7.3 Controlled output voltage operation with LV dc port as load.

A second set of experimental tests was performed to evaluate the dynamic behaviour of the converter over a wide voltage range. In this case, the LV dc voltage source was replaced with a resistive load, and the output voltage control loop is implemented in order to regulate the output voltage. Thus, this configuration allows the evaluation of the converter and its control scheme under three scenarios:

1. Output voltage step response at fixed load.
2. Dynamic behaviour under changes in the output load.
3. Dynamic behaviour under perturbation of the input voltage.

7.3.1 Output voltage step response at fixed load.

The first tested scenario is the output voltage step response, starting from low-voltage operation. This test allows the evaluation of the converter operation over wide output voltage range, which is required for the MMC converter when the capacitors are pre-charging and for black start operation.

Fig. 7.6 shows the V_{LV} step response of the converter with a controlled output voltage when the LV dc port is loaded with a 56Ω resistor, starting from a low voltage operation (20 V) until the nominal output voltage is reached ($V^*_{LV} = 187.5V$). The dynamic behaviour of the duty cycles (Fig. 7.6 (b))

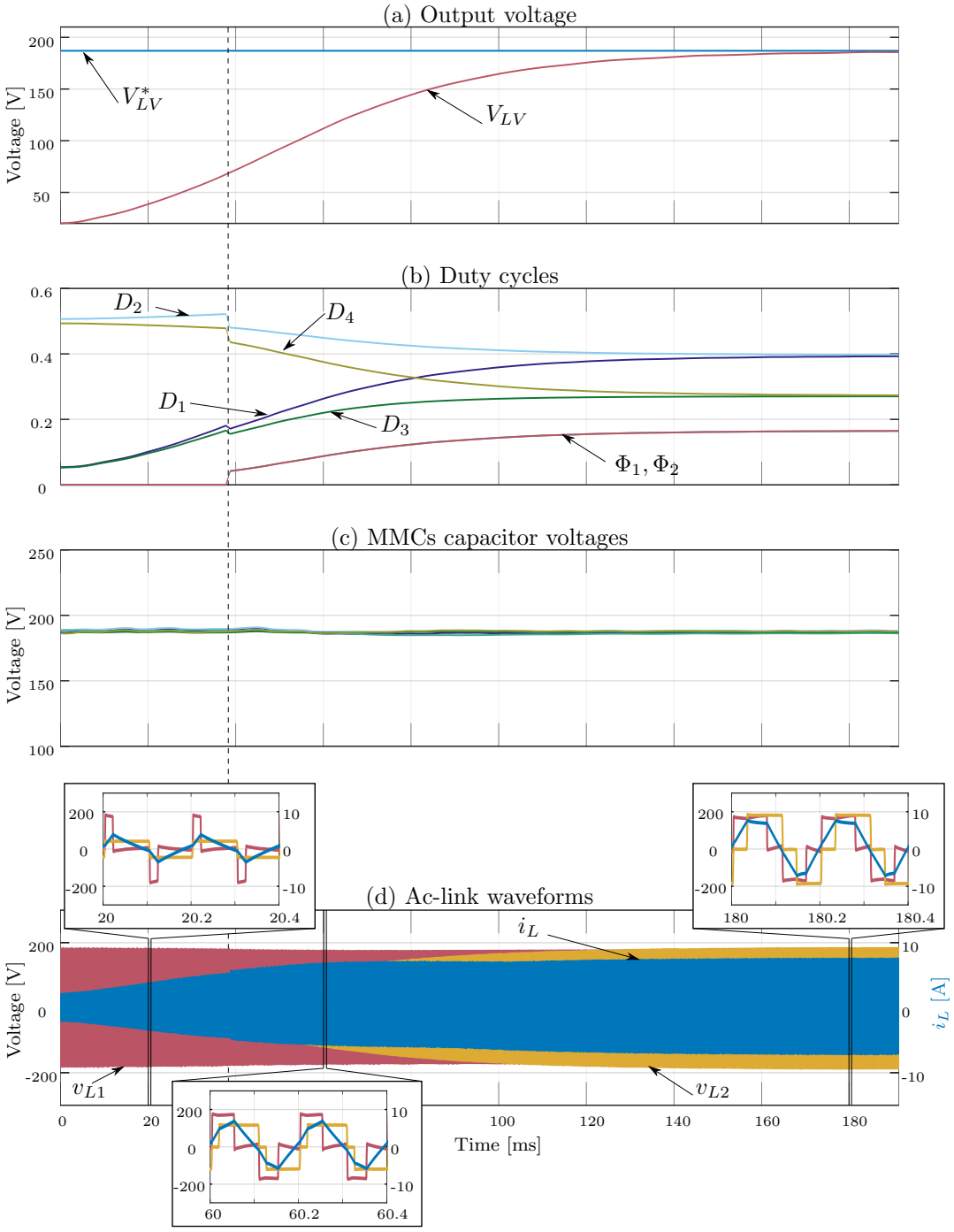


Figure 7.6: *Experimental results for V_{LV} step response: (a) Output voltage, (b) Duty cycles, (c) MMC capacitor voltages and (d) Ac-link waveforms.*

shows a well damped response even during the transition from the triangular to trapezoidal current mode. This transition occurs when Φ_i begins to be non-zero at 38 [ms] (dashed-line), indicating that prior to this time the converter was operating in triangular current mode zone due to the low value of r_V, and after this in trapezoidal mode to enhance the power transfer. At the end of the time-window the duty-cycles D_1, D_2 and D_3, D_4 converge as is predicted by (3.17), since the parameter r_V is close to unity at this point.

The MMC capacitor voltages are consistently balanced, regardless of the operating mode without affecting the voltage and power control (Fig. 7.6 (c)), as a result of the phase-shift stack modulation scheme, the power modelling and the natural tendency for voltage balance in this topology.

The ac-link waveforms of the current and the voltages at the inductor verifies the triangular/trapezoidal operation with reduced rms current operation in the dynamic response (Fig. 7.6 (d)). Furthermore, the zoomed part captures confirm the soft-switching operation of the converter regardless of the value of the output voltage V_{LV} and its operating mode.

7.3.2 Dynamic behaviour under changes in the output load.

In order to analyse the dynamic response of the converter under a perturbation at the LV dc port, a second test is performed with the controlled output voltage operation under a stepped change of the output load.

Fig. 7.7 shows the behaviour of the converter under an instantaneous change of the load R_o at $10ms$ (dashed line). Before this time the converter operates with nominal voltages and light load (77Ω), and thereafter the load is increased to its nominal value (56Ω).

The output voltage V_{LV} responds with a short transient before returning to its desired value in less than $70ms$ (Fig. 7.7 (a)). This is possible as a result of the fast transient response of the duty cycles (Fig. 7.7 (b)) and the MMC

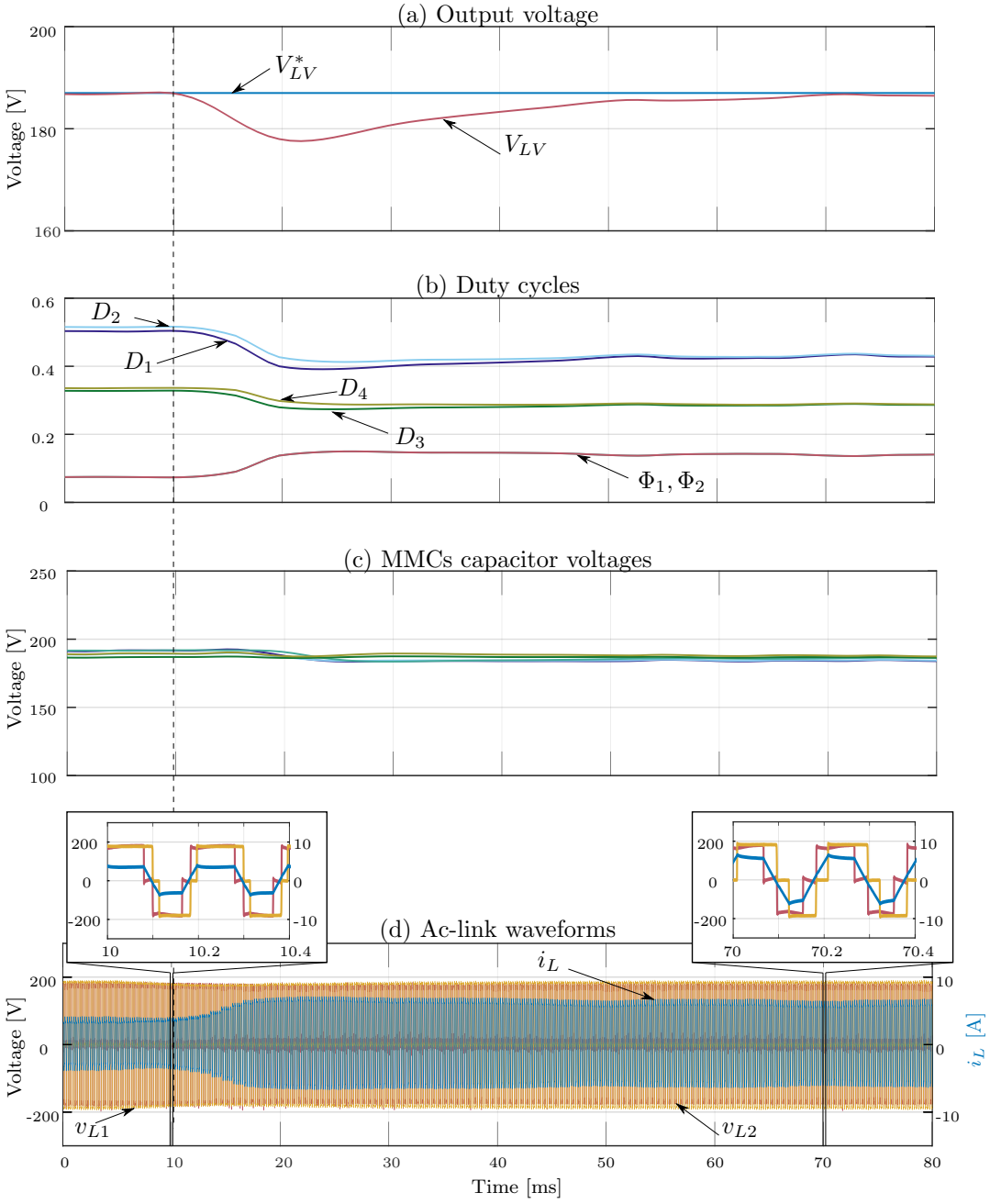


Figure 7.7: *Experimental results for R_o step response: (a) Output voltage, (b) Duty cycles, (c) MMC capacitor voltages and (d) Ac-link waveforms.*

capacitor voltages balancing over the whole period (Fig. 7.7 (c)).
The ac-link waveforms show a soft transition to the new operating point (Fig. 7.7 (d)). Furthermore, the zoomed captures confirm the soft-switching operation of the trapezoidal current for both load conditions.

7.3.3 Dynamic behaviour under perturbation in the input voltage.

The final test performed enables a view of the dynamic response of the converter under a voltage perturbation at the input port (Fig. 7.8).
The perturbation is generated with a controlled input voltage reduction of 10% at HV dc port, which is shown after the dashed line in Fig. 7.8 (a).
The output voltage V_{LV} is able to respond to the input voltage perturbation with a dynamic behaviour similar to the last test, as is illustrated in Fig. 7.8 (b). The duty-cycles quickly adapt to the new state (Fig. 7.8 (c)), whilst the MMC capacitor voltages reach the new voltage level according to (3.9) (see Fig. 7.8 (d)).
Finally, Fig. 7.8 (e) illustrates the ac-link waveforms during the test. The trapezoidal current operation is distinguishable at both V_{HV} voltage levels (zoomed captures above), whilst the zoom part of the figure details the ac-link waveforms during the disturbance itself. In the latter capture, the voltage v_{L1} (red line) is disturbed as a result of the difference between the MMCs capacitor average voltage V_C (Fig. 7.8 (d)) and its new required value after the input voltage drop. Thus, the distortion on v_{L1} causes a high transient current. However, once V_C is stabilised to its new voltage level the converter returns to the expected operational value.

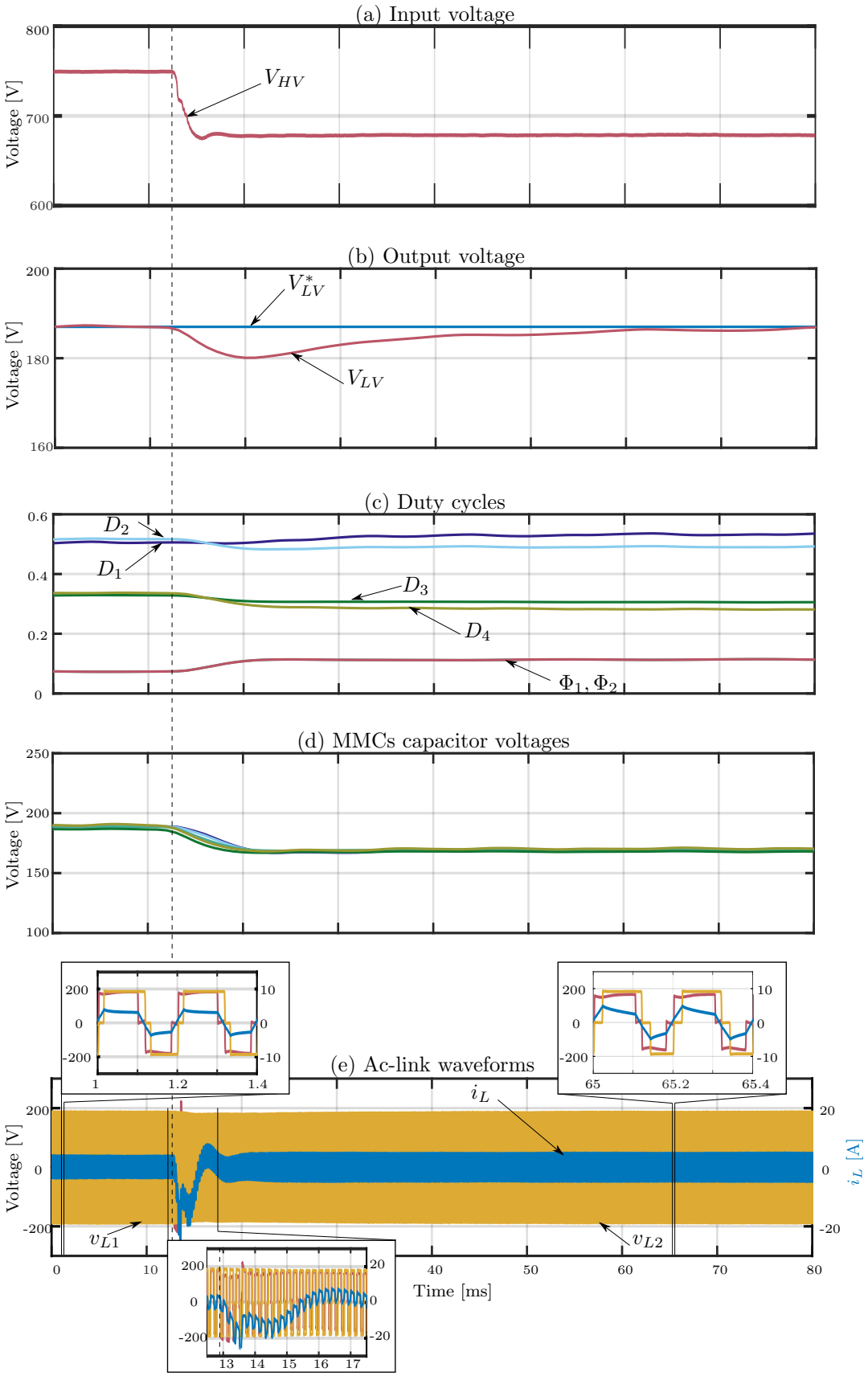


Figure 7.8: *Experimental results for V_{HV} step response: (a) Input voltage, (b) Output voltage, (c) Duty cycles, (d) MMC capacitor voltages and (e) Ac-link waveforms.*

7.4 Experimental results with sorting modulation

This section includes the main experimental results of the proposed converter working with sorting modulation, which validates its performance for the same testing scenarios described in previous results.

Fig. 7.9 illustrates the typical waveforms of one half-bridge cell and ac-link inductor using both modulation strategies. The output voltage for one cell v_1 shows its periodic nature for the case of the phase-shift modulation (Fig. 7.9 (a) above), whilst this periodic pattern could get lost for the sorting modulation, as is shown in Fig. 7.9 (b) above. In any case, the ac-link waveforms are identical for both modulation strategies.

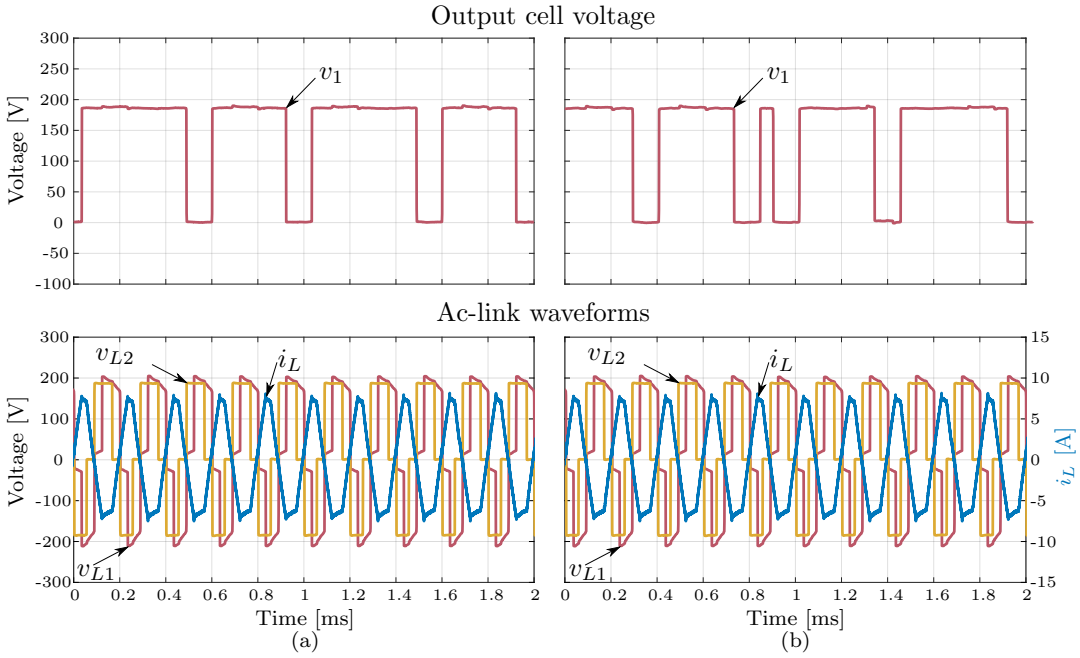


Figure 7.9: *Comparative of proposed stack modulation schemes (a) Phase-shift modulation, (b) Sorting modulation. Steady-state experimental results with* $r_V = 1$ *and negative power-flow.*

The set of dynamical results with the sorting modulation are shown in Figs. 7.10-7.13. These scenarios were tested under the same conditions as those previously described, obtaining similar results to phase-shift modulation. Thus, the experimental results validates the sorting modulation as a suitable strategy to modulate the stack voltage and to keep the voltage balance among the cell capacitors.

Although both modulations present almost identical results, the sorting modulation allows a slightly faster dynamics under perturbation in the input voltage (Fig 7.13). This can be performed since the faster response of the modulation to the transient imbalance of the MMCs capacitor voltages, as is shown in Fig. 7.13 (d) and (e).

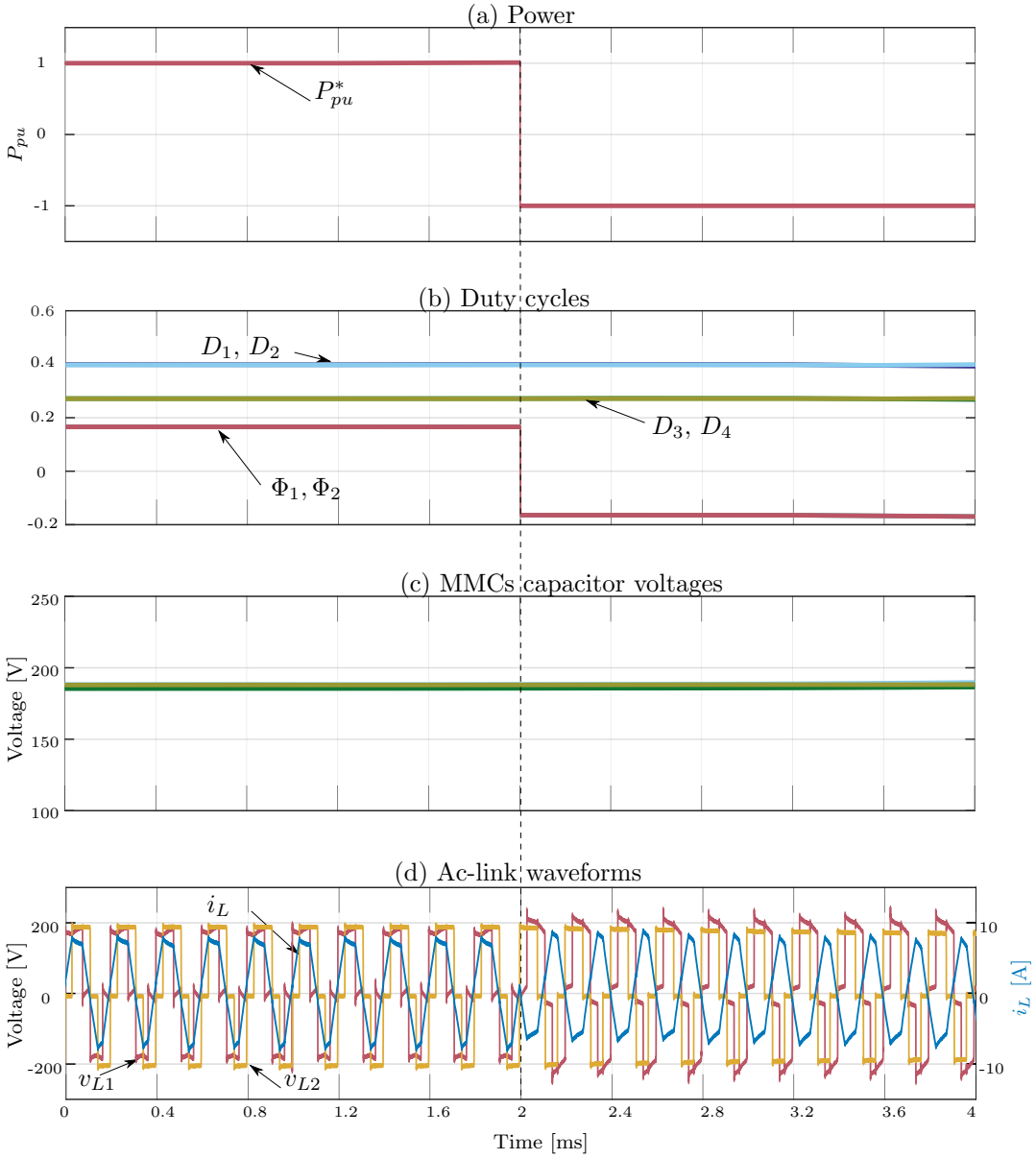


Figure 7.10: *Experimental results for maximum power reversal with sorting modulation: (a) Power reference, (b) Duty cycles, (c) MMC capacitor voltages and (d) Ac-link waveforms.*

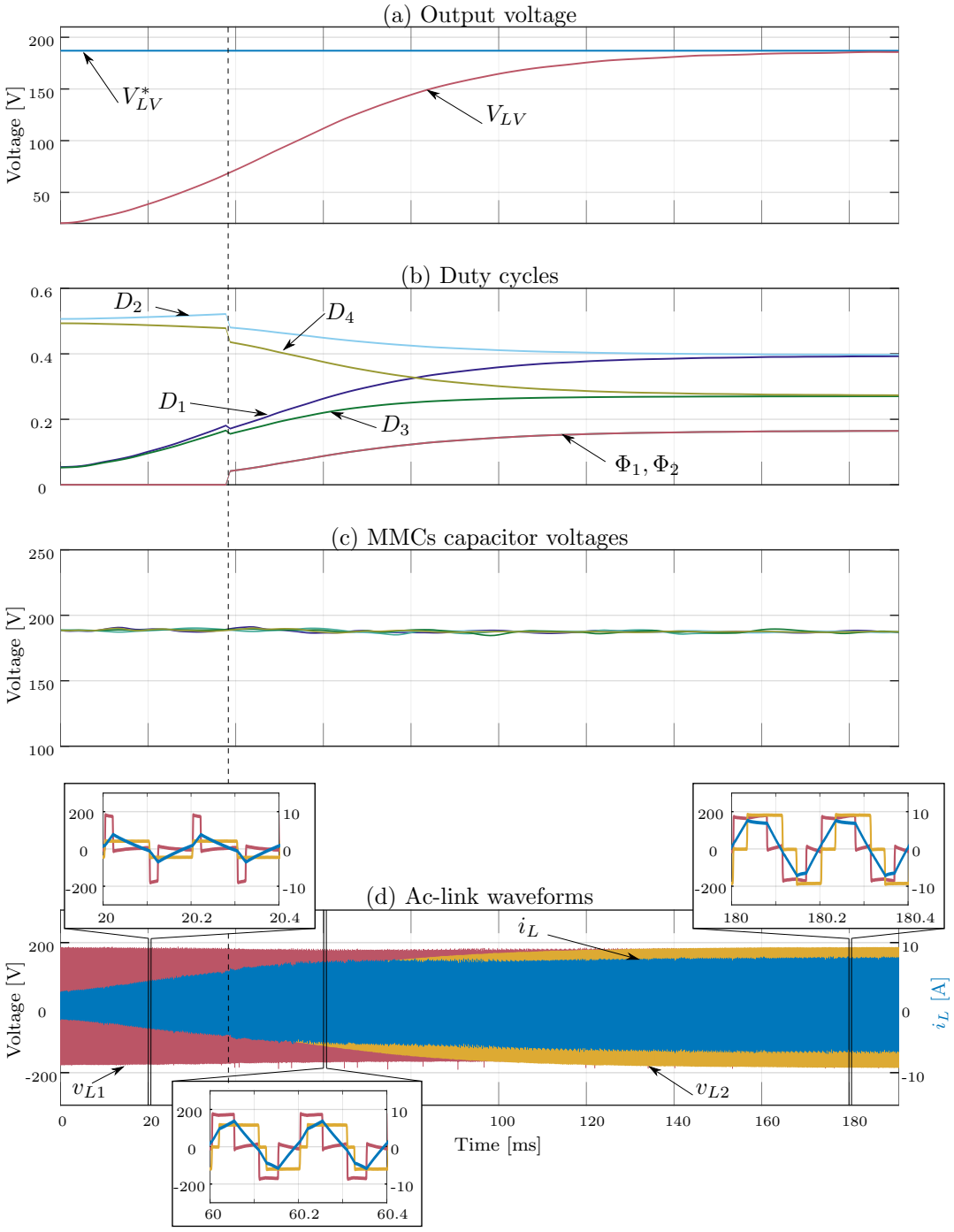


Figure 7.11: *Experimental results for V_{LV} step response with sorting modulation: (a) Output voltage, (b) Duty cycles, (c) MMC capacitor voltages and (d) Ac-link waveforms.*

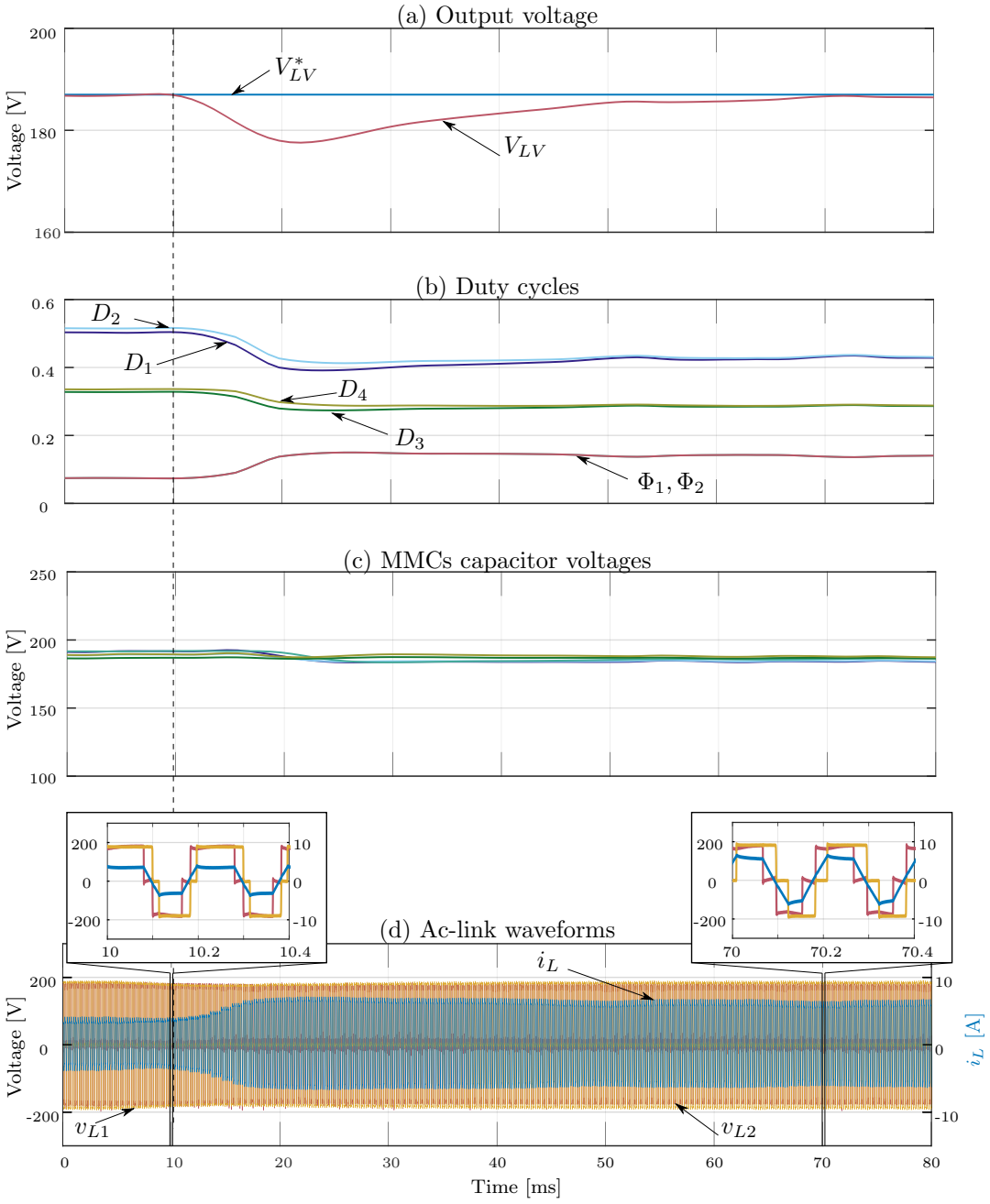


Figure 7.12: *Experimental results for R_o step response with sorting modulation: (a) Output voltage, (b) Duty cycles, (c) MMC capacitor voltages and (d) Ac-link waveforms.*

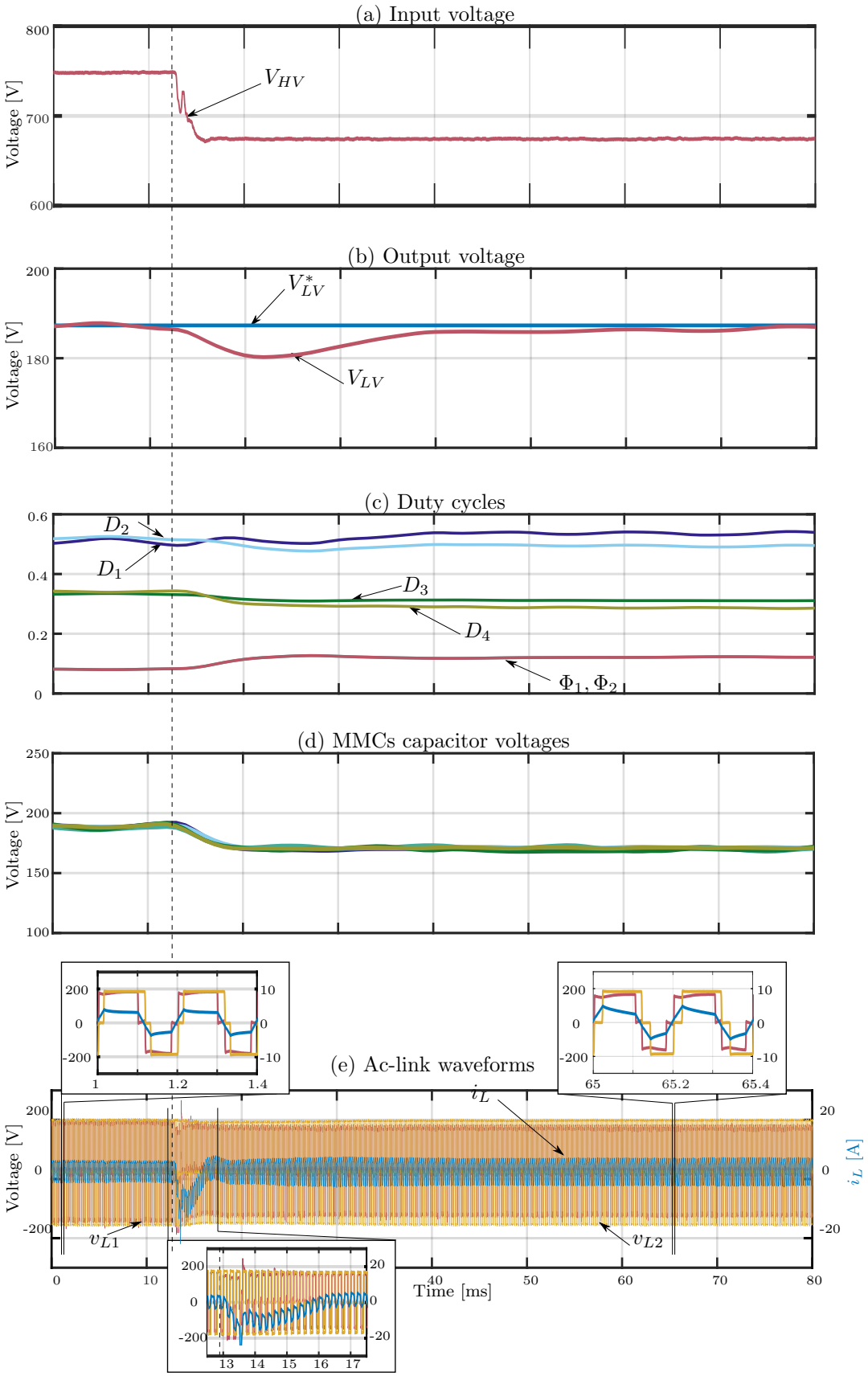


Figure 7.13: *Experimental results for V_{HV} step response with sorting modulation: (a) Input voltage, (b) Output voltage, (c) Duty cycles, (d) MMC capacitor voltages and (e) Ac-link waveforms.*

Chapter 8

Conclusion

Recent developments in dc powered technologies have increased interest in highly efficient dc-dc converters, especially at high voltage and high-step voltage ratios. MMCs are an attractive alternative approach to this demand because they can manage medium and high dc voltages while using standard semiconductor devices with high efficiency if they employ soft-switching techniques.

According to the results obtained, the high step ratio MMC dc-dc proposed in this PhD project is a suitable power converter that can be successfully applied for the interconnection between low and medium-high voltage dc grids. Also, the MMC dc-dc can achieve soft-switching, high dc-dc voltage step ratio and bidirectional power flow, without the need of a resonant circuit. Finally, a control scheme can provide proper capacitor voltage balancing for a wide voltage and power output.

Additionally, the major findings of this thesis are summarised below:

The TCM scheme can be adapted to be applied in the high step ratio MMC dc-dc, maintaining the benefits of TCM over the resonant operation. These advantages are fixed frequency operation, ZCS at the whole operating range, easier and less restrictive design due the absence of the resonant tank and simpler power control and modelling. Also, TCM enables a bidirectional power flow operation. All these features have been confirmed in simulations and

experimental validation.

The asymmetrical trapezoidal current operation presents an extra degree of freedom. Thus, an optimisation problem can be defined to minimise the rms inductor current. Since the soft-switching operation of the TCM naturally leads to reduced switching losses, the minimisation of the rms current is an attractive objective of the optimisation problem in order to reduce the conduction power losses and the sizing of the semiconductor devices and passive components. The solution of the optimisation problem can be implemented without much computational effort using look-up tables, as it was performed in the experimental prototype.

The TCM modulation can be incorporated in a simple control scheme to regulate the output voltage. Thanks to the wide output voltage range, the proposed control scheme enables grid forming and black start operation. Furthermore, the converter has satisfactory dynamic response under perturbations at the input and output ports. Simulations and experimental results have confirmed the correct performance of the control scheme.

The voltage balance among the floating cell capacitors is achieved in all tested scenarios. Thus, the natural negative feedback loop between the mean voltage of the cell capacitors and the slope of the trapezoidal current reduces the voltage balance problem to a proper stack modulation. This stack voltage modulation can be addressed with a phase-shift or sorting modulation. Both modulations have been validated by simulations and experimental results. Although both modulations present adequate results, the sorting modulation allows a slightly faster dynamics in the event of disturbances. However, it requires additional sensors to be implemented.

8.1 Main Contributions

The main contributions of this Phd. project are listed below:

1. A general model of the a high step voltage ratio MMC dc-dc avoiding

the resonance operation.

2. A TCM modulation scheme which achieves a bidirectional power flow in a wide power and voltage operating range.

3. An optimised solution for the modulation problem which achieves zero-current switching and minimal rms current.

4. Two modulation strategies for the stack voltage (phase-shift and sorting based) to generate reduced ac-link voltage and keep the voltage balance among the cell capacitors.

5. A simple control strategy which enables grid forming and black start.

Finally, the research developed during this Phd. project has led to the publication of 5 international conference papers and 2 journal papers submitted to Q1 indexed journals.

8.2 Future work

The following topics may be attractive for future research, taking this thesis as a starting point:

1. The incorporation of a medium frequency transformer at the ac-link could increase the voltage transformation and improve the overall efficiency if its additional losses were low enough to compensate the reduction of the conduction losses in the cell stack. This defines an interesting engineering problem to select the amount of voltage conversion performed by the SM stack and by the transformer. However, the incorporation of a transformer must deal with the dc component present in the ac-link in order to avoid saturation of the core.

2. The TCM modulation might be adapted to a bipolar stack configuration. This adaptation would avoid the flow of the dc component through the

ac-link, creating additional current loops. Therefore, a transformer could be easily incorporated in the ac-link since the absence of voltage and current dc components.

3. Additional applications for the MMC dc-dc could appear if it incorporates energy storage. This could be achieved if the cell capacitors are replaced by batteries or fuel cells.

4. The modulation optimisation problem could be resolved using alternative objective functions in order to incorporate additional features. Furthermore, this model could be extended to apply more complex control schemes such as model predictive pulse pattern control.

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Appendix A

Derivations of average power expressions

In order to obtain the expressions for the average power in one cycle, the current piece-wise function found in (3.34) is used to model the trapezoidal current waveform.

$$i_L(t) = \begin{cases} 0 & \text{if } t \in [t_0, t_1] \\ \frac{r_S V_{HV}}{L}(t–t_1) & \text{if } t \in [t_1, t_2] \\ \frac{r_S V_{HV}}{L}\Phi_1 T_s + \frac{r_S \cdot V_{HV} \cdot (1–r_V)}{L}(t–t_2) & \text{if } t \in [t_2, t_3] \\ \frac{r_S V_{HV}}{L}\Phi_1 T_s + \frac{r_S \cdot V_{HV} \cdot (1–r_V)}{L}(D_1–\Phi_1)T_s - \frac{r_S \cdot V_{HV} \cdot r_V}{L}(t–t_3) & \text{if } t \in [t_3, t_4] \\ 0 & \text{if } t \in [t_4, t_5] \\ –\frac{r_S V_{HV}}{L}(t–t_5) & \text{if } t \in [t_5, t_6] \\ –\frac{r_S V_{HV}}{L}\Phi_2 T_s - \frac{r_S \cdot V_{HV} \cdot (1–r_V)}{L}(t–t_6) & \text{if } t \in [t_6, t_7] \\ –\frac{r_S V_{HV}}{L}\Phi_2 T_s - \frac{r_S \cdot V_{HV} \cdot (1–r_V)}{L}(D_3–\Phi_2)T_s + \frac{r_S \cdot V_{HV} \cdot r_V}{L}(t–t_7) & \text{if } t \in [t_7, t_8] \\ 0 & \text{if } t \in [t_8, t_0 + T_s] \end{cases} \tag{A.1}$$

A.1 Derivation of P_{HV}

The expression for the average power at the high-voltage port in one cycle P_{HV} is deducted in (A.2), as function of the current i_L.

$$\begin{aligned} P_{HV} &= \frac{1}{T_s}\int_{t_0}^{t_0+T_s} V_{HV} \cdot i_L \cdot dt \\ &= \frac{V_{HV}}{T_s}\Big(\int_{t_1}^{t_2} i_L \cdot dt + \int_{t_2}^{t_3} i_L \cdot dt + \int_{t_3}^{t_4} i_L \cdot dt + \int_{t_5}^{t_6} i_L \cdot dt + \int_{t_6}^{t_7} i_L \cdot dt + \int_{t_7}^{t_8} i_L \cdot dt\Big) \end{aligned} \tag{A.2}$$

The first integral is obtained in (A.3), noticing that $t_2 - t_1 = \Phi_1 \cdot T_s$ (see Fig.3 (a)).

$$\int_{t_1}^{t_2} i_L \cdot dt = \int_{t_1}^{t_2} \frac{V_{HV} \cdot r_S \cdot (t–t_1)}{L} \cdot dt = \frac{V_{HV} \cdot r_S \cdot T_s^2}{L} \cdot \frac{\Phi_1^2}{2} \tag{A.3}$$

The second integral is deducted in (A.4), noticing that $t_3 - t_2 = (D_1 - \Phi_1) \cdot T_s$ (see Fig.3 (a)).

$$\begin{aligned} \int_{t_2}^{t_3} i_L \cdot dt &= \int_{t_2}^{t_3} \Big(\frac{V_{HV} \cdot r_S}{L} \Phi_1 T_s + \frac{V_{HV} \cdot r_S \cdot (1–r_V)}{L} (t–t_2) \Big) \cdot dt \\ &= \frac{V_{HV} \cdot r_S \cdot T_s^2}{L} \Big(\Phi_1 + (1–r_V) \frac{(D_1–\Phi_1)}{2} \Big) (D_1–\Phi_1) \end{aligned} \tag{A.4}$$

Finally, as $t_4 - t_3 = (\Phi_1 + D_1 - D_2)T_s$ (see Fig. 3 (a)) and using (10), this period can be obtained as

$$t_4 - t_3 = \Big(\Phi_1 + D_1 (\frac{1}{r_V} - 1) \Big) T_s \tag{A.5}$$

Thus, the third integral can be expressed as

$$\begin{aligned} \int_{t_3}^{t_4} i_L \cdot dt &= \int_{t_3}^{t_4} \Big(\frac{V_{HV} \cdot r_S}{L} \Phi_1 T_s + \frac{V_{HV} \cdot r_S \cdot (1–r_V)}{L} (D_1–\Phi_1) T_s – \frac{V_{HV} \cdot r_S \cdot r_V}{L} (t–t_3) \Big) \cdot dt \\ &= \frac{V_{HV} \cdot r_S \cdot T_s^2}{L} \Big(\Phi_1 + (1–r_V)(D_1–\Phi_1) – \frac{r_V (\Phi_1 + D_1 (\frac{1}{r_V}–1))}{2} \Big) \Big(\Phi_1 + D_1 (\frac{1}{r_V}–1) \Big) \end{aligned} \tag{A.6}$$

Therefore, (A.3)+(A.4)+(A.6) yields to the integration of the positive semi-cyle as

$$\int_{t_1}^{t_2} i_L \cdot dt + \int_{t_2}^{t_3} i_L \cdot dt + \int_{t_3}^{t_4} i_L \cdot dt = \frac{V_{HV} \cdot r_S \cdot T_s^2}{2L} \Big(2 D_1 \Phi_1 + D_1^2 (\frac{1}{r_V}–1) \Big) \tag{A.7}$$

In the same way, the integrals for negative semi-cycle leads to

$$\int_{t_5}^{t_6} i_L \cdot dt = – \frac{V_{HV} \cdot r_S \cdot T_s^2}{L} \cdot \frac{\Phi_2^2}{2} \tag{A.8}$$

$$\int_{t_6}^{t_7} i_L \cdot dt = – \frac{V_{HV} \cdot r_S \cdot T_s^2}{L} \Big(\Phi_2 + (1–r_V) \frac{(D_3–\Phi_2)}{2} \Big) (D_3–\Phi_2) \tag{A.9}$$

$$\int_{t_7}^{t_8} i_L \cdot dt = -\frac{V_{HV} \cdot r_S \cdot T_s^2}{L}\Big(\Phi_2 + (1–r_V)(D_3–\Phi_2)–\frac{r_V(\Phi_2 + D_3(\frac{1}{r_V}–1))}{2}\Big)\Big(\Phi_2 + D_3(\frac{1}{r_V}–1)\Big) \tag{A.10}$$

Thus, (A.8)+(A.9)+(A.10) yields to the integration of the negative semi-cycle as

$$\int_{t_5}^{t_6} i_L \cdot dt + \int_{t_6}^{t_7} i_L \cdot dt + \int_{t_7}^{t_8} i_L \cdot dt = -\frac{V_{HV} \cdot r_S \cdot T_s^2}{2L}\Big(2D_3\Phi_2 + D_3^2(\frac{1}{r_V}–1)\Big) \tag{A.11}$$

Thus, replacing (A.7) and (A.11) on (A.2) yields

$$P_{HV} = \frac{V_{HV}^2 \cdot r_S \cdot T_s}{2L}\Big(2D_1\Phi_1 - 2D_3\Phi_2 + (D_1^2 - D_3^2)(\frac{1}{r_V}–1)\Big) \tag{A.12}$$

Finally, considering the power base as

$$P_{base} = \frac{V_{HV}^2 \cdot r_S^2 \cdot T_s}{12L} \tag{A.13}$$

the power per-unit is expressed as

$$P_{HV,pu} = \frac{P_{HV}}{P_{base}} = \frac{6}{r_S}(2D_1\Phi_2–D_3\Phi_2+(D_1^2–D_3^2)(\frac{1}{r_V}–1)) \tag{A.14}$$

A.2 Derivation of P_{LV}

The same procedure can be performed to obtain the average power at the low-voltage port in one cycle P_{LV} if the power losses of the active full-bridge are neglected. Thus, the average power at the ac-link is equivalent to the power delivered to the low-voltage port. The expression of P_{LV} is deducted in (A.15), using (5).

$$\begin{aligned} P_{LV} &= \frac{1}{T_s}\int_{t_0}^{t_0+T_s} v_{L1} \cdot i_L \cdot dt \\ &= \frac{V_{HV} \cdot r_S}{T_s}\Big(\int_{t_1}^{t_2} i_L \cdot dt + \int_{t_2}^{t_3} i_L \cdot dt - \int_{t_5}^{t_6} i_L \cdot dt - \int_{t_6}^{t_7} i_L \cdot dt\Big) \end{aligned} \tag{A.15}$$

Thus, replacing (A.3), (A.4), (A.8) and (A.9) in (A.16) yields

$$P_{LV} = \frac{V_{HV}^2 \cdot r_S^2 \cdot T_s \cdot r_V}{2L}\Big(2D_1\Phi_1{+}2D_3\Phi_2{+}(D_1^2{+}D_3^2)(\frac{1}{r_V}{-}1){-}\Phi_1^2{-}\Phi_2^2\Big) \quad \text{(A.16)}$$

Finally, considering the power base P_{base}, the power per-unit is expressed as

$$P_{LV,pu} = \frac{P_{HV}}{P_{base}} = 6 \cdot r_V(2D_1\Phi_1{+}2D_3\Phi_2{+}(D_1^2{+}D_3^2)(\frac{1}{r_V}{-}1){-}\Phi_1^2{-}\Phi_2^2) \quad \text{(A.17)}$$

Appendix B

RMS inductor current for Trapezoidal Current Mode

In this Appendix the resulting rms inductor current i_L^{rms} as function of the duty-cycles $(D_1, D_3, \Phi_1, \Phi_2)$ is found for all r_V. Also, the particular case where $r_V \approx 1$ is analysed in order to find an alternative and simpler objective function for the NLP.

B.1 General case

The rms inductor current under ZCS trapezoidal current mode in a switching cycle T_s is defined in (B.1). Since the internal addition property of a definite integral i.e. supposing that a point c belongs to the interval [a,b], then the definite integral of a function $f(x)$ over the interval [a,b] is equal to the sum of the integrals over the intervals [a,c] and [c,b], the integral of i_L^2 over the interval $(t_0, t_0 + T_s)$ can be separated in six definite integrals for the intervals (t_1, t_2), (t_2, t_3), (t_3, t_4), (t_5, t_6), (t_6, t_7) and (t_7, t_8). The integral for the resting intervals is null, noticing that the inductor current remains at zero in the intervals (t_0, t_1), (t_4, t_5) and $(t_8, t_0 + T_s)$ if the conditions of ZCS are met.

$$
\begin{aligned}
i_L^{rms} &= \sqrt{\frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_L^2 \cdot dt} \\
&= \sqrt{\frac{1}{T_s}\Big(\int_{t_1}^{t_2} i_L^2 \cdot dt + \int_{t_2}^{t_3} i_L^2 \cdot dt + \int_{t_3}^{t_4} i_L^2 \cdot dt + \int_{t_5}^{t_6} i_L^2 \cdot dt + \int_{t_6}^{t_7} i_L^2 \cdot dt + \int_{t_7}^{t_8} i_L^2 \cdot dt\Big)}
\end{aligned}
\tag{B.1}
$$

Thus, it is possible to find in (B.2) the definite integrals of the square inductor current of the positive semi-cycle considering the ZCS operation under trapezoidal current mode operation, considering the expression for the current i_L

described in (3.34).

$$\begin{aligned}
\frac{1}{T_s}\int_{t_1}^{t_2} i_L^2 \cdot dt &= \frac{1}{T_s}\int_{t_1}^{t_2} \Big(\frac{V_{HV}\cdot r_S\cdot (t–t_1)}{L}\Big)^2 \cdot dt = \Big(\frac{V_{HV}\cdot r_S}{f_s L}\Big)^2 \cdot \frac{\Phi_1^3}{3} \\
\frac{1}{T_s}\int_{t_2}^{t_3} i_L^2 \cdot dt &= \frac{1}{T_s}\int_{t_2}^{t_3} \Big(\frac{V_{HV}\cdot r_S}{L}\Phi_1 T_s + \frac{V_{HV}\cdot r_S\cdot (1–r_V)}{L}(t–t_2)\Big)^2 \cdot dt \\
&= \Big(\frac{V_{HV}\cdot r_S}{f_s L}\Big)^2 \frac{(D_1–\Phi_1)(D_1^2(r_V–1)^2 + D_1\Phi_1(1+r_V–2r_V^2)+\Phi_1^2(r_V^2+r_V+1))}{3} \\
\frac{1}{T_s}\int_{t_3}^{t_4} i_L^2 \cdot dt &= \frac{1}{T_s}\int_{t_3}^{t_4} \Big(\frac{V_{HV}\cdot r_S}{L}\Phi_1 T_s + \frac{V_{HV}\cdot r_S\cdot (1–r_V)}{L}(D_1–\Phi_1)T_s – \frac{V_{HV}\cdot r_S\cdot r_V}{L}(t–t_3)\Big)^2 \cdot dt \\
&= \Big(\frac{V_{HV}\cdot r_S}{f_s L}\Big)^2 \frac{(D_1–D_1 r_V+\Phi_1 r_V)^3}{3r_V}
\end{aligned} \tag{B.2}$$

In the same way, the expressions for the definite integrals of the negative semicycle are deducted in (B.3).

$$\begin{aligned}
\frac{1}{T_s}\int_{t_5}^{t_6} i_L^2 \cdot dt &= \frac{1}{T_s}\int_{t_5}^{t_6} \Big(\frac{–V_{HV}\cdot r_S\cdot (t–t_5)}{L}\Big)^2 \cdot dt = \Big(\frac{V_{HV}\cdot r_S}{f_s L}\Big)^2 \cdot \frac{\Phi_2^3}{3} \\
\frac{1}{T_s}\int_{t_6}^{t_7} i_L^2 \cdot dt &= \frac{1}{T_s}\int_{t_6}^{t_7} \Big(–\frac{V_{HV}\cdot r_S}{L}\Phi_2 T_s – \frac{V_{HV}\cdot r_S\cdot (1–r_V)}{L}(t–t_6)\Big)^2 \cdot dt \\
&= \Big(\frac{V_{HV}\cdot r_S}{f_s L}\Big)^2 \frac{(D_3–\Phi_2)(D_3^2(r_V–1)^2 + D_3\Phi_2(1+r_V–2r_V^2)+\Phi_2^2(r_V^2+r_V+1))}{3} \\
\frac{1}{T_s}\int_{t_7}^{t_8} i_L^2 \cdot dt &= \frac{1}{T_s}\int_{t_7}^{t_8} \Big(–\frac{V_{HV}\cdot r_S}{L}\Phi_2 T_s – \frac{V_{HV}\cdot r_S\cdot (1–r_V)}{L}(D_3–\Phi_2)T_s + \frac{V_{HV}\cdot r_S\cdot r_V}{L}(t–t_7)\Big)^2 \cdot dt \\
&= \Big(\frac{V_{HV}\cdot r_S}{f_s L}\Big)^2 \frac{(D_3–D_3 r_V+\Phi_2 r_V)^3}{3r_V}
\end{aligned} \tag{B.3}$$

Thus, replacing (B.2) and (B.3) into (B.1) yields to

$$\begin{aligned}
i_L^{rms} = \frac{V_{HV} r_S}{f_s L}\Big(&\frac{(r_V-1)^2}{3r_V}(D_1^3+D_3^3) – \frac{r_V}{3}(\Phi_1^3+\Phi_2^3) + \\
&r_V\Big(\Phi_1 D_1(\Phi_1 + D_1(\frac{1}{r_V}-1)) + \Phi_2 D_3(\Phi_2 + D_3(\frac{1}{r_V}-1))\Big)\Big)^{0.5}.
\end{aligned} \tag{B.4}$$

Considering the current base I_{base} as

$$I_{base} = \frac{V_{HV}\cdot r_S}{12 f_s L} \tag{B.5}$$

the rms inductor current per-unit is simplified to

$$i_{L,pu}^{rms} = 12\Big(\frac{(r_V-1)^2}{3r_V}(D_1^3+D_3^3) - \frac{r_V}{3}(\Phi_1^3+\Phi_2^3)+ r_V\Big(\Phi_1 D_1(\Phi_1 + D_1(\frac{1}{r_V}-1)) + \Phi_2 D_3(\Phi_2 + D_3(\frac{1}{r_V}-1))\Big)\Big)^{0.5}. \tag{B.6}$$

B.2 Equivalent objective function for the case $r_V \approx 1$

If $r_V \approx 1$, the square of the rms inductor current per-unit from (B.6) yields to

$$(i_{L,pu}^{rms})^2 \approx 12^2\Big(\Phi_1^2(D_1 - \frac{\Phi_1}{3}) + \Phi_2^2(D_3 - \frac{\Phi_2}{3})\Big) \tag{B.7}$$

which can be expresed as

$$(i_{L,pu}^{rms})^2 \approx (i_{L,pu}^{rms+})^2 + (i_{L,pu}^{rms-})^2 \tag{B.8}$$

if the square of the rms inductor current is separated in the terms of the positive and negative semi-cycle, as is shown (B.9).

$$\begin{aligned}(i_{L,pu}^{rms+})^2 &= 12^2\Big(\Phi_1^2(D_1 - \frac{\Phi_1}{3}))\Big)\\ (i_{L,pu}^{rms-})^2 &= 12^2\Big(\Phi_2^2(D_3 - \frac{\Phi_2}{3})\Big)\end{aligned} \tag{B.9}$$

The same separation can be applied to the power per-unit $P_{LV,pu}$ found in (3.40) when $r_V \approx 1$. Thus, this power could be expressed as

$$P_{LV,pu} \approx P_{LV,pu}^{+} + P_{LV,pu}^{-} \tag{B.10}$$

considering

$$\begin{aligned}P_{LV,pu}^{+} &= 12\left(D_1\Phi_1 - \frac{\Phi_1^2}{2}\right)\\ P_{LV,pu}^{-} &= 12\left(D_3\Phi_2 - \frac{\Phi_2^2}{2}\right).\end{aligned} \tag{B.11}$$

Inspecting (B.9), it is noticeable that these square rms inductor currents could be expressed in terms of the powers per-unit $P_{LV,pu}^{+}$ and $P_{LV,pu}^{-}$, as is shown in (B.12).

$$\begin{aligned}(i_{L,pu}^{rms+})^2 &= 12\Phi_1\Big(P_{LV,pu}^{+} + 2\Phi_1^2\Big)\\ (i_{L,pu}^{rms-})^2 &= 12\Phi_2\Big(P_{LV,pu}^{-} + 2\Phi_2^2\Big)\end{aligned} \tag{B.12}$$

From (B.12) and for constant powers per-unit $P_{LV,pu}^{+}$ and $P_{LV,pu}^{-}$, it is straightforward that the minimal square rms currents are achieved when the phase-

shifts Φ_1 and Φ_2 are respectively minimised. Therefore, the problem of minimise $(i_{L,pu}^{rms})^2$ is equivalent to the minimisation of $\Phi_1 + \Phi_2$ for the case $r_V \approx 1$, reminding that the square rms current $(i_{L,pu}^{rms})^2$ is equal to the sum of the $(i_{L,pu}^{rms+})^2$ and $(i_{L,pu}^{rms-})^2$.

Also, it is possible to analyse the behavior of Φ_1 and D_1 for a fixed power per-unit $P_{LV,pu}^{+}$, finding Φ_1 in terms of D_1 from (B.10). This leads to the expression

$$\Phi_1 = D_1 - \sqrt{D_1^2 - \frac{P_{LV,pu}^{+}}{6}}. \tag{B.13}$$

Thus, it is possible to deduct that the derivate of $\frac{d\Phi_1}{dD_1}$ is always negative, as is shown in (B.14). Hence, the behavior of Φ_1 and D_1 is strictly inverse i.e. as Φ_1 decreases D_1 must increases to obtain the same power. The same conclusion can be obtain for the negative seme-cycle with Φ_2 and D_3.

$$\frac{d\Phi_1}{dD_1} = 1 - \frac{D_1}{\sqrt{D_1^2 - \frac{P_{LV,pu}^{+}}{6}}} < 0 \tag{B.14}$$

Therefore, the minimisation of $\Phi_1 + \Phi_2$ can also interpreted as the maximisation of $D_1 + D_3$. Thus, the objective function of the NLP can be set as (B.15) for the case $r_V \approx 1$.

$$\min_{\Phi_1,\Phi_2,D_1,D_3} J = (i_{L,pu}^{rms})^2 \iff \min_{\Phi_1,\Phi_2} J = \Phi_1 + \Phi_2 \iff \max_{D_1,D_3} J = D_1 + D_3 \tag{B.15}$$

Appendix C

Practical implementation

C.1 Gate signal generation

The pulse pattern required for modulation scheme demand for a highly flexible gate signal generation block. Therefore, the gate signal generation is implemented with finite state machines (FSMs) being executed in the FPGA. This approach allows a precise control of the transition times of the semiconductor devices thanks to the high frequency of the FPGA clock (20MHz).
The gate signal generation block consists of several state machines; one FSM for each half-bridge and H-bridge. The configuration of each FSM is detailed below for both stack modulations and for the H-bridge modulation.

C.1.1 FSMs for the phase-shift modulation

Since the time-controlled phase-shift modulation is defined for a time-window several times the switching period T_s, each pulse pattern incorporates the operation of multiple periods T_s. Thus, for the case of five cells in the stack and $j = 2$, the pulse pattern of each cell switch signals S_{HB_i} is generated by a FSM which sets the gate signal event over the time-window $5T_s$. The implementation of the five half-bridge FSMs is illustrated in Fig. C.1.
To exemplify the operation of the FSMs, the FSM of the first cell is explained below. The initial state of this FSM starts on the colored state (Fig. C.1 above), resetting the time counter, reading the times vector $\boldsymbol{t_i}$ and triggering the upper semiconductor device of the half-bridge ($S_{HB_1} = 1$). Thus, to generate the modulated voltage v_1 (see Fig. 4.3 (b)), it remains in this state until the time counter reach the time t_1, where the state changes to $S_{HB_1} = 0$. In this new state the cell is bypassed, generating zero voltage in its terminals. Three additional transitions succeed next, which are controlled by the times t_5, t_7+2T_s and t_3+3T_s. Finally, when the time counter reaches the whole time-window of the modulation at $5T_s$, the FSM resets the time counter, updates the time vector $\boldsymbol{t_i}$ and start the cycle again.

C.1.2 FSMs for the sorting modulation

The gate signal block for time-controlled sorting modulation in the stack is also implemented using FSMs. The FSM for each cell generates the gate signal event over the time-window T_s, reducing the time-window of the FSM in

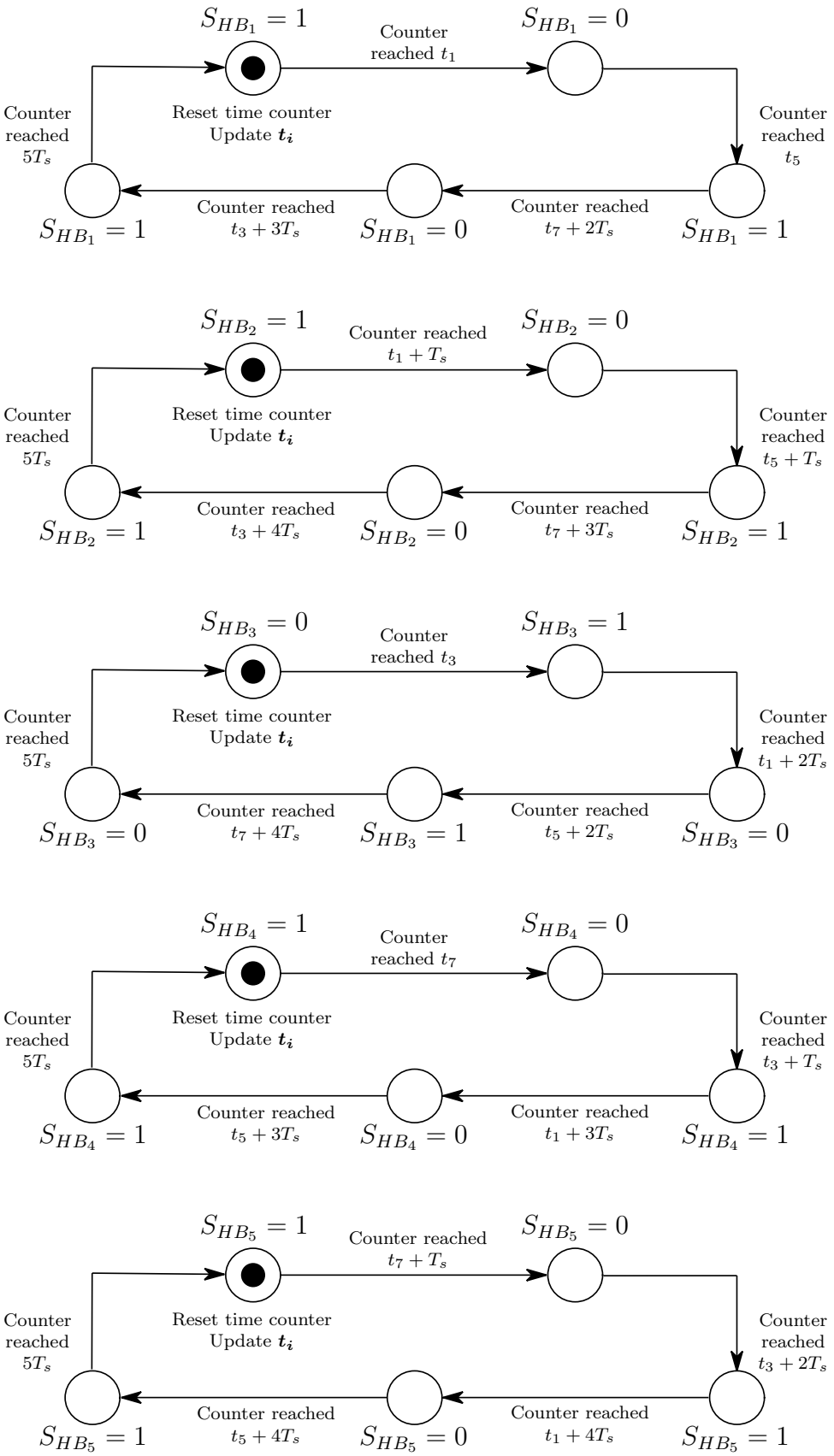


Figure C.1: *Half-bridge finite state machines (FSMs) for the case of five cells in the stack and time-controlled phase-shift modulation with $j = 2$.*

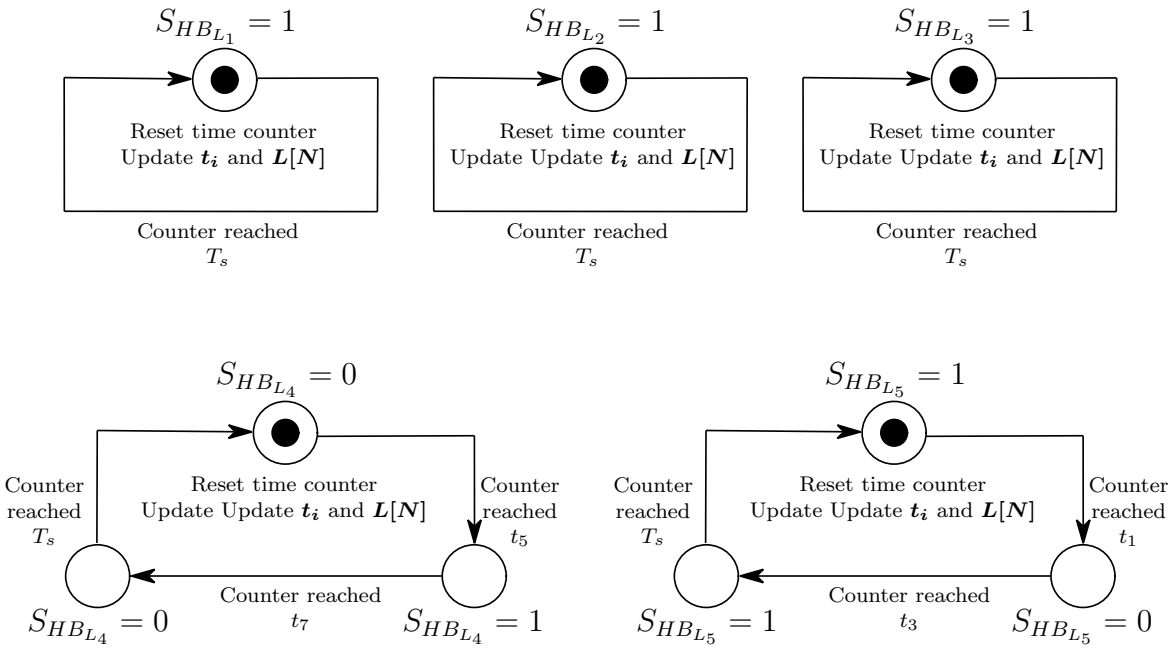


Figure C.2: *Half-bridge finite state machines (FSMs) for the case of five cells in the stack and time-controlled sorting modulation.*

comparison with the phase-shift implementation. Even though the utilization of the cells are unequal in this period, the capacitor voltage balance is assured in a wider time-window due to the sorting algorithm.
The implementation of the FSMs using the sorting modulation is illustrated in Fig. C.2 for the case of five cells in the stack (wave-forms in Fig. 4.4). At the beginning of each cycle, the vector times $\boldsymbol{t_i}$ and the sorted list $\boldsymbol{L}[\boldsymbol{N}]$ are updated, selecting the inserted cells ($S_{HB_{L_1}}$, $S_{HB_{L_2}}$ and $S_{HB_{L_3}}$) and the modulating cells ($S_{HB_{L_4}}$ and $S_{HB_{L_5}}$) identified by the sorting algorithm. Thus, the three FSMs of the inserted cells are kept in state equal to 1 in the whole period T_s (Fig. C.2 above), triggering the upper semiconductor device of the half-bridges, and thus, inserting its capacitor voltage. On the other hand, the modulating cells selected by the sorting algorithm (Fig. C.2 below) are assigned to generate the pulse pattern which results in the desired output voltage. The state of the first modulating cell $S_{HB_{L_4}}$ are controlled by the times t_5 and t_7, whilst the states of the second modulating cell $S_{HB_{L_5}}$ by t_1 and t_3.

C.1.3 FSMs for the H-bridge modulation

The implementation of the FSM for the H-bridge modulation is illustrated in Fig. C.3, considering the times $\boldsymbol{t_j}$ of the modulated voltage v_{L2} (see Fig. 3.10). At the beginning of the cycle, the times vector $\boldsymbol{t_j}$ is updated and the time counter starts. The initial state of this FSM is allocated in the colored state, keeping it in zero ($S_{FB} = 0$). This state by-pass the full-bridge, triggering both upper or lower semiconductor devices in the H-bridge. For a distributed usage of the devices, the zero state is successively interspersed between both cases. The zero state remains until the time counter reaches t_2, where the

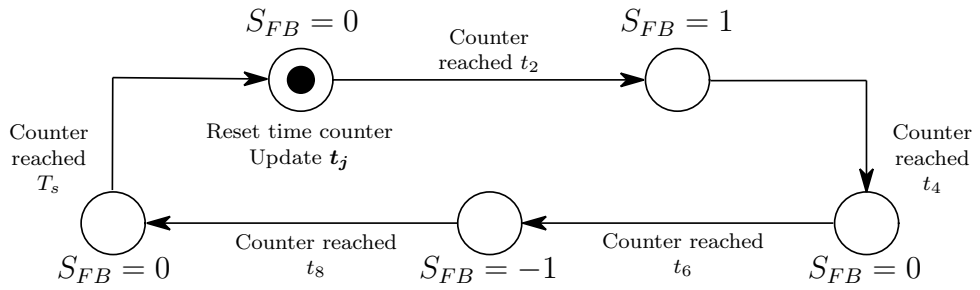


Figure C.3: *Full-bridge finite state machine (FSM).*

state changes. In this new state, the H-bridge insert the capacitor voltage ($S_{HB_1} = 1$). When the counter reaches t_4, the state returns to zero state, by-passing again the full-bridge.
The negative cycle of v_{L2} is modulated next. At t_6, the state of the H-bridge changes to $S_{HB_1} = -1$, inserting the inverted capacitor voltage at its terminals. When the time counter reaches t_8, the state changes to zero state for the last time. Finally, when the time counter arrives to T_s, the FSM resets the time counter, updates the time vector $\boldsymbol{t_j}$ and starts the cycle again.