

Novel Approaches to Modular Multiport DC Power Systems

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Abstract

New trends in radar remote sensing satellites are aiming to implement small, low cost satellites instead of large ones. Radar imaging payloads currently targeting small satellite platforms require peak powers of ≥1kW, whilst the peak power capability of these satellites is at present limited to 100-200W. This calls for new power system designs that meet the new power requirements imposed by these trends, but with a restricted weight/volume budget to fit this platform.

In this research, a novel modular multiport converter (MMPC) is proposed. It enables higher voltage power buses without the need to build PV/battery strings with a large number of series connected cells, which can result in a poor utilization of available PV energy and battery capacity. It also removes the need for additional battery cell/module equalizer circuitry by being able to directly implement energy management strategies that can adapt to different of battery modules. The converter modes of operation, control strategy and design considerations are presented. A 75V/1kW integrated power system prototype is built and tested to validate the proposed concept.

An optimized energy storage system considering a radar imaging payload power profile is also investigated based on different devices (Li-ion batteries, electric double layer capacitors (EDLC) and Li-ion capacitors). A hybrid system consisting of Li-ion batteries/EDLC was found to be the optimal solution considering overall weight and thermal stress on the energy storage devices. However, conventional converters for interfacing the EDLC limit the utilization of its nominal energy capacity to 75% resulting in larger sizes. Therefore, a novel multiport converter that enables maximum utilization of EDLC energy capacity is also proposed. It allowed a 20% size reduction in the EDLC stack for the same energy capacity. Furthermore, a size reduction for the converter inductors could be achieved by a novel interleaved modulation technique proposed. The converter modes of operation, control strategy and design considerations are derived and experimentally validated on the same converter prototype that was reconfigured accordingly.

To my parents

- I owe them everything -

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Contents

Acronyms and Abbreviations viii

List of Figures xi

List of Tables xxii

Chapter 1. Introduction 1

1.1 Motivation for the research project 1

1.2 Project aim and objectives 2

1.3 Achievements and contribution of this thesis 3

1.4 Thesis outline 5

Chapter 2. A Review of Small Satellites Power System Architectures 7

Chapter 3. Power System Modelling 16

3.1 Battery modelling 16

3.1.1 Proposed modelling methodology 18

3.1.2 Energy loss estimation methods 23

3.1.3 Model Validation 27

3.1.4 Simulink® based battery model 37

3.1.5 Model parameters identification for candidate battery cells 38

3.2 Supercapacitor Modelling 40

3.2.1 Equivalent circuit model of SC-cell 40

3.2.2 Thermal model of SC cells 42
3.2.3 Model validation 45
3.3 PV array modelling 48
3.3.1 PV cell modelling 48
3.3.2 Effects of temperature and irradiance 51
3.3.3 PV cell model validation 54
3.3.4 PV-panel modelling 59
3.3.5 Thermal modelling of the PV-panel 60
3.4 Load modelling 64
3.5 Integrated model for satellite EPS 66
3.5.1 Sizing of the PV array 66
3.5.2 Battery sizing 68
Summary 70
Chapter 4. Issues with Batteries and PV Strings 71
4.1 Issues with battery strings 71
4.1.1 Usable capacity of battery packs 72
4.1.2 Charge balancing techniques 73
4.1.3 Alternative battery management techniques 86
4.1.4 Proposed battery system 88
4.2 Issues with PV strings 105

4.2.1 Effects of space environment on PV cells 105
4.2.2 Conventional designs of PV arrays and regulators 109
4.2.3 Proposed designs for PV panels and power regulators 116
Summary 118
Chapter 5. Proposed Modular Multiport Power Converter 119
Introduction 119
5.1 System level analysis of the proposed MMPC 125
5.1.1 Global control of the converter 125
5.1.2 Battery charge balancing range 127
5.2 Proposed MPC topology for power modules 128
5.2.1 Single input, double output operating mode 129
5.2.2 Double input, single output mode 132
5.2.3 Single input, single output mode 135
5.3 Analysis of the proposed MMPC 136
5.3.1 Converter operation and control 136
5.3.2 Converter design analysis 139
5.4 Simulation studies 142
5.4.1 Operation with imbalanced battery-modules 143
5.4.2 Operation with unbalanced PV-modules 146
5.4.3 Operation with peak-pulse loading 148

5.5 Experimental Validation 150
5.5.1 Testing prototype 150
5.5.2 Experimental results 159
Summary 167
Chapter 6. Investigating Optimal Designs for the ESS 168
6.1 Introduction 168
6.2 Re-sizing of power system 168
6.2.1 Resizing of PV array 170
6.2.2 Resizing of battery pack 171
6.3 Designing the ESS based on Li-ion batteries 173
6.3.1 Designing the ESS based on Li-ion energy battery cells 174
6.3.2 Designing the ESS based on power battery cells 178
6.3.3 Designing the ESS based on hybridization of energy & power battery cells 180
6.4 Designing of the ESS based on LIC 183
6.5 Design of an EDLC only based ESS 186
6.6 Design of Battery-Supercapacitor hybrid ESS 188
6.6.1 Design of the Li-ion EB-LIC hybrid ESS 188
6.6.2 Design of the of Li-ion EB/EDLC hybrid ESS 191
6.6.3 Proposed improved Li-ion EB/EDLC hybrid ESS 193
6.7 Comparative analysis 196

Summary 198

Chapter 7. Proposed MPC for HESS 200

7.1 Introduction 200

7.2 The proposed multiport converter topology 202

7.3 Operation of the proposed converter 205

7.3.1 Operation principle of the proposed MPC during the SIDO mode 207

7.3.2 Operation principle of the SITO mode 210

7.3.3 Operation principle of the DISO-I and TISO modes 212

7.3.4 Operation principle of the SISO modes 213

7.3.5 Operation principle of the DISO-II modes 216

7.4 Design of the proposed multiport power converter 217

7.4.1 Selection of input voltages 217

7.4.2 Sizing of the inductors 219

7.5 The control structure of the proposed MPC converter 224

7.6 Evaluation of the proposed MPC by Simulations 226

7.6.1 Evaluating the MPPT for the PV-array 227

7.6.2 Performance of the converter under peak power loads 228

7.6.3 Performance of the converter under PV-power disturbance 230

7.6.4 Operation with Phase-shifted carriers modulation 231

7.7 Experimental evaluation 233

7.7.1 Evaluating the handling of a peak power loading 234

7.7.2 Evaluation of converter operation under load changing 236

7.7.3 Evaluation of converter operation under PV power disturbances 236

Summary 239

Chapter 8. Conclusions and Future Work 240

8.1 Conclusions 240

8.2 Summary of achievements and contribution of this thesis 243

8.3 Future work 245

List of publications 246

References 247

Acronyms and Abbreviations

ADC	Analog-to-Digital Converters
BCDR	Battery Charge Discharge Regulator
BCR	Battery Charge Regulator
BDR	Battery Discharge Regulator
BMS	Battery Management Systems
BoL	Beginning of Life
C2C	Cell-to-Cell
C2S	Cell-to-String
CBS	Centralized Battery Systems
CCBS	Conventional Centralized Battery Systems
CCM	Continuous Conduction Mode
CMBS	Cascaded Modular Battery Systems
CMPC	Centralized Multiport Converter
CMS	Cascaded Modular System
CPE	Constant Phase Element
CRAC	Capacity Requiring Additional Circuitry
CVM	Constant Voltage Mode
DET	Direct Energy Transfer
DISO	Double Input Single Output
DoD	Depth of Discharge
DSP	Digital Signal Processor
DTSC	Double Tiered Switched Capacitor

DUC	Direct Usable Capacity
EB	Energy Battery
ECM	Equivalent Circuit Models
EDLC	Electrical Double Layer Capacitors
EIS	Electrochemical Impedance Spectroscopy
EoL	End of Life
EPS	Electrical Power System
ESR	Equivalent Series Resistance
ESS	Energy Storage System
FFR	Full Frequency Range
FSR	Fixed Shunt Resistor
GUI	Graphical User Interface
IS	Impedance Spectroscopy
LEO	Low Earth Orbit
LIC	Lithium Ion Capacitor
MI	Multi-Inductor
MMPC	Modular Multiport Converter
MOSFET	Metal Oxide Semiconductor Field-Effect Transistors
MPC	Multiport Converter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MSC	Modularized Switched Capacitor
MT	Multiple Transformer
MWT	Multi-Winding Transformer
PB	Power Battery

PDU	Power Distribution Unit
PM	Power Module
PR	Power Regulator
PSB	Power Share Balancing
PSCM	Phase Shifted Carrier Modulation
PV	Photovoltaic
PWM	Pulse Width Modulation
S2C	String-to-Cell
SC	Supercapacitor
SE	Specific Energy
SI	Single Inductor
SIDO	Single Input Double Output
SISO	Single Input Single Output
SITO	Single Input Triple Output
SM	Sub-Module
SoC	State of Charge
SoH	State of Health
SSC	Single Switched Capacitor
SSM	State Space Model
SWT	Single Winding Transformer
TFR	Targeted Frequency Range
TISO	Triple Input Single Output
TPC	Three Port Converter
UC	Usable Capacity
USE	Usable Specific Energy

List of Figures

Fig. 2-1 Sun-regulated DET architecture of EPS 8

Fig. 2-2 Full regulated DET architecture of EPS 9

Fig. 2-3 PV-panel wasted power in DET architecture under specific conditions 10

Fig. 2-4 Full regulated MPPT EPS architecture 12

Fig. 3-1: Curve fitting of battery IS with (a) 2nd order ECM model; (b) Complex model 17

Fig. 3-2: Curve fitting of battery IS within FFR by 3rd order ECM 19

Fig. 3-3: Curve fitting of battery IS with: (a) 3rd order ECM; (b) 5th order ECM 20

Fig. 3-4: Curve fitting of battery IS with a 3rd order ECM within TFR 21

Fig. 3-5: Battery IS at (a) Different temp.at 50% SoC ; (b) SoC (10% to 90%) at temp. 25 ºC 22

Fig. 3-6: 3rd order ECM model for TFR with estimated parameters at 25ºC and 30ºC at 50%SoC 23

Fig. 3-7: Frequency domain based loss estimation 25

Fig. 3-8: Time domain based loss estimation 27

Fig. 3-9: (a) Voltage and energy for the actual battery and the three different models during testing with different load profiles; (b) magnification of one-cycle for each profile 28

Fig. 3-10: 5th ECM error analysis with (a) Evolution of energy loss estimation error and temperature; (b) Battery Re(Z) fitting error and load current profiles spectrum; (c) Energy losses per cycle for the real battery and the 5th order ECM; (d) Re(Z) for the real battery and the model and the load current profiles spectrums. 31

Fig. 3-11: 3rd ECM for FFR error analysis with (a) Evolution of energy loss estimation error and temperature; (b) Battery Re(Z) fitting Error and load current profiles spectrum; (c) Energy losses per cycle for the real battery and 3rd ECM for FFR; (d) Re(Z) for the real battery and the model and the load current profile spectrum. 33

Fig. 3-12: 3rd ECM for TFR error analysis with (a) Evolution of energy loss estimation error and temperature; (b) Battery Re(Z) fitting Error and load current profiles spectrum; (c) Energy losses per cycle for the real battery and the three models; (d) Re(Z) for the real battery and the model and the load current profiles spectrums. 34

Fig. 3-13: Battery versus 3rd ECM for TFR for profile D: (a) Energy loss estimation error; (b) Energy and loss for battery and model..... 35

Fig. 3-14: Battery versus 3rd ECM for TFR energy losses and corresponding errors for: (a,b) Profiles A, B and C;(c,d) Profile D..... 36

Fig. 3-15: Proposed battery model based on 3rd order ECM using Simulink® 37

Fig. 3-16: Curve fitting of IS for Panasonic‘’NCR18650B’’cell within TFR by 3rd order ECM 38

Fig. 3-17: Curve fitting of IS for A123systems ‘’ANR26650 M1-B’’ cell within TFR by 3rd order ECM 39

Fig. 3-18: Electrochemical impedance spectroscopy of SC cell..... 40

Fig. 3-19: ECM of SC cell (a) simplified series RC model (b) higher order model 41

Fig. 3-20: Fitting SC-cell impedance spectroscopy with 5th order model..... 42

Fig. 3-21: Fitting SC-cell impedance spectroscopy with 3rd order model..... 42

Fig. 3-22: EC based thermal model of supercapacitor cell 43

Fig. 3-23: 350F SC-cell electrode and surface temperatures during cycling 44

Fig. 3-24: 350F SC-cell current and voltage during charge/discharge cycling..... 44

Fig. 3-25: Block diagram of the developed SC-cell stress model 46

Fig. 3-26: cycling experiment for the SC-cell for model validation 46

Fig. 3-27: BCAP0150 SC-cell simulation during 2kW power loading of the SC-unit..... 47

Fig. 3-28: Simplified-equivalent circuit of photovoltaic cell. 48

Fig. 3-29: simulated Ipv/Vpv and Ppv/Vpv characteristics of S32 silicon PV cell 51

Fig. 3-30: Irradiance dependence of I_{sc}, V_{oc} and P_{max} at cell Temp. of 25^{o}C [57]..... 52

Fig. 3-31: Characteristics of S32 PV cell under different irradiances at cell temperature of 28^{o}C. 53

Fig. 3-32: Characteristics of S32 cell under different cell temperatures at irradiance of 1350W/m^2 54

Fig. 3-33: model based estimated characteristics of AZURSPACE S32 PV cell under different cell temperatures at constant irradiance of 1350W/m^2. 56

Fig. 3-34: Simulated Ipv/Vpv and Ppv/Vpv characteristics of 3G30C Tj PV cell 57

Fig. 3-35: Characteristics of 3G30C PV cell PV cell under different cell temperatures at an irradiance of 1350W/m^2 58

Fig. 3-36: Simulated Ipv/Vpv and Ppv/Vpv characteristics PV-panel constructed using AZURSPACE S32 PV cells (Ns=100, Np=4). 59

Fig.3-37 : In-orbit positions of satellite PV panels 62

Fig.3-38: Irradiation and PV array temperature within two orbits..... 64

Fig.3-39: Simulation of power consumption of the satellite's subsystems over two orbits..... 65

Fig.3-40: Power profile of radar imaging satellite over two orbits..... 66

Fig.3-41: Power system performance over one orbit..... 69

Fig. 4-1: Capacity mismatch of cells within a battery pack..... 72

Fig. 4-2: battery system architecture of centralized battery system..... 73

Fig. 4-3: Passive balancing techniques with (a) fixed shunt resistors method and (b) switched shunt resistors method..... 75

Fig. 4-4: Single inductor based active balancing technique..... 76

Fig. 4-5: Multi-inductor based active balancing technique..... 77

Fig. 4-6: Pack-to-Cell single winding transformer topology..... 78

Fig. 4-7: Cell-to-pack Single winding transformer topology..... 79

Fig. 4-8: the MWT balancing with: (a) flyback topology (b) forward topology..... 80

Fig. 4-9: Multi transformer based balancing circuit..... 81

Fig. 4-10: Switched capacitors balancing circuit..... 82

Fig. 4-11: Single switched capacitors balancing circuit..... 82

Fig. 4-12: Double-tiered switched capacitor circuit..... 83

Fig. 4-13: MSC balancing circuit..... 84

Fig. 4-14: Converter based balancing system: (a) C2C topology (b) C2S/S2C topology..... 85

Fig. 4-15: Battery system architectures: (a) CCBS (b) CMBS..... 87

Fig. 4-16: Effect of increased M on the DUC and CRAC as a percentage of total capacity..... 89

Fig. 4-17: Step-down topology based CMBS 90

Fig. 4-18: inductance and core size of the inductors in CMBS 93

Fig. 4-19: Estimated equivalent overall copper DC resistance of CMBS inductors..... 94

Fig. 4-20: core/copper weight of each inductor and overall inductor weight in the CMBS 95

Fig. 4-21: R_{DSon} and gate charge for switches for different configuration of CMBS..... 99

Fig. 4-22: Power losses at different configuration of the CMBS..... 100

Fig. 4-23: Overall converter efficiency for different configuration of the CMBS..... 100

Fig. 4-24: Minimum achievable output voltage under partial faults at different designs of CMBS 102

Fig. 4-25: CMBS multi-objective analysis 103

Fig. 4-26: Degradation in I–V characteristics of S32 PV cell under radiation. 106

Fig. 4-27: I-V characteristic of the PV cells from a returned PV panel from ‘’MIR’’ space station: 1,2 standard I-V characteristics; 3,4,5,6,7 – anomalous I-V characteristics [95]..... 107

Fig. 4-28: Safe operating voltage and current criteria for satellite PV strings [12] 108

Fig. 4-29: Construction of a satellite PV-panel/wing..... 110

Fig. 4-30: PV panel configuration..... 111

Fig. 4-31: V-I and V-P characteristic curve of a PV-panel..... 113

Fig. 4-32: Unextracted power from a partially degraded PV-panel for the two regulation options 115

Fig. 4-33: Minimum unextracted power from a partially degraded PV-panel for the two regulation options..... 115

Fig. 4-34: Simulated performance of a PV-panel with partially degraded cells 116

Fig. 4-35: PV-panels and interfacing PRs in: (a) CMS architecture, (b) Centralized architecture 117

Fig. 5-1 Satellite EPS MPPT architectures: (a) Conventional centralized architecture for PV-panels and batteries (b) Cascaded modular based design for PV-panels and batteries 119

Fig. 5-2 Conventional centralized multiport converter based power system 121

Fig. 5-3 EPS based on distributed three port converter as proposed in [122] 122

Fig. 5-4 Proposed modular architecture for satellite EPS based on the proposed MMPC 123

Fig. 5-5. The proposed MMPC architecture 124

Fig. 5-6 Possible MPC topologies (a) Boost-Boost MPC (b) Proposed topology 129

Fig. 5-7 Current flow paths for the operating modes in SIDO mode: (a) Mode I, (b) Mode II, and (c) Mode III. 130

Fig. 5-8 Typical waveforms for SIDO mode for CCM 131

Fig. 5-9 Current flow paths during DISO mode: (a) Mode I, (b) Mode II, and (c) Mode III. 133

Fig. 5-10 Typical waveforms in DISO mode at CCM 134

Fig. 5-11 Block diagram of the proposed MMPC 137

Fig. 5-12 Block diagram for the control strategy of the proposed MMPC 138

Fig. 5-13 Block diagram for the PM voltage local control in the proposed MMPC 139

Fig. 5-14 PSIM based simulation model for the proposed MMPC 144

Fig. 5-15 Simulated operation of the proposed MMPC with unbalanced battery modules: 145

Fig. 5-16 Simulated operation of the proposed MMPC with unbalanced power of PV-modules: 147

Fig. 5-17 Simulated operation of the proposed MMPC with peak-pulse loading: 149

Fig. 5-18 Experimental setup for testing of the proposed MMPC 150

Fig. 5-19 Single power module board 151

Fig. 5-20 Single gate-drive module board 153

Fig. 5-21 schematic diagram for gate-drive circuit of a single MOSFET 153

Fig. 5-22 The FPGA board 154

Fig. 5-23 DSP board with DSK6XXXHPI Daughter-card attached 155

Fig. 5-24 interfacing between FPGA and DSP boards 156

Fig. 5-25 Data acquisition board for a single PM 157

Fig. 5-26 Application circuit of the current transducer 158

Fig. 5-27 Application circuit of the voltage transducer 159

Fig. 5-28 Battery charge balancing with unbalanced PVs power 161

Fig. 5-29 Bus voltage control with/without PVs power 162

Fig. 5-30: Reduction of SoC imbalance of the battery modules under various conditions (PVs power imbalances, load power surges, no irradiance). 164

Fig. 5-31 Operation of the MMPC under partial failure 166

Fig.6-1: Power consumption profile of the satellite subsystems over two orbits 169

Fig.6-2: Power profile of the radar imaging satellite over two orbits 170

Fig.6-3: Ragone plot of various battery technologies with specification at cell level [131]..... 173

Fig.6-4: EIS test based measurement of battery internal resistance for a Panasonic NCR18650B cell used to derive the equivalent model as defined in Chapter 3 (section 3.1.5) 174

Fig.6-5: Simplified thermal model with identified parameters for 26650 cylindrical battery cell 176

Fig.6-6: Simulated performance of the Panasonic NCR18650B cell in normal ground conditions under proposed load power profile over one orbit : (a) cell power (b) cell voltage (c) cell current (d) cell power loss (e) cell surface and core temperatures (f) cell state of charge.. 177

Fig.6-7: EIS test based measurement of battery internal resistance for a A123 ANR26650M1-B cell used to derive the equivalent model as defined in Chapter 3 (section 3.1.5) 179

Fig.6-8: Simulated performance of A123systems (ANR26650M1-B) cell in normal ground conditions proposed a radar type microsatellite load power profile over one orbit: (a) cell power (b) cell voltage (c) cell current (d) cell power loss (e) cell surface and core temperatures (f) cell state of charge. 179

Fig.6-9: Simulated performance of ANR26650M1-B single cell behaviour in an oversized ESS in normal ground conditions under proposed load power profile over one orbit: (a) cell power (b) cell voltage (c) cell current (d) cell power loss (e) cell surface and core temperatures (f) cell state of charge 182

Fig.6-10: Simulated performance of the PB and EB cells in the hybrid ESS in normal ground conditions under proposed load power profile over one orbit: (a) PB/EB cells power (b) PB/EB cells voltage (c) PB/EB cells current (d) PB/EB cells power loss (e) PB/EB cells surface and core temperatures (f) PB/EB cells state of charge 183

Fig.6-11: Schematic diagram of a supercapacitor based ESS..... 186

Fig.6-12: Simulated performance of the LIC and EB cells in the hybrid ESS in normal ground conditions under proposed load power profile over one orbit: (a) LIC/EB cells power (b) LIC/EB cells voltage (c) LIC/EB cells power loss (d) LIC/EB cells surface and core temperatures (e) LIC/EB cells state of charge 190

Fig.6-13: Simulated performance of the EDLC and EB cells in the hybrid ESS in normal ground conditions under proposed load power profile over one orbit: (a) EDLC/EB cells power (b) EDLC/EB cells voltage (c) EDLC/EB cells power loss (d) EDLC/EB cells surface and core temperatures (e) EDLC/EB cells state of charge 192

Fig.6-14: Simulated performance of the EDLC and EB cells in the hybrid ESS with improved EDLC desing in normal ground conditions under proposed load power profile over one orbit: (a) EDLC/EB cells power (b) EDLC/EB cells voltage (c) EDLC/EB cells power loss (d) EDLC/EB cells surface and core temperatures (e) EDLC/EB cells state of charge 195

Fig. 7-1 Power system implemented with (a) separated converters and (b) multiport power converter 201

Fig. 7-2 MPCs structure based on (a) the boost MPC topology and (b) the proposed topology 203

Fig. 7-3 Variation of USE of an SC stack with different design choices for maximum and minimum stack voltages as relative to the constant bus voltage. 204

Fig. 7-4 Illustration of the power flows for all operation modes of the proposed MPC: (a) SIDO mode, (b) SITO mode, (c) DISO-I mode, (d) TISO mode, (e) SISO mode and (f) DISO-II mode. 206

Fig. 7-5 Illustration of the current paths during the different stages of operation of SIDO mode: (a) Step I, (b) Step II, (c) Step III and (d) Step IV. 208

Fig. 7-6 Relevant voltage and current waveforms during SIDO mode. 209

Fig. 7-7 Illustration of the current paths during the different stages of operation of SITO mode: (a) Step I, (b) Step II, (c) Step III and (d) Step IV. 211

Fig.7-8 Relevant voltage and current waveforms during SITO mode 213

Fig.7-9 Illustration of the buck operation of the converter during SISO mode 214

Fig. 7-10 Illustration of the current paths during the different stages of operation of SISO mode: (a) Step I, (b) Step II, (c) Step III and (d) Step IV. 215

Fig.7-11 Relevant voltage and current waveforms during SISO mode 216

Fig.7-12 Interrelation of voltage ranges for the I/O ports of the proposed MPC 218

Fig.7-13 Relevant voltage waveforms for deriving the analytical model of the battery side inductor current ripple at the operation boundaries (A, B, C and D) 221

Fig.7-14 Relevant voltage waveforms for deriving the analytical model of the SC side inductor current ripple at the operation boundaries (A, B, and C) 223

Fig.7-15 Control scheme of the proposed multiport hybrid storage converter 225

Fig.7-16 Simulation model for the proposed converter 226

Fig.7-17 Simulation of MPPT operation of the proposed converter: (a) PV-array available and extracted powers (b) SC-stack voltage (c) PV-array and output voltages (d) PV-array current (e) PV-array temperature (f) Irradiance at the PV-array. 228

Fig.7-18 Simulated performance of the proposed converter under peak power loading: (a) PV-array available and extracted powers (b) PV-stage inductor current and PV-array current at MPP (c) SC-stack, battery and output voltages (d) Battery stage inductor actual and reference currents (e) SC stage inductor actual and reference currents (f) load power. 229

Fig.7-19 Simulated performance of the proposed converter under PV power disturbances(a) PV-array available and extracted powers (b) PV-stage inductor current and PV-array current at MPP (c) SC-stack, battery and output voltages (d) Battery stage inductor actual and reference currents (e) SC stage inductor actual and reference currents (f) load power. 231

Fig.7-20 Simulated performance of the PSCM technique for proposed converter with: (a) 0^{o} phase shift and (b) PSCM technique with 180^{o} phase shift. 232

Fig. 7-21 Experimental setup for validating the proposed converter 233

Fig. 7-22 Experimental results of the proposed converter during peak power loading operation: (a) Battery, SC, output voltages and output current measurements captured from oscilloscope 235

Fig. 7-23 Experimental results during different loading scenarios with: 237

Fig. 7-24 Experimental results during disturbances in PV power captured from the control system: (a) battery, SC-stack, PV emulator and output voltage measurements (b) battery, SC-stack and PV measured currents and their references 238

List of Tables

Table 3-1: 3rd order ECM parameters identified for Panasonic and A123systems batteries..... 39

Table 3-2 3RD ORDER MODEL PARAMTERS FOR SC-CELLS..... 45

Table 3-3: Specified parameters for AZURSPACE S32PV cell [55]..... 55

Table 3-4: Specified parameters for AZURSPACE 3G30C PV cell [16]..... 56

Table 4-1: Converter design parameters..... 91

Table 4-2: CMBS inductor design parameters for different No. of modules..... 96

Table 5-1 Comparison between the MPC topologies..... 136

Table 5-2 Experimental setup specifications..... 152

Table 6-1: Details of the power consumption of the different subsystems during one-orbit.... 170

Table 6-2: Details of the power consumption of the different subsystems during eclipse over one-orbit..... 172

Table 6-3: Conceptual design parameters for a LIC only based ESS..... 185

Table 6-4: Conceptual design parameters for the EDLC based ESS..... 187

Table 6-5: Conceptual design parameters for LIC pack used in the EB-LIC hybrid ESS..... 189

Table 6-6: Conceptual design parameters for EDLC stack used in the EB-EDLC hybrid ESS 191

Table 6-7: Different designs for EDLC-part of the EB-EDLC hybrid ESS..... 194

Table 6-8: Specifications of the ESS based on different designs..... 198

Table 7-1 Analytical formulas for the peak-to-peak current ripple in the battery side inductor (L2) at the boundaries of the operating range with and without using the PSCM technique ... 220

Table 7-2 Analytical formulas for the peak-to-peak current ripple in the SC side inductor (L1) at the boundaries of the operating range with and without using the PSCM technique 222

Table 7-3 Technical specification of the experimental setup..... 234

Chapter 1. Introduction

1.1 Motivation for the research project

New trends for remote sensing satellites with integrated radar imaging payloads aim to replace the conventional large satellites that weight a few tons and are therefore costly to build and launch [1] by employing a constellations of low cost small satellites. This approach can significantly reduce the development and launching costs and improve the temporal performance of the observation systems, enable fast acquiring of information in response to a sudden crisis occurring on various geographical scales [2-6]. However, these smaller satellites have reduced weight/volume budget available for these kind of payloads as well as reduced capabilities to power them. This calls for new design solutions for the different systems installed on this satellite platform in order to fulfil the increased power requirements for these missions at a minimum added weight/volume. Among the different systems integrated in a small satellite platform, the power system, which consists of photovoltaic (PV) array as a primary energy source and batteries as secondary energy source as well as power conditioning circuitries, can represent up to 25% of the overall weight of these satellites [7, 8]. Additionally, under large peak power pulses required for supplying the radar imaging payload, may reach 10-20 times larger than the average power consumptions of these satellites platforms [2, 9, 10], the weight/volume of the power system will increase significantly. This is because the area to be occupied by the PV array and its associated power generated is limited by the available area limited by the satellite size, which means that the energy storage system should supply the power deficit during these large load power peaks. This requires high discharging power from the battery that may shorten its lifetime which will demand either utilization of high specific power (W/kg) batteries that usually have lower specific energy (Wh/kg)[11], or oversizing the stack of high specific energy battery cells due to their limited power capability [11]. These two options can result in a heavier battery pack which contributes to the increase of the overall

weight/size of power system. Finally, the higher power requirements imposed by the radar imaging payload calls for higher voltage buses for these satellites (currently these are using the 28V power bus) in order to minimize the power loss for power distribution which may enable reduction of the cross-section of cables/harness and weight. This in turn requires battery packs and PV-panels with higher rated voltage to be able to interface efficiently with a high voltage power bus. Design of battery packs with high voltage requires a series connection of large numbers of battery cells. This increases the complexity of the cells' balancing/equalization system required for battery systems to handle the expected battery cells mismatch which also contributes to additional weight. On the other hand, increasing the voltage of the PV panels requires strings with large number of series connected PV cells. This results in poor utilization of the overall available PV power due to limitations imposed by the weaker PV cells affected by different levels of degradation. Also, increasing the voltage of the PV panels increases the risks of sustained arcs that may damage the PV-cells [12, 13] or the wire harness of the PV-panel as suggested for some failed missions [14, 15]. All these challenges together justify the need for modular architectures for the power system used in small satellites, which can be customized according to a variety of mission requirements with minimal redesign to reduce the time and cost of development. These are the reasons why the research in this thesis is aim to propose novel solutions towards designs of power system for small satellites.

1.2 Project aim and objectives

Based on the challenges identified in the previous section, this research project aims to develop a new modular architecture for the satellite electrical power system that enables: weight minimization, modular structure as well as inherent fault tolerant operation. The objectives of the research work to be addressed in this thesis in order to achieve this aim are as follow:

1. Review the existing research toward improving the design and performance of small satellites power systems.

2. Investigating the different design options for the energy storage system (ESS) of small satellites considering the typical power requirements of radar imaging payloads that are desired to be integrated in this satellite platform. Architectures based on Li-ion batteries, electric double layer capacitors (EDLC) and lithium-ion capacitors (LIC) will be investigated by considering the overall weight and lifetime of the ESS as well as thermal stress of utilized energy storage devices.

3. Propose a novel integrated converter topology for interfacing PV-panels and ESS with the power bus. The modular structure of the converter in conjunction with appropriate battery modules management strategies that eliminate the need for conventional battery cell balancing circuitries allowing further weight/volume reductions, and also enable better utilization of PV-panels available power that can facilitate further size reduction of the PV array.

- Validate the proposed converter topology through simulation modelling.
- Build an experimental prototype for an integrated power system including the proposed converter to validate the benefits of the concept.

1.3 Achievements and contribution of this thesis

i) The development of a novel methodology for developing accurate power loss models for battery and supercapacitor cells at reasonable complexity of the models. The current models either are based on complex electrochemical models or the models are too simple having a reduced accuracy. The developed models based on this methodology can achieve good accuracy for

estimating the power loss that is then used to evaluate the thermal stress of the battery and supercapacitor cells accurately for a given load power profile.

ii) The Development of a novel multiport converter with modular architecture for photovoltaic/battery based power systems which significantly improves the utilization of available PV energy and battery capacity as it does not uses a high number of series connected PV and battery cells in a single string but rather utilises multiple modules. This approach also removes the need for additional battery cell/module equalizer circuitry used in conventional systems to handle a limited capacity mismatch between battery cells. The proposed converter can be also a promising solution for terrestrial applications for large scale PV/battery based power systems. Furthermore, it can handle large mismatch between battery cells (enable the use of wide variety of second life batteries) and also large mismatch in PV-panel powers so that different panels at different orientations can be easily interfaced allowing maximum utilization of the available space (i.e. different roof surfaces with different sun orientations) for installing PV panels.

iii) The development of a novel multiport converter for integrating to a power bus photovoltaic array and hybrid energy storage system, which consists of battery and supercapacitor stack. The current converter topologies interfacing supercapacitor stack to the power bus through a voltage boost-stage limit the utilization of its available energy capacity due to the limited operating voltage range of the stack. The proposed converter provides buck-boost operation for the supercapacitor stack that enables the extending of the voltage range of stack maximising the utilization of the nominal energy capacity of the cells which reduces the size of the stack for the same energy stored.

1.4 Thesis outline

The second chapter presents a literature review for a few solutions shortlisted for further investigation that aiming to improve small satellites power system.

The following chapters in the thesis present the conducted research towards achieving the further project objectives and are structured as follow:

In Chapter 3, modelling of different elements in the power system including the PV-array, the battery, and the supercapacitors are presented. The development of power loss models for battery and supercapacitor cells with good accuracy and reasonable complexity are proposed and validated. The development of a thermal model for supercapacitor cells based on the developed power loss model is also presented and validated. Finally, the models of different elements are combined for simulating the operation of the power system.

In Chapter 4, the problems related to battery and PV-panels for higher voltage power buses considering the conventional architectures of small satellites power systems are investigated. Conventional mitigation techniques for battery related problems and their limitations are discussed and a proposed modular architecture is investigated considering the interfacing converter efficiency, the complexity and the fault tolerant operation in conjunction with the better utilization of battery overall capacity. The modular architecture of PV-panels has also been investigated considering the converter parameters and the better utilization of the available power under uneven degradation levels for the PV cells.

In Chapter 5, a novel modular multiport converter (MMPC) is proposed to enable the implementation of a modular structure for battery and PV-panels. The added features compared to the ones offered by conventional multiport converters are presented. The operation of the proposed converter topology and its related control strategies are discussed. Simulated operation of the proposed converter under various conditions is presented. Finally, a 75V/1kW integrated

PV-battery power system experimental prototype implementing the proposed converter topology is built to validate the concept and the experimental results are presented.

In Chapter 6, the different design options for the energy storage system are investigated based on the radar imaging payload power requirements by considering Li-ion batteries, electric double layer capacitor and lithium-ion capacitors as the available energy storage devices. The overall weight of the energy storage system and the thermal stress on the candidate devices under the different designs are assessed by using the models developed in Chapter 3.

In Chapter 7, a novel multiport converter topology derived from the proposed MMPC is proposed for interfacing the PV-array and the battery/supercapacitor hybrid energy storage system to the power bus. The added features offered by the proposed converter compared to the available topologies are discussed. The converter operation and the system level control are presented. Operation of the converter under various conditions is demonstrated through simulations. Finally, a 30V/0.5kW integrated power system based on PV and battery/supercapacitor hybrid energy storage experimental prototype implementing the proposed converter topology is built to validate the concept and experimental results are presented.

In Chapter 8, the conclusions on the presented work and summary of the contributions of this thesis are presented and the future improvements are summarised.

Chapter 2. A Review of Small Satellites Power System Architectures

A satellite consists of various systems that are designed to meet the mission requirements. These systems can be classified into two main groups, the payload and the platform. The payload consists typically of imaging equipment for remote sensing satellites, communication equipment used in communications satellites or science instruments as needed by research satellites. The platform consists of all the remaining equipment grouped into several functional systems that support the payload. Essential platform systems are including: (i) communications and data handling systems performing the required communication with the ground stations, (ii) telemetry sensors for monitoring of satellite states, (iii) a central computer coordinating the control activities of all the systems and (iv) the electrical power system that captures the necessary energy and supplies the required power for all systems on-board the satellite, some consuming constant power, whilst others consume pulsed power as needed by the operational routine.

The electrical power systems (EPS) in small satellites primarily consists of a PV array (made of several PV cells integrated in a number of panels/wings) as a primary energy source, a rechargeable battery as a secondary power source and a power regulator which regulates power flow between various EPS components to control the bus voltage. Recent advances in photovoltaic cell and battery technologies have led to significant improvement in power systems. The development of triple junction cells that have significantly improved conversion efficiency of sunlight (above 30% [16, 17]) which started to gain real work experience of deployment in space led to significantly improved specific power (kW/kg) of the PV-arrays and hence weight reduction for a given energy requirement. Also, the implementation of Li-ion batteries that have higher specific energy (120-150Wh/kg) instead of Nickel-Cadmium and

Nickel-Metal Hybrid batteries with lower specific energies (60-100 Wh/kg), led to further reduction of battery weight/volume for a given stored energy requirement. However, further developments in the performance of solar energy capturing and storage cells/components rely on the development of new materials; therefore it is beyond the scope of this research.

Other developments that are related to the structure of the power system have been proposed, under which the power system can be classified into two architectures, the direct energy transfer (DET) architecture and the maximum power point tracking (MPPT) architecture. In the DET architecture, the power from the PV-panels is transferred directly to the power bus without any series power regulators in-between. This architecture is subdivided into two topologies, the sun-regulated and the full regulated buses. In the sun-regulated bus topology shown in Fig. 2-1[18], the bus voltage is being regulated during the sun-duration of the orbit using the battery charge regulator (BCR) to regulate battery charging power and the shunt dissipater is used to dissipate the surplus power that exceeds the load and the battery charging power requirements. However, during an eclipse, as the battery is directly coupled to the power bus through a blocking diode (that preventing any un-controlled charging of the battery), the bus voltage is un-regulated, and decreases as the battery discharges.

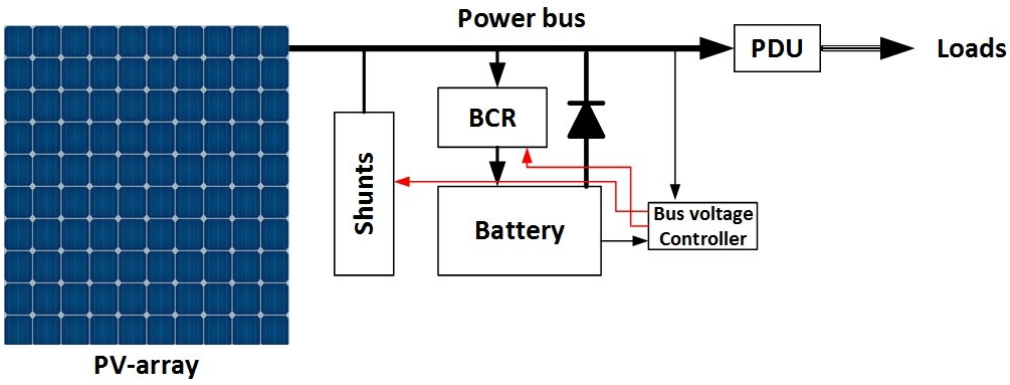


Fig. 2-1 Sun-regulated DET architecture of EPS

The second topology of the DET architecture is the full regulated bus (Fig. 2-2) [18] in which the bus voltage is being regulated during the full orbit (sun and eclipse durations). In this topology, the battery interfaces to the power bus through a battery charge/discharge regulator (BCDR) which enables the regulation of the bus voltage also during the eclipse by adapting its duty cycle according to the change in battery voltage as it discharges, whilst the regulation of the bus voltage during the sun-duration is achieved by the shunt dissipater in the same way as with the sun-regulated topology.

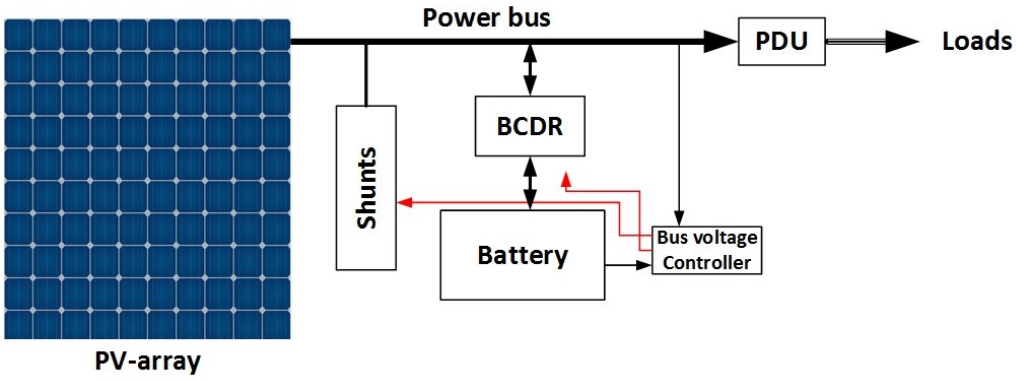


Fig. 2-2 Full regulated DET architecture of EPS

The full regulated bus topology of the DET architecture offers several advantages over the sun-regulated bus topology that include:

- Lightweight load converters with higher efficiency, since they are supplied from a constant voltage power bus.
- Lighter power distribution wires/harness due to lower currents needed for a constant bus voltage, whilst heaver wires/harness are required to carry the higher current needed at the minimum voltage in the sun-regulated bus topology.
- Reduced size of the PV-array due to not having battery latch-up problems occurring due to direct coupling of the battery to the voltage bus in the sun-regulated topology. The way this happens is that the lower battery voltage at eclipse exit is forcing a lower

power extraction from the PV-array which may not be enough to supply the required load power causing the battery to further discharge instead of charging. In order to avoid this problem, the PV-array has to be oversized by 10% or more depending on the PV- array and battery characteristics [18].

The PV- array produces variable output power due to variable irradiance/temperature over the orbit as well as performance degradation due to space environment over the years of mission. This makes DET topologies unable to maintain maximum utilization of the PV-array available power under these variable conditions whilst keeping the bus voltage regulated that results in wasted power as demonstrated in Fig. 2-3 based on the developed PV panel model described in Chapter3 considering PV panel temperatures of -60°C for the cold state and +60° for the hot state and 30% reduction in the performance of the PV panel at end of life (EoL) compared to its performance at beginning of life (BoL).

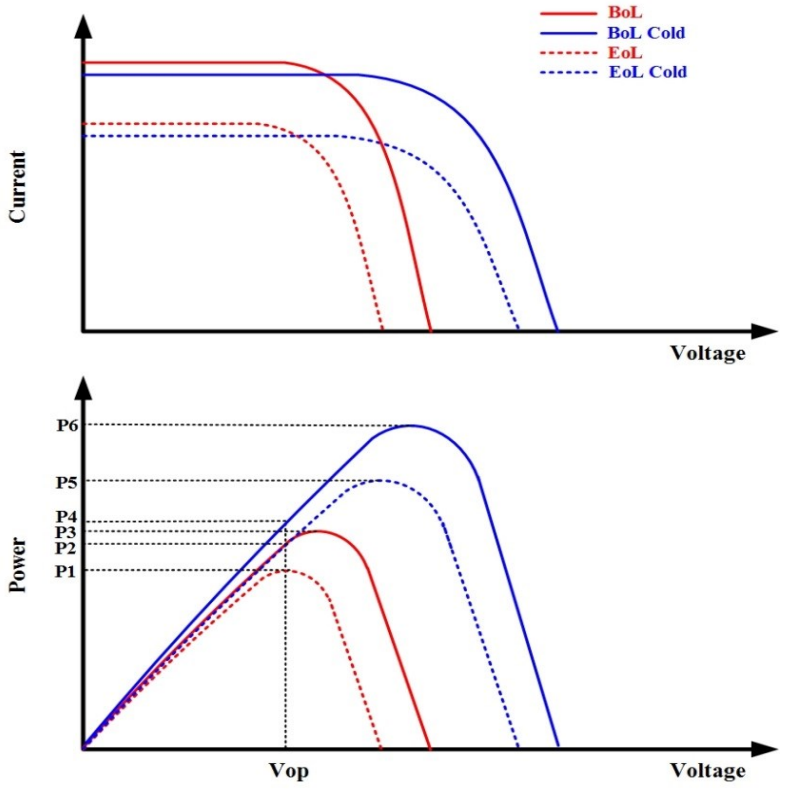


Fig. 2-3 PV-panel wasted power in DET architecture under specific conditions

It can be seen that at a regulated bus voltage of V_{op}, whilst the PV-panel sized to deliver its required power considering the EoL characteristics (despite oversizing for reliability purposes), the wasted power at EoL when the PV-panel is cold for several minutes just after a return from eclipse will be (P_5-P_2). This wasted power can increase the extracted energy from this panel over the sun-duration of the orbit by up to12% (depending on the characteristics of the utilized PV cell) if it is captured which can enable size reduction of the PV panel by the same ratio. The powers wasted at the BoL hot condition (P_3-P_2), and cold conditions (P_6-P_4), have to be wasted anyway as the PV-panel has to be sized considering EoL characteristics. However, if these extra powers can be captured as well, it can be considered as a reserve power that can be used to compensate for partial failures or unexpected degradation in the overall array performance that can eliminates the need for oversizing for reliability purpose allowing for further reduction in PV array size. As it can be observed, the need to waste power from the PV-array in DET architectures can result in oversized PV-array which may cause additional disadvantages at the spacecraft level [18] including additional drag that increases the burden for the attitude control system.

Some research has been conducted to improve the DET architecture by adapting the shunt regulator topology to track the maximum power point of the PV panels ensuring the extraction of maximum available power [19-25]. However, due to the large change in PV-panel temperature and consequently the voltage over the low earth orbit (LEO), tracking of maximum power point under regulated bus voltage may not be always be achievable. Accordingly, the DET architecture has to either clamp the higher voltage available when the PV panels are cold for several minutes after return from eclipse [19] causing a power waste as described earlier, or to allow the bus voltage to change to allow tracking of the maximum power point which will result in an unregulated bus voltage and accordingly additional power electronic circuitries will be needed to achieve a regulated bus or load voltage [24, 25].

MPPT is the other option for the satellite EPS architecture [26-33] which inserts a series switching regulators between the PV-panels and the power bus as shown in Fig. 2-4.

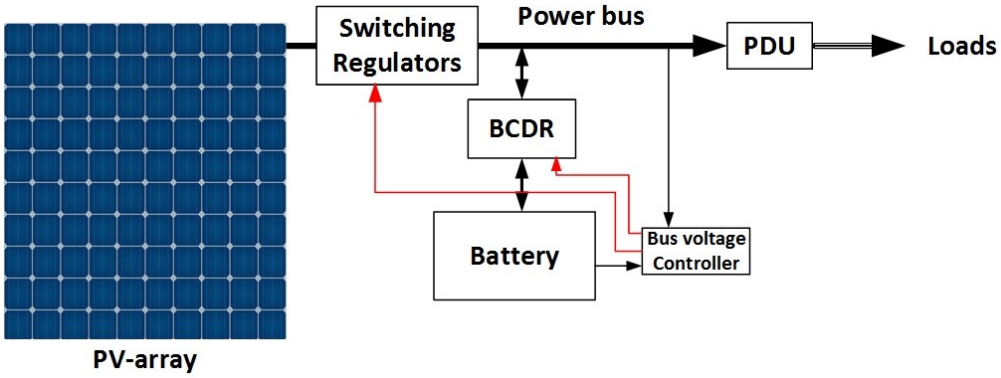


Fig. 2-4 Full regulated MPPT EPS architecture

As described earlier, the PV-array panels generate more power at higher voltage at the BoL, when these are cold as the satellite is coming out of an eclipse. Accordingly, for a constant bus voltage, the series switching regulator allows adapting the voltage of the PV panels to operate at maximum power point (MPP) for extraction of maximum power. However, at a reduced load and battery power demand (battery is charged), the regulators force the PV panels to operate away from MPPs and the excess power is left un-extracted from the PV-array panels that causes the raising of their temperatures.

The main advantages of the MPPT architecture are: it enables the maximum utilization of the available PV power all the time, and it does not require the shunt dissipater. However, it has lower conversion efficiency compared to the DET architecture due to the additional power losses in the series switching regulators. Moreover, since these losses are dissipated inside the spacecraft body, it may negatively impact the thermal control system. Furthermore, the passive components required for the switching regulators in the MPPT architecture can represent added weight for the EPS. However, development of an enhanced topology for the switching regulator that achieves reduced size of the passive components and better efficiency can enable the

implementation of a superior MPPT architecture to achieve size reduction in the PV-array without added penalties to the EPS in terms of weight and efficiency. The implementation of compact power electronics in the form of multiport converters for interfacing the PV-array with a battery and the power bus using a MPPT architecture of EPS as proposed in [34-36] can also allow further reduction in size/weight of the interfacing converters.

Although the MPPT architecture of the EPS has obvious advantages over the DET architecture, both architectures typically utilise a centralized battery which has to be designed to match the voltage of the power bus in order to achieve a high efficiency of the BCDR. This in turn requires the series connection of a large number of battery cells, especially when a high voltage power bus (≥100V) is considered. Accordingly, the complexity of the battery cells balancing/equalization circuits that are utilized in these types of EPS architectures to handle the mismatch between cells, will be increased significantly resulting in added weight. The PV-panels in these architectures are also required to be designed at the voltage of the power bus to achieve a higher efficiency for the interfaced regulators. This also requires series connection of a large number of PV-cells. In cause of a failure or weakness introduced to a number of PV cells within the panel, which is more likely in a high voltage design due to larger numbers due to uneven degradation, this may result in a poor utilization of the available power from these panels. Also, increasing the voltage of the PV panels increases the risks of sustained electrical arcing that may cause damage to the PV-cells or the wire harness of the PV-panels. The centralized structure of the switching regulators (each PV-panel interfaces the power bus through central regulator) reduces the fault tolerance range for the EPS, as the failure of a single regulator causes the interfaced PV-panel, which may supply 25-35% of EPS power, to become unusable. This problem can be addressed by implementing redundancy as proposed in [36], but with the cost of added weight to the EPS, whilst the problems described related to PV and battery remained.

Improving the ESS for the satellite EPS has been investigated by other researchers considered the EDLC and the LIC as alternatives to the Li-ion batteries. In [37], the design of the ESS based on EDLC has been investigated considering its higher specific power and longer lifetime even when subject to a higher depth of discharge (DoD). However, it required changing of the working duty cycle of the imaging period in order to reduce the size of the ESS, which reduces the capability of the payload. In [38], the design of an ESS based on LIC has been investigated considering its longer lifetime at higher DoD that can achieve comparable weight to a Li-ion battery based ESS if certain considerations including the use of lower specific energy batteries (150Wh/kg) and a DET architecture for the power system are taken into account. However, additional considerations must be included for a better comparison that includes the use of a MPPT architecture of the power system and higher specific energy batteries (250Wh) which are now commercially available [39]. A hybrid ESS based on the use of both batteries and EDLC has been investigated in [9] to achieve high specific energy and high specific power for the energy storage system to be able to support pulsed operated payloads with high power requirement. This approach can provide great advantages in terms of weight/volume reduction as well as improving robustness of the system, as the EDLC can operate over a wide temperature range (-40ºC to +70ºC). However, the weight/volume reductions are highly dependent on the power profile, i.e. as the duration of the high power pulse increases, the required energy capacity of the EDLC-part of the ESS (that has lower specific energy) will increase resulting in a significantly increased overall weight and causing other ESS designs based on an energy battery alone or energy battery/power battery hybrid (as proposed in [4]) to be more beneficial in terms of weight/volume reductions. LIC can be used in conjunction with a battery in a hybrid ESS due to its higher specific energy (compared to EDLC), as proposed in terrestrial applications [40], that might achieve further weight/volume reductions for the ESS. However, for reduced duration high power pulses, the energy requirements from the LIC part of

the ESS reduces. This results in the utilization of LIC cells with smaller capacity that might be subjected to significant power stress during these power pulses affecting their lifetime.

Therefore, the optimal design of the ESS should be investigated based on the specific mission power profile considering not only the weight reduction of the ESS but also the thermal stress on the potential energy storage devices.

In conclusion, the current EPS structures of small satellites which are based on either DET or MPPT architectures, use a centralized battery and PV panels designed for the full voltage of the power bus which results in poor utilization of PV available energy and battery capacity, especially when a higher bus voltage is considered (these issues will be investigated in detail in Chapter 4). However, a fault tolerant battery system based on the cascaded modular structure of the battery system that improves the reliability of the battery system and eliminates the need for conventional cell voltage balancing circuitry as needed in centralized convention systems has not as yet been investigated. Also, optimizing the design of the energy storage system considering the overall weight and the thermal stress of the energy storage devices for a specific load profile based on utilization of state of art energy storage devices has not as yet been investigated.

This research aims to investigate the development of a novel power converter that enable the target modular structure for the EPS and investigate the benefits and limitations associated with the different components of the EPS including PVs and energy storage systems sizing that can help address some of these gaps.

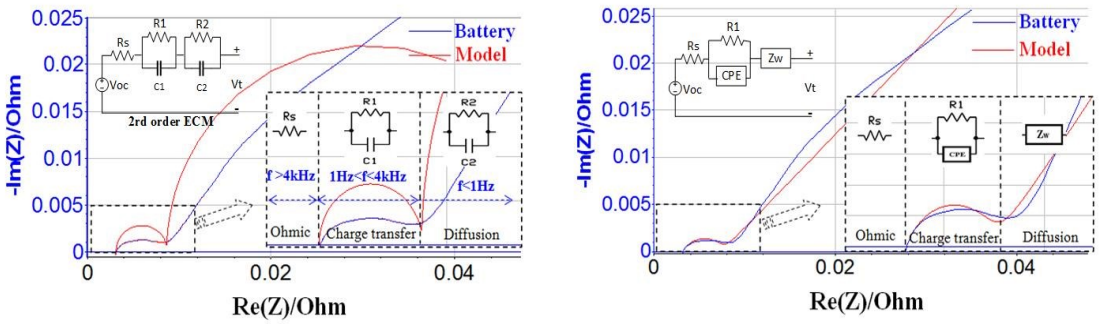
Chapter 3. Power System Modelling

In order to evaluate the operation and performance of the proposed satellite EPS under different designs, it is required to have models for the different parts of the EPS including the batteries and PVs as well as the supercapacitors that will be used in conjunction with the battery in hybrid energy storage system proposed in Chapter6. The models should have a reasonable accuracy especially for batteries and supercapacitors as they used to evaluate the thermal stress on the battery and supercapacitor cells to evaluate the performance of different designs of the energy storage system. This chapter investigates the methodologies for developing these models and their validation. The results from the proposed modelling methodology for battery and supercapacitor have been published in EPE 2016 and ESARS-ITEC 2018 conferences [41, 42].

3.1 Battery modelling

Accurate battery power loss estimation requires accurate information regarding battery internal resistances which is usually available in datasheets for specific frequencies and temperature; however the resistances change significantly with frequency and temperature. In addition the high frequency resistance which can be measured online through measuring transitions of battery voltage that corresponding to transitions in current, is also small compared to the actual resistances at low frequencies, and therefore a model that is able to better represent battery dynamics is required to accurately describe battery behaviour. Equivalent circuit models (ECM) for batteries are widely used with battery management systems (BMS) instead of electrochemical models due to their simplicity and ease of implementation; however the simplicity of the ECM usually results in low accuracy. There are many ECMs that have been proposed for representing battery dynamics starting from simple resistor models to represent

battery internal resistance, up to more complex models with constant phase elements [43-46]. Among the different ECMs, the 2nd order RC model (Fig. 3-1 (a)) is widely used for modelling battery dynamics as it is considered to be closer to the physical principles of battery operation. It utilizes a series resistance R_s to represent battery ohmic resistance and two R//C branches, one to represent the charge transfer process and the other to represent the diffusion process. Although this model is considered to be simple, it does not have sufficient accuracy to fit battery impedances measured through electrochemical impedance spectroscopy (EIS) experiments as can be seen in Fig. 3-1(a). The EIS experiment was made for a 8Ah LiFePo4 battery cells at the an ambient temperature of 25°C using Biologic SP-150 Potentiostat. As it can be seen, large errors can be observed between the measured battery impedances (blue line) and the model impedance (red line) because the Nyquist plot of the battery impedance spectroscopy (IS) has a depressed semicircle within the frequency range of the charge transfer process (1Hz<f<4 kHz) that cannot be modelled accurately by a single R//C branch. Also the plot shows a behaviour similar to the Warburg impedance [47, 48] within the frequency range of the diffusion process (1mHz<f<1Hz) that also cannot be modelled accurately by a single R//C branch.



(a) (b)

Fig. 3-1: Curve fitting of battery IS with (a) 2nd order ECM model; (b) Complex model

A complex model can be obtained by replacing the simple capacitor of the $R_1//C_1$ branch representing the charge transfer process by a constant phase element (CPE) to accurately fit the

depressed semicircle of the impedance plot, as well as replacing the $R_2//C_2$ branch by Warburg impedance to enhance the fitting accuracy as shown in Fig. 3-1b[46, 47]. However, due to the complex mathematical modelling of CPE and Warburg impedance the resulted battery model will be more complex. Many attempts have been made to improve the accuracy of modelling especially for the diffusion process. Some methods use a constant phase element and hence a fractional order model [45, 46]; other modelling techniques use an unlimited chain of RCs to represents the Warburg impedance, trying to approximate by a finite number N (suggested as 5 in [48]). Although these modelling techniques achieved a good accuracy, it extended the model complexity that might be inappropriate if low cost microcontrollers are considered for the BMS.

3.1.1 Proposed modelling methodology

The accurate estimation of energy loss requires a model that is able to fit battery IS data accurately especially for the real part. The proposed model will be developed by fitting battery IS data using curve fitting techniques targeting a good accuracy. Simple R//C branches are used for the ECM for the battery and the methodology described in [49] is adapted to fit the of the real part of the battery IS with a 3rd order RC model to the full frequency range (FFR) of (1mHz to 4kHz).

In order to simplify the fitting process, the given frequency range of the IS data, obtained by the EIS experiment using the Biologic SP-150 Potentiostat for 8Ah LiFePo4 battery cell at ambient temperature of 25ºC, has been divided into six bands from A to F as shown in Fig. 3-2. Model parameters can be estimated simultaneously by considering the elements of the ECM which dominate in each band and hence the ECM for each band as shown in Fig. 3-2. The principle of constructing the ECM for each band is that at very low frequencies (less than 1mHz) all capacitors of the model have infinite reactance and can be considered as an open circuit. As the frequency increases and moves to band A, capacitor C3 starts to conduct where C1 and C2 are

still considered open circuit, so the ECM is an RC branch of R3//C3 in series with a resistance of (Rs+R1+R2). A similar analysis is made for all other bands (B to F).

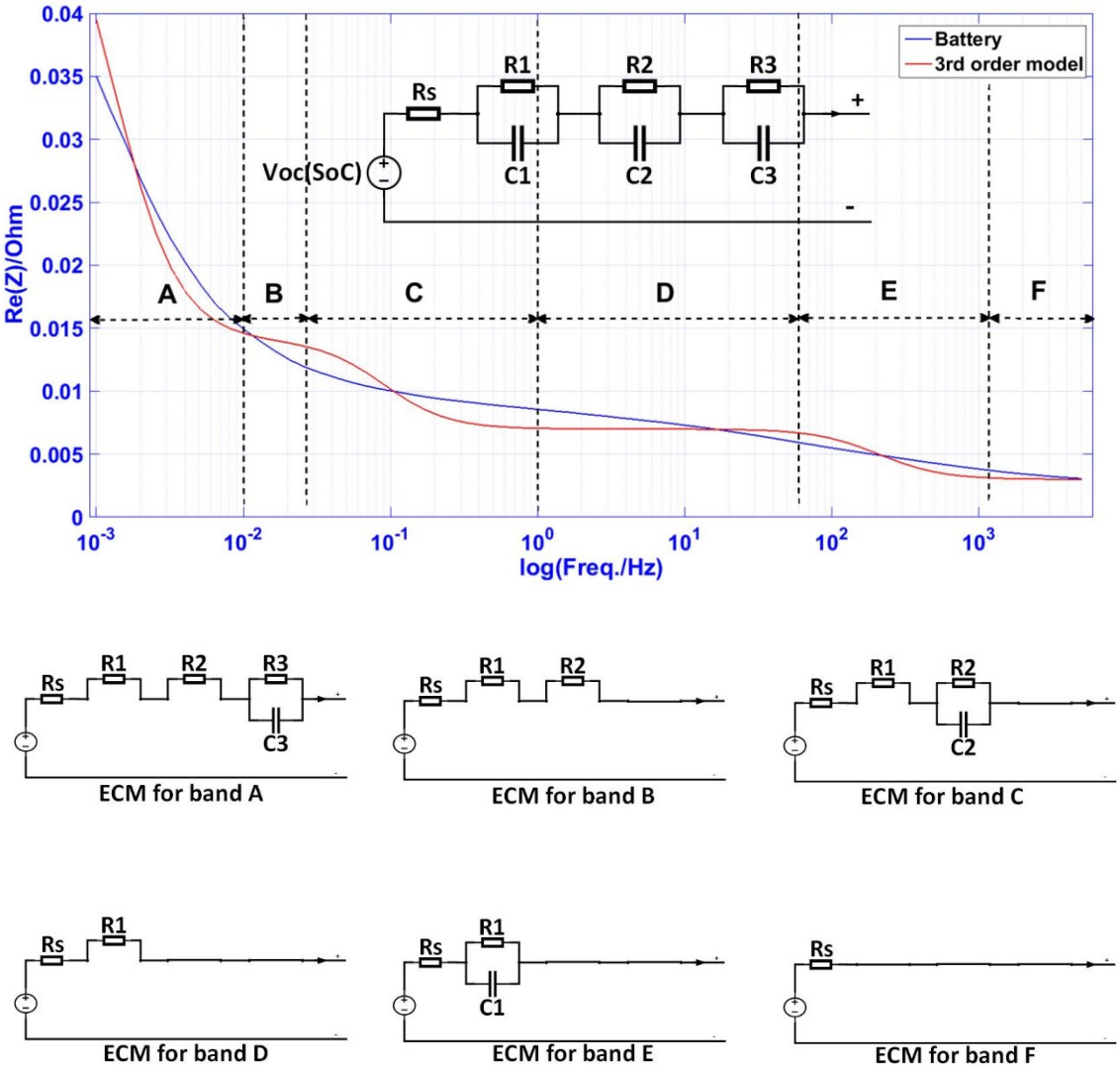
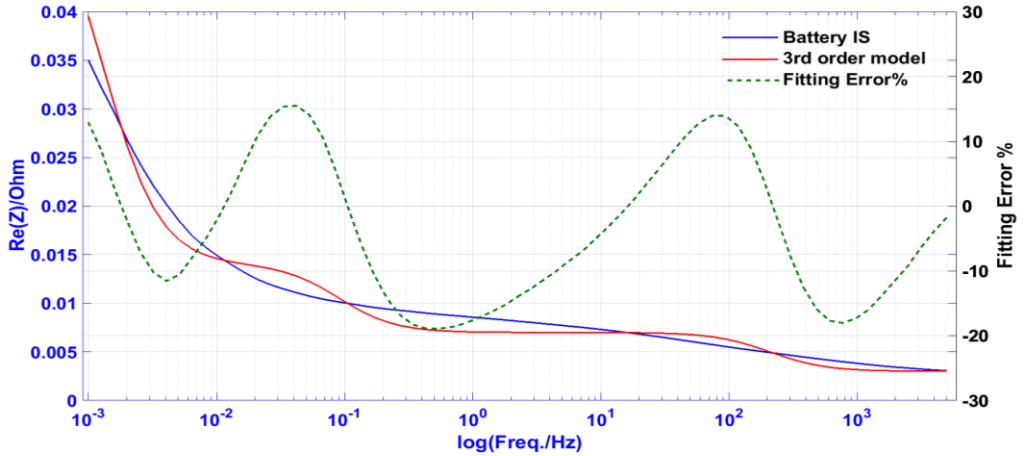
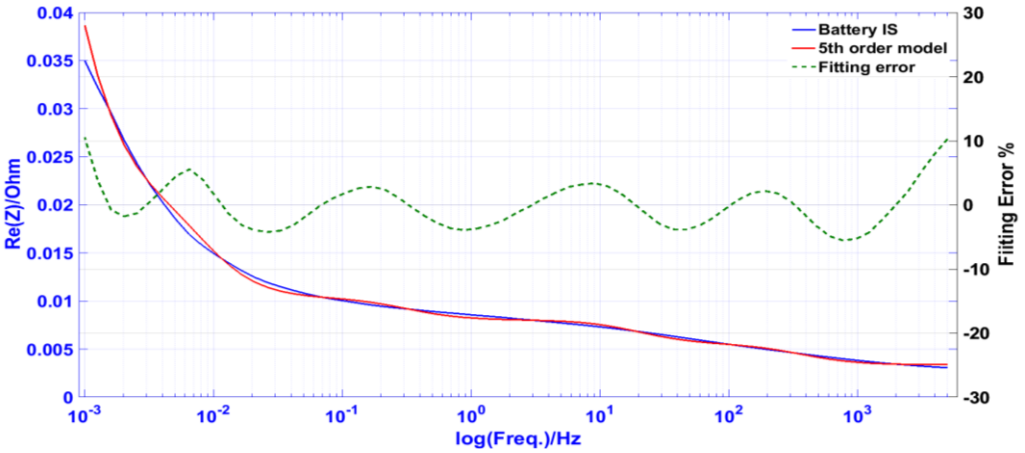


Fig. 3-2: Curve fitting of battery IS within FFR by 3rd order ECM

In order to decrease the amplitude of the overshoots of the fitted curve to decrease the error, it is required to increase the number of the R//C branches to allow more cutoff frequencies. A second fit with a 5th order ECM has also been made to compare with the 3rd order ECM to evaluate the curve fit accuracy as shown in Fig. 3-3.



(a)



(b)

Fig. 3-3: Curve fitting of battery IS with: (a) 3rd order ECM; (b) 5th order ECM

It is obvious that the 3rd order model cannot maintain good accuracy within the full frequency range (FFR) and the error varies between ± 20% based on frequency as shown in Fig. 3-3(a). However the 5th order model maintained good accuracy within the FFR with a maximum error of ±5% as shown in Fig. 3-3 (b). It can be concluded that the order of the model should be increased as the frequency range to be considered increases in order to maintain a good level of accuracy. Based on this, an accurate model with reduced order can be obtained if the curve fitting effort is made for a targeted frequency range (TFR) that contains the dominant spectrum of the load profiles instead of fitting within the overall FFR.

By using a 3rd order ECM to fit the battery IS within a TFR of (1mHz up to 0.5Hz) that is selected based on the dominant spectrum of an assumed load profile with a period of (2s up to 16min) , a good accuracy level can be achieved as shown in Fig. 3-4. The error within the TFR is maintained within ±2%; however it reached 200% outside this range and this does not contribute to the model accuracy as will be presented later.

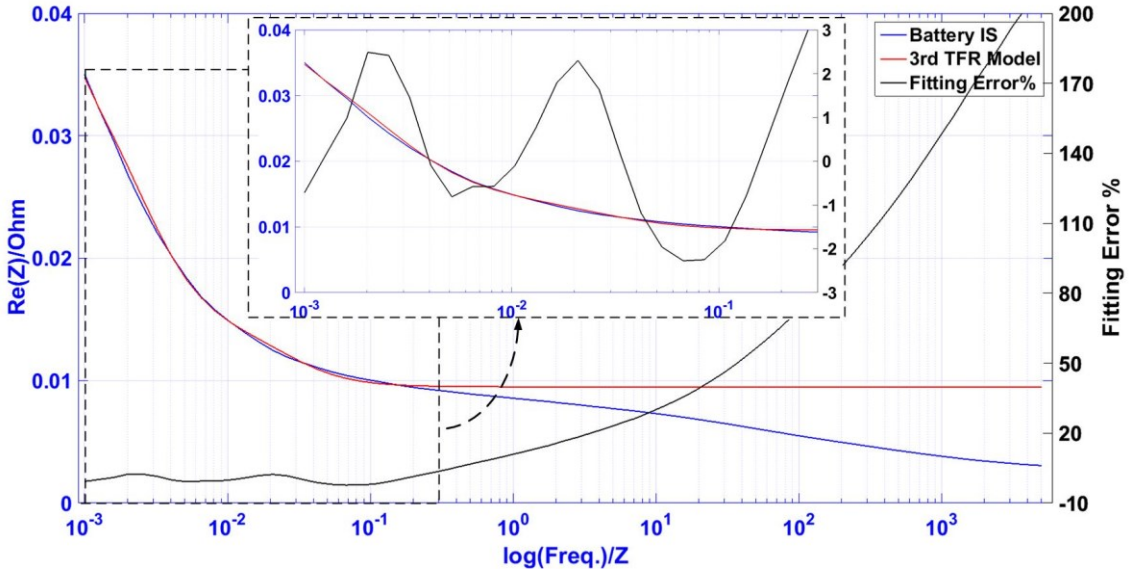
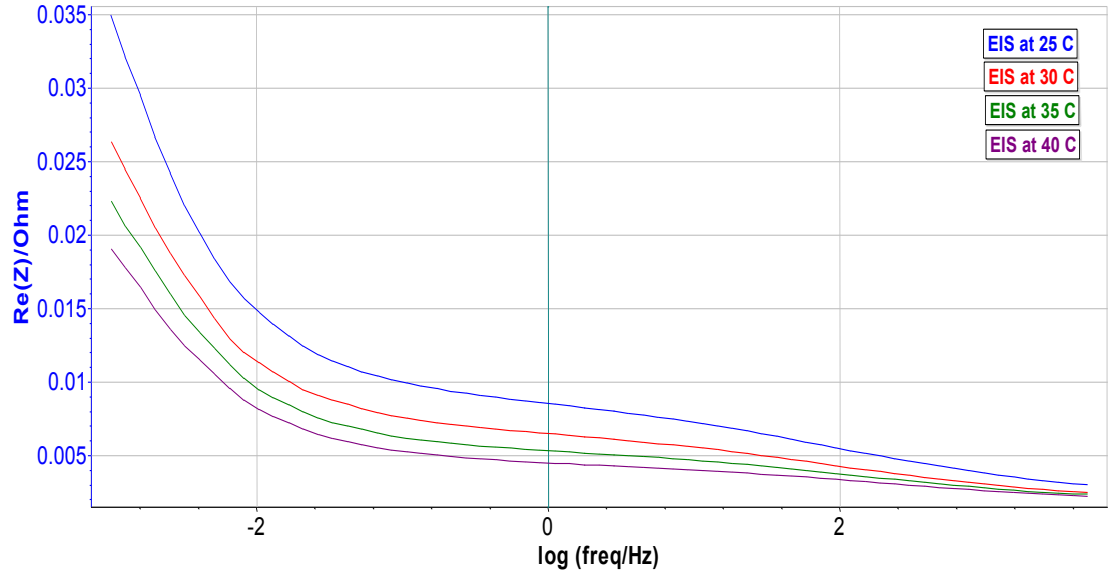


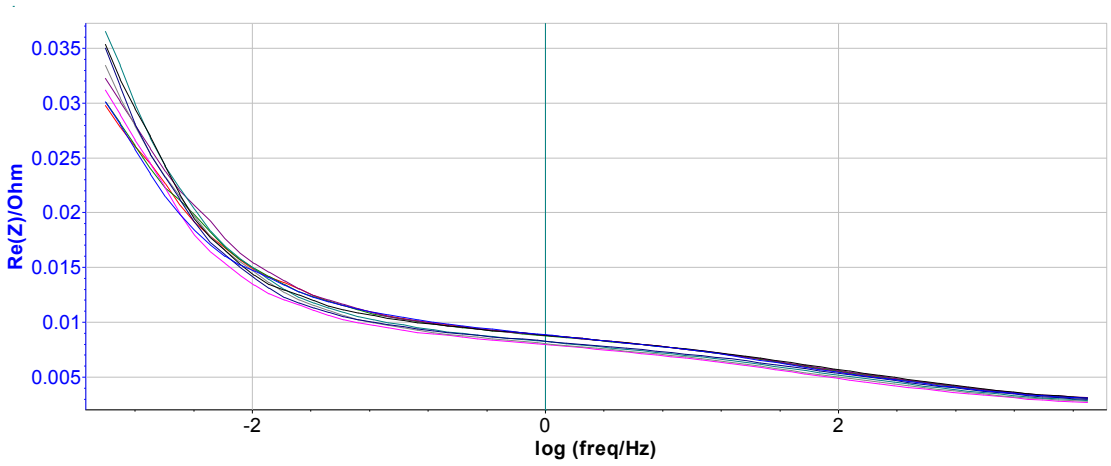
Fig. 3-4: Curve fitting of battery IS with a 3rd order ECM within TFR

The model parameters are estimated offline based on battery IS data that have been measured under defined conditions of temperature and state of charge (SoC). Therefore changes in these conditions will contribute to model errors. A change of temperature is the biggest contributor to model errors due to the significant change in battery IS with temperature as can be seen in Fig. 3-5 (a) which represent the measured IS data obtained by EIS experiments for the same previously described battery at different temperatures. Changing the battery cell temperatures was made using a thermally isolated box with controlled temperature. A change of temperature from 25°C to 40°C causes a change of 80% in the real part of impedance Re(Z). By contrast, a change in SoC from 10% to 90% causes a change of 16% in Re(Z) (Fig. 3-5 (b)). In order to maintain model accuracy, it is suggested that the model parameters are estimated under different

conditions of temperature and SoC and then these estimates are used during operation based on online measurement of temperature and SoC estimation to update the model parameters.



(a)



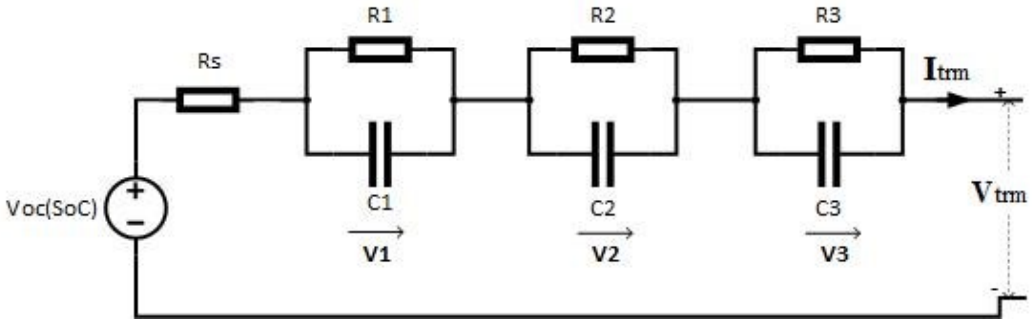
(b)

Fig. 3-5: Battery IS at (a) Different temp.at 50% SoC ; (b) SoC (10% to 90%) at temp. 25 ºC

3.1.2 Energy loss estimation methods

3.1.2.1 Method 1

The proposed energy loss observer is created by implementing the 3rd order ECM model (Fig. 3-6) with the parameters estimated by fitting the IS measurements obtained by Bio-logic© SP-150 Potentiostat for LiFePO4 battery cell (8Ah capacity) within a TFR as discussed in the previous section. The observer utilizes battery current measurements (I_{trm}) as the input to the state space model (SSM) described by (3-1) and (3-2) to estimate the model states ($V_{1,\dots 3}$) that are then used to drive the estimation of the battery terminal voltage (V_{trm}) and energy losses E_{loss}.



Parameters	Rs (mΩ)	R1 (mΩ)	C1 (F)	R2 (mΩ)	C2 (F)	R3 (mΩ)	C3 (F)
at 25°C	9.3	2.95	885	15.2	2378	76.7	5710
at 30°C	7	2.7	1256	11.8	3293	73.5	7471

Fig. 3-6: 3rd order ECM model for TFR with estimated parameters at 25°C and 30°C at 50%SoC

$$\begin{bmatrix} \dot{V}_1 \\ \dot{V}_2 \\ \dot{V}_3 \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_1 C_1} & 0 & 0 \\ 0 & -\frac{1}{R_2 C_2} & 0 \\ 0 & 0 & -\frac{1}{R_3 C_3} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \begin{bmatrix} \frac{1}{C_1} \\ \frac{1}{C_2} \\ \frac{1}{C_3} \end{bmatrix} I_{trm} \tag{3-1}$$

$$V_{trm} = V_{oc} - (I_{trm} R_s + V_1 + V_2 + V_3) \tag{3-2}$$

The term "energy loss" E_{loss} (Wh) refers to the power losses P_{loss} (W) during a period of time t_e (hour) and can be estimated as:

$$E_{loss} = \int_0^{t_e} P_{loss} dt \tag{3-3}$$

Whilst the power losses (P_{loss}) is estimated online through the observation of the states ($V_{1,\ldots 3}$) of the ECM model shown in Fig. 3-6 using the SSM ((3-1) and (3-2)) as:

$$P_{loss} = R_s I_{trm}^2 + \sum_{i=1}^{3} \frac{V_i^2}{R_i} \tag{3-4}$$

In order to validate the proposed loss observer, two other methods are used to estimate the energy loss for the battery and the results of the three are compared.

3.1.2.2 Method 2

The second method uses the frequency domain spectrum of the load current profile and the values of the real part of the impedance (Re (Z)) at these frequencies [50], then estimates the power losses produced by each relevant harmonic as demonstrated in Fig. 3-7 that shows that

fitting of 3rd ECM with the measured IS data obtained for 8Ah LiFeO4 battery cells at 25°C ambient temperature. The assumed load profile was as 30s charge by 2A then 30 rest followed by 30 discharge by 2A then 30 rest. The power loss during this cycle based on this method is estimated based on (3-5):

$$P_{loss} = \sum_{k=1}^{n} I_k^{\,2}\,\mathrm{Re}(Z)_k \tag{3-5}$$

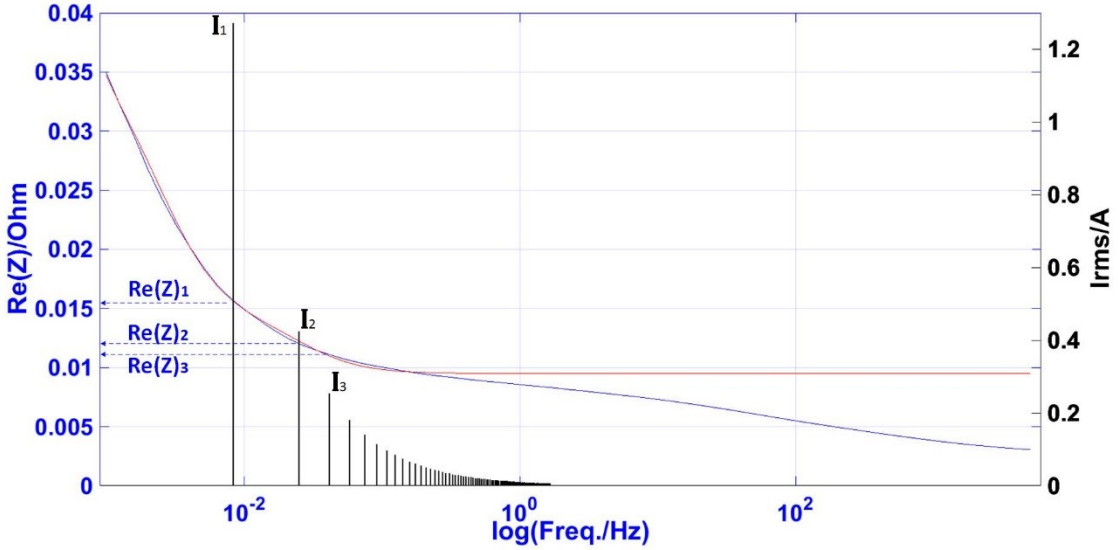


Fig. 3-7: Frequency domain based loss estimation

where I_k is the RMS current (A) of the frequency component k while $Re(Z)_k$ is the real part of impedance (Ohm) at that frequency. The number of relevant harmonics n is set to 3 as the first three components of the current spectrum are the most dominant in the spectrum.

3.1.2.3 Method 3

In this method, the difference between the energy consumed during charging of the battery by a defined charge amount (Ah) and the energy taken during discharging the same charge amount is considered to be the energy loss which can be justified as follows:

When the charging process is considered for the battery to a defined state of charge SoC_1 starting from initial state SoC_o, the energy that is supposed to be stored in the battery after this charging (E_1) is:

$$E_1 = E_o + \int_0^{t_{chr}} I_1(t)V_1(t)dt - E_{loss1} \tag{3-6}$$

where E_o is the energy stored in the battery at the initial state of charge SoC_o, $I_1(t)$ and $V_1(t)$ are measured battery current and voltage during the charge process time t_{chr}, and E_{loss1} is the assumed energy loss during charging process.

When the discharging process is considered for the battery from the state of charge SoC_1 to the state of charge SoC_2; the energy that is supposed to be stored in the battery after discharging (E_2) is:

$$E_2 = E_1 - \int_0^{t_{dchr}} I_2(t)V_2(t)dt - E_{loss2} \tag{3-7}$$

where $I_2(t)$ and $V_2(t)$ are the measured battery current and voltage during the discharge process time (t_{dchr}), and E_{loss2} is the assumed energy loss during this discharging process.

The discharged capacity ($I_2 \times t_{dchr}$) is adjusted to be the same as the charged capacity ($I_1 \times t_{chr}$) so that ($SoC_2 = SoC_o$) and hence ($E_2 = E_o$), then by substituting from (3-6) into (3-7):

$$E_{loss} = \int_0^{t_{chr}} I_1(t)V_1(t)dt - \int_0^{t_{dchr}} I_2(t)V_2(t)dt \; ; \quad (E_{loss} = E_{loss1} + E_{loss2}) \tag{3-8}$$

This method was validated experimentally by considering the charge/discharge cycle shown in Fig. 3-8, for same battery cell ($LiFePO_4$) at room temperature (25°C) by the Bio-logic© SP-150 Potentiostat which can perform cell cycling with accurate measurements for cell current, voltage, power and energy during cycle. It can be seen that ($Voc_2 = Voc_o$) and hence ($SoC_2 = SoC_o$), this means that the battery after the completed charge/discharge cycle has returned to the initial SoC before this cycle (SoC_o), so the difference between the charge and discharge energies represents the energy lost as it did not contributed to the change of the battery SoC which agrees with (3-8).

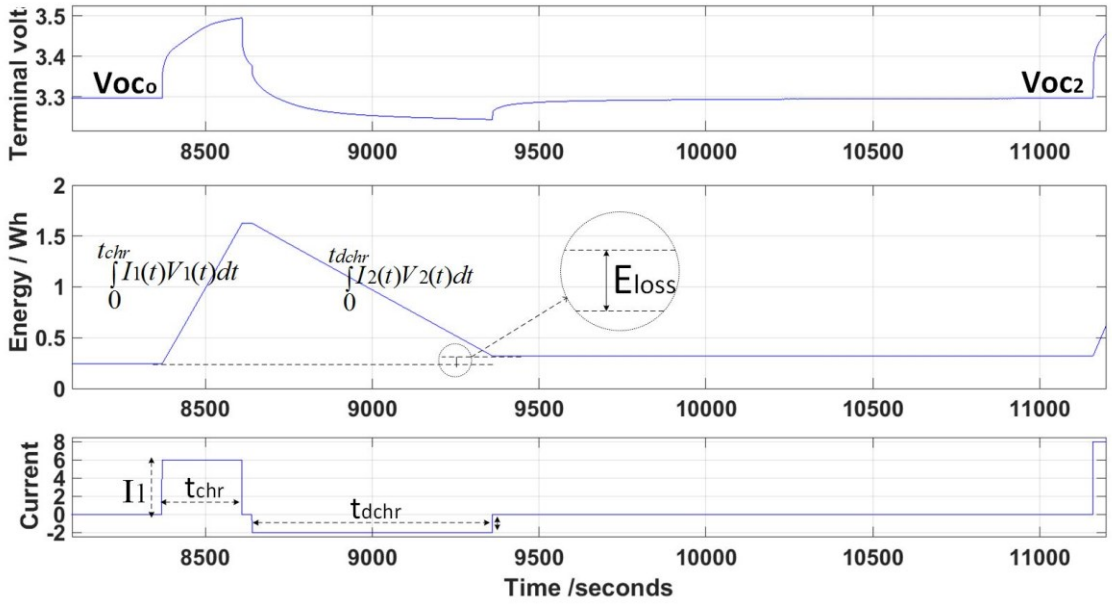
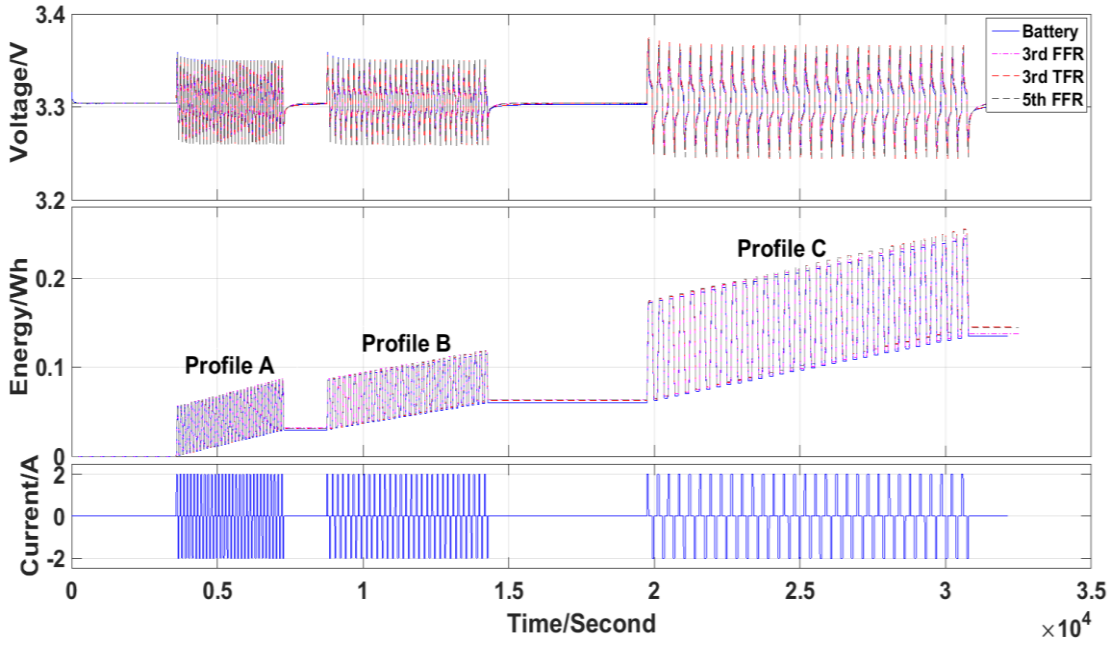


Fig. 3-8: Time domain based loss estimation

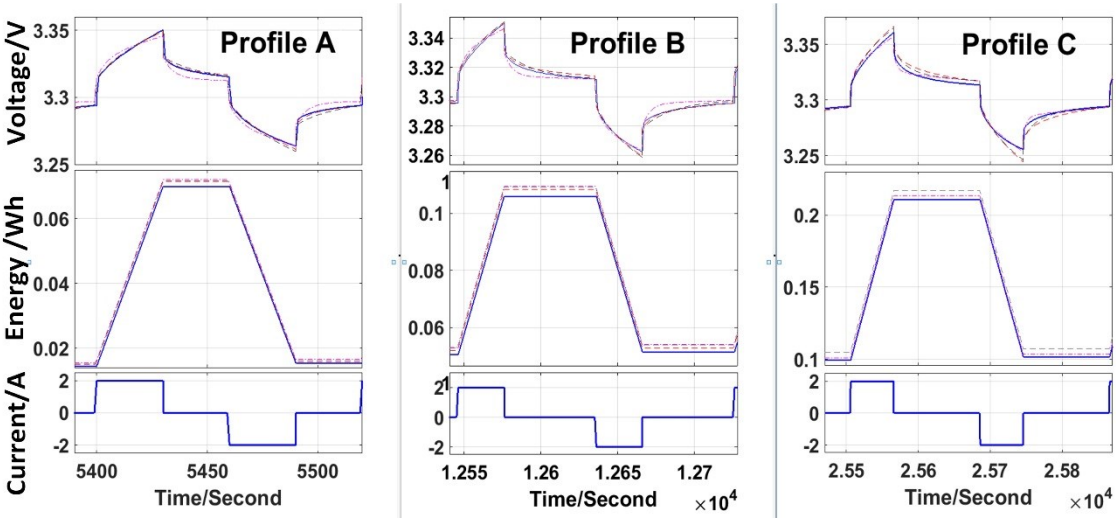
3.1.3 Model Validation

In order to validate the battery observer and the modelling technique used with it, the battery was subjected to different load profiles to validate the proposed loss models. The proposed 3rd order ECM for TFR results are compared with the more complex 5th order ECM as well as 3rd order ECM for a FFR. Different load profiles are chosen to create a changing load frequency spectrum in order to test the model accuracy within the overall targeted frequency range (TFR). Fig. 3-9 shows the results obtained based on the three models. When compared to the true

battery voltage measured by the Potentiostat, it is clear that the 5th order ECM for FFR and the 3rd order ECM for TFR show smaller errors than the 3rd order ECM for FFR for load profiles A and B; for profile C however, the latter model shows accidentally a better accuracy, due to a higher temperature as it will be discussed in more details later.



(a)



(b)

Fig. 3-9: (a) Voltage and energy for the actual battery and the three different models during testing with different load profiles; (b) magnification of one-cycle for each profile

In the following subsections, the three models will be evaluated. The model parameters were estimated based on battery IS data obtained at a temperature of 25ºC. The experimentally measured energy loss per cycle (blue plot) in Fig. 3-10, and Fig. 3-11 and Fig.3-12c is estimated based on Method 3 described previously based on voltage and current measurements obtained by the SP-150 Potentiostat; the energy loss observers however, are based on Method 1 (black plot) as well as Method 3 (red plot).

3.1.3.1 5th order ECM for full frequency range

As seen in Fig. 3-10(a), the energy loss estimation error increases with temperature. The battery temperatures are measured by two sensors: one is located on the battery surface; the second sensor is located on a battery terminal, which being metal can give a better indication of its internal temperature. Different profiles have different fitting errors as shown in Fig. 3-10(b). For example the energy loss estimation error for profile A is expected to be around 4% as the dominant spectrum has a 4% fitting error (Fig. 3-10(b)) and Fig. 3-10(a) confirms this expectation; however this energy loss error increases from 4% during the initial cycles to 7% due to an increase in battery temperature due to the losses during the cycling.

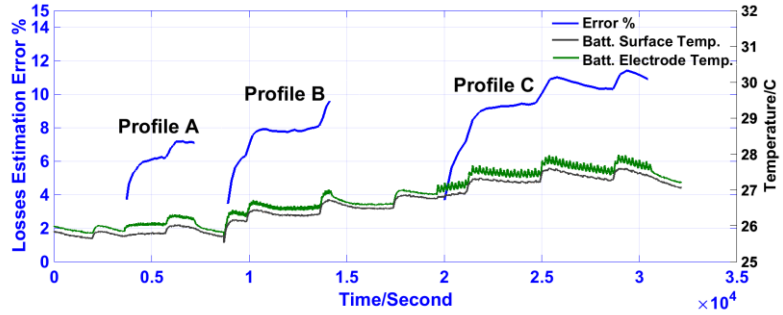
The increase in battery temperature causes the battery's resistance *Re(Z)* to decrease as shown before in Fig. 3-5 (a). This causes the battery energy loss per cycle to decrease during the cycling which leads to the increase of the error between the real battery and the model as shown in Fig. 3-10 (c).

3.1.3.2 3rd order ECM for full frequency range

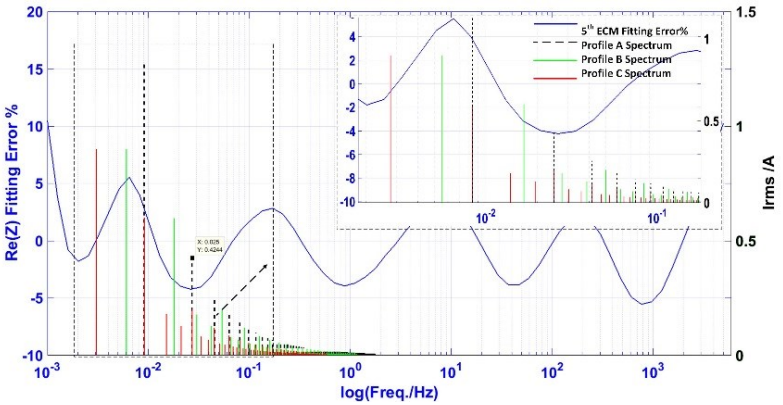
As can be seen in Fig.3-11, the 3rd order ECM for FFR has different results based on the load profiles.

Fig. 3-11(a) shows that profile A has the biggest error as the 2nd harmonic of its spectrum is located near the peak of the *Re(Z)* fitting error. On the other hand, profile B has two dominant frequency components matching with a positive and a negative *Re(Z)* fitting error that partly cancel each other and the result is a smaller error than for Profile A. By comparing the loss estimation errors of the 5th order ECM for FFR shown in Fig. 3-10(a) with the 3rd order ECM for FFR shown in Fig. 3-11(a), it can be seen that for both load profiles A and B, the precision of the 5th order ECM is better, as expected due to its lower fitting error.

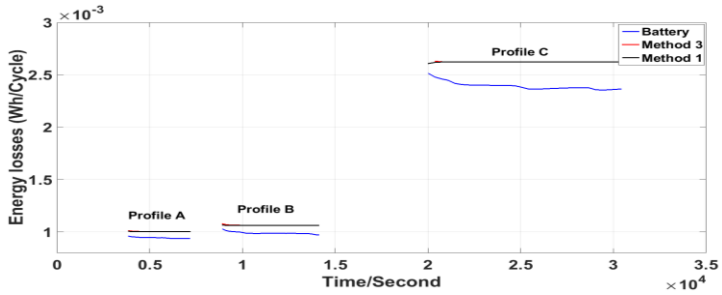
For profile C however, due to higher losses/temperature in the battery which causes a decrease of Re(Z), the error of the 3rd order ECM for FFR shows an error range (-6% to +2%) with a significantly smaller average than the 5th order ECM for FFR. The reason is that the Re(Z) error in the curve fitting at the fundamental frequency of profile C (red bar) is unusually smaller compared to the actual Re(Z) of the battery at 30ºC as seen in Fig.3-11(d) , which seems to be closer to the actual battery temperature (Fig.3-11(a)).



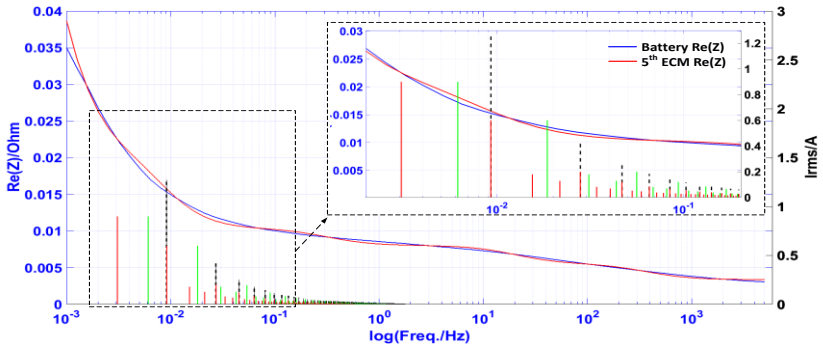
(a)



(b)



(c)



(d)

Fig. 3-10: 5th ECM error analysis with (a) Evolution of energy loss estimation error and temperature; (b) Battery Re(Z) fitting error and load current profiles spectrum; (c) Energy losses per cycle for the real battery and the 5th order ECM; (d) Re(Z) for the real battery and the model and the load current profiles spectrums.

3.1.3.3 Proposed 3rd order ECM for a targeted frequency range

As seen in Fig. 3-12a, the 3rd order ECM for TFR has good loss estimation results within the overall targeted frequency range (TFR) for load profiles A and B (errors span from 1% - 7%) which is better compared to the error range of the 5th order ECM for FFR. However, for profile C, the loss estimation error is ranging from 8% to 14% which is not consistent with the expectations of having only a 2% fitting error in *Re(Z)* as can be seen in Fig. 3-12b. This means that the significant increase in the error is mainly caused by the increase of the battery temperature during cycling. Fig. 3-5 confirms that *Re(Z)* can drop by approximately 18% at 4mHz when battery temperature increases from 25°C to 30°C which is similar to the change in the temperature of the battery terminal shown in Fig. 3-12(a). It is therefore clear that the significant errors in the loss estimation found when using a model that has small fitting Re(Z) errors, this due to the temperature variation of the battery during cycling.

It is possible to imagine a system that estimates the internal temperature of a battery cell, which is very hard to measure, based on an energy loss error observer. But it is also possible to improve the accuracy of the energy loss observer by allowing it to adapt to temperature variations.

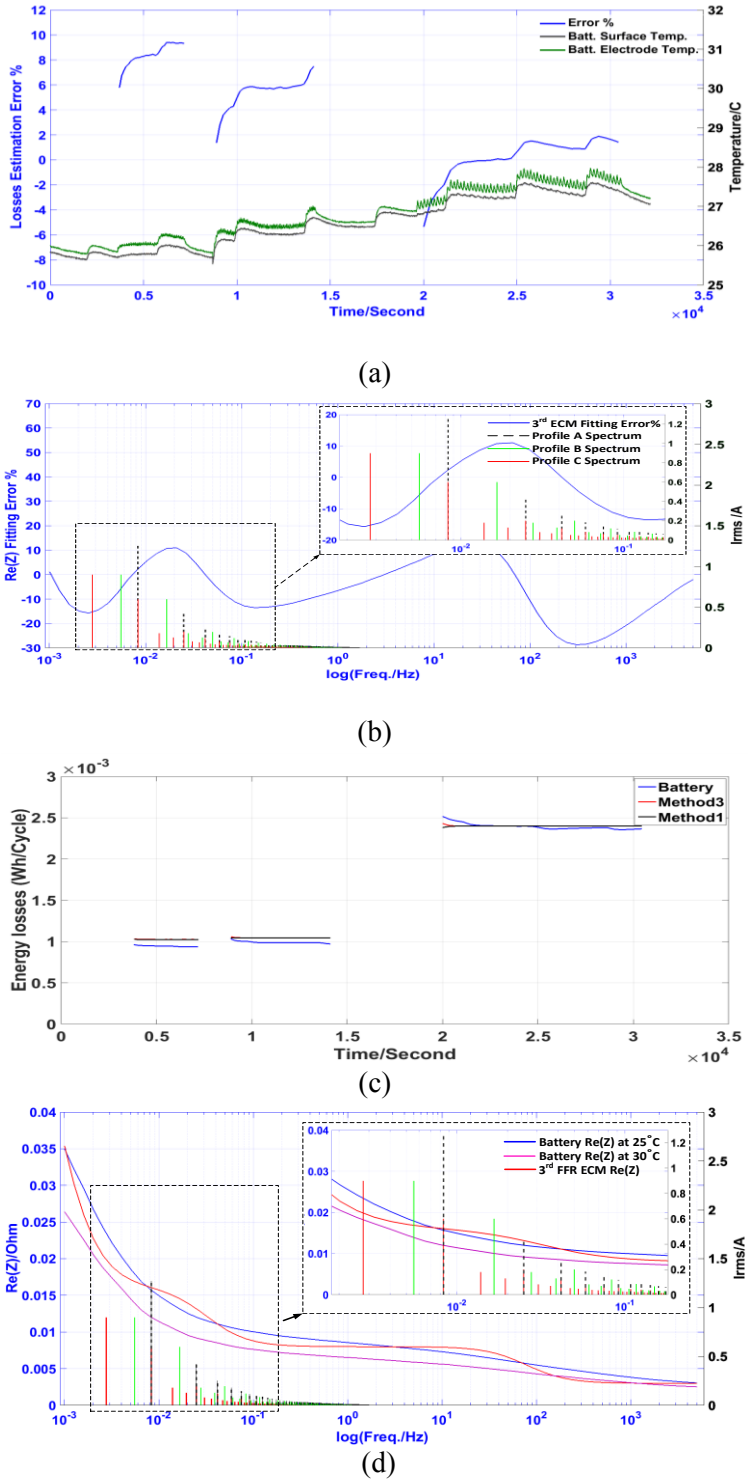
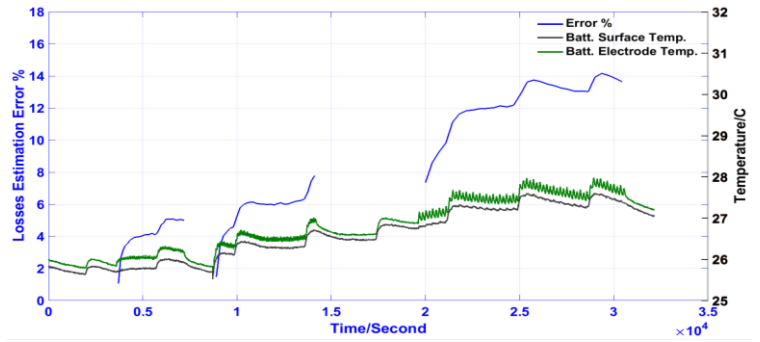
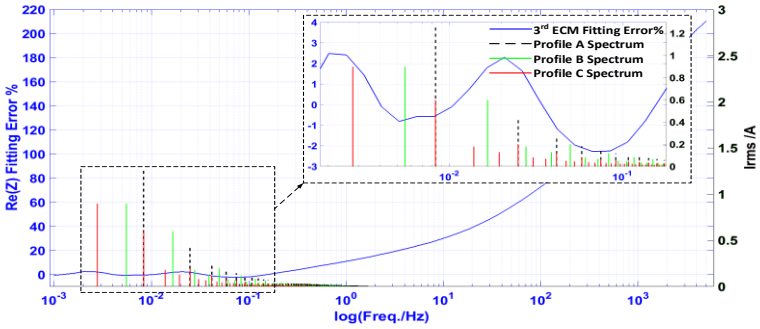


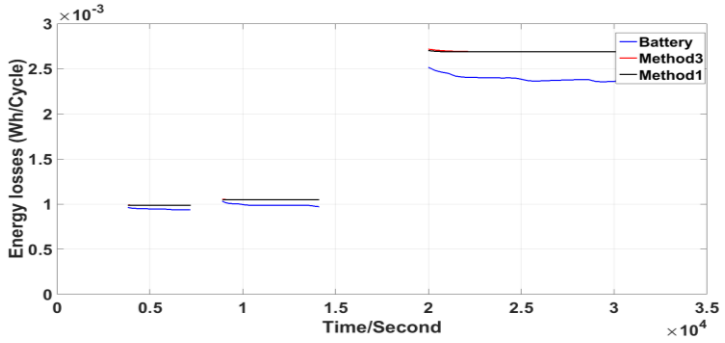
Fig. 3-11: 3rd ECM for FFR error analysis with (a) Evolution of energy loss estimation error and temperature; (b) Battery Re(Z) fitting Error and load current profiles spectrum; (c) Energy losses per cycle for the real battery and 3rd ECM for FFR; (d) Re(Z) for the real battery and the model and the load current profile spectrum.



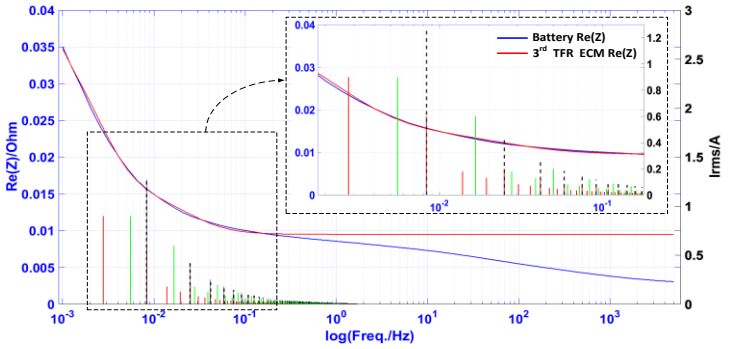
(a)



(b)



(c)

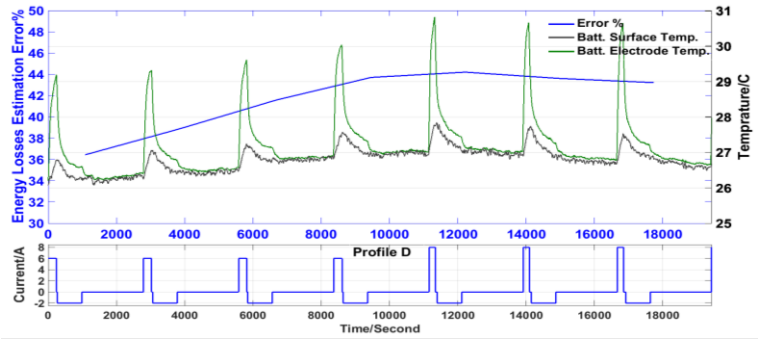


(d)

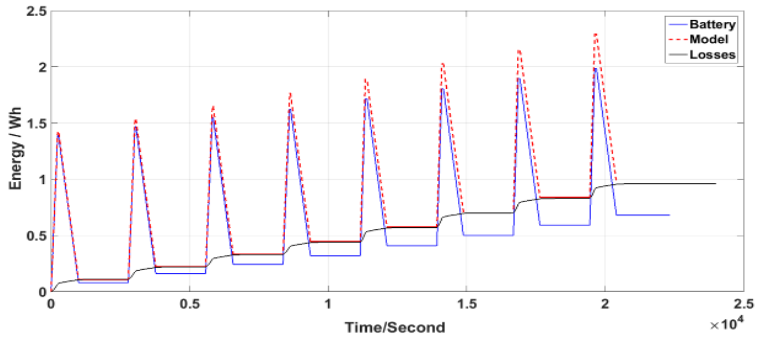
Fig. 3-12: 3rd ECM for TFR error analysis with (a) Evolution of energy loss estimation error and temperature; (b) Battery Re(Z) fitting Error and load current profiles spectrum; (c) Energy losses per cycle for the real battery and the three models; (d) Re(Z) for the real battery and the model and the load current profiles spectrums.

In order to test these ideas, a further test (profile D) with higher load currents that would lead to significantly higher battery internal temperatures has been applied and the results are shown in Fig. 3-13b. Without a temperature correction, it can be seen that the energy loss estimation has large errors (34% - 44%) due to the significant increase in battery terminal (and also internal) temperature (up to 31°C) although the surface temperature does not show a large increase (27.5°C).

In order to improve the energy loss observer accuracy, a lookup table for model parameters determined at different temperatures has been used to update the model parameters based on the temperature measured at the battery terminal. Fig. 3-14 shows that this method gives a consistent accuracy for all load profiles A, B and C as well as profile D with maximum error of ±2% for profiles A, B and C and ±4% for profile D.

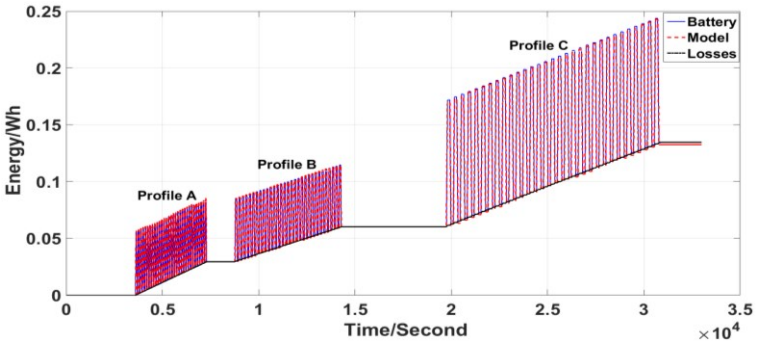


(a)

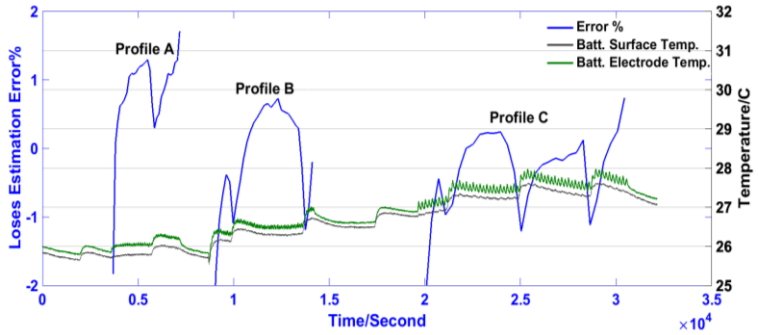


(b)

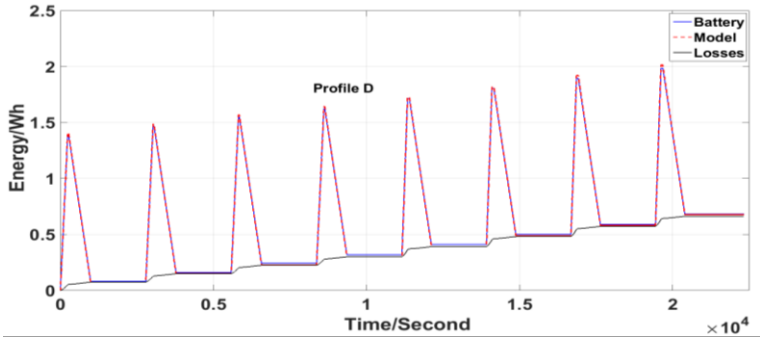
Fig. 3-13: Battery versus 3rd ECM for TFR for profile D: (a) Energy loss estimation error; (b) Energy and loss for battery and model



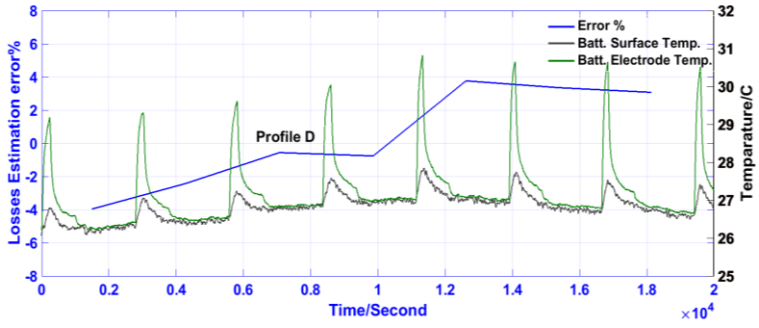
(a)



(b)



(c)



(d)

Fig. 3-14: Battery versus 3rd ECM for TFR energy losses and corresponding errors for: (a,b) Profiles A, B and C; (c,d) Profile D

3.1.4 Simulink® based battery model

The developed battery model based on the proposed modelling methodology using Simulink® is shown in Fig. 3-15, the model inputs are the cycling current and battery temperature (which is used to extract the model parameters from the implemented look-up tables based on the temperature). The look-up tables contains model parameters (Rs, R1:R3 and C1:C3) at different temperatures which are identified offline by curve fitting within a TFR for the EIS data obtained experimentally at these temperatures for the 8Ah LiFeO4 battery cells. Based on the value of temperature input of the look-up table it gives the corresponding outputs for the values of model parameters that used by the state space model to estimated battery terminal voltage and estimate energy loss based on method 1 and 3 as well as the estimation of the power losses which will be used as an input to the battery cell thermal model to estimate cell temperature and update the model parameters accordingly.

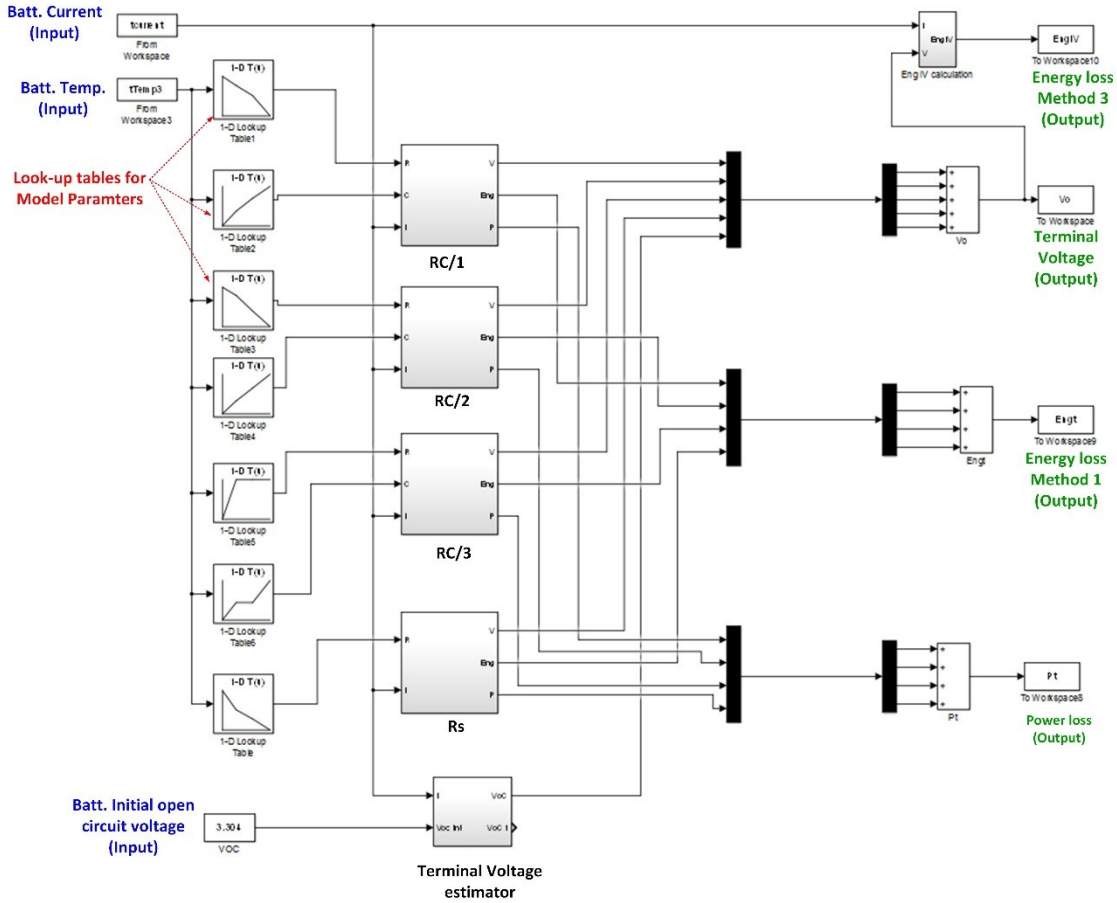


Fig. 3-15: Proposed battery model based on 3rd order ECM using Simulink®

3.1.5 Model parameters identification for candidate battery cells

So far, model parameters were identified for a LiFeO4 battery cell with capacity of 8Ah, however the proposed modelling methodology can be adapted and applied for other battery cell chemistries and model parameters can be identified same way. In Chapter6, two different battery cells will be investigated for utilization in the different designs of the energy storage system (ESS). Accordingly, electrical and thermal modelling is required in order to analyse the thermal stress on these cells in different designs of the ESS. Therefore, the ECM parameters need to be identified for these battery cells which are the Panasonic ‘’NCR18650B’’cell, and A123systems ‘’ANR26650 M1-B’’ cell. In order to identify model parameters, the impedances of both cells have been measured through impedance spectroscopy (IS) experiments at room temperature (25^{o}C), then model parameters are estimated by means of curve fitting with the measured impedance within a TFR as proposed earlier. Fig. 3-16 and Fig. 3-17 show fitting of the real part of the impedance for Panasonic ‘’NCR18650B’’ and A123systems‘’ANR26650 M1-B’’ respectively, used to identify the 3rd order ECM parameters for the cells within a TFR of (1mHz-1Hz). The identified parameters for both cells the model summarized shown in Table 3-1.

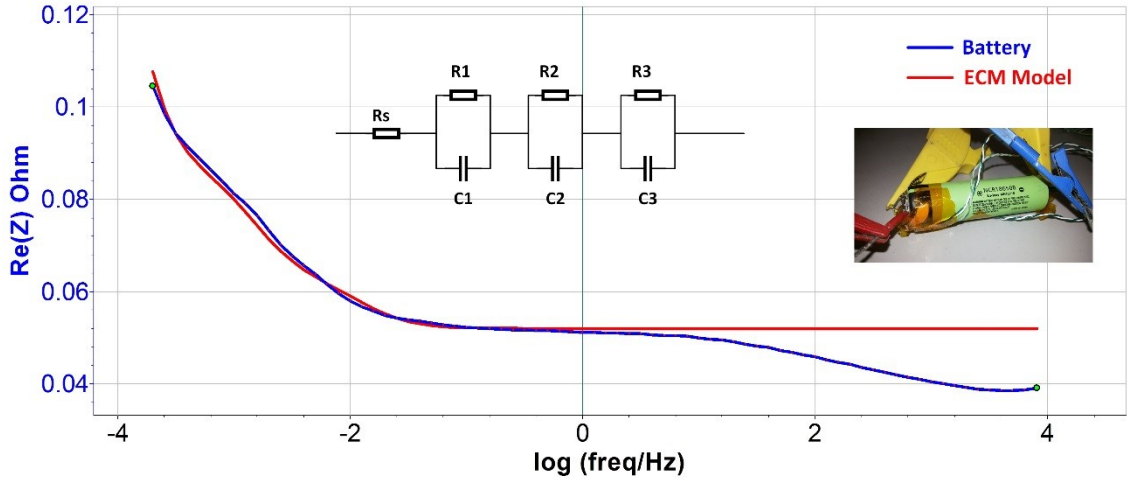


Fig. 3-16: Curve fitting of IS for Panasonic‘’NCR18650B’’cell within TFR by 3rd order ECM

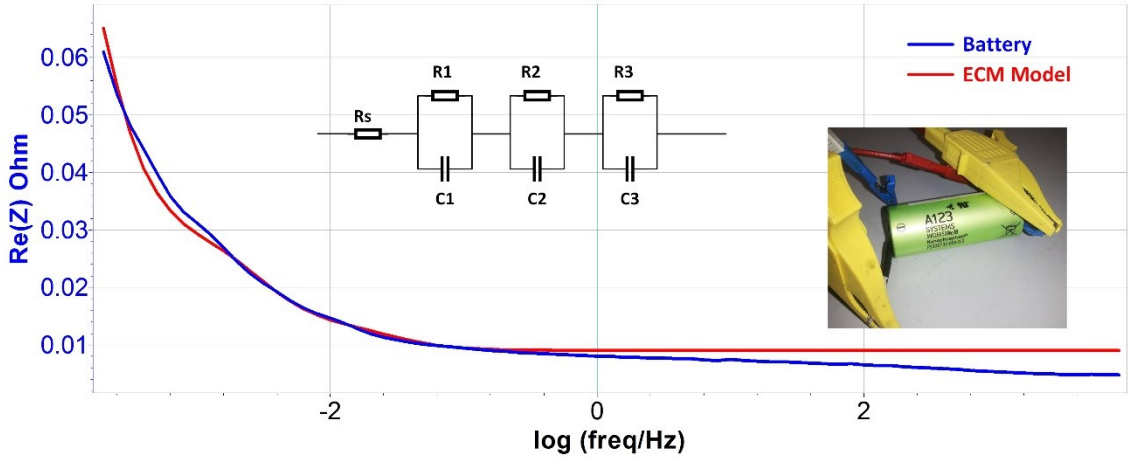


Fig. 3-17: Curve fitting of IS for A123systems ‘’ANR26650 M1-B’’ cell within TFR by 3rd order ECM

Table 3-1: 3rd order ECM parameters identified for Panasonic and A123systems batteries

Model parameters	**Panasonic ‘’NCR18650B’’cell**	**A123systems ‘’ANR26650 M1-B’’cell**
Rs (mΩ)	52	9
R1(Ω)	23	15
C1(F)	4314	3406
R2(mΩ)	10	4.5
C2(F)	1198	1196
R3(mΩ)	400	108
C3(F)	8115	10321

It can be observed that the resistances of A123systems battery cell are significantly lower compared to the Panasonic battery cell especially at higher frequencies which is expected as the A123systems battery cell is a power battery that designed to deliver significantly high power for a short time.

3.2 Supercapacitor Modelling

In order to accurately evaluate the thermal stress on the supercapacitor (SC) cells, accurate electrical and thermal models are required to accurately estimate the power losses inside the candidate SC-cells.

3.2.1 Equivalent circuit model of SC-cell

The equivalent circuit model (ECM) is used here to represent the behaviour of the SC cell placing the most importance for extracting the correct internal resistances to evaluate the thermal stress during charge/discharge cycling. In order to identify the behaviour of the SC-cell, an experimental characterization through electrochemical impedance spectroscopy (EIS) has been performed on the selected SC-cell using the Biologic® SP-150 potentiostat. EIS test measurements for a Maxwell 350F SC-cell within a frequency range of 50mHz to 10kHz and at different bias voltages are shown in Fig. 3-18.

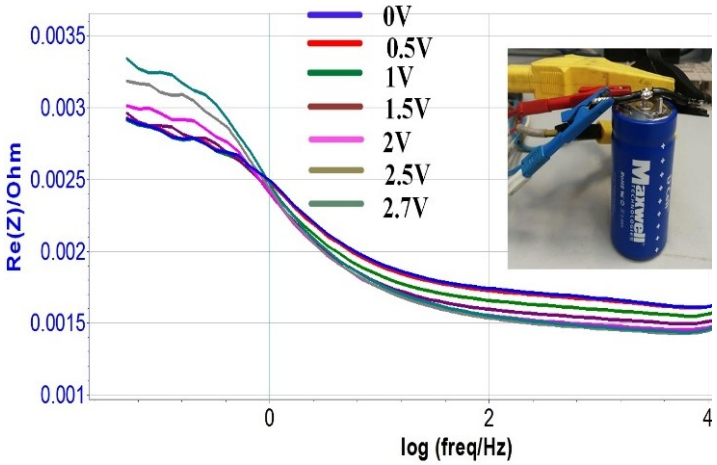


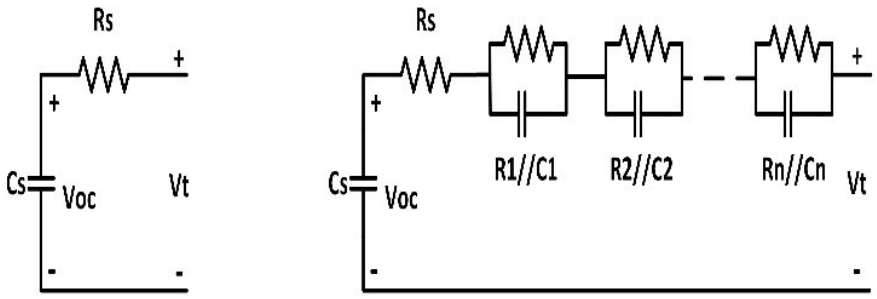
Fig. 3-18: Electrochemical impedance spectroscopy of SC cell

It can be seen that the cell resistance changes with frequency as well as bias voltage (equivalent to state of charge). The change of SC-cell's resistance with bias voltage is less significant,

therfore a good approximation can be achieved by considering the operating voltage range of the SC cell (1.25V to 2.5V in this design), therfore the resistance at 2V which is close to the cycle average can be used causing ESR errors of maximum 5% On the other hand, changing the SC-cell's resistance with frequency is significant. The resistance at 50 mHz is 100% more compared to the resistance at 50Hz, so it cannot be approximated accurately by a single average value. Thus, the simplified ECM consisting of a single resistor represents the device equivalent series resistance (ESR) in series with the bulk capacitor shown in Fig. 3-19(a) is not accurate for detailed loss estimations where the features of the load cycle are available [50].

Modelling the observed behaviour of the SC cell resistance accurately requires a dynamic model with *n* number of R//C branches as shown in Fig. 3-19(b). Increasing the number of R//C branches increases the accuracy of the model but increases the model complexity, Fig. 3-20 shows the accuracy of fitting the SC-cell EIS with the 5th order ECM.

In order to obtain an accurate model with reasonable complexity, the proposed methodology for battery modelling has been used by fitting SC-cell's EIS data within a defined targeted frequency range (TFR) selected based on the possible load profiles. Fig. 3-21 shows the accuracy of fitting a SC-cell EIS with a 3rd order ECM within TFR.



(a) (b)

Fig. 3-19: ECM of SC cell (a) simplified series RC model (b) higher order model

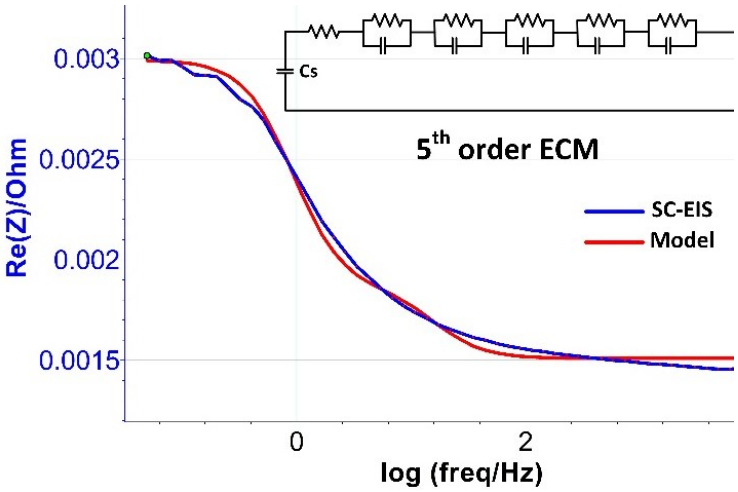


Fig. 3-20: Fitting SC-cell impedance spectroscopy with 5th order model

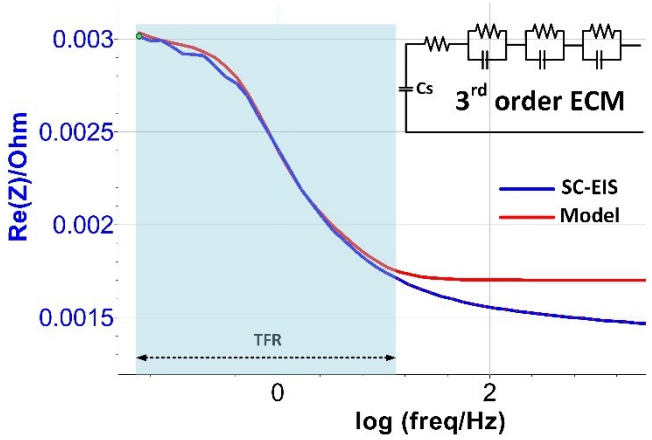


Fig. 3-21: Fitting SC-cell impedance spectroscopy with 3rd order model

3.2.2 Thermal model of SC cells

The thermal model of the SC-cell can be developed considering the energy loss due to the ionic and electronic transport and neglecting the energy loss caused by the thermodynamic phenomena taking place inside the cell [51]. The simplified equivalent circuit (EC) based thermal model can be adapted as in [52] and is illustrated in Fig. 3-22, with R_{cond} representing the thermal resistance (internal to case) of SC-cell and R_{covc} representing the thermal resistance (case to ambient) between SC-cell and ambient air and C_{th} is the thermal capacitance of the SC-

cell. To identify the parameters of the thermal model, cycling experiments for a SC-cell with sufficient charge/discharge current under constant ambient temperature were performed followed by a rest period.

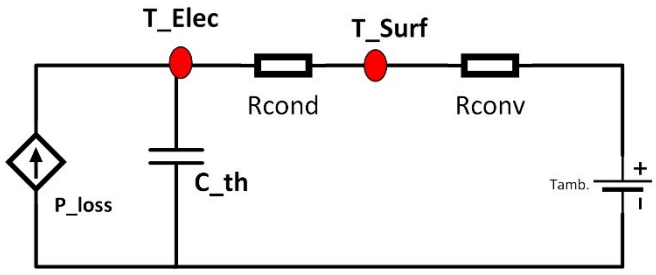


Fig. 3-22: EC based thermal model of supercapacitor cell

The temperatures of the SC-cells were measured at the electrode terminal (assuming that the thick metal enables fast transfer of internal heat) as an indication of the internal temperature and at surface of the SC-cell by means of thermocouples. The cycling of the SC-cell were performed for sufficient time to allow it to reach a steady state temperature as seen in Fig. 3-23, where charge/discharge current amplitude was set to 18A to produce significant power loss that will result in a sufficient/precisely measurable temperature rise as seen in Fig. 3-24 where the cell's voltage range was from 2.2V to 2.65V at ambient temperature of the 25^{o}C. Unlike the batteries, the SC cells are designed for wide temperature range with insignificant change in its ESR [143,144], temperature change will not be considering with modeling SC cell ESR.

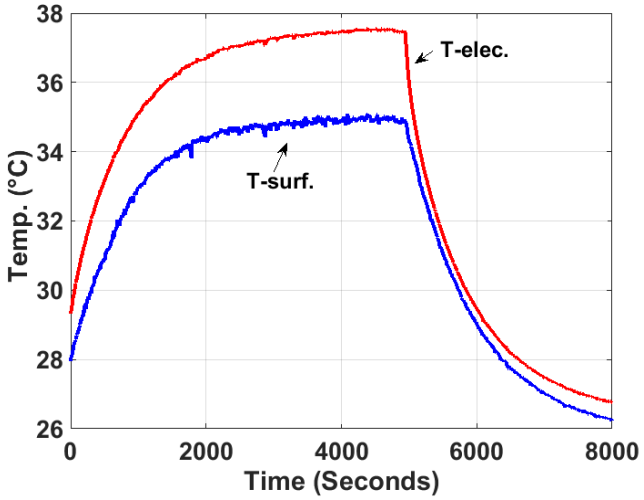


Fig. 3-23: 350F SC-cell electrode and surface temperatures during cycling

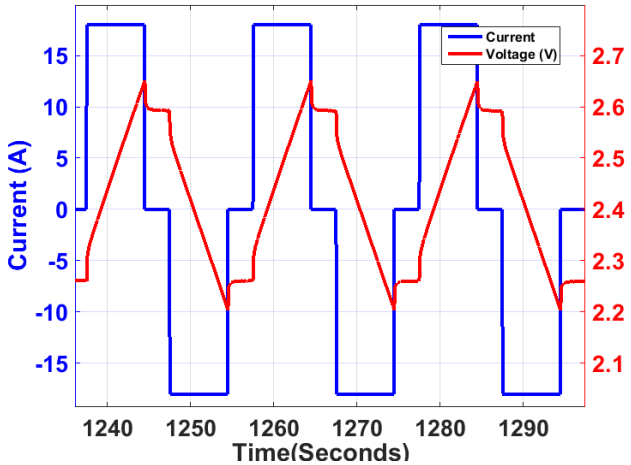


Fig. 3-24: 350F SC-cell current and voltage during charge/discharge cycling

When the temperature reaches steady state during cycling, the model parameters R_{cond} and R_{conv} can be obtained as:

$$R_{cond} = \frac{T_{elec} - T_{surf}}{P_{loss}} \tag{3-9}$$

$$R_{conv} = \frac{T_{surf} - T_{amb}}{P_{loss}} \tag{3-10}$$

The thermal capacitance can be estimated after identifying the thermal time constant (τ) of the SC-cell during the rest period as:

$$C_{th}=\frac{\tau}{R_{cond}+R_{conv}} \tag{3-11}$$

3.2.3 Model validation

In order to validate the developed model, a simulation model has been built using Simulink® implementing a 3rd order ECM with the identified parameters for the candidate cells for investigations which are Maxwell BCAP0350 (350F) and BCAP0150 (150F) cells by means of curve fitting with the EIS experimental data. The ECM parameters are shown in Table 3-2.

Table 3-2 3RD ORDER MODEL PARAMTERS FOR SC-CELLS

Model parameter	BCAP0150	BCAP0350
Cs (F)	150	350
Rs (mΩ)	5.4	1.7
C1 (F)	66	202
R1(mΩ)	1.67	0.9
C2 (F)	48.8	89
R2(mΩ)	0.7	0.3
C3(F)	3000	3000
R3(mΩ)	1	2

Also, thermal model parameters have been obtained for both SC-cells based on cycling experiments as discussed earlier. For the 150F cell, the thermal resistance (*Rcond*), the thermal resistance (*Rconv*) and thermal capacitance are 3.8 °K/W, 14.5 °K/W and 30 J/°K respectively and for the 350F cell, the values of the parameter are 2.5 °K/W, 7.5°K/W and 60 J/°K.

A simulation model for the BCAP0150 cell consisting of the 3rd order ECM and a thermal model (Fig. 3-25) with the identified parameters has been built using Simulink® and a cycling

profile has been applied to both the model and the real cell. The estimated temperature based on the cell model is compared with the measure temperature on the real cell.

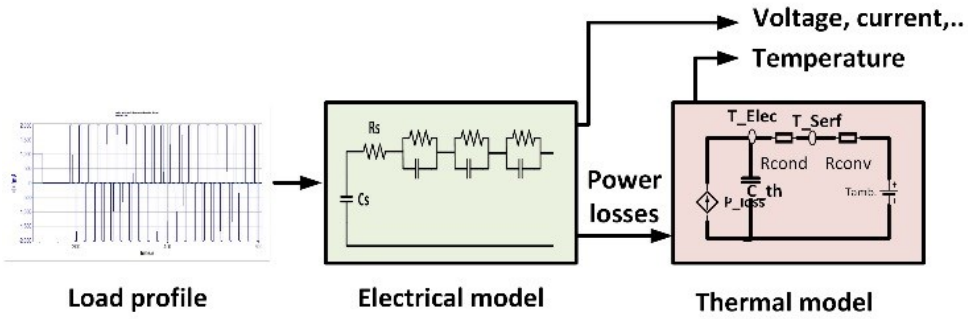


Fig. 3-25: Block diagram of the developed SC-cell stress model

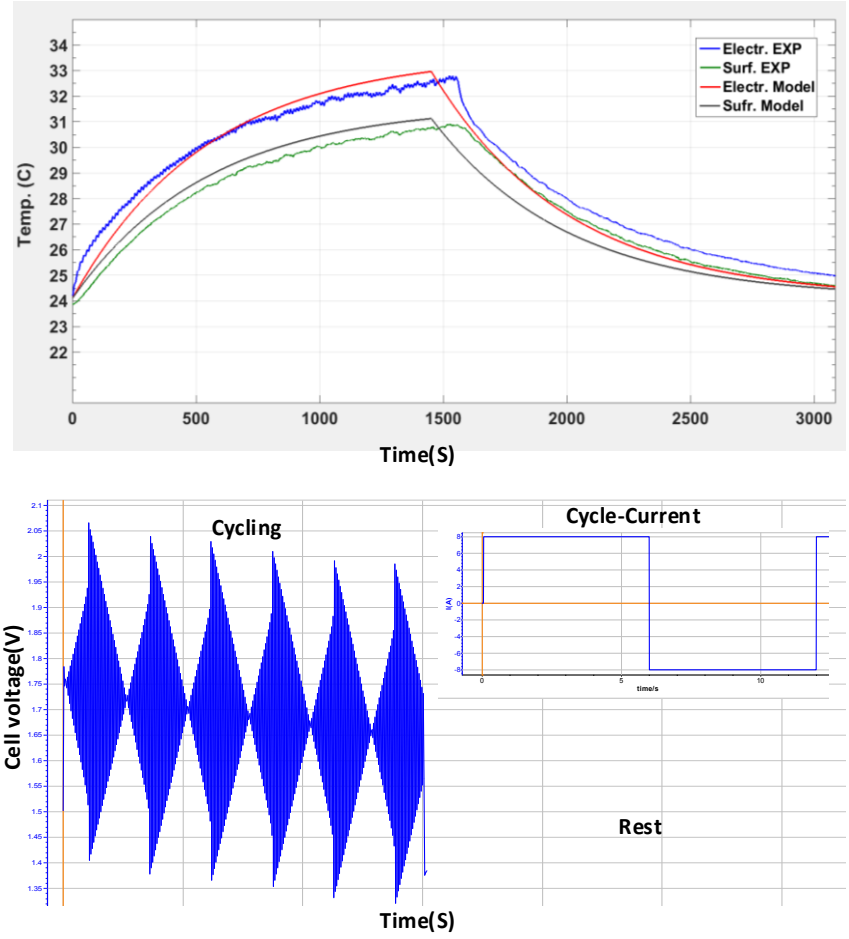


Fig. 3-26: cycling experiment for the SC-cell for model validation

Fig. 3-26 shows the experimental results for cycling of 8 Ampere current for a cycle duration of 12S for 125 cycles to ensure the cell reaches a steady state temperature. As can be seen, the estimated electrode temperature (Electr.Model) and surface temperature (Surf.Model) of the SC-cell based on the developed simulation model are reasonably consistent with the actual electrode temperature (Electr.EXP) and surface temperature (Surf.EXP) measured during the experiment. Accordingly, the developed model can be used to evaluate the thermal behaviour of the SC-cell with reasonable accuracy level. Fig. 3-27 shows the simulated electrical parameters for the BCAP0150 SC-cell in a string of 104 series-connected cells during discharge to supply a 2kW power loaded for a duration of 20 seconds.

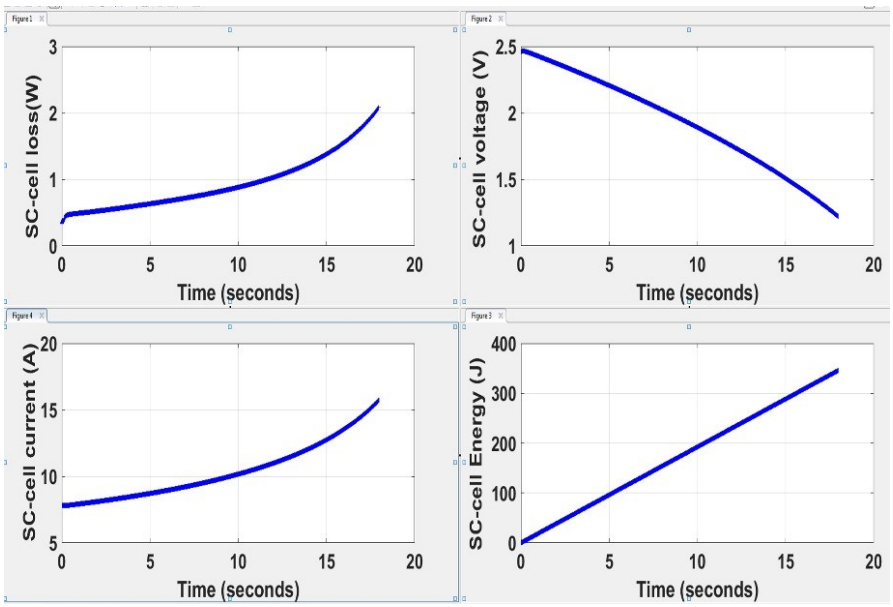


Fig. 3-27: BCAP0150 SC-cell simulation during 2kW power loading of the SC-unit

3.3 PV array modelling

The PV array is one of the main components in a satellite EPS which affects its size and performance. In order to better evaluate the design and performance of the EPS, a simulation model for the PV array with a reasonable accuracy is required. The model is used for in-orbit simulation of the PV array performance where it is subjected to large irradiance and temperature variations in order to evaluate the effect on the performance of the EPS. Within the following sub-sections the development of the PV cell model will be investigated then the developed model will be used to build the PV array model. Also, as the PV arrays are facing a large variation in temperature within the orbit, a thermal model for the PV array will also be developed in order to evaluate these effects on the design and performance of EPS.

3.3.1 PV cell modelling

A mathematical description of the current/voltage (I/V) terminal characteristic for PV cells can derived from the simplified equivalent circuit model (Fig. 3-28) [53, 54] which is usually used to represent its behaviour.

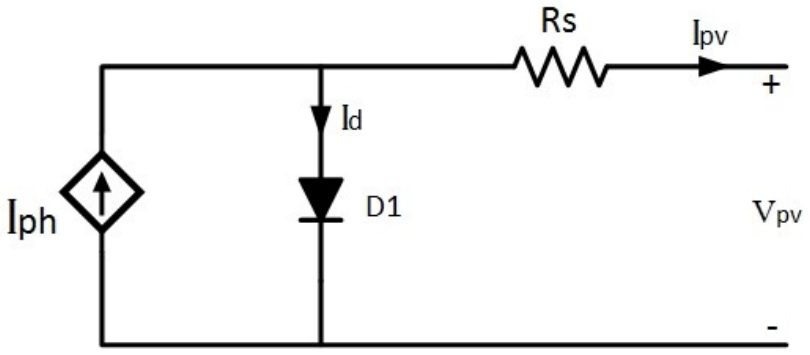


Fig. 3-28: Simplified-equivalent circuit of photovoltaic cell.

Based on circuit analysis, the I/V characteristics can be described as:

$$I_{pv} = I_{ph} - I_d \tag{3-12}$$

where I_{ph} is the light generated current, and I_d is the diode current which given by:

$$I_d = I_o(Exp(\frac{V_j}{nV_T}) - 1) \tag{3-13}$$

where I_o is saturation current, V_j is the diode terminal voltage, n is ideality factor (1.2 to 2 based on manufacturing technology) and V_T is the thermal voltage that is given as:

$$V_T = \frac{KT}{q} \tag{3-14}$$

where q is electronic charge (1.6 x 10^{-19} C), K is Boltzmann's constant (1.38 x 10-23 J/K) and T is ambient temperature in Kelvin.

From (3-12), (3-13) and (3-14), the terminal voltage of the PV cell can be estimated as:

$$V_{pv} = \frac{nKT}{q} \ln\left(\frac{I_{ph} + I_o - I_{pv}}{I_o}\right) - I_{pv}R_s \tag{3-15}$$

Model parameters I_{pv}, R_S and I_O are required to be identified in order to enable the calculation of the I_{pv}/V_{pv} characteristics. These parameters can be approximated by applying two known conditions which are the short circuit and the open circuit conditions as follow:

Firstly: under the short circuit condition, referring to the ECM shown in Fig. 3-28, the diode current I_d is negligible under a very small diode terminal voltage (V_j) according to (3-13). So, the light generated current (I_{ph}) under a defined condition of temperature and irradiance can be

approximated to the short circuit current (I_{sc}) specified by the PV cell manufacturer under this condition, so that:

$$I_{pv} \approx I_{ph} \approx I_{sc} \tag{3-16}$$

Secondly: under the open circuit condition under the same conditions of temperature and irradiance specified for the short circuit condition above, the voltage of the PV cell under this condition is equal to specified open circuit voltage (V_{pv}= Voc). Accordingly, and by substituting (3-16) in (3-15) the reverse saturation current (I_O) for the PV cell can be approximated as:

$$I_O = \frac{I_{sc}}{e^{\frac{qV_{oc}}{nKT}} - 1} \tag{3-17}$$

Based on (3-17) the I/V characteristics of the PV cell can be obtained after using the available information from the cell datasheet for I_{sc} and V_{oc} and Rs under the specified conditions to estimate the saturation current I_o based on (3-15). Fig. 3-29 shows the simulated characteristics based on (3-17) for a S32 silicon PV cell produced by AZUR SPACE under different cell currents at ambient temperature of 28^{o}C and Irradiance of 1350W/m^2. The specified short circuit current and open circuit voltage of the cell are 1.081A and 0.628V respectively where the series resistance of the cell is 7mΩ [55]. As can be observed, there is a consistency between the specified values for Isc and Voc in cell's datasheet and the model generated ones. Also, the specified voltage at maximum power point (Vmpp) obtained from the model is 0.522V which is very close to the specified value (0.528V).

3.3.2 Effects of temperature and irradiance

In the previous sections, the Ipv/Vpv characteristics of the PV cell have been estimated under defined constant temperature and irradiance at which the specified values for I_{sc} and V_{oc} are given and used to estimate model parameters. However, these specified values change when these conditions vary. Therefore, it is required to develop an estimator for the I_{sc} and V_{oc} which can estimate the values of these parameters under changed temperature and irradiance. In order to develop this estimator, [56] suggested the implementation of correction factors for V_{oc} and I_{sc} based on the temperature coefficient which are provided in PV cell datasheet.

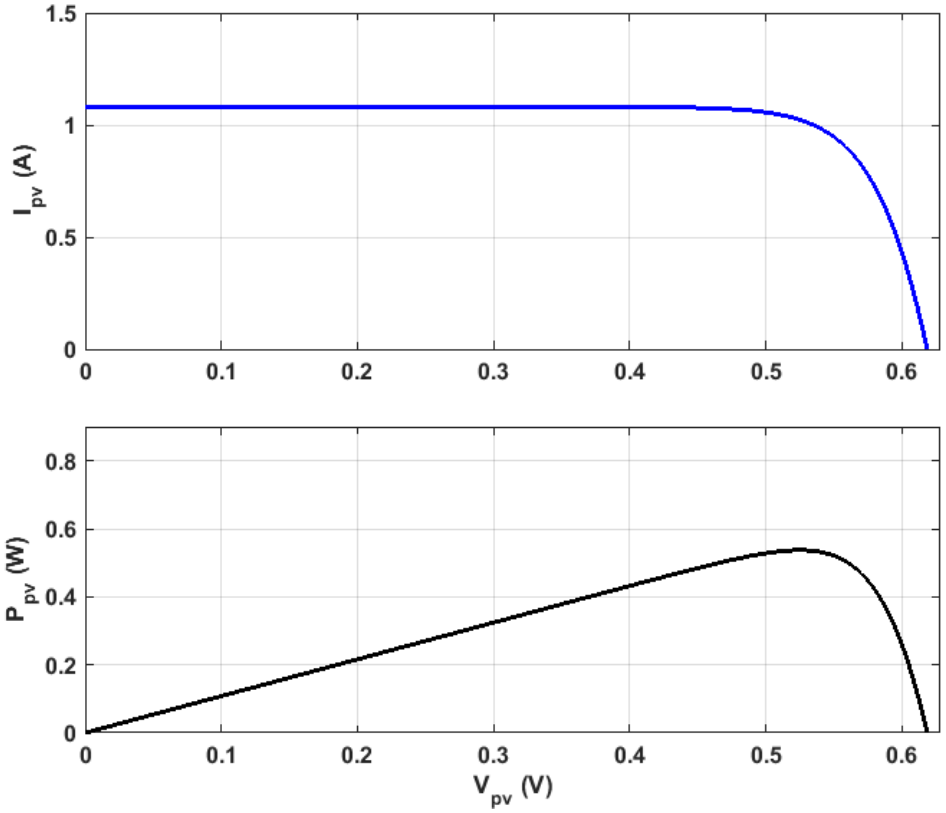


Fig. 3-29: simulated Ipv/Vpv and Ppv/Vpv characteristics of S32 silicon PV cell

Considering the parameters given in the PV cell data sheet for the short circuit current and open circuit voltage are I_{sc1} and V_{oc1} which are defined at cell temperature of T_{ref} and irradiance level

S_{ref}. For a different cell temperature of T_x, the cell parameters are assumed to be changed to I_{scx} and V_{ocx} which can be estimated as:

$$Iscx = Isc1 + \alpha(Tx - Tref) \tag{3-18}$$

$$Vocx = Voc1 + \beta(Tx - Tref) \tag{3-19}$$

where α and β are the temperature coefficients of the PV cell which are defined in the its datasheet.

The change of the irradiation mainly affects the short circuit current I_{sc} as can be observed form the linear relationship shown in Fig. 3-30. Accordingly, if the irradiance on the PV cell has been changed from S_{ref} to S_y under the same temperature, then the short circuit current at S_{ref} (I_{sc1}) will be changed to I_{scy} which can be calculated as:

$$Isc_y = Isc_1(1+\frac{S_y - S_{ref}}{S_{ref}}) \tag{3-20}$$

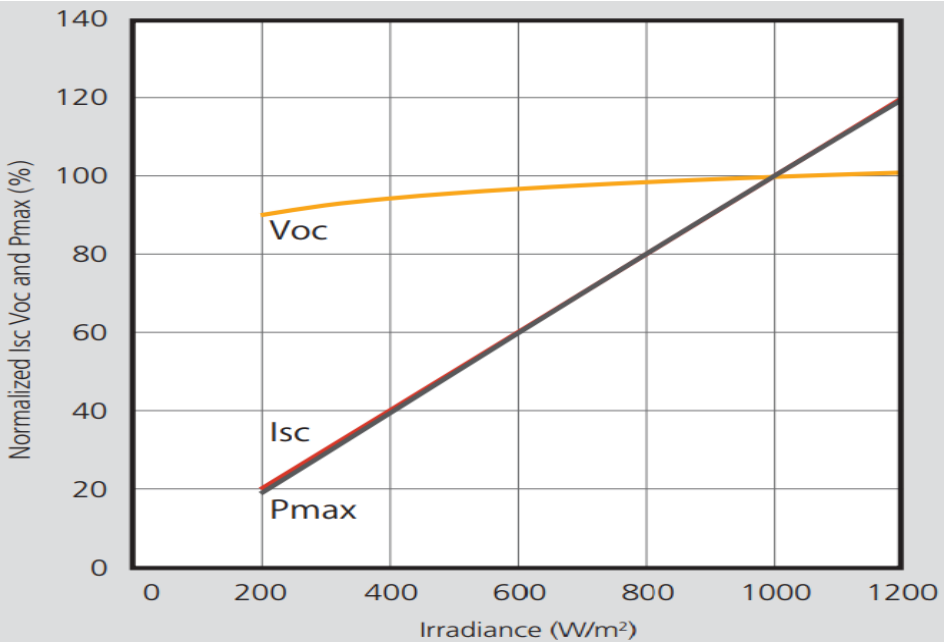


Fig. 3-30: Irradiance dependence of I_{sc}, V_{oc} and P_{max} at cell Temp. of 25°C [57]

Now, the complete PV cell model has been developed based on the specified parameters under defined conditions in the product datasheet. The model updates its parameters based on the current temperature and irradiance to keep an accurate estimate for the Ipv/Vpv characteristics of the PV cell. Fig. 3-31 shows the simulated Ipv/Vpv and Ppv/Ipv for the AZURSPACE S32 PV cell under different irradiance levels ranging from full irradiance (1350W/m^2) down to 20% irradiance (270W/m^2) all at a constant temperature of 28^{o}C. As can be observed, the change in irradiance mainly affects I_{sc} with minor impact on V_{oc}.

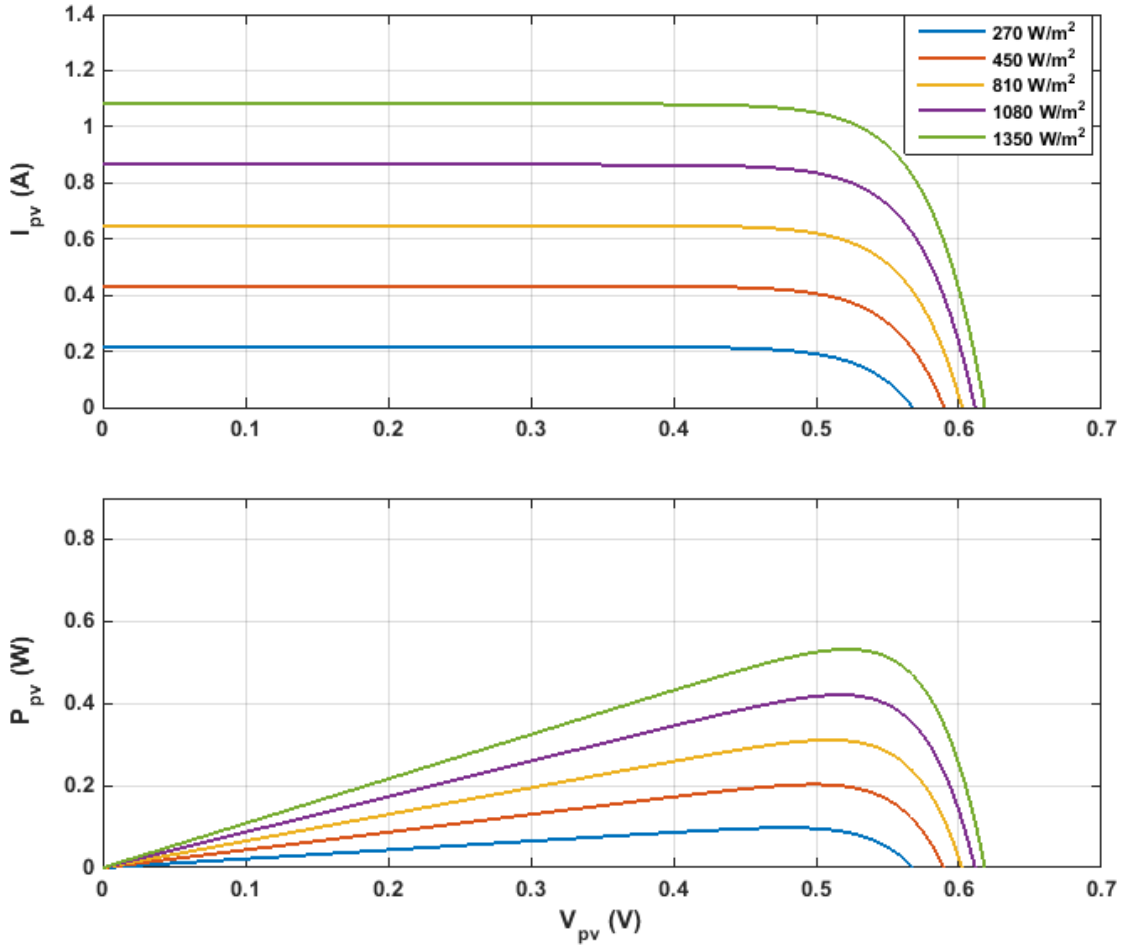


Fig. 3-31: Characteristics of S32 PV cell under different irradiances at cell temperature of 28^{o}C.

On the other hand, the change of the cell's temperature mainly affects V_{oc} with only a minor impact on the Isc as can be observed from

Fig. 3-32 which shows the simulated Ipv/Vpv and Ppv/Ipv for the same PV cell under different temperatures ranging from -60°C up to +60 °C all at constant irradiance of 1350W/m^2.This range represents the expected temperature variations of the satellite PV array during the single orbit

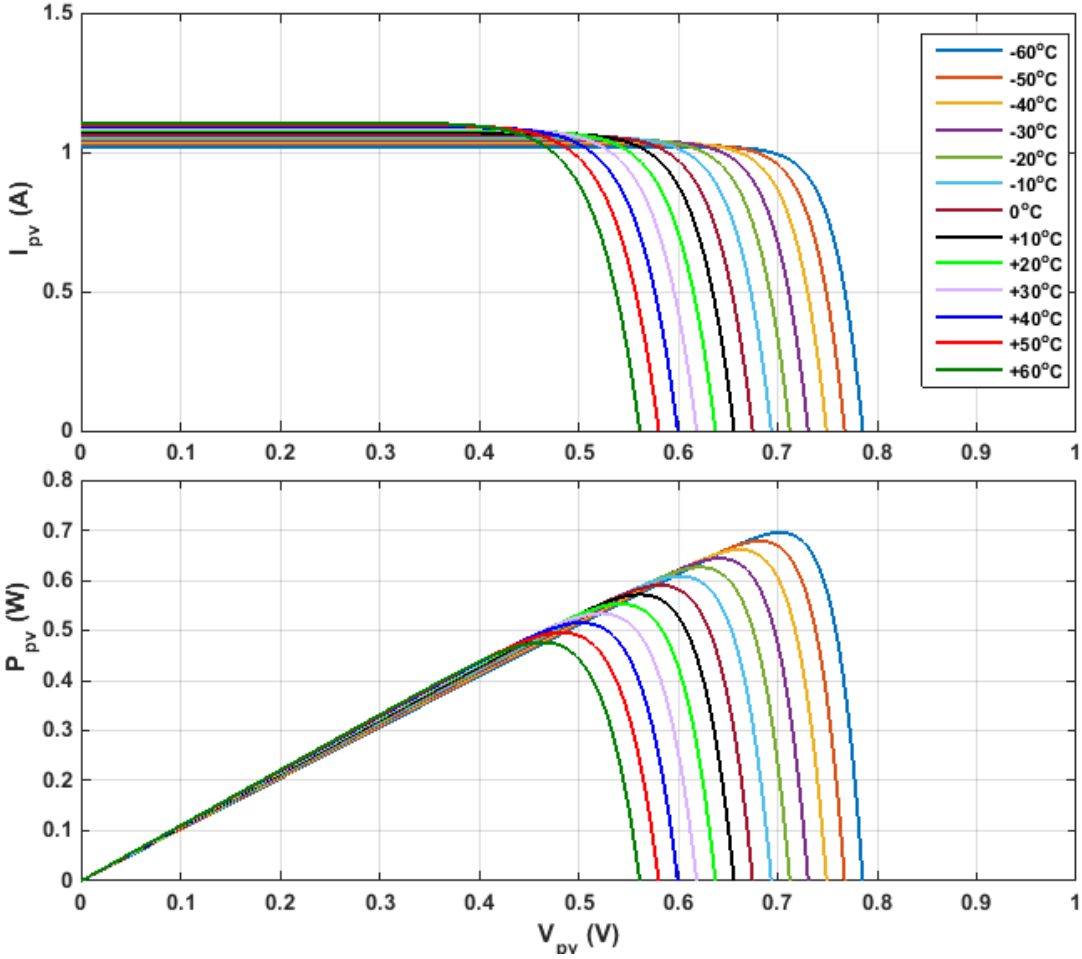


Fig. 3-32: Characteristics of S32 cell under different cell temperatures at irradiance of 1350W/m^2

3.3.3 PV cell model validation

In order to validate the developed PV cell model, the Ipv/Vpv characteristics have been estimated using the developed model under different temperatures and irradiances. These are compared with the specified parameters from the manufacturer product datasheet, for the silicon

PV cell, AZURSPACE S32 PV cell with the specified parameters shown in Table 3-3. The parameters used to validate the model are the temperature gradients for V_{oc}, I_{sc}, voltage at maximum power point (V_{mpp}) and power at maximum power point (P_{mpp}). The cell I_{pv}/V_{pv} and P_{pv}/V_{pv} characteristics obtained using the developed model under different temperatures and constant irradiance level shown in

Fig. 3-32 are used to quantify the effect of temperature on different parameters of the cell as can be seen in Fig. 3-33. Accordingly, model based temperature gradients for the cell parameters can be obtained from fitting the curves of different parameters against temperature. As can be seen, the model based estimated temperature gradient of V_{oc} is -1.9mV/ºC which is very close to the specified value (-2.02mV/ºC). Similarly, estimated temperature gradient of V_{mpp} is -2.1mV/ºC which is very close to the specified value (-2.07mV/ºC).

Table 3-3: Specified parameters for AZURSPACE S32PV cell [55].

Average Open Circuit V_{OC}	[mV]	628
Average Short Circuit I_{SC}	[mA/cm²]	45.8
Voltage at max. Power V_{pmax}	[mV]	528
Current at max. Power I_{pmax}	[mA/cm²]	43.4
Average Efficiency η_{bare}	[%]	16.9
Temperature Gradients		
Voltage dV_{oc}/dT	[mV/°C]	- 2.02
Short Circuit dI_{sc}/dT	[mA/cm²/C°]	0.030
Voltage dV_{pmax}/dT	[mV/°C]	- 2.07
Power dP_{mpax}/dT	[mW/cm²/°C]	0.004

The estimated temperature gradient of I_{sc} is +0.8mA/ºC which is very close to the specified value (0.71mA/ºC) given that the PV cell area is 23.61cm^2. Also, the estimated temperature gradient of P_{mpp} is -2.8mW/ºC whilst the specified value is (-0.09mW/ºC) which seems to be mistyped as it is incorrect considering the specified temperature gradient of V_{mpp} and I_{sc}.

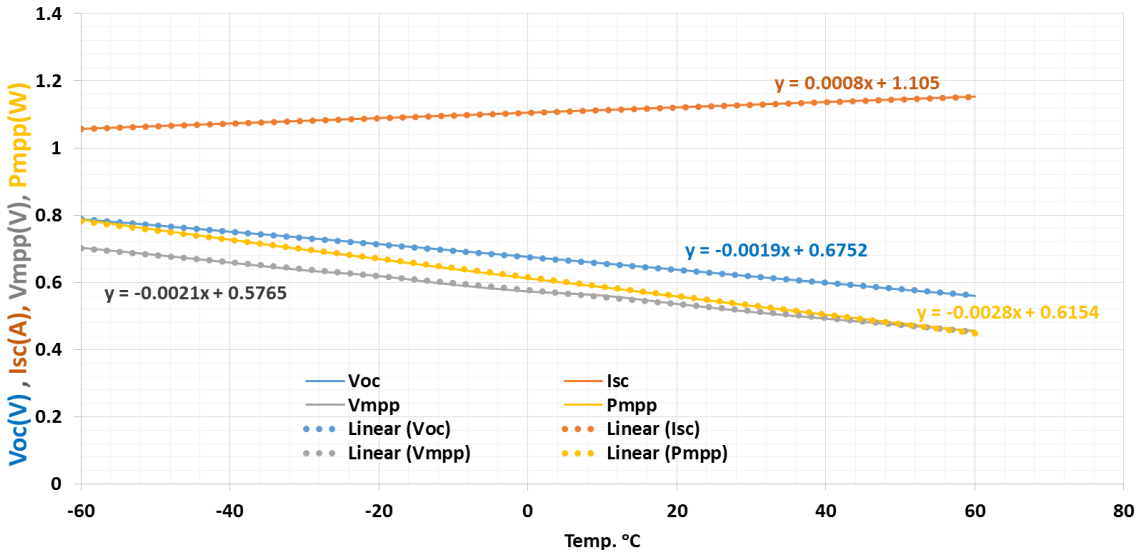


Fig. 3-33: model based estimated characteristics of AZURSPACE S32 PV cell under different cell temperatures at constant irradiance of 1350W/m^2.

Model parameters have been identified also to model the characteristics of the advanced AZRSPACE 3G30C triple junction GaAs higher efficiency (30%) PV cell. It has the parameters specified in Table 3-4 .

Table 3-4: Specified parameters for AZURSPACE 3G30C PV cell [16].

Average Open Circuit V_{oc}		[mV]	2700
Average Short Circuit I_{sc}		[mA]	520.2
Voltage at max. Power V_{mp}		[mV]	2411
Current at max. Power I_{mp}		[mA]	504.4
Average Efficiency η_{bare} (1367 W/m^2)		[%]	29.5
Average Efficiency η_{bare} (1353 W/m^2)		[%]	29.8
Open Circuit Voltage	$\Delta V_{oc}/\Delta T\uparrow$	[mV/°C]	- 6.0
Short Circuit Current	$\Delta I_{sc}/\Delta T\uparrow$	[mA/°C]	0.32
Voltage at max. Power	$\Delta V_{mp}/\Delta T\uparrow$	[mV/°C]	- 6.1
Current at max. Power	$\Delta I_{mp}/\Delta T\uparrow$	[mA/°C]	0.28

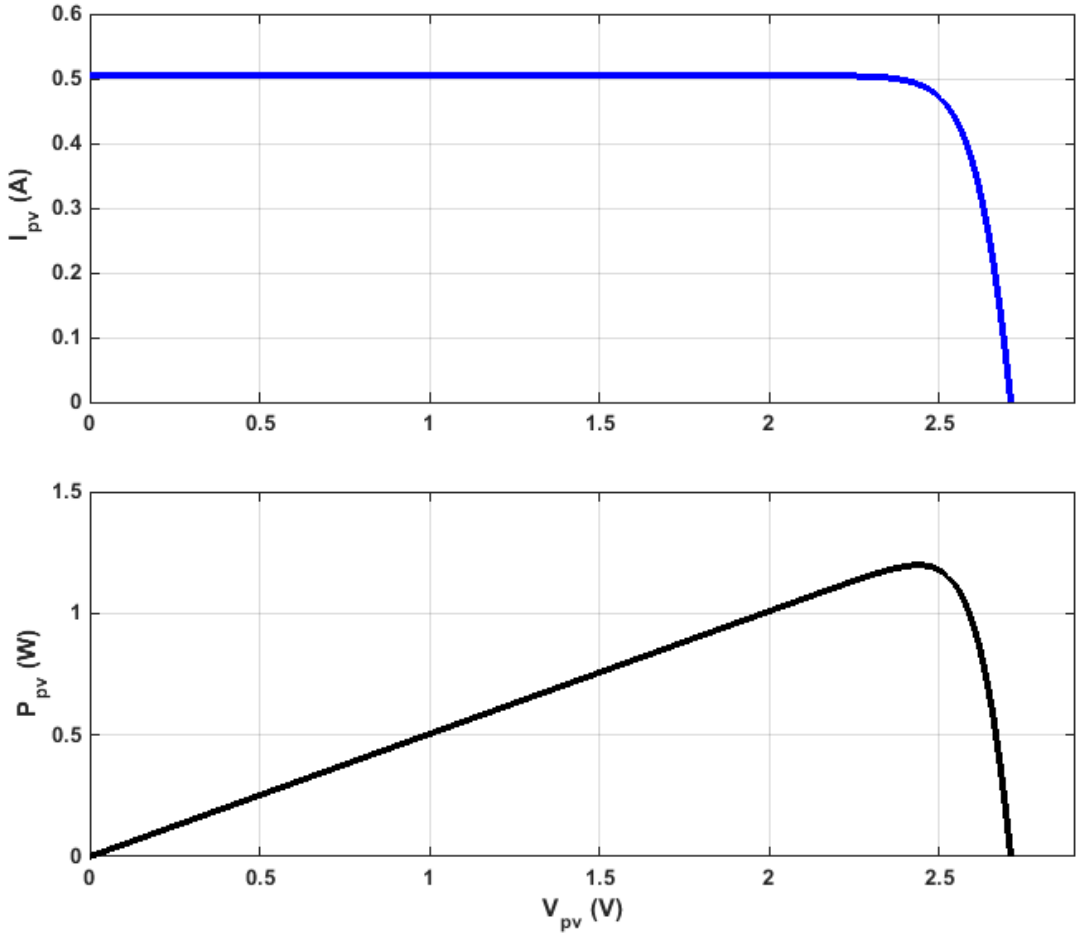


Fig. 3-34: Simulated Ipv/Vpv and Ppv/Vpv characteristics of 3G30C Tj PV cell

Fig. 3-34 shows the simulated characteristics of 3G30C Tj PV cell under different loading current at an ambient temperature of 28^{o}C and Irradiance of 1350W/m^2 . As can be seen, the model based estimated cell parameters V_{oc}, I_{sc}, V_{mpp} and I_{mpp} are 2.709V, 0.5047A, 2.44V and 0.491A respectively which are very close to the specified values in Table 3-4 (2.7V, 0.5044A, 2.41V and 0.504A). Also, the temperature gradients observed from the model show consistency with the specified values as can be observed form Fig. 3-35. The model based estimated temperature gradient of V_{oc} is -6.2mv/^{o}C which is very close to the specified value (-6 mv/^{o}C). Also the model based estimated temperature gradients of I_{sc} and V_{mpp} are 0.4mA/^{o}C and 6.4 mv/^{o}C respectively which are close to the specified values (0.32mA/^{o}C and 6.1 mv/^{o}C). From

the temperature based characteristics of the single junction silicon PV cell (S32) and the TJ PV cell (3G30C) shown , it can be observed that the temperature has a higher effect on the silicon PV (S32) cell, as it's V_{mpp} changed by ≈45% due to a change of 120°C in the cell's temperature where the TJ PV cell's V_{mpp} changed by ≈27%. Accordingly, the power outputs at the MPP of the two PV cells changes nearly by the same ratio, as the temperature has a minor effect on the I_{mpp}.

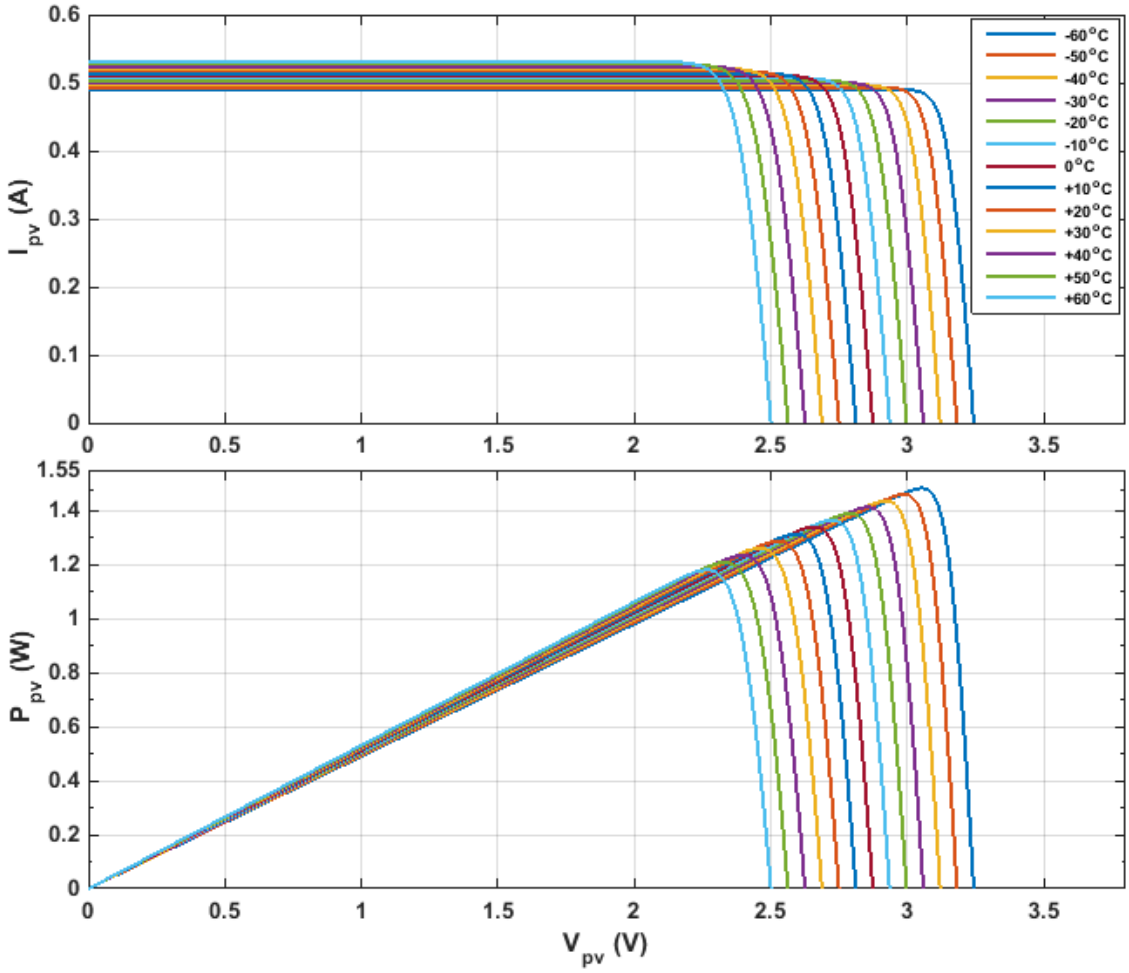


Fig. 3-35: Characteristics of 3G30C PV cell PV cell under different cell temperatures at an irradiance of 1350W/m^2

3.3.4 PV-panel modelling

As the developed PV cell model showed a good consistency with the specified parameters of the selected PV cells with errors in range of 5-8%, the cell model can be used to develop a PV-panel model. As the PV panels are simply constructed as series/parallel combinations of PV cells, it is easy now to build the PV-panel model based on the PV cell model developed by multiplying the cell voltage by the number of cells in series per string to obtain the voltage of the panel. The PV-panel current is found by multiplying the cell current by number of strings in parallel. Fig. 3-36 shows the simulated Ipv/Vpv and Ppv/Vpv characteristics of the PV panel constructed using AZURSPACE S32 PV cells which is constructed as 4 parallel strings (Np=4). Each string consists of 100 series connected PV cells (Ns= 100) in order to obtain the required voltage and power level.

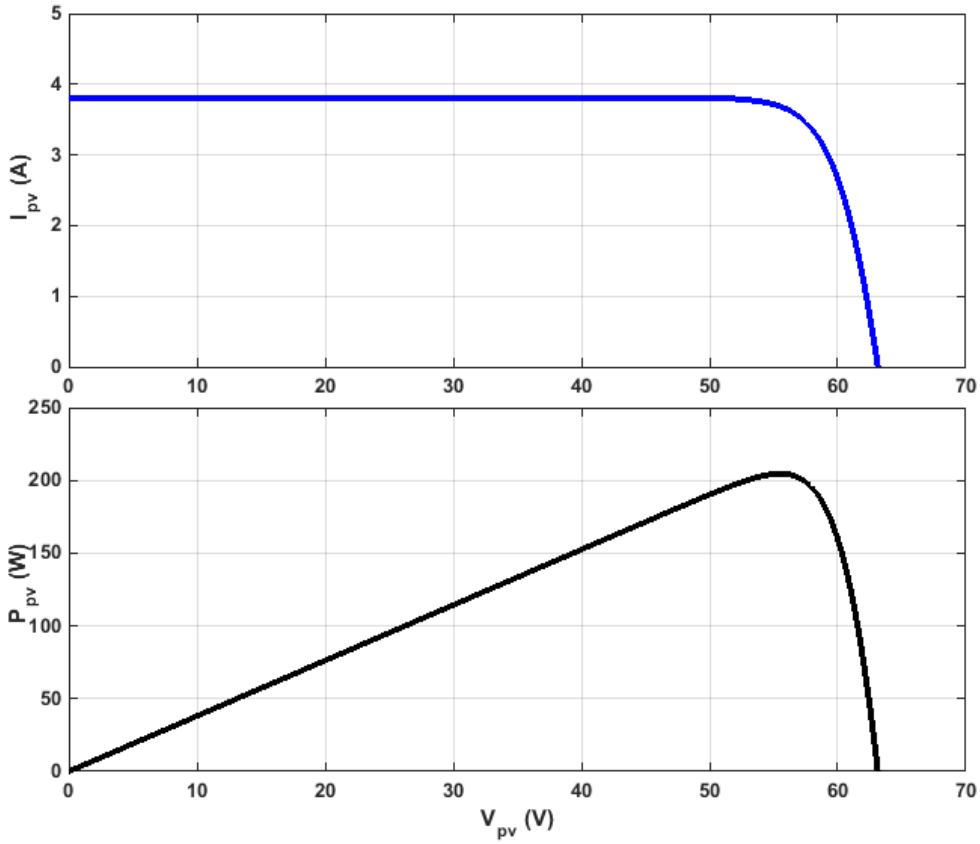


Fig. 3-36: Simulated Ipv/Vpv and Ppv/Vpv characteristics PV-panel constructed using AZURSPACE S32 PV cells (Ns=100, Np=4).

3.3.5 Thermal modelling of the PV-panel

As can be observed from the simulated characteristics of the PV-panel using the developed model, the irradiance and the panel temperature strongly affect the performance of the PV-panel. In this research, the satellite PV panel's orientation is considered to be sun-pointing during the illuminated period of the orbit by means of a sun tracking technique. This keeps the irradiation constant. Accordingly, the thermal characteristics of the PV panel will be considered as the only source which disturbs the generated power from the PV panels during the illuminated-period of the orbit. Accordingly, a PV panel thermal model with reasonable accuracy is required in order to estimate the temperature of the PV-panel during the orbit to evaluate its performance.

In order to produce a simplified thermal model for the PV-panel, the following assumption were made:

- The PV panel was assumed to be a single-lumped weight.

- Both sides of the PV panel are thermally coupled with the deep space radiation.

- The PV-panels are in sun-pointing position as mentioned earlier.

Based on the above assumptions, the thermal balance governing equation can be obtained as:

$$mCp\frac{dT}{dt} = Q_{FS} + Q_{BS} - k * \varepsilon_{FS} * A * (T^4 - T_\infty^4) - k * \varepsilon_{BS} * A * (T^4 - T_\infty^4) \qquad (3\text{-}21)$$

Where

mCp: PV panel thermal capacity

Q_{FS} : Incident heat rate on the PV panel front side

Q_{BS} : Incident heat rate on the PV panel backside

k : Stefan–Boltzmann constant (5.670 108 W/ m^2 K^4)

ε_{FS} : IR emittance of the PV panel front side

ε_{BS} : IR emittance of the PV panel backside

T : PV panel temperature.

T_∞ : Deep space temperature (0K)

A : PV panel area

The incident heat rate on the PV panel front Q_{cell} and back Q_{back} can be calculated as:

$$Q_{FS} = q_{Fs}A \tag{3-22}$$

$$Q_{BS} = q_{BS}A \tag{3-23}$$

where q_{FS} and q_{BS} are the incident heat flux on the PV panel front and back respectively, and A is the PV panel area.

Substituting (3-22) and (3-23) into (3-21), and by applying deep space condition (T_∞= 0K) then the PV panel temperature can be estimated as:

$$T = \frac{A}{mCp} \int (q_{FS} + q_{BS} - k * \varepsilon_{FS} * T^4 - k * \varepsilon_{BS} * T^4)dt \tag{3-24}$$

The heat flux on the PV array (q_{FS} and q_{BS}) are change within the orbit as the position of the PV panel with respect to the sun and the earth changes as the satellite orbits the earth as illustrated in Fig.3-37.

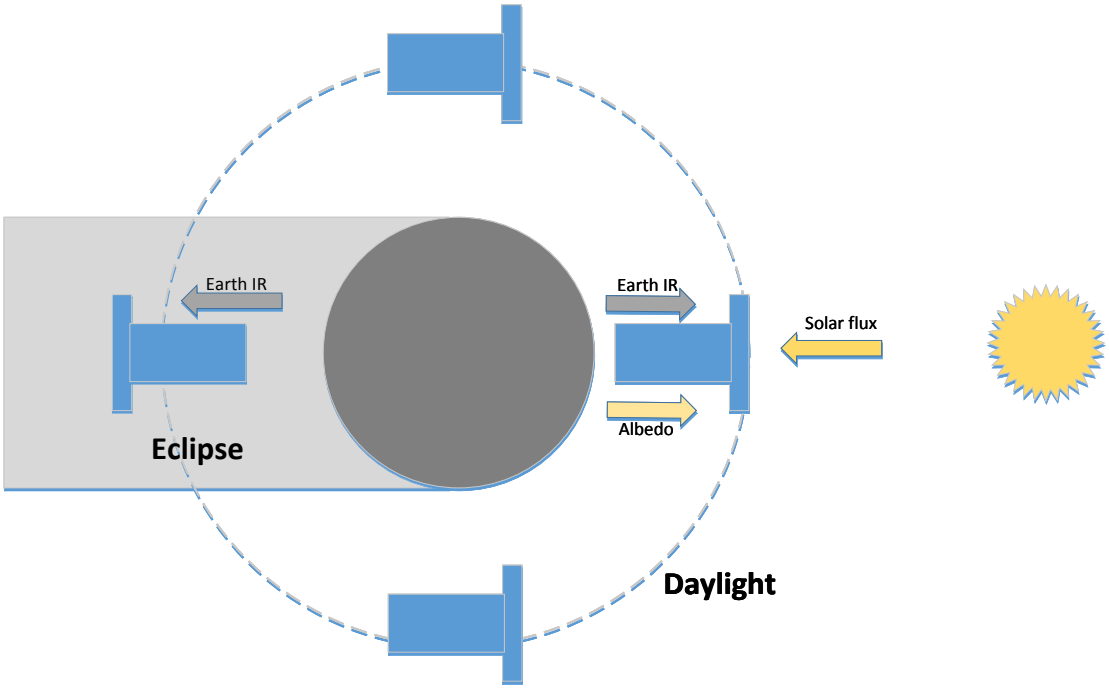


Fig.3-37 : In-orbit positions of satellite PV panels

During the daylight period of the orbit the PV panel front faces the sun flux (q_{solar}) and the panel back faces the earth albedo (q_{Albedo}) as well as the thermal power emitted from the earth in the form of infrared ($q_{earth\ IR}$) radiation. Accordingly, the incident heat flux on the PV panel front q_{cell} and back q_{back} during daylight can be calculated as:

$$q_{FS} = \alpha_{FS} q_{solar} \tag{3-25}$$

and

$$q_{BS} = \varepsilon_{BS} * q_{earth\ IR} + \alpha_{BS} * q_{Albedo} \tag{3-26}$$

where α_{FS} and α_{BS} are the solar absorptivity of the PV panel front and back respectively. The fluxes are q_{solar} = 1420W/m^2 , q_{Albedo} = β* q_{solar}, β =35% and $q_{earth\ IR}$ = 249 W/m^2 [58].

Based on the PV panel efficiency (η), a part of the PV flux absorbed by the panel front is converted to electrical power which should be deducted from that flux. Accordingly, the amount of the flux that contributes to heating of the panel can be calculated as:

$$q_{FS} = \alpha_{cell}\, q_{solar} - \eta * q_{solar} \tag{3-27}$$

rearranged as:

$$q_{FS} = (\alpha_{cell} - \eta) q_{solar} \tag{3-28}$$

The PV panel front parameters (α_{FS} and ε_{FS}) depend on the specifications of the PV cells provided by the manufacturer. However, the back parameters (α_{BS} and ε_{BS}) depend on the coating of the back of the PV panel which is selected to achieve a targeted thermal design to keep the PV panels temperature within targeted limits.

The PV panel thermal model has been developed for a panel modelled based on the AZURSPACE S32 PV cell which has front parameters given as (η = 16.9%, α_{cell} = 78% and ε_{cell} = 81%) [55]. The back parameters for the model developed have been selected based on the optimized thermal design proposed in [58] as (α_{back} = 20% and ε_{back} = 95) which is achieved by using SG121FD white paint. Also it should be considered that the back parameters change with the years in orbit by degradation of the painting materials.

Fig.3-38 shows the temperature and power of a PV panel within two orbits estimated based on these models implemented in the PSIM® simulation environment. The orbit considered is the low earth orbit (LEO) with 65 minutes of illuminated period and 35 minutes of eclipse and the PV panels in the sun-pointing position during the illuminated period. The estimated temperatures agreed with the expected temperature range mentioned in [18, 58, 59]. Also, the available power from the PV panel when the satellite just returns from the eclipse is ≈50% more

compared to the power at the steady state temperature (70ºC) due to the effect of the temperature on the voltage of the PV panel as discussed in the PV cell modelling subsection.

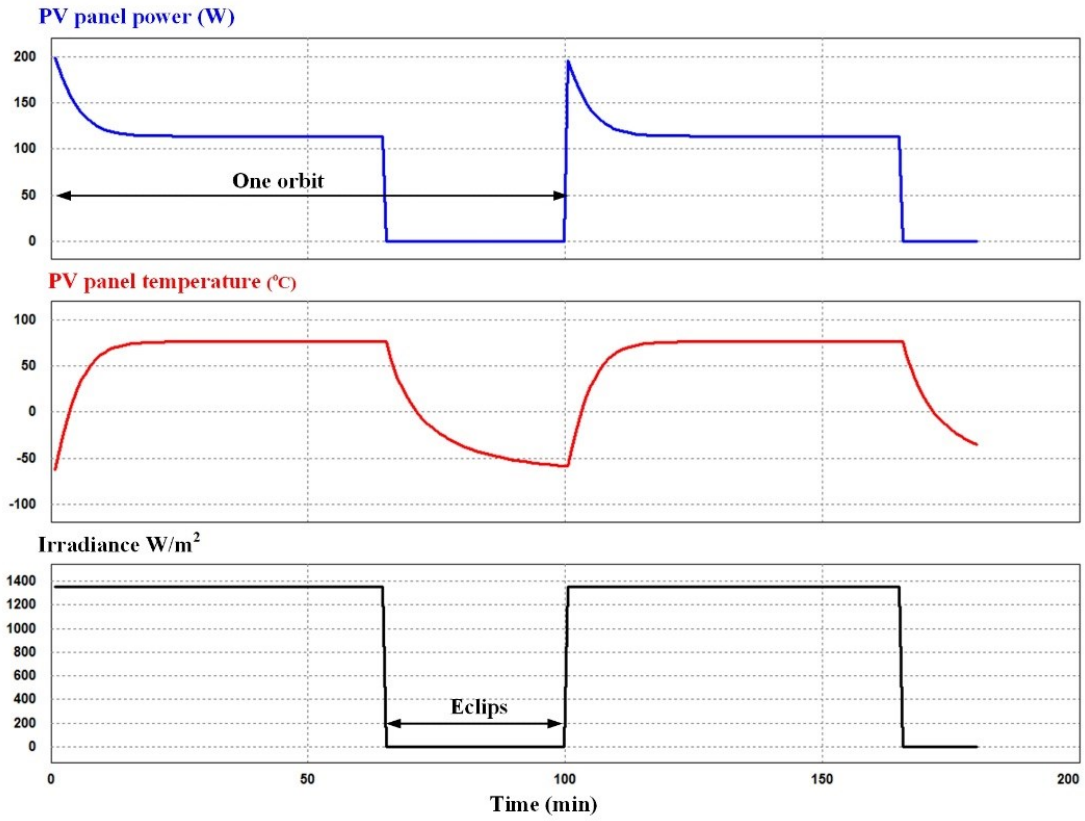


Fig.3-38: Irradiation and PV array temperature within two orbits

3.4 Load modelling

The scope of the research is to improve the EPS of small satellites (class 100kg) to enable the support of high power pulsed payloads without any significant increase in power system weight. The power consumption of the different subsystems for such types of small satellites is to be considered for both the lower power optical based imaging payloads and the high power radar based imaging payloads in order to evaluate effects of adding the high power pulsed loads to the design and performance of the EPS. For this class of small satellites with optical based imaging

payload, the power required during standby for satellite housekeeping electronics is in range of 55W and each orbit has a period of 10 minutes for communications with a total power consumption of 100W [60]. The load is modelled as constant power loads implemented in the PSIM® Simulation environment, and simulation results for the power consumption within two orbits are shown in Fig.3-39.

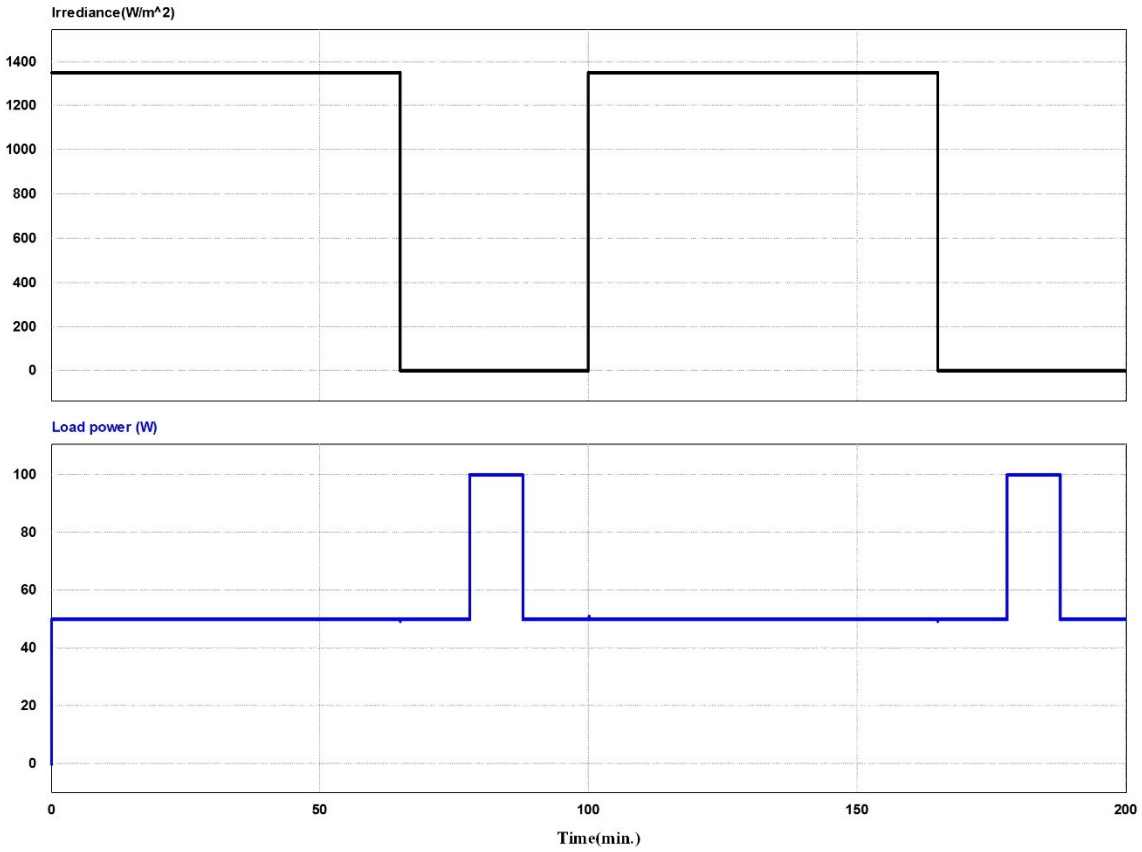


Fig.3-39: Simulation of power consumption of the satellite's subsystems over two orbits

For small satellites with pulsed power peaks like the case of a radar imaging payload, the standby power for satellite housekeeping electronics is still in the range of 50W as the same platform to be used. However, the 1kW pulsed power required by a radar imaging payload which should be added acts for ≈ 60 seconds as proposed in [3, 37]. Therefore the simulation of the load profile for such missions are shown in Fig.3-40.

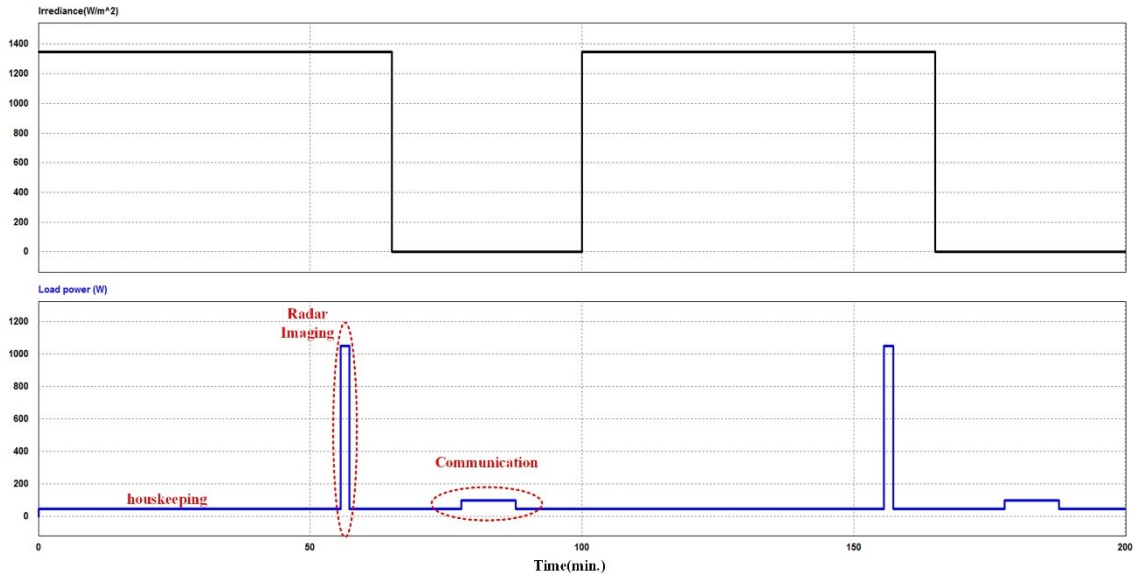


Fig.3-40: Power profile of radar imaging satellite over two orbits

3.5 Integrated model for satellite EPS

In order to complete the targeted model for the satellite EPS, it is required to have an estimate for the PV array size as well as the battery size as a key elements for power generation and storage. The sizing undertaken in the following section will be for a microsatellite platform with power requirements in range of 50W for housekeeping electronics during standby and 100W for a duration of 10 minutes during data transmission/receiving session. In Chapter 6, the resizing of the power system as well as energy storage options will be investigating in detail for supporting the pulsed power peak of (1kW) required for the radar imaging payload.

3.5.1 Sizing of the PV array

The size of the PV array required for the EPS depends on the energy required for the loads during the sun-duration and eclipse period taking into account the operating temperature range within the orbit and an additional 25% at least oversizing in order to compensate for the reduction of the efficiency of the PV cells due to degradation of the cells caused by doses of

space radiation [9]. Accordingly, the required energy to support the satellites power system's loads can be estimated as:

$$E_{total} = E_{sun} + E_{eclipse} \tag{3-29}$$

where:

$$E_{sun} = P_{Avg.(sun)} * t_{sun} \tag{3-30}$$

$$E_{\text{eclipse}} = P_{Avg.(\text{eclipse})} * t_{\text{eclipse}} \tag{3-31}$$

and $P_{av(sun)}$ and $P_{av(eclips)}$ are the load average power during the sun and eclipse periods respectively and t_{sun} and $t_{eclipse}$ are the sun and eclipse durations which are defined by the satellite orbit.

From (3-29) to (3-31), the required power from the PV array can be estimated as:

$$P_{pv.A} = \frac{\sum_{i=0}^{n} P_i * t_i + \sum_{x=0}^{n} P_x * t_x}{\eta_{PR} t_{sun}} \tag{3-32}$$

Where η_{PR} is the efficiency of the series regulator interfacing the PV-array, P_i is the power consumption of the (i^{th} load) and t_i is the duration of its operation considering the loads operated during the sun-duration (t_{sun}), and similarly for loads P_x operated during the eclipse period. For simplicity, the load converters assumed to have very high efficiency (≈1).

By considering the microsatellite mission at LEO orbit for the 65 minutes sun-duration and 35 minute eclipse with the proposed load profile, the required PV array power is calculated to be around 94Wconsidering 90% efficiency for the series regulator. However, considering the 25% over size for compensation of the degradation effects, the PV array size should be around

≈125W in total which can be subdivided into 3 or 4 panels according to the satellite structure design.

3.5.2 Battery sizing

As the battery is required to support the loads during the eclipse period, the size of the battery depends on the energy required during the eclipse time. On the other hand, the battery lifetime strongly depends on the depth of discharge (DoD) during the cycling of the battery. In order to ensure long life time of the battery, the battery DoD should be considered for the sizing of the battery as:

$$Battery\ Energy\ (Wh) = \frac{E_{eclipse}}{\eta_{dis} DoD} \tag{3-33}$$

where η_{dis} is the efficiency of the battery discharge regulator. For a targeted 5 years lifetime for the battery (≈ 30,000 cycle in LEO orbit), the DoD is advised to be 30%-35% as per the battery cell's datasheet [61].

The battery pack should be designed as a series/parallel combination in order to achieve the required voltage and required energy capacity defined by (3-33). Considering the proposed load profile, the required energy for loads during the eclipse period is around 37Wh. By considering 35% DoD and 90% efficiency of the battery discharge regulator, the battery size should be ≈119 Wh. By considering Li-ion battery cells with 3.6V nominal voltage and around 3Ah capacity, the battery pack can be constructed as a single string of 10-series connected cells to interface with a 28V power bus.

A complete simulation of the power system performance over one orbit based on the developed integrated model is shown in Fig.3-41 . The architecture of the power system considered here is the 28V regulated bus with MPPT.

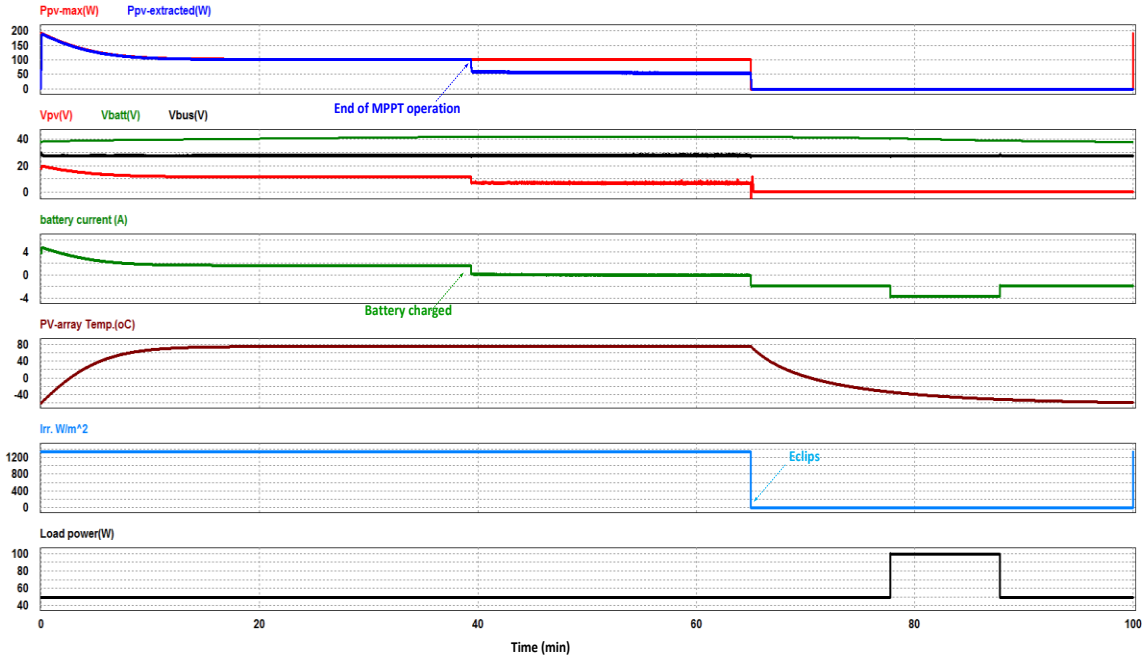


Fig.3-41: Power system performance over one orbit

As can be seen, the PV array's maximum available power changes as the temperature of the PV array changes. Accordingly, the MPPT acts to extract maximum power from the PV to supply the load and charge the battery. As the PV array is oversized to compensate for the decrease of its efficiency caused by degradation and space radiation effects, the energy generated from the PV at the beginning of life (BoL) will be more than the required energy. Accordingly, once the battery has become completely charged, the MPPT has to alter its operation to limit the extracted power from the PV to match the load power as can be seen in Fig.3-41. As the PV degrades its efficiency, the duration of the MPPT operation will be extended to compensate for the decrease in the power level to maintain the energy balance.

Summary

In this chapter, the models for different components of the satellite power system have been developed. The model developed for the battery cell showed good accuracy for estimating the power loss within the cell which will be used later in the following chapters to evaluate the stress on the battery cells under different power system designs. Similarly the supercapacitor cell model developed showed reasonable accuracy and will be used for the evaluation of the SC cell performance under the design evaluation of battery-supercapacitor hybrid energy storage investigated in Chapter6 for radar payload based satellites. PV cell/array model with reasonable accuracy has been developed to evaluate the performance of the PV array during the orbit and in addition a thermal model for the PV array has been developed as the temperature of the array changes significantly during the orbit which significantly affects its efficiency. Finally an integrated model for the EPS has been developed implementing the models developed for the battery and PV sized to fulfil the power requirements for common small satellites (50W continuous power for housekeeping electronics with peak of 100W for 10 minutes for communication) and a complete operation of the EPS has been simulated.

Chapter 4. Issues with Batteries and PV Strings

The higher power requirements for future satellites call for higher voltage buses in order to minimize the energy loss for power transmission and reduce the cables sizes. This in turn will require batteries and PV-arrays with higher voltages to interface to their power buses. Battery packs with high voltages require a series connection of a large number of battery cells in order to form the required pack voltage. The overall performance of such battery packs is highly affected by imbalances between the series connected cells as the overall capacity and power capability is limited by the weakest cells in the stack which results in sub-optimal utilization of its capabilities. Similarly, the performance of PV-strings formed by series connection of a large number of PV cells to form the required string voltage is limited by the weakest cells in the string and this effects the overall array performance. Within this chapter the different problems and limitations affecting PV and battery strings will be described as well as the different techniques which have been researched so far to address such problems. Also, a cascaded modular battery and PV system will be proposed and its benefits over the conventional system in terms of efficiency, weight and fault tolerance will be investigated.

4.1 Issues with battery strings

Battery packs are usually constructed as one or more strings in parallel in order to form the required pack capacity. Each string consists of a number of series-connected battery cells in order to form the required pack voltage. However, the individual cells within the single string are never identical due to the manufacturing tolerance or the different levels of degradation during cycling which cause a mismatch in terms of capacity and/or power capability of each cell. This mismatch affects the overall string/pack performance, as it is limited by the

performance of the weakest cell in the string which requires a charge/voltage balancing circuits in the conventional battery systems to avoid overcharging/overdischarging or stressing these weak cells as will be described in the following subsections.

4.1.1 Usable capacity of battery packs

In order to evaluate the effects of mismatch between battery cells on the behaviour of battery packs, a battery pack consisting of one string of *n* series connected battery cells has been considered to simplify the analysis. Accordingly, the total usable capacity (UC) of this battery pack can be approximated as:

$$U_{cap} = \frac{\sum_{i=1}^{n} Cap(cell_i)}{n} \tag{4-1}$$

where *Cap(Cell)* is the cell capacity. However, based on a capacity mismatch between the cells within the sting as demonstrated in Fig. 4-1, (4-1) can be redefined as:

$$U_{cap} = \underbrace{Cap(cell_{weak})}_{\textbf{DUC}} + \underbrace{(\frac{\sum_{i=1}^{n-1} Cap(cell_i)}{n-1} - Cap(cell_{weak}))}_{\textbf{CRAC}} \tag{4-2}$$

where Cap ($cell_{weak}$) is the capacity of the weakest cell in the string.

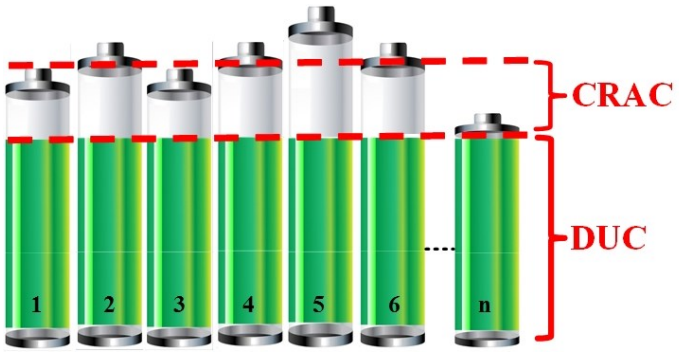


Fig. 4-1: Capacity mismatch of cells within a battery pack

Based on (4-2), the total usable capacity (U_{cap}) of the pack is consists of two terms. The first term is the direct usable capacity (DUC) that can be utilized directly without any additional circuitry. The second term represents the remaining part of the capacity which cannot be utilized unless there is an additional circuity to enable the utilization of this part without overcharging/overdischarging of the weak cells (with lower capacity). This part will be called the capacity requiring additional circuitry (CRAC). The function of the additional circuity, which built based on one of known topology that will be described later, is used with centralized battery systems (CBS) shown in Fig. 4-2 to perform charge balancing among battery cells to enable the utilization of the CRAC. The CRAC is determined by the capacity of the weakest cell as can be observed from (4-2), Assuming a 10% larger capacity fade of the weakest cell ($Cell_{weak}$) compared to other cells, this results in the CRAC of the battery pack to be 10 % of the overall usable capacity. Accordingly, without cell balancing/equalization circuitry in place, the battery pack loses 10% of its available usable capacity which forcing the implementation of balancing techniques.

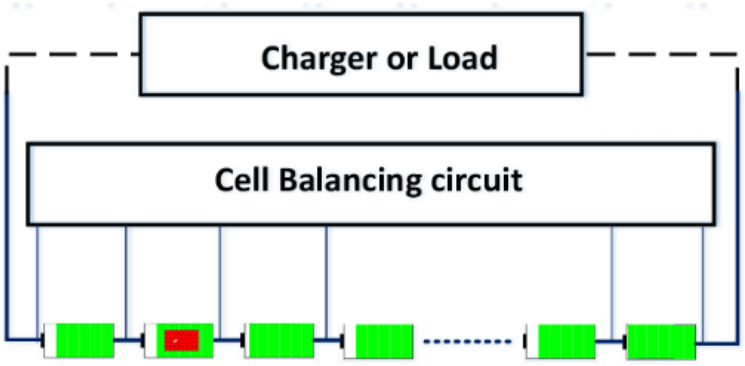


Fig. 4-2: battery system architecture of centralized battery system

4.1.2 Charge balancing techniques

The charge balancing techniques of battery cells are classified into two main categories. The first one is passive balancing which depend on the dissipation of the excess energy from cells

with higher states of charge (SoC) by means of shunt resistors [62, 63]. The second category is active balancing that depend on the transfer of the extra energy from the cells at higher SoC to the cells with lower SoC through inductors, capacitors or transformers. Within the following subsections a review of the different balancing techniques will be provided, including their advantages and limitations.

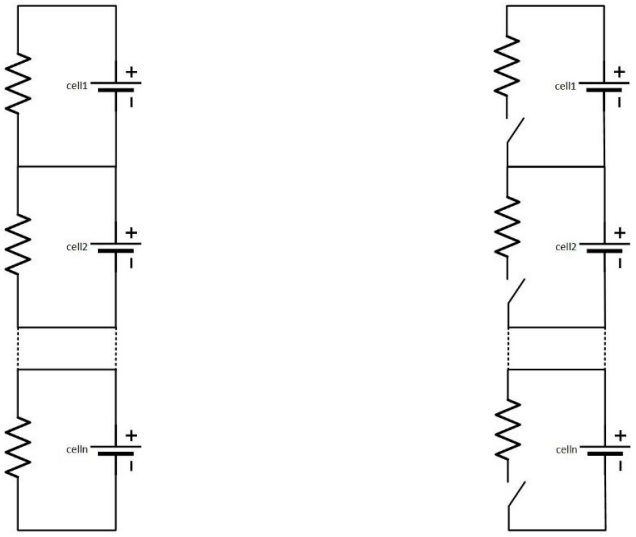
4.1.2.1 Passive balancing techniques

Passive balancing techniques rely on the dissipation of the excess energy from the cells which are at higher SoC by means of shunt resistors. The dissipation method can be either through a fixed shunt resistor (FSR) or a switched shunt resistor (SSR). The FSR technique [62, 64] uses *n* shunt resistors connected across *n* battery cells as shown in Fig 4.3a. The current drawn by each resistor is linearly proportional to the voltage of each battery cell, so the cells at higher voltage will drive higher currents through their shunt resistors resulting in decreasing the voltage difference among cells. It can be observed that the balancing currents through the shunt resistor and accordingly the balancing time cannot be controlled and the voltage of the battery cells are not fully regulated which make it unsuitable for Li-ion batteries because they are very sensitive to overvoltage [62].

In order to control the balancing current through the shunt resistors, the SSR method implants control switches as shown in

Fig. 4-3 (b) [63, 65, 66]. A control circuit controls the switches to prevent overcharging of the cells at higher SoC while allowing cells at lower SoC to continue charging. The control of the switches can be either in continuous mode by controlling all the switches using the same control signal, or in detection mode in which the activation of the switches is done based on measured voltages. Although the SSR method has the advantage of balancing current regulation compared

to the FSR method, both methods are not efficient as they rely on the dissipation of the excess energy which brings the need for a thermal control (with added weight) due to the generated heat. Additionally, since this energy dissipated inside satellite body it negatively impact its thermal control system.



(a) (b)

Fig. 4-3: Passive balancing techniques with (a) fixed shunt resistors method and (b) switched shunt resistors method

4.1.2.2 Active balancing techniques

The active balancing techniques have the advantage of being efficient as the operating principle of these techniques is based on the manipulation of the energy between unbalanced cells until the pack reaches a state of balanced SoCs instead of dissipating the excess energy as with the passive balancing techniques. The active balancing techniques are divided into inductor/transformer based active balancing techniques and capacitor based active balancing techniques.

4.1.2.2.1 Inductor/transformer based balancing techniques

Inductor/transformer based balancing techniques are usually designed based on the implementation of inductors or transformers to manipulate the energy between battery cells until the pack reaches a charge balanced state. The inductor based techniques can be divided into single inductor based techniques and multi-inductor based techniques. The transformer based techniques are divided into single-winding transformer based techniques, multi-winding transformer based techniques, and multiple transformers.

4.1.2.2.1.1 Single inductor technique

The single inductor (SI) based active balancing technique proposed in [67] is constructed using 2*n* switches, 2*n* diodes and a single inductor for balancing a string of *n*-series connected cells as shown in Fig. 4-4. The operating principle of the circuit is based on the transfer of energy from cells at higher SoC to cells at lower SoC using the inductor as an energy buffer.

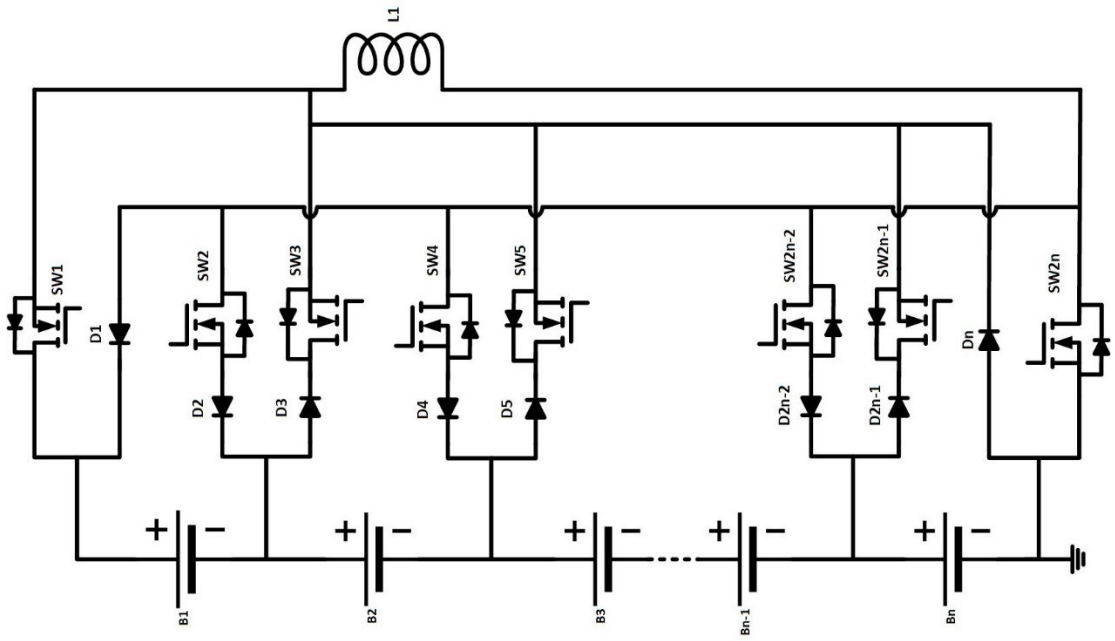


Fig. 4-4: Single inductor based active balancing technique

For example, if the battery cell B1 is at the highest SoC and cell B2 is at the lowest, then the energy should be transferred from B1 to B2. Accordingly, the switches SW1 and SW2 are initially turned on to charge the inductor, then SW1 is turned off and switch SW4 is turned on to transfer energy stored in the inductor to cell B2. Although this technique is efficient and can handle a reasonable balancing current, the balancing speed can be very slow, especially when many cells are unbalanced as the balancing of the cells has to be made sequentially due to the use of a single inductor.

4.1.2.2.1.2 Multi-inductors technique

The multi-inductor (MI) based balancing techniques implements *n-1* sub-modules (SM) to balance a string of *n* series connected cells. Each SM consists of two switches and an inductor as shown in Fig. 4-5 [64]. Using this technique, the energy can be manipulated between the adjacent cells which leads to a longer balancing time if energy needs to be transferred between two nonadjacent cells. Also, this technique is bulky due to the large number of inductors and these will also contribute to energy losses due to the core and copper losses of these inductors [68].

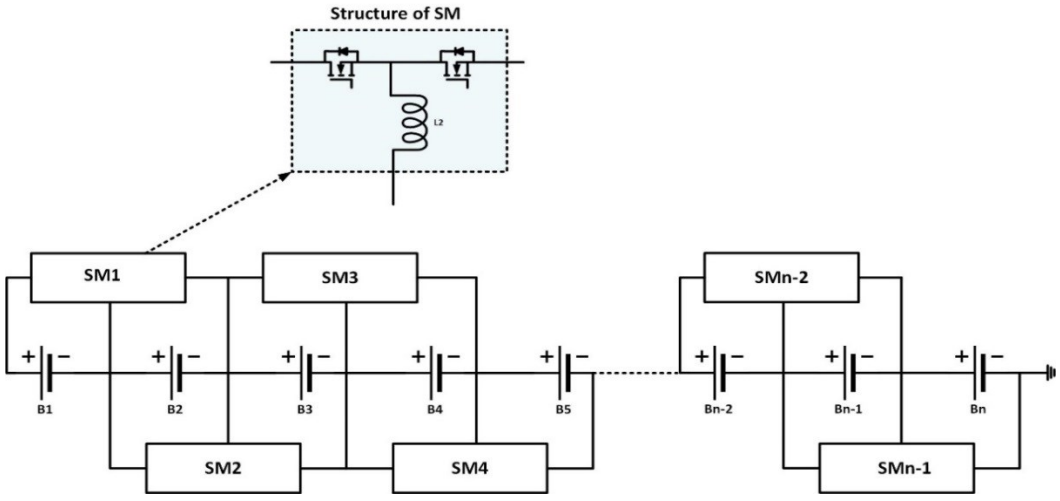


Fig. 4-5: Multi-inductor based active balancing technique

4.1.2.2.1.3 Single winding transformer technique

The single winding transformer (SWT) technique implements a single transformer to manipulate the energy between the unbalanced battery cells using the Pack-to-Cell technique or the Cell-to-Pack topologies. The Pack-to-Cell topology as shown in Fig. 4-6, transfers the energy from the whole pack through the switching transformer to the weak cell(s) using the corresponding switch(s) [65, 66].

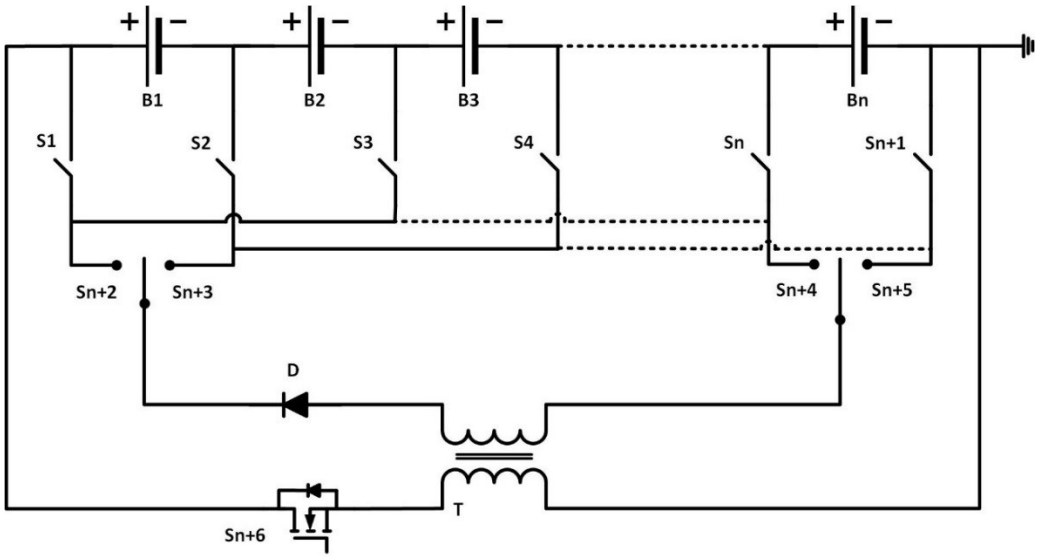


Fig. 4-6: Pack-to-Cell single winding transformer topology

The second topology is Cell-to-Pack which transfers energy from the cells at higher SoC through the transformer to the battery pack until all cells reach equal SoC [69]. This topology implements *2n+1* switches, *2n-1* diodes and a single transformer as shown in Fig. 4-7. Although the single winding transformer topologies can achieve a fast balancing speed at lower core losses, it requires a complex control and is not expandable as the transformer must be changed if more cells need to be added to the design of battery pack.

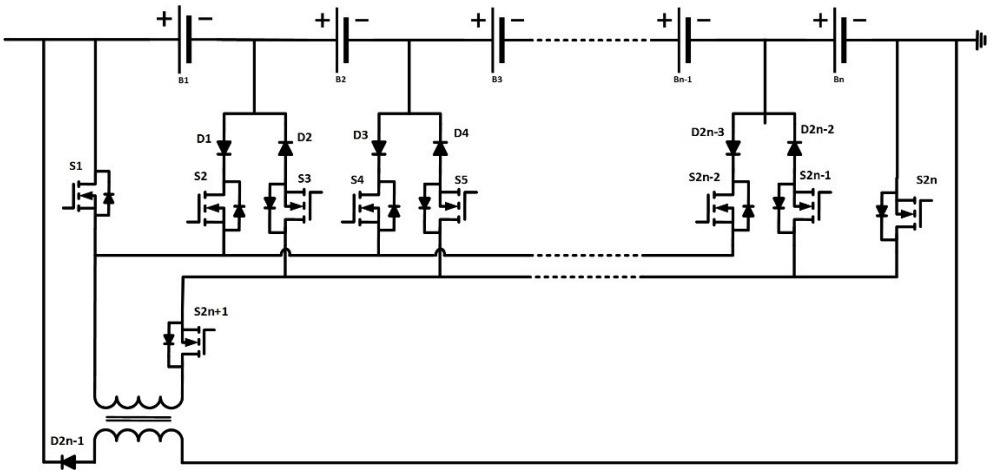
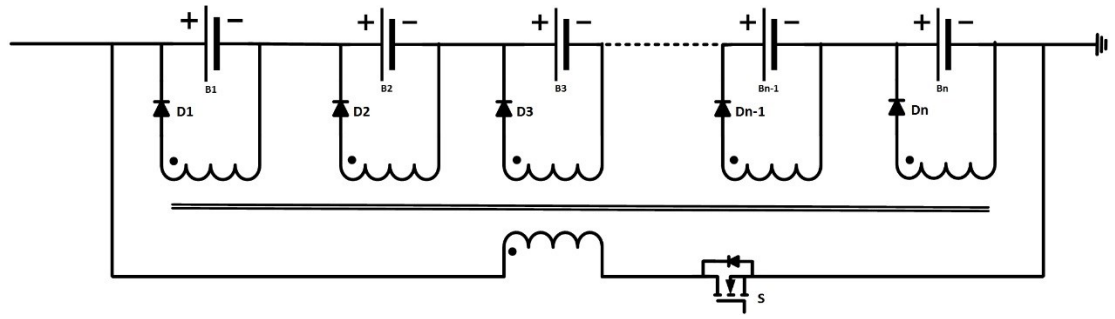


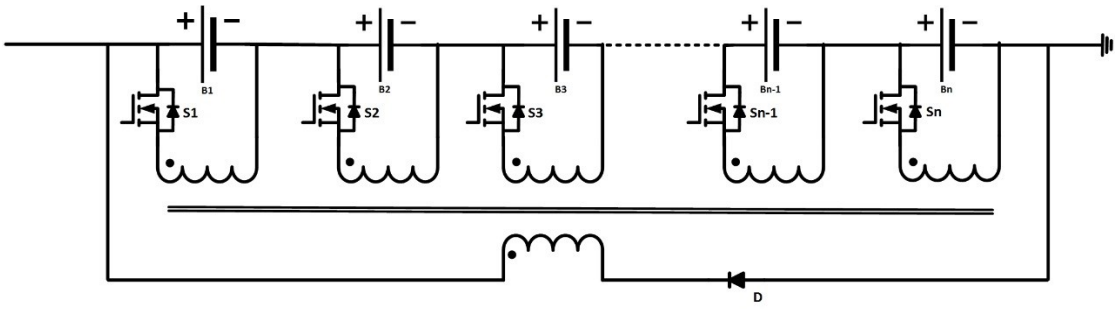
Fig. 4-7: Cell-to-pack Single winding transformer topology

4.1.2.2.1.4 Multi-winding transformer techniques

The multi-winding transformer (MWT) based balancing topology implements a single transformer with one primary winding and *n* secondary windings for balancing of *n* series connected battery cells. The MWT technique has two topologies: the first is the flyback topology which utilizes *n* diodes and one switch in additional to the transformer as shown in Fig. 4-8(a). The operating principle of this topology is based on energizing the primary winding of the transformer by switching-on S1, then when S1 switched-off the energy will be transferred to the secondary windings and the induced current charges cells at lower voltages through the corresponding diodes. The second topology of the MWT is the forward topology which utilizes *n* switches and a single diode in addition to the transformer as shown in Fig. 4-8(b). In this topology, the corresponding switch connects cells that have the highest voltage/SoC to the corresponding secondary winding, which enables the transfer of energy from this specific cells to all the others through the transformer and the anti-parallel diodes of the switches. The MWT technique has higher balancing speed but at the cost of a complex structure and it is also not expandable.



(a)



(b)

Fig. 4-8: the MWT balancing with: (a) flyback topology (b) forward topology

4.1.2.2.1.5 Multiple transformer technique

The multiple transformer (MT) balancing techniques implements *n* transformers, *n* diodes and a single switch for balancing of *n* battery cells [65, 70] as shown in Fig. 4-9. The balancing current is drawn from the whole battery pack through the transformers' primary winding and transferred to all the secondary windings and hence to the cells through the diodes. The charging currents through the cells are determined by the voltage of the cells. This method is more flexible for expansion compared to the MWT but it is bulky due to the large number of transformers.

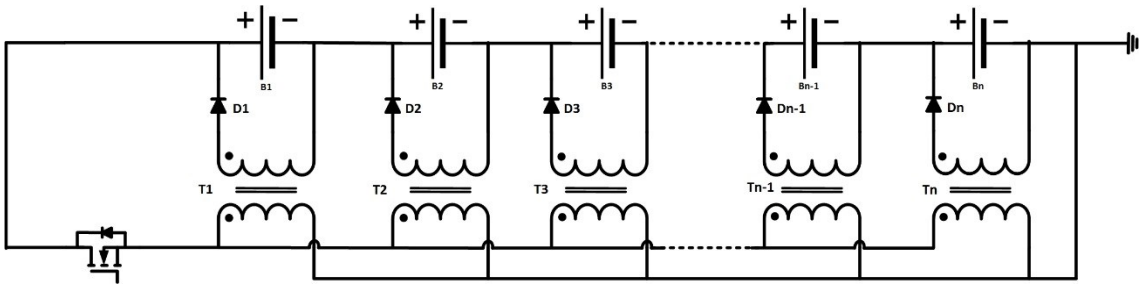


Fig. 4-9: Multi transformer based balancing circuit

4.1.2.2.2 Capacitor based balancing techniques

Capacitor-based balancing techniques implement capacitors for energy manipulation between battery cells instead of inductors and transformers. They can be divided into switched capacitors, single switched capacitors, double-tiered switched capacitors, and modularised switched capacitors.

4.1.2.2.2.1 Switched capacitor technique

The switched capacitor balancing technique implements *n-1* capacitors and *2n* switches for balancing of *n* series-connected battery cells [65, 71] as shown in Fig. 4-10. The energy is transferred between the adjacent cells through the shared capacitor which switches between the two cells by controlling the appropriate switches. This method requires a simple control strategy as it has two states only. However, it is bulky due to the large number of capacitors and the balancing speed is very limited [65].

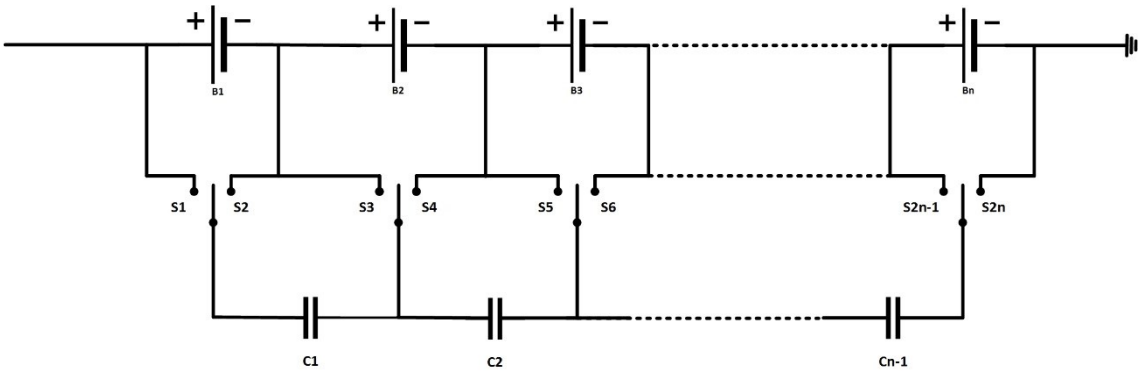


Fig. 4-10: Switched capacitors balancing circuit

4.1.2.2.2.2 Single switched capacitor technique

The single switched capacitor (SSC) balancing technique can be considered as a derivation from the switched capacitor technique. However, it utilizes only one capacitor to manipulate the energy between the battery cells. As can be seen in Fig. 4-11 , it utilizes *n+5* switches and a single capacitor for balancing *n* series-connected battery cells [65, 66, 72]. The control strategy of this technique is such that the highest and lowest voltage cells are selected for energy manipulation using the corresponding switches and capacitor, until a balanced state is reached. Although this method has a reduced size compared to the switched capacitor method, the balancing speed still is very slow especially when more cells need to be balanced.

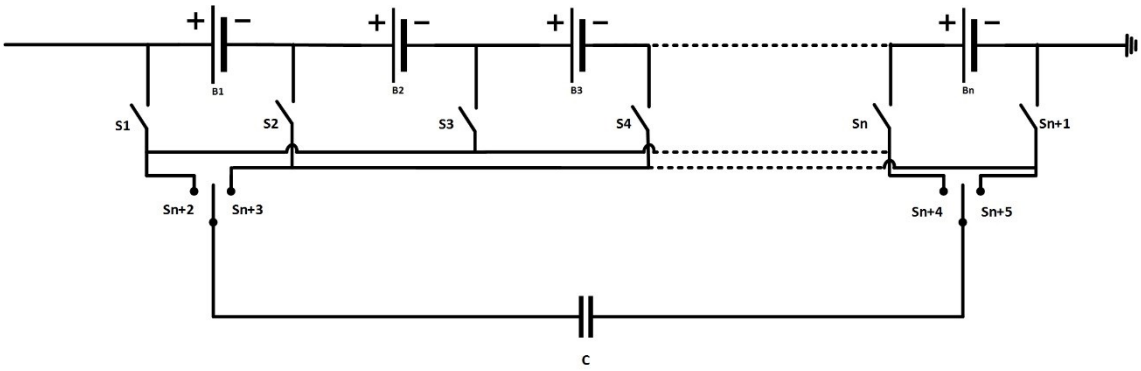


Fig. 4-11: Single switched capacitors balancing circuit

4.1.2.2.2.3 Double-tiered switched capacitor technique

The double tiered switched capacitor (DTSC) balancing technique implements two tiers of capacitors in order to reduce the balancing time [65, 72, 73]. The DTSC implements 1.5(*n-1)* capacitors and *2n* switches for balancing of a string of *n* series connected battery cells (which must be an odd number) as shown in Fig. 4-12 .The idea of this technique is similar the switched capacitor balancing technique, but it implants a second tier to enable the energy manipulation between non-adjacent cells in order to increase the balancing speed. Although this technique can achieve a faster balancing speed compared to the switched capacitor technique, it still has the disadvantage of being bulky due to the large number of capacitors.

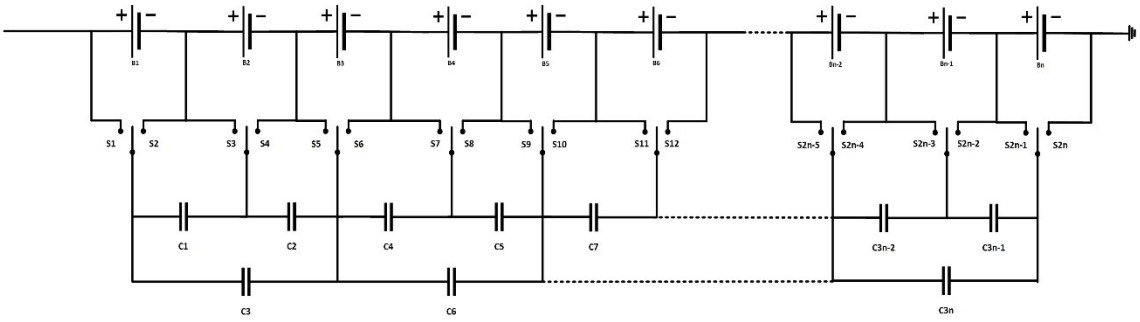


Fig. 4-12: Double-tiered switched capacitor circuit

4.1.2.2.2.4 Modularized switched capacitor technique

In order to eliminate the number of capacitors used for balancing in the DTSC balancing technique especially for battery strings with a large number of battery cells, the modularized switched capacitor (MSC) technique has been proposed in [74]. This technique divides the *n* battery cells into a number of modules and each module consists of a number of series connected battery cells with separate balancing through the switched capacitor technique. In

addition, another equaliser is added externally to achieve balancing between adjacent modules as shown in Fig. 4-13. Although this technique can achieve reasonable balancing speed for battery strings with a large number of cells, it still requires a large number of capacitors resulting in a bulky system.

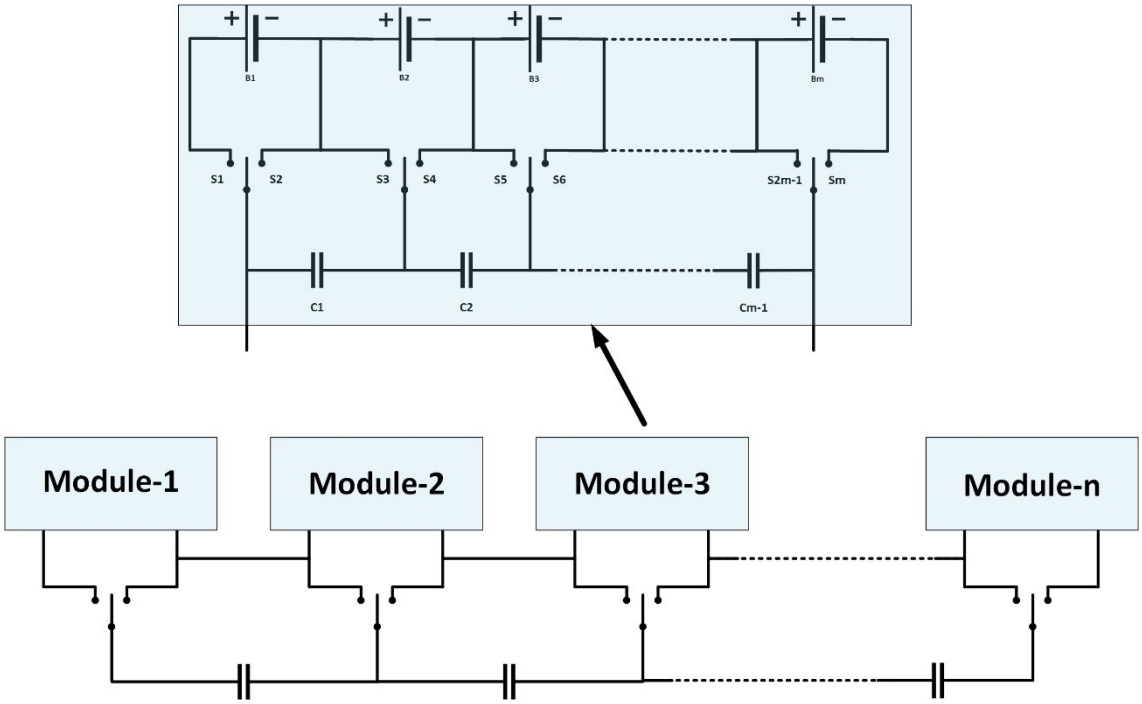
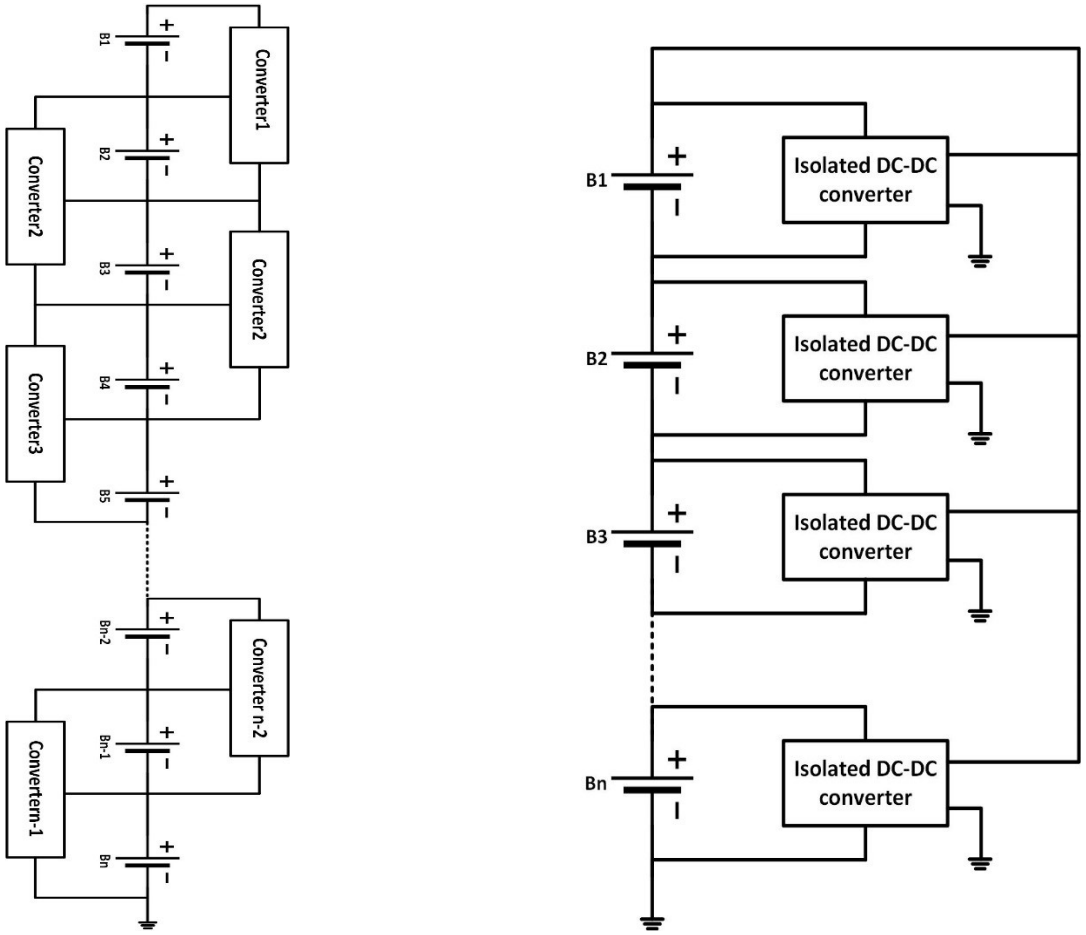


Fig. 4-13: MSC balancing circuit

4.1.2.2.2.5 Converter based balancing techniques

The converter based balancing techniques utilizes one of the known converter topologies either for Cell-to-Cell (C2C) energy manipulations [75-79] as shown in Fig. 4-14(a) , or Cell-to-String (C2S)/String-to-Cell(S2C) energy manipulation by means of isolated converters [80-82] as shown in Fig. 4-14(b). It can be observed that the C2C topology requires a large number of converters with associated passive elements which will contribute to the system weight as well as complexity. On the other hand, the C2S/S2C topology requires high gain converters in order to interface the cells to the string voltage which affecting its size and efficiency.



(a) (b)

Fig. 4-14: Converter based balancing system: (a) C2C topology (b) C2S/S2C topology

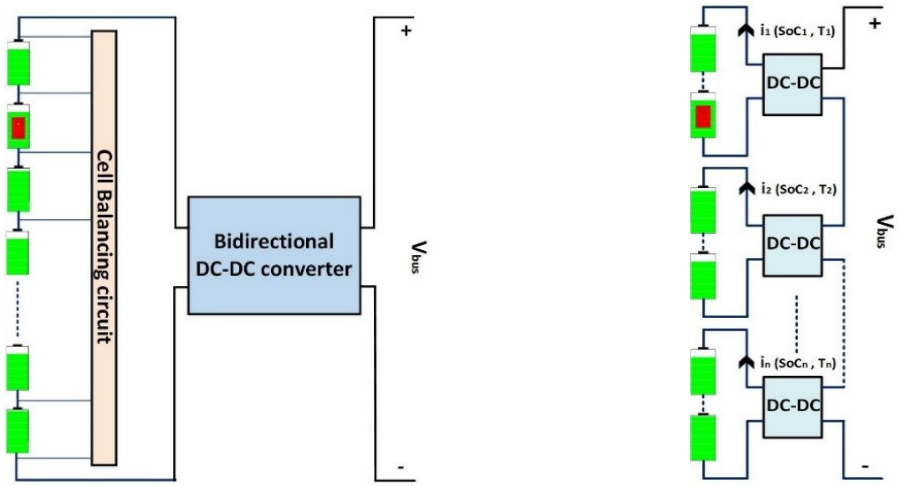
In conclusion, the battery balancing techniques that depends on either passive or active topologies represent added weight and complexity to battery management system due to the large number of switches and energy dissipating/manipulating devices. Although the inductors/transformers based active balancing techniques are more energy efficient compared to the passive techniques as it relys on manipulating the energy from cells at higher SoC to cells at lower SoC rather than dissipate it in the form of heat as in passive balancing techniques, it still have some losses due to core and copper losses as well as switches losses. The capacitor based active balancing techniques have fewer losses compared to the inductors/transformers

techniques but in the cost of added weight/size introduced by the implementation of the capacitors as energy storage element.

4.1.3 Alternative battery management techniques

Conventional centralized battery systems (CCBS) usually implement a centralized bidirectional DC-DC converter acting as a charge/discharge regulator (CDR) rated at the full power/voltage of the battery pack in additional to a cell balancing system which designed based on one of the previously described balancing techniques as shown in Fig. 4-15.

The main advantage of the CCBS is that it is simple, requiring a single converter with its dedicated measurements. However, it has many disadvantages including poor efficiency and reliability due to the centralized architecture. Also the CCBS is not inherently fault tolerant as any failure in one or more battery cells or in the central converter makes the overall battery system unusable. Also, the implemented cell balancing systems affect the overall system performance. Firstly, they can contribute to overall system energy loss due to power dissipation (in the case of passive balancing), or converter losses during energy redirection between battery cells (in the case of active balancing). Secondly, if any particular cell reached the voltage limits during charging or discharging due to the limited capability of the implemented balancing technique, the charge/discharge process for the whole string needs to be halted until the balancing system recovers to the limit of these cells [63]. The halt time will cause the charging time to be increased and may cause loss of available energy e.g. in the case of charging from a limited availability power source such PV arrays which is the case in satellite EPS applications.



(a) (b)

Fig. 4-15: Battery system architectures: (a) CCBS (b) CMBS

An additional limitation of CCBS is that they cannot balance the thermal stress among cells with mismatched impedances which is significant as it can be up to 20% at the beginning of life (BoL) [83], and may reach a large value with cycling over years of services. Loading all cells with the same power share under this impedance mismatching can contribute to the temperature rises in some cells further affecting its life time. Based on this, it is important for the BMS to perform a power share balancing (PSB) strategy in addition to the charge balancing strategy in order maintain battery life time and ensure safe operation.

Recently, much research has been conducted into cascaded modular battery systems (CMBS) which consist of distributed converters connected in cascade. Each converter interfaces to a battery module as shown in Fig.4-15b. This type of structure has been used for interfacing different chemistries of second life batteries as proposed in [84, 85]. These configurations can implement the suggested PSB strategy, but the balance between each module's internal cells has not been provided and may require an additional balancing circuit. The modular battery system can be achieved at the cell level, i.e each converter interfaces to a battery cell instead of a battery module [86]. This can ensure charge balancing and with the possibility of implementing

PSB at cell level, but at a cost of system complexity as such a system will become very complex for systems with a large number of cells as each cell requires a separate converter with a control loop and dedicated measurements.

4.1.4 Proposed battery system

The proposed structure of the battery system is based on the utilization of the CMBS architecture with an optimized design for the number of modules (*M*) to maximize the utilization of battery capabilities and overall system efficiency and reliability at minimum size and complexity. The following subsections will investigate the effect of the selected number of modules on the overall converter weight, efficiency and fault tolerance as well as the usable capacity of the battery pack.

4.1.4.1 Effect of increased number of modules on usable capacity

This section describes the effect of an increased number of modules for a defined string voltage. The modularization of battery pack consists of a single string of *n* series-connected battery cells configured into *M* modules. The total usable capacity of the pack assuming that one of the modules has a weak cell, can be estimated from the rearranging of (4-2) as:

$$U_{cap} = \underbrace{Cap(cell_{weak}) + \frac{M-1}{M}\left((Cap(cell) - Cap(cell_{weak})\right)}_{\textbf{DUC}} + \underbrace{\left(\frac{\sum_{i=1}^{\frac{n}{M}-1} Cap(cell_i)}{\frac{n}{M}-1} - Cap(cell_{weak})\right)}_{\textbf{CRAC}} \quad (4\text{-}3)$$

where *Cap(cell)* is the capacity of healthy cells and $Cap(cell_{weak})$is the capacity of the weak cell. From (4-3), it can be observed that increasing the number of modules *M* for a given number of

cells *n* increases the DUC and reduces the CRAC. For example, if a string of 30-series connected battery cells to be considered, if one of the cells has a larger capacity fade of 10% compared to the rest of the cells, and if a CCBS (M=1) is considered, then the DUC is 90% and the CRAC is 10% of the usable capacity (Ucap). This means that, although the actual lost capacity represents only 0.3% of the overall capacity of the pack, the pack will lose 10% of its overall capacity unless a cell balancing is system implemented to enable the utilization of this 10% CRAC. On the other hand , for the CMBS as the number of modules *M* increases, the CRAC decreases until it reaches zero at the extreme case where each cell is interfaced by a separate converter (M=30) as in [86]. The effect of increasing *M* on both DUC and CRAC is shown in Fig. 4-16. Although the increasing number of modules reduces the CRAC which removes the need for balancing systems, it adds other penalties on system complexity, efficiency and weight which will be analysed in the following subsections in order to determine the optimal configuration.

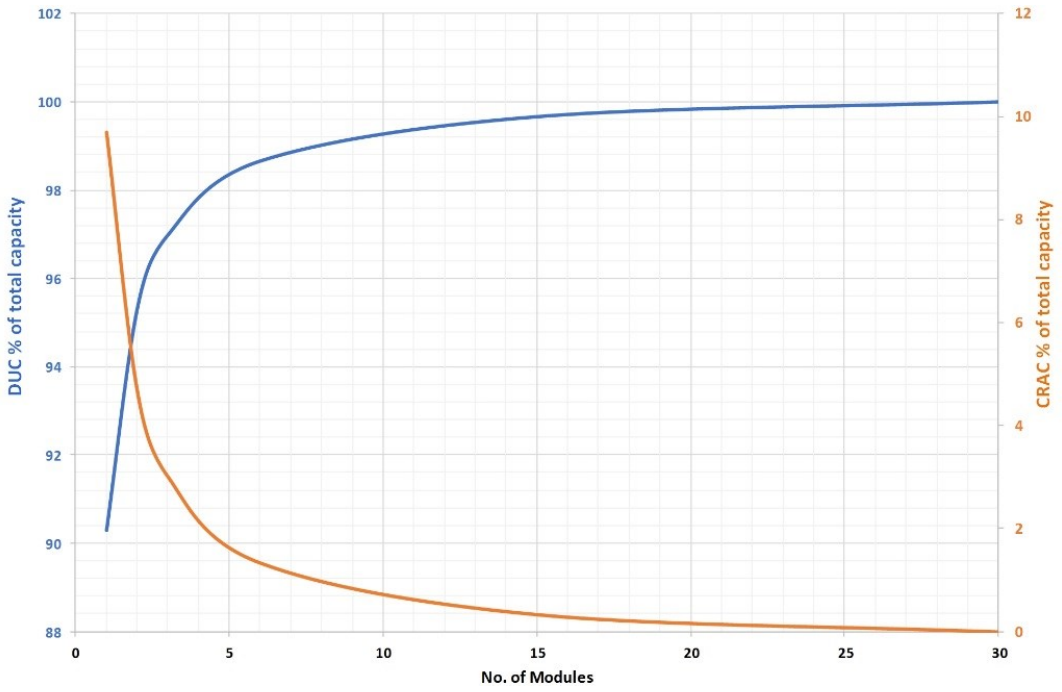


Fig. 4-16: Effect of increased M on the DUC and CRAC as a percentage of total capacity

4.1.4.2 Battery system design

The analysis will be performed on the CMBS based on a step-down converter topology (Fig. 4-17) as it is inherently fault tolerant as any module can be bypassed with no need for extra switches [87]. This can enable power share balancing among cells and ensure the thermal balancing between cells. This can be controlled by the system controller which monitors the voltages of the individual battery cells and observe the current state of charge and state of health. The efficiency of CMBS is defined by the efficiency of the converters which should be designed with high efficiency; however this topology will have a better efficiency compared CCBS as it eliminates the need for balancing circuits with its accompanied power loss during energy manipulations (in active balancing techniques) or energy dissipation (in passive balancing techniques) as described earlier.

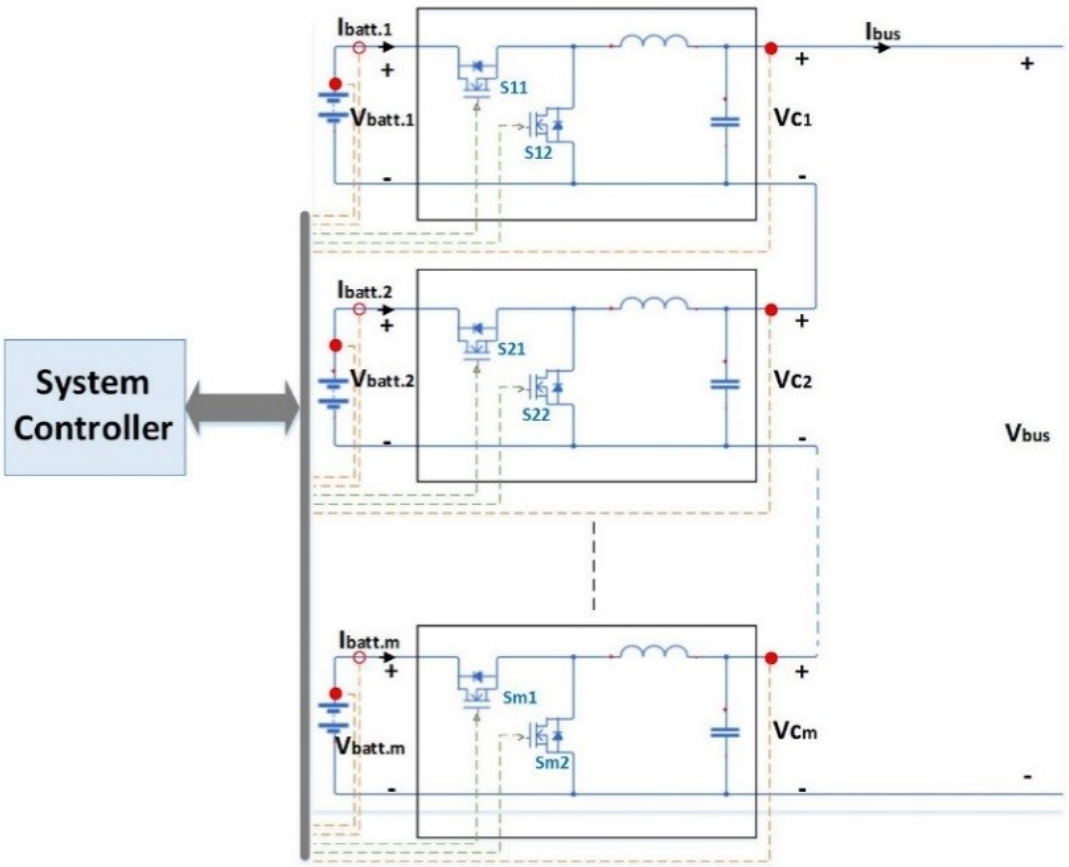


Fig. 4-17: Step-down topology based CMBS

4.1.4.2.1 Converter weight

Based on the selected buck-topology, the inductance of the inductor for each converter can be estimated as [88]:

$$L = \frac{n * V_{cell} * (1 - D) * D}{M * \Delta I * f_s} \tag{4-4}$$

where n is the overall number of battery cells (=30), V_{cell} is the voltage of the battery cell, D is the duty cycle of the converter top switch (S_{i1}), M is the number of modules. ΔI is the peak-to-peak current ripple of the inductor and f_s is the switching frequency. The maximum depth of discharge (DoD) of the battery for satellite EPS is in range of 30-35% which results in a 20% change in the cell voltage [39]. Accordingly, the battery voltage should be designed to have a voltage which is 20% larger than the main bus which results in a minimum duty cycle (D) of 80%. The values of the other design parameters are included in Table 4-1.

Table 4-1: Converter design parameters

Parameter	description	Value
V_{cell}	Battery cell voltage	3.6 – 4.2V
n	Total number of battery cells	30
ΔI	Inductor current ripple(p-p)	0.3A
f_s	Switching frequency	100kHz
D	Converter duty ratio	80-100 %
I_{bus}	Load current	1.5A
M	Number of modules	1-30

Based on standard inductor design rules, core sizing should satisfy the constraint of (4-5)[89]:

$$\frac{A_c{}^2 * W_A}{MLT} \geq \frac{\rho * L^2 * I^2{}_{\max}}{B^2{}_{\max} * R_{DC} * K_u} \tag{4-5}$$

where A_c is the core cross section area, W_A is the core winding area. MLT is mean length per turn, ρ is the resistivity of the winding wire, I_{max} is the maximum inductor current, B_{max} is the maximum flux density, R_{DC} is the winding resistance, K_u is the winding utilization factor and L is the inductance. The left hand side of (4-5) represents the core geometry, so a core geometrical

$$K_g = \frac{A_c{}^2 * W_A}{MLT} \tag{4-6}$$

constant K_g can be used to define the size of required core, which should satisfy:

For the CMBS, changing the number of modules does not affect the required current rating of the inductors, considering defined power requirement for charging/discharging of the battery. Considering the same core material, (4-5) and (4-6) can be rearranged as:

$$K_g = C_1 \frac{L^2}{R_{DC}} \tag{4-7}$$

where

$$C_1 = \frac{\rho * I^2{}_{\max}}{B^2{}_{\max} * K_u} \tag{4-8}$$

From (4-5) and (4-8) the CMBS inductor core size can be determined as:

$$K_g = C_1 \frac{L^2}{M^2 * \frac{R_{DC}}{f_1(M)}} \tag{4-9}$$

where $f_1(M)$ is a function that is assigned based on the required reduction in equivalent R_{DC} (per inductor) with increasing M in order to maintain the overall equivalent winding resistance for all inductors below a required specified value. As can be observed from (4-9), the reduction of the core size with increasing M is affected by $f_1(M)$, so a trade-off may be required between the achievable reduction in the core size with increasing M (to maintain the overall size at a minimum) and the achievable reduction in the equivalent R_{DC} with increasing M (to maintaining the overall winding resistance at a minimum). In the following investigation, the f_1(M) function is selected to be M in order to maintain an overall equivalent DC copper resistance of 8 mΩ.

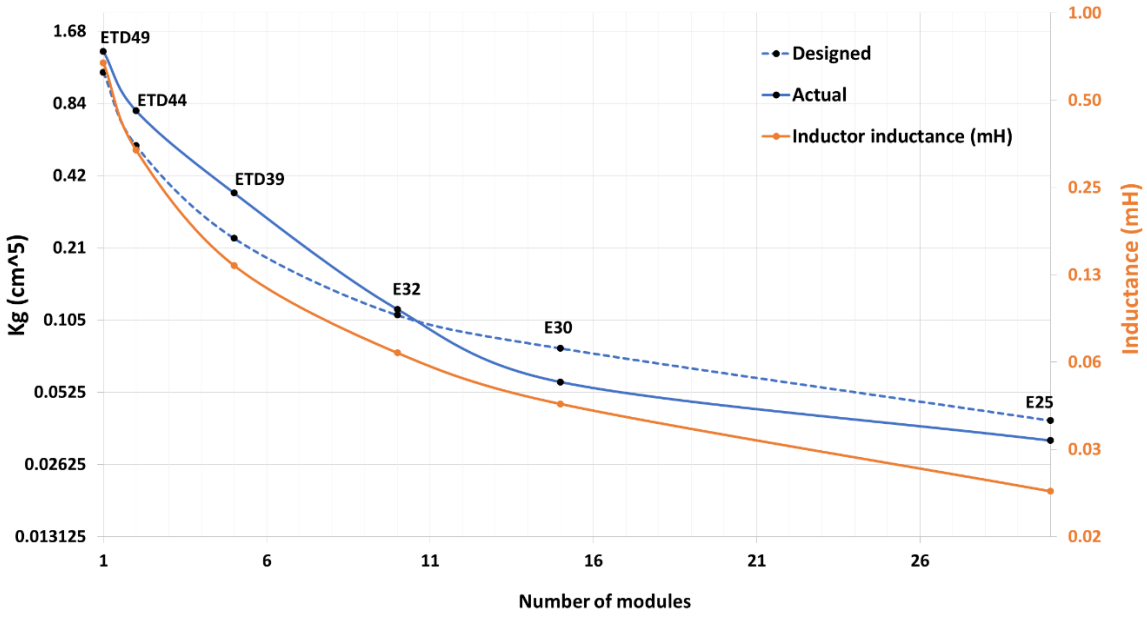


Fig. 4-18: inductance and core size of the inductors in CMBS

Fig. 4-18 shows the required inductance and designed core size as well as the actual corresponding core size and their part numbers based on TDK® core materials for each configuration. It can be observed that, for the designs with M=1,2,5, the commercially available cores are slightly larger than the estimated sizes which results in slightly larger core sizes but a lower estimated equivalent overall copper DC resistance than the designated value (8mΩ) as can be seen in Fig. 4-19. On the other hand, for the designs with M=15 and 30 the commercially available cores are slightly smaller than the estimated sizes which pushed the estimated equivalent copper DC resistance to be slightly higher than the designated value. Where the estimated core size has agreed with the commercially available core at the design with (M=10) and hence the estimated DC-R agreed with the designed value.

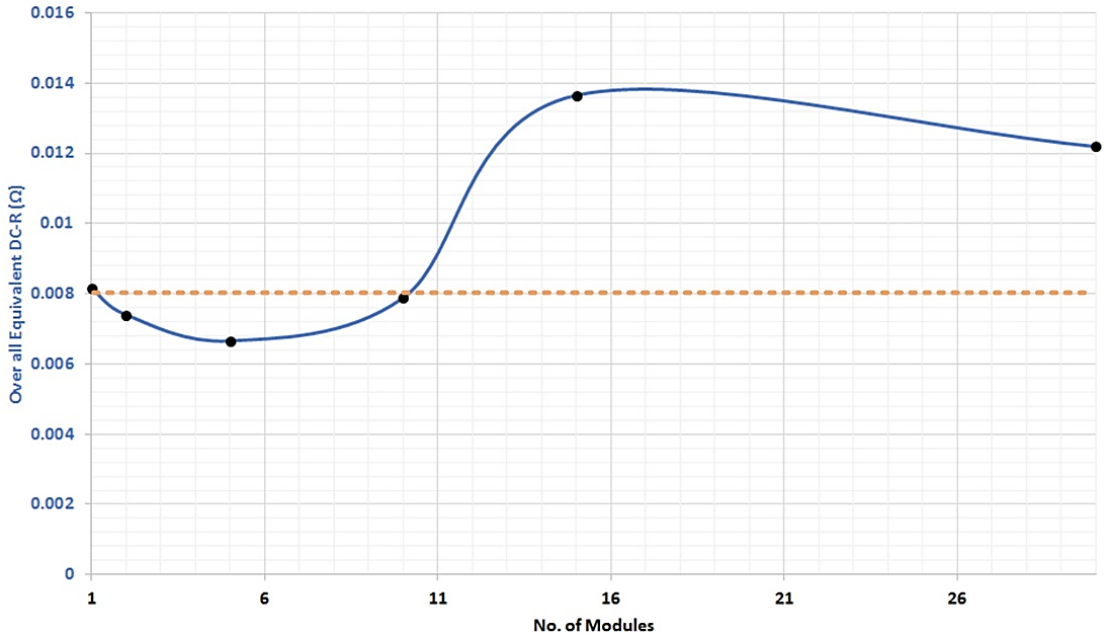


Fig. 4-19: Estimated equivalent overall copper DC resistance of CMBS inductors

In order determine the overall system weight, the inductor weight for different systems designs was estimated. The overall weight of the converters' inductors can be approximated by excluding the weight of the formers as:

$$W_{overall} = M\left(m_{core} + m_{copper}\right) \; ; \qquad m_{copper} = d * A_i * MLT * n_T \tag{4-10}$$

where m_{core} is the core weight, m_{copper} is the winding conductor weight, d is the density of the conductor material, A_i is the conductor cross section area, MLT is the mean length per turn and n_T is the number of turns. As can be observed from (4-10), the overall weight of all the inductors increases as M increases, however the reduction in the required inductance as M increases ramps down the increase of overall inductor weight as can be seen in Fig. 4-20. It can be seen that, for the single module design (M=1) the weight of the inductor was minimum (≈200g) as it required only a single converter with single inductor. However, for the two-module based design which required two converters with two inductors (but with reduced inductance compared to the single module design) this results in an overall weight of ≈300g. Similarly, for the modular design with M=10, the overall inductor weight is only five times bigger compared to the single module design. Table 4-2 show the inductor design parameters for the CMBS for different number of modules.

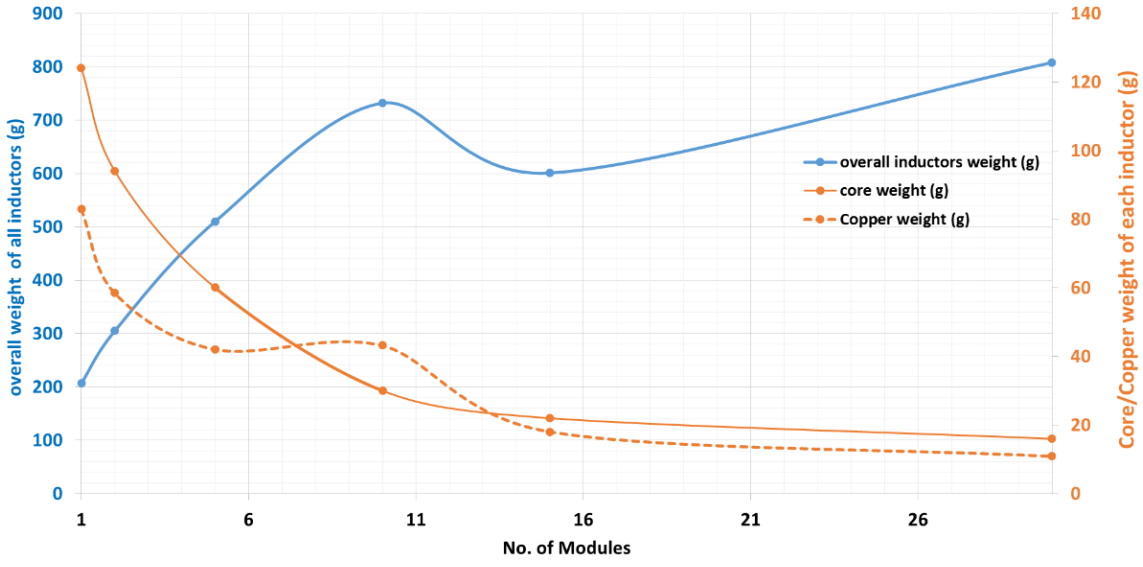


Fig. 4-20: core/copper weight of each inductor and overall inductor weight in the CMBS

Table 4-2: CMBS inductor design parameters for different No. of modules

No of Modules(M)	1	2	5	10	15	30
Inductance(mH)	0.59	0.30	0.12	0.06	0.04	0.02
(Kg (cm^5) (designed)	**1.13**	**0.56**	**0.23**	**0.11**	**0.08**	**0.04**
Types of Magnetic cores	**ETD49**	**ETD44**	**ETD39**	**E 32**	**E 30**	**E 25**
Kg *10e8 cm^5 (Actual)	1.38	0.78	0.35	0.12	0.06	0.03
Ac(cm^2)	2.10	1.70	1.20	0.83	0.60	0.52
Aw(cm^2)	2.69	2.10	1.70	1.08	0.90	0.61
MLT(cm)	8.60	7.77	6.90	6.40	5.60	5.00
Lm(cm)	11.40	10.30	9.22	5.70	5.70	5.75
G-window height(cm)	3.54	3.20	2.82	2.20	1.90	1.70
Core weight(g)	124	94	60	30	22	16
Material	**N27**	**N27**	**N27**	**N27**	**N27**	**N27**
Inductor design Calculations						
No of turns	25.84	15.96	9.04	6.54	6.03	3.48
Air gap length (cm)	0.03	0.02	0.01	0.01	0.01	0.00
Fringing factor (Kfr)	1.11	1.08	1.06	1.05	1.06	1.04
Number of turns (modified)	24.50	15.34	8.79	6.37	5.87	3.42
maximum wire diameter (mm)	2.37	2.64	3.14	3.88	2.80	3.02
Penetration depth (mm)	0.21	0.21	0.21	0.21	0.21	0.21
inductor DC resistance (DC-R) (mΩ)	8.16	3.70	1.33	0.79	0.91	0.41
inductor AC resistance (AC-R) (Ω)	1.04	0.59	0.30	0.27	0.16	0.08
Copper weight (g)	82.91	58.48	42.04	43.19	18.06	10.93
Overall weight of the single inductor (g)	206.91	152.48	102.04	73.19	40.06	26.93

4.1.4.2.2 Converter efficiency

As the overall system losses are mainly determined by the inductor and switch losses. Inductor power losses can be estimated as:

$$P_{inductor} = M\left(P_{core} + I_{bus}^2 R_{DC} + I_{AC-RMS}^2 R_{AC}\right) \quad (4\text{-}11)$$

where P_{core} is the inductor core losses, $I_{AC\text{-}RMS}$ is the RMS value of the inductor current ripple, R_{DC} is the winding DC resistance and R_{AC} is winding AC resistances which can be approximated as [89]:

$$R_{AC} = C_2 R_{DC} \tag{4-12}$$

where

$$C_2 = \frac{\pi r^2}{\pi r^2 - \pi(r - D_{pent})^2} \quad ; \quad D_{pent} = \sqrt{\frac{\rho}{\pi \mu f_s}} \tag{4-13}$$

where D_{Pent} is the penetration depth, to which the current exists at a particular frequency (due to skin effect), r is the conductor radius and μ is the conductor's permeability. The inductor core losses here are negligible as the core power losses of the ferrite core material used (N27) at the switching frequency of 100kHz and AC field flux density of 20mT is only 0.01W/cm^3. Accordingly the inductor losses will be considered as copper losses only.

The second part of the losses are the switch (MOSFET) losses which divide into the conduction and switching losses that can be estimated according to [90] as following:

$$P_{MOSFETs} = P_{cond} + P_{SW} \tag{4-14}$$

where P_{Cond} and P_{SW} are the conduction and switching losses of the MOSFETs and can be estimated as:

$$P_{cond} = M(I_{rms}^2 R_{DSon}) \tag{4-15}$$

where R_{DSon} is the drain-source ON-resistance of the MOSFET and I_{rms} is the RMS value of the switch current that can be estimated as [86]:

$$I_{rms} = \sqrt{I_{bus}^2 + \frac{\Delta I^2}{12}} \tag{4-16}$$

where ΔI is the peak-to-peak inductor current ripple.

The switching losses P_{SW} are dominated by the power losses caused by the overlap of current and voltage during the transition period and these can be estimated as:

$$P_{SW} = M\left(\frac{nV_{cell}I_{bus}}{2M}\right)(t_r + t_f)f_s \tag{4-17}$$

where t_r and t_f are the rise and fall times of the switching transition which depends on the device gate capacitances, gate voltages and current as described in detail in [91].

As can be observed from (4-15), the conduction losses are assumed to increase linearly as M increases; however increasing M reduces the required voltage rating of the MOSFET and accordingly, the corresponding devices are assumed to have a smaller R_{DSon} which reduces the rate of change of total conduction losses. Similarly, based on (4-17) the total switching losses decrease as M increases due to the reduction of the MOSFTE voltage rating and the reduction of gate charges as a result. The reduction of the R_{DSon} resistance and gate capacitance as the voltage rating of the device reduces are shown in Fig. 4-21 based on VISHAY® MOSFETs (with part number shown). The corresponding switches have been selected with a voltage rating 170-200% of the module voltage for each configuration for more reliability. For example, for the single module configuration (M=1) the module maximum voltage is assumed to be 120V, accordingly, the selected switch voltage rating is 200V.

MOSFET losses (conduction and switching) as well as inductor losses are shown in Fig. 4-22. The switch losses are estimated based on VISHAY® MOSFETs with part numbers indicated in Fig. 4-21 for each design point on the graph.

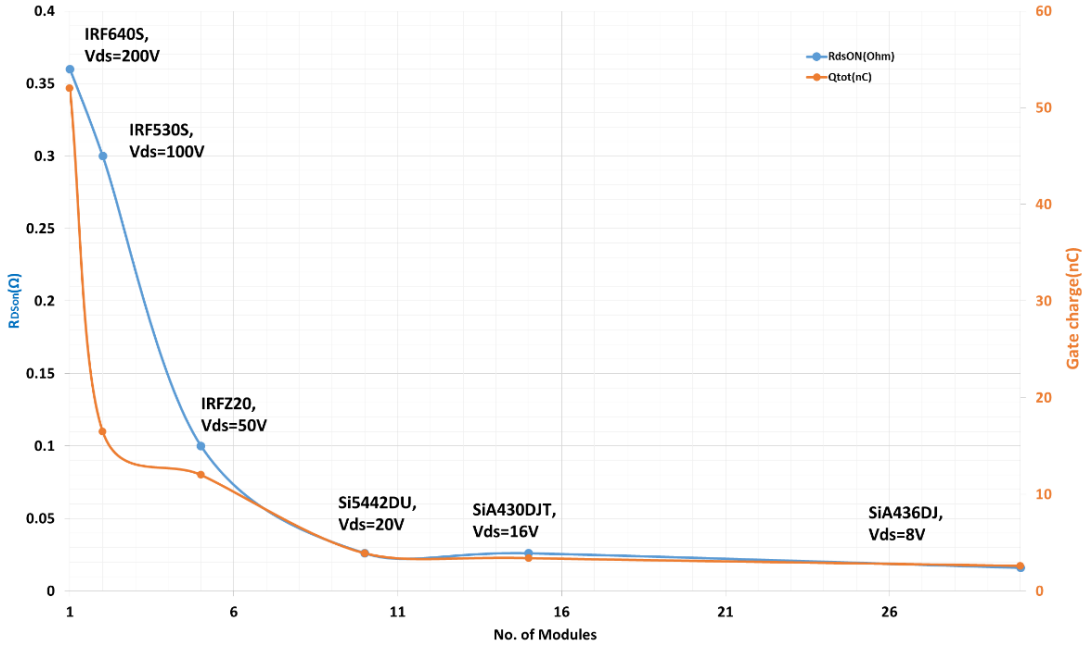


Fig. 4-21: R_{DSon} and gate charge for switches for different configuration of CMBS

As it can be seen, the overall power losses are dominated by the MOSFET losses as the inductors were designed to have very small copper losses from the beginning. For the CCBS design with M=1 the MOSFET power losses are dominated by the switching losses due to the larger gate charge of the switches which are rated at 200V. On the other hand, the modular design with M=2 enables the selection of lower voltage switches (100V) with lower (R_{DSon} and gate charge). The selected device for this rating is optimized in terms of gate charge rather than R_{DSon} which caused a significant reduction in the switching losses rather than the conduction losses. As M increases the devices parameters improves, allowing better overall system efficiency up to M=15 before it slightly decrease again at M=30 as can be seen in Fig. 4-23. This because the reduction factor for device R_{DSon} is slightly lower than M causing increased conduction losses according to (4-15).

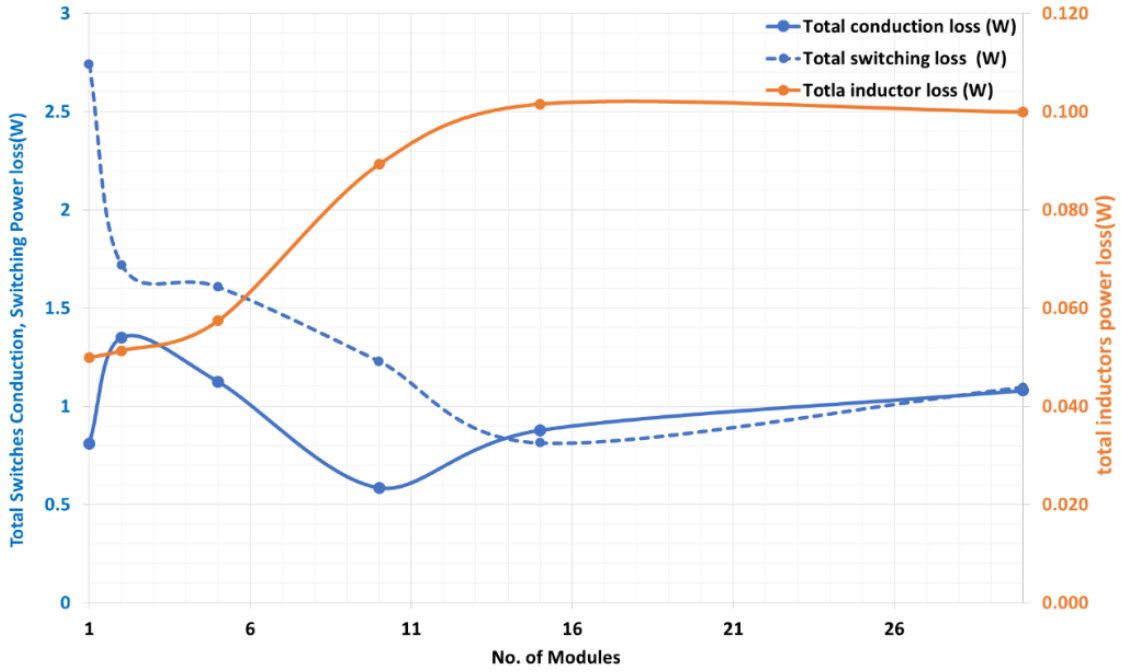


Fig. 4-22: Power losses at different configuration of the CMBS

As can be observed, the overall converter efficiency maintained high (97.6% - 98.8%) even with increased number modules but at the cost of increased overall weight of inductors designed to maintain overall copper losses very small.

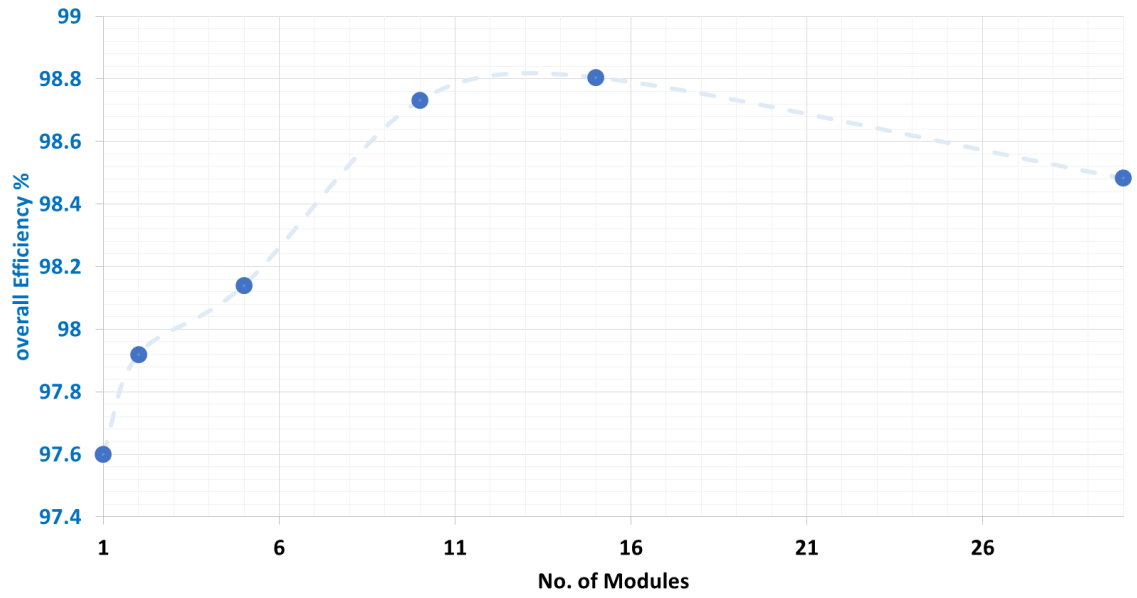


Fig. 4-23: Overall converter efficiency for different configuration of the CMBS

4.1.4.2.3 Fault tolerant operation

The performance of the battery system during a fault is very important as it affects the overall performance of the power system. In order to analyse the performance of the CMBS under different faults scenarios, it is important to consider how the fault affects the output voltage as well as the available usable capacity of the battery pack under this fault. The minimum achievable output voltage for a fault occurring in one or more battery modules due to battery cell failure or converter failure of these modules can be estimated as:

$$V_{O_{min}} = (M - x)\frac{n}{M}V_{cell_{min}} \quad where\ x < M \tag{4-18}$$

where x is the number of faulty modules and $V_{cell_{min}}$ is the minimum voltage of the battery cell at the maximum depth of discharge (DoD). The available usable capacity can be estimated as:

$$E_{cap_{min}} = (M - x)\frac{E_{cap}}{M} - E_{untlz}(V_{cell_{min}}) \tag{4-19}$$

where E_{cap} is the total energy capacity of the pack (Wh) and E_{untlz} is the unutilized energy capacity of the battery when setting $V_{cell_{min}}$ to a specific value to maintain the target value for the output voltage.

As can be observed from (4-18) and (4-19), increasing the minimum cell voltage $V_{cell_{min}}$ for which the discharging of the battery should be stopped (which affects both the output voltage and the available energy capacity E_{cap}), will increase the minimum output voltage but will also increase the unutilized energy capacity (E_{untlz}) which will therefore decrease the available usable energy capacity of the battery pack ($E_{cap_{min}}$) as a result. An analysis has been made of minimum output voltage and available energy capacity for different fault conditions and is shown in Fig. 4-24. The analysis has been made for $V_{cell_{min}}$=3.4V to allow a maximum DoD to

compensate for the lost capacity in the faulty modules. It can be seen that, for CCBS (M=1) at a failure in one of the battery cells or converter switches, the complete battery system become unusable and the output voltage collapses. On the other hand, for the CMBS, as M increases the ability of the system to compensate for a faulty module increases. Although, the designs with a lower number of modules (M<5) cannot maintain the output voltage at an acceptable level even with a single module failure, the designs with a higher number of modules (M>10) could maintain the output voltage above 80% of its designated voltage even with failure of two modules.

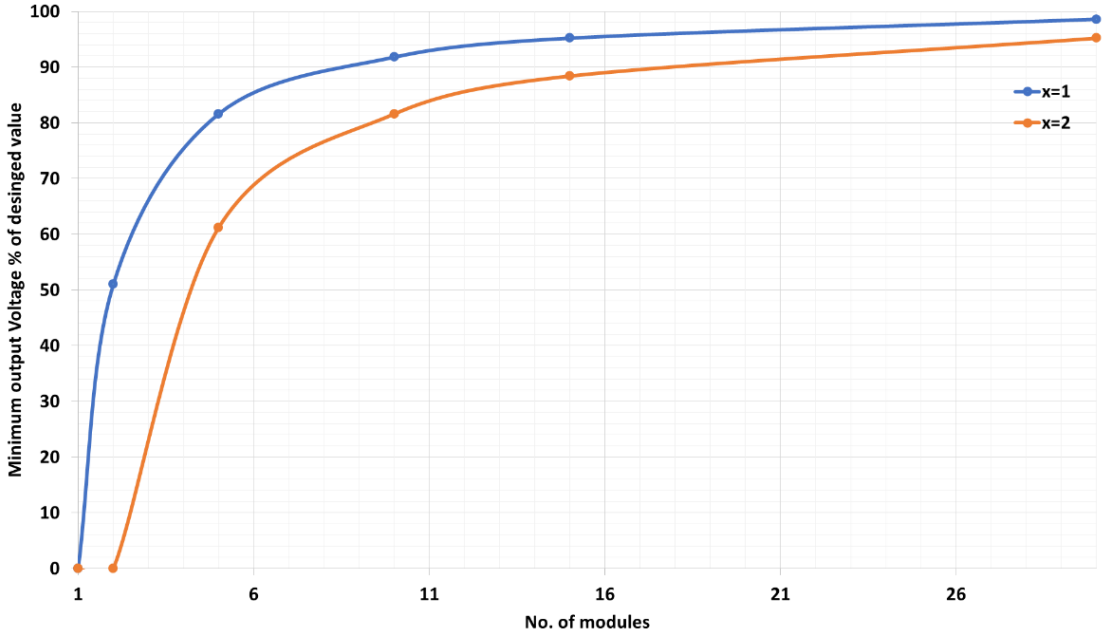


Fig. 4-24: Minimum achievable output voltage under partial faults at different designs of CMBS

4.1.4.2.4 CMBS system multi-objective analysis

As can be observed from the previous subsections, the different parameters of the system are affected differently with increased number of modules (M), so a multi-objective analysis is required in order to define the best configuration based on these parameters. A system analysis has been made based on the combined parameters that have been investigated in the previous subsections. These include the direct usable capacity (DUC) of the battery pack, the overall converter efficiency, weight, fault tolerance by the ability of maintaining the output voltage within its acceptable range under faults conditions as well as system simplicity (defined as the number of control loops required and the measurements required for different configurations).

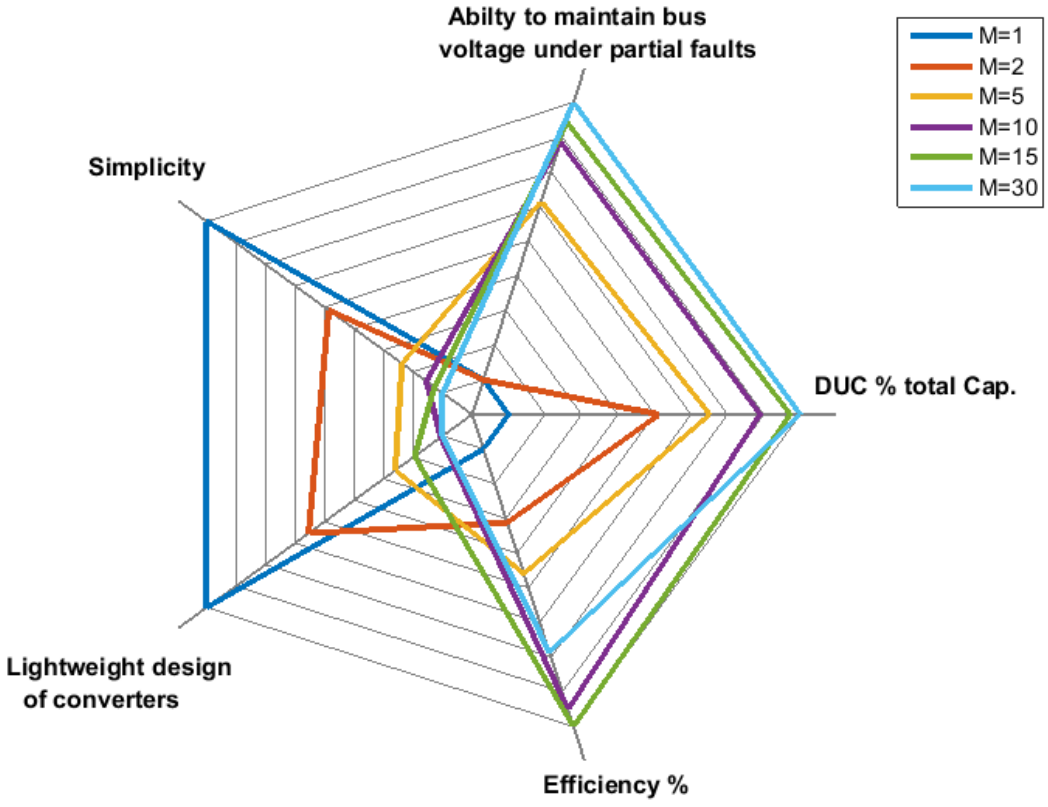


Fig. 4-25: CMBS multi-objective analysis

It can be seen in Fig. 4-25 that the CCBS (M=1) is the best option in terms of weight (inductor weight is only 207g) and simplicity, as it requires a single control loop with its dedicated measurements. However, the DUC of the battery pack under this configuration, for 10% more capacity fade in one of the cells compared to others, is 90% which may require additional balancing circuits with added weight to enable the full utilization of the available capacity. Also, this configuration showed lower efficacy (97.6%) as can be seen in Fig. 4-23 due to the higher voltage rating required for the switching devices. This centralized design also cannot provide fault tolerant operation. On the other hand, for the design configuration with the highest number of modules (M=30), although it could be consider the best in terms of DUC (100%) and fault tolerance, it has the heaviest inductor weight (4-times more than the CCBS design), and it would be extremely complex due to the large number of control loops and dedicated measurements. As can be observed from Fig. 4-25, the design configuration with M=5 and M=10 can be consider as the better solutions as they provide a reasonable DUC (97%-98.5%) and efficiency (98%). However, the design configuration with M=5 has lower inductor weight (510g) compared to (790g) for the design configuration with M=10 and also the number of control loops and their dedicated measurements are doubled compared to the design configuration with M=5. The design configuration with M=10 is better in terms of fault tolerance as it can maintain the output voltage above 80% of its designated value with faults in two modules, whereas the design configuration with M=5 could achieve only 60%. Accordingly, a trade-off between the system complexity and fault tolerance is required in order to select the best design configuration from the two design options (M=5 and M=10). With the boost converter topology (inductor in the battery side), the design configuration with M=5 can easily maintain the output voltage above 80% which enhance its fault tolerance and boosts its advantages over the design with M=10, promoting it as the best solution. However, the boost converter topology limits the ability of the CMBS in terms of controlling the power share of battery modules as described in details in [87]. A buck-boost converter topology can be

considered as an improved solution as it will enable the extension of the fault tolerance range for the CMBS by maintain the output voltage within acceptable limits without limiting the power share controllability of the battery module which the boost converter does. Accordingly, the best configuration of the CMBS is achieved by implementing a buck-boost converter topology for interfacing the battery modules in the design configuration with M=5.

4.2 Issues with PV strings

The second concern for constructing satellite EPS with higher bus voltages is that the PV arrays are required to be constructed based on a number of parallel strings, each string with a high number of series connected PV cells, in order to form the array required voltage and power. The performance of PV cells within the string may not be identical, this due to the different possible degradation mechanisms that happen due to the space environment which might differently affect the performance of each PV cell within the string. The power generated from these types of PV arrays is strongly affected by the performance of the weakest PV cells within the string as will be discussed in the following subsections.

4.2.1 Effects of space environment on PV cells

The on-orbit environmental factors have a great effect on the degradation of the PV cells. The presence of charged particles (electrons and protons) caused by solar radiation is one of those factors. The accumulated charged particles over the mission life of the satellites can seriously degrade the electrical characteristics of PV cells [18, 92-94]. The degradation of the current-voltage characteristics of the PV cell, as a function of increasing fluence (energy released by the accumulated number of charged particles impinging upon a unit surface array over some time duration in orbit in million electron volt (MeV)) for S32 PV cell compared to its beginning of

life (BOL) characteristics are shown in Fig. 4-26, based on the specified values form the manufacturer [55]. As can be seen, space radiation has a strong effect on the degradation of the I-V characteristics of PV cells depending on the cell's characteristics (which may not be identical due to manufacturing tolerance) and the radiation dose (fluence) which is a function of orbital parameters. The effects of the space radiation on the PV cell can be eliminated by using of a cover glass of a suitable structure over the PV cells which can provide a degree of protection against space radiation based on the density and thickness of the material [59], but with a cost of added weight to the PV array.

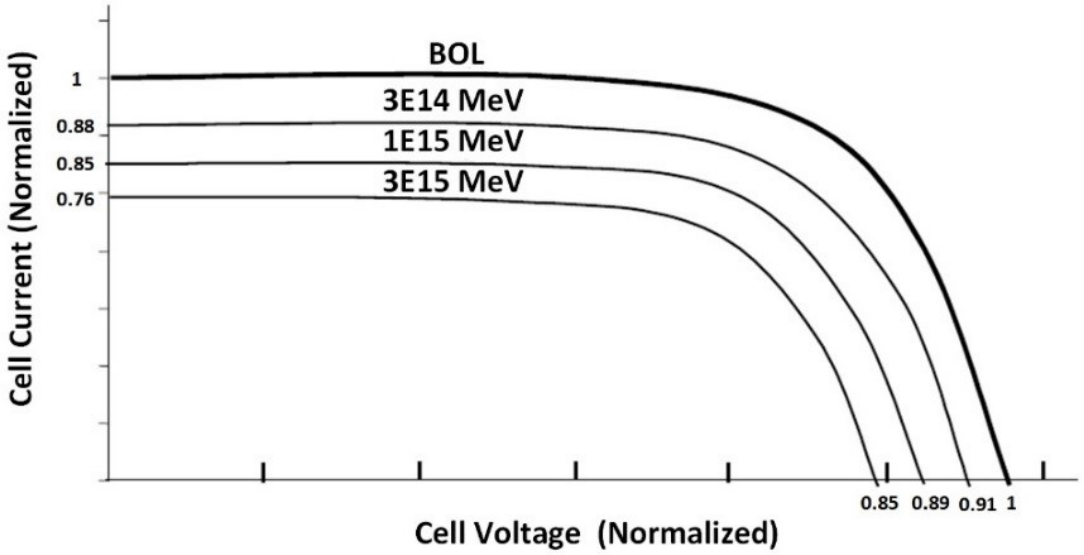


Fig. 4-26: Degradation in I–V characteristics of S32 PV cell under radiation.

The second factor associated with the space environment that significantly affects the characteristic of the PV cells causing degradation is micro meteoroids and space debris. The impact of these solid objects can cause damage to PV arrays, where the small particles that are not large enough to cause immediate damage can cause gradual degradation in output power over time [18, 95]. The effect of micro meteoroids and space debris can be optical damage to the cover glass in the form of micro-cracks, scratches and crater; and this partially affects the absorbance of incident light in the affected area. The other form of PV cell damage due to micro

meteoroids and space debris is the physical damage due to the disturbance of the impurity structure within the cell caused by the shock-wave during the collision of these high speed particles with the PV cells. The effects of meteoroids and space debris on PV cells are shown in Fig. 4-27 based on test results obtained for a PV array panel returned from the ''MIR'' space station [95-97].

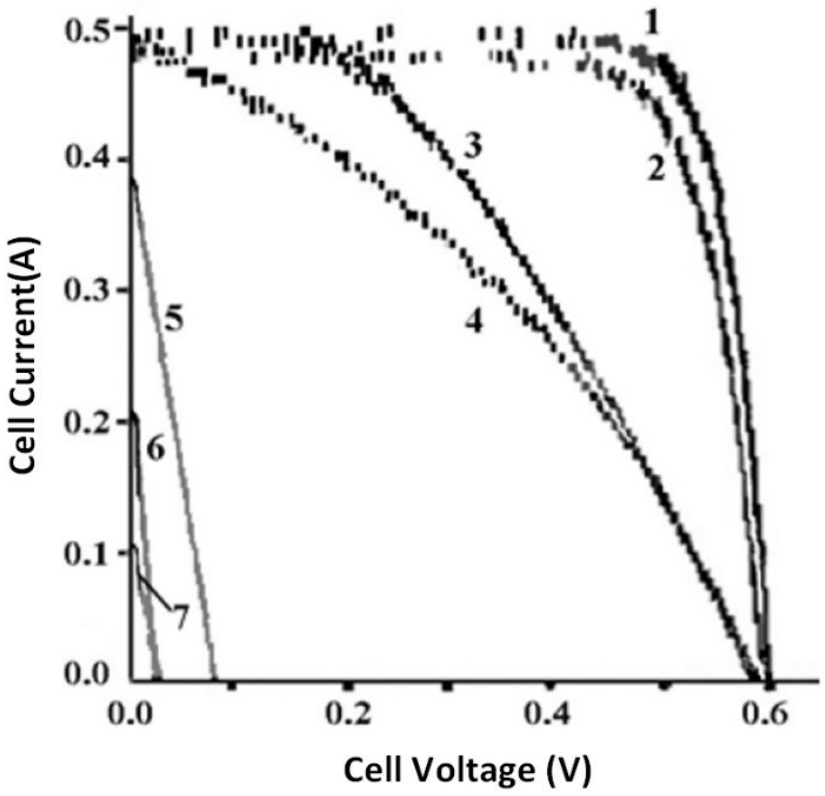


Fig. 4-27: I-V characteristic of the PV cells from a returned PV panel from ''MIR'' space station: 1,2 standard I-V characteristics; 3,4,5,6,7 – anomalous I-V characteristics [95]

As can be seen, different cells have been degraded in a different manner due to the accidental damage that might be introduced to each cell or portion of a cell at different boundary conditions, which cause the PV cells to perform differently within the same string under the

same irradiance and temperature conditions. This affects the overall performance of the PV array as will be demonstrated in the following subsection.

The third factor associated with the space environment is the space plasma under which arcing can be triggered between the coverglass and two adjacent cells where a reasonable voltage gradient exists, causing current coupling directly between cells [18]. The cell-to-cell coupling is driven by current and voltage produced by the PV array string, and can become a sustained arc which might cause permanent damage for the string or power cables if sufficient string voltage/current is available. This was the failure scenario reported for some missions [14, 15]. Increasing the voltage of the PV strings increases the risks of sustained arcs even with only small possible currents from PV strings [12, 13] as can be seen in Fig. 4-28. The possibility of a sustained arc in PV strings with a voltage below 50V is very small even with high possible currents in the string. As the voltage increases the possibly of sustained arcing is exists even for a small currents (1A-1.5A).

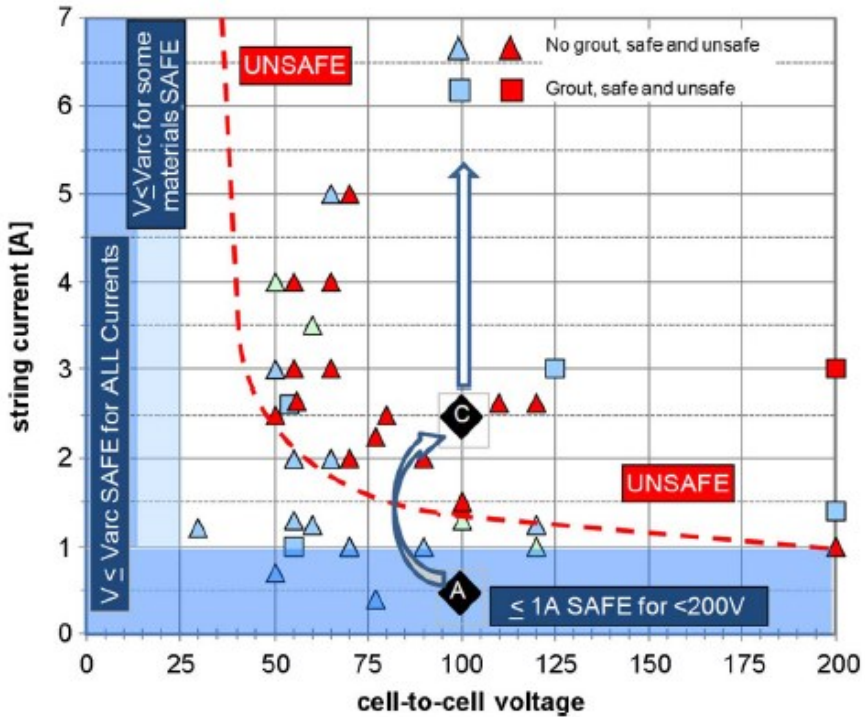


Fig. 4-28: Safe operating voltage and current criteria for satellite PV strings [12]

Therefore, PV strings with higher voltages (Above 50V) were not preferred in low power satellite due to the high risk of sustained arcing. Alternatively, lower bus voltage (28V) with lower voltage PV string (35V) is typically implemented. However, the power requirements for new small satellites mission are increasing and pushing towards the implementation of a higher voltage bus in order to minimize the weight of cables and harnesses. Improved designs for the PV array and its MPPT are required in order to enable the implementation of higher bus voltages and mitigate the risks of sustained arcing as well as providing a fault tolerance for the operation of the power system with the degradation and partial failure that might be introduced to the PV cells during on-orbit lifetime due to the space environmental factors discussed.

4.2.2 Conventional designs of PV arrays and regulators

The usual designs for the PV array in satellites EPS is based on a number of panels/wings depending on satellite structure, with each panel/wing constructed based on a number of parallel PV strings to achieve the required current/power. Each string is constructed based on a number of series connected PV cells to achieve the required panel voltage [18, 59, 98], and each PV cell is equipped with a bypass diode for cell protection or to bypass damaged cells. Each string is also equipped with a blocking diode to prevent current flowing back to the strings as can be seen in Fig. 4-29. This approach requires a large number of series connected PV cells especially for these missions which require a higher bus voltage. PV-panels are usually interfaced to the power bus through power regulators (PR), such that each panel interfaces the power bus by its own PR, which control the extracted power from the PV panel according to the power requirement for the load and battery charging in order to regulate the bus voltage.

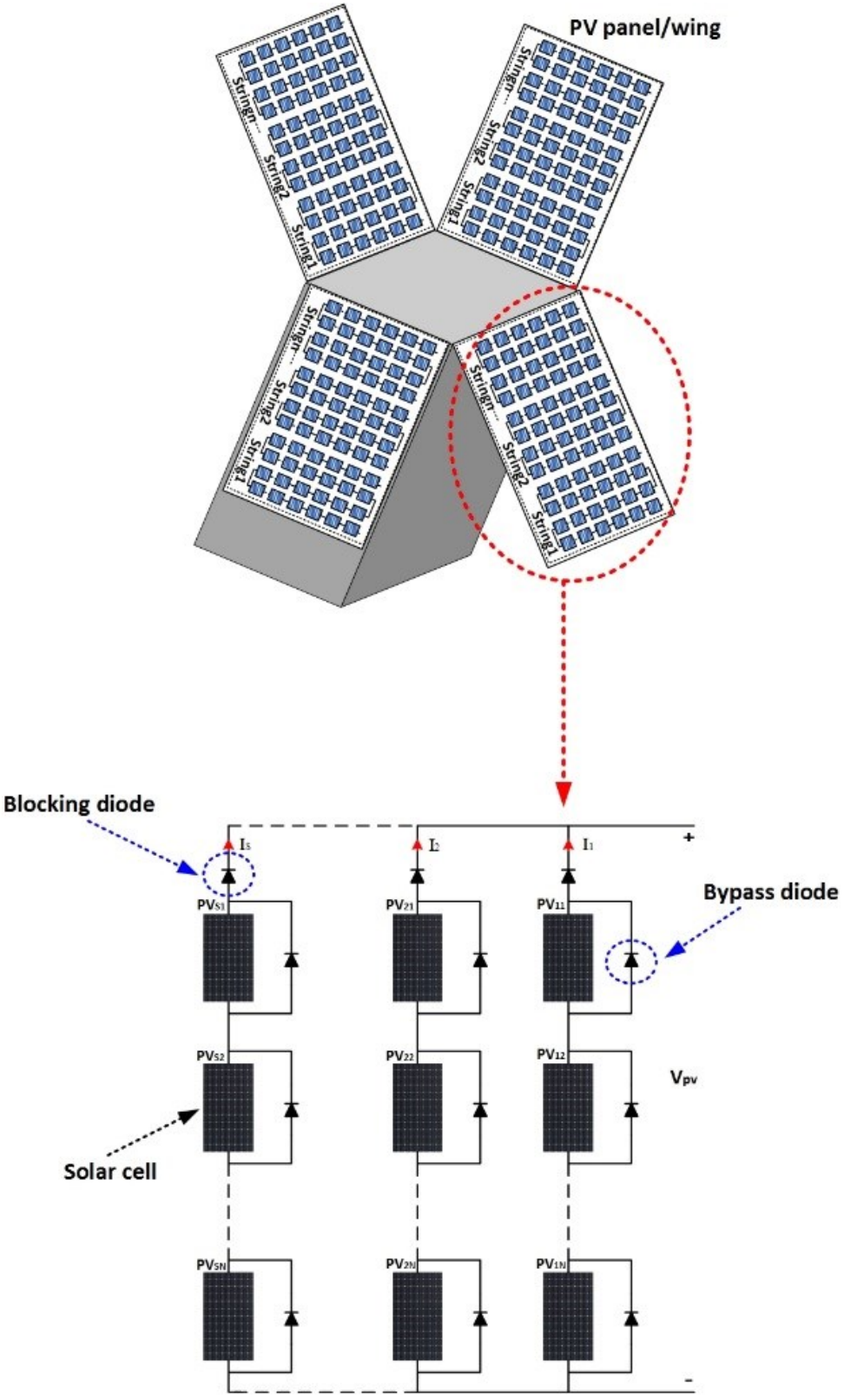


Fig. 4-29: Construction of a satellite PV-panel/wing

The EPS to be consider is based on the MPPT architecture (described in Chapter2) in which the PRs are designed as series converter rated at the full voltage/power of the PV-panel for controlling its operating point based on the power requirement.

In order to investigate the performance of the PV array with different designs for PR, a single PV-panel with its associated PR will be considered for the analysis. The PV panel consists of ''*S*'' strings connected in parallel, each string consists of ''*N*'' series connected PV cells as shown in Fig. 4-30.

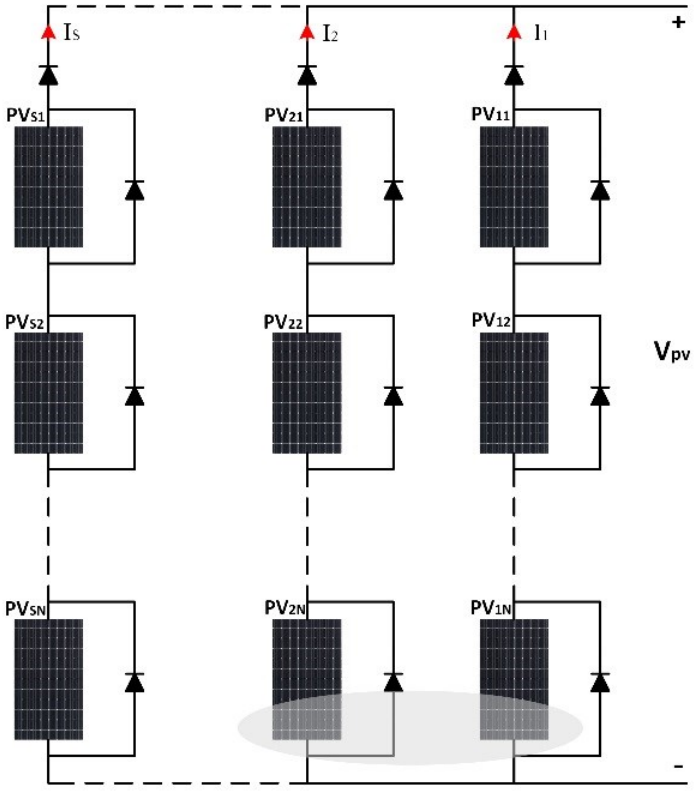


Fig. 4-30: PV panel configuration

For a uniform irradiance on all the PV cells and with them operating at the same temperature, the overall maximum available power from the PV-panel can be estimated as:

$$P_{PV_{max}} = SNI_mV_m \tag{4-20}$$

where I_m and V_m are PV cell's current and voltage at maximum power point (MPP). Assuming the number of strings ''*Y* '' which have *''X''* PV cells that have lower power generation compared to the other cells due to for example partial shading caused by the satellite structure in some positions/orientations, or due to more degradation introduced to those specific cells caused by environmental factors as described previously, the maximum available power from the PV-panel for a uniform irradiance can be redefined as:

$$P_{PV_{max}} = (S - Y)NI_{m1}V_{m1} + Y((N - X)I_{m1}V_{m1} + XI_{m2}V_{m2}) \quad (4\text{-}21)$$

where I_{m1} and V_{m1} are the current and voltage at MPP for the normal PV cells, and I_{m2} and V_{m2} are the current and voltage at MPP for the impaired PV cells. Based on the characteristics of the PV cells and the nature of the degradation, the operating points of the degraded cells will be different compared to the normal cells as seen in Fig. 4-31. The PR has two options to handle the power from the PV panel. The first option is to force the normal PV cells within the partially affected strings to operate at point *A* of the PV-characteristic curve which is the MPP of these specific cells. As a result, the current within these specific strings would be *Im1* which results in a reduction in the operating voltage of the weak cells with the possibility of turning on the dedicated bypass diodes reducing string voltage. Un-affected strings parallel to these affected strings will tend to operate at a lower voltage which results in the operating point of its cells being pushed to point B. The extracted power under this condition can be estimated as:

$$P_{PV} = (S - Y)NI_1V_1 + Y(N - X)I_{m1}V_{m1} \quad (4\text{-}22)$$

where I_1 and V_1 are the current and voltage of the PV cell at the operating point B, where V_1 is estimated as:

$$V_1 = \left(1 - \frac{X}{N}\right) V_{m1} \tag{4-23}$$

The second option for the PR is to force the affected strings to work at the MPP of the weak cells by decreasing the current of these strings to be I_{m2}. As a result, the voltage of the un-affected strings would be increased to V_3 which in turn pushes the unaffected strings to operate at point *C* away from MPP. The extracted power under this condition can be estimated as:

$$P_{PV} = (S - Y)NI_2V_2 + Y((N - X)I_{m2}V_3 + XI_{m2}V_{m2}) \tag{4-24}$$

where I_2 and V_2 are the current and voltage of the PV cell at the operating point *C* within the unaffected strings, where V_2 is estimated as:

$$V_2 = XV_{m1} + (N - X)V_3 \tag{4-25}$$

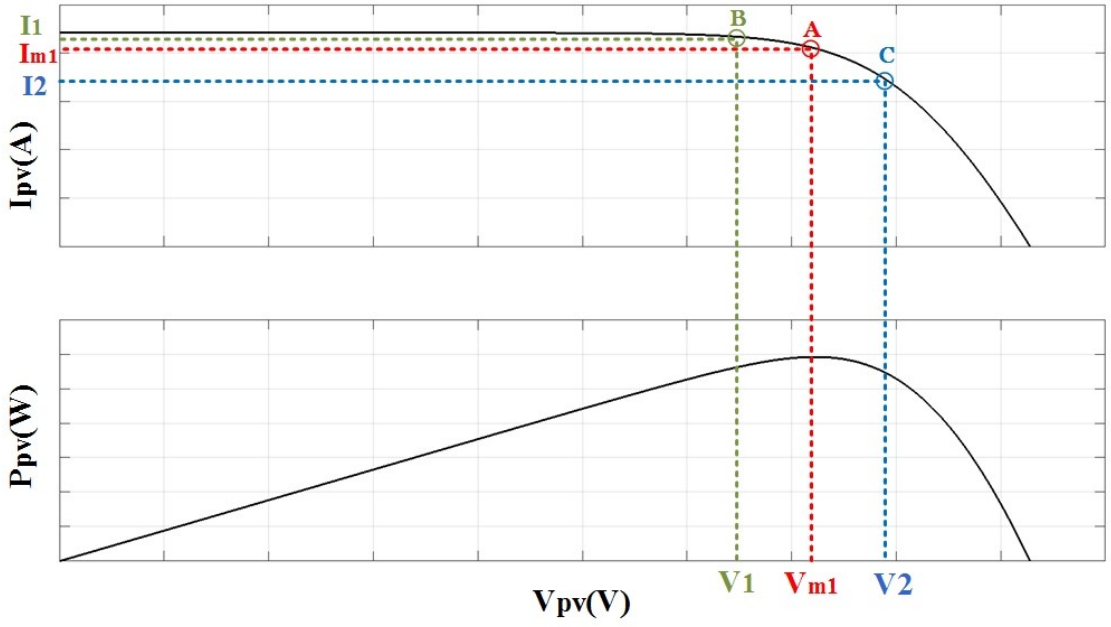


Fig. 4-31: V-I and V-P characteristic curve of a PV-panel

Fig. 4-32 shows the PV-panel power lost (unextracted power) as a percentage of total available power for partially degraded strings that have a number of weaker cells (assumed to be 50% lower performance compared to a normal cell) within the panel. The total available power is estimated based on (4-21) considering a PV-panel constructed of 4-parallel strings. Each string has 40-series connected PV cells. The PV cell considered is a triple junction PV cell (3G30C) specified in [16]. As can be seen, option1 has lower unextracted power for s lower number of weaker cells within the affected strings even with a higher number of affected strings. However, if there is a high number of weaker cells, this option will result in a large reduction of string voltage causing a large unextracted power by pushing the unaffected cells to operate away from MPP. However, option2 can operate better under this condition by maintain the string voltage allowing the unaffected strings to work at their MPP and minimizing the unextracted power.

In fact, the implemented MPPT in the PR should be able to operate the interfaced PV-panel at maximum power extraction by selecting the best option for each situation, and this selection is made passively during the process of searching for the MPP. Fig. 4-33 shows the minimum unextracted power from the PV-panel which can be achieve by implementing the best option for each operating condition. However, in a real PV-panel the degraded cells within the affected strings will cause the characteristic power curve of the panel to have a number of local maxima (local MPP) depending on the degradation and number of affected cells and strings. This local maxima can results in additional power loss in the form of unextracted power if the MPPT stay at one of these local maxima rather than the global MPP.

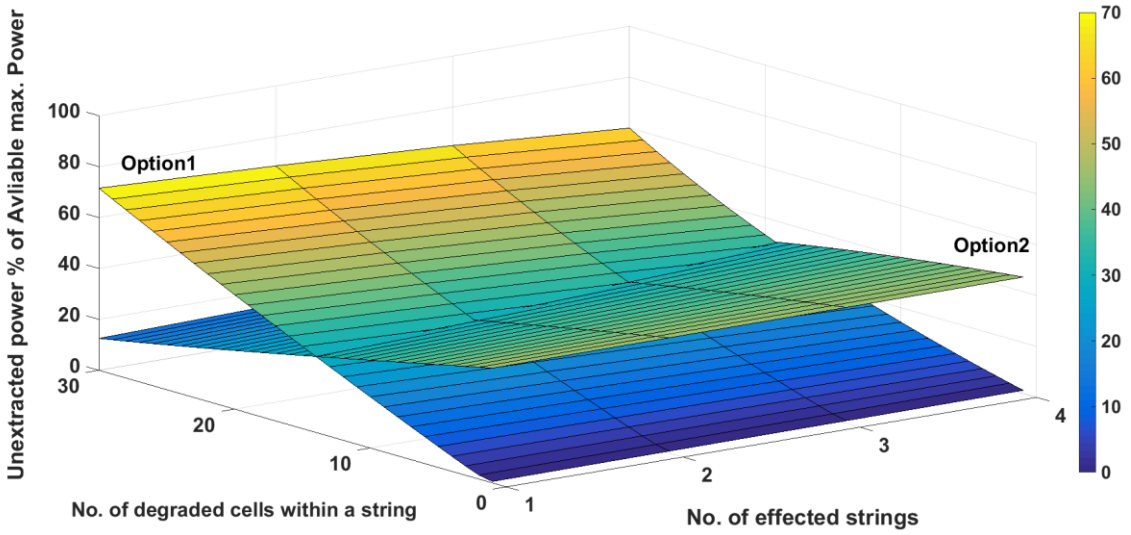


Fig. 4-32: Unextracted power from a partially degraded PV-panel for the two regulation options

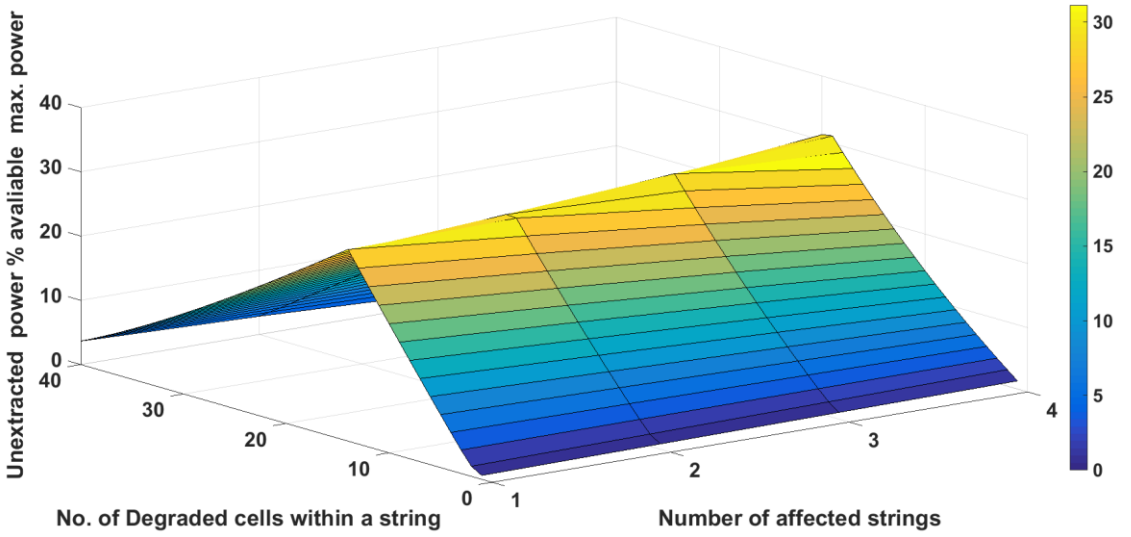


Fig. 4-33: Minimum unextracted power from a partially degraded PV-panel for the two regulation options

Fig. 4-34 shows the simulated performance of the PV-panel with the previously described structure for 50% degradation in the performance of 10 PV cells (out of 40) in a single string (out of 4). It can be seen that the MPPT can easily stay at the local maxima causing a loss of ≈ 15-20% of the available power in addition to the lost power due to the effect of the degraded

cells on the array's performance. In order to overcome the problem of power loss due to local maxima, a complex MPPT algorithm that is able to find and track the global MPP is required [99-101] which contributes to system's complexity.

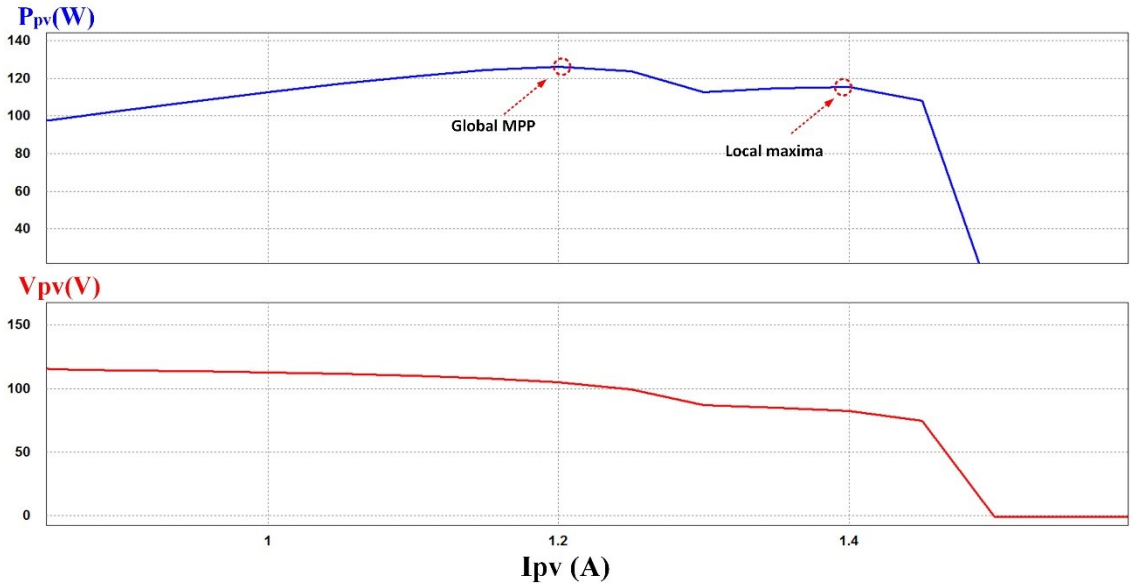


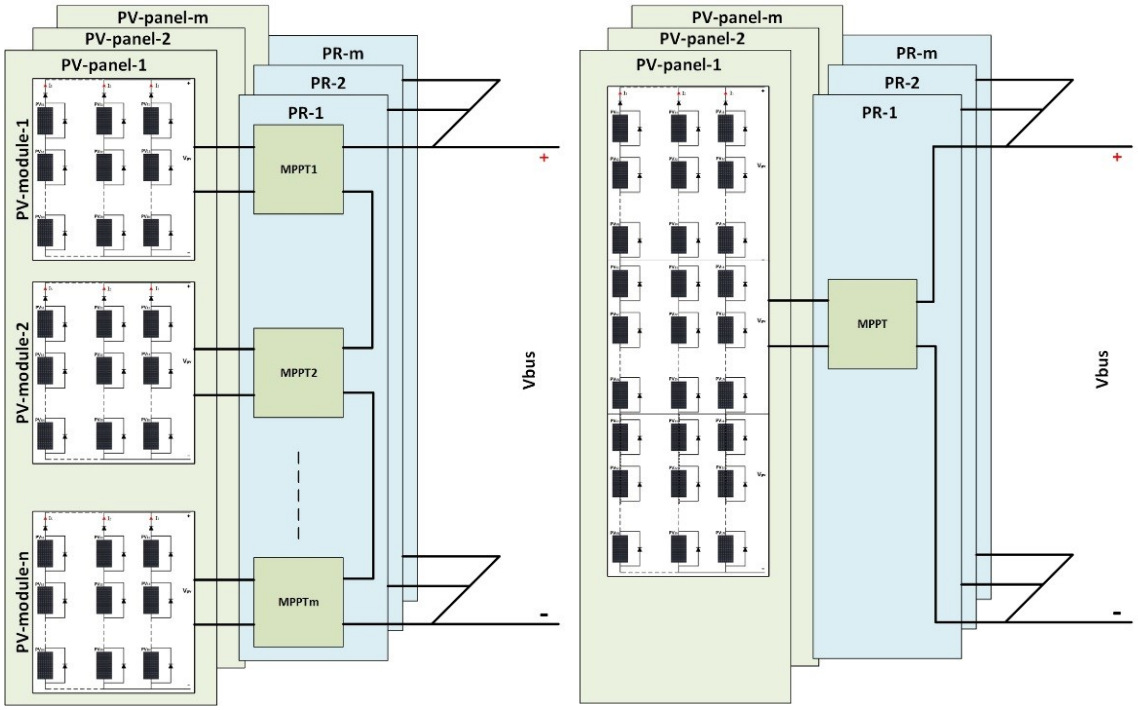
Fig. 4-34: Simulated performance of a PV-panel with partially degraded cells

4.2.3 Proposed designs for PV panels and power regulators

The conventional centralized (per panel) PR causes a power waste in the form of unextracted power, caused by the effect of weak PV cells on the overall performance of the panel. In addition to the problem of wasted power, the centralized architecture of the PV-panel and the PR increases the complexity of the bypass system required to allow fault tolerant operation of the power system. Additionally, the centralized design of the PV-panel with higher voltage bus EPS increases the risk of sustained arcing in the PV-strings especially under cold conditions (when the satellite just returns from eclipse) where the string voltage increases significantly.

The implementation of a cascaded modular system (CMS) design for the PV-panel and its interfacing PR (Fig. 4-35 a), similar to the proposed CMBS that was introduced earlier in this

chapter for the battery, could be considered as a promising solution for most of the problems in a conventional centralized architecture (Fig. 4-35 b). The concept of the CMS has been investigated for interfacing PV-panels in terrestrial applications in order to overcome the problems related to partial shadings improving the extracted power from the panels [102-104].



(a) (b)

Fig. 4-35: PV-panels and interfacing PRs in: (a) CMS architecture, (b) Centralized architecture

The implementation of the CMS with the proper selection of the number of cascaded modules, similar to what has been investigated for the proposed CMBS, can bring many advantages for satellite EPS. Such as reducing string voltages (to minimises the risk of sustained arcs), and also reduces the voltage rating of the switches (to improves overall efficiency). Additionally, the modular structure enables inherent fault tolerant operation as well as design flexibility and expandability.

Summary

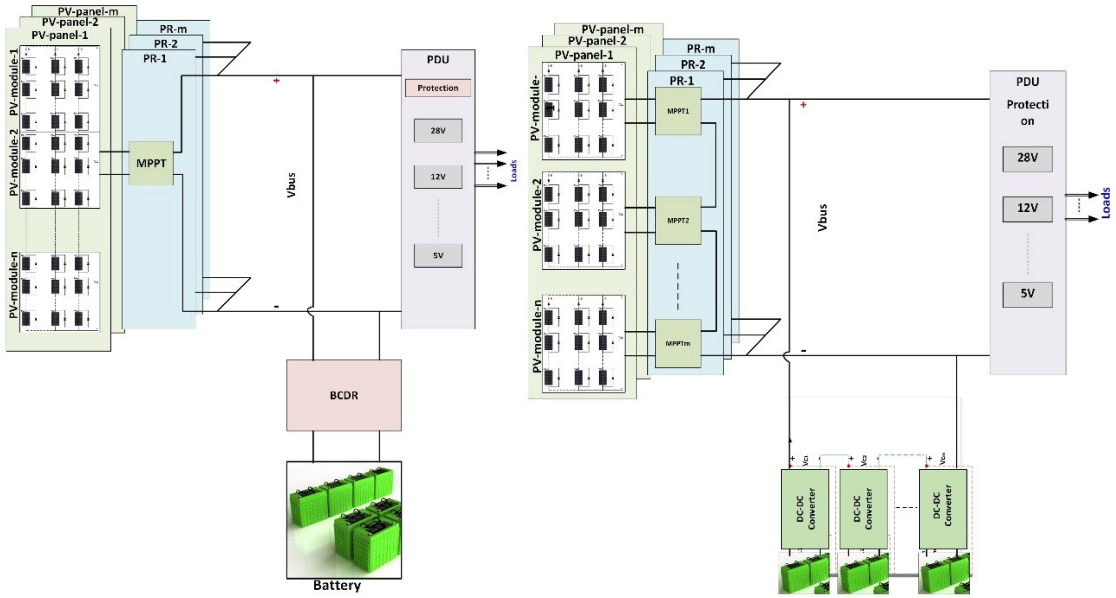
In this chapter, the issues with PVs and battery strings have been investigated. The problems associated with battery strings were mainly found with the capacity imbalances between battery cells within the strings which is caused by manufacturing tolerance or asymmetrical degradation. The imbalances limit the overall performance of the battery pack in the conventional centralized battery systems. This issue has been addressed by implementing passive or active balancing which lead to a bulky and complex management system with limited capabilities. The proposed cascaded modular battery system architecture can address the energy balancing directly, removing the need for the conventional balancing techniques, and also improves the battery system by performing power balancing and bypassing faulty battery modules, this improving system reliability. However, the number of modules should not be increased too much as the complexity and weight of the battery management system will be significantly increased with lower benefits gain.

The problems with PV arrays included the effect of the degraded PV cells (due to the space environment) on the overall performance of the PV-array. Also, the strings with high voltage are at a risk of sustained arcing which might triggered by electrostatic discharge (resulting in permanent damage to these strings). The conventional centralized architectures for PV-panels and their interfaced power regulators could provide a solution for their problems, but tend to oversize the PV-array in order to compensate for this limitations when it occurs. The proposed architecture based on the cascaded modular system can improve the overall performance of the PV-panel as it can control each PV-module separately preventing the weaker cells to affect the overall panel. Also, the PV-modules are not at high voltage levels, so the risk of sustained arcing are significantly reduced. In addition, the modular structure of the PV-panel and its interfacing power regulators make the system inherently fault tolerant and thus improves the system reliability and design flexibility.

Chapter 5. Proposed Modular Multiport Power Converter

Introduction

In previous Chapters, the conventional architecture of the MPPT regulated bus based EPS has been described. This architecture is usually designed based on a number of PV panels with voltages close to the bus voltage. Each PV panel interfaces to a centralized power regulator (PR) which controls the power extracted from the panel based on the power requirements for battery charging and loads as can be seen in Fig. 5-1a .



(a) (b)

Fig. 5-1 Satellite EPS MPPT architectures: (a) Conventional centralized architecture for PV-panels and batteries (b) Cascaded modular based design for PV-panels and batteries

The battery in this architecture is usually interfaced to the DC bus through a bidirectional DC-DC converter which acts as a battery charge/discharge regulator (BCDR) which controls

charge/discharge operations of the battery. The different loads are interfaced to the power bus through the power distribution unit (PDU) with incorporates protection and dedicated isolated DC-DC converters to provide the required different bus voltages. This architecture requires the PV-panels and batteries to be designed with voltages close to the bus voltage which brings the problems related to the PV-strings and battery strings which have been described in Chapter 4.

In Chapter 4, the cascaded modular architectures for the batteries and PV-panels as seen in Fig. 5-1b, were investigated and shown to have advantages over the conventional centralized architectures. However, they may require a higher number of converters connected in cascade with dedicated control loops with measurements, and also the overall system efficiency may be reduced due to multiple conversion stages. The multiport converter (MPC) topologies have been shown to provide more advantages over the conventional distributed converter based systems, including lower cost, higher power density and better efficiency due to the reduced number of conversion stages. The MPC topology can be fully isolated using transformers [105-109] which allow full isolation between all ports. Other alternatives are partially isolated [34, 110-114] or non-isolated topologies [115-120]. The isolated and partly isolated MPCs can provide a galvanic isolation which may be required for some specific applications where the loads are directly connected to the power bus. However the use of a transformer may reduce the power density of these converters, increasing the system weight. Non-isolated MPCs can have simpler control design and better efficiency [121] as well as high specific power. In a satellite EPS, the loads can interface to the power bus through isolated DC-DC converters which adapt the bus voltage to the load specified voltages as well as providing galvanic isolation to protect the power system from faults on the load sides. This means it is feasible to implement the non-isolated MPC on the power generation and storage sides to gain the benefits of these topologies.

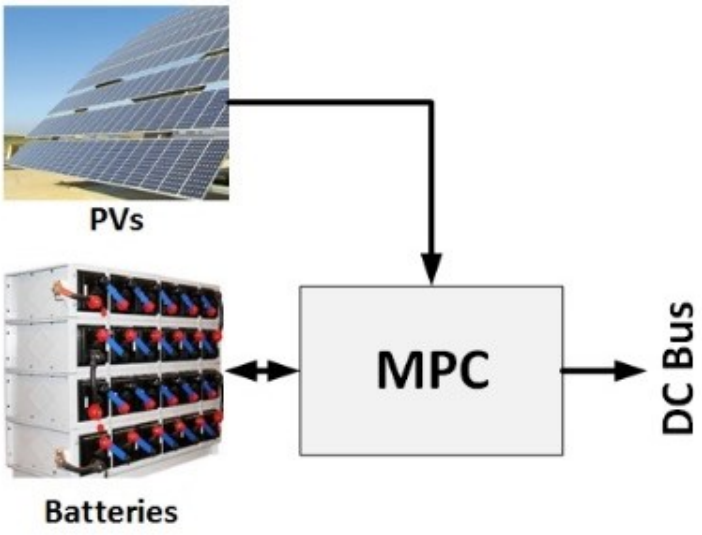


Fig. 5-2 Conventional centralized multiport converter based power system

The structure of most of the proposed MPCs for terrestrial applications was based on centralized architectures, i.e. a central converter interfaces different power sources and energy storage with the load bus as seen in Fig. 5-2. The problem with these centralized multiport converters (CMPCs) when a PV-battery system is considered as in the case of a satellite EPS, is that it must have strings with a high number of series connected PV-cells (and similarly for battery pack) in order to interface conveniently to the higher bus voltage, to minimize the converter current rating which leads to the problems related to battery/PV strings described in chapter4. Also, the centralized architectures of MPCs cannot provide fault tolerance as failure of a converter will cause overall power system failure unless a redundancy has been taken into account.

The first attempt to implement a multiport converter concept for a satellite EPS has been proposed in [122] through the development of an isolated three port converter (TPC) which was used as a building block to be implemented in a distributed architecture to interface independent PV panels and a centralized battery pack as seen in Fig. 5-3. The architecture provided redundancy through implementing two parallel TPCs for each PV-panel channel, each rated at

the full PV-panel power, so that if one converter fails the other can still process the full power of the PV-panel.

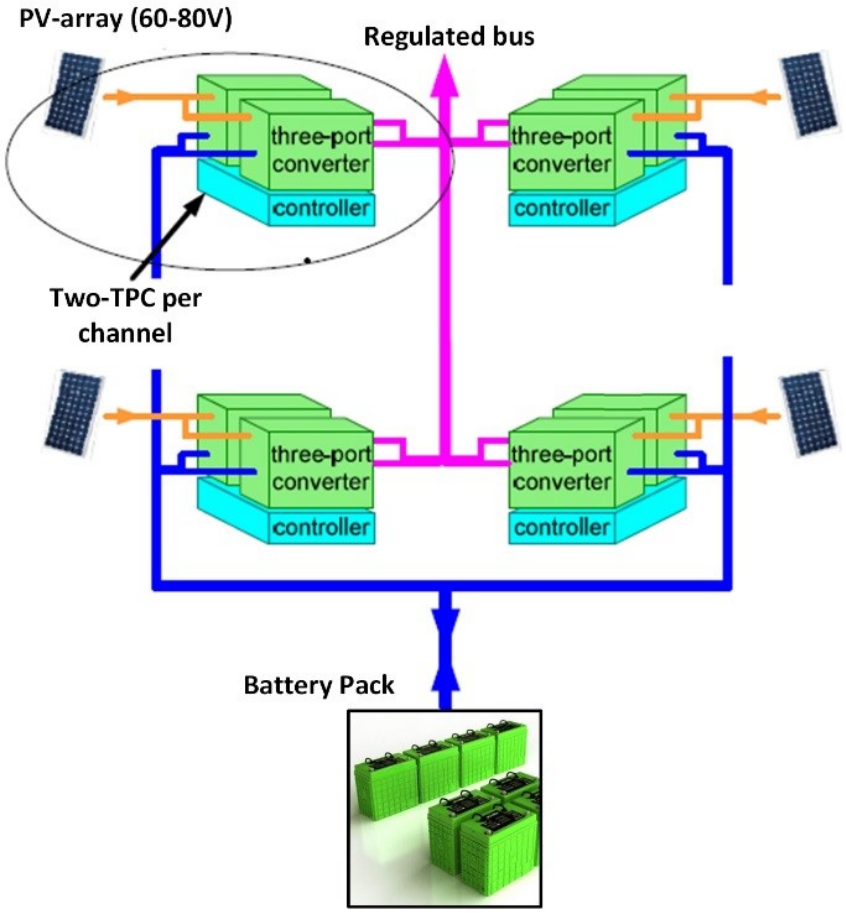


Fig. 5-3 EPS based on distributed three port converter as proposed in [122]

Although this architecture is simple and compact due to the implementation of integrated converters in the form of TPCs, it still has some disadvantages. Firstly, the proposed TPC was based on a partially-isolated topology implementing a transformer which limits the power density of the converter. Secondly, the PV-panels and batteries still need to be designed close to bus voltage by implementing a higher number of series connected cells with their related problems. Also, even if the proposed architecture can be considered as fault tolerant from the

PV-array point of view due to the distributed architecture, it cannot provide any tolerance for partial failures in the battery pack unless additional bypassing mechanisms are implemented.

The proposed modular architecture for a satellite power system is shown in Fig. 5-4. It implements a number of modular multiport converters (MMPC), which will be proposed in this chapter, to interface the PV-array and battery to the power bus. Each MMPC interfaces a number of PV-modules that forms the PV-panel as well as a number of battery modules that form the battery string. This architecture removes the need for a high number of series connected PV/battery strings and their related problems as it combines the advantages of having cascaded battery and cascaded PV-panels.

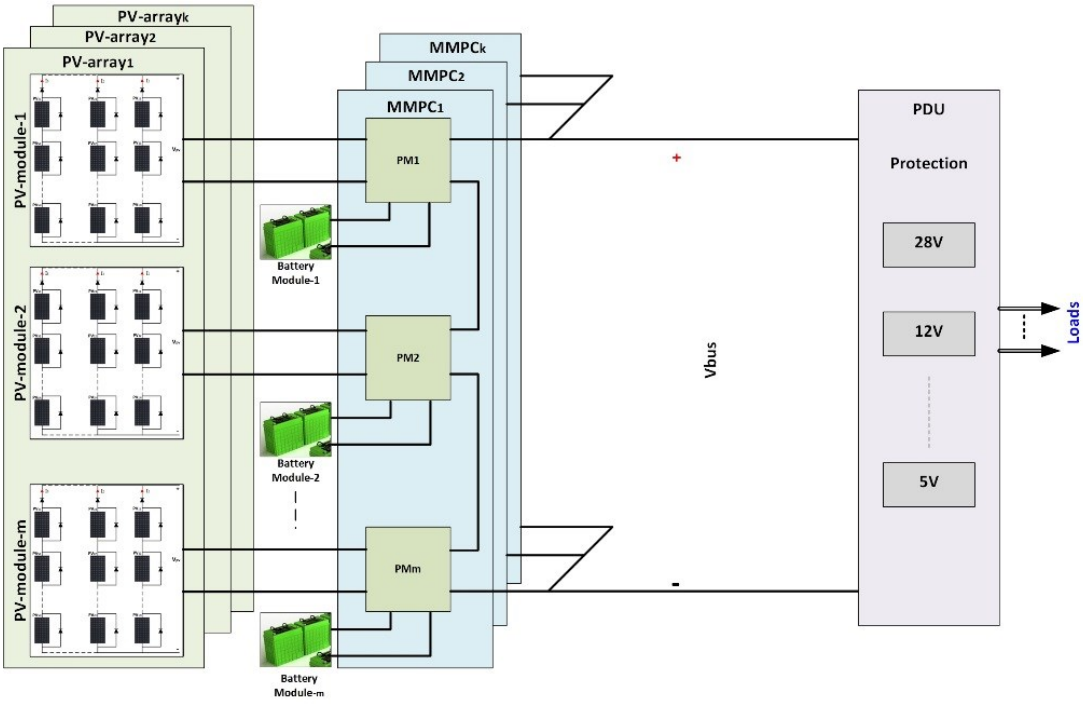


Fig. 5-4 Proposed modular architecture for satellite EPS based on the proposed MMPC

One of the most important features of the proposed architecture is that it can undertake a battery charge and power balancing between battery modules by controlling the power share of each

power module (PM) within the MMPC. In addition, the proposed architecture enables the utilization of battery modules with different characteristics and similarly for PV modules which can allow the demonstration of new battery and PV technologies onboard satellites to gain space heritage with an insignificant effect on the operation or the sizing of the power system. Finally, this architecture can also provide a great fault tolerance for both battery and PV modules as the modules have smaller power contributions within the overall power system.

In this chapter, the topology and analysis of the proposed MMPC will be discussed. The operation of the converter will be simulated under different operating conditions and an experimental setup for an integrated power system implementing a single MMPC will be described to validate the concept, and test data will be discussed. A complete EPS architecture having a number of parallel MMPCs would require a complex experimental setup and require an expensive power management strategy: this is outside the research scope of this project.

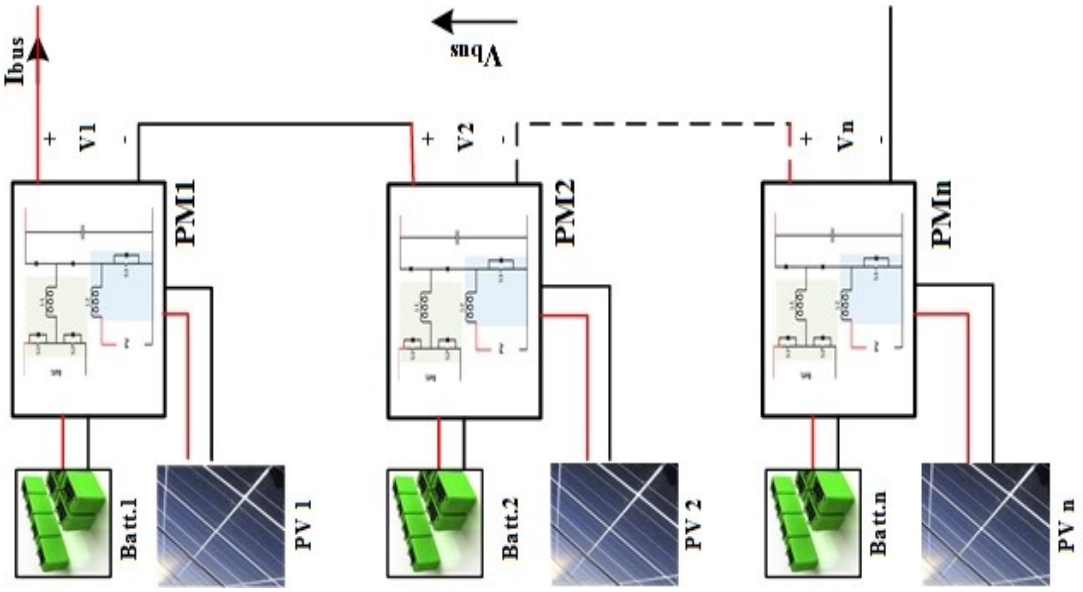


Fig. 5-5. The proposed MMPC architecture

5.1 System level analysis of the proposed MMPC

The proposed MMPC utilizes a number of series connected low power multiport converter (MPC) modules. Each MPC module (power module (PM)) has two input ports interfacing a PV-module and a battery-module to a single output port. The output of the modules which can accommodate different ratings for PV/batteries, are connected in series to form the required full bus voltage as shown in Fig. 5-5.

5.1.1 Global control of the converter

The global controller should ensure the regulation of the bus voltage at the desired value, and manage the power sharing among the PMs according to the available power from the different PV modules as well as the state of charge (SoC)/state of health (SoH) of the battery modules. This is to ensure maximum power extraction from all the PVs as well as charge/stress balancing among all the battery modules.

The power sharing of the individual PMs is controlled through controlling the ratio of output voltage that each PM contributes to the required bus voltage as:

$$P_{bus} = V_{bus} I_{bus} = \sum_{i=1}^{m} P_i \quad ; \quad P_i = I_{bus} V_i \quad \forall i = 1 \dots m \tag{5-1}$$

where P_{bus} is the bus power, I_{bus} is the bus current, m is number of PMs, P_i is the power contribution of the i^{th} PM and V_i is its output voltage which is defined as:

$$V_i = K_i \frac{P_{pv_i} - \frac{\sum_{i=1}^{m} P_{pv_i} - I_{bus} V_{bus}}{m}}{I_{bus}} \tag{5-2}$$

where P_{pvi} is the PV module power of the i^{th} PM and K_i is a sharing factor defined based on the SoC of a module's battery and can be estimated as:

$$K_i = \frac{m\,SOC_i}{\sum_{k=1}^{m} SOC_k} \quad and \sum_{i=1}^{m} K_i(SoC) = m \tag{5-3}$$

The global controller then forwards the module's share of the bus voltage V_i as a reference voltage to the module's local output voltage controller.

During time periods when the PV power exceeds the load and the batteries should be in charging mode, the PMs which interface to the battery modules with lower SoCs should contribute less to the bus voltage/power (smaller V_i) to allow more PV power to be used for charging their battery modules. On the other hand, PMs which interface to the battery modules with higher SoCs contribute higher voltage/power to the bus to maintain the required bus voltage. As a result, a lower PV power will be directed from their PV modules to their battery modules for slower charging.

During the time periods when the PV power is lower that the load, the battery modules will be in discharging mode to supply the load power. PMs which interface to battery modules with lower SoCs should contributes less to the bus voltage/power to allow slower discharging whilst PMs which interface to battery modules with higher SoCs should contribute more to the bus voltage/power to compensate, and this will mean faster discharging and reduction of the SoCs imbalances. Through this strategy, charge balancing can be achieved among battery modules that may be at different SoCs due to batteries capacity mismatching. Balancing of thermal stress among battery modules under mismatched equivalent series resistances (ESR) in the battery cells (which can be significant if there are peak charge/discharge power of the battery) can also

be achieved by adapting the energy management strategy accordingly, however this will not be considered further within this research.

5.1.2 Battery charge balancing range

As the charge balancing among the battery modules is controlled by the different voltage share among the PMs as previously described, the range of output voltage for the PMs determines the range of imbalance in battery modules SoC that can be handled by the MMPC.

The voltage contribution of the PM which interfaces to the battery module at lowest SoC is defined as:

$$V_{min} = K_{min}\frac{V_{bus}}{m} \tag{5-4}$$

In order to keep the bus voltage at the reference value and ensure it is unaffected by the balancing process, based on (5-3), the sharing factor of the PM that interfaces the battery module with highest SoC should satisfy:

$$K_{max} = m - K_{min} - \sum_{i=2}^{m} K_i \tag{5-5}$$

where K_{min} is the sharing factor of the PM which interfaces the battery module with lowest SoC. K_{min} is estimated from (5-4) based on the minimum achievable output voltage which is limited by the voltage transfer ratio of the converter. The voltage share of the PM which interfaces the

battery module with highest SoC should be able to satisfy (5-6) in order to maintain the bus voltage.

$$V_{max} = K_{max} \frac{V_{bus}}{m} \tag{5-6}$$

As can be observed from (5-4) and (5-6), the wider the output voltage range of the PM, the bigger the disparity between battery modules can be handled. The topology of the PM's converter will determine the operating range of the SoC balancing as will be analyzed in the following subsection.

5.2 Proposed MPC topology for power modules

Non-isolated MPCs are usually developed based on a combination of basic DC-DC converters (such as buck, boost, buck-boost) or a reduced form of the combined converter. The most common topology for MPCs is the boost-boost topology which implements boost converters to interface the different power sources to the load port as can be seen in Fig. 5-6a. Although this topology is commonly used in MPCs, it can add some limitations to the proposed MMPC if it is implemented as its PM, due to the limited output voltage range. The minimum output voltage of the PM based on this topology is limited to the battery voltage whilst the maximum output voltage is determined by the boost ratio of the PV converter during the availability of PV power, and the battery converter when PV power is unavailable. If the maximum voltages for battery and PV are designed to be equal at a value of V_{pv} , then the minimum achievable output voltage under this condition is V_{pv}, whilst the maximum achievable output voltage will be more than V_{pv} depending on the boost ratio of the converters. Accordingly, if a boost ratio of two is considered (although feasible, this may affect efficiency), the operating voltage range of the converter will be from V_{pv} up to $2V_{pv}$.

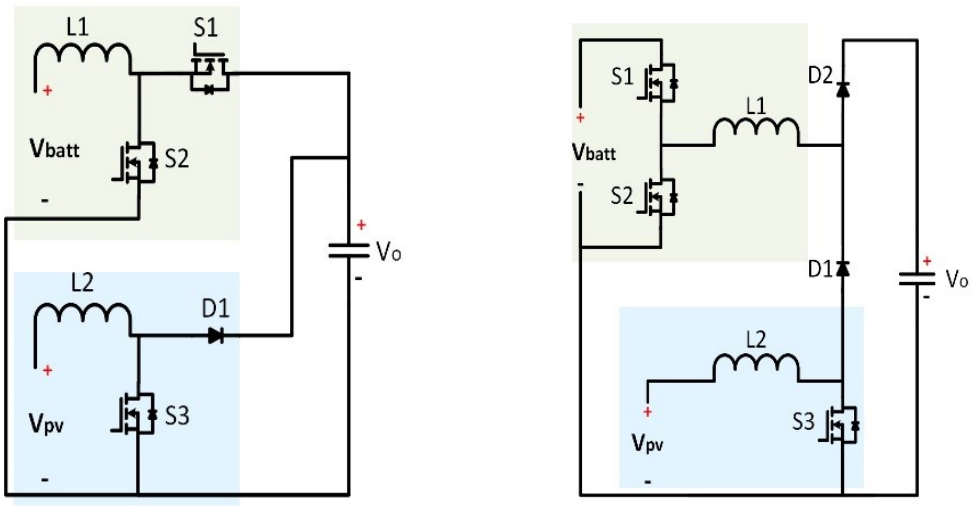


Fig. 5-6 Possible MPC topologies (a) Boost-Boost MPC (b) Proposed topology

The proposed topology for the PM (MPC cell) shown in Fig. 5-6 (b) has been developed based on the integration of a boost cell which interfaces to the PV module and a buck cell which interfaces to the battery module. This topology enables a dual step-down and step-up voltage conversion for the battery voltage providing more flexibility for the choice of battery voltage. To achieve this, blocking diodes D1 and D2 are needed to decouple the PV boost from battery converter in order to extend power flow controllability of the developed MPC. To better analyze the operations of the proposed converter, the three different operating modes will be further analyzed under continuous conduction mode (CCM). Assuming ideal switches with zero dead time between the states of the upper and lower switches (S1,S2) and neglecting the diode forward voltages and inductors and capacitors parasitics.

5.2.1 Single input, double output operating mode

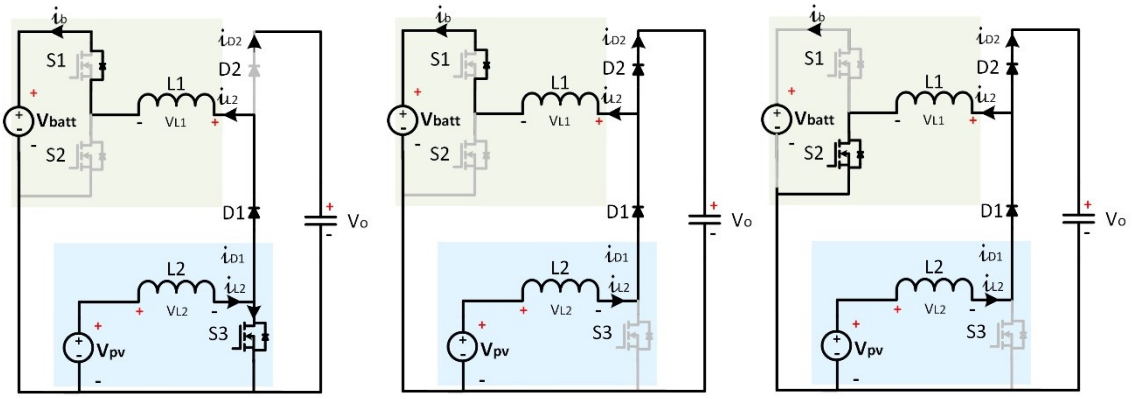
For the single input double output (SIDO) mode, the PV-module provides the power for the load and battery charging which means for all modes described below, the current in L1 will

flow towards the battery. In this mode, the operating modes of the converter which are illustrated in Fig. 5-7 are as follows:

Mode I: is illustrated in Fig. 5-7a: switch S3 is turned ON which means the power extracted from the PV will be used to increase the energy stored in L2 i.e. the voltage across inductor L2 is V_{PV}; due to the initial current in L1, diode D1 will have to be turned on and if switch S2 is OFF, S1 is conducting through its body diode so the voltage across inductor L1 is $-V_{batt}$ which will cause the current to reduce in amplitude.

Mode II: is illustrated in Fig. 5-7b: switch S3 is turned OFF whilst switch S2 is still OFF and S1 is conducting through its body diode. The difference between the currents in inductors L1 and L2 will flow to the output via D2 which means the voltage potential at the common point between L1 and L2 is clamped to Vo. Therefore the voltage across inductor L1 is $(V_O - V_{batt})$ and the voltage across inductor L2 is $(V_{PV}-V_O)$.

Mode III: is illustrated in Fig. 5-7c: switch S3 is OFF whilst switch S2 is ON and S1 is OFF. This has the following implications: the battery is disconnected ($i_{batt}=0$), the voltage across inductor L1 is V_O, therefore the current in L1 increases in amplitude and the current in L2 continues to decrease because the voltage across the inductor L_2 remains negative $(V_{PV}-V_O)$.



(a) (b) (c)

Fig. 5-7 Current flow paths for the operating modes in SIDO mode: (a) Mode I, (b) Mode II, and (c) Mode III.

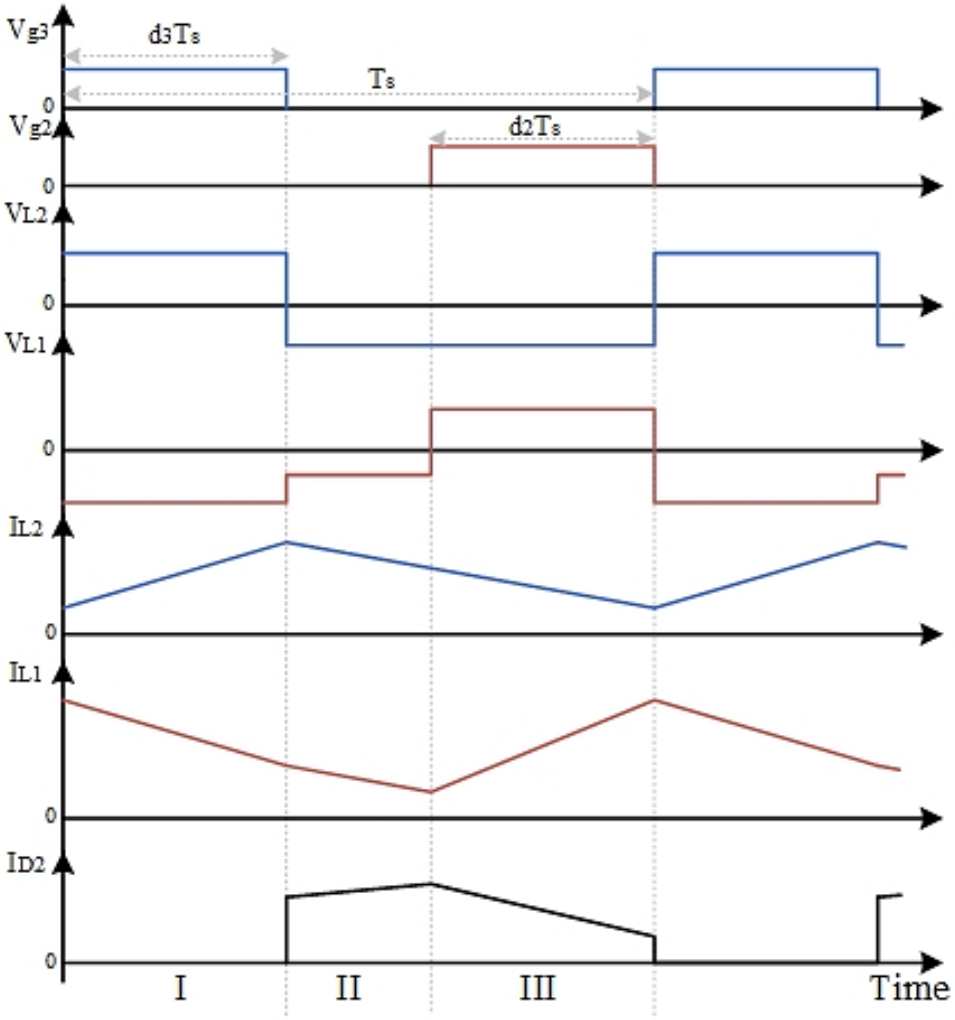


Fig. 5-8 Typical waveforms for SIDO mode for CCM

The typical waveforms of the converter during SIDO mode are shown in Fig. 5-8. By applying the voltage balance principle to inductor L_2, (5-7) can be obtained.

$$V_{PV}d_3 + (V_{PV} - V_O)(1 - d_3) = 0 \tag{5-7}$$

Therefore,

$$V_{PV} = (1 - d_3)V_O \tag{5-8}$$

where d_3 is the duty ratio of the switch S3, V_{PV} is the PV-module's voltage and V_O is the output voltage.

Similarly, by applying the voltage balance principle to inductor L_1, (5-9) can be obtained.

$$-V_{batt}d_3 + (V_O - V_{batt})(1 - d_3 - d_2) + V_O d_2 = 0 \tag{5-9}$$

Therefore the relationship between battery and output voltages and switch duty cycles defined as:

$$V_O = \frac{(1 - d_2)}{(1 - d_3)} V_{batt} \tag{5-10}$$

where d_2 is the duty ratio of switch S2 (noting switches S2 and S1 operate complementary), (5-10) can be reconstructed as:

$$V_O = \frac{d_1}{(1 - d_3)} V_{batt} \tag{5-11}$$

Based on (5-8) and (5-11), the output voltage of the proposed MPC-cell is determined by the duty cycles of switches S1 and S3 (*d1* and *d3* respectively). However, d_3 controls the operating voltage of the PV-module for a defined output voltage to control the extracted power. Therefore d_1 controls the output voltage of the converter based on (5-11) for a given d_3 and actual value of battery voltage V_{batt}.

5.2.2 Double input, single output mode

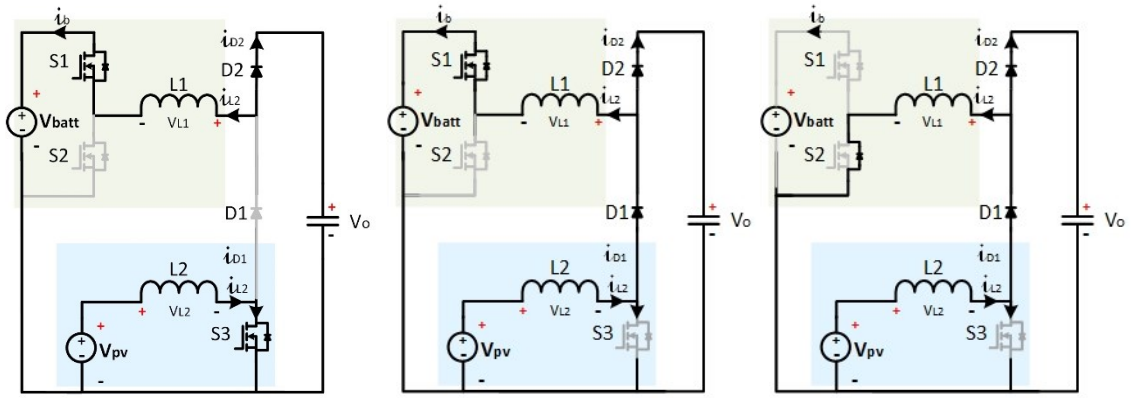
The converter operates in double input single output (DISO) mode when the load demand exceeds the power capability of the PV-module. Therefore the extra power is supplied by the

battery module which means the direction of the current in L_2 is negative. For this mode, the operating modes of the converter are as:

Mode I is illustrated in Fig. 5-9a: switches S3 and S1 are turned ON and switch S2 is OFF which means that the PV is shorted via L_1 forcing the diode D_1 to be reverse biased (OFF) and only the battery provides the required current to the load. This means that the voltage across inductor L_1 is negative (V_O-V_{batt}) and its current raises and the voltage across inductor L_2 is (+V_{PV}) forcing its current to increase.

Mode II is illustrated in Fig. 5-9b: switch S3 is turned OFF whilst switch S1 is still ON. This means the PV will contribute current towards the load and the diode D_1 will conduct. Therefore the voltage across inductor L_1 remains (V_O -V_{batt}) and the voltage across inductor L_2 is negative (V_{PV}-V_O) forcing its current to decrease.

Mode III is illustrated in Fig. 5-9c: switches S1 and S3 are turned OFF whilst switch S2 is conducting through its body diode so the voltage across inductor L_1 is (V_O) causing the amplitude of its current to decrease. The voltage across inductor L_2 remains negative (V_{PV}-V_O) and it current continues to decrease.



(a) (b) (c)

Fig. 5-9 Current flow paths during DISO mode: (a) Mode I, (b) Mode II, and (c) Mode III.

The typical waveforms of the converter during DISO mode are shown in Fig. 5-10. As can be observed, the operation of the PV-converter remains unchanged and consequently it is still governed by (5-8). For the battery converter, applying voltage balance principle on inductor L_1, (5-12) can be obtained.

$$(V_O - V_{batt})d_1 + V_O(1 - d_1) = 0 \tag{5-12}$$

Therefore,

$$V_O = d_1 V_{batt} \tag{5-13}$$

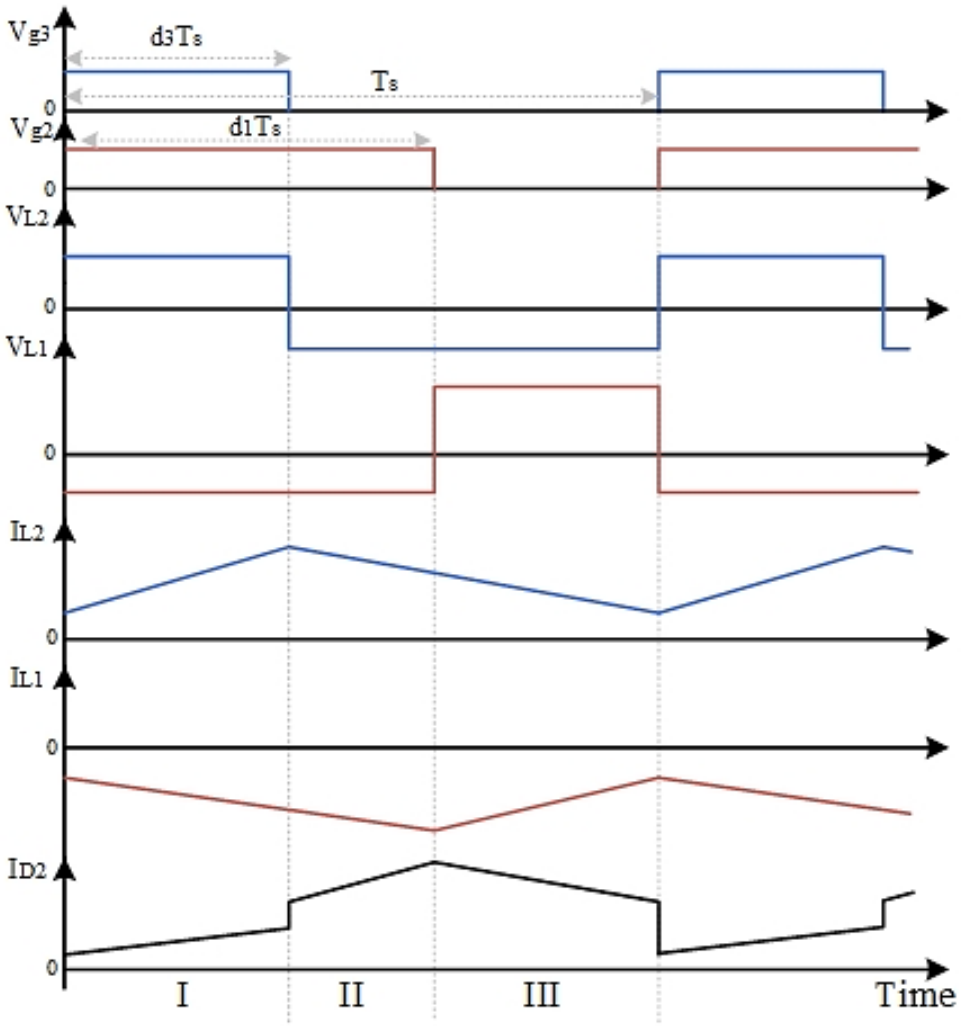


Fig. 5-10 Typical waveforms in DISO mode at CCM

5.2.3 Single input, single output mode

The proposed MPC-cell works in the single input single output (SISO) mode when there is no power available from the PV-module (eclipse condition), therefore all the load power has to be supplied by the battery module. The PV-converter is not in operation, therefore the proposed converter operation during this mode is determined by the battery converter which operates as a normal buck converter and its output voltage is determined by (5-13) in the same way as for DISO mode.

Based on the analysis of the proposed MPC-cell under the different modes of the operation, it can be observed that the output voltage range of the converter ranges is determined by the mode of operation as follow:

During SIDO mode: Based on (5-11), the output voltage of the proposed converter can be varied between 0V up to several times the battery voltage (V_{batt}).

During DISO and SISO modes: The operating voltage range of the proposed converter within this mode based on (5-13) is from 0V up to V_{batt}.

A comparison has been made between the proposed topology and Boost-Boost topology for MPC-cell based on the output voltage ranges at different modes of operations. These are presented in Table 5-1 for 50% maximum duty cycle of the PV-stage switch for better efficiency, and considering the voltage of the PV-module at MPP (V_{MPP}) to be equal to V_{batt}. As can be seen, the proposed topology has a wider range for the output voltage for the SIDO mode which enables a wider control range for the power sharing of each PM for handling a wider range of imbalances between different battery modules as discussed in section 5.1.1.

Table 5-1 Comparison between the MPC topologies

Operation mode	Boost-Boost topology	Proposed topology
SIDO	$V_{batt} < V_O < 2\ V_{batt}$	$0 < V_O < 2\ V_{batt}$
DISO	$V_{batt} < V_O < 2\ V_{batt}$	$0 < V_O < V_{batt}$
SISO	$V_{batt} < V_O < 2\ V_{batt}$	$0 < V_O < V_{batt}$

5.3 Analysis of the proposed MMPC

5.3.1 Converter operation and control

The main objectives of the control scheme of proposed MMPC is to maintain the bus voltage at its desired value whilst ensuring corrective measures are taken to address the imbalance in the SoC of the batteries and/or available PV power among the PMs. To achieve this, a global controller (shown in Fig.5-11) has been proposed to determine the power contribution of each PM. It uses a weighting factor (Ki) calculated according to (4-6), (5-2) and (5-3) and also considers the maximum power available from the PVs of all PMs. These are used to calculate PM's output voltage references V_{i_R} accordingly as can be seen in Fig. 5-12. These are then passed to the local PM control loops which control the duty cycles of S_{i3} (d_{i3}) and S_{i1} (d_{i1}) in order to achieve the reference output voltage as seen in Fig. 5-13. The gains of the PI controllers are selected such that avoiding interaction between the control loops and fine-tuned based on trial and error until reaching an accepted performance for the converter. However, the future work will consider the proper design of these control loops based on the analytical model of the converter. The controller parameters of the global bus voltage controller were (kp=7,ki=20), where the parameters of the local voltage controller were (kp=2,ki=20) and (kp=0.1,ki=10) for the battery current controller. During the battery module charging process, based on the maximum possible charging power of PM's battery, each PM local controller determines the

operating mode of its PV-converter (MPPT) either to work at or away from MPP in order achieve the module's reference output voltage requested by the global controller.

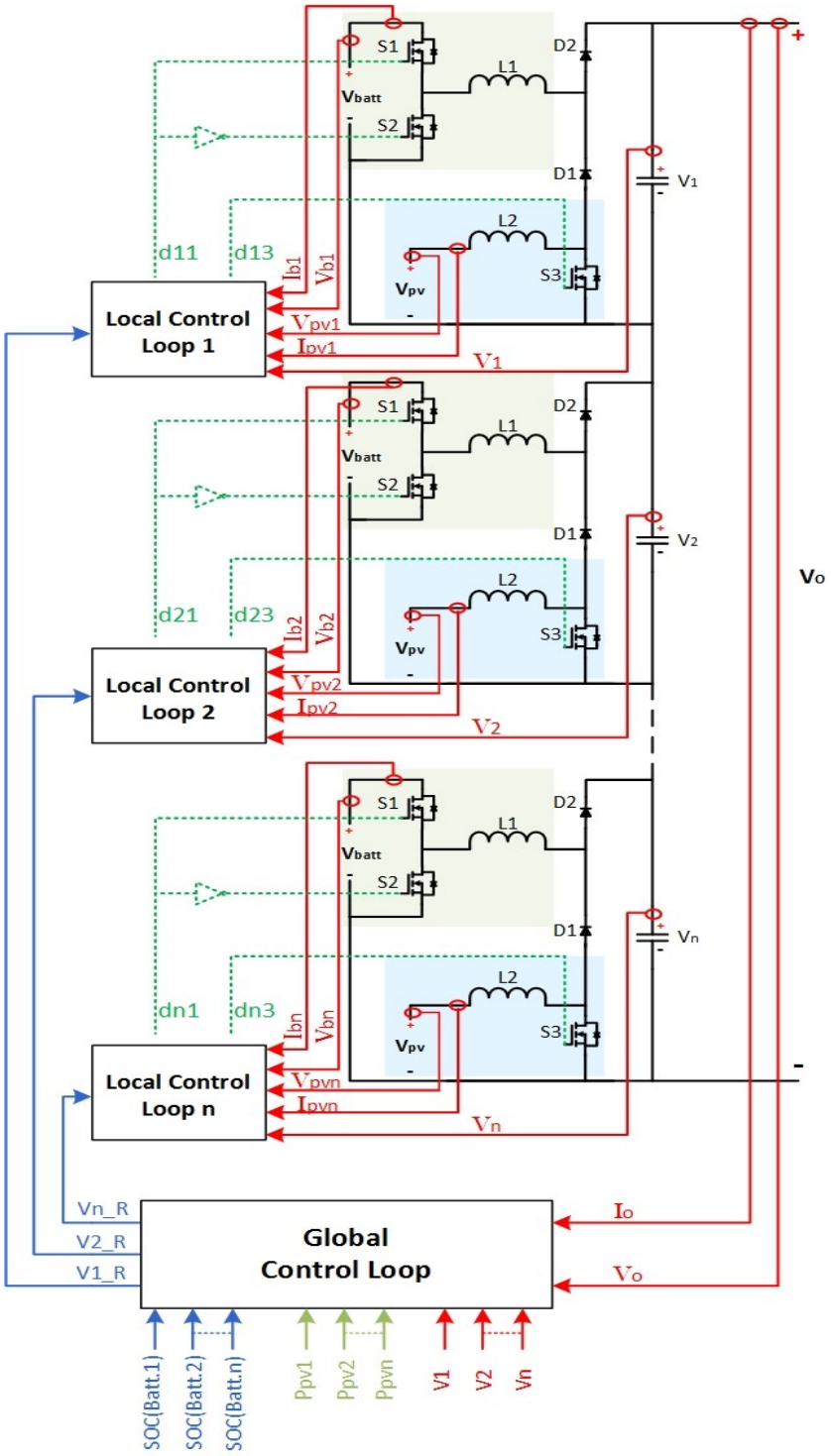


Fig. 5-11 Block diagram of the proposed MMPC

If a fault in any one of the PMs is prevents it delivering its desired power contribution to the bus, this imbalance will cause its output voltage to drop down to zero, causing the forward bias and therefore conduction of the diodes D1 and D2 as well as the anti-parallel (body) diode of S3. This means there will be a natural bypassing of the faulty module. Losing the voltage contribution of this faulty module will be detected by the global controller which will then modify the reference voltage of the remaining PMs in order to compensate for that fault and to maintain the bus voltage at its reference value. These measures can provide a wide range of fault tolerance for the proposed power system: this is one of the important advantages of the proposed MMPC.

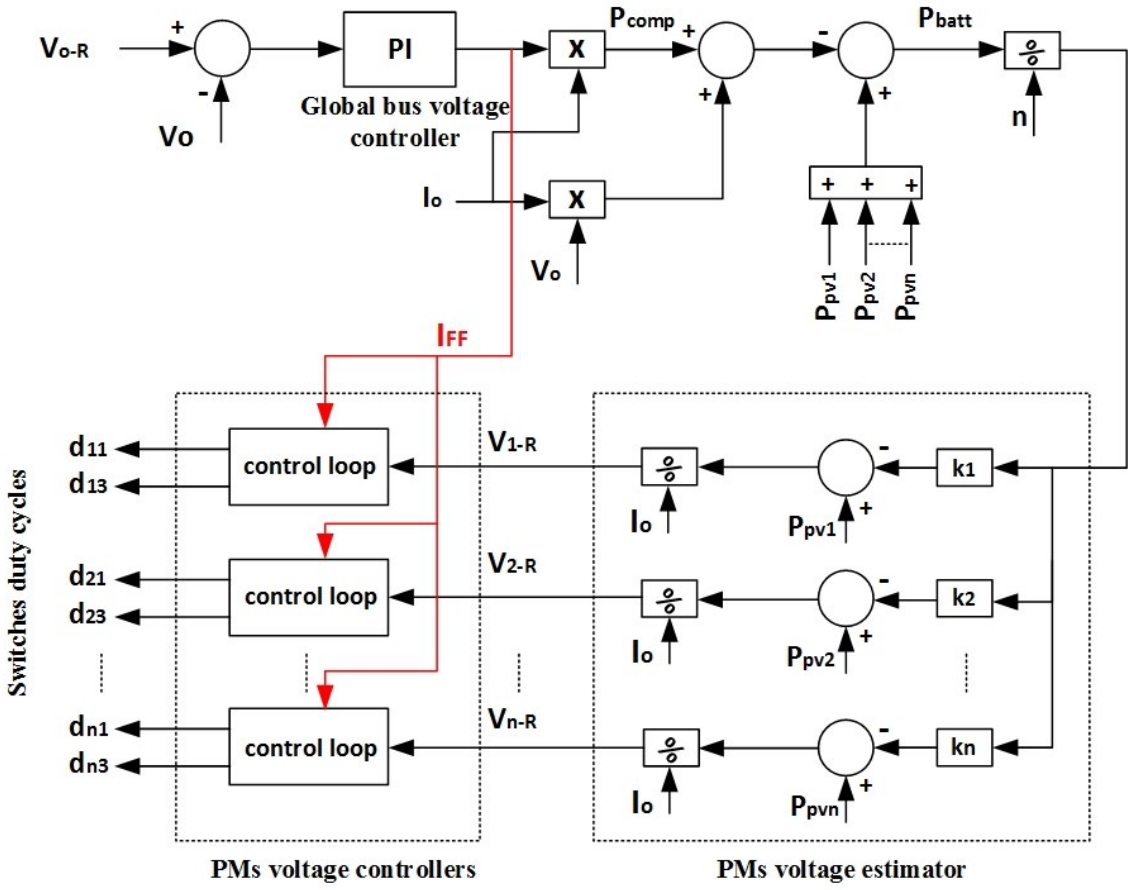


Fig. 5-12 Block diagram for the control strategy of the proposed MMPC

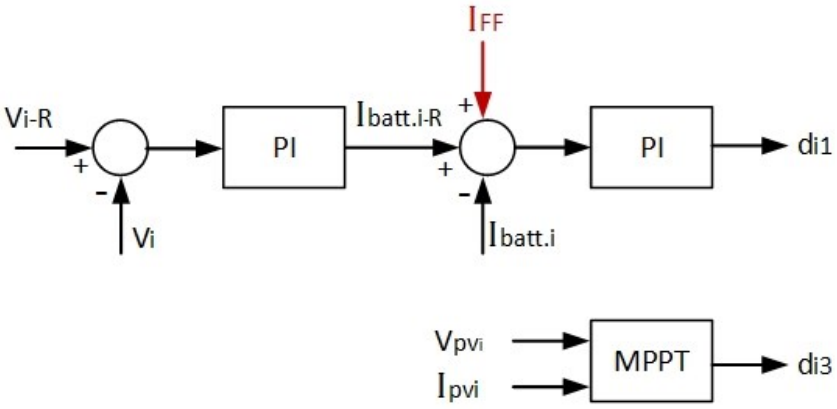


Fig. 5-13 Block diagram for the PM voltage local control in the proposed MMPC

5.3.2 Converter design analysis

The selection of the voltage ratio between the battery-module and the PV-module which interface to the PMs is one of the important design parameters of the proposed MMPC as it determines the imbalance range that can be handled between different battery-modules used in PMs. Based on the converter topology developed for the PM cells, during battery charging, if the PM's PV-module is operating at its MPP, then the minimum achievable output voltage for this PM is $V_{pv\text{-}max}$ which is the voltage of its PV-module at MPP. During the battery charge/discharge cycle, the maximum achievable output voltage of the PM is the voltage of its battery-module (V_{batt}). As a result, the maximum imbalance in SoCs between the PMs' batteries that can be handled can be estimated based on (5-3) and (5-4) under these conditions as:

$$\frac{SOC_{max}}{SOC_{min}} = \frac{V_{batt}}{V_{pv-max}} \tag{5-14}$$

As can be observed from (5-14), the wider the range between the battery-module's voltage and the PV-module's voltage at MPP, the wider the imbalance among the PMs' batteries can be handled. However, the wider range of voltage increases the maximum duty cycle of the battery

and PV switches which in turn increases the size of the inductors and affects converter efficiency as well due to the increased RMS current through the PV switch and the current ripples for the battery inductor that lead to increased power losses. Therefore a trade-off between balancing range, size of the inductors and converter efficiency must be applied for best selection of the PMs' battery and PV-array voltages. The proposed model and the experimental setup have been designed considering a battery-module voltage which is twice the PV-module voltage at MPP ($V_{batt} \approx 2V_{pv\text{-}max}$). Accordingly, under balanced power from the PV modules and balanced SoCs for the battery modules at all PMs, the voltage contribution of each PM will be:

$$V_i = \frac{V_{pv-max}+V_{batt}}{2} = \frac{Vo}{m}; \qquad V_{batt} = 2V_{pv-max} \tag{5-15}$$

where *Vo* is the MMPC output voltages and *n* is the number of PMs. As $V_{batt=} 2V_{pv\text{-}max}$, the exact value of the PV-module voltage that interfaces to each PM can be defined as:

$$V_{pv-max} = \frac{2}{3}\frac{Vo}{m} \tag{5-16}$$

Sizing of the PM's inductors for both the battery-stage (L1) and the PV-stage (L2) should ensure the targeted inductor current ripple even under the conditions which cause the biggest mismatch between the output voltages of the PMs. The minimum inductance of the PV-stage's inductor *L2* can be estimated considering the maximum current ripple that occurs at maximum output voltage of the PM ($V_i \approx V_{batt} \approx 2V_{pv\text{-}max}$) as:

$$L_2 = \frac{V_{pv-max}}{2\Delta I_{pv} f_s} \tag{5-17}$$

where ΔI_{pv} is the peak-to-peak inductor current ripple of the PV-stage and f_s is the switching frequency. Similarly, the minimum inductance of the battery-stage's inductor *L1* can be

estimated considering the maximum current ripple that occurs at minimum output voltage of the PM ($V_i \approx 0.5V_{batt} \approx V_{pv\text{-}max}$) as:

$$L_1 = \frac{V_{batt}}{4\Delta I_b f_s} \tag{5-18}$$

where ΔI_b is the peak-to-peak inductor current ripple of battery-stage.

According to equations (5-17) and (5-18), the inductance of the battery-stage inductor is expected to be much bigger than the PV-stage inductor. This is because the battery-stage inductor average current is much smaller than the PV-inductor current especially during the battery charging cycle under constant voltage mode (CVM). This requires a bigger inductor to keep the current ripple within a reasonable value as a percentage of the average current.

Determining the number of PMs is also one of the key design parameters of the proposed MMPC, as it defines the maximum utilization of the battery modules and the available power from the PVs. A larger number of PMs improves the utilization of the battery cell capacities under battery cell imbalances, and also increases the maximum power extraction from the PV-cells under cell mismatch. Increasing the number of PMs also decreases the voltage stress of the switches which enables the use of low voltage rating devices with significantly reduced parasitic resistances and capacitances which reduce conduction and switching losses of the switches and boosts system efficiency.

Increasing number of PMs also increases the fault tolerance range of the MMPC, but it also increases its complexity due to the increased number of control loops and their associated measurements and PWMs. The selection of the number of modules is a tradeoff between efficiency, complexity, and maximum utilization of battery capacity and available power from PVs defined by the application. Based on the multi-objective analysis made in chapter4 for the selection of the best number of cascaded modules, five PMs are considered the best choice for a

100V bus voltage, and the overall number of battery cells to be connected in series is 30 cells. However, for the experimental work, due to the limited capability of the available control platform in terms of analog inputs (only 20 channels), the number of PMs has been reduced to three modules. The future designs of the proposed MMPC should investigate the implementation of distributed controllers for the PMs by using low cost controllers at each PM which interface to the global controller through a communication channel.

5.4 Simulation studies

In order to evaluate the performance of the proposed MMPC under different conditions, a simulation model for the converter has been developed using PSIM® simulation environment in conjunction with the battery and PV models that were developed in chapter3. The SoC of the battery module are estimated using Coulomb-Counting method as:

$$SoC(\%) = SoC_o(\%) + \frac{I(t)\Delta t}{Cap} \qquad \text{Ah} \tag{5-19}$$

where SoC_o is the initial state of charge of the battery, Cap is the battery module's capacity and I is the battery current during the time Δt which is the time-step. Accordingly, SoC imbalance between the different modules can be simulated by setting SoC_o for each module differently. A long simulation time is required to give a noticeable change in battery module SoC as a very small time-step ($1e^{-5}$ Second) is required to simulate the operation of the converter for 10kHz switching frequency. For this reason, an accelerated model for the battery SoC has been used by considering Δt in (5-19) to be 100 times the time-step which in turn accelerates the simulated change in battery SoC by 100-times.

The imbalances in the performance of the PV modules are simulated by the input of different irradiance values to the models of the PV-modules which in turn generate different powers. The

model of the PV module gives the estimated maximum power available from the PV which can be compared to the extracted power from that module to check the operation of the MPPT.

The operation of the converter is simulated for different conditions including imbalanced battery-modules, imbalanced PV power available at the PV-modules as well as load steps using the developed simulation model shown in Fig. 5-14.

5.4.1 Operation with imbalanced battery-modules

The simulated operation of the proposed converter for imbalanced battery modules over a single charge/discharge cycle is presented in Fig. 5-15. The reference value for converter output voltage is set to 90V where the load power was 200W during both sunlight and eclipse periods. Initially, the battery modules were at different SoCs. The battery module (*batt1*) interfaced to PM1 was at the highest state of charge (SoC1=84%) and battery module (*batt3*) that interfaced to PM3 was at the lowest (SoC3=50%), where battery module (*batt2*) that interfaced to PM2 SoC2=68%. During the sunlight period (0< t > 6 S), the maximum power available at the PV-module1 (*PsaAv1*), PV-module2 (*PsaAv2*) and PV-module3 (*PsaAv3*) were the same (≈180W each). The MPPT succeed to maintain the extracted power from the PV-modules (*Ppv1*, *Ppv2* and *Ppv3)* at the estimated maximum available power (*PsaAv1, PsaAv1 and PsaAv1)*. In order to perform charge balancing for imbalanced battery modules, the voltage contribution of PM1 (Vc1) is set to be highest (≈40V) in order to direct higher power from its PV-module to the power bus and less power to its battery module. On the other hand, the voltage contribution of PM3 (Vc3) is set to be lowest (≈20V) in order to direct lower power from its PV-module to the power bus and more power to its battery module. The voltage contribution of PM2 (Vc2) is set to between Vc1 and Vc3 (≈30V) to allow moderate power to the bus and its battery-module.

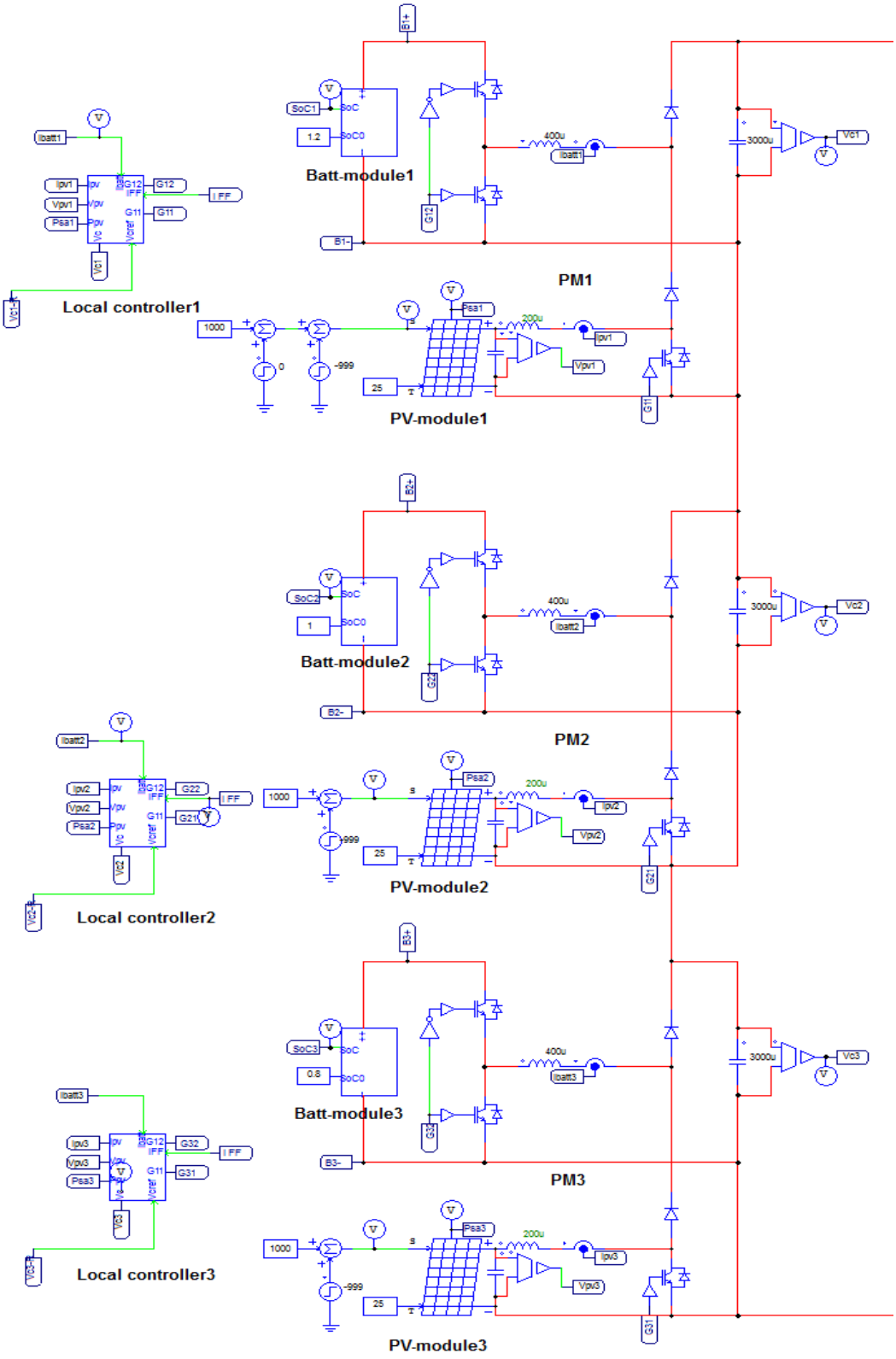


Fig. 5-14 PSIM based simulation model for the proposed MMPC

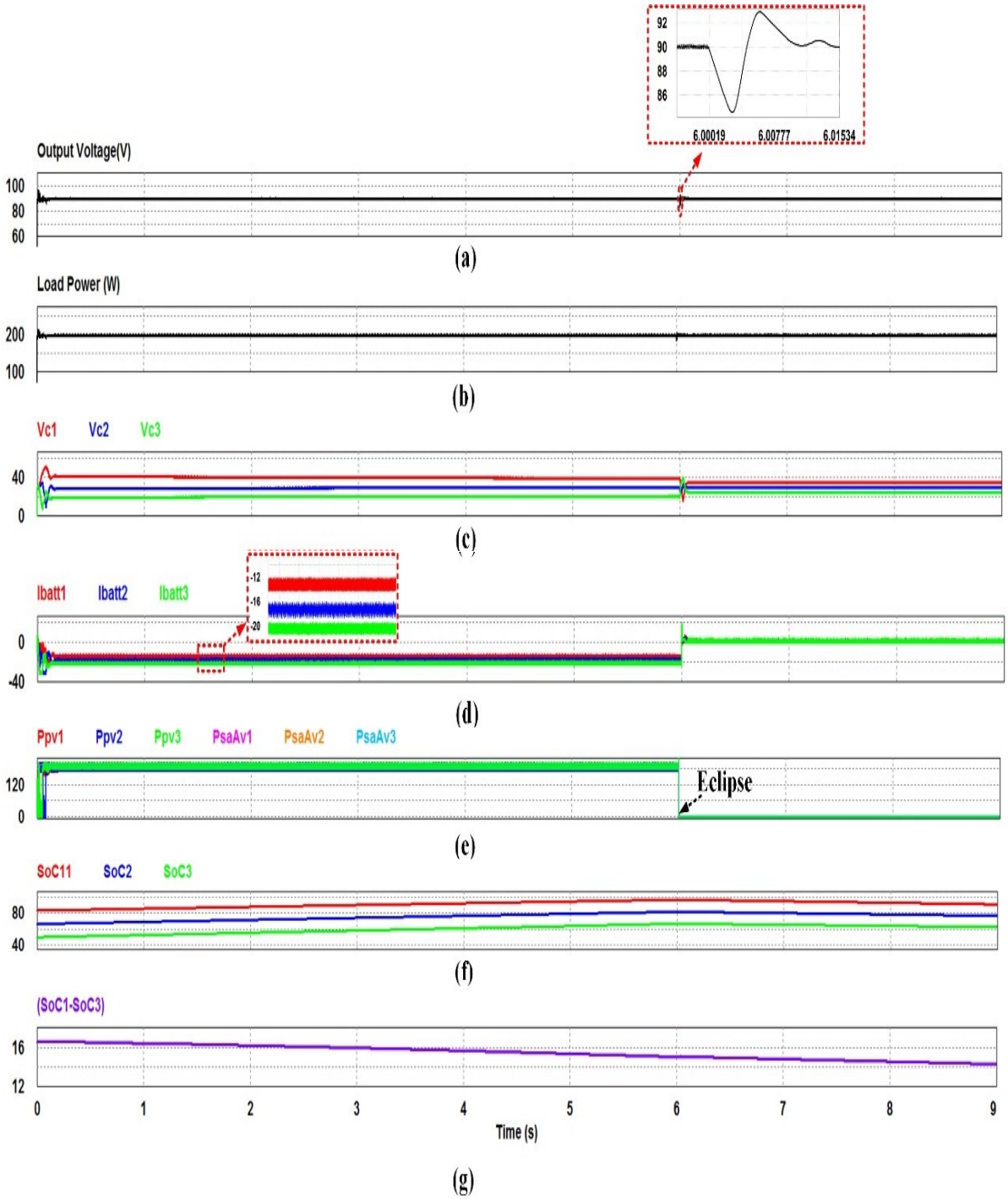


Fig. 5-15 Simulated operation of the proposed MMPC with unbalanced battery modules: (a) converter output voltage (b) load power (c) PMs output voltages (d) battery-modules inductor currents (e) PV-modules power (f) battery-modules SoCs (g) difference in SoC between *batt1* and *batt3*.

As can be seen, the charging currents of the battery-modules are different, the average inductor current at *batt1* was the lowest (Ibatt1≈13A), where *batt3* was the highest (Ibatt3≈21A) and *batt2* was in between (Ibatt2≈18A). As a result, differences in the SoCs of the battery-modules started to converge as can be seen in Fig. 5-15(g) representing the difference between *SoC1* and *SoC3* (*SoC1*-*SoC3*). At time (t=6s), the power from the PV-modules disappears due to eclipse. The battery modules are then switched to discharge mode to supply the load power.

The charge balancing mechanism is still in place and the differences in the SoCs continued to converge. Reaching the full balanced charge may take a number of cycles based on the level of imbalances between the batteries.

The transient response of the converter output voltage due to the disturbance caused by the sudden removal of PV power has been magnified in Fig. 5-15(a). It shows a drop of ≈ 6% of the output voltage for a duration ≈ 5mS due to the time constant of battery inductor circuit and small value of output capacitor. If this transient level is not acceptable for the application, the capacitance of the output capacitor should be increased to support the required energy during the transient time.

5.4.2 Operation with unbalanced PV-modules

The simulated operation of the proposed converter with imbalanced power from PV-modules over a single charge discharge/cycle is presented in Fig. 5-16. Initially, the SoC of all battery modules are balanced, also the available power from all the PV-modules are the same. Accordingly, the voltage contributions from all the PMs are the same (*Vc1*=*Vc2*=*Vc3*=30V) and the battery inductor currents are the same. At time (t=2s), a disturbance is introduced to the converter by reducing the available irradiance to the PV-module at PM2 by 50% which in turn

reduces the power available from this module by 50%. The converter responded to this disturbance by setting the voltage contribution of PM2 to minimum, in order to minimize the

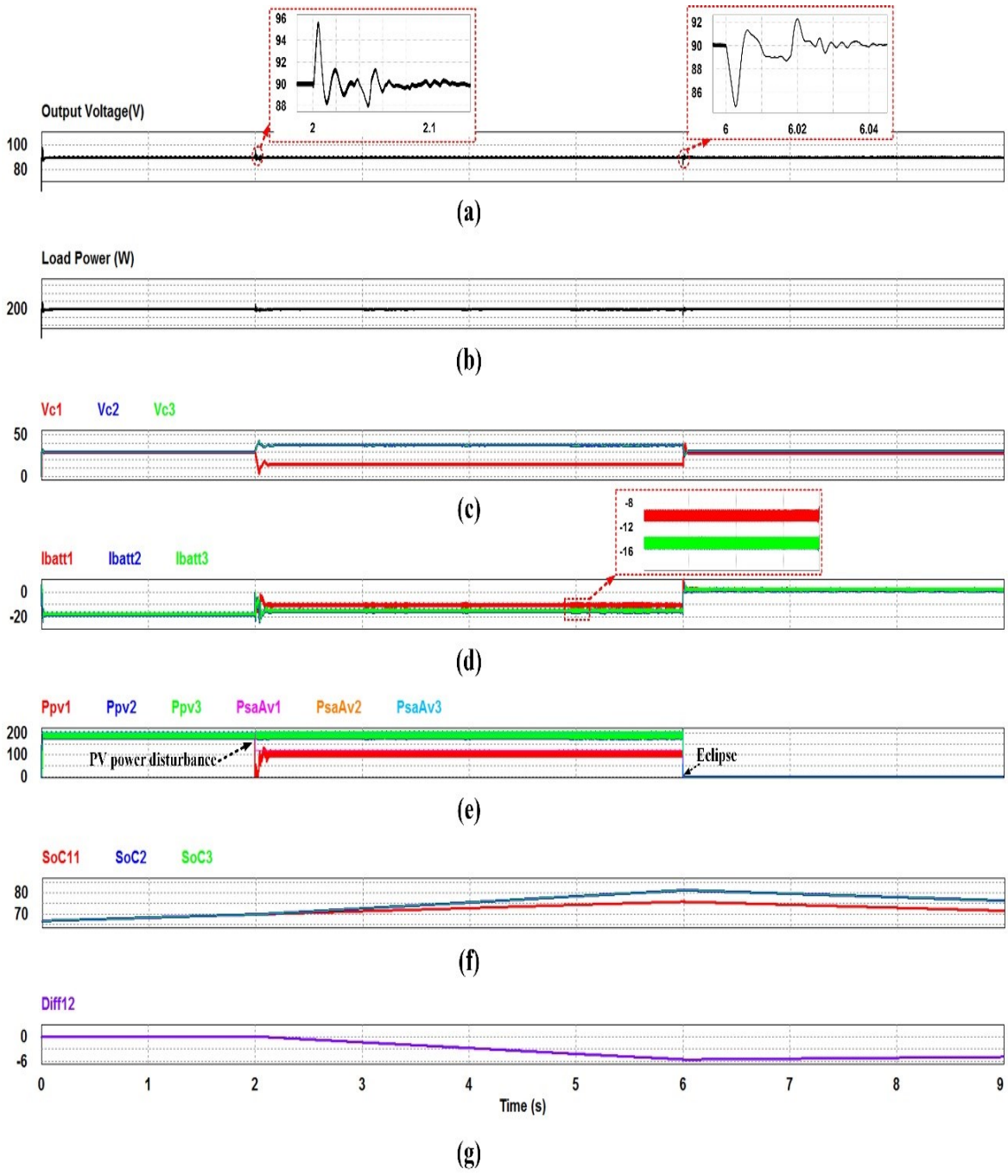


Fig. 5-16 Simulated operation of the proposed MMPC with unbalanced power of PV-modules: (a) converter output voltage (b) load power (c) PMs output voltages (d) battery-modules inductor currents (e) PV-modules power (f) battery-modules SoCs (g) difference in SoC between *batt1* and *batt2*

power contribution to the bus allowing maximum charging power to its battery-module to minimize the divergence in the SoCs of the battery-modules. PM2 and PM3 compensate equally for the lower voltage/power contribution of M1 to the bus. As a result, the difference in the SoC between batt1 at PM1 (which has 50% less PV power), and batt2 and batt3 at PM2 and PM3 was limited to 6% at the end of charge process before the starting of the eclipse. The MPPT required a time of 100ms until it reached the new MPP after the disturbance was introduced which caused a small transient to the output voltage of the converter. At time (t=6s), the power from the PV-modules has been removed due to the eclipse. The battery modules are switched to discharge mode to supply the load power. The small imbalance in the SoC of the battery-modules that occurred during the charging period is detected which in turn activates the charge balancing mechanism and the differences in the SoCs start to converge. As can be seen, the converging of the SoCs is slow, due to the small difference in the SoCs (6%) which in turn triggers a small difference in the voltage/power contribution of the PMs batteries power according to the linear relationship in equations (5-2)(5-3). For this reason, it may be more useful in the future (depending on the application) to implement a smart algorithm that can define the sharing factors (Ki) by taking into account the targeted time to achieve the balanced state, in additional to the imbalance level and the capability range converter.

5.4.3 Operation with peak-pulse loading

The simulated operation of the proposed converter under peak power pulse is presented in Fig. 5-17. It simulate a peak loading of 1kW applied during the time (1s < t > 1.5s) to test the response of the converter under balanced SoCs for the battery-modules and balanced powers from the PV modules. As can be seen, the power from the PV modules exceeded the load power during time (0 < t > 1s). The extra power was directed to charge battery modules equally due to the balanced SoCs. At time (t=1s). The load power was increased from 200W to 1kW which

exceeds the available power from the PVs, the battery-modules switched from charging mode to discharging mode in order to supply the extra power for the load. As the battery current did not

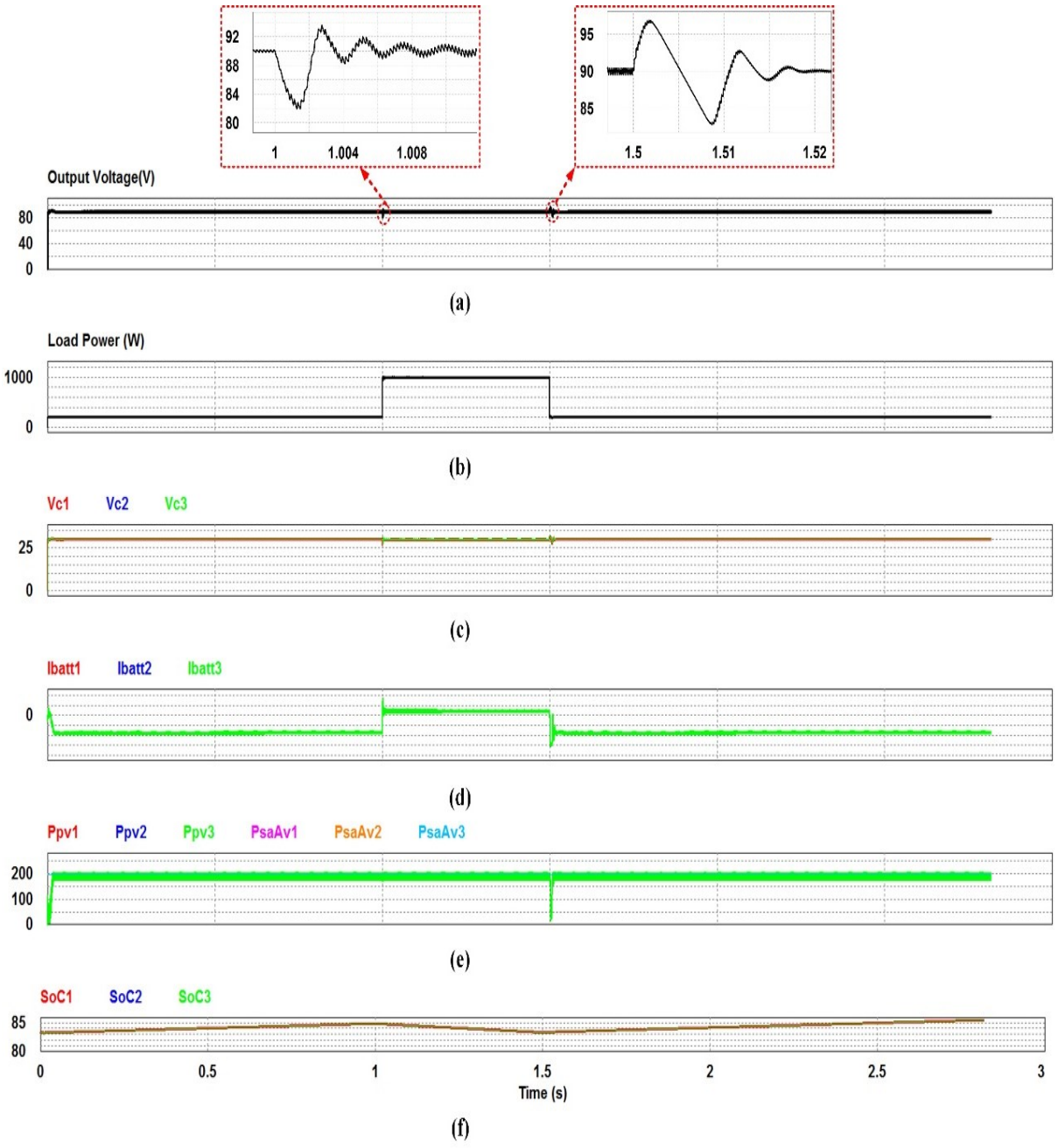


Fig. 5-17 Simulated operation of the proposed MMPC with peak-pulse loading:
(a) converter output voltage (b) load power (c) PMs output voltages (d) battery-modules inductor currents (e) PV-modules power (f) battery-modules SoCs

respond immediately to this change (due to the time constant of the inductor of the battery-module L1), the output capacitor had to supply a part of load power until the battery current reaches its reference value which caused the output voltage to drop to 82V (-6%). Similarly, when the load reduced again to 200W at (t=1.5s) the output voltage was disturbed by (±6%) due to the battery current response as well as the disturbances on the MPPT.

5.5 Experimental Validation

5.5.1 Testing prototype

In order to validate the proposed MMPC topology, an experimental prototype has been built for a 1kW integrated power system with 75V bus voltage Fig. 5-18.

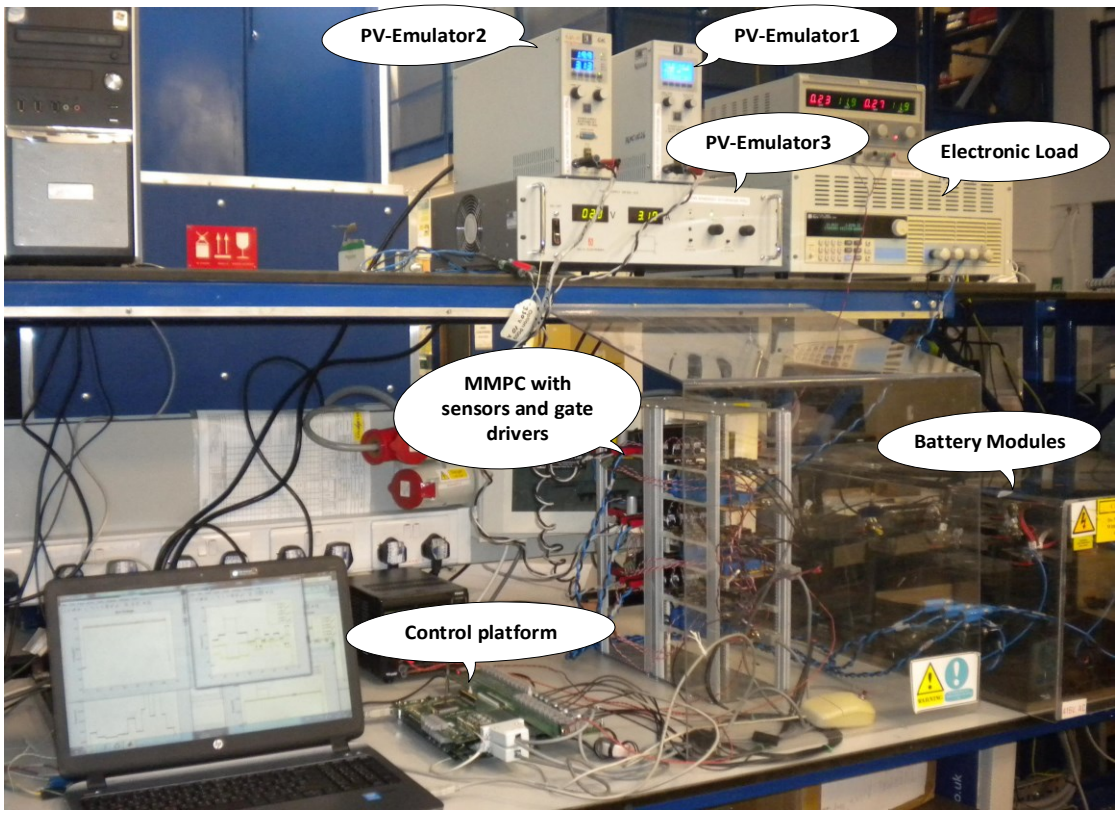


Fig. 5-18 Experimental setup for testing of the proposed MMPC

The prototype consists of three PMs (M1, M2 and M3) built based on the proposed topology discussed in section 5.2. Each PM interfaces a lead acid battery-module that has been used as energy storage element as a cheap alternative to the Li-ion battery for this experimental setup. This is not affecting the validation of the proposed converter and its ability to interface Li-batteries as it interfaces batteries in modules rather than cells and being able to interface different chemistries at the different battery ports. Programmable power supplies was used as PV-modules emulators.

5.5.1.1 Design of the PMs

The design specifications of the PM are shown in Table 5-2. The switching frequency has been set to 10kHz due to the limited speed of the available control platform. This meant the MMPC prototype was bulky and not compact: this can be accepted for a proof of concept experimental setup. However, a real design for the proposed MMPC should implement a powerful control platform with reasonable speed to enable the switching frequencies up to 100 kHz or more which would results in a significant reduction in passive component size, producing a very compact and light weight converter.

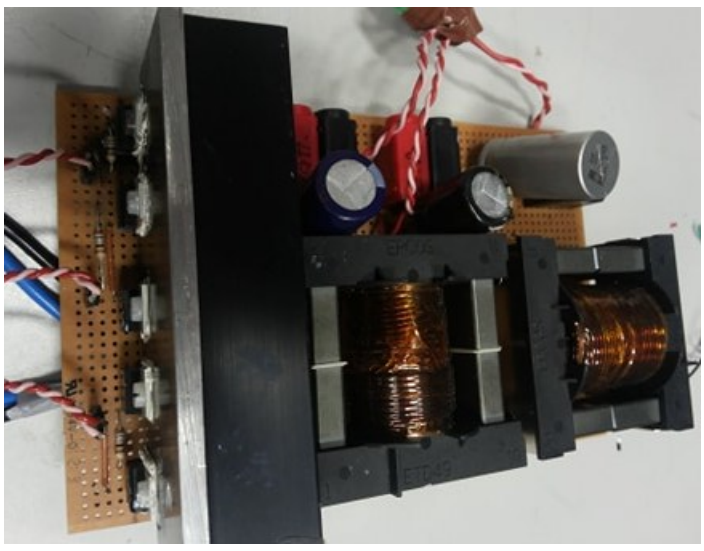


Fig. 5-19 Single power module board

The MOSFETs within the PMs are connected to gate drive circuits which have been designed based on modular architecture to enable reconfigurable designs. Three gate-driving modules have been designed to drive the MOSFETs of the three PMs, each gate drive-module can drive up to four MOSFETs. In order to ensure the isolation between the power system and the control platform, the connections of PWM signals from the control platform to the gate driving circuit are made through optical fibres. The PWM signal are sent optically by an optical transmitter in the FPGA board and received by the optical receiver implemented in the gate driving modules.

Table 5-2 Experimental setup specifications

Symbol	**description**	**Value**
V_{batt}	Battery module voltage	36 V
$V_{PV\text{-}max}$	PV module voltage at MPP	17 V
L_1	Battery converter inductor	375 μH
L_2	PV converter inductor	187 μH
M	Total number PMs	3
I_{bus}	Maximum Load current	14A
V_{bus}	Bus voltage	75V
f_s	Switching frequency	10kHz

5.5.1.2 Gate driving modules

The gate drive circuits for the MOSFETs have been designed in a modular form. Each gate drive module is designed to drive the three MOSFETs located in the single PM, plus one additional drive as a spare as presented in Fig. 5-20. The PWM signals are carried though the fiber optic cables, where the presence of light representing logic ‘’1’’ which in turn received by fiber optic receiver and is inverted to logic ‘’0’’ due to the operation of the receiver. The signal generated from the receiver should therefore be inverter. Schmitt trigger and inverter selected in order to enhance the noise immunity of the gate driving circuits. A delay of the rising edge of the PWM signal is introduced to prevent the upper and lower switches of the converter from

being ON at the same time. This is controlled by the FPGA based on the settings defined in the DSP code, so the gate drive circuits are not equipped with a hardwired time delay.

The MOSFET gating signals are isolated from the 5V power supply at the logic side by means of the implemented optocouplers (HCPL3120), while isolated DC-DC converters are used to provide the ±15V gating voltage for every MOSFET separately. The schematic diagram for a single gate drive circuit per gate drive module are presented in Fig. 5-22Fig. 5-21.

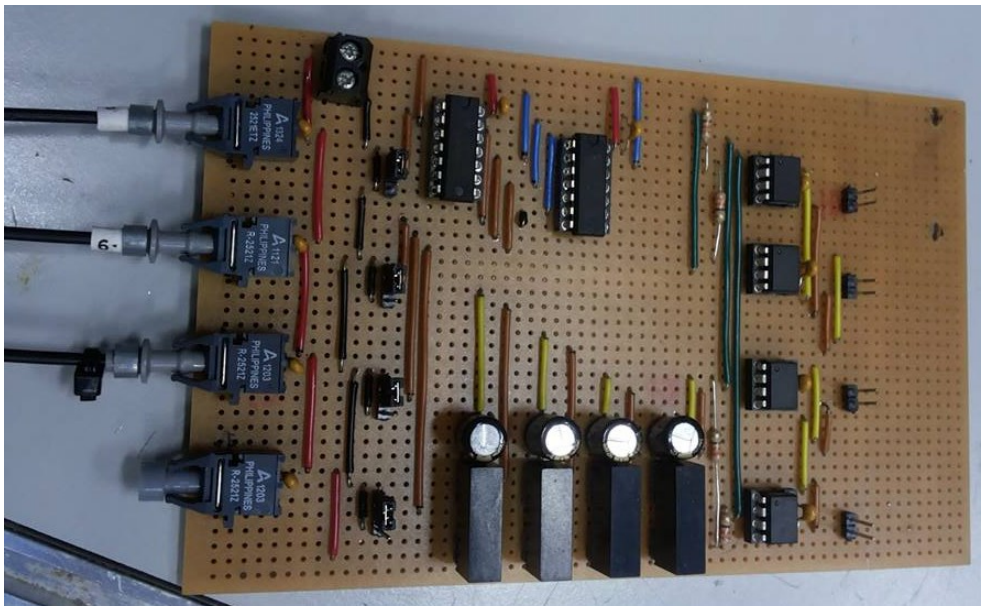


Fig. 5-20 Single gate-drive module board

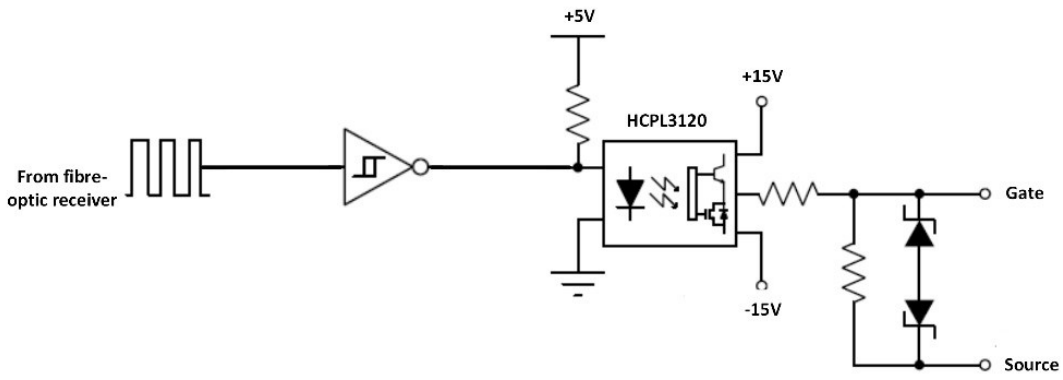


Fig. 5-21 schematic diagram for gate-drive circuit of a single MOSFET

5.5.1.3 Control platform

The digital control platform consists of two parts. The first part is an Actel ProASIC®3 based FPGA based board designed within PEMC research group at University of Nottingham. The second part is the DSP board C6713 DSK developed by Texas Instruments [123]. The DSP board is additionally equipped with a HPI daughter-card which is used by the graphical user interface (GUI) for communication with the DSP to enable monitoring of different parameters and measurements from the DSP. The FPGA board presented in Fig. 5-22, generate the PWM signals based on the received control variables from the DSP. It also reads the ADCs and interrupt the DSP to pass the readings based on configurable time periods. It includes 21 registers to be used for storing the relevant settings and data, such as interrupt period, control bits, trip status/control registers, the readings from analog-to-digital converters (ADC), and the DSP can read/write from those registers. The clock of the FPGA board is 50MHz, which is used for main operations including the interrupt generation, reading ADC channels, and generation of PWM signals. Additionally, there are 10MHz and 3MHz clocks used for less demanding and smaller priority tasks, such as display refreshing.

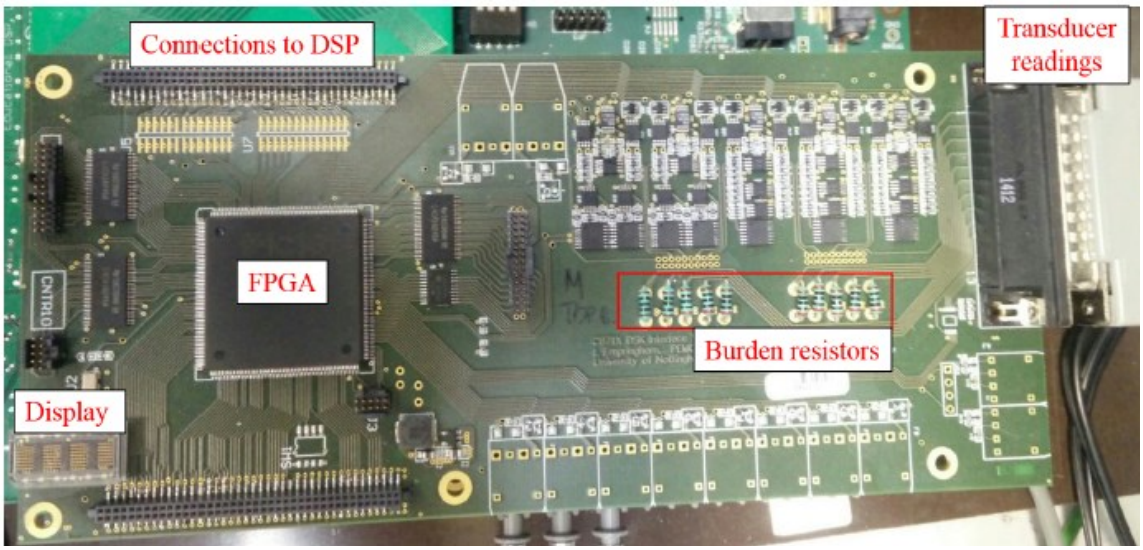


Fig. 5-22 The FPGA board

The LED display is implemented in the board and used to indicate the information about different operating modes of the board, such as PWM-enable, PWM-disable and trip source messages.The FPGA board features 10 ADC channels, and trip levels for all channels are configurable. i.e. when some of the measured signals reach the trip level a trip occurs and all PWM outputs are disabled. The DSP can write an information message about the trip on the LED display on the FPGA board. As the proposed MMPC is based on three PMs, the design requires the overall number of current and voltage measurements to be seventeen, two FPGA boards are required to be stacked.

The DSP-board (C6713 DSK) presented in Fig. 5-23, utilizes the high precision TMS320C6713 DSP. The board also includes a JTAG interface which enables the programming and debugging of the DSP via a USB port. The board is also equipped with a DSK6XXXHPI Daughter-card Educational DSP [124], which enables the downloading of the code through the HPI port of the DSK and also, a serial communication allows the PC-based GUI to perform real time monitoring of the different variables and measurements. A PC-based GUI for the HPI is also developed within the PEMC research group using Matlab® and it is capable of plotting the read variables and write to the DSP control variables.

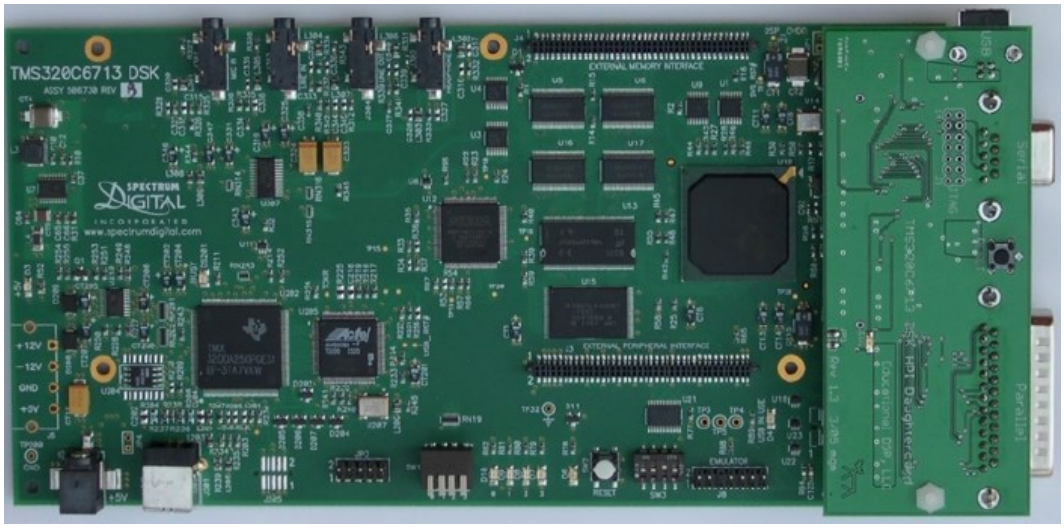


Fig. 5-23 DSP board with DSK6XXXHPI Daughter-card attached

The DSP board implements a 32-bit parallel communication link for the addressing and the data to access FPGA board's registers as an external memory. In order to make initial settings, the DSP board writes to the FPGA registers after reset. After that, the FPGA board produces periodical interrupt signals for the DSP, forcing the execution of an interrupt service routine on the DSP. During this routine the DSP reads the measured signals, processes the data and executes the control algorithms. At the end, the control outputs are passed from the DSP to the FPGA to be compared with the carriers in the FPGA to generate the PWM signals as demonstrated in Fig. 5-24.

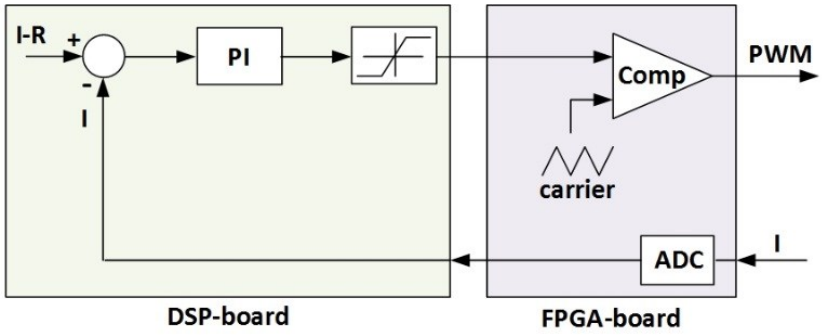


Fig. 5-24 interfacing between FPGA and DSP boards

5.5.1.4 Data acquisition

The data acquisition system has been made based on modular design, i.e. each PM is interfaced by a data acquisition board equipped with two current transducers for measuring PV and battery stages inductor current as well as three voltage transducers to measure the voltages of the PV-module, the battery module and the PM's output. Only one of the acquisition boards equipped with additional current transducer for measuring load current and a voltage transducer to

measure converter output as seen in Fig. 5-25. The outputs from the acquisition boards are combined and connected to the FPGA boards.

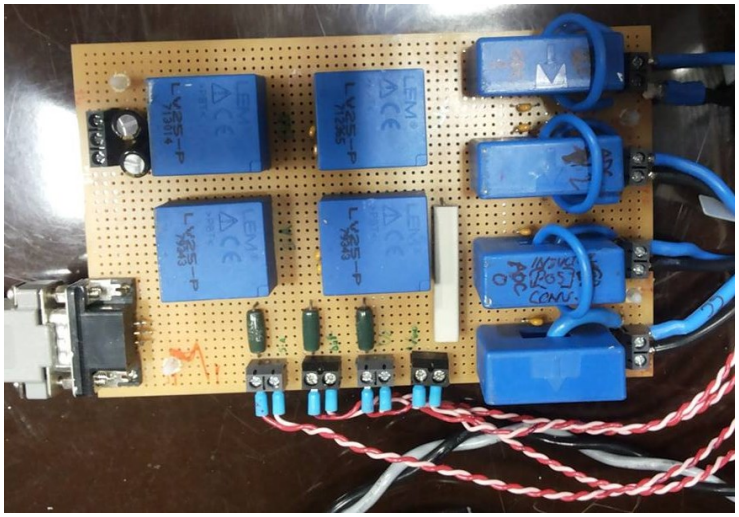


Fig. 5-25 Data acquisition board for a single PM

The implemented current and voltage transducers are both produced by LEM® and are based on a Hall Effect closed-loop current sensor to provide galvanic isolation [125, 126]. The operating principle is based on measuring the input current and provide an output current proportional to that current. Both current and voltage transducers require an external power supply with ±15V voltage with respect control platform's 0V potential.

The current transducer used is the LEM® (part number: LA 55-P), the application circuit of the transducer and its operating concept is shown in Fig. 5-26 . The measured current carrying wire should passed through the dedicated hole in the transducer with one or more turns. As the rated current of the transducer is 50A, the nominal current of all turns together should not exceed 50A. For the designed data acquisition board, the wire passed though transducers hole in two turns in order to increase the resolution and accuracy of the measurements as the currents to be measured are below 20A. The output current of the current transducer is in the range of ±50 mA, so a burden resistor is required to translate this current range to a voltage range of ±5V to suit the interfacing conditioning circuits and ADCs on the FPGA board. It selected to be 100Ω.

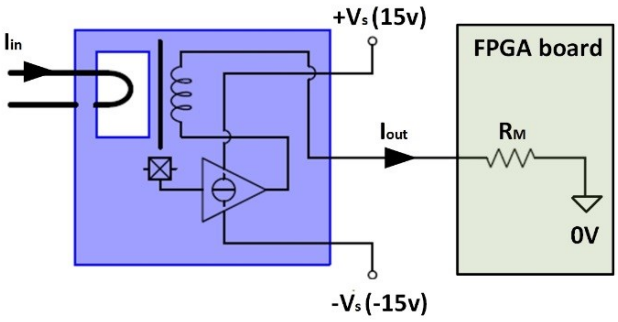


Fig. 5-26 Application circuit of the current transducer

The voltage transducer implemented for the voltage measurements is the LEM® (part number: LV 25-P), the operating principle of the transducer as mentioned previously is based on measuring input current and gives output current proportional to that current. Accordingly, an input resistor R_{in} is required to translate the applied measured voltage into an input current to the sensor as seen in the application circuit in Fig. 5-27. Selection of the input resistor R_{in} depends on both the voltage to be measured and the specified nominal input current for the transducer. For the designed data acquisition board, the input resistors for the voltages transducers measuring the voltages at power modules have been selected to be 5kΩ as the maximum voltages are below 50V in order to maintain high resolution and measurement accuracy. However, the voltage transducer for bus voltage measurement has been selected to be 12kΩ as the bus voltage could be above 100V. The output current of the voltage transducer selected is in range of ±24mA, so in order to transform this output current to a voltage ±5V, a burden resistor R_M is used at the FPGA board with value of 200Ω.

If the values of the burden resistor and input resistor of voltage transducers as well as the transfer ratio of transducer and ADC characteristics are known, then an approximated transfer function from the measured signal to the ADC output value can be obtained. However, this would be inaccurate due to the tolerances of the resistors and transducers. Therefore, precise

voltage and current sources are used to calibrate the transducers circuits. Accordingly, a relation between readings and the measured signals can be obtained. The calibration is made for all the transducers in the ranges of interest, a linear equation is derived that relates the actual measured values for voltage and current to the ADCs outputs values. The process of calibration needs to be carried out from time to time in order to correct for any change that may happen due to temperature variation or aging of the transducers.

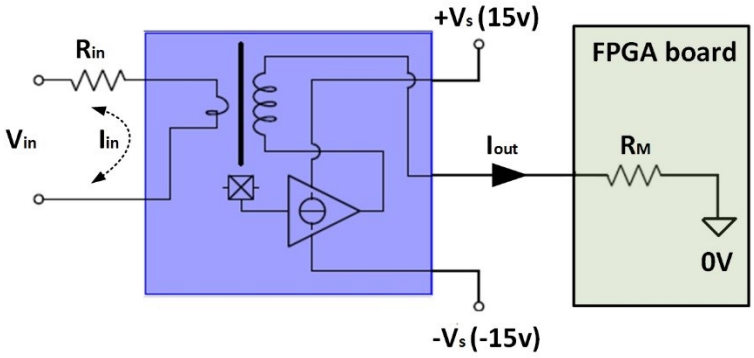


Fig. 5-27 Application circuit of the voltage transducer

5.5.2 Experimental results

5.5.2.1 MMPC Operation with unbalanced PV power

The first test which is shown in Fig. 5-28 , is made for battery charging and assumes balanced batteries (i.e the three battery-modules have the same SoC) whilst the power from the PV modules are unbalanced during a specific time which is similar to the simulated test in section 5.4.2 but with changing the power of two modules instead of one. Initially the three PV-sources provide nearly equal power (around 117W each) which results in an equal voltage contribution (around 25V) for all the PMs to the MMPC bus voltage (75V) and also in maintaining balanced charging powers (3x55W) for the battery modules. At t=10s, a disturbance has been introduced to the system by slightly reducing the load power by 5% as well as imposing an imbalance in

the PV powers (Ppv1=150W; Ppv2=117W; Ppv3=85W). Accordingly, if the module voltage contributions were kept the same, the imbalance in PV powers would cause a direct imbalance in the charging powers of the battery modules which in turn, would lead to a significant SoC imbalances. In order to minimize this, the proposed management algorithm allows the modules to contribute with imbalanced voltage/power to the bus voltage/load power in order to minimize the battery power imbalance which ultimately will provide minimum SoC imbalance. This can be seen during the time (10<t<19 s), where the voltage contribution of M1 with highest PV power has been increased from 25V to 35V to direct most of the increased PV power (117W→152W = +30%) to the bus/load. On the other hand, the voltage contribution of M3 with lowest PV available power (120W→85W= -30%) has been decreased to 17V (this is the minimum possible, equal to the PV voltage) to minimize the module power contribution to the bus, allowing for more power to charge the battery module (53W→42W= -20% instead of 37W). These imbalances in the voltage contributions of PMs is nearly compensating for the PV power imbalances, limiting the buildup of battery SoC divergence. Throughout the whole test, it can be seen that the control is able to maintain the bus voltage at 75V under all conditions, un-affected by the PV imbalance. These results are in line with results obtained through the similar simulated test in section 5.4.2 except for the disturbance introduced to the output voltage in the simulated test as can be seen in Fig. 5-16. This disturbance was caused by the large disturbance in the power of PV-module1 caused by its MPPT during its search for the new MPP in response to the step change in its irradiance. This disturbances could not be tested in the experimental setup due to the use of power supply, rather than a real PV of capable PV emulator, that does not emulate the real PV characteristics.

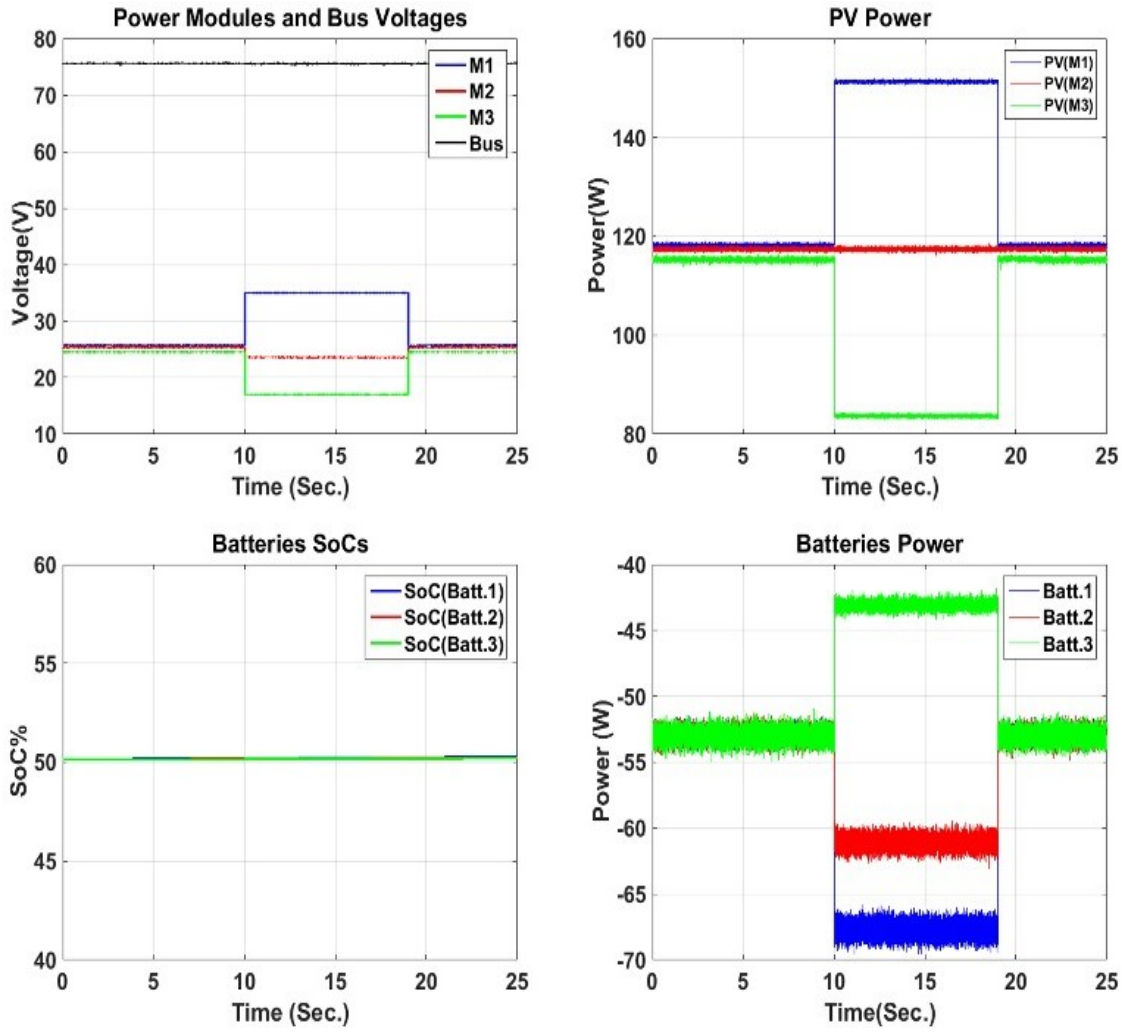


Fig. 5-28 Battery charge balancing with unbalanced PVs power

5.5.2.2 MMPC Operation with/without PV power

The second test shown in Fig. 5-29 evaluates the capability of the MMPC to maintain the bus voltage as well as balanced SoCs for the battery modules under the presence/absence of PVs power. Initially (t<10s), the power of all the PV-sources were almost the same (=118W) and all batteries were charging with the same power (=44W) to maintain balanced SoCs. At t=10s the PV-source of M3 was switched OFF. This forced the battery of M3 to switch from charging to discharging state in order to contribute power to the load requirement, which needs to be kept at

a minimum in order to limit the divergence of the battery module SoC. Therefore, the voltage contribution of M3 was set to the minimum (17V). To compensate for this, the voltage contributions of M1 and M2 are increased delivering more power to the bus/load and less power (44W ↓30W) to charge their batteries but keeping the bus voltage at the reference level (75V although a small dip is visible). When another PV-source (PV1) is switched OFF (t=12.5), the

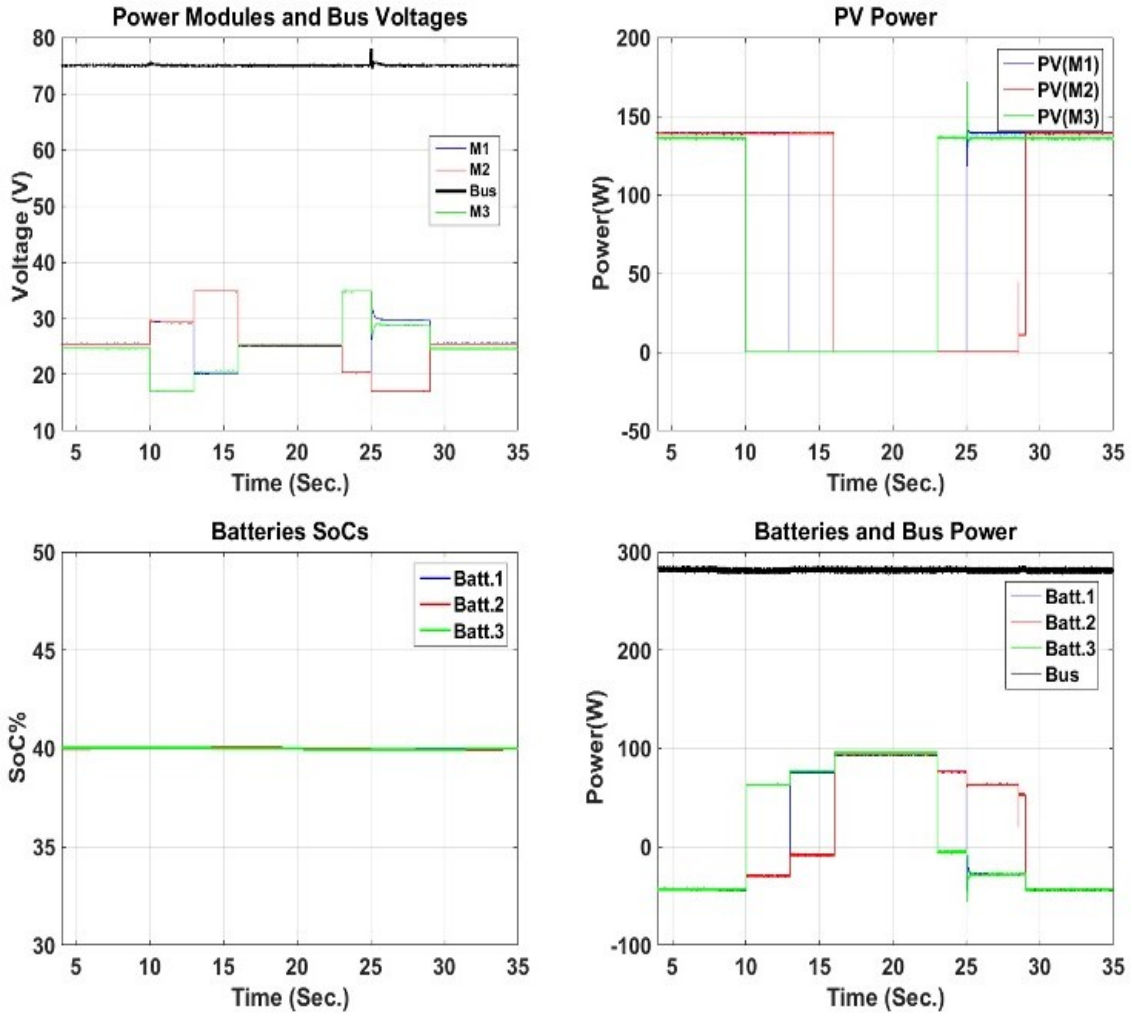


Fig. 5-29 Bus voltage control with/without PVs power

voltage contribution of M2 increases to the maximum (36V) to maximize its power share to the load and minimize the charging power of its battery module (30W ↓9W), allowing the modules without their PV source (M1 and M3) to minimize their power contribution to the load. The last PV-source (PV2) to be switched off is M2 at t=16s which means all the three battery modules

are discharging, therefore the voltage/power contributions of all the modules are the same, to have same discharge power and maintain balanced SoCs.

The second part of this test consisted of switching ON the PV sources in the same order. It can be seen that the voltage contribution of each module changes in a similar way as in the previous steps which is consistent with the aim of minimizing as much as possible the power imbalance of the batteries whilst delivering a constant bus voltage to the load.

5.5.2.3 MMPC Operation with unbalanced battery modules

The third test shown in Fig. 5-30, evaluates the capability of the MMPC to reduce the charge imbalance of the battery modules. As it requires a long time to obtain a noticeable change in the SoC of the battery modules when using their real capacity, the capacity used in the SoC estimator in this test is reduced by a factor of 10. The test starts with the following imbalance in the SoC of the battery modules 62% (M1), 52% (M2) and 42% (M3). In order to reduce this SoC imbalance, whilst the three PV sources provide balanced power (t<11s), the MMPC management strategy defines the voltage contribution of the PMs according to the SoC of their battery modules. M1 has contributed with the highest voltage to the bus (28V) according to its battery SoC, whilst M2 contributed with (25V) and M3 which has the lowest SoC, contributed with (21V). As a result, the charging power of M1 battery-module was the minimum (33W) whilst the charging power for M3 battery was the maximum (49.6W). The charging power of M3's battery was (40W).

At t=11s, a simulated step change in the irradiance has been applied to the PV-source of M1 that causes a power increase from 120W to 160W, whilst the PV power of M2 and M3 remain the same. In order to have the fastest reduction of battery imbalance, the voltage contribution of M1 increased to its maximum (36V) whilst the voltage contribution of M2 and M3 decreased to

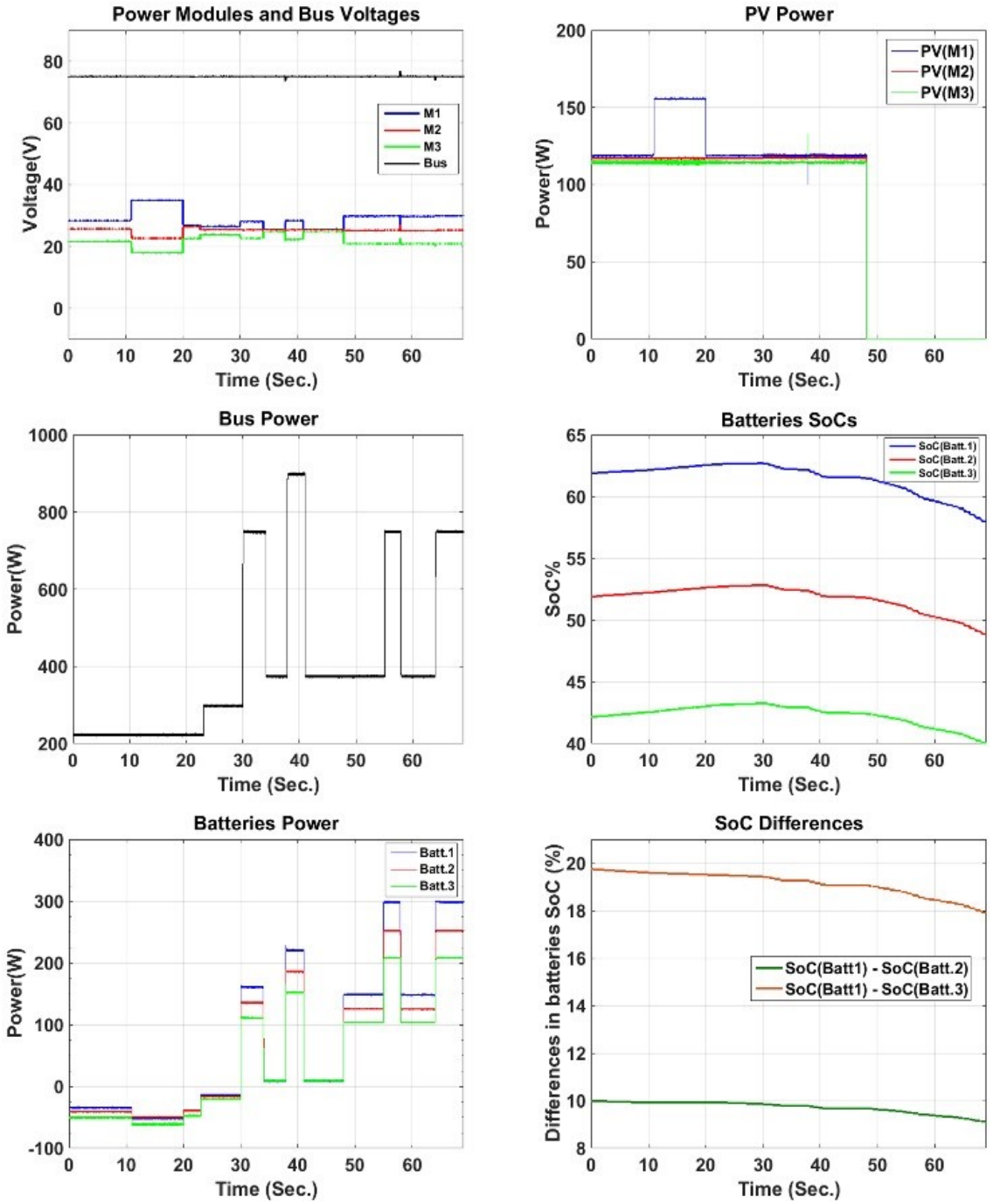


Fig. 5-30: Reduction of SoC imbalance of the battery modules under various conditions (PVs power imbalances, load power surges, no irradiance).

22.5V and to its minimum (17V) respectively. Most of the increase of the PV power of M1 was directed to the bus/load allowing M2 and M3 to decrease their power contribution to the

bus/load, which results in an increase of their battery charging powers: This will reduce the differences among the batteries SOCs. The test continues by having the load absorbing several power peak surges (600W and 900W at 32s<t<34s and 38s<t<41s), which requires power to be supplied by the batteries and PVs. Available PV powers are equal. To further reduce the SOC imbalance, the voltage contribution to the bus and the discharging power of M1's battery is larger compared to M2 and M3. The test concludes with a sudden reduction of the power of all three PVs (t=48s.).

It can be seen that the reduction of imbalance continues even when the PV power is absent. In order to facilitate a better observation of the imbalance reduction process, the difference in SoC between PM1-PM2 and PM1-PM3 is shown in Fig. 13e where a continuous decrease of the imbalance is obvious (20% to 18% and 10% to 9% respectively).

5.5.2.4 MMPC Operation with single module failure

The last test is shown in Fig. 5-31, where the operation of the MMPC for a single module failure was investigated. At t=12s, a failure has been imposed to the MMPC by disconnecting the PV-source and the battery of M3. As can be seen, the collapse of M3 voltage causes the MMPC to immediately respond by increasing the voltage contribution of M1 and M2 to the maximum level to compensate for the loss of the M3 and to attempt to maintain the bus voltage at the nominal value. However, as the maximum voltage contribution of the power modules is limited to the battery voltage (36V), the maximum reachable bus voltage is less than 72V, which is less than the specified value (75V). This means that if the system had consisted of a sufficient number of modules, or if the battery module rated voltage were slightly higher, it would have been possible to completely compensate for the loss of one module whilst maintaining the bus voltage at its specified value. Increased loading also had been applied (19s<t<23s) to verify the effect of this failure at different loads.

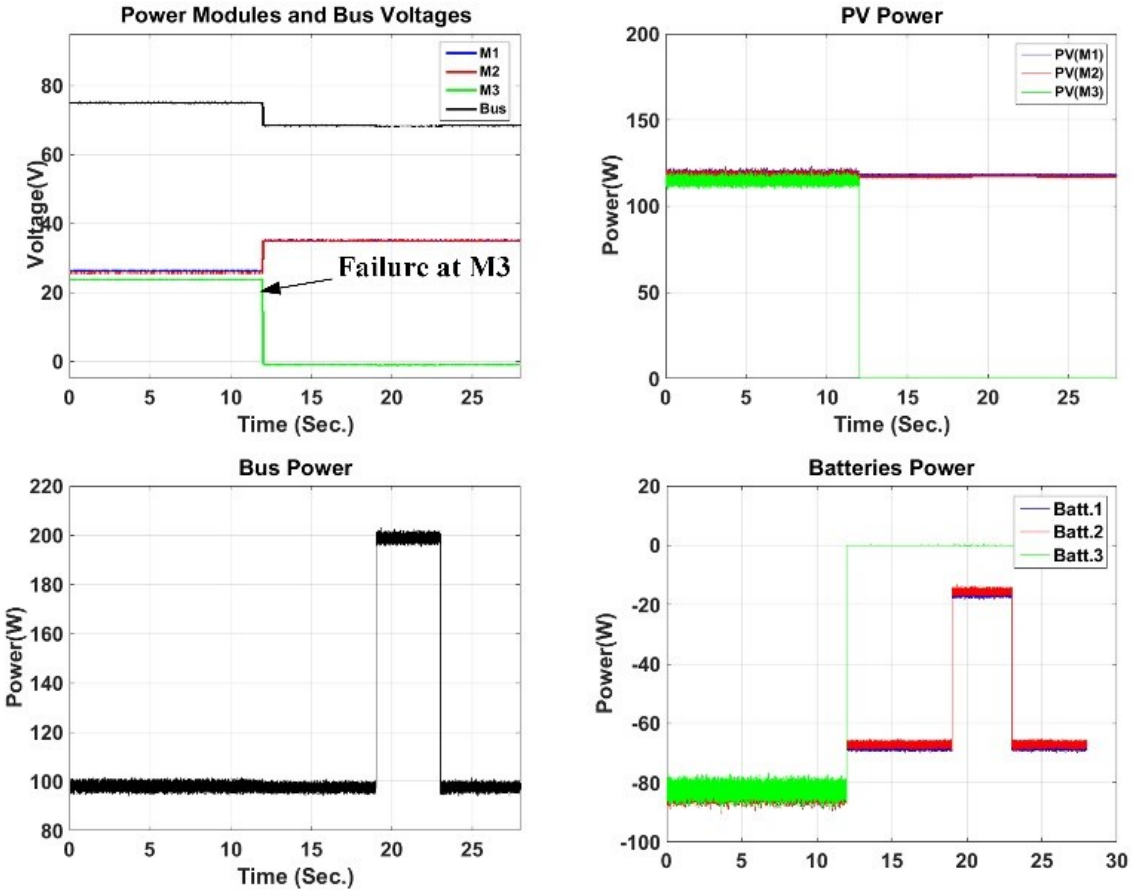


Fig. 5-31 Operation of the MMPC under partial failure

Summary

A new modular multiport converter for photovoltaic-battery based power systems has been proposed in this chapter. The proposed converter topology is based on a modular architecture. Compared to conventional centralized multiport converter, this solution is able to operate with a high degree of PV power imbalance whilst reducing/maintaining the battery SoC imbalance/balancing. It can also accommodate partial failure of a module. The converter topology operation and control are derived. The proposed converter has been prototyped at 75V/1kW based on three modules to validate the concept. The experimental results showed the performance of the proposed converter confirming the expected benefits including capability to achieve battery balancing whilst operating with PV power imbalance or with a module fault.

As a stepping stone, this study opens a new approach to using modular architectures of multiport converters to enable the use of low voltage/high current photovoltaic modules and battery modules to implement a high voltage power system bus instead of using high voltage strings made of a large number of series connected PV-modules and battery cells with the related known problems. Also, due to the low voltage levels, low voltage/high current power semiconductors can be used within the converter modules which may improve overall efficiency.

Chapter 6. Investigating Optimal Designs for the ESS

6.1 Introduction

In the previous chapters, the design of EPS considered was based on the load power profile considering a passive optical imaging payload. Recently, the use of an active imaging payloads like radar on-board micro-satellites platforms has been investigated in order to reduce the cost and as improve the performance of observation systems in terms of revisit and response time [3]. This application is posing more challenges for the design of the EPS as it should fulfil the power requirements of these kinds of payloads that required high power (with short duration) under the restricted weight and volume budget available in this kind of satellites.

In this chapter, the design of the power system to fulfil the typical power requirements for radar imaging payloads, as an example of these kinds of loads that require high power peaks will be investigated. Also, the design of an energy storage system (ESS) based on different battery chemistries and supercapacitors will be evaluated considering the resulted overall weight of the ESS and the thermal stress of the energy storage devices for each potential design.

6.2 Re-sizing of power system

In Chapter 3, the power system has been sized considering the specific micro-satellites platform with passive optical imaging payload in LEO orbit which is subject to a 65 minutes sun-duration and 35 minutes eclipse. For this platform, the continuous power consumed by satellite housekeeping electronics was 50W. Each orbit, the communication system consumes additional 50W for a duration of 10 minutes as shown in Fig.6-1. According to this power profile, the PV

array has been sized in based on (3-29)-(3-32) to be rated at 125W which is considering 90% efficiency for the interfacing power regulator (PR) and 25% oversizing to compensate for performance degradation of the array near end of life (EoL).

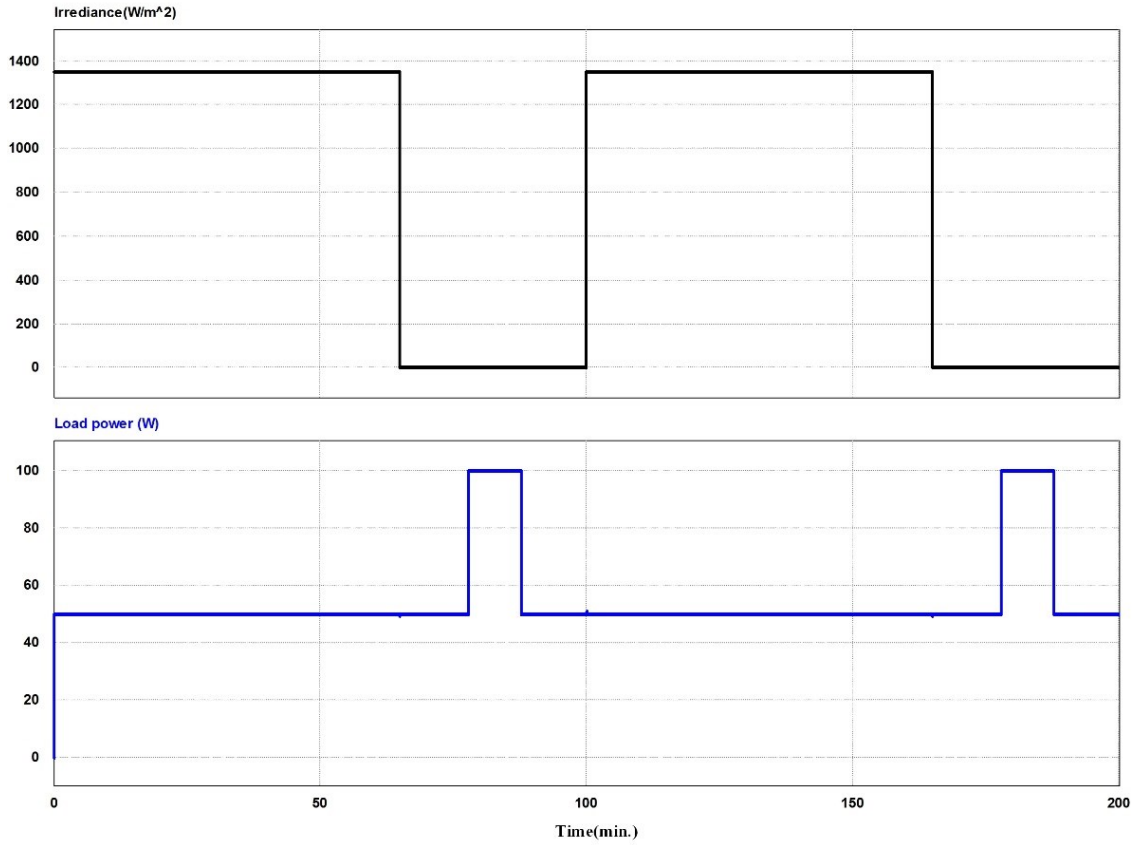


Fig.6-1: Power consumption profile of the satellite subsystems over two orbits

For the same class of small satellites that require power peak pulse for the radar imaging payload, the power consumption of satellite housekeeping electronics is assumed to be the same (50W) as in the previous situation and also the power consumption for communication system remains the same (50W) for the duration of 10 minutes each orbit. However, a 1kW power pulse has been added to this power consumptions profile as required by the radar imaging payload which is active for approximately one minute each orbit as proposed in [3] [37] and the resulted profile is shown in Fig.3-40. Accordingly, the PV array and battery pack need to be resized in order to fulfil the new power consumption profile that is also summarized in Table 6-1.

Table 6-1: Details of the power consumption of the different subsystems during one-orbit

Subsystems	Power consumption(W)	Duration(min.)	Energy (Wh)
Housekeeping	50	100	84
Communication	50	10	9
Radar imaging	1000	1	17

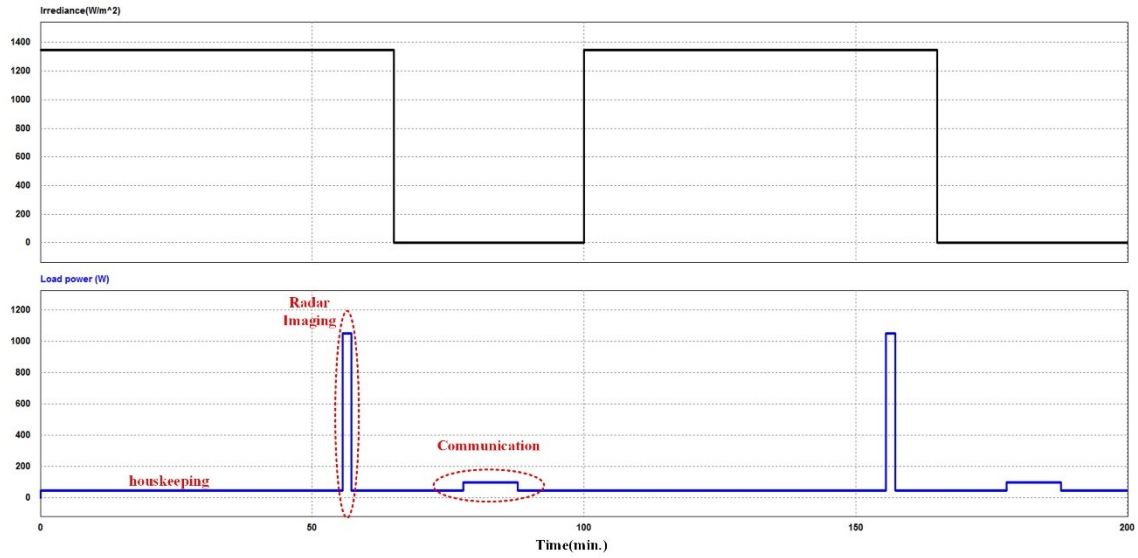


Fig.6-2: Power profile of the radar imaging satellite over two orbits

6.2.1 Resizing of PV array

According to the energy consumption of the different subsystems described in Table 6-1, and in order to keep the energy balance within the orbit, the generated power from PV array should satisfy:

$$P_{S.A} \geq \frac{E_h + E_{com} + E_R}{\eta_{PR}\, t_{sun}} \tag{6-1}$$

where t_{sun} is the sun-duration of the orbit, η_{PR} is the efficiency of PV-panels' power regulators, E_h, E_{com} and E_R are the required energy over one orbit when supplying the power for

housekeeping electronics , communication system and radar payload respectively, whilst the point of load (PoL) converters have been assumed with very high efficiency (≈1).

According to (6-1), and by considering 90% efficiency for power regulators interfacing the PV-panels, the PV array should be sized to deliver 123W during the sun-duration in order to fulfil the energy requirements for this platform. When a 25% over size to compensate of the performance degradation of the PV array is considered, the PV array should be sized at ≈145W in total with 16% increase in the size of the PV array compared to same satellite platform with optical imaging payload.

Considering the rigid-honeycomb construction for the PV panels with the utilization of triple junction solar cells, the specific power of the PV array that can be achieved in satellite applications is 50-70W/kg [38, 127, 128]. Accordingly, the overall weight of the required PV array in the microsatellite platform with optical imaging payload is 2.05 kg, whilst the overall weight of the PV array for the same satellite platform but with a radar imaging payload is 2.4kg with an increase of 0.4kg (20%) in the weight of the PV array.

6.2.2 Resizing of battery pack

In Chapter 3, the minimum size battery pack required to handle eclipse duration has been sized at 217 Wh which is assumed to be 90% efficiency for the interfacing battery discharge regulator (BDR) and considering 20% depth of discharge (DoD) for the battery in order to achieve an extended lifetime as recommended by manufacturers [61]. When considering the radar imaging payload, the minimum nominal energy size of the battery pack has to be resized to satisfy:

$$Battery\ cap.(Wh) \geq \frac{E_{h-eclp} + E_{com} + E_R}{\eta_{dis} DoD} \tag{6-2}$$

Where $E_{h\text{-}eclp}$ is the energy required to supply housekeeping electronics power during eclipse, E_R is the energy required for supplying the radar imaging payload power and η_{dis} is the conversion efficiency of BDR. The energy requirements from the battery pack during eclipse are detailed in Table 6-2. Accordingly, by considering 90% efficiency for the BDR and 20% DoD for the battery, the minimum rated energy capacity of the battery should be 312Wh.

Table 6-2: Details of the power consumption of the different subsystems during eclipse over one-orbit

Sub-system	Power consumption(W)	Duration(min.)/orbit	Energy(Wh)
Housekeeping	50	35	30
Communication	50	10	9
Radar imaging	1000	1	17

It can be observed that the required energy size of the battery pack has been increased by 43.5% compared to the same satellite platform with optical imaging payload and this is a direct implication of the extra energy needed (+17Wh) compared to the previous case (39Wh) .

It should be noted that, during the radar imaging duration, the discharging rate of the battery pack will be quite significant (more than 3.5C) where C is the capacity current (Ah) of the chosen battery pack. Based on the properties of the chemistry of the utilized battery cells, this discharging rate might be inadequate and shorten the lifetime, especially for those batteries with high specific energy, as this aspect will be investigated in more details in the following sections. Therefore, additional over sizing for the battery pack may be required in order to lower the discharging rate to an acceptable level according to the capability of the selected battery cell chemistry and specified discharging rate.

6.3 Designing the ESS based on Li-ion batteries

Lithium ion (Li-ion) batteries have been used extensively as an energy storage device in satellite energy storage systems (ESS) since the first successful in-orbit demonstration in 2001 on Proba-1 satellite mission, as a replacement for the Nickle-cadmium and Nickle-metal hybrid batteries that were commonly used. Li-ion batteries that provide better characteristics compare to other energy storage devices, are available with different chemistries and exhibit different performance/characteristics that may suit different application requirements as can be seen in Fig.6-3. The Lithium Nickel Cobalt Aluminium Oxide $LiNiCoAlO_2$ (NCA) battery has found relatively widespread commercial use due to its highest specific energy (250Wh/kg) compared to other chemistries [39] and therefore can be considered an energy battery (EB). The problem with these EB is that the maximum discharging rate is limited to 1-1.5C [39]. Other chemistries can support significantly higher discharging rates of up to 30C like the $LiFePO_4$ (LFP) or $Li_4Ti_5O_{12}$, and for this reason these are referred to as power batteries (PB). The problem with these PB is that these have significantly lower specific energy, typically 90-120Wh/kg for LFP batteries [129] and 50-80Wh/kg for LTO batteries [130].

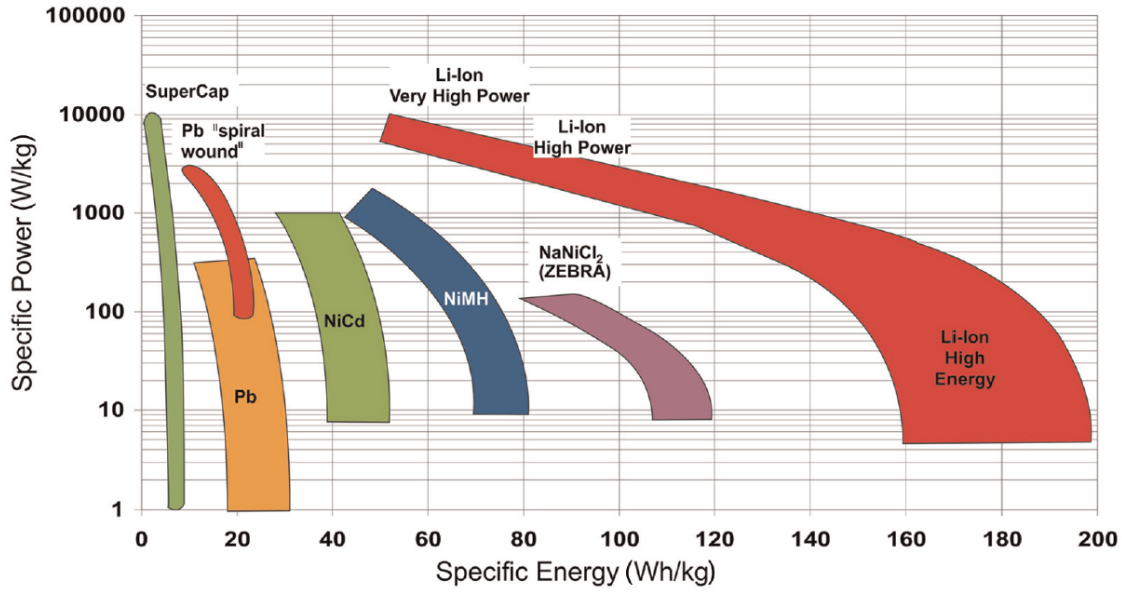


Fig.6-3: Ragone plot of various battery technologies with specification at cell level [131]

Accordingly, selecting the most suitable battery for an application is driven by minimising the ESS weight as this influenced by the energy requirement of the application and the battery specific energy (Wh/kg) in one hand and by the power requirement of the application and the discharging power capability and the battery's specific power (W/kg) in the other hand. These aspects will be investigated in the following subsections.

6.3.1 Designing the ESS based on Li-ion energy battery cells

Considering EB cells like the NCA as the chosen energy storage device for ESS, the maximum discharging rate for this cell for a duration of (>30s) should not exceed 1.5C as recommended by the manufacturer [39]. The limitation in the discharging rate of these batteries may be due to the higher internal resistance compared to power batteries. Fig.6-4 shows the internal resistance for one of the NCA battery cells (Panasonic NCR18650B) which has been measured through an electrochemical impedance spectroscopy (EIS) test using the Bio-Logic SP-150 Potentiostat described in section 3.1.5 in Chapter 3.

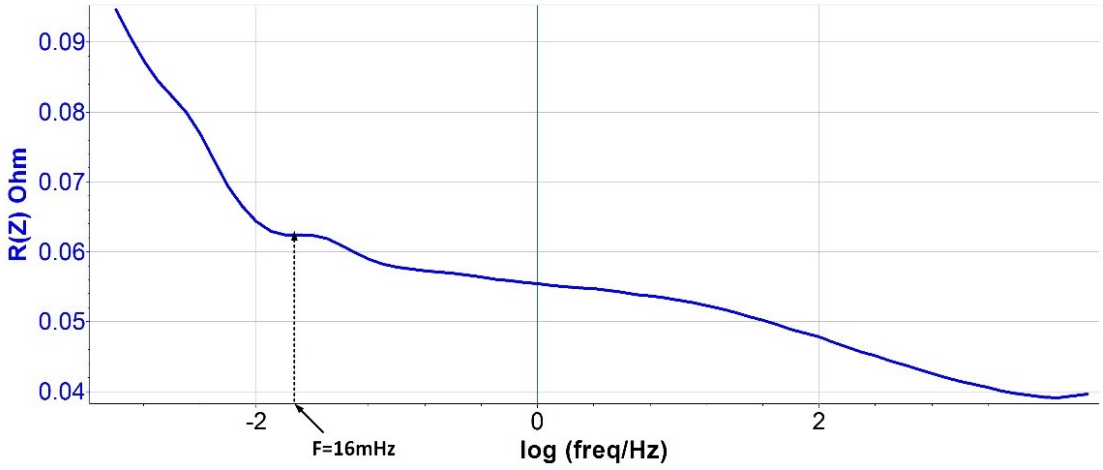


Fig.6-4: EIS test based measurement of battery internal resistance for a Panasonic NCR18650B cell used to derive the equivalent model as defined in Chapter 3 (section 3.1.5)

As it can be seen, the internal resistance at a discharging pulse for a duration of 60s (that corresponding to frequency of 16mHz) is ≈62mΩ. This battery cell has an energy capacity of 12Wh with nominal voltage of 3.6V and capacity of 3.34Ah. According to the energy requirements, the battery pack should consist of 26 cells in order to provide the required overall capacity of 312Wh.

Based on this design, during the radar imaging pulse (Δt=60s), the battery discharging current would be ≈11.8A resulting in high power loss inside each of the battery cells which in turn increases the internal temperature of the cells significantly, accelerating the degradation of the cells which will further increase the internal resistance and may cause at some point a thermal runway. In order to quantify and simulate the power loss and thermal stress at the cell level, the power profile has been rescaled down to a single cell level (26:1) to estimate the power exchange and the power loss of each battery cell. Battery cell power loss are estimated based on the developed model for the battery cell in in Chapter 3 (section 3.1.5). The thermal model used (shown in Fig.6-5.) is based on the simplified modelling methodology proposed in [132] which is similar to the method used for SC-cell thermal modelling described in Chapter 3 (section 3.2.2). However, better estimation for the internal temperature could be achieved through the using of thermocouple inserted inside the cell. The thermal model parameters used are identified for the A123 Systems ANR26650M1-B battery cell based on the measurements performed on the same cell presented in [133]. However, due to the non-availability of similar measurements for the Panasonic NCR18650B battery cell, the same thermal model will be used for both cells, the Panasonic NCR18650B and A123 system ANR26650M1-B. This may result in estimation errors for cell temperatures of the Panasonic NCR18650B due to the different materials and size (diameter of 18mm and length of 65mm) compared to the modelled cell (diameter of 26mm and length of 65mm). The smaller size may result in lower thermal capacity compared to the model cell, and consequently the estimated temperatures are expected to be lower than the real

temperatures. Therefore, this errors should be taken into account when comparing the thermal stress of this cells under different design option of the ESS.

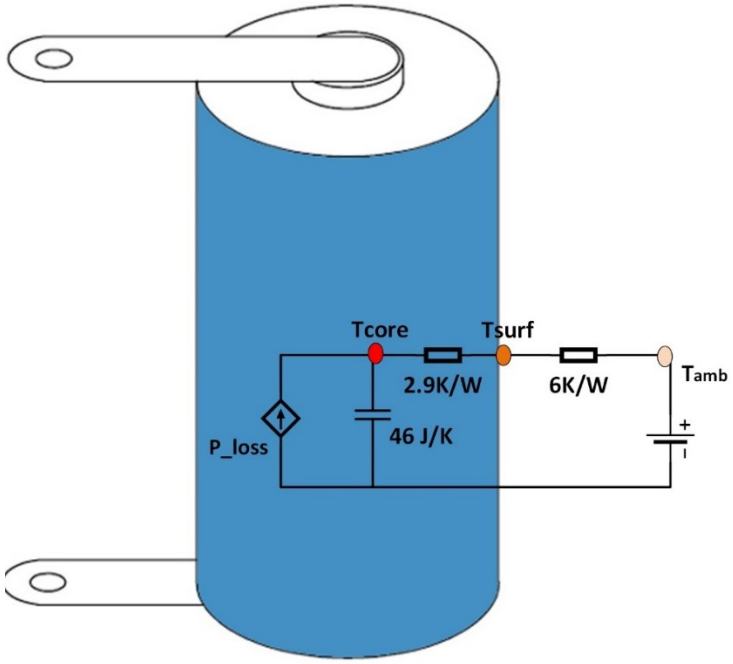


Fig.6-5: Simplified thermal model with identified parameters for 26650 cylindrical battery cell

Considering the corresponding power profile of a single cell, the power loss and the thermal stress for the cell are simulated as shown in Fig.6-6 using the described models. It can be seen that during the eclipse period, under the low power consumed by the housekeeping electronics (50W), the power contribution of the single cell was small (1.92W) and consequently the power loss inside the cell was negligible causing its temperature to remain fairly unchanged. However, during the high power peak (1kW) caused by the radar imaging payload, the power contribution of each battery cell increased to 42W which caused the power loss of the cell to increase significantly. At the first, instant the power loss of the cell was 7.5W which corresponding to the cell current at this moment (11.8A) and the ESR at 1Hz (corresponding to the sample time of 1s) which is 55mΩ. As the time increases, the voltage drop across the RC branches of the ESR model (3rd order ECM developed in Chapter 3 (section 3.1.5)) increases causing more

power loss and reduce the cell voltage which in turn increase the cell current (due to the constant power loading) which again increase the loss till reach 17.5W at the end of the peak. This resulted in an increase in the core temperature of cell (Tcore) to 43ºC and surface temperature (Tsurf) to 37ºC whilst the test assumes normal ground conditions (1bar) and an ambient temperature of 25ºC. The thermal stress may further increase when the battery cells experience aging/degradation which increase the internal impedance accelerating the degradation.

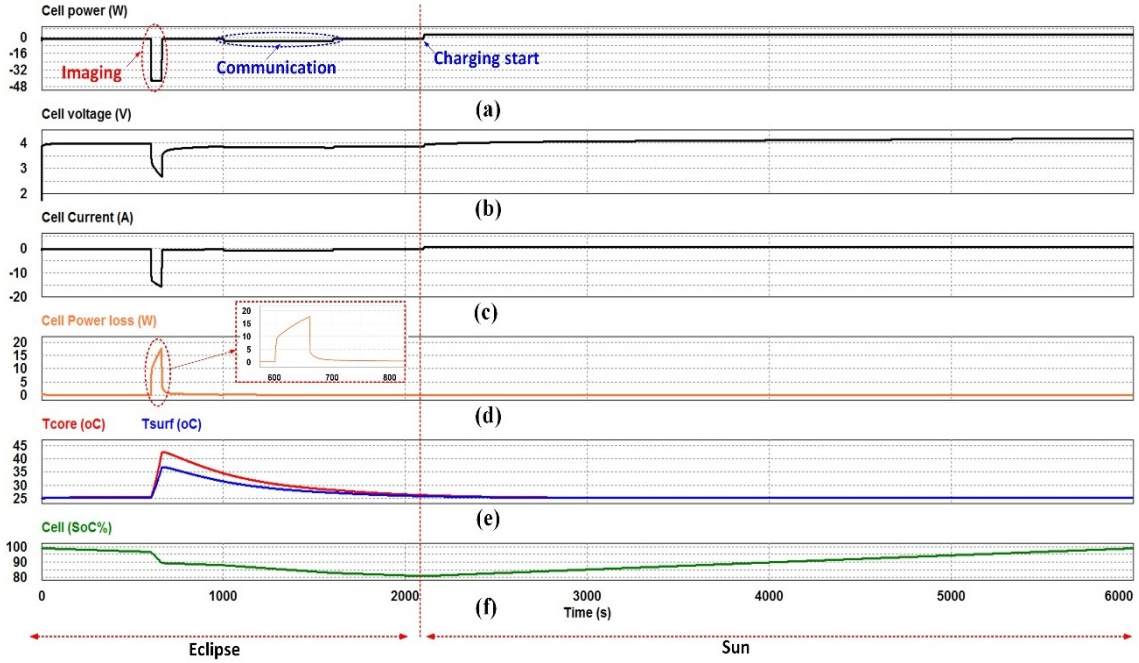


Fig.6-6: Simulated performance of the Panasonic NCR18650B cell in normal ground conditions under proposed load power profile over one orbit : (a) cell power (b) cell voltage (c) cell current (d) cell power loss (e) cell surface and core temperatures (f) cell state of charge

Although the utilization of the EB cells with high specific energy (250Wh/kg) can minimize the weight of the required battery capacity (312Wh) to 1.25kg, the battery cells would be significantly stressed during the peak power consumed by the radar imaging payload. Therefore, in order to ensure the safe operation of the battery cells and to guarantee the specified lifetime,

the battery pack needs to be oversized in order to limit the discharging rate. Accordingly, to limit the discharging rate of the battery cell to 1C to minimize the thermal stress, the battery pack needs to be oversized to 1.1kWh which results in an overall weight of the battery cells to be 4.5 kg and this is excluding the weight of the packaging support which can be 20% of the total cells weight [134]. Accordingly, the overall weight of the oversized battery pack including the mechanical support would be 5.6kg. Of course, the packaging support might be reduced significantly below this value due to the recent advances in material science, but this has a minor effect on the proposed comparison between the different designs of the ESS as long as the same percentage is used for all designs.

6.3.2 Designing the ESS based on power battery cells

By considering PBs (like the LFP battery cells) as energy storage devices for the satellite ESS, the maximum discharge rate for these battery cells is very high (up to 20C), however these batteries have lower specific energy (100Wh/kg) [129]. Accordingly, sizing the battery pack should be made based on the overall required energy during eclipse (312Wh) considering 20% DoD and 90% efficiency for the interfacing BCDR. The battery cell considered is the A123 Systems ANR26650M1-B has 2.5Ah capacity, 3.3V nominal voltage and energy capacity of 8.25Wh. During the radar imaging duration (60s), the battery discharging rate will be in range of 3.6C which is below the recommended maximum discharge rate (20C) by the manufacturer [129]. The expected power loss inside the cell is small due to the small internal resistance of this battery cell as seen in Fig.6-7. The total number of battery cells under this design required to provide the energy during eclipse is 37-cells. Accordingly, in order to simulate the operation a single battery cell over one-orbit stress, the power profile should be scaled down to a single cell level by a factor of (37:1). The simulated cell power contribution, voltage, current and thermal behaviour over one- orbit are based on the developed electrical and thermal models described

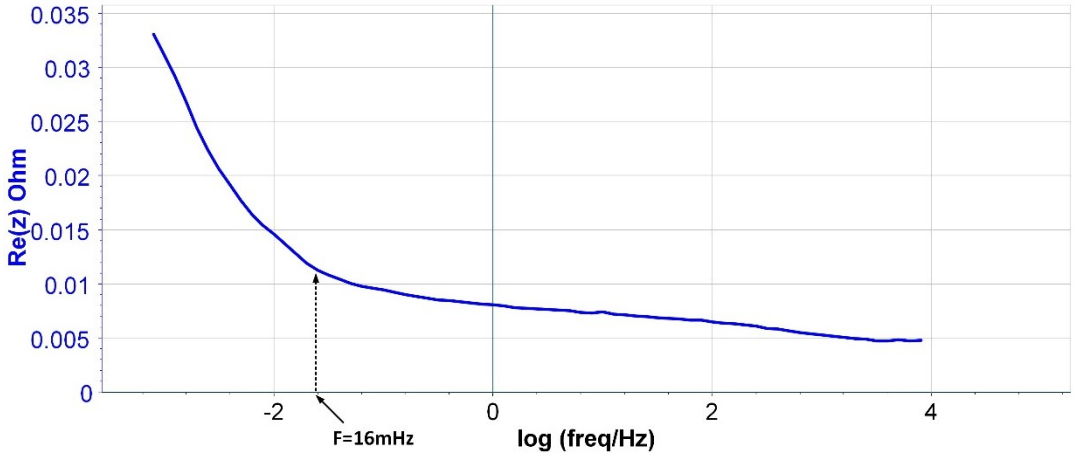


Fig.6-7: EIS test based measurement of battery internal resistance for a A123 ANR26650M1-B cell used to derive the equivalent model as defined in Chapter 3 (section 3.1.5)

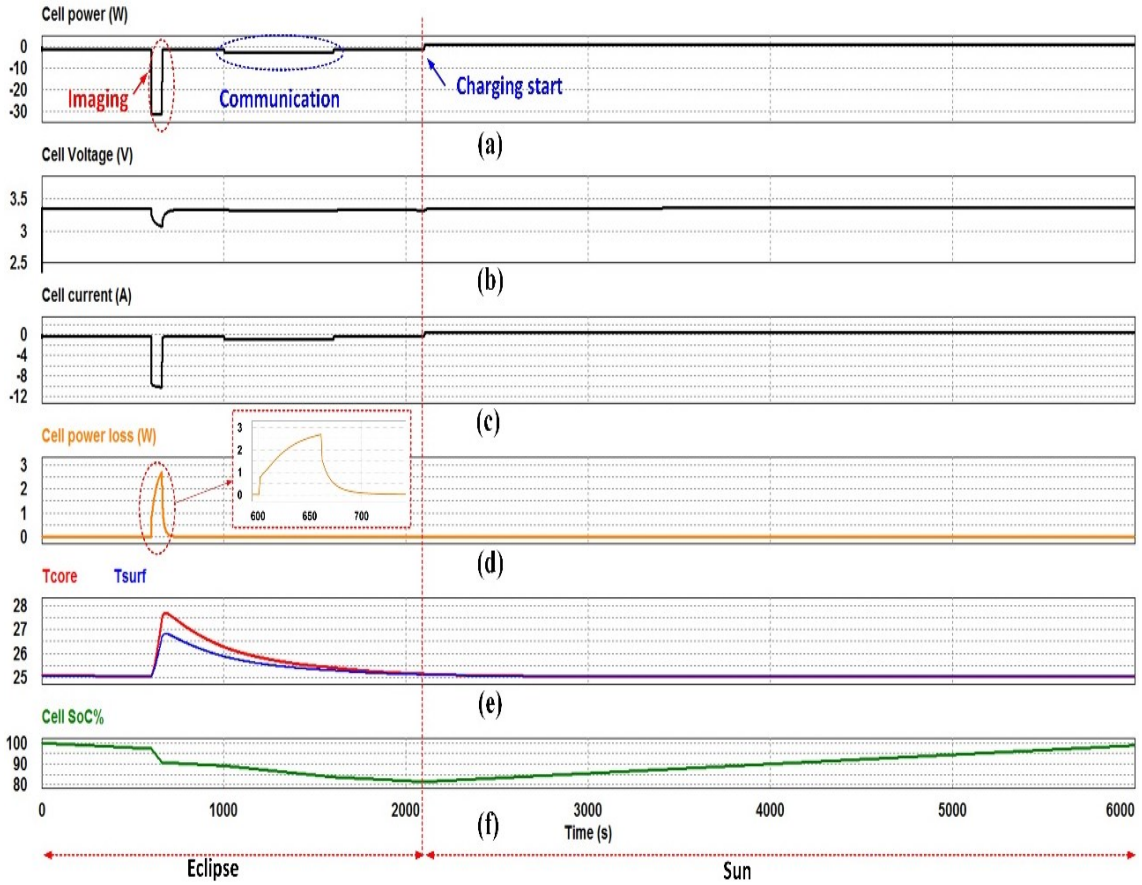


Fig.6-8: Simulated performance of A123systems (ANR26650M1-B) cell in normal ground conditions proposed a radar type microsatellite load power profile over one orbit: (a) cell power (b) cell voltage (c) cell current (d) cell power loss (e) cell surface and core temperatures (f) cell state of charge.

earlier under testing ground conditions (1bar and 25°C) and the simulation results are shown in Fig.6-8. It can be seen that the thermal stress for the battery cell under this PB cell design has been significantly reduced compared to EB cell and the cell temperatures increased by only 3°C. However, based on the results of the experimental testing and investigations done for this specific battery cell (ANR26650M1-B) to characterize the degradations and aging mechanisms[135-137], a maximum DoD of 10% should be considered in order to be able to extend the life time of the battery up to >29000 load cycles required during 5 years of on-orbit life operation. Accordingly the size of the battery pack capacity should be increased to 634Wh which results in an overall weight of the battery cells of 6.34kg and of the battery pack of 7.6kg that is including the packaging support. Due to the need to oversize the battery pack to reduce the DoD, the power contribution of each cell has been reduced to half and this allows a significant reduction of the power loss and thermal stress of the cell as it can be seen in the simulation results for cell voltage, current, power contribution, power losses and temperatures shown in Fig.6-9.

It can be observed that, although the utilization of the PB with higher discharging rate capability removed the need for oversizing (in terms of power) the battery pack to avoid stresses during the peak power loading, the lower specific energy of these batteries resulted in a heaver design (7.6kg) compared to the EB based ESS (5.6kg) with the same lifetime.

6.3.3 Designing the ESS based on hybridization of energy & power battery cells

A hybrid energy storage system that combines both EB and PB can be considered in order to combine the benefits of high specific energy of EBs and the high specific power of PBs. This concept had been suggested in [4] by implementing two battery packs. One utilizes Li-ion cells with high specific energy to supply the continuous loads (significantly lower power level but

longer duration) during the eclipse, whilst the other battery pack utilizes Li-ion (PB) cells to supplies the required high power peak for the radar imaging payload. By considering this concept, the first battery pack (will be referred as energy pack (EP)) should be sized based on the energy requirements for satellite housekeeping electronics as well as communication subsystem during eclipse (39Wh). Accordingly, the rated energy capacity of this pack should be (≈217Wh) which is accounting for a 90% efficiency for the interfacing BCDR and 20% DoD for the battery. As this pack utilizes EB cells with high specific energy (250Wh/kg), the overall weight of the battery cells will be 0.86kg and the predicted overall weight including packaging support will be 1.1kg. Considering the use of the Panasonic (NCR18650B) cell with 12Wh energy capacity, this pack will consist of 18-cells.

The second battery pack (will be referred as power pack (PP)) should be designed based on the energy requirement for the radar imaging operation over an orbit (≈17Wh). Accordingly, the capacity of this pack should be ≈190Wh considering 90% efficiency for the interfacing BCDR and 10% DoD for the battery. As this pack utilizes PB cells with lower specific energy (≈100Wh/kg), the overall weight of the battery cells will be 1.9kg and the predicted overall weight of the pack including packaging would be 2.38kg. Considering the use of the A123systems (ANR26650M1-B) cell with 8.25Wh energy capacity, this pack will consist of 23-cells. The simulated performance of the hybrid implementation using the two battery cells (EB and PB) is shown in Fig.6-10. This shows the situation of two single cells (one from each pack) by resizing the power profile of the whole 18 cells EB pack by a scaling factor of 18:1 and by resizing the power profile of the 23-cell PB pack by scaling factor of 23:1. It can be seen that the thermal stress of the EB cell (Panasonic NCR18650B) is very small even at its maximum discharging power during the communication session. However, the PB cell (ANR26650M1-B) was subjected to noticeable (although small) thermal stress during the imaging period that increased the cell temperature by 7^{o}C. The reason is that this pack has been sized to supply the required energy for the power intensive radar imaging payload only which resulted in relatively

lower capacity for the required discharging power which led to a high current rate of 5.9C as a result. The thermal stress may be increase as it cycled due to increase the internal ESR that can reach 150% compared to the initial ESR after 1000 cycles depending on cycling conditions as described in [138, 139].

The estimated overall weight of the hybrid battery system based on the hybridization of energy/power battery cells is 3.46 kg.

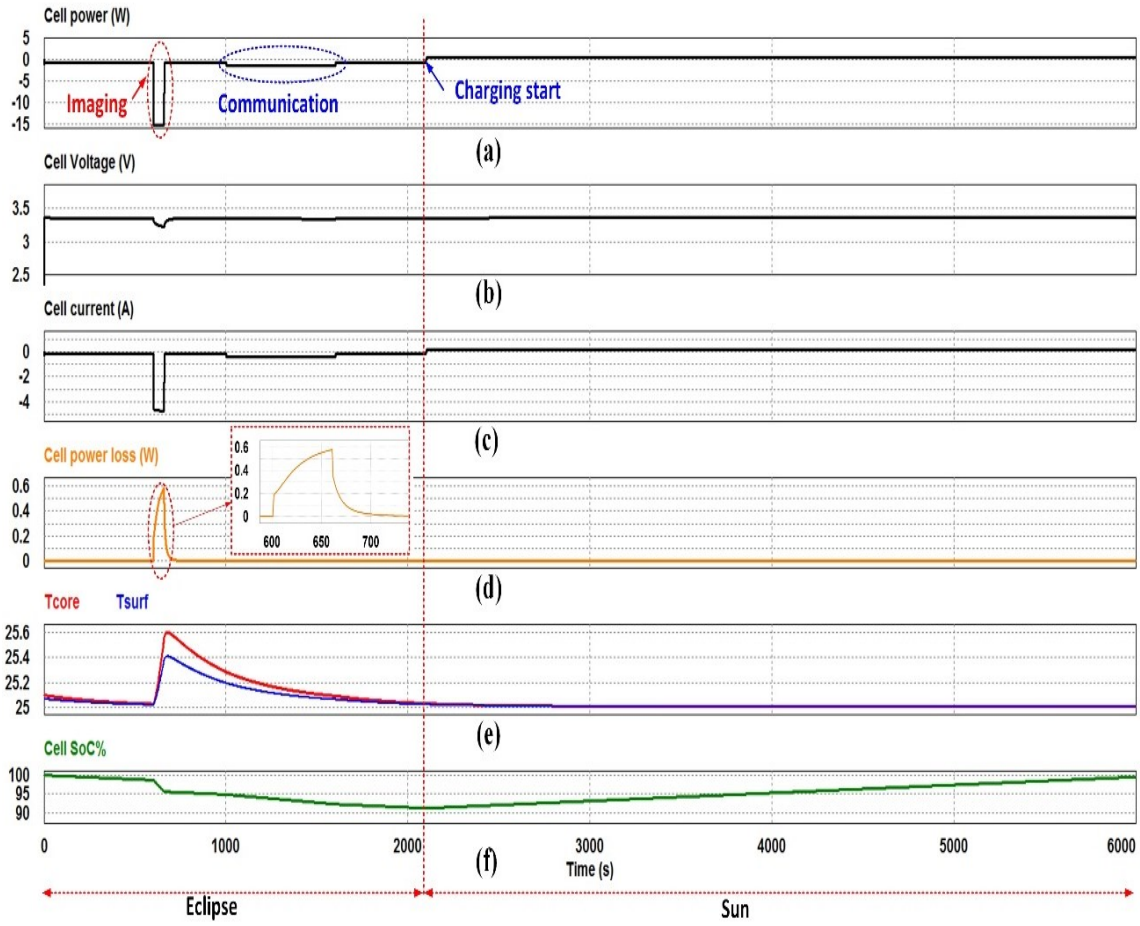


Fig.6-9: Simulated performance of ANR26650M1-B single cell behaviour in an oversized ESS in normal ground conditions under proposed load power profile over one orbit: (a) cell power (b) cell voltage (c) cell current (d) cell power loss (e) cell surface and core temperatures (f) cell state of charge

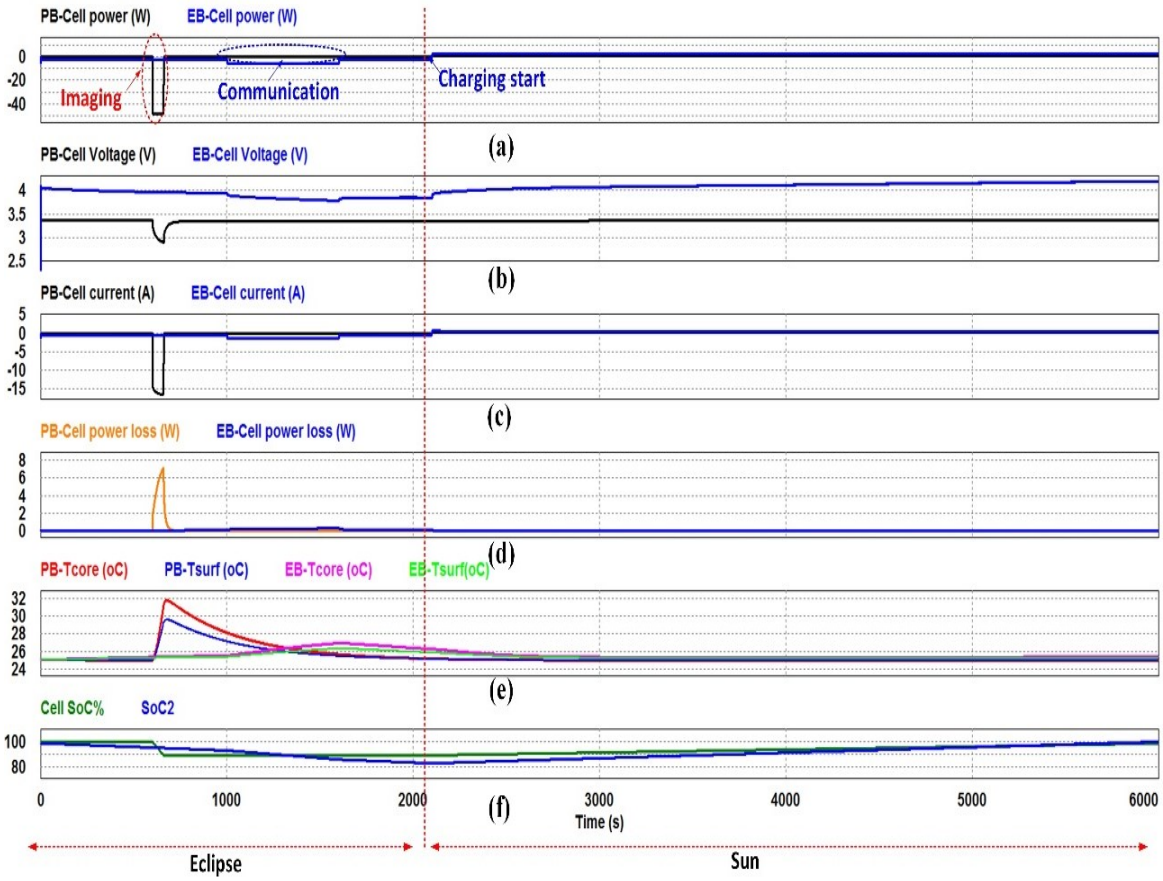


Fig.6-10: Simulated performance of the PB and EB cells in the hybrid ESS in normal ground conditions under proposed load power profile over one orbit: (a) PB/EB cells power (b) PB/EB cells voltage (c) PB/EB cells current (d) PB/EB cells power loss (e) PB/EB cells surface and core temperatures (f) PB/EB cells state of charge

6.4 Designing of the ESS based on LIC

The use of the lithium-ion capacitor (LIC) in satellite ESS has been investigated in [140] as an alternative for the lithium-ion battery (LIB) due to the LIC ability to provide long life cycling at higher DoD (>80%) compared to the LIB which requires shallow DoD (<30%) and therefore significant oversizing in order to extend its lifetime (>30000 cycle) as required by a 5-years in-orbit operation of the satellite. Accordingly, the net specific energy of the storage element (LIC or LIB) can be defined based on the targeted DoD as [140]:

$$Net\ specifc\ energy = specific\ energy * DoD \quad (6\text{-}3)$$

As a result, when considering EB cells with a rated specific energy of 250Wh/kg but used at 20% DoD as described earlier, the resulting net specific energy of this battery will be only 50Wh/kg. On the other hand, the specific energy of commercially available LICs are in range of 8-13 Wh/kg [141] which in turns gives a net specific energy of up to 10Wh/kg considering 80% DoD. This means that although the rated specific energy of the EB cells is nearly 20 times higher compared to the LIC cells, an ESS system based on LIC will be only 5 times heaver compared to the ESS based on Li-Ion EB cells. Also, due to the high specific power of the LIC, it can supply the high power peak required for the radar imaging payload, so the LIC stack does not need to be oversized to be able to supply these power peaks.

The device temperature and DoD are strongly affecting the degradation of the LIC cells as investigated in [142]. Consequently, these two parameters should be considered when sizing the LIC based ESS. According to the results obtained from the long cycling tests in [142], the LIC cell may lose 5-10% of its initial capacity after 10,000 operating cycles under 80% DoD and an operating temperature range of 25-30^{o}C. Further capacity fade has been predicted to reach 15-20% of its initial value after 30,000 cycles considering the same operating conditions (temperature and DoD) [142]. Also, significant accelerated capacity fading has been observed at higher operating temperatures (45-60^{o}C) where LIC cells lost 15-20% of initial capacity after the first 10,000 cycles even though the lower charge-discharges current used in the cycling tests that means more capacity fade might be expected due to the higher discharging current during radar imaging period. However, these reported values will be considered as a minimum capacity fade that can occur under the given load power due to the lack of cycling test measurements under this specific load profile. According to these degradation measurements, it is essential to ensure a maximum DoD of 80% when designing the ESS for satellite EPS based on LIC, assuming a controlled surrounding temperature of 25^{o}C, in order to achieve a minimum

capacity retention of 80% after the targeted number of cycles(>30,000). This means that sizing the ESS by considering an initial DoD of 80% is not adequate to achieve the targeted life span (>30,000 cycles). The reason is that the DoD will be increase above 80% when the actual capacity of the LIC cells fades after a number cycles, which in turn accelerate the capacity fading preventing the achievement of targeted number of cycles(>30,000). To prevent this, the initial DoD to be considered when sizing the ESS should be at least 60% in order to ensure that the maximum DoD will not exceed 80% at the LIC end of life when it is expected to have a 20% capacity fade at (≈30,000 cycles).

Considering the utilization of LIC in the ESS, the total energy required for payload, housekeeping electronics and communications as summarised in Table 6-2 is (≈56Wh). Accordingly, the energy capacity of the ESS based on (6-2) should be (≈104Wh), considering a 90% efficiency for the interfacing charge/discharge regulator (CDR) and 60% DoD for the LIC cells. So, the overall weight of the LIC-cells used in ESS would be ≈9kg and the detailed conceptual design parameters based on [42] are summarised in Table 6-3, by considering the utilization of the ULTIMO 3300F cell that has a specific energy of 13Wh/kg [141].

Table 6-3: Conceptual design parameters for a LIC only based ESS

Minimum Voltage (V)	58
Maximum Voltage (V)	97
Usable Energy capacity(Wh)	104
Equivalent stack capacitance(F)	124
No. of series connected cells/string	26
No. of parallel connected strings	1
Cell capacitance(F)	3224
Cell weight(kg)	0.365
Total weight of LIC cells only (kg)	9.5
Overall weight including packaging (kg)	11.9

6.5 Design of an EDLC only based ESS

The utilisation of electric double layer capacitors (EDLC) (known as supercapacitors) in satellite ESS has been investigated in [37]. The study relied on long cycle life of the EDLC at deep DoD (>80%) as well as the known high specific power of the EDLC compared to the LIB, which in LIB only designs required oversizing in order to be able to supply the high load power peaks. Unlike the LIC, the degradation EDLC is not influenced by the DoD, allowing operation at deeper DoD (>80%) for better utilization of the rated stored energy. The trade-off is that as the voltage of the EDLC decreases as it discharges, at deeper DoD the voltage of the EDLC-stack is significantly reduced and consequently the current of the EDLC stack, whilst having to deliver the load (constant) power, will be significantly higher, increasing the thermal stress of the EDLC cells and increasing the current rating of the interfacing CDR which causes a significant increase of its weight.

Usually, EDLC-ESS are interfacing with the DC power bus through a boost type DC-DC converter that acts as CDR and the topology is shown in Fig.6-11. This topology allows for a maximum voltage of the EDLC-stack to be V_{bus} (here is 100V), whilst the minimum voltage of EDLC-stack is 50% of the maximum stack voltage in order to limit the maximum stack/converter current, which allows for a maximum DoD of 75%.

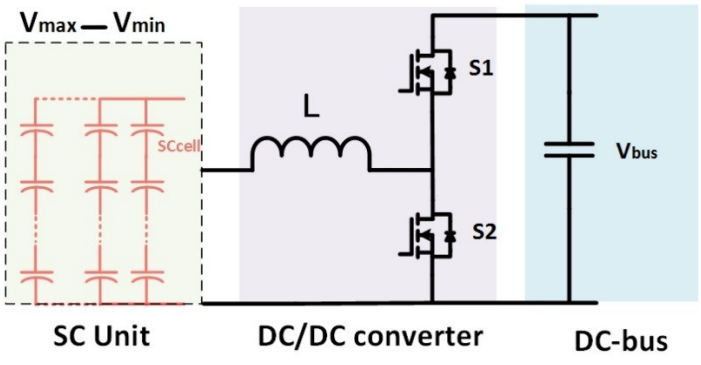


Fig.6-11: Schematic diagram of a supercapacitor based ESS

In terms of life span, it was shown that the EDLC has longer life (higher number of operating cycles) compared to a LIC even at higher operating temperatures range. This is based on the results obtained from long term cycling tests that were analysed in [143] where it is mentioned that the capacity fade of EDLC after 30,000 cycles, at 80% DoD and operating temperature of 25ºC was only 10% of its initial capacity. Therefore, only a 10% oversizing is required in order to compensate for the capacity fade near EoL. Therefore, the rated capacity of the EDLC based ESS should be oversized by 35%: 10% for compensating the capacity fade near EoL and 25% to compensate for the limited 75% utilization of the rated energy at the minimum voltage limit. This is equivalent to sizing the ESS based on a 65% DoD in (6-2).

The starting of the design process is based on the given energy requirement shown in Table 6-2, which accounts for the total required energy for the payload, housekeeping electronics and communications and totals ≈56Wh. Accordingly, the energy capacity of the ESS that utilises EDLC devices should be ≈95.8Wh which is considering 90% efficiency for the interfacing CDR and a 65% DoD for the EDLC cells. As a result, the overall weight of the EDLC cells, considering that the specific energy of the commercially available EDLC is 5.9-6.3Wh/kg [144-147] will be ≈15.2kg. The detailed conceptual design parameters based on [42] are summarised in Table 6-4 that consider the utilization of YUNASKO 1200F cells with specific energy of 5.7Wh/kg [146].

Table 6-4: Conceptual design parameters for the EDLC based ESS

Minimum Voltage (V)	50
Maximum Voltage (V)	100
Usable Energy capacity(Wh)	69.1
Equivalent capacitance(F)	67
No. of series connected cells/string	36
No. of parallel connected strings	2
Cell capacitance(F)	1200
Cell weight(kg)	0.22
Total cells weight(kg)	15.8
Overall weight including mech. Support(kg)	19.8

6.6 Design of Battery-Supercapacitor hybrid ESS

Due to their complementarity, the utilisation of SCs in conjunction with batteries to implement a hybrid ESS is a logical approach whereby the SC operates as a high-power energy buffer to complement the limitation of the main rechargeable batteries. This approach has been investigated in terrestrial applications [148-151] as well as in space applications [9, 152]. Due to higher specific energy, it is expected that the utilisation of the LIC compared to EDLCs in conjunction with Li-ion batteries in a hybrid ESS can significantly contribute to weight savings for ESS, however EDLCs have higher specific power and a better life span. Therefore, both hybrid system options, the hybrid ESS based on Li-Ion EB/LIC and the Li-Ion EB/EDLC will be considered for detailed investigations that will consider the thermal stress on the cells and these aspects will be analysed in the following subsections.

6.6.1 Design of the Li-ion EB-LIC hybrid ESS

A hybrid ESS that combines both EB and LIC can be considered in order to combine the benefits of high specific energy from the EB and the high specific power from the LIC. Accordingly, the resulting ESS will be consists of two parts: the battery pack and the LIC pack. The battery pack is sized based on the energy requirements for satellite housekeeping electronics during eclipse same as in the EB/PB hybrid ESS described in section 6.3.3 with overall weight of the pack including packaging of 1.1kg.

The LIC pack should be sized based on the energy required during the peak power loading that takes place during the radar imaging period (≈17Wh). Accordingly, the capacity of the LIC stack should be ≈31Wh that is considering 60% DoD needed to prolong its lifetime as described earlier and 90% efficiency for the interfacing CDR. As the energy required from the LIC stack in this case is much lower than in the LIC only case, a much smaller LIC cell is considered that

has lower specific energy (≈8-10Wh/kg). The detailed conceptual design parameters are summarised in Table 6-5, that consider the utilization of the Taiyo Yuden 270F LIC cell with a specific energy of 8Wh/kg. The resulting estimated overall weight of the hybrids ESS based on the hybridization of LIC/Li-on EB cells is 6.1kg.

Table 6-5: Conceptual design parameters for LIC pack used in the EB-LIC hybrid ESS

Minimum Voltage (V)	58
Maximum Voltage (V)	93
Usable Energy capacity(Wh)	31
Equivalent capacitance(F)	43
No. of series connected cells/string	25
No. of parallel connected strings	4
Cell capacitance(F)	269
Cell weight(kg)	0.04
Total cells weight(kg)	4.0
Overall weight including packaging (kg)	5.0

In order to simulate the thermal stress on the EB cells and the LICs cell when used in the hybrid ESS, the power loss model and thermal model of the EB (Panasonic NCR18650B cell) still in use. However, as the targeted LIC cell (Taiyo Yuden 270F) is not available in the market yet, the power loss model used is based on ESR specified by the manufacturer (50mΩ) [153]. The thermal model developed in Chapter 3 (section 3.2.2) for the Maxwell BCAP0150 cell will be used to estimate the temperatures of targeted LIC cell as they have similar package size which may results in small errors with temperature estimations for the LIC cell. However, this can provide an indication of the expected range of thermal stress experienced by the LIC cells rather than the exact temperature estimations. The power profile of the battery pack is scaled down to cell level by factor of 18:1 as the total number of battery cells is 18 similar to the EB/PB hybrid. Similarly, the power profile of the LIC stack is scaled down to cell level by factor of 100:1 as the total number of LIC cells in the stack is 100 (25S4P). The simulated performances of the

EB-cell and LIC-cell as subject to single cell scaled down stresses during one orbit operation are shown in Fig.6-12.

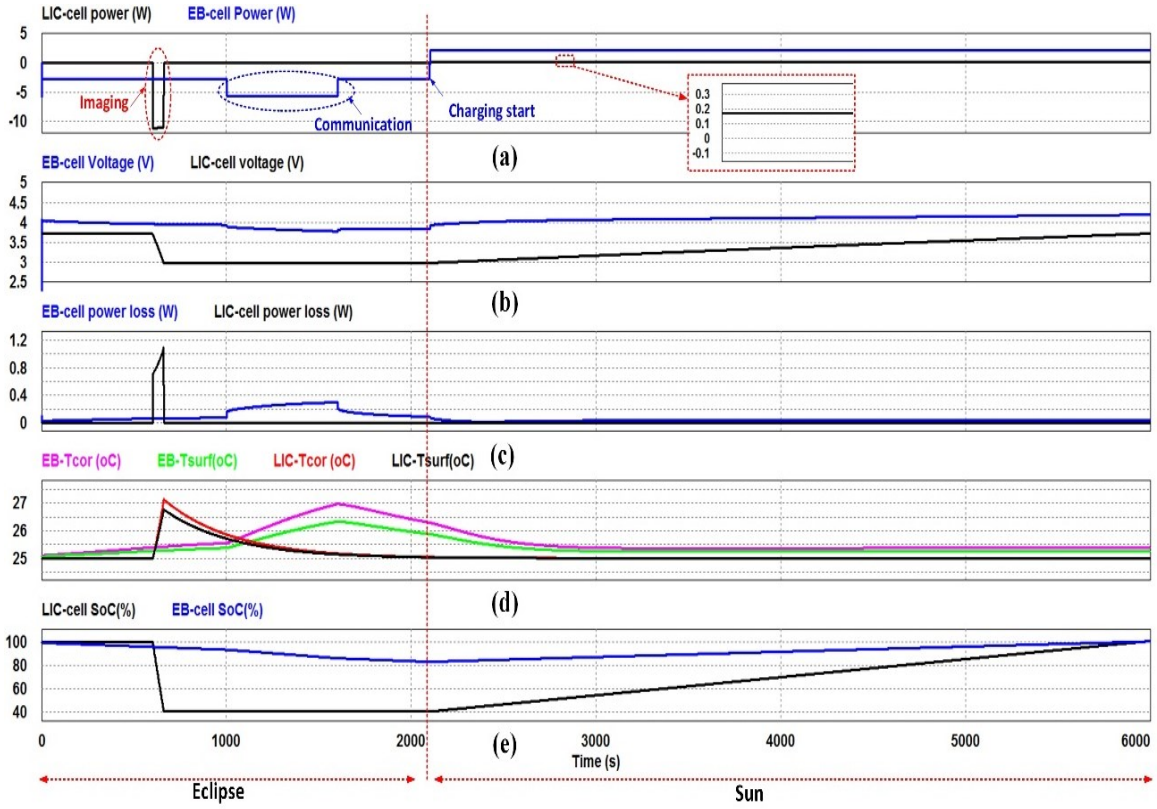


Fig.6-12: Simulated performance of the LIC and EB cells in the hybrid ESS in normal ground conditions under proposed load power profile over one orbit: (a) LIC/EB cells power (b) LIC/EB cells voltage (c) LIC/EB cells power loss (d) LIC/EB cells surface and core temperatures (e) LIC/EB cells state of charge

It can be seen that the power losses experienced by the LIC cell is much smaller compared to the PB in the EB/PB hybrid ESS causing only a 2 ^{o}C increase in the cell temperature. A similar small raise in cell temperature is predicted also for the EB cell. The thermal stress of the LIC cells are expected to be more considerable under higher levels of cell degradation due to the increased internal resistances and also the decreased capacitances which reduces the minimum

voltage of the stack causing more current to be needed for the same power, increasing the power loss as a result.

6.6.2 Design of the of Li-ion EB/EDLC hybrid ESS

A hybrid ESS that uses both EB and EDLC cells can be considered in order to combine the benefits of high specific energy of EBs and the high specific power of EDLCs. Accordingly, the energy storage system will consist of two parts. The battery pack will have the same energy sizing as in the EB-LIC hybrid system discussed previously, with an overall weight of 1.1kg.

The EDLC stack is sized based on the energy requirement of the peak power loading needed during the radar imaging period only (≈17Wh). Accordingly, the capacity of the EDLC stack should be ≈29Wh which considers a 90% efficiency for the interfacing CDR and a 65% DoD for the EDLCs. As this stack utilizes EDLC cells with lower specific energy (≈5-7Wh/kg), the overall weight of the EDLC cells will be 4.4kg with the detailed conceptual design parameters being summarised in Table 6-6. The overall weight of the stack including the packaging will be 5.6kg.

Table 6-6: Conceptual design parameters for EDLC stack used in the EB-EDLC hybrid ESS

Minimum Voltage (V)	50
Maximum Voltage (V)	100
Usable Energy capacity(Wh)	20.6
Equivalent capacitance(F)	20
No. of series connected cells/string	37
No. of parallel connected strings	2
Cell capacitance(F)	740
Cell weight(kg)	0.06
Total cells weight(kg)	4.4
Overall weight including packaging (kg)	5.6

In order to simulate the thermal stress on the EB cells and the EDLCs cell, the power loss model and thermal model of the EB (Panasonic NCR18650B cell) still in use. However, for the targeted EDLC cell (Maxwell BCAP0350), the developed power loss and thermal models described in Chapter 3 (section 3.2.2) is implemented.

The power profile of the EB cell is the same as the one used with LIC-EB hybrid simulations. However, the power profile of the EDLC-pack needs to be scaled down to cell level by factor of 74:1 as the total number of EDLC cells in the pack is 74.

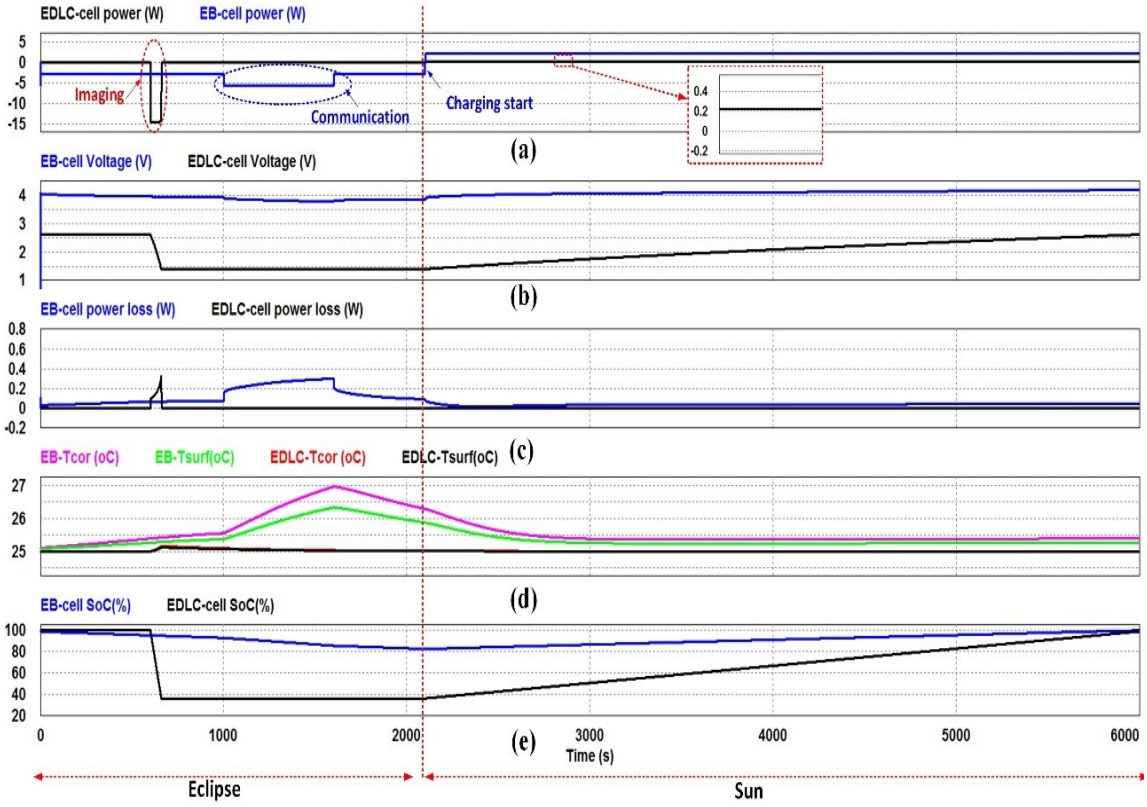


Fig.6-13: Simulated performance of the EDLC and EB cells in the hybrid ESS in normal ground conditions under proposed load power profile over one orbit: (a) EDLC/EB cells power (b) EDLC/EB cells voltage (c) EDLC/EB cells power loss (d) EDLC/EB cells surface and core temperatures (e) EDLC/EB cells state of charge

The simulated performances of the EB-cell and EDLC-cell subject to a rescaled power stress during one orbit are shown in Fig. 5-12. It can be seen that the power loss in the EDLC cell is

negligible due to the small internal resistance and the scaling down of the power load to a large number of cells which is causing an insignificant increase of the cell temperature.

The estimated overall weight of the hybrid ESS based on the hybridization of EDLC/Li-on EB cells is ≈6.7kg which is comparable (although 10% higher) with the LIC/Li-on EB ESS (6kg).

6.6.3 Proposed improved Li-ion EB/EDLC hybrid ESS

In previous section it was shown that the EB/EDLC hybrid ESS has comparable weight to the other ESS solutions based on power batteries and energy batters as well as LICs with less thermal stress and longer life cycle. However, the weight of the EDLC can be further reduced if the usable energy capacity of the EDLC cells can be better utilized. The usable energy of the EDLC-cell can be defined as:

$$UE(J) = \frac{1}{2}C(V_{max}^2 - V_{\min}^2) \tag{6-4}$$

where C in the cell capacitance and V_{max} and V_{min} are its maximum and minimum voltages respectively.

So far, sizing of the EDLC pack has been done based on a usable energy of 75% of the rated energy. This was in order to limit the minimum voltage of the stack to 50% of maximum voltage (which is close to the rated DC bus voltage), to limit the current rating and the weight of the interfaced converter and the thermal stress of the cells during maximum load power when discharging. This limitations are based on the characteristics of the Boost converter topology which is commonly used to interface the EDLC pack to the bus voltage as described earlier (Fig.6-11). However, if a different converter topology with a buck-boost capability is used for interfacing the EDLC pack to the power bus, it will allow the EDLC stack voltage to be designed at a much higher voltage level (much higher than the DC bus voltage), whilst the

design of minimum voltage maintained at 50% of the bus voltage. Accordingly, a higher number of smaller sized series connected EDLC cells are utilized subject to a wider voltage range per cell which further maximises the energy extraction of the cells according to (6-4). The conceptual design parameters of an EDLC-pack based on the proposed concept is compared to the conventional design presented earlier and the result is presented in Table 6-7. Both designs are considering the utilization of the same cell Maxwell BCAP0350 (350F) cells and the same DC bus voltage of 100V. For the conventional design, the maximum voltage has been chosen equal to the bus voltage (100V) whilst the minimum voltage has been selected at half (50V) as described earlier. On the other hand, the maximum voltage of the stack in the proposed designed has been selected at 167.4V, whilst the minimum voltage remains at 50V, same as for the conventional design to maintain the same maximum current at minimum voltage.

Table 6-7: Different designs for EDLC-part of the EB-EDLC hybrid ESS

Design parameters	**conventional design**	**proposed design**
Minimum Voltage (V)	50	50
Maximum Voltage (V)	100	167.4
Usable Energy capacity(Wh)	20.6	20.6
Equivalent capacitance(F)	20	6
No. of series connected cells/string	37	62
No. of parallel connected strings	2	1
Cell capacitance(F)	740	372
Cell weight(kg)	0.06	0.06
Total cells weight (kg)	4.4	3.7
Overall weight including mech. support(kg)	5.6	4.7

It can be observed that the proposed design results in lower number of cells (62 vs 74) which saves around 16% in cost and weight of the EDLC pack compared to the conventional design due to the better utilization of the available energy capacity of the cells. In the proposed design,

the voltage of the single EDLC-cell decreases from 2.7V at maximum SoC (corresponding to maximum stack voltage of 167.4V) down to 0.8V at minimum SoC (corresponding to minimum stack voltage of 50V), whilst the cell voltage in the conventional design decreases from 2.7V at maximum SoC (corresponding to maximum stack voltage of 100V) down to 1.35V at minimum SoC (corresponding to minimum stack voltage of 50V).

A simulated operation of the single cell as subject to the 62:1 rescaled load power in the EDLC-pack based on the proposed design during one-orbit cycle is shown Fig.6-14.

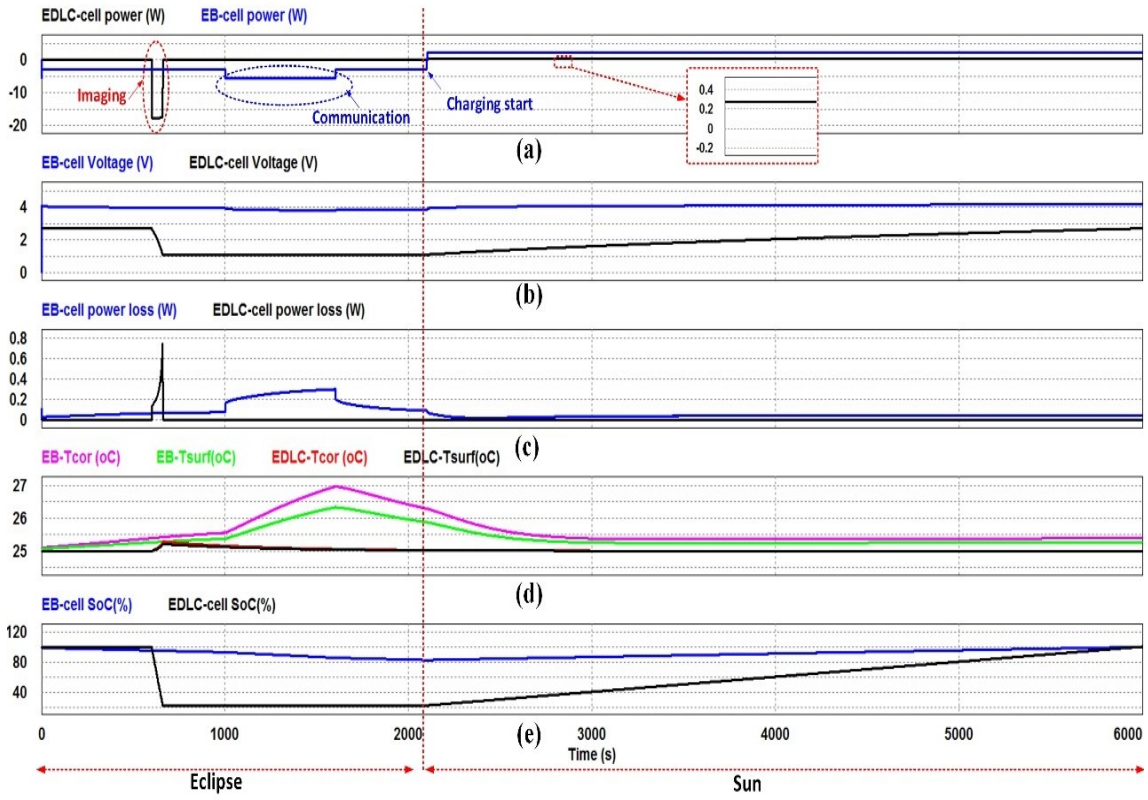


Fig.6-14: Simulated performance of the EDLC and EB cells in the hybrid ESS with improved EDLC desing in normal ground conditions under proposed load power profile over one orbit: (a) EDLC/EB cells power (b) EDLC/EB cells voltage (c) EDLC/EB cells power loss (d) EDLC/EB cells surface and core temperatures (e) EDLC/EB cells state of charge

It can be observed that the utilized energy of the cell has been increased to 90% which can be seen in the SoC curve that reached 80% at the end of discharge cycle (there is 10% reserved

energy due to oversizing of the pack by 10% in order to compensate for degradation near EoL). On the other hand, an increased thermal stress can be noted that is caused by an increased power share of the cell due to the reduced number of cells in the proposed design but this increase is still negligible as can be seen in the temperature curves.

Based on the proposed design concept for the EDLC pack to be used in the EDLC-EB hybrid ESS, the overall weight of the ESS will be reduced to 5.7kg which is less compared to the LIC-EB hybrid ESS (6.7 kg) and nearly same weight compared to the EB based ESS (5.6kg) but has more advantages including lower thermal stress that can translate in longer life time.

Further reductions for the EDLC pack can be achieved by increasing the maximum voltage of the pack and this will be investigated in more details in Chapter7 where a new multiport converter topology will be proposed. This is able to provide the features needed by the proposed hybrid design such as providing a port with buck/boost voltage capability for interfacing with the battery and the supercapacitor packs and a port with voltage boost only capability for interfacing with the PV array.

6.7 Comparative analysis

The specifications of the ESS based on the described design options are summarized in Table 6-8. As it can be seen, the designs of the ESS based on supercapacitors (EDLC and LIC) results in extremely heavy designs (11.9kg and 15.4kg) although it can provide insignificant thermal stress on SC cells as an energy storage devices due to the high specific power of these devices. This cause the design of the ESS based on EDLC or LIC only to be of no beneficial solution even though it can provide many advantages including the wider operating temperature range and the insignificant thermal stress on the cells during peak power loading. Similarly, the design of the ESS based on the Li-ion power batteries that weights 7.6kg due to the low specific energy

of these battery cells. This design also provides very small thermal stress on the battery cells but it has the disadvantage of the increased weight in additional to the limited operating temperature range that introduce the need for thermal control with added weight. Also, it has a limited charging power especially with the shallow DoD (always charged in constant voltage mode) being used that will reflect on the utilization of the available power from the PV especially under the higher power available when the PVs are cold for few minutes after returning from eclipse which in turn affects PV array sizing. On the other hand, the design of the ESS based on Li-ion energy batteries that has been oversized in order to handle the peak power loading safely showed an overall weight of 5.6kg which is significantly less compared to the other design options based on SCs and power batteries. However, this design has the disadvantages of the power battery based ESS related to the limited operating temperature range and limited charging power.

The design of the ESS based on EB/PB hybrid showed the lowest overall weight (3.48kg) in the described options but in the cost of moderate thermal stress in the PB cells. Also, the two parts of the ESS are based on batteries it still has the disadvantages of limited operating temperature range and limited charging power.

The design of the ESS based on EB/LIC hybrid showed and EB/EDLC hybrid with weights of 6.1kg and 6.6 kg respectively which is in range compared to the ESS design based on EB only with weight of 5.6kg. It added more advantages to the ESS including high charging power, therefore it can be recharged many times during the single orbit enabling repeated imaging sessions providing more flexibility for the payload operations. However, the EB/EDLC hybrid ESS showed less thermal stress under the peak power loading compared to EB/LIC hybrid ESS. Additionally, the weight of EDLC-EB hybrid ESS under the proposed interfacing methodology is less (5.8kg compared to 6.6kg for the EB/EDLC hybrid). This can promote the EB/EDLC hybrid to be considered as a better design option for the ESS.

Table 6-8: Specifications of the ESS based on different designs

Design option	utilized devices	Initial DoD %	weight (kg)/part	ESS overall weight (kg)	Thermal stress
Energy Battery	EB	20	5.6	5.6	small
Power battery	PB	10	7.6	7.6	very small
Battery (EB/PB hybrid)	EB PB	20 10	1.1 2.38	3.48	small moderate
LIC	LIC	60	11.9	11.9	insignificant
EDLC	EDLC	75	15.2	15.2	insignificant
EB-LIC hybrid	EB LIC	20 60	1.1 5	6.1	small small
EB-EDLC hybrid	EB EDLC	20 75	1.1 5.6	6.6	small insignificant
EB-EDLC hybrid with proposed interfacing	EB EDLC	20 90	1.1 4.7	5.8	small insignificant

Summary

In this chapter, the different options for the design of the energy storage system (ESS) based on Li-ion battery cells as well as and supercapacitors (EDLC and LIC) have been investigated in terms of the overall weight of the ESS cells and the thermal stress the storage device cell is subjected to. The design of the ESS based on the high specific energy Li-ion batteries (energy battery (EB)) requires the oversizing of the battery pack in order to limit the discharging rate during the peak load power required during radar imaging operation to an acceptable level, and this resulted in an overall weight of 5.6kg for the ESS. Utilisation of high specific power Li-ion battery (referred to a power battery (PB) cells) for the ESS has been investigated which showed negligible thermal stress under peak power, but it resulted in a heaver design (7.5kg) due to the use of lower specific energy PBs. A hybrid ESS implementation based on PB and EB cells has

been investigated in order to combine the benefits of both batteries which achieved reduced overall weight for the ESS (3.48kg). However, sizing the PB based on only the energy requirement of the peak power pulse resulted in a smaller capacity, and consequently higher discharging rate compared to this capacity that resulted in higher thermal stress, especially when a higher internal resistance is assumed as when the PB cells degrade. This significant stress that was observed requires additional oversizing for the PB-pack in order to prolong the life time to the expected operation lifetime of the satellite. Utilisation of supercapacitors in the ESS has been also investigated due to its long life time whilst being able to operate under deep depth of discharge (DoD) and its high specific power. However, it both available SC technologies resulted in extremely heavy designs with overall weight of 11.9kg for the LIC based ESS and 19.8kg for the EDLC- based ESS. Finally, a hybrid ESS design concept based on EBs and supercapacitors (EDLC/LIC) has been investigated. The EDLC-EB hybrid ESS that is following a conventional design of the EDLC pack resulted in a slightly heavier design with overall weight of 6.7kg compared to the LIC-EB hybrid ESS that had an overall weight of 6kg. However, the proposed design for the EDLC pack could reduce the overall weight of the EDLC-EB hybrid ESS to 5.7kg whilst maintaining the thermal stress of the SC cells at negligible levels compared to the LIC-EB hybrid ESS. Accordingly, the EDLC-EB hybrid ESS can be considered as better option for the ESS, even though it has a heaver weight compared to the energy battery/power battery hybrid ESS (5.7kg compared to 3.46k), if the operating temperature range and fast charging are taken into account .

Chapter 7. Proposed MPC for HESS

In Chapter 6, the hybrid energy storage systems (HESS) based on Li-ion energy batteries and EDLC (will be referred as supercapacitor (SC)) was considered the best design for the energy storage system based on the given load power profile as it shows minimum stress on the energy storage devices and wider operating temperature range at comparable weight compared to other design. However, conventional converter topologies to interface the SC-stack to the power bus is limiting the utilization of the available energy capacity to 75% to limit the current rating of the converter that resulted in suboptimal design of SC-stack. Therefore, development of novel integrated converter that enables maximum utilization of the available energy of the SC-stack without penalties on the converter size will be investigated.

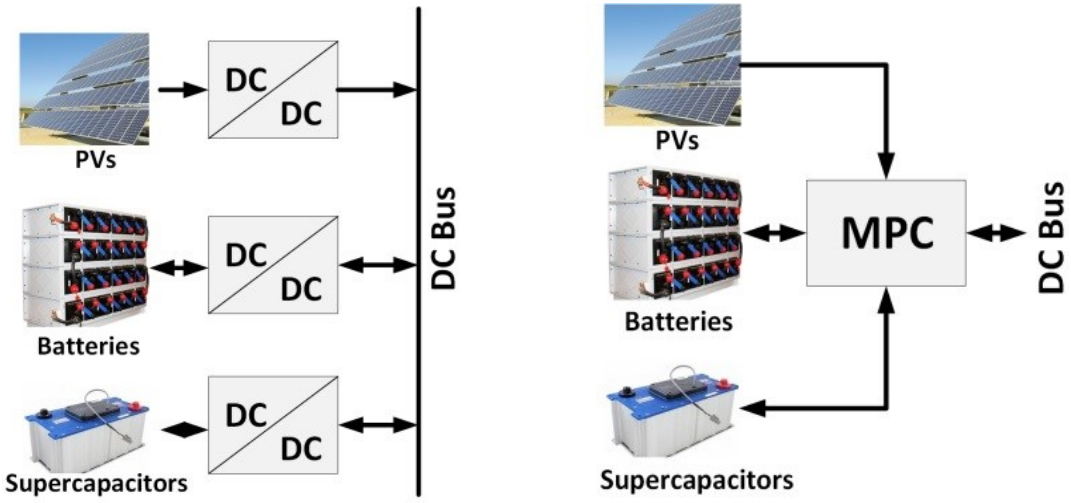
7.1 Introduction

Integrating the HESS with the primary power source (i.e. PV array) when implementing a power system was conventionally achieved by employing separate converters, so that each source interfaces with the DC-bus through its own independent converter, as illustrated in

Fig. 7-1a. Recently [110, 118], multi-port converter (MPC) topologies have been proposed for integrating the HESS with a primary electric power source and connect to the DC-bus, a concept illustrated in Fig.7-1b. This concept may provide higher system efficiency, lower cost and a more compact design.

Most of the proposed converter topologies that are used in either the multi-input-port or in the separate converters structures are based on the voltage boost-stage for interfacing with the supercapacitor (SC) unit [154-159]. This resulted in poor utilization of the SC-stack/unit due to

narrower voltage range which impacts the Usable specific energy (USE), as it will be discussed in more details in Section 7.2.



(a) (b)

Fig. 7-1 Power system implemented with (a) separated converters and (b) multiport power converter

In this Chapter, a novel MPC for integrating the Li-Ion EB stack, the SC stack and the PV array with the DC power bus in a single power conversion system is proposed. The proposed multiport converter can provide two input ports with buck-boost operation for interfacing the battery and the SC-stack that allows their voltages to be below or above the power bus voltage. This enables maximizing of the USE of the SC-stack enable a 1:4 voltage range (rather than 1:2) which in turn can reduce the required capacitance and consequently the size/weight of the SC-stack. Furthermore, a new modulation methodology is proposed that enables a significant reduction of the sizes of inductors by manipulating the phase shifting of the carrier modulation signals of the different conversion stages.

7.2 The proposed multiport converter topology

Typical topologies that can interface with multiple sources such as battery, SC and PV use a voltage boosting stage for interfacing with SC-stack as seen in Fig. 7-2a. Such topologies limit the maximum voltage of the SC-stack at the bus voltage (V_O). In order to investigate the effect of this on the utilized energy capacity of the SC-stack, the nominal specific energy (*SE*) of the SC-cell, which can be used to estimate the weight of the SC-stack at a required energy capacity, can be defined as:

$$SE = \frac{\frac{1}{2} C V_{max}^2}{3600 \times m} \quad \text{[Wh/kg]} \tag{7-1}$$

where C, V_{max} and m are the capacity, maximum voltage and weight of a single SC-cell respectively. The SE is usually specified by manufacturers under specific conditions [145, 160]. However, as it can be observed from (7-1), the estimation of the *SE* assumes full utilization of the energy capacity of the SC-cell, but this would requires full utilization of the voltage range of the SC-cell (i.e. from V_{max} down to 0), which is impractical due to the extremely high charging/discharging currents of SC-stack at extremely low voltages. Since for practical reasons it is not possible to utilize the whole rated energy capacity of the SC-cell, the usable specific energy (*USE*) of the SC-cell can be used instead which can be defined based on the actual utilized voltage range for the SC-cell as:

$$USE = \frac{\frac{1}{2} C (V_{max}^2 - V_{min}^2)}{3600 \times m} \quad \text{[Wh/kg]} \tag{7-2}$$

where V_{min} is the minimum voltage of the SC-cell. As it can be observed from (7-2), at a specified V_{max} that is fixed for a given technology of SC-cells (defined by manufacturer), the USE is influenced by V_{min} of the SC-cell.

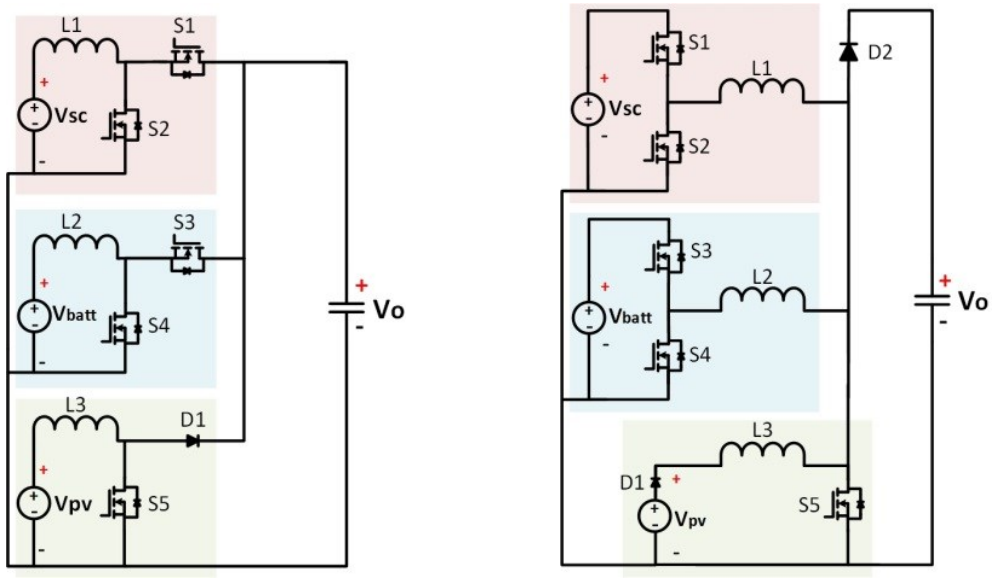


Fig. 7-2 MPCs structure based on (a) the boost MPC topology and (b) the proposed topology

By interfacing the SC-stack to the power bus through a boost converter, the maximum voltage of the SC stack is limited to the bus voltage (Vbus $\geq n\mathrm{V}_{max}$ where n is the number of series connected SC-cells), whilst the minimum stack voltage will be ($=n\mathrm{V}_{min}$). The lower the minimum voltage of the SC-stack and consequently V_{min} of the SC-cell, a higher USE can be achieved which in turn reduces the weight of the SC-stack for a required amount of energy stored. However, reducing the voltage of SC-stack below a reasonable level results in a significant increase in the maximum charging/discharging current (I_{max}) that is needed to deliver the rated power at the minimum voltage of the SC-stack which will affect the current ratting of the converter that results in larger weight and reduced efficiency whilst it may also increase the thermal stress of the SC-cells.

The proposed MPC topology shown in Fig. 7-2 (b) changes the way the SC converter operates from a boost to a buck-boost functionality when the S1-S2 half bridge converter stage operates in conjunction to the S5 boost stage, without needing any extra added components. The buck-boost functionality of the SC-stack interfacing port is allowing the maximum voltage of SC

stack to be significantly higher than the bus voltage *Vo* which results in an increased number of series connected SC-cells (*n*). Increasing *n* whilst keeping minimum stack voltage constant (nV_{min}) allows significant reduction in SC-cell minimum voltage (V_{min}), which maximizes the USE according to (7-2) compared to a boost SC-stage.

Fig. 7-3 show the relative *USE* as percentage of the nominal *SE* for SC-cells used in the different designs depending on minimum and maximum voltages of the SC-stack as relative to the bus voltage. In a conventional MPC where the SC-stack is interfaced through a boost-stage, the maximum voltage of the SC-stack (nV_{max}) is limited at V_O. Accordingly, for a given SC-stack power, if the minimum voltage of the SC-stack (nV_{min}) is chosen $0.5V_O$, then the *USE* of the SC-cells will be 75% of the rated *SE*. However, lower values of (nV_{min}) can be considered in order to increase the *USE*, but the maximum current of the converter/SC-stack (I_{max}) will be significantly increased compared to the load current (I_O).

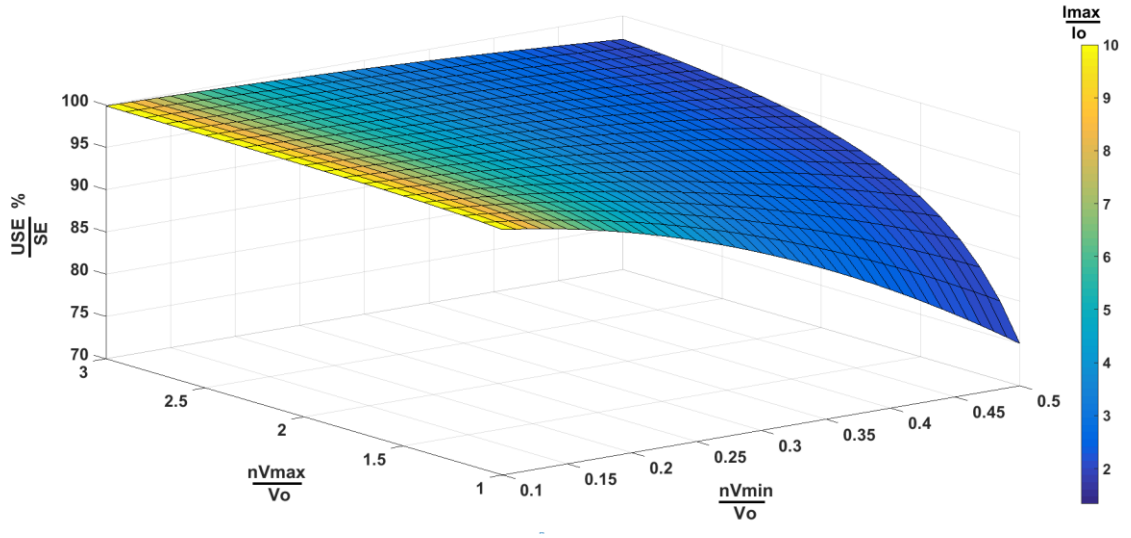


Fig. 7-3 Variation of USE of an SC stack with different design choices for maximum and minimum stack voltages as relative to the constant bus voltage.

On the other hand, as the proposed MPC enables the increase of SC-stack maximum voltage (nV_{max}) to a higher level than the bus voltage, a *USE* of 95% of the nominal SE can be easily

achieved at (nV_{max}=2V_O) and (nV_{min}=0.5V_O) with no additional increase in maximum converter current rating (I_{max}) compared to the previous design that achieved a *USE* of only 75% of the nominal SE. This means that the utilization of the available energy capacity of the SC-stack has been increased by 20% which for a given energy storage requirement allows a 20% reduction in the weight of the SC-stack. Further increase in the SC-stack maximum voltage is providing less significant increase in the *USE* as the increasing as can be seen in Fig. 7-3.

7.3 Operation of the proposed converter

The proposed converter topology shown in Fig. 7-2b consists of five power switches, three inductors and a single separate diode (D2). The diode (D1) is a blocking diode which usually equips PV-arrays to prevent reverse conduction during night and is not a functional part of the proposed converter. V_{pv} is the voltage of the PV-array connected to the unidirectional input power port of the converter and V_{batt} is the voltage of the battery stack which experiences a relatively narrow voltage range and is therefore connected to the one of the bidirectional input power ports and V_{SC} is the voltage of the SC-stack connected to the other bidirectional input power port.

The possible operation modes of the proposed MPC, are illustrated in Fig. 7-4:

*Single Input Double Output (SIDO) mode (*Fig. 7-4*a):* in which the PV supplies the required load power whilst any excess is charging the battery.

*Single Input Triple Output (SITO) mode (*Fig. 7-4*b):* in which a significant amount of power is produced by the PV that is able to supply the load power and due to limitations of maximum charging battery current, all excess is stored in the SC stack.

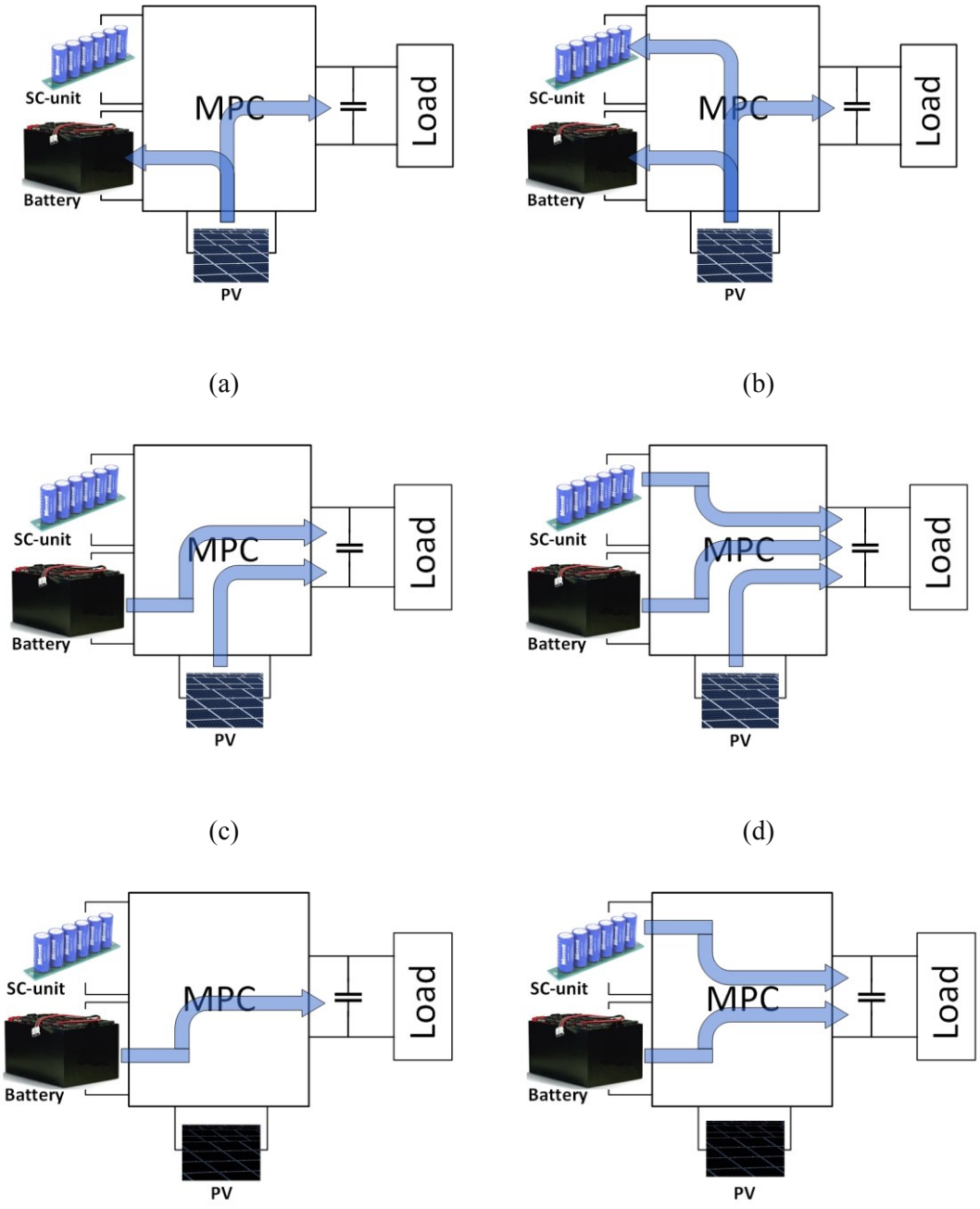


Fig. 7-4 Illustration of the power flows for all operation modes of the proposed MPC: (a) SIDO mode, (b) SITO mode, (c) DISO-I mode, (d) TISO mode, (e) SISO mode and (f) DISO-II mode.

*Double Input Single Output (DISO) mode-I (*Fig. 7-4*c)*: in which the PV is unable to supply the load power and any deficit is provided by the battery, where load is not excessive and (medium power peaks).

*Triple input single output (TISO) mode (*Fig. 7-4*d):* in which the PV, the battery and the SC-stack are supplying the load power during high power peaks which exceed the available PV power and the battery discharge current capability.

*Single Input Single Output (SISO) mode (*Fig. 7-4*e):* in which battery provides power for supplying the load during unavailability of the PV power.

*Double input power single output power (DISO) mode-II(*Fig. 7-4*f):* in which both the battery and the SC-stack provide power for supplying the load during significant load power peaks which happen during unavailability of PV power.

In order to simplify the analysis of the converter, the following assumptions are made: continuous conduction mode (CCM) is considered for all modes of operations and the power MOSFETs and diodes are considered to be ideal (R_{ds}=0, V_f=0), and the upper and lower switches of the battery stage are working in complementary order with zero dead time and similarly for SC stage switches. The Inductors and capacitors parasitics are also neglected.

7.3.1 Operation principle of the proposed MPC during the SIDO mode

The typical waveforms and current paths of the converter under SIDO mode are shown on

Fig. 7-5 and Fig. 7-6 by assuming that the SC-stack is completely charged and its voltage is higher than V_O. The operating modes can be described as follows:

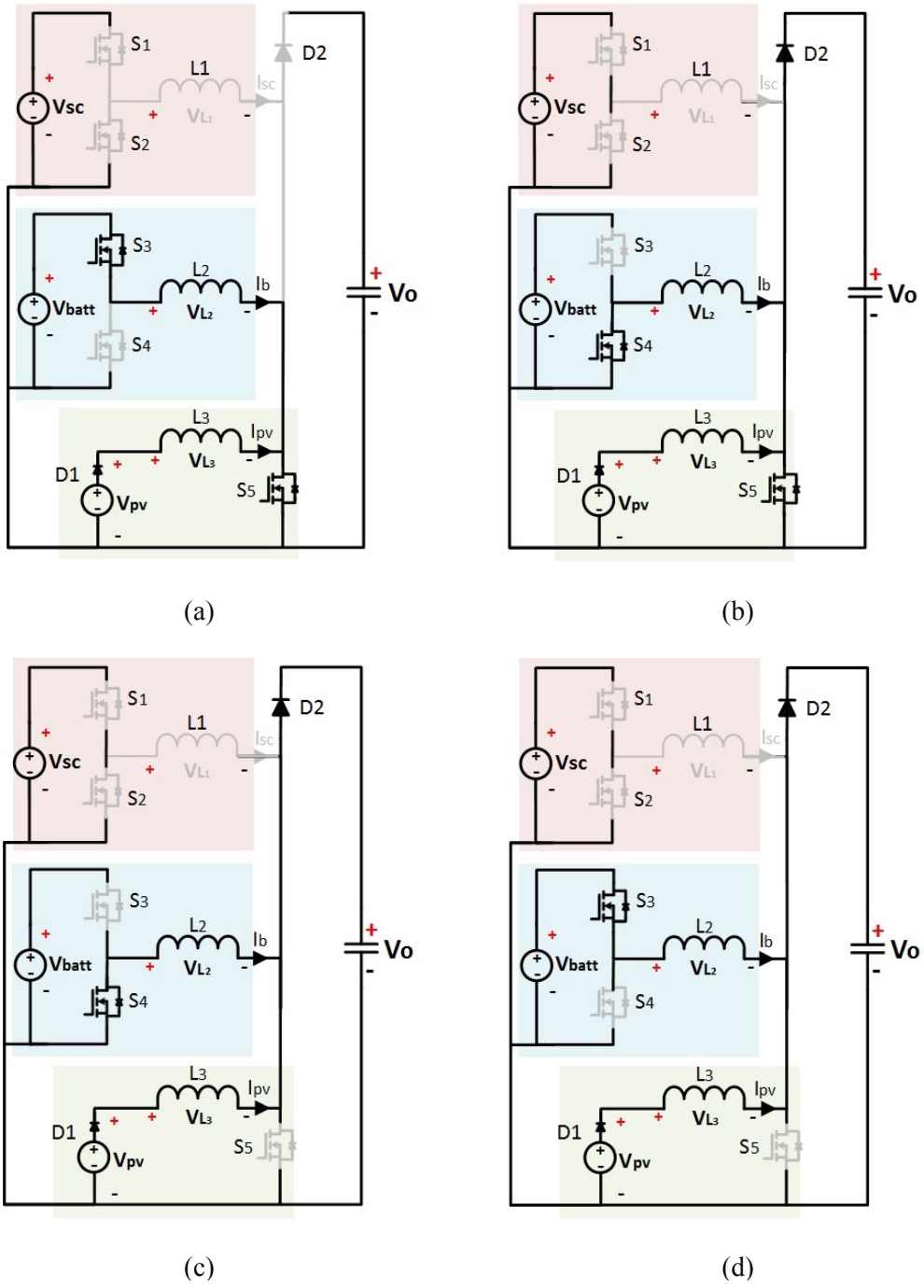


Fig. 7-5 Illustration of the current paths during the different stages of operation of SIDO mode: (a) Step I, (b) Step II, (c) Step III and (d) Step IV.

Step I : PV switch S5 is turned ON whilst the battery converter switch S3 is still in conduction from the previous cycle. The voltage across L3 is V_{pv} and the voltage across L2 is V_{batt} where D2 is OFF.

Step II : S5 is still in conduction when S3 is switched OFF. The voltage across the L2 becomes zero (shorted to ground via S4 and S5) whilst the voltage across L3 is still V_{pv}.

Step III: S5 is switched OFF whilst S3 is still OFF, so the voltage across the L2 is ($-V_O$) and the voltage across L3 is (V_{pv}-Vo).

Step IV: S5 is still OFF when S3 is switched ON, so the voltage across the L2 is (V_{batt}-V_O) and the voltage across L3 is (V_{pv}-V_O).

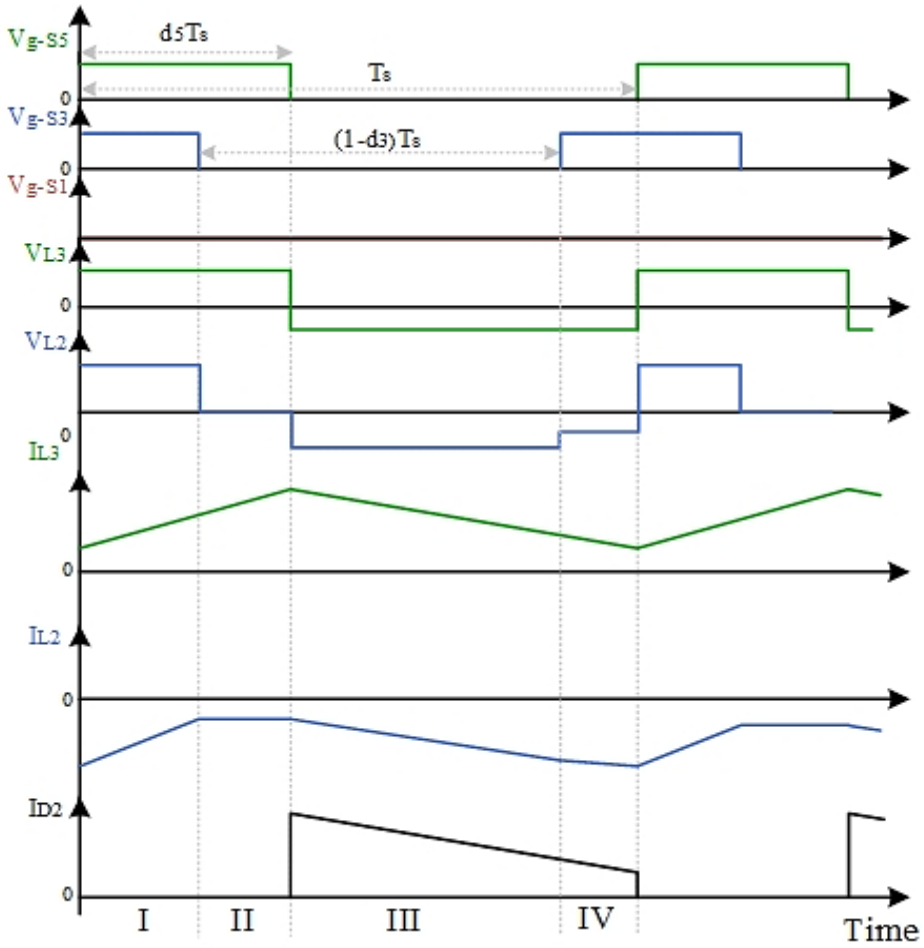


Fig. 7-6 Relevant voltage and current waveforms during SIDO mode.

By applying the voltage balance principle for inductor L3, the following equation can be obtained:

$$d_5 V_{PV} + (1 - d_5)(V_{PV} - V_O) = 0 \tag{7-3}$$

Therefore

$$V_{PV} = (1 - d_5)V_O \tag{7-4}$$

where d_5 is the duty cycle of the PV converter switch S5 and for a given bus voltage Vo, is dependent only on PV voltage to enable the desired MPP extraction.

Similarly, by applying the voltage balance principle for inductor L2, the following equation can be obtained:

$$d_3 V_{batt} - (1 - d_5)V_O = 0 \tag{7-5}$$

Therefore

$$V_O = \frac{d_3}{(1-d_5)} V_{batt} \tag{7-6}$$

Where d_3 is the duty cycle of the switch S3, which for a particular d_5, and bus voltage is dependent only on the battery voltage.

7.3.2 Operation principle of the SITO mode

The operation of the converter under the SITO mode is similar to the SIDO mode with SC in operation, as can be observed from the typical waveforms and current paths shown in Fig. 7-7 and Fig.7-8. During this mode, the voltage of the SC-stack changing significantly from Vsc_{min} up

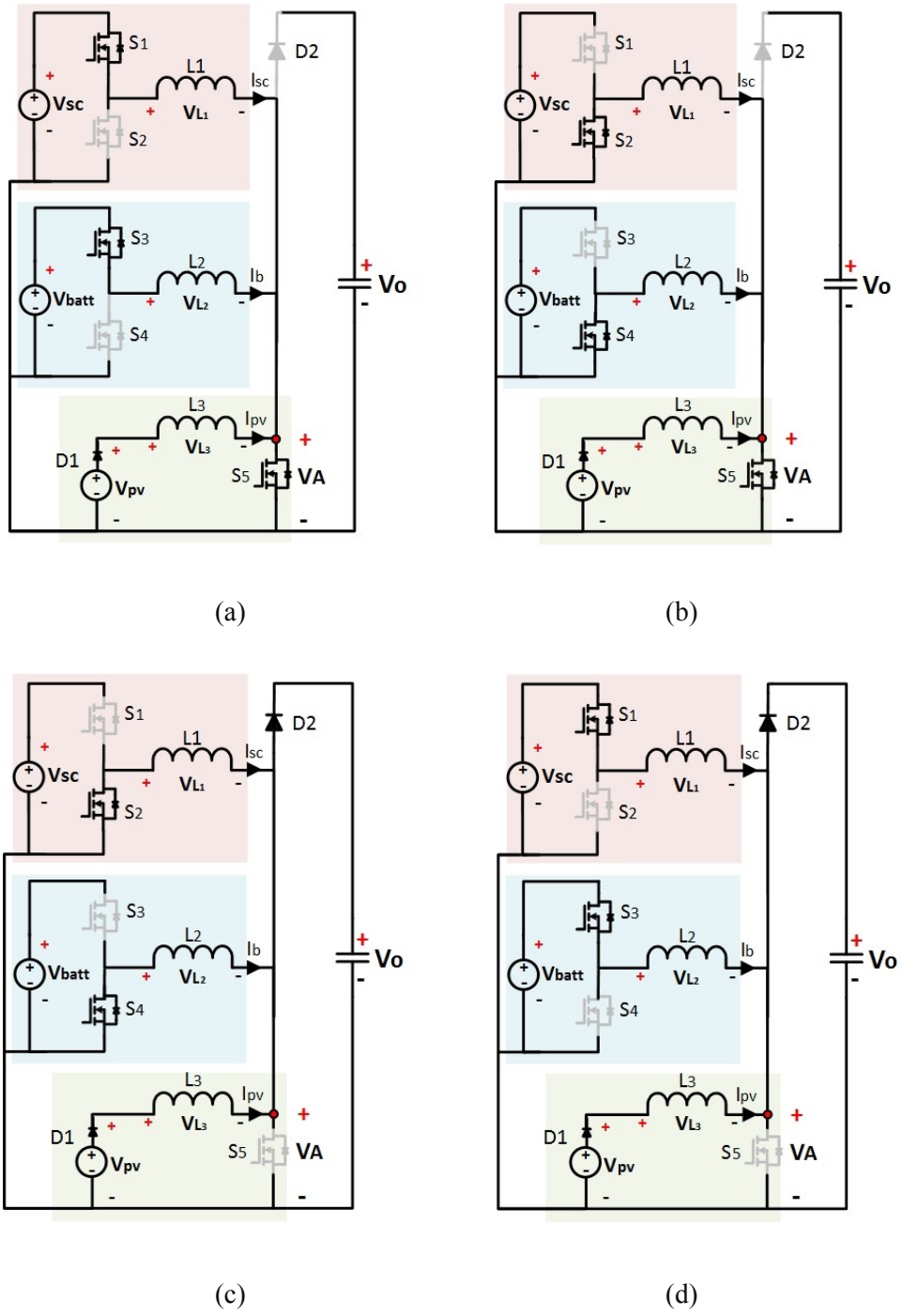


Fig. 7-7 Illustration of the current paths during the different stages of operation of SITO mode: (a) Step I, (b) Step II, (c) Step III and (d) Step IV.

to Vsc_{max}. So, in order to prevent the undesired conduction of the switch S1 through its body diode to maintain the controllability of its charging current, the average voltage at point A (V_A) should be always less than V_{SC}. The average voltage of V_A under this mode can be defined as:

$$V_A = (1 - d_5)V_O \tag{7-7}$$

Accordingly, in order to ensure controllability of the SC-stack current under the large variation of its voltages during charge/discharge operations, the minimum duty cycle of the switch S5 should satisfy:

$$d_{min_5} \geq 1 - \frac{Vsc_{min}}{V_O} \tag{7-8}$$

where Vsc_{min} is the minimum voltage of the SC-stack.

It can be observed that the maximum power point tracking (MPPT) function of the PV stage can be overridden when the required duty cycle of S5 (d5) is less than d_{min5}. In this particular case the switch S5 will be forced to work by the duty cycle d_{min5} causing the PV to work away from MPP, which can be accepted for short time, until the SC-stack voltage increased to PV voltage. The output voltage of the converter during this mode is defined by (7-6) as well.

7.3.3 Operation principle of the DISO-I and TISO modes

The operation of the converter during the DISO-I mode is similar to the operation during the SIDO mode, with opposite polarity for the current of L2. Also, the operation in TISO mode is similar to the operation during SITO, with opposite polarity for the currents of L1 and L2.

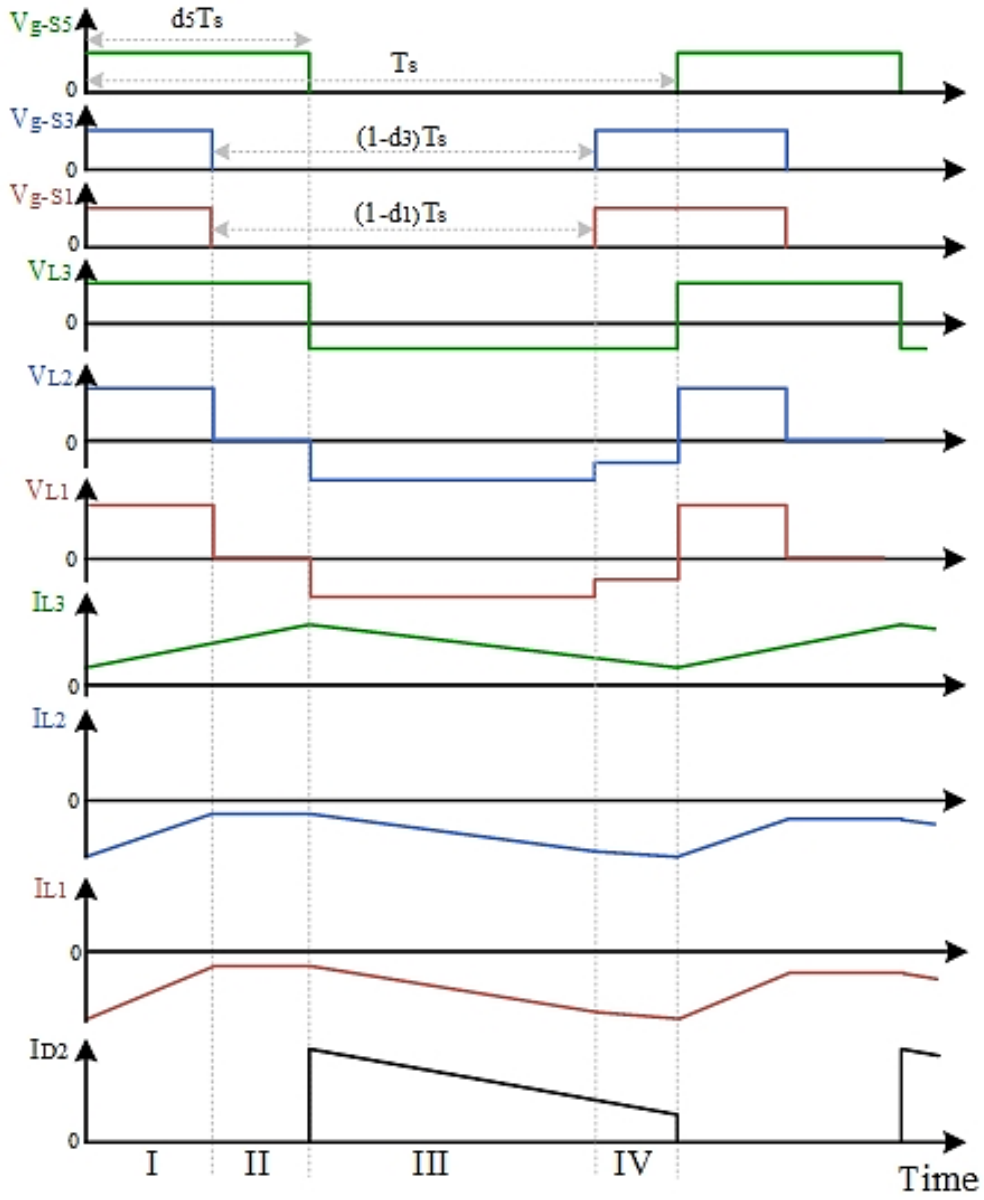


Fig.7-8 Relevant voltage and current waveforms during SITO mode

7.3.4 Operation principle of the SISO modes

During the SISO mode, as there is no power available from the PV and consequently the switch S5 is OFF, the converter acts like a conventional buck converter as seen in Fig.7-9, assuming SC-stack's voltage at (V_{max}>V_O). The output voltage can be defined as:

$$V_O = d_3 V_{batt} \tag{7-9}$$

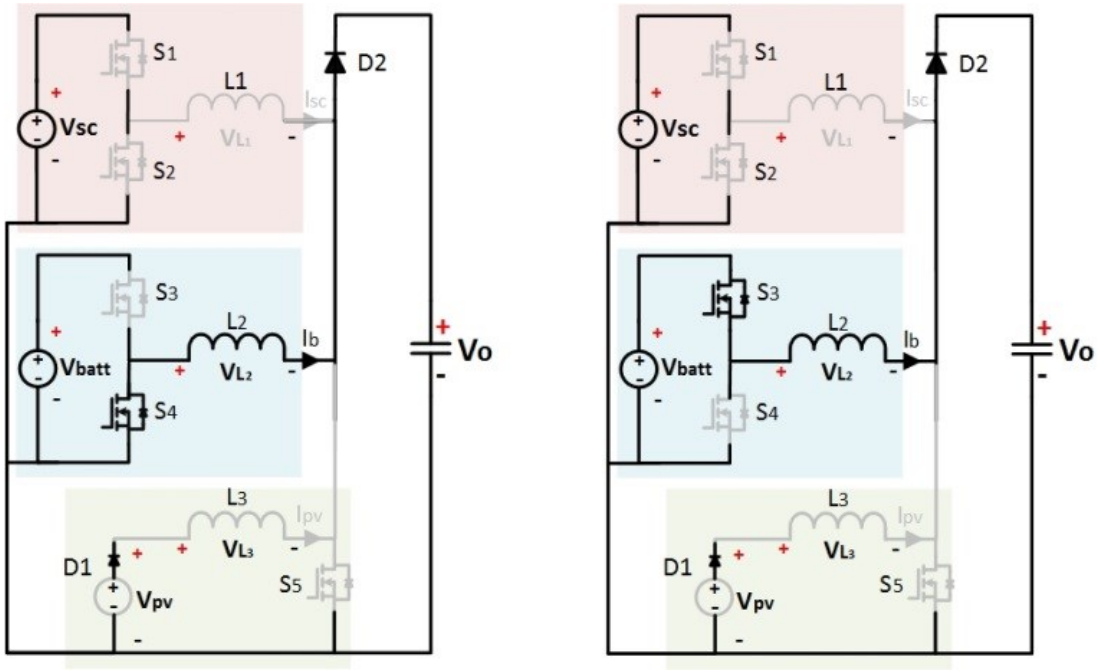


Fig.7-9 Illustration of the buck operation of the converter during SISO mode

As can be observed, the maximum output voltage during this mode is limited to the battery voltage, compared to the previous modes of operation at which the maximum output voltage can be higher than battery voltage.

Operating the switch S5 during this mode with a duty cycle controlled by the output voltage control loop can sustain the buck-boost operation of the converter achieved in other modes of operation. Accordingly, in order to ensure the controllability of the battery current, the minimum duty cycle of the switch S5 should satisfy:

$$d_{min_5} \geq 1 - \frac{V_{batt_{min}}}{V_O} \tag{7-10}$$

where $V_{battmin}$ is the minimum voltage of the battery at lowest state of charge (SoC).

Typical waveforms and current paths of the converter under this mode of operation are shown in Fig. 7-10 and Fig.7-11. The output voltage during this mode can be derived by applying voltage balance on L2 same as in (7-5) and (7-6).

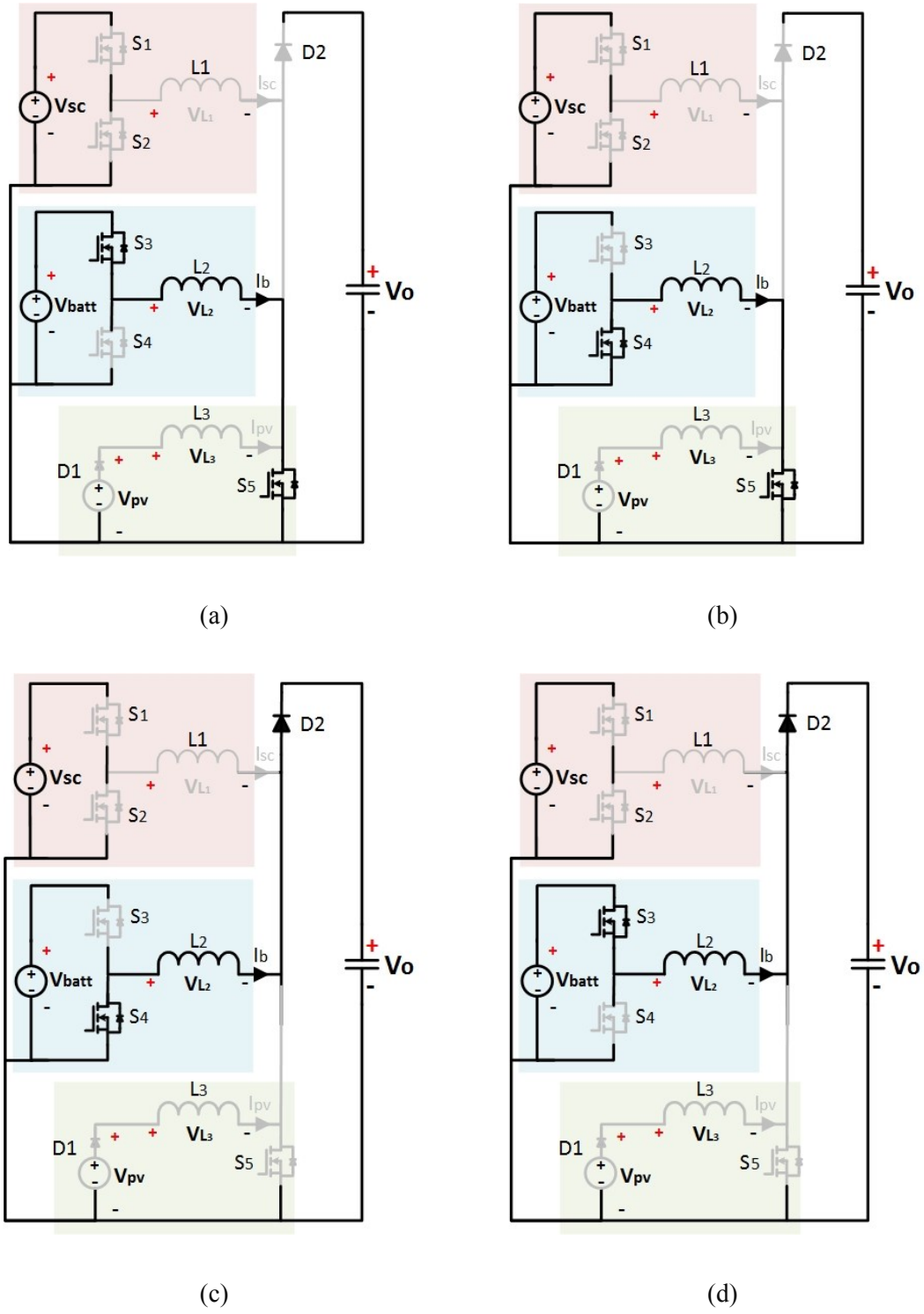


Fig. 7-10 Illustration of the current paths during the different stages of operation of SISO mode: (a) Step I, (b) Step II, (c) Step III and (d) Step IV.

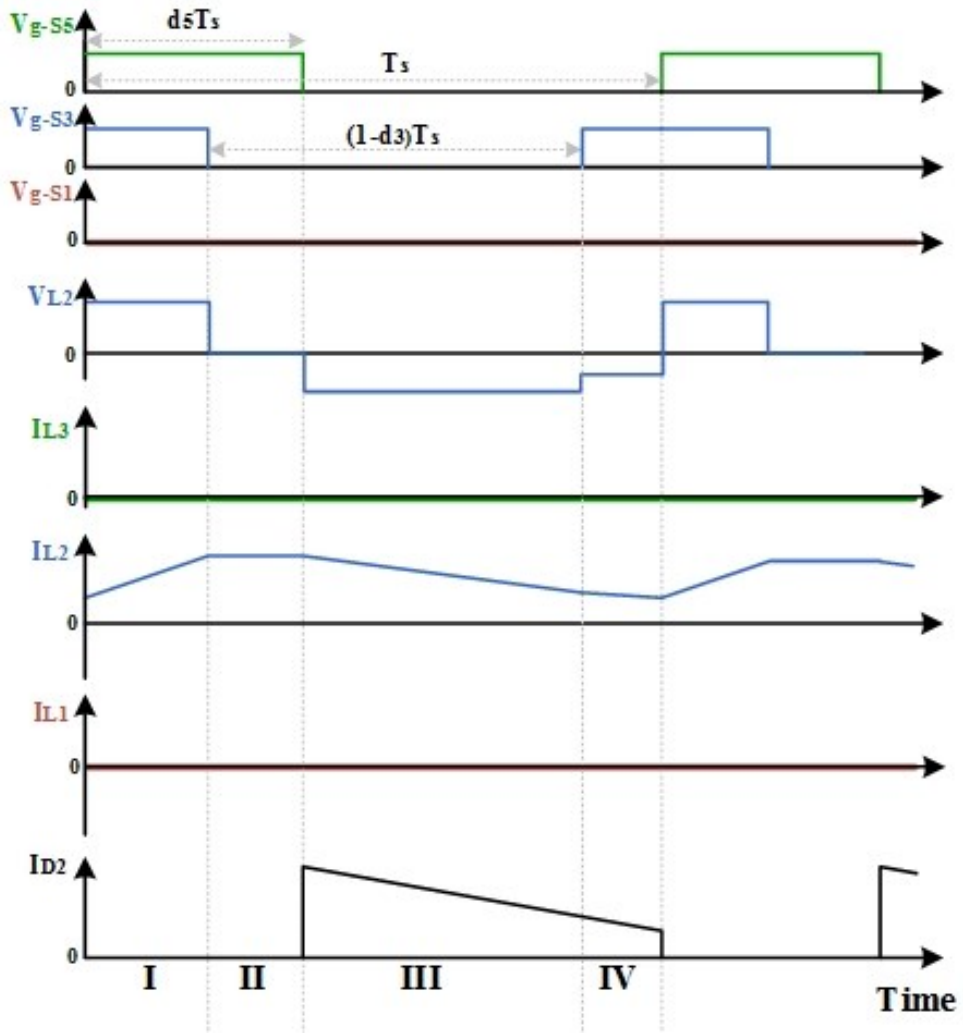


Fig.7-11 Relevant voltage and current waveforms during SISO mode

7.3.5 Operation principle of the DISO-II modes

During this mode, as the SC-unit discharges and its voltage decreasing significantly, the duty cycle of the switch S5 should satisfy (7-8), as described previously in operations of SITO mode. The output voltage during this mode can be driven by applying voltage balance on L2 same as in (7-5) and (7-6) as well.

7.4 Design of the proposed multiport power converter

This section will present the design of the proposed converter main elements and the selection of voltage levels for the PV, the battery and the SC-stack to enhance the performance and functionality of the proposed converter.

7.4.1 Selection of input voltages

Although the proposed converter can provide a wide operating range for the input/output voltages as described in the previous sections, attention should be paid when selecting the voltages levels for its inputs to maximize the performance. At a desired output voltage (Vo) that is defined by the application, the maximum and minimum voltages of the SC-stack can be selected as 2Vo and 0.5Vo respectively, according to the considerations presented in section 7.2. This enables a better utilization of the energy capacity of SC-cells and achievement of the higher *USE* as described earlier which minimizes significantly the weight of SC-stack with direct implication in the overall system weigh. On the other hand, as the current ratings of the inductors L1 and L2 are influences by the duty cycle of the switch S5 (affected by the ratio V_{pv}/Vo) at given charging/discharging power for battery and SC, the minimum voltage of the PV-array can be selected at ($0.5Vo$) to ensure that duty cycle will not exceed 50% to minimize inductors current ratings.

The maximum voltage of the PV-array should be selected to be lower than Vo but at a reasonable level effected by the minimum voltage of the battery and SC-unit in order to ensure the controllability of L1 and L2 currents at MPPT. However, when the PV-array voltage became more than SC voltage, S5 duty cycle would be d_{5min} causing the PV-array to operate away from MPP but only for a short time needed to charge the SC-stack until its voltage reaches the PV-array voltage. Since the battery is characterized by a higher energy rating has significantly

flatter voltage vs SoC dependency, the maximum voltage of the PV-array should be selected considering the minimum voltage of the battery only as it requires longer time to change which otherwise will cause poor capturing of the available energy from the PV-array.

The battery/SC HESS is usually utilizing high SE batteries based on Lithium-Cobalt or Lithium-Sulfur in conjunction with the SC. The minimum voltages for such batteries at the lowest SoC are 50-65% of their maximum voltages at the highest SoC [161, 162]. Accordingly, by selecting the minimum voltage of the battery to be Vo, the maximum voltage of the PV-array can be selected to be up to Vo, allowing the converter operating range to be defined by the red dashed area highlighted in Fig.7-12 that obtained based on equations (7-4) and (7-6). The voltage of the PV array is significantly affected by temperature, with a negative coefficient of 0.25%-0.33% /^{o}C depending on the utilized PV cell technology [16, 55].

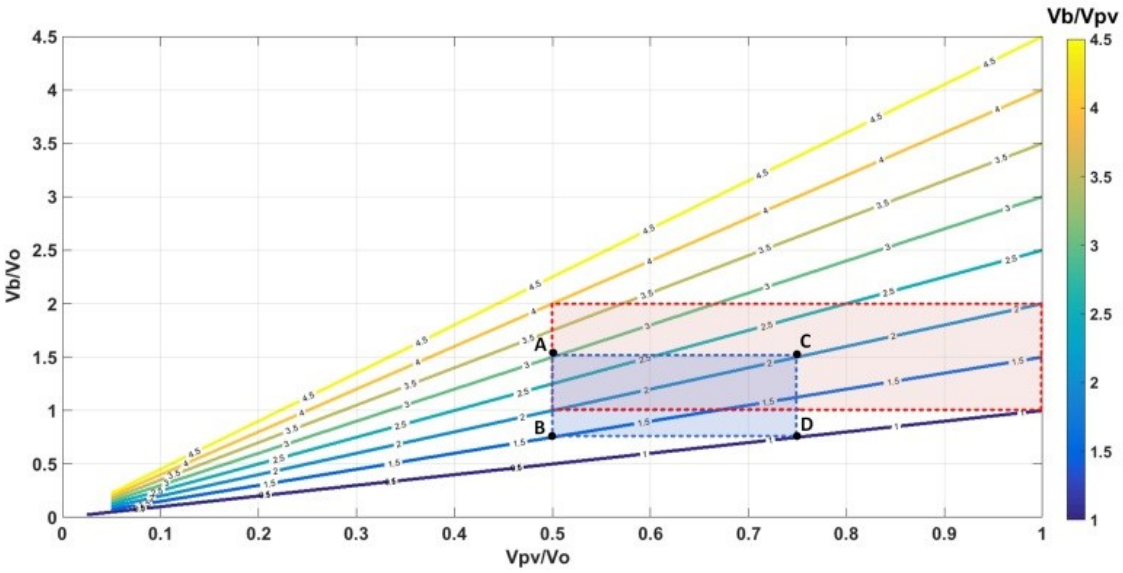


Fig.7-12 Interrelation of voltage ranges for the I/O ports of the proposed MPC

Considering satellite application, the array temperature increases 100^{o}C compared to its temperature during the several minutes just after return from eclipse as illustrated in Chapter 3 (Section 3.3). Accordingly the minimum array voltage at maximum array temperature reaches 50% of the maximum array voltage at minimum temperature. Considering maximum array

voltage (at cold temperature) designed at Vo, then the minimum array voltage will be (75% Vo). Based on these voltage boundaries of the PV-array which are marked on horizontal and vertical axis, an optimized operating range for the PV and battery voltages can be re-defined by the blue area (ABDC). The advantage of the this design is that the maximum voltage of the battery has been reduced by 25% compared to the previous design considering same output voltage which in turn reduces the voltage rating of the switches by the same ratio and requires less number of series connected battery cells reducing the complexity of its voltage monitoring and balancing circuitries.

7.4.2 Sizing of the inductors

In order to size the battery/SC side inductors (*L1, L2*), the current ripple of both inductors at the defined boundaries of the operating range for the battery and SC-stack should be considered. The boundary points of the operating range for the battery are highlighted in Fig.7-12 by (A, B, C and D). For point A and B, the PV array voltage is minimum (0.5Vo), whilst battery voltage is maximum (due to highest SoC) at point A and minimum (due to lowest SoC) at point B. On the other hand, at point C and D, the PV array voltage is maximum (0.75Vo), whilst battery voltage is maximum (due highest SoC) at point C and minimum (due to lowest SoC) at point D. The corresponding duty cycles for the battery and PV stages switches as well as the current ripple of the battery inductor (*L2*) at each point are shown in Table 7-1 and the corresponding voltage waveforms are shown in Fig.7-13.

In order to minimize the current ripple of the inductor L2, a phase shifted carrier modulation (PSCM) technique has been developed by implementing a phase shift angle of (θ^o) between the PWM carriers of the switches *S5* and *S3*. The angle should be adjusted based on the duty cycles in order to avoid the deadlock situations preventing power flow to/from the battery which can occur when $d_3=(1-d_5)$ and $\theta^o=d_5*360$. Therefore, in order to minimize the switching current

ripple in L2 as well as to avoid the deadlock situations, the phase shift angle for the proposed PSCM technique can be defined as:

$$\theta = (2d_5 + 0.25) \tag{7-11}$$

Table 7-1 Analytical formulas for the peak-to-peak current ripple in the battery side inductor (L2) at the boundaries of the operating range with and without using the PSCM technique

V_{pv} \ V_{batt}	1.5Vo	0.75Vo
0.5Vo	$d_3 \approx 0.33$ $d_5 = 0.5$ A $\Delta I\|_{\theta=0} = \frac{0.5V_O}{L_2 f_s}$ $\Delta I\|_{\theta=\frac{5\pi}{4}} = \frac{0.165V_O}{L_2 f_s}$	$d_3 \approx 0.67$ $d_5 = 0.5$ B $\Delta I\|_{\theta=0} = \frac{0.375V_O}{L_2 f_s}$ $\Delta I\|_{\theta=\frac{5\pi}{4}} = \frac{0.187V_O}{L_2 f_s}$
0.75Vo	$d_3 = 0.5$ $d_5 = 0.25$ C $\Delta I\|_{\theta=0} = \frac{0.5V_O}{L_2 f_s}$ $\Delta I\|_{\theta=\frac{3\pi}{4}} = \frac{0.25V_O}{L_2 f_s}$	$d_3 = 1$ $d_5 = 0.25$ D $\Delta I = \frac{0.187V_O}{L_2 f_s}$

As can be seen, with PSCM technique not implemented (θ=0), the maximum inductor (L2) current ripple (to be considered for the sizing of this inductor) occurs at points A and C. Implementing the proposed PSCM technique could significantly reduce the current ripple at these points. For point A, the current ripple is reduced by 67%, whilst it reduced by 50% for point B and point C. However, as the inductor should be sized based on the maximum current ripple (which is now occurs at point C), the reduction in the inductor size is limited to 50% compared to the case with size PSCM technique not implemented.

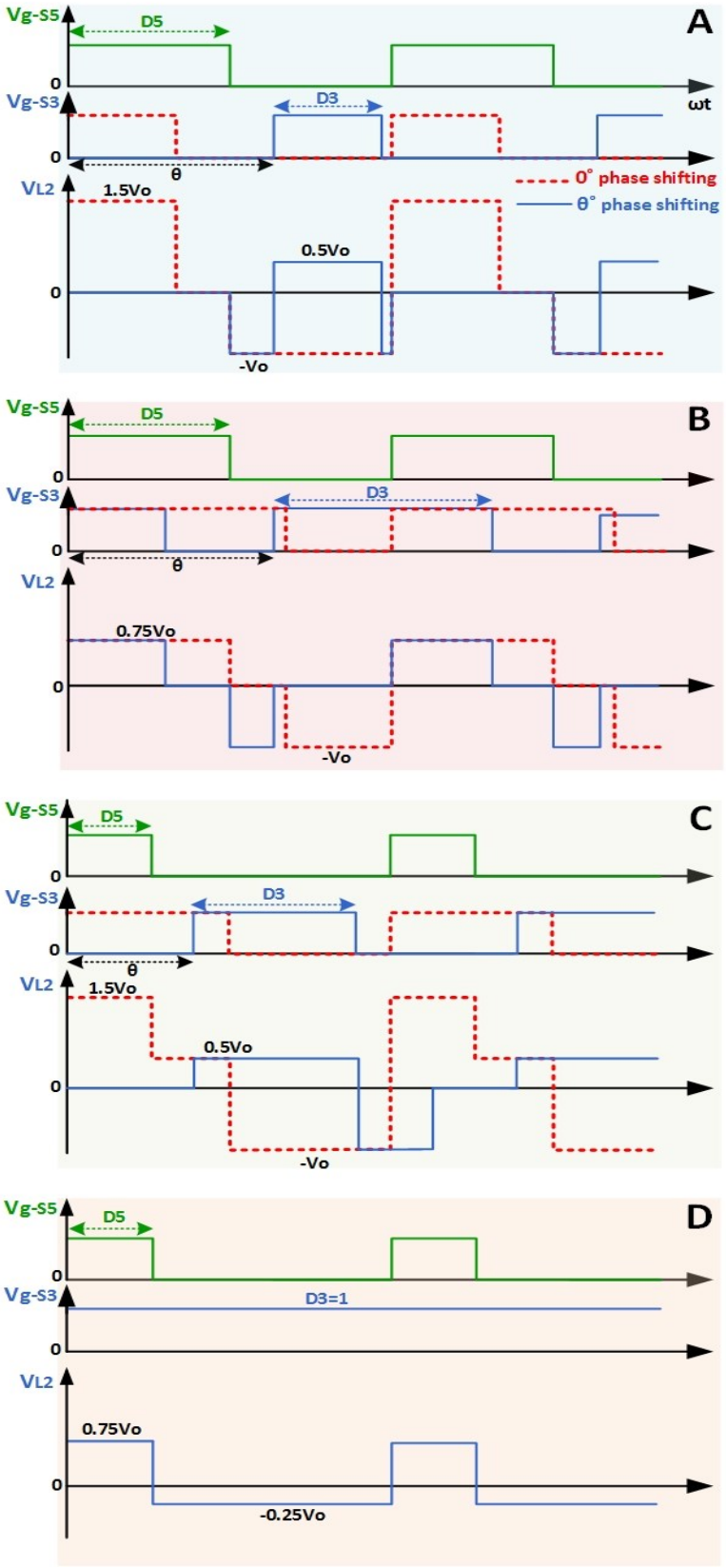


Fig.7-13 Relevant voltage waveforms for deriving the analytical model of the battery side inductor current ripple at the operation boundaries (A, B, C and D)

Similarly, the SC stage inductor ($L1$) current ripple can also be reduced by implementing the proposed PSCM technique. Table 7-2 summarizes the corresponding duty cycles for the SC and PV stage switches as well as the analytical derivation of the current ripple at each point whilst the corresponding waveforms are shown in Fig.7-14.

Table 7-2 Analytical formulas for the peak-to-peak current ripple in the SC side inductor (L1) at the boundaries of the operating range with and without using the PSCM technique

<table>
<tr><th>V_{SC} / V_{pv}</th><th>2Vo</th><th>0.5Vo</th></tr>
<tr><td>0.5Vo</td><td>d_1=0.25
A
d_5=0.5
$\Delta I\|_{\theta=0} = \frac{0.5V_O}{L_1 f_s}$
$\Delta I\|_{\theta=\frac{5\pi}{4}} = \frac{0.25V_O}{L_1 f_s}$</td><td rowspan="2">B
d1≈1
d5=0.5
$\Delta I = \frac{0.25V_O}{L_1 f_s}$</td></tr>
<tr><td>0.75Vo</td><td>d_1=0.375
C
d_5=0.25
$\Delta I\|_{\theta=0} = \frac{0.5V_O}{L_1 f_s}$
$\Delta I\|_{\theta=\frac{3\pi}{4}} = \frac{0.375V_O}{L_1 f_s}$</td></tr>
</table>

As can be seen, implementing the PSCM technique could reduce the maximum current ripple occurs at point A and point C. For point A, the current ripple is reduced by 50%, whilst it reduced by 25% for point C comparing the values of the current ripple without phase shifting. However, as the inductor should be sized based on the maximum current ripple (which is now occurs at point C), the reduction in the inductor size is limited to 25% compared to the case with PSCM technique not implemented (θ=0). When the voltage of the PV-array (at MPP) is $0.75Vo$ and Vsc is $0.5Vo$, the SC-stage will be forced to work at point B, which is away from the MPP,

until *Vsc* reaches *Vpv*=0.75*Vo*. Considering that the very small amount of energy/time is needed to reach this point, it can be considered that this is acceptable.

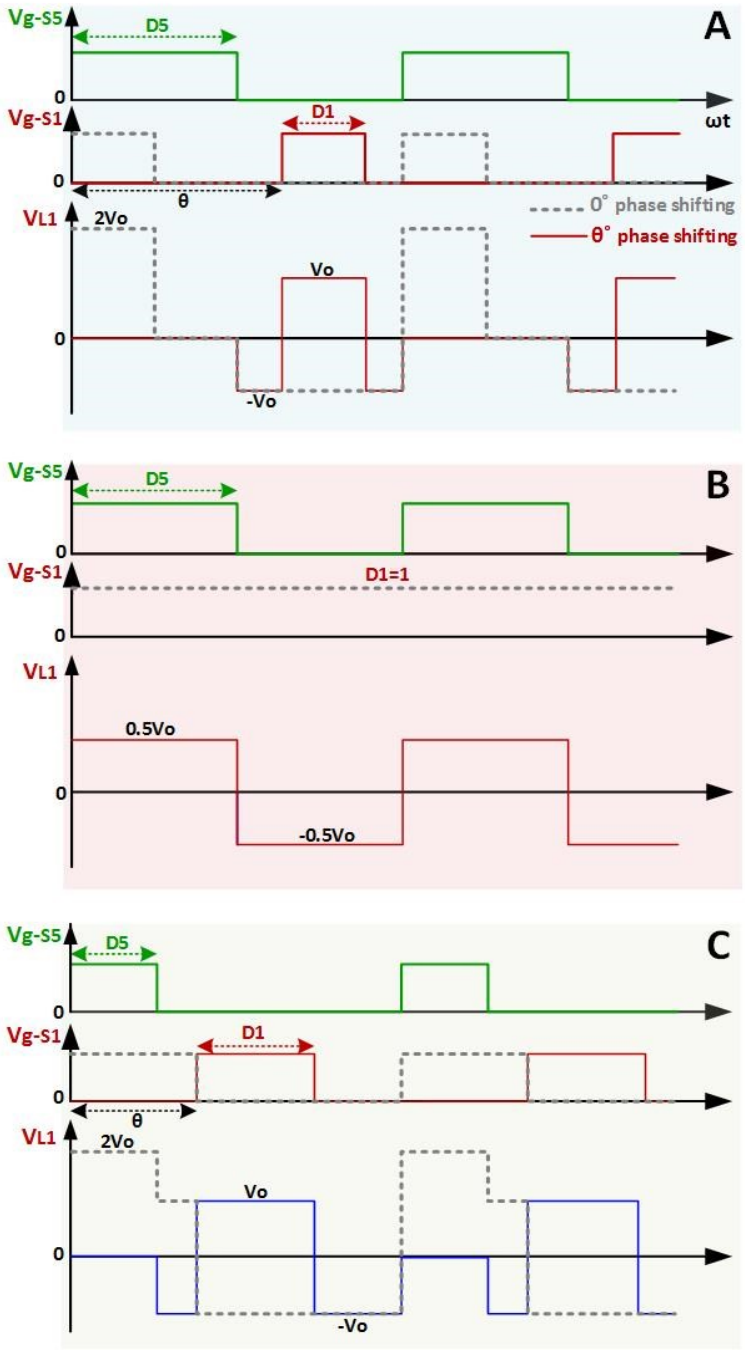


Fig.7-14 Relevant voltage waveforms for deriving the analytical model of the SC side inductor current ripple at the operation boundaries (A, B, and C)

7.5 The control structure of the proposed MPC converter

The main idea of the control strategy in HESS is that the SC-stack should support the high frequency power requirement whilst battery supports the low frequency power requirement. The simplest implementation is to use a low pass filter (LPF) to separate the low frequency power component which is converted into a reference current to the battery current control loop whilst the difference containing only the high frequency power component is converted into a reference current to the SC-unit control loop [163, 164]. In order to further reduce the current stress in the battery, a rate limiter has been considered in [165] to limit the battery current at the safe level. The control strategy of the proposed converter has been built based on this due to the limited current capability of the high SE batteries that are used in HESS.

As it can be seen in the control scheme of the proposed converter shown in Fig.7-15, with the PV stage controlled to extract maximum power available from PV array (MPPT), the converter output voltage PI-controller determines the total power to be supplied to/from both battery and SC-stack and accordingly total current (I_t) to be supplied from both battery stage inductor current (I_{batt}) and SC-stack stage inductor current (I_{SC}). The total current is then separated into low and high frequency components by means of a LPF. The reference current for battery stage inductor (I_{b_R}) is obtained by applying a rate limiter to the low frequency current component to limit the battery charge/discharge rate based on a specified value assumed, then I_{b_R} is passed to the current control loop which generates the PWM signals for the switches S3 and S4. On the other hand, reference current for the SC stage inductor (I_{SC_R}) is obtained by subtracting (I_{b_R}) from the total current (I_t) and considering the uncompensated battery power caused by the error in the battery current due to the slow dynamics, then I_{SC_R} is given to SC stage inductor current control loop which generates the PWM signals for the switches S1 and S2. The gains of the PI controllers are selected to avoid interaction between the control loops and fine-tuned based on trial and error until reached an accepted performance for the converter. The controller

parameters selected such that the global bus voltage controller were (*kp*=7,*ki*=20), whilst the parameters the battery current controller were (*kp*=0.1,*ki*=10) and the parameters of the SC stack current were (*kp*=0.05,*ki*=10) . However, the future work will consider the proper design of these control loops based on the analytical model of the converter.

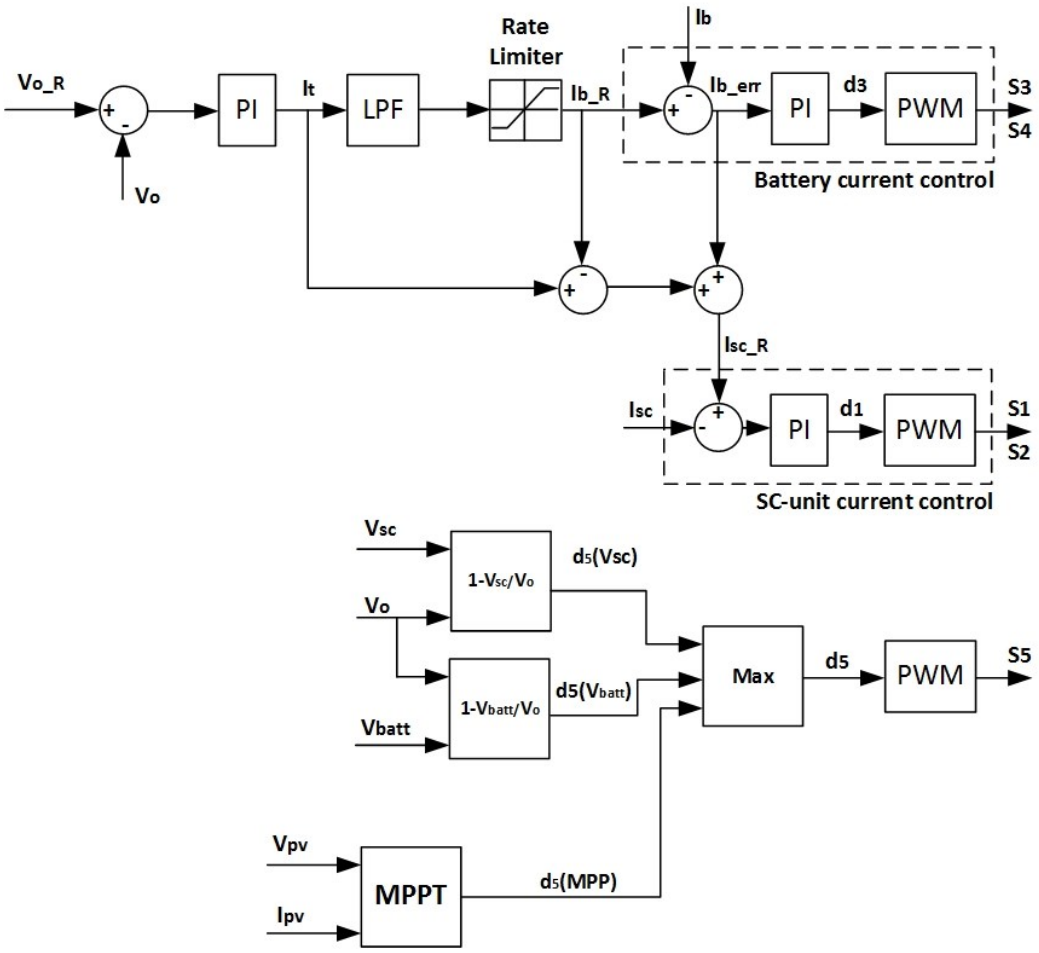


Fig.7-15 Control scheme of the proposed multiport hybrid storage converter

The switch S5 has two shared functions, one is to ensure the operating point of the PV-array at MPP which controlled by the MPPT. The second function with higher priority is to ensure the controllability of the currents of the SC and battery stages inductors (*L1, L2*) which is affected by the voltages of SC-stack and battery as indicated in (7-8) and (7-10), derived earlier. Accordingly, the duty cycle of S5 is selected as the bigger out of the two values obtained based on the two shared functions. For example, when the PV power is not available, assuming the

battery voltage is V_{batt}=0.75V_O and this is less than the voltage of SC-stack, the duty cycle obtained from the MPPT is $d_5(MPP)$=0, whilst the duty cycle value as obtained according to battery voltage is $d_5(V_{batt})$=0.25, therefore the duty cycle of S5 will be set to d_5=0.25. However, if the SC-stack voltage is lower (V_{SC}=0.5Vo) then the duty cycle obtained according to SC-stack voltage $d_5(V_{SC})$=0.5, which requires that this duty cycle of S5 to be selected (d_5=0.5).

7.6 Evaluation of the proposed MPC by Simulations

In order to evaluate the performance of the proposed MPC under different conditions, a detailed simulation model for the converter has been developed under the PSIM® simulation environment and this is illustrated in Fig.7-16. The PV model used is based on the developed model in Chapter 3 (Section 3.3).

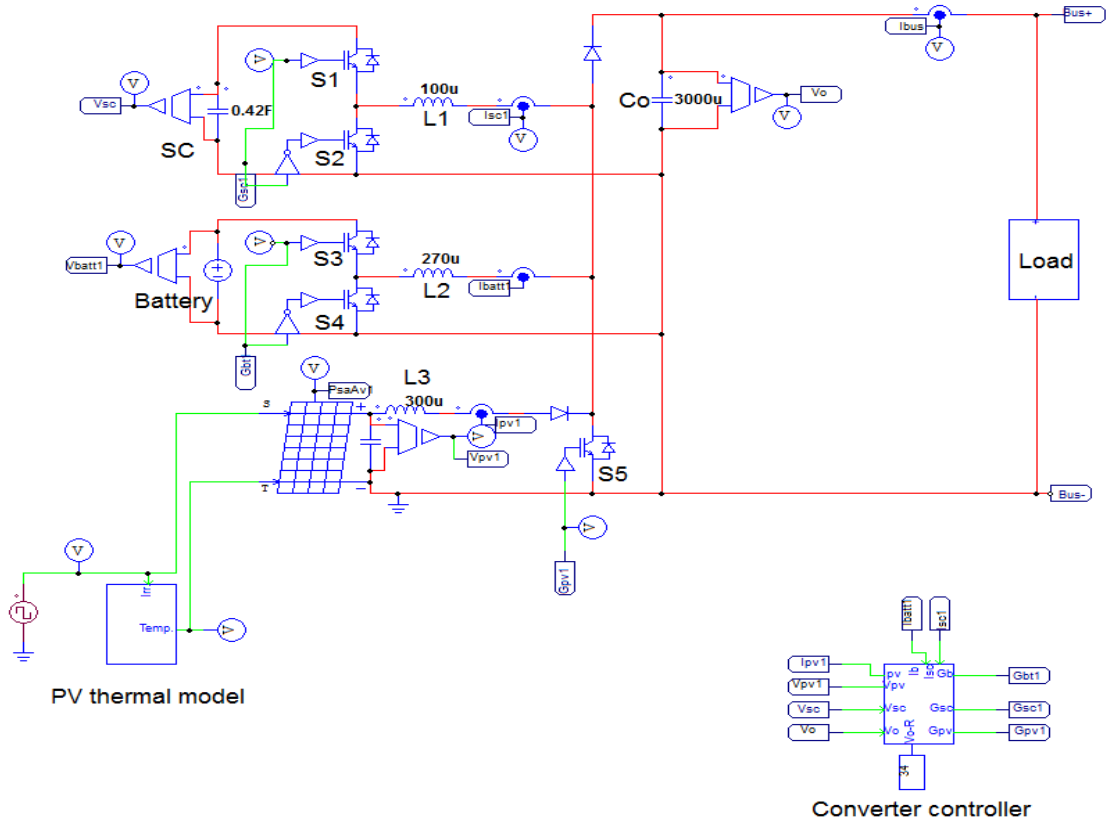


Fig.7-16 Simulation model for the proposed converter

7.6.1 Evaluating the MPPT for the PV-array

The MPPT functionality of the proposed MPC for the interfaced PV-array under varying environmental conditions has been simulated. Considering the satellite application, the irradiance under sun-pointing orientation of the PV-array is nearly constant whilst the PV array temperature changes significantly and rapidly (100^{o}C change during the first 10 minutes just after return from eclipse) as described earlier in Chapter 3 (Section 3.3). As a long simulation time would be needed to show the full change in PV-array temperature, especially when a simulation step of 1μs is required to simulate the converter switching at the switching frequency of 10kHz, the simulated thermal behaviour of the PV-array has been accelerated by a factor of 100:1 by reducing the thermal capacitance of the array. As it can be seen in Fig.7-17, the voltage of the PV-array initially was 23V when the PV array temperature was -60^{o}C that is corresponding to a return from eclipse. As the array heats up, its voltage decreases to 15V and consequently the available power reduces from 450W to 300W. During this transition, the converter control maintained the bus voltage at its desired value (34V) as well as tracking the varying MPP to maintain the extraction of maximum power available from the PV-array even under the rapid changing in the MPP caused by the rapid change in the temperature. The implemented MPPT was based on a simple incremental conductance (IncCon) algorithm [166]. The power available from the PV-array is higher during cold temperature, exceeding the load required power and also the battery charging power limit, therefore the excess has been directed to charge the SC-unit. Whilst delivering constant load power of 150W, it can be seen that as the extracted power from the PV-array decreases (as its temperature increases), the excess power used to charge the SC-module decreases.

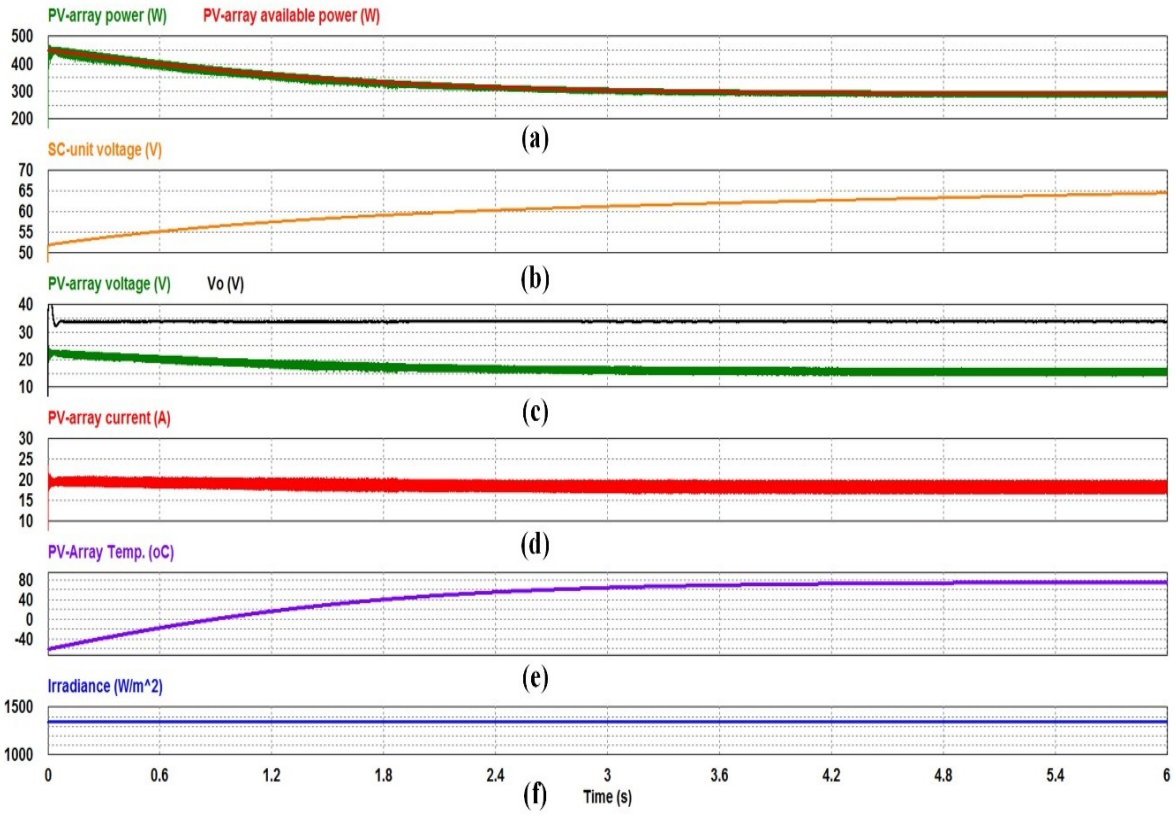


Fig.7-17 Simulation of MPPT operation of the proposed converter: (a) PV-array available and extracted powers (b) SC-stack voltage (c) PV-array and output voltages (d) PV-array current (e) PV-array temperature (f) Irradiance at the PV-array.

7.6.2 Performance of the converter under peak power loads

The performance of the proposed converter under peak power demand from the load that exceeds both the PV-array available power and the discharging power limit of the battery which consequently prompts to the utilisation of the SC-stack to provide most of this peak power are evaluated and the simulation results are shown in Fig.7-18. The simulation started with a load power consumption of 150W whilst the generated power from the PV-array was 180W. Accordingly 30W was directed to the battery which was below its charging power limit (here this is set to 120W) and consequently the SC-stack was not charging. At (t=0.5s), the load

power consumption has been increased to 950W which exceeds the power available from the PV-array and consequently the battery has to be discharged but the necessary power is well above the assumed discharging power limit. Accordingly, the SC-stack started to discharge to supply the excess required power causing its voltage to decrease from 60V to 17V at the end of the load power peak. Whilst the output voltage marinated under control at 34V.

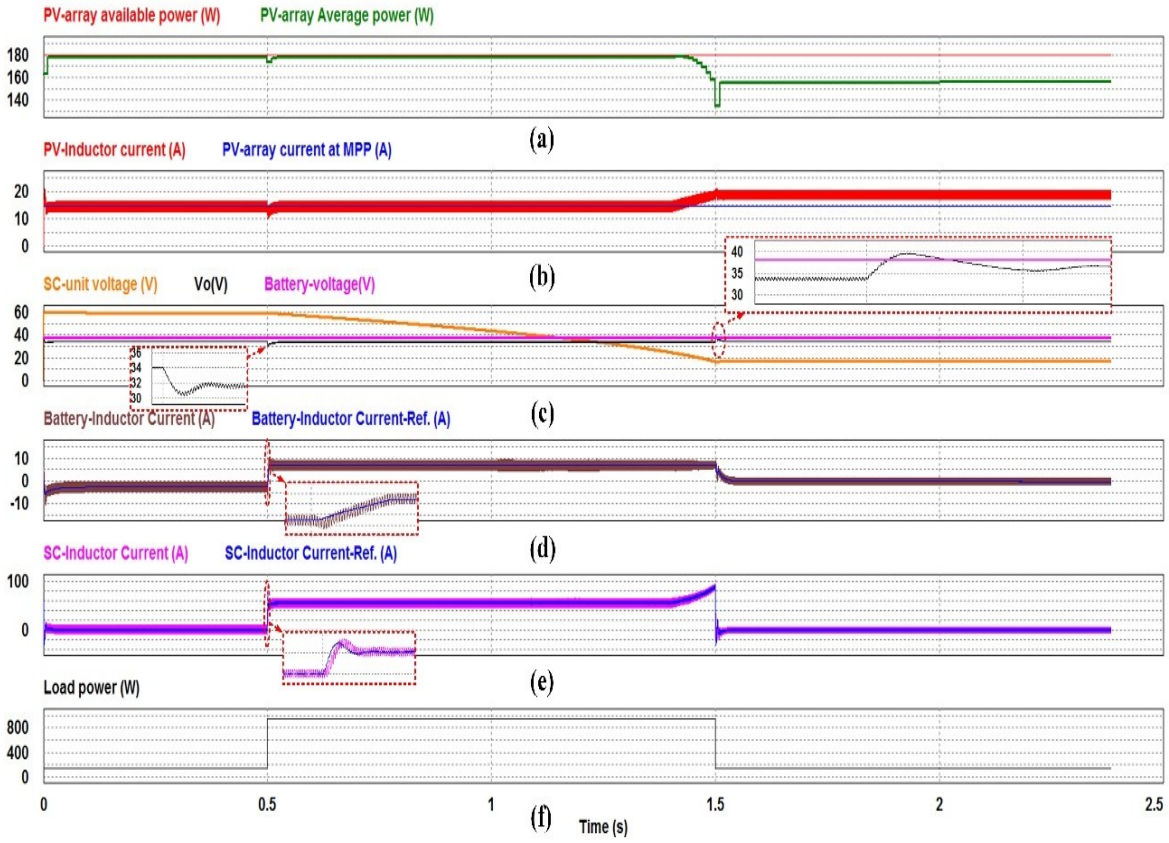


Fig.7-18 Simulated performance of the proposed converter under peak power loading: (a) PV-array available and extracted powers (b) PV-stage inductor current and PV-array current at MPP (c) SC-stack, battery and output voltages (d) Battery stage inductor actual and reference currents (e) SC stage inductor actual and reference currents (f) load power.

As it can be seen, once the voltage of the SC-stack drops below the output voltage, the duty cycle of the PV-switch (S5) has been controlled according to the SC-unit voltage based on (7-8)

which overrides the operation of the MPPT causing the PV-array to work away from MPP (at t=1.4s). Therefore, in order to resume the operation of the MPPT again, at the end of the power peak, the higher level controller should push the SC-unit charging again until its voltage reaches the PV-array voltage, however this operation is not simulated here. The dips in output voltage occurred at the start and end of the power peak can be eliminated by increasing the size of the output capacitor according to the required energy during the transients of the battery/supercapacitor inductor currents as well as the maximum accepted percentage of the dip in the output voltage.

7.6.3 Performance of the converter under PV-power disturbance

The simulated performance of the converter under the disturbances caused by the availability/un availability PV-array power during sun/eclipse durations is shown in Fig.7-19. As it can be seen, the converter could perfectly maintain the output voltage constant at the desired value of 34V throughout the test although a large disturbances has been introduced to its power input by the disturbing the availability of PV power. The PV-array power dropped to zero at (t=0.5s), and accordingly the battery switched from charging to discharging, whilst the SC-stack discharged for a very short duration to compensate the high frequency component of the power only, after which it returned to idle state as the load power level was below the battery power limit. Another disturbance has been introduced at (t=1s) where the PV-array started to supply power again, and accordingly, the battery switched from the discharging to charging.

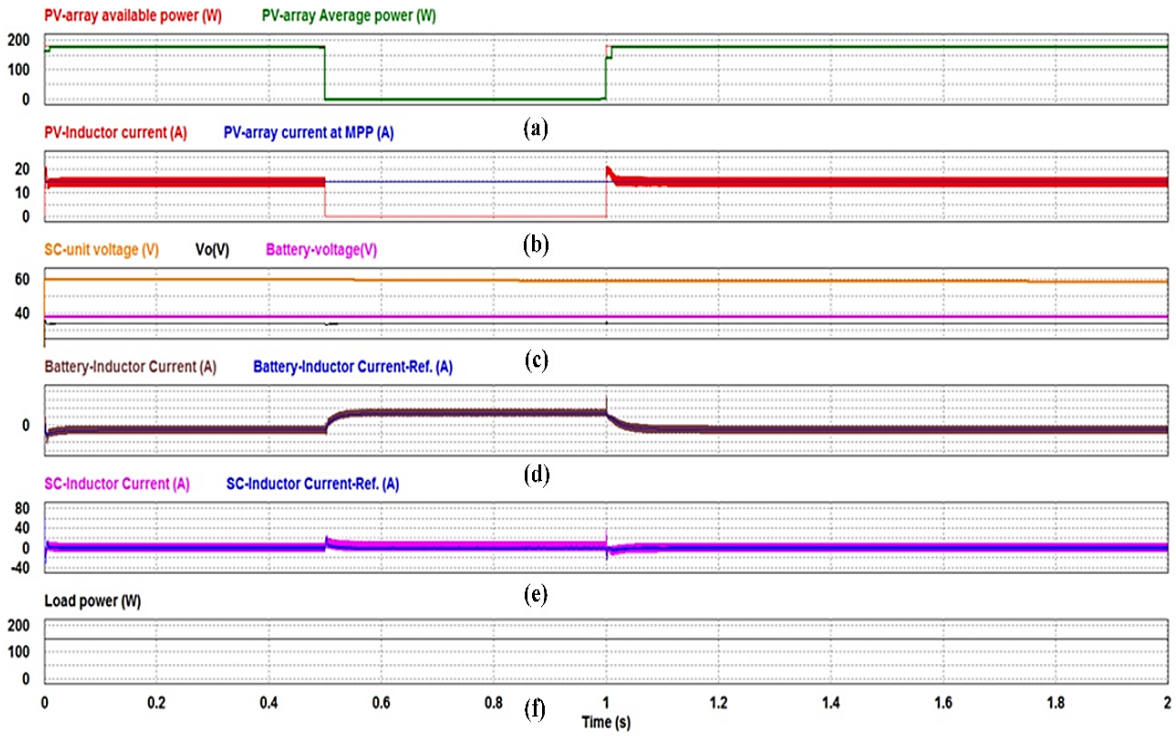
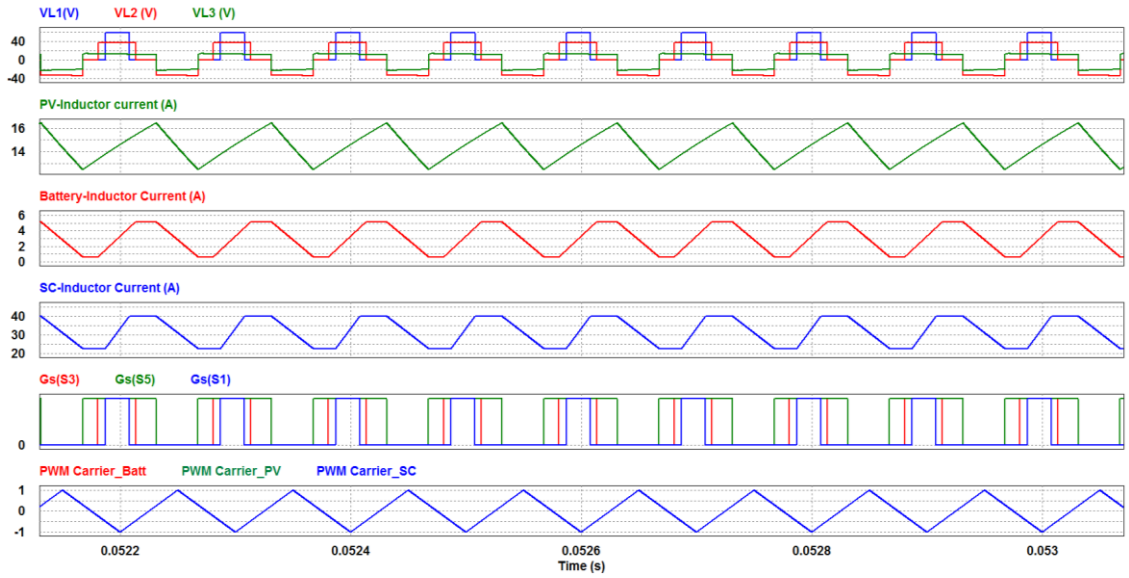


Fig.7-19 Simulated performance of the proposed converter under PV power disturbances(a) PV-array available and extracted powers (b) PV-stage inductor current and PV-array current at MPP (c) SC-stack, battery and output voltages (d) Battery stage inductor actual and reference currents (e) SC stage inductor actual and reference currents (f) load power.

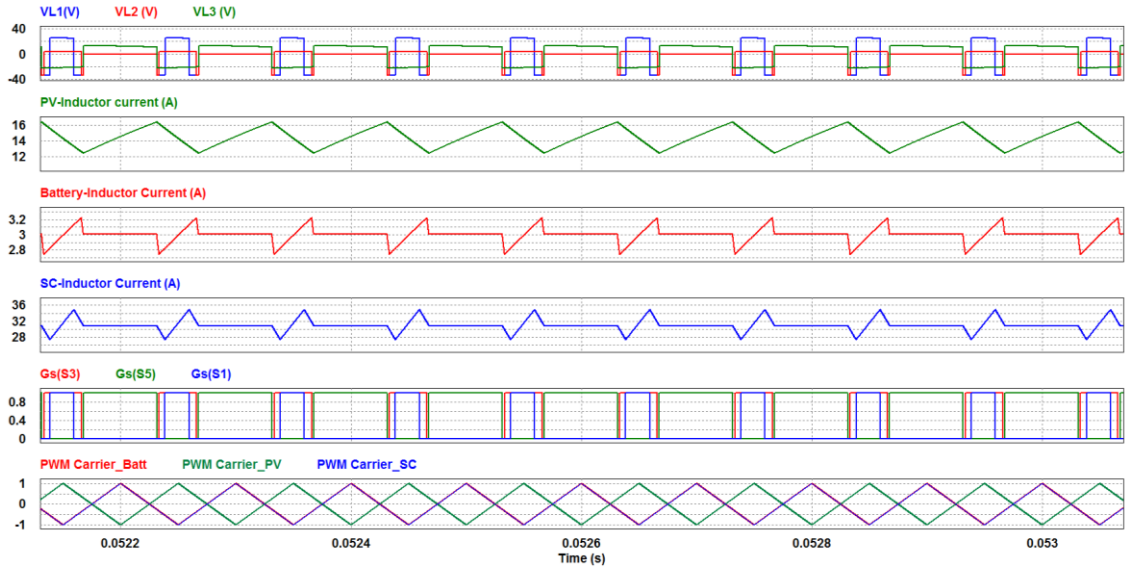
7.6.4 Operation with Phase-shifted carriers modulation

The simulated operation under the proposed PSCM technique described earlier is shown in Fig.7-20. In Fig.7-20a, it can be seen that all PWM carrier signals are in phase (0^o-phase shift) and consequently, the gating signals of the SC-unit switches (Gs(S1)), battery switches (Gs(S3)) and PV-switch (Gs(S5)) also are in phase. Under this condition, the maximum peak-peak current ripple in the SC-inductor (L1) was 18A, whilst in the battery-inductor (L2) it was 4.5A and in the PV inductor-current (L3) it was 4A. Applying the PSCM technique with an 180^o-phase shift between the PWM carriers of battery and SC PWM signals in one hand and the PV signal PWM signal in the other hand, the battery and SC inductors current ripples are reduced

significantly. As it can be seen in Fig.7-20b, the maximum peak-peak current ripple for the SC stage inductor is been reduced from 18A to 8A and the battery stage inductor current ripple is reduced from 8A to 0.5A compared to the 0°-phase shift reference, whilst the current ripple of the PV-inductor is un affected by the use of PSCM.



(a)



(b)

Fig.7-20 Simulated performance of the PSCM technique for proposed converter with: (a) 0° phase shift and (b) PSCM technique with 180° phase shift.

7.7 Experimental evaluation

In order to validate the proposed converter, an experimental 500W/30V integrated power system experimental prototype with hybrid energy storage is built. The system is based on the proposed converter topology that is interfacing a Li-ion energy battery, a SC-stack as well as programmable power supply that acts as a PV-array, whilst an electronic load is used to emulate system loads. The digital control platform is the same one used with the proposed MPPC that described in Chapter 5 (Section5.5.1). The complete experimental system is shown in Fig. 7-21 with the detailed specifications listed in Table 7-3.

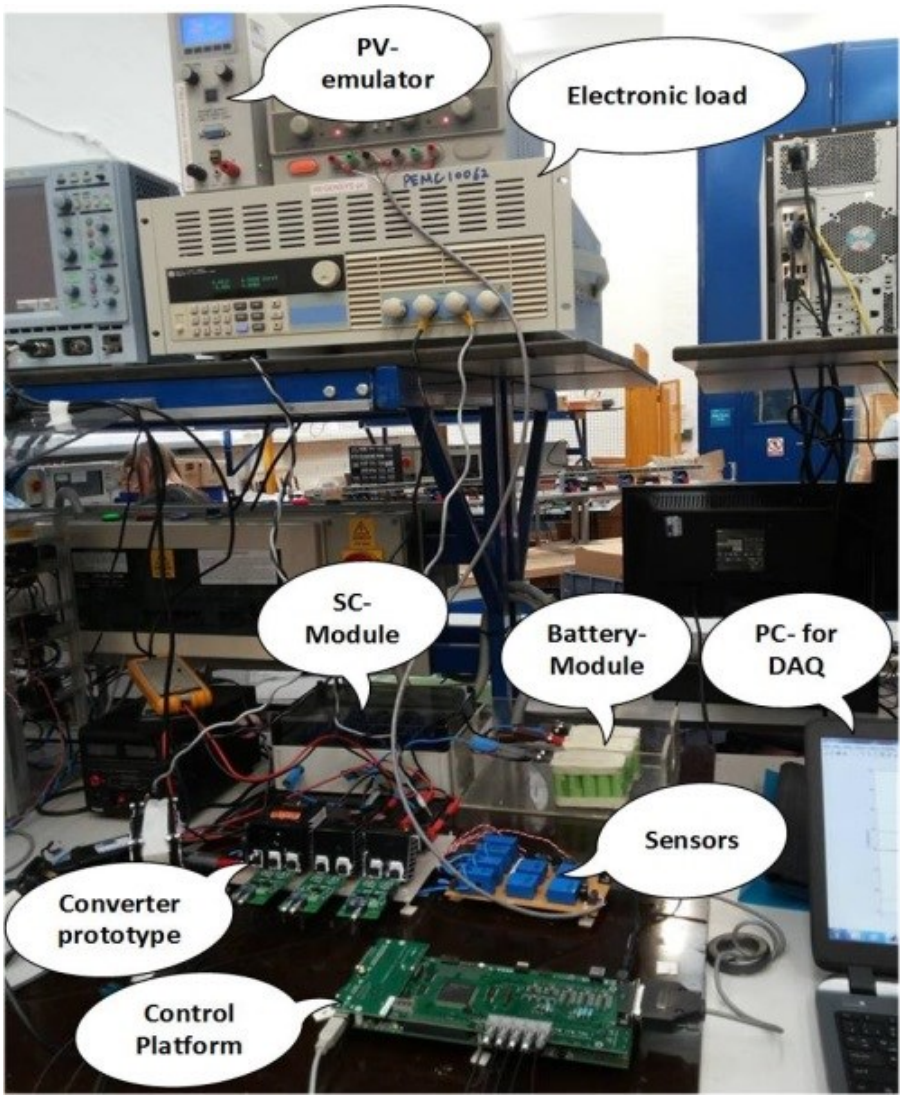


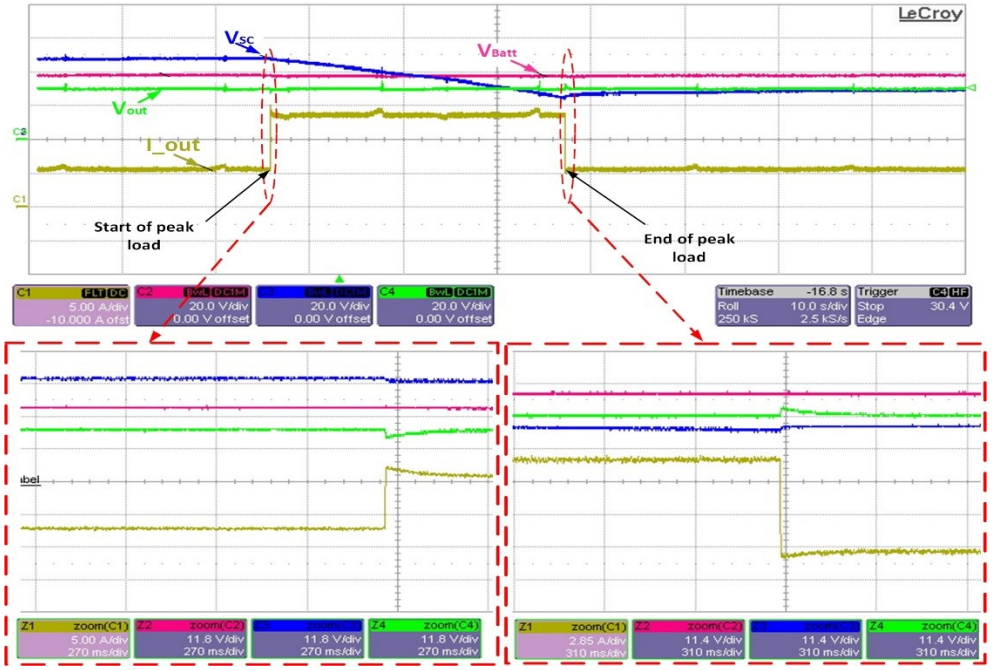
Fig. 7-21 Experimental setup for validating the proposed converter

Table 7-3 Technical specification of the experimental setup

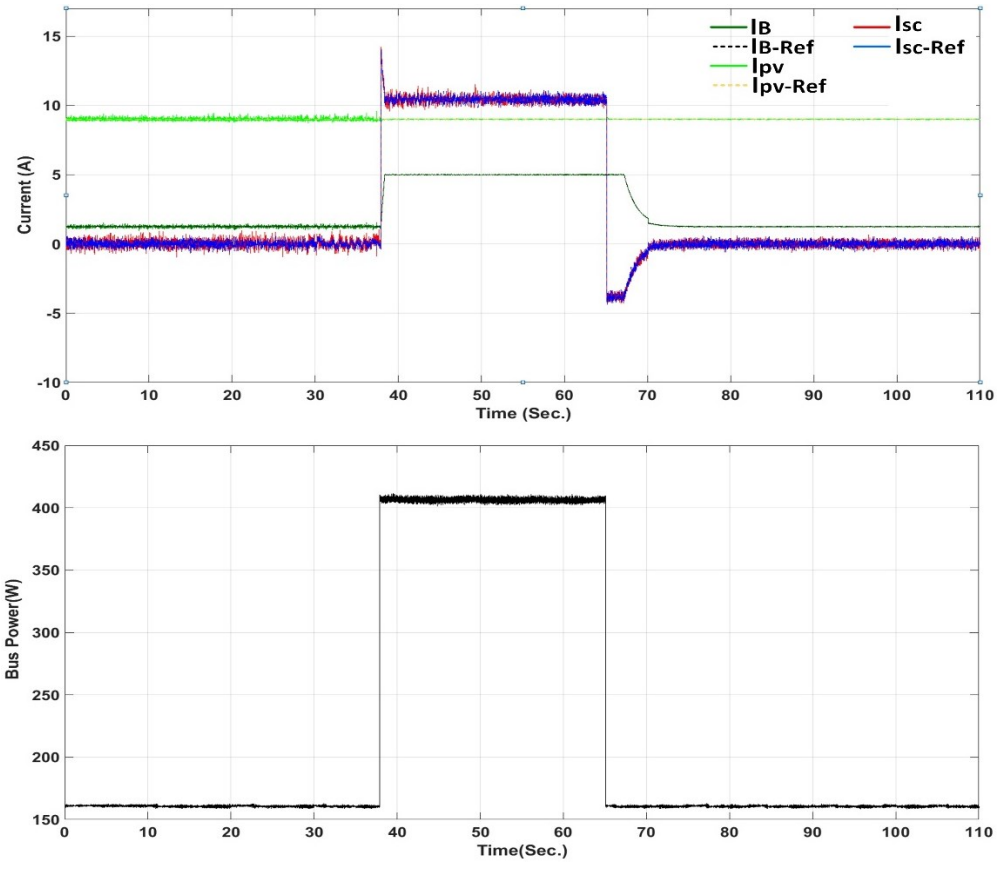
Type/Name	Rating/Specifications
Battery module	42V/6Ah based on Panasonic NCR18650B cell with V_{max}=42V and V_{min}=25V
SC-stack	8F/60V based on AVX SCCW45B107 cell with V_{max}=60V and V_{min}=15V
PV-array emulator	Vpv_{MPP}= (15 - 22.5)V, Ipv_{MPP}=(6-9)A
Electronic load	150V, 1.8kW
SC-unit inductor (L1)	120µH
Battery inductor (L2)	240µH
PV inductor (L3)	120µH
DC-link capacitor (C_O)	3000 µF
MOSFETs	IRF3710
Switching frequency (Fs)	10kHz

7.7.1 Evaluating the handling of a peak power loading

In Fig. 7-22, the operation of the proposed converter at peak power loading was investigated. Initially, at a constant power load of 160W which is slightly more than the PV available power, the required power from the energy storage was small. The battery inductor current was (≈ 1A), corresponding to a battery discharging power below the imposed limit, and accordingly the SC-stack current is zero as it can be seen in Fig. 7-22b. At (t=38s), a step change in the load has been applied causing the required power from the energy storage to increase significantly. Accordingly, battery stage inductor current reached its imposed limit (5A) whilst the SC stage inductor current increased to (≈11A) to compensate for the required extra power. This causes the voltage of the SC-stack to decrease significantly from 50V at the start of the power peak down to 22V at the end of the peak at (t=65s), as it discharged most of its stored energy as can be seen in Fig. 7-22a.



(a)



(b)

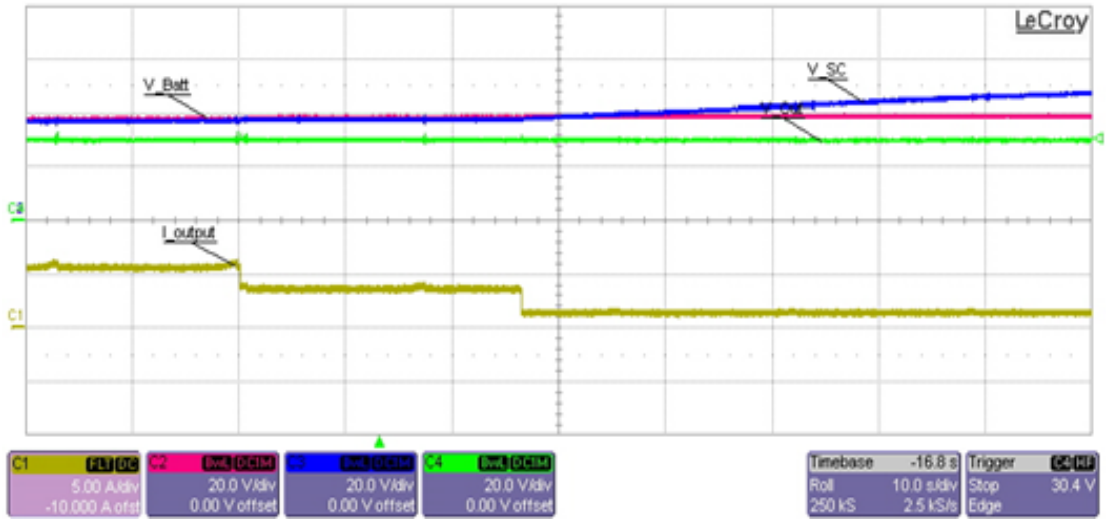
Fig. 7-22 Experimental results of the proposed converter during peak power loading operation: (a) Battery, SC, output voltages and output current measurements captured from oscilloscope (b) Battery, SC, PV currents and bus power measurements captured from the control system.

7.7.2 Evaluation of converter operation under load changing

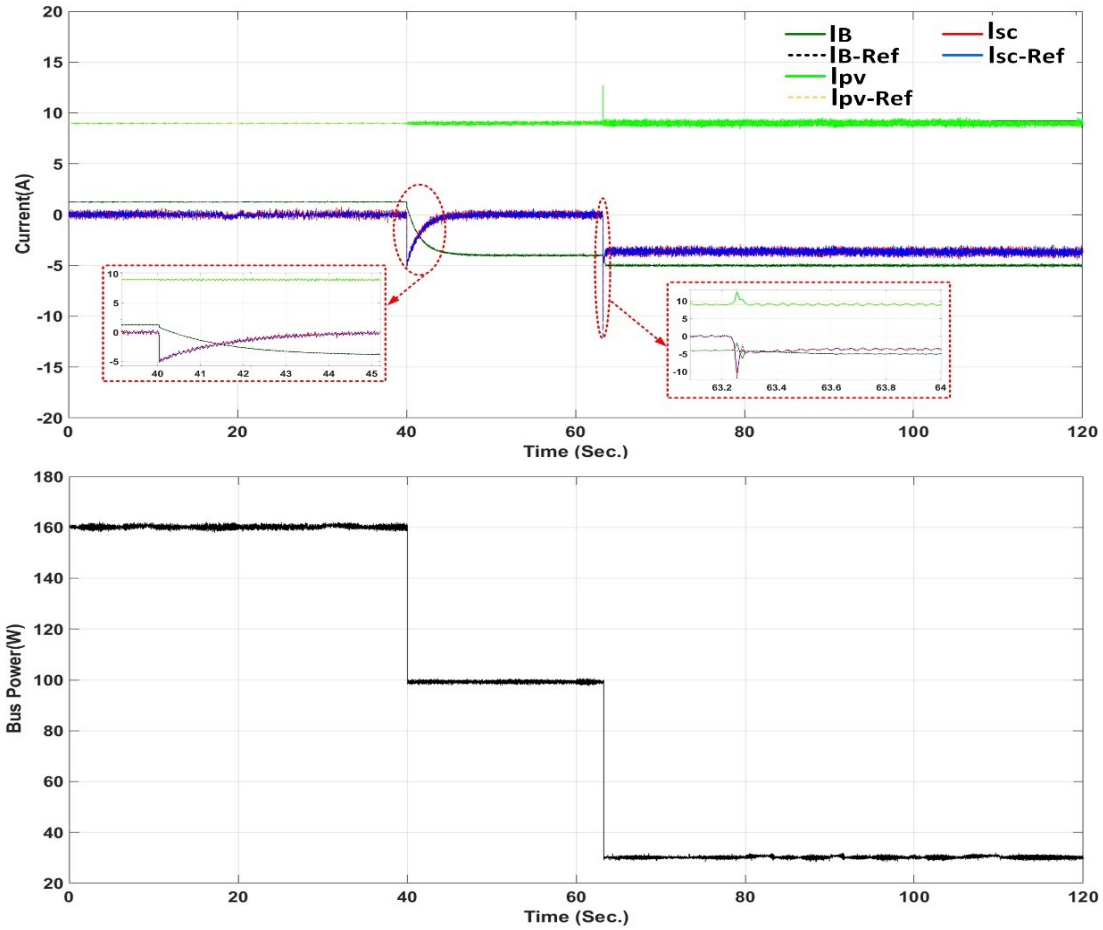
In Fig. 7-23 the performance of the proposed converter under different load changing scenarios was investigated. The test is starting with a constant power load of 160W which forced the battery to discharge in order to supply the excess power. The supplied power from the battery was small and resulted in a battery inductor current of (≈1A) and this lasts until the load power is reduced to 100W at (t=40 s). Accordingly, the extra power has directed to charge the battery resulting in a battery inductor current of (≈ -4A). As this current is below the battery current limit (assumed to be 5A), the SC-stack was charging during the transient only, then set back to zero after the battery inductor-current reached its reference value. In response to a significant reduction in the load power at (t=63 s), the SC-stack has to be charged a power during the transient period as well as part of the power during the short duration where the power exceeds battery charging limit, so the battery inductor-current is held at its maximum limit and the extra excess power is directed to charge the SC-stack.

7.7.3 Evaluation of converter operation under PV power disturbances

In Fig. 7-24, the performance of the converter under the disturbances caused by the sudden availability/unavailability of the PV power was investigated. Initially, the load power consumption was 70W which is below the PV available power (≈155W). Accordingly, the PV array was supplying the power required for the load and charging also battery with the excess. The battery inductor current was ≈ -6A until the PV power was removed at (t=30 s) when the battery started to discharge to supply the load power until the PV power becomes available again at (t=70 s). It can be observed that due to low power load, the battery current did not exceed its limit (here assumed to be 10A) so the SC-unit compensated only the higher frequency power component of the load power during the transient period.

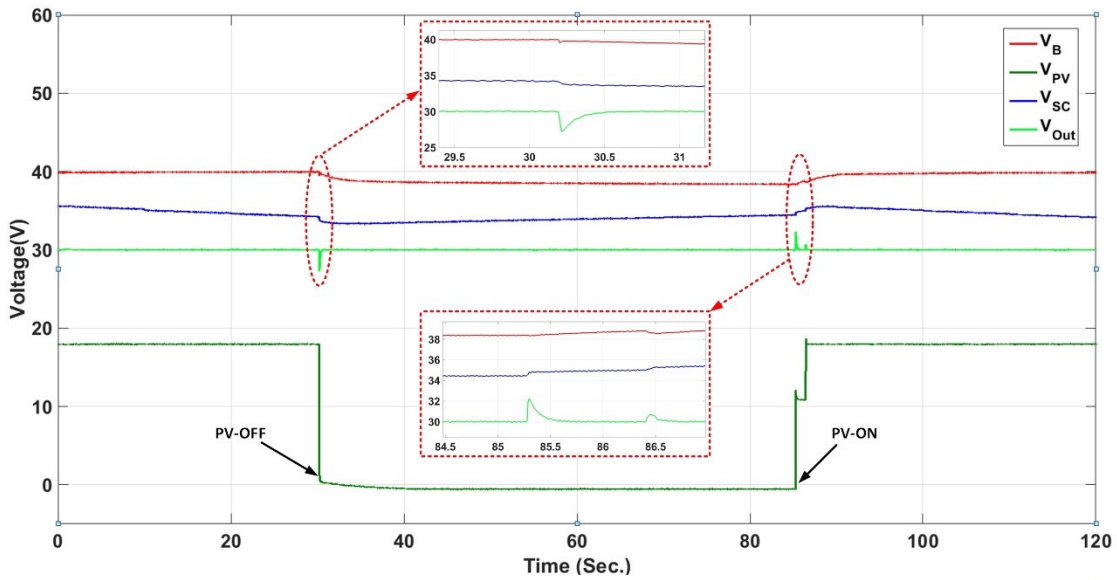


(a)

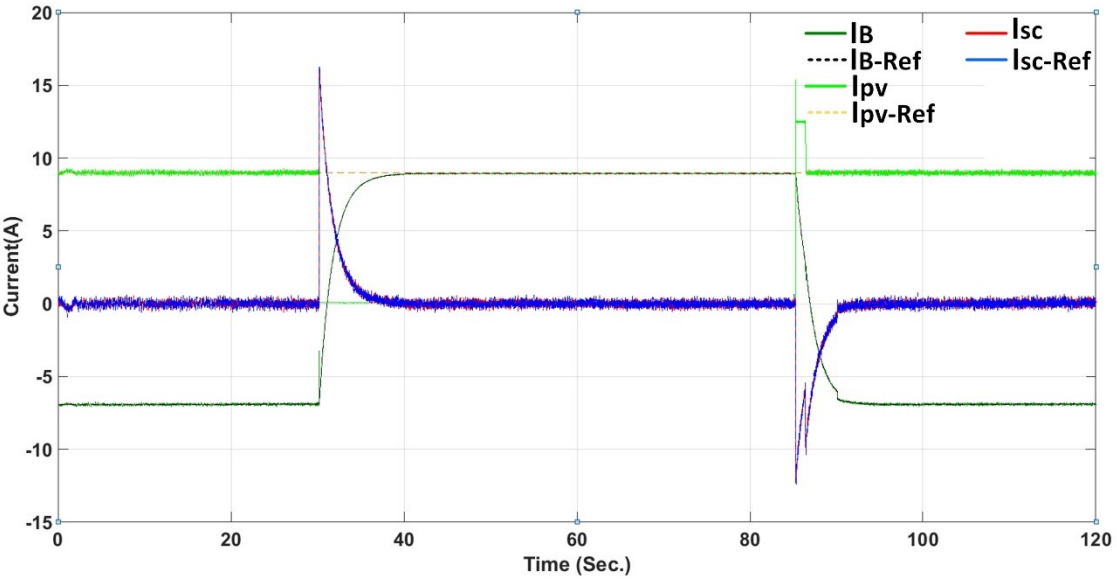


(b)

Fig. 7-23 Experimental results during different loading scenarios with:
(a) Battery, SC, output voltages and output current measurements captured from oscilloscope
(b) Battery, SC, PV currents and bus power measurements captured from the control system



(a)



(b)

Fig. 7-24 Experimental results during disturbances in PV power captured from the control system: (a) battery, SC-stack, PV emulator and output voltage measurements (b) battery, SC-stack and PV measured currents and their references

Summary

In this chapter, a new multiport converter topology for interfacing the photovoltaic array with a battery-supercapacitor hybrid energy storage to power bus has been proposed. The proposed converter provides two buck-boost ports for interfacing with the battery and the supercapacitor units and one boost port for interfacing with the PV array. The buck-boost voltage capability of the supercapacitor port allowed a 20% reduction in the size of the supercapacitor stack compared to a conventional topology that used to interface supercapacitors, considering the same energy capacity. A phase shifted carries modulation technique has been proposed which has been demonstrated analytically and in simulation that it allowed further reduction in battery and supercapacitor inductors sizes. The performance of the converter has been experimentally tested on a reduced scale fully functional prototype. The results validated the functionality and the performance of the proposed converter and its added features including the wide range of supercapacitor voltage variation to allow for the supercapacitor size reduction.

The proposed converter can be implemented in a modular architecture to construct a modular multiport converter similar to the one proposed in Chapter 5. This topology can provide a wider operating output voltage range compared to the topology used as the building block of the MMPC that was investigated.

Chapter 8. Conclusions and Future Work

8.1 Conclusions

In this research a new modular architecture for satellites power system has been investigated based on a proposed converter. Compared to conventional centralized architectures, the proposed architecture does not require series connection of a large number of battery/PV cells in a single string, which in case of faulty/weak cells causes poor utilization of available PV energy and battery capacity due to the limitations introduced by the these cells. This has been achieved by developing a novel modular multiport converter that consists of a number of multiport power modules interconnecting a group of low voltage PV and battery modules through multi input ports, whilst the output port of all modules are series connected to produce the high voltage power bus that powers the payloads. The modular structure of the proposed converter provides many advantages.

I) Maximum utilization of PV available power and battery available capacity is achieved even when a weaker PV/battery cell situation develops, as this will only affect their corresponding power module and with the proposed converter, a power mismatch between modules can be handled with minimum impact on overall available power compared to the conventional approach where the overall power/storage capability of the PV/battery system is significantly affected).

II) Secondly, the voltage stress of the power switches is reduced as the number of power modules increases for a fixed total number of PV/battery cells defined by energy/power requirements and consequently the parasitic resistance/capacitances of the low voltage switches are reduced with the potential to improve the overall system efficiency, as long as the reduction factor for parasitic resistance/capacitance of the switch is more than the number of series connected power modules.

III) Fault-tolerant operation of the power system can be inherently achieved by simply bypassing a faulty module and increase the power share of the healthy modules to compensate for the missing power.

IV) The utilization of battery/PV modules with different characteristics is facilitated without compromising the full mission, which can allow for the demonstration and real mission validation of the capabilities of new battery/ PV technologies on-board satellites.

V) The proposed converter topology enabled a modular design for the power system, which can be easily reconfigured and reused for a variety of mission requirements with minimal redesign effort.

Although increasing the number of power modules for the proposed converter could provide better utilization of the battery capacity and PV power as well as enhancing the fault-tolerant capability of the power system, it increases the system complexity by the increasing number of required control loops, the associated feedback measurements and the PWM generation. Therefore, the selection of the number of power modules is a trade-off between efficiency, complexity, and maximum utilization of battery capacity and available power from PVs as defined by the power system specification.

The applications of the proposed converter is not limited to space/satellite power system applications, and it can be also implemented in terrestrial applications that require PV-battery power systems or when considering the utilisation of mismatched second life batteries (battery retired from electric vehicles) which are now receiving considerable attention.

The behaviour and the control structure of the proposed converter has been analysed and its performance has been characterised via simulations then a prototype demonstrator designed at a relevant voltage and power range has been developed and validated by experiments based on three power modules. The experimental results showed the performance of the proposed

converter confirming the expected benefits including the capability to achieve battery balancing following a capacity mismatched between the battery modules and/or a power imbalance between PV modules. Also, the fault-tolerant operation of the proposed converter has been tested by a simulated failure of one of the three power modules, whilst the converter was shown to be able to maintain the bus voltage at 96% of its designated value due to the limitations introduced by the maximum possible output voltage of the power module which is lower than the voltage of battery module.

This thesis also investigated the different design options for implementing the energy storage system considering a specific load power profile that contain a high peak power pulse, several order of magnitude larger than the average power, which is the case for a small satellite power system with a radar imaging payload. The investigation considered different energy storage devices including different types of Li-ion batteries, Li-ion capacitors (LIC) and Electric double layer capacitors (EDLC). A hybrid energy storage system based on high specific energy Li-ion batteries (energy batteries) and EDLCs was selected. Compared to the other design options, this design showed a minimum thermal stress on the energy storage devices and had a wider operating temperature range, whilst it reached an overall weight of 6.7kg which is comparable with the other design options including energy battery only (5.6kg), power battery only (7.6kg) or energy battery/Li-ion capacitor hybrid (6 kg). Design of the energy storage system based on only LIC or EDLC resulted in significantly heavier designs with overall weights larger than 12kg due to the significantly lower specific energy of these devices. Design of the energy storage system based on energy battery/power battery hybrid could also provide a lower weight (3.45 kg) but will cause a higher thermal stress for the power battery cells as well as allowing a narrower operating temperature range.

In the proposed battery/EDLC hybrid system, it was found that the EDLC part contributed with 84% of the overall weight. Therefore, reducing the weight of the EDLC stack by maximizing the utilization of its nominal energy capacity was needed to significantly reduce the overall

weight of the energy storage system. Therefore, a novel multiport converter has been proposed that increases the utilization of the nominal energy capacity of the EDLC to 95% compared to 75% for conventional converters whilst maintaining the same current stresses for semiconductors and magnetics. This in turn allowed a weight reduction of 20% for the EDLC stack resulting in an overall weight of the energy storage system of 5.6kg (with 16.8% weight reduction compared to the previous design without the proposed converter with 6.5kg weight).

The proposed multiport converter provides two buck-boost ports for interfacing with the battery and the supercapacitors and a voltage boost port for interfacing with the PV array. The buck-boost capability of the EDLC port enabled wider voltage range for the stack and consequently maximum utilization of the available energy capacity. Using a phase shifted carries modulation technique has been proposed which allowed further reduction in the sizes of the converter inductors due to interleaving. The behaviour and the control structure of the proposed converter has been analysed and its performance has been characterised via simulations then a prototype demonstrator designed at a relevant voltage and power range has been developed and validated by experiments.

The results confirmed the expected performance of the proposed converter and its features including the possibility to reduce the inductors current ripple and to exploit the EDLC stack with a wider operating range of voltage.

8.2 Summary of achievements and contribution of this thesis

i) The development of a novel methodology for developing accurate power loss models for battery and supercapacitor cells at reasonable complexity of the models. The current models either are based on complex electrochemical models or the models are too simple having a reduced accuracy. The developed models based on this methodology can achieve good accuracy

for estimating the power loss that is then used to evaluate the thermal stress of the battery and supercapacitor cells accurately for a given load power profile.

ii) The Development of a novel multiport converter with modular architecture for photovoltaic/battery based power systems which significantly improves the utilization of available PV energy and battery capacity as it does not uses a high number of series connected PV and battery cells in a single string but rather utilises multiple modules. This approach also removes the need for additional battery cell/module equalizer circuitry used in conventional systems to handle a limited capacity mismatch between battery cells. The proposed converter can be also a promising solution for terrestrial applications for large scale PV/battery based power systems. Furthermore, it can handle large mismatch between battery cells (enable the use of wide variety of second life batteries) and also large mismatch in PV-panel powers so that different panels at different orientations can be easily interfaced allowing maximum utilization of the available space (i.e. different roof surfaces with different sun orientations) for installing PV panels.

iii) The development of a novel multiport converter for integrating to a power bus photovoltaic array and hybrid energy storage system, which consists of battery and supercapacitor stack. The current converter topologies interfacing supercapacitor stack to the power bus through a voltage boost-stage limit the utilization of its available energy capacity due to the limited operating voltage range of the stack. The proposed converter provides buck-boost operation for the supercapacitor stack that enables the extending of the voltage range of stack maximising the utilization of the nominal energy capacity of the cells which reduces the size of the stack for the same energy stored.

8.3 Future work

The controllers for the proposed converter topologies may not achieved the optimal performances for these converters in terms of transients/dynamics as these have not been tuned based on an accurate analytical modelling of the converters which is not so straightforward since in some operating modes, the different converter stages interact with each other. Therefore, future work will focus on developing a detailed modelling and a control system design for the proposed converters to enhance their performance especially during transient/dynamic changes. Also the developed converter topologies have been implemented based on a switching frequency of 10kHz due to the limitations of the used control platform that resulted in bulky size which can be accepted for a proof of concept experimental setup. Therefore, the future work will also focus on the implementation of suitable control platform that enable a switching frequency of ≥ 100kHz in order to gain the benefits of the proposed converters.

The developed multiport converter topology can be used in a centralized form as proposed or in a modular architecture similar to the proposed modular multiport converter that would be the better option for higher voltage power buses to eliminate the need for balancing circuits for the batteries and EDLC cells within a module. However, the complexity of the system will be significantly increase due to the large number of feedback measurements needed per single power module. Therefore, the future work will focus also on the development of a decentralized control architecture for the proposed modular multiport converter in which each power module can be controlled locally by a simple/low cost controller which can be supervised by the power system controller by means of a power reference and an available power feedback signal.

List of publications

Published papers:

1. A. Fares, C. Klumpner, and M. Sumner, "Development of a battery energy loss observer based on improved equivalent circuit modelling," in 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), 2016, pp. 1-10.

2. A. Fares, C. Klumpner, and M. Sumner, "Investigating the benefits and limitations of cascaded converter topologies used in modular battery systems," in 2017 IEEE 26th International Symposium on Industrial Electronics (ISIE), 2017, pp. 2123-2130.

3. A. Fares, C. Klumpner and M. Sumner, "Optimising the structure of a cascaded modular battery system for enhancing the performance of battery packs," presented at the 9th International Conference on Power Electronics, Machines and Drives, Liverpool, UK, 2018

4. A. Fares, C. Klumpner, and M. Rashed, "Design Considerations to Optimise Supercapacitor-based Energy Storage Systems for Aerospace Applications," in 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), 2018, pp. 1-8.

Journal articles under review:

1. A. Fares, C. Klumpner and M. Sumner, "A Novel Modular Multiport Converter for Enhancing the Performance of Photovoltaic-Battery Based Power Systems".

2. A. Fares, C. Klumpner and M. Sumner, "A Novel Multiport DC-DC Converter for Enhancing Battery-Supercapacitors Hybrid Energy Storage Systems for Nonstationary Applications".

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