

The University of Nottingham

UNITED KINGDOM · CHINA · MALAYSIA

SIEMENS

Real Time Monitoring of Capacitor Degradation in Industrial Variable Speed Drives

Abdurrahman Raqib

Thesis submitted to the University of Nottingham for the degree of Doctor of Philosophy

December 2021

Abstract

This thesis investigates a condition monitoring strategy suitable for use with monitoring the impedance of electrolytic capacitors in the DC-link of a motor drive, in contribution to the development of advanced intelligent variable speed drives.

Condition monitoring via signal injection is investigated, where signals of known frequencies are injected into the DC-link and electrical quantities are measured and used to estimate the impedance of the electrolytic capacitors at the specific frequency. Injection is achieved using two different methods: injection of a signal via a controlled AC power supply unit, and also injection of a signal via applying a controlled perturbation to motor speed. The limitations of each injection method are described, with simulation studies and experimental validation being used to verify the use of each method in estimating impedance accurately.

In partnership with the project sponsor, a commercial drive was used for practical testing of developed methods: the Siemens G120C. The practical limitations of applying an estimation scheme to a commercial drive were demonstrated, and both simulation studies and experimental validation were used to verify the accuracy of estimates found via use of signal injection into the commercial drive.

To verify that an impedance estimation method may be used with aged capacitors, an accelerated ageing process was devised for producing batches of aged capacitors, where electrolytic capacitors used in the DC-link had their impedances measured using laboratory impedance measurement units and then had their impedances estimated using in-situ measurements of voltage and currents. Taking a measurement of impedance as well as estimating impedance allowed for estimation accuracy to be compared as test conditions varied.

Acknowledgements

My thanks to God, for providing me the strength of will to not give up in my studies or work.

I owe my thanks to my supervisors – Prof Mark Sumner, Dr Christian Klumpner, and Dr Tom Cox – for their support throughout this project, as well as providing support during my undergraduate studies.

I would like to thank my family members, especially my father Muhammad Abdur Raqib, my sister Juairiyah Raqib, and my brother Ubayedullah Raqib, who provided amusing conversation which helped to ease my mind for a while.

Always in my thoughts are the many friends who encouraged me to undertake my doctoral studies, as well as provided good company outside of the lab. In particular, I would like to thank Dr Sanjana Ahmed, Dr Abdallah Hussein, as well as Dr Hayder Jahanger.

Many thanks to Richard Kenney, Imran Agha, Mike Davies, Garry Brown, Pete Lonsdale, as well as so many other people at Siemens PLC who provided me support through both equipment and advice regarding engineering theory and profession.

Chapter 1 – Introduction 1
1.1 – Introduction 1
1.2 – Aims and objectives of the research 4
1.3 – Research contributions 4
1.4 – Thesis structure 5
1.5 – Publications 5
1.6 – Impact of external issues on the project scope 6
Chapter 2 – Understanding the Variation in Capacitor Parameters 7
2.1 – Introduction 7
2.2 – Physical mechanisms involved in capacitor degradation 7
2.3 – Variation of capacitor impedance 12
2.3.1 – Variation in ESR 12
2.3.2 – Variation in capacitance 15
2.3.3 – Variation in circuit models 16
2.4 – Failure modes caused by degradation 18
2.5 – Acceleration of degradation 20
2.6 – Detection of degradation in-situ in power converters 25
2.6.1 – Impedance estimation using measurement of DC-link capacitor current 25
2.6.2 – Impedance estimation using signal injection 29
2.6.3 – Impedance estimation as part of an intelligent system 34
2.7 – Detection of degradation using chemical characterisation 40
2.8 – Detection of degradation in terms of reliability engineering 41
2.9 – Summary 43
Chapter 3 – DC-Link Impedance Estimation 46
3.1 – Introduction 46
3.2 – Electrical analysis 46
3.2.1 – Overview 46
3.2.2 – Simulation of electrical models 46
3.2.3 – Time domain analysis 52
3.2.4 – Frequency domain analysis 54
3.3 – Thermal analysis 65
3.3.1 – Structure of an electrolytic capacitor 65
3.3.2 – Thermal network model 66
3.3.3 – Variations in ESR 67
3.4 – Experimental implementation of the impedance estimation methods 76

3.4.1 – Estimation using the electrical method 76
3.4.2 – Estimation using the thermal method 83
3.5 – Aging of capacitors 88
3.5.1 – Lifetime curves 88
3.5.2 – Using a high ambient temperature 90
3.5.3 – Using a reverse bias voltage 96
3.6 – Summary 99
Chapter 4 – DC-Link Impedance Estimation via Capacitor Current 102
4.1 – Introduction 102
4.2 – Identification of frequencies of interest 102
4.3 – Drive DC-Link frequency spectrum 106
4.3.1 – Measurement of inverter quantities 106
4.3.2 – The loading system 108
4.3.3 – Experimental results 110
4.3.4 – Conclusions from initial tests 116
4.4 – Improving the SNR of DC-link measurements through signal injection 117
4.4.1 – Introduction to signal injection 117
4.4.2 – Proposed signal injection approach 117
4.4.3 – Data capture and data processing 119
4.4.4 – Conclusions from signal injection tests 126
4.5 – Sensitivity analysis of the identification of capacitor parameters 127
4.5.1 – Overview 127
4.5.2 – Results of sensitivity analysis 128
4.5.3 - Conclusions from sensitivity analysis tests 138
4.6 – Variation of capacitor core temperature 139
4.6.1 – Measurement of capacitor core temperature variations 139
4.6.2 – Estimation of impedance at different capacitor core temperatures 144
4.6.3 - Conclusions on variation in capacitor core temperature 148
4.7 – Impedance estimation under transient conditions 148
4.7.1 – Overview 149
4.7.2 – Estimation via FFT 150
4.7.3 – Estimation via the continuous wavelet transform (CWT) 152
4.7.4 – Conclusions from transient responses tests 154
4.8 – Comparison of estimates between new and aged capacitors 154
4.8.1 – Measurement of and estimation of the impedance of “new” capacitors 154

4.8.2 – Estimation of the impedance of “aged” capacitors 157
4.8.3 – Analysis of estimates found using “aged” capacitors 158
4.8.4 – Conclusions from estimation using “aged” capacitors 164
4.9 - Summary 165
Chapter 5 – DC-Link Impedance Estimation via Motor Speed Perturbation 167
5.1 – Introduction 167
5.2 – Motor speed perturbation 168
5.2.1 – Basic concept 168
5.2.2 – Identifying the capacitor current 172
5.2.3 – The influence of grid-side impedance 177
5.2.4 – Conclusions on injection via motor speed perturbation 182
5.3 – Estimation via simulated motor speed perturbation 183
5.3.1 – Outline of simulated motor speed perturbation 183
5.3.2 – Estimates found via simulated motor speed perturbation 184
5.3.3 – Conclusions on estimation via simulated motor speed perturbation ... 190
5.3.4 – Limitations on experimental validation 190
5.4 – Experimental test rig limitation: sampling frequencies 191
5.4.1 – Outline of the limitation 191
5.4.2 – Effect of the limitation on estimation accuracy 193
5.4.3 – Effect of the limitation on the choice of the DC reactor 194
5.4.4 – Effect of the limitation on the choice of injection frequency 197
5.4.5 – Conclusions on the effect of the limitation on sampling frequencies ... 197
5.5 – Experimental test rig limitation: inverter current estimation 198
5.5.1 – Outline of the limitation 198
5.5.2 – Inverter current estimation within the limitation 200
5.5.3 – Impedance estimation within the limitation 203
5.5.4 – Conclusions on the effect of the limitation on inverter current estimation 208
5.6 – Summary 209
Chapter 6 – Conclusion 211
6.1 – Summary 211
6.1.1 – Impedance estimation 211
6.1.2 – Accelerated ageing 211
6.2 – Research contributions 212
6.3 – Future recommendations 212
6.3.1 – Impedance estimation 212

6.3.2 – Accelerated ageing..... 213
6.4 – References 213
Appendix A.....227
Appendix B.....229
Appendix C.....234
Appendix D.....235
Appendix D.1 – <1kHz range..... 235
Appendix D.2 – 4kHz range..... 236
Appendix D.3 – 8kHz range..... 239

Chapter 1 – Introduction

1.1 – Introduction

Motor drives, referred to by many phrases including variable speed drives and variable frequency drives, are integral to delivering power to electric motors in applications ranging from pumps or fans in industrial or residential settings through to cranes or hoists on construction sites or oil rigs [1].

Typically, motor drives are used where there is a need to provide power to a motor whilst maintaining control of the motor via use of feedback signals from the motor or the application itself. This is referred to as closed-loop control [2], and is commonly used where there is a need for precise control of the motor speed or electric torque in cases where open-loop control (i.e. control without any feedback) is considered inadequate [3], and is increasingly being used due to advances in microcontroller complexity and reductions in the cost of microcontrollers [4].

Fig1.1 shows a block-diagram of the general structure of a conventional motor drive system. The power electronic converter and the supporting control algorithm lie at the heart of the system, where signals are fed back using measurement transducers to allow actuation signals to be adjusted to help the motor drive control system to better react to system transients.

Depending on the complexity of the system, different system variables may be monitored by the control algorithm. If the current flowing between the grid and the power electronic converter is controlled, the voltages and currents related to the grid may be used as feedback to help decide switching states of the PWM rectifiers in active front ends [5]. If the motor at the output of the drive requires speed to be maintained with minimal error during transients, motor current may be used as feedback to help reduce error in torque or flux producing current [3]. If parts of the system cause faults or warnings to be triggered in the control algorithm – especially in safety critical applications - the drive's diagnostic system would be able to decide on how best to safely bring the rotating motor to a halt [5].

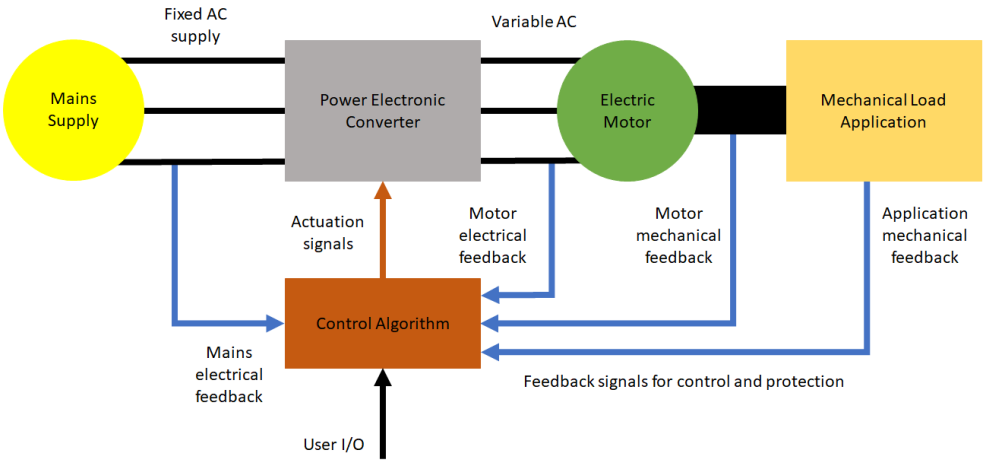


Fig1.1 – General structure of a conventional motor drive system

In the literature, various topologies may be found that are used in power electronic converters, with the most common being shown in Fig1.2, where power is drawn from the fixed frequency/amplitude AC supply, smoothed by the energy storage components of the DC-link, and then converted to a variable AC power for the power. Other examples of converters do exist, such as the matrix converter which can be used to avoid the need for a DC-link, but these examples are uncommon outside of niche applications [6] and academic research [7].

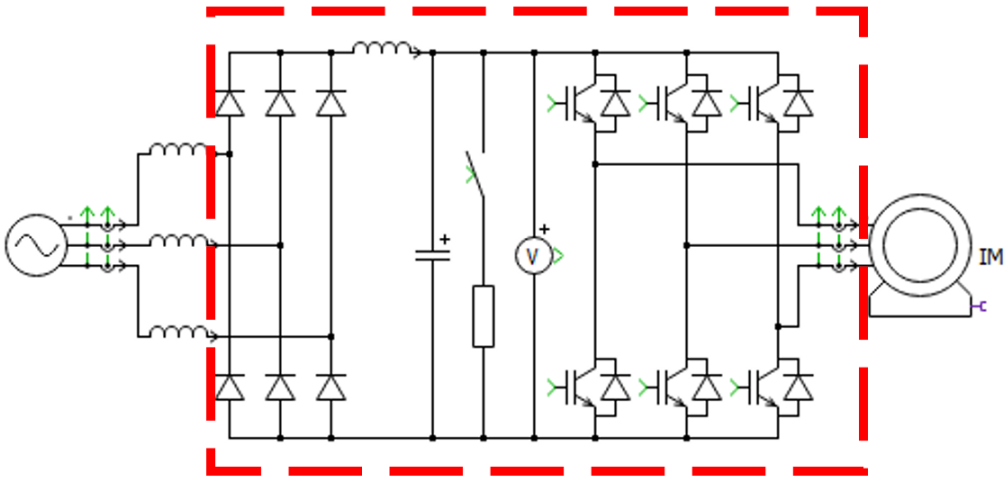


Fig1.2 – General circuit topology of a conventional industrial motor drive system

Fig1.2 shows the general circuit topology of a conventional motor drive system, with the specific region within the red dashed lines indicating the parts that make up the power electronic converter.

This example is typical for industrial motor drives, where six-pulse diode rectifiers are used at the input of the drive for reasons of cost and low complexity; the DC-link is

made up of electrolytic capacitors used to smooth and maintain DC voltage for use with the switching inverters at the output of the drive; and mechanisms are provided to allow usage of a braking resistor during fault conditions such as overvoltage of the DC-link capacitors. The DC-link voltage is typically measured for PWM switching purposes, and at least one phase of motor current is measured for protection and control.

As was shown on Fig1.1, feedback signals from various parts of the system are used by the control algorithm to determine system response at any given moment. From the point of view of drive manufacturers, an issue that arises is the complexity of the algorithm/software which may be deployed onboard the drive controller.

Using the previously mentioned example of a drive deployed in a construction site or an oil rig, the drive may experience adverse conditions due to the environment or due to system transients [8]. These conditions may cause issues in the system which may be simple for the drive's onboard controller or human operator to diagnose and mitigate, such as overheating of the drive enclosure due to inadequate ventilation. Alternatively, these same conditions may cause issues to arise which are only evident if looking for particular behaviour in electrical waveforms, such as motor issues through motor current signature analysis or drive component issues through monitoring of degradation via measuring electrical quantities related to IGBT power modules or DC-link electrolytic capacitors.

Academic literature has explored issues such as the aforementioned motor current signature analysis [9] [10] and degradation of IGBT power modules [11] [12] and DC-link electrolytic capacitors [13] [14], exploring these issues for the purpose of generating knowledge that may be used industrially. Many such issues which are related to system diagnostics and prognostics are also considered as part of cohesive health-monitoring systems [15] [16], where a central controller may use feedback from various parts of the system to better gauge the health of the system – just as was indicated in Fig1.1.

The motivation of this project came from the industrial desire to develop and implement intelligent systems into existing commercial motor drives as part of internet-of-things ecosystems [17] [18] [19] [20]. As condition monitoring principles already exist in academic literature, there is an industrial interest in integrating these

principles into future products in order to increase value offered to customers and also to maintain an edge in the market.

At the suggestion of the project sponsor, condition monitoring of critical components of motor drives was considered an avenue of research, where this project examined degradation of DC-link electrolytic capacitors within the practical limitations of existing drive usage and design.

1.2 – Aims and objectives of the research

This research aims to investigate and devise a condition monitoring strategy to be used to monitor the impedance of electrolytic capacitors in the DC-link of a Siemens G120C, in contribution to the development of advanced intelligent variable speed drives.

The main research objectives are:

1) To determine an appropriate technique for condition monitoring of electrolytic capacitors in an operational drive utilising an impedance estimation method.
2) To investigate the effect of accelerated ageing on electrolytic capacitors used in an operational drive.
3) To investigate the usage of the impedance estimation method applied to a drive in a laboratory setting.
4) To investigate the usage of the impedance estimation method applied to a drive considering practical measurement limitations.

1.3 – Research contributions

This section summarises the main contributions presented in this thesis:

1) Investigating and developing an impedance estimation scheme appropriate for an industrial drive operating under a range of conditions, as shown in sections **4.5**-**4.7** and section **5.6**.
2) Investigating and developing a simple and repeatable accelerated ageing scheme to rapidly age batches of test capacitors for use in validation of the impedance estimation scheme, as shown in section **3.5** and section **4.8**.

1.4 – Thesis structure

Chapter 2 discusses physical mechanisms involved in capacitor degradation, as well as how capacitor impedances and equivalent circuit models vary. This chapter also investigates degradation of capacitors: specifically, failure modes caused by degradation; methods of accelerating the degradation of capacitors; and detection of degradation of these electrochemical devices by way of use in power converters, as well as some chemical characterisation techniques and models based in reliability engineering.

Chapter 3 discusses impedance estimation using mathematical transforms, making use of measured capacitor voltages and currents. Equivalent electrical and thermal models of the electrolytic capacitors are presented and discussed. Simulations and experimental work are used to describe and compare the usage of each model.

Chapter 4 goes on to discuss frequencies of interest in the drive waveforms which may be used to achieve accurate impedance estimates where test capacitors are used with a test drive and motor operated under a range of conditions of load torques, frequencies, and capacitor core temperatures. A brief comparison study is undertaken, looking at a batch of aged capacitors in an operational drive.

Chapter 5 discusses injection of disturbance signals into reference motor speed, considering practical limitations of the industrial motor drive. Relevant theory is discussed, after which a simulation study and experimental validation are carried out.

Chapter 6 presents a summary of the work performed during the course of the thesis and the project. It summarises the contributions and learnings of the work presented in this thesis, as well as provides a few recommendations for further research.

1.5 – Publications

The work in this thesis have been presented as follows:

1) A. Raqib, H. Jahanger, M. Sumner, T. Cox, C. Klumpner, “Comparison of Frequency Transform Methods for Condition Monitoring of a DC-Link Capacitor”, The 10th International Conference on Power Electronics, Machines and Drives, December 2020 [21]
2) A. Raqib, “White paper on impedance estimation of DC-link electrolytic capacitors in the Siemens G120C”, December 2021

1.6 – Impact of external issues on the project scope

Initially, the project was expected to be a four-year investigation into auto-commissioning of high-quality motor drive systems, specifically looking at the impact of usage of wide-bandgap devices on motor control. At the suggestion of the project sponsor, the project direction was changed at the end of the first year to instead focus on condition monitoring of industrial motor drives. A secondment period was then undertaken at the sponsor's factory to better understand the industrial context of this work. As a result, the work upon which this thesis is based began properly at the start of the third year of the expected four-year project.

Due to effect of restrictions via the COVID pandemic on lab-based experimental work, long-term electrical stressing of batches of capacitors could not be carried out as part of the work in Chapter 3. Beyond acknowledging the use of long-term electrical stressing in literature, work was not undertaken as the long time-scales involved were impractical considering the effect of the restrictions on the time-line of the project.

Ill health impacted the project, where illness in the supervisory team meant there was a limited access to looking at building or procuring a custom research converter for the tests in Chapter 5. An attempt was still made to mitigate this issue: for the tests in Chapter 5, commercial motor drives were provided by the project sponsor so the developed ideas could be tested in practice. This solution was imperfect, however, as there was a limited access to the converter control variables due to the converter source code being intellectual property that the project sponsor was unable to share.

Chapter 2 – Understanding the Variation in Capacitor Parameters

2.1 – Introduction

This chapter discusses the physical mechanisms involved in capacitor degradation, as well as how capacitor impedances vary according to physical mechanisms. The variety of circuit models which may be used to represent a capacitor impedance will also be discussed.

As the stated aim of this project is to investigate and devise a condition monitoring scheme for use in monitoring impedance of electrolytic capacitors, this chapter will also investigate degradation of capacitors: specifically, failure modes caused by degradation; methods of accelerating the degradation of capacitors; and detection of degradation of these electrochemical devices when used in power converters, as well as some chemical characterisation techniques and models based in reliability engineering.

2.2 – Physical mechanisms involved in capacitor degradation

Aluminium electrolytic capacitors are typically used to maintain charge in DC-links, or DC-buses, when positive DC voltages with superimposed AC ripple voltages are required to be maintained for use in separate stages of circuits. Despite having relatively high ohmic losses compared to other capacitors and despite being polarised, aluminium electrolytic capacitors have a low cost to energy ratio compared to other types of capacitors and as a result, there are many converter applications that use these capacitors for maintaining charge, with some common applications including switch-mode power supplies and motor drives [22] [23]. These electrolytic capacitors are common points of failure in converters [24] [8] [14].

The transfer function of the reactance of an ideal capacitor may be represented mathematically in the Laplace domain by (2.1):

$$\overline{X_C}(s) = \frac{1}{sC} \tag{2.1}$$

where $\overline{X_C}(s)$ refers to the reactance of a capacitor in the Laplace domain; where C refers to the capacitance of a capacitor; and where s refers to the Laplace operator.

For the purpose of simplifying mathematical problems such as linear differential equations, use of (2.1) is appropriate when generally considering capacitors. However, the transfer function in (2.1) is unrealistic when trying to investigate the effect of components such as aluminium electrolytic capacitors, as well as examine the effect

of changes within these capacitors. For these purposes, it is more appropriate to consider the diagram in Fig2.1, where this diagram is more representative of an aluminium electrolytic capacitor than (2.1).

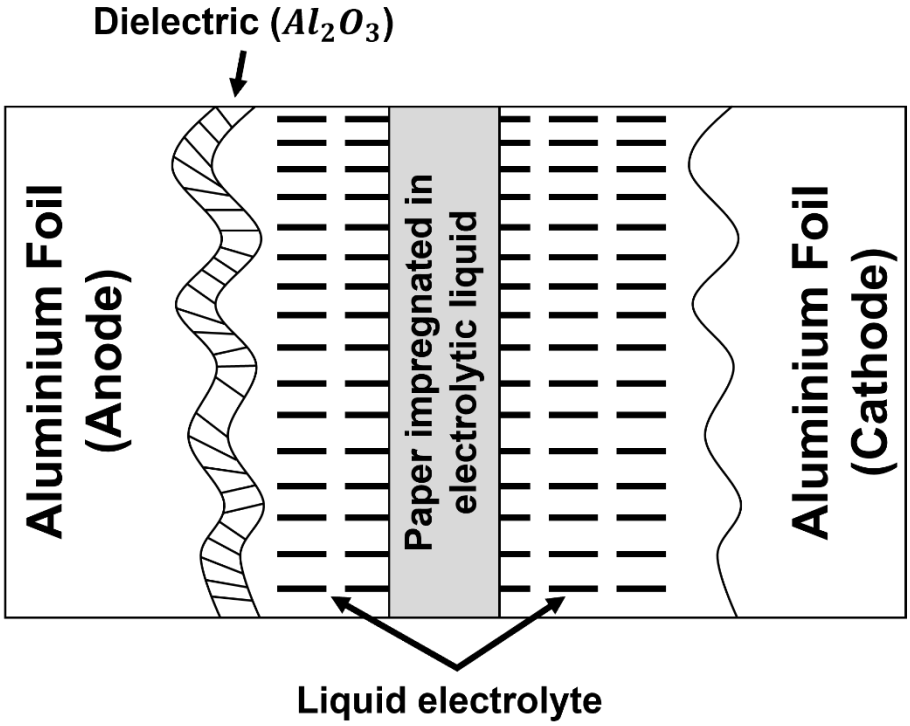


Fig2.1 – Physical structure of an aluminium electrolytic capacitor

Fig2.1 shows the physical structure of an aluminium electrolytic capacitor. This figure is illustrative of only one layer of foil within the can of an aluminium electrolytic capacitor. On either side of the image are pieces of aluminium foil, each of which represent the anode and cathode of the capacitor. The presence of the anode and cathode indicate that the capacitor is polarised. Between the anode and cathode is liquid electrolyte, as well as paper which is impregnated within this electrolytic liquid. Also shown is the dielectric medium, which is deposited on the foil of the anode. A deeper mathematical explanation of Fig2.1 is presented in [25], where each part of the figure is described in theory and validated using computer simulation.

The manufacturing processes of aluminium electrolytic capacitors vary marginally between manufacturers, but the same general process is observed in the details which are commercially available, even historically. For example, [26] [27] [28] [29] all agree on the general physical structure shown in Fig2.1 in terms of manufacturing these

capacitors, with the major difference between each source being the specific composition of the solution of liquid electrolyte.

The sections of aluminium foil shown in Fig2.1 are made up of very pure aluminium to minimise ohmic losses. Some impurities are present in the aluminium foil, although impurities are sometimes intentionally introduced to increase total capacity provided by the wound foils [30]. Although the method varies between manufacturers, etching processes are applied to the aluminium foil to increase the apparent surface area of a roll of foil [31]. This increase in surface area can be understood through (2.2), where net capacitance is a function of the surface area of the parallel foil plates:

$$C = \frac{A\varepsilon_0\varepsilon_r}{d} \tag{2.2}$$

where C refers to the net capacitance of an aluminium electrolytic capacitor; where A refers to the surface area of the conducting foil; where ε_0 refers to the absolute permittivity; where ε_r refers to relative permittivity (dielectric constant) of the dielectric medium; and where d refers to the distance between the parallel foil surfaces.

The section of paper is used to prevent short-circuits between the anode/dielectric medium layer and the cathode layer, as well as to physically hold the liquid electrolyte. This storage is achieved through designing the paper to be very porous, where the many pores may be used to store as much electrolytic liquid as possible when the paper is submerged and impregnated with electrolyte within the capacitor can.

The electrolyte solution is made up of a combination of solvents and solutes (salts). A major component of the liquid electrolyte is ethylene glycol, as understood by examining capacitor material data sheets [32], by consulting knowledge bases on chemical compositions and usages [33], or by investigating structures of electrolytic capacitors using an understanding of chemical compositions [34]. One of the main purposes of the electrolyte is to exist solely to allow the dielectric medium to be regenerated on the anode layer whilst a forward bias voltage is applied across the anode and cathode layers, meaning that maintaining an appropriate level of forward bias voltage across an electrolytic capacitor helps maintain a healthy dielectric medium, assuming the core temperature is maintained at a safe level.

The dielectric medium, Al_2O_3, is deposited as a layer on the anode foil during the manufacturing process, normally through the use of electrolysis. Being a dielectric, this

medium prevents the passage of electric current unless a sufficiently high forward bias voltage is applied across the medium. In practice, this means that a forward bias voltage would need to be applied between the anode and cathode to allow current to flow between these poles. The presence of this dielectric medium layer on the anode foil contributes to an effect of a rectifier diode, where current may flow from the anode to the cathode if a forward bias voltage were to be applied across them. Another use of the dielectric is to help limit the stray leakage current between the anode and cathode foils [35]. This diode effect is the reason that aluminium electrolytic capacitors are polarised: they are designed to allow unidirectional flow of current from anode and cathode, and these polarised capacitors can only tolerate a small reverse bias voltage (approximately 1.5V) before failing. The specific failure mechanism would be the migration of the dielectric medium from the anode foil to the cathode foil, which is an exothermic process which causes rapid heating of the liquid electrolyte and eventually failure capacitor.

Considering the presence of the aluminium foil, the electrolyte, and also the dielectric medium, (2.3) may be used to find the equivalent series resistance (ESR) of the aluminium electrolytic capacitor:

$$ESR = R_O + R_E + R_D \tag{2.3}$$

where ESR refers to the equivalent series resistance of an electrolytic capacitor; where R_O refers to the ohmic resistive contribution of the aluminium foil inside the capacitor casing and the metallic contacts outside the casing; where R_E refers to the resistive contribution of the electrolyte; and where R_D refers to the resistive contribution of the dielectric medium.

Improving upon Fig2.1, Fig2.2 may be drawn where this figure shows an equivalent series representation of a capacitor. Electrical circuit elements are used to represent each component described in Fig2.1.

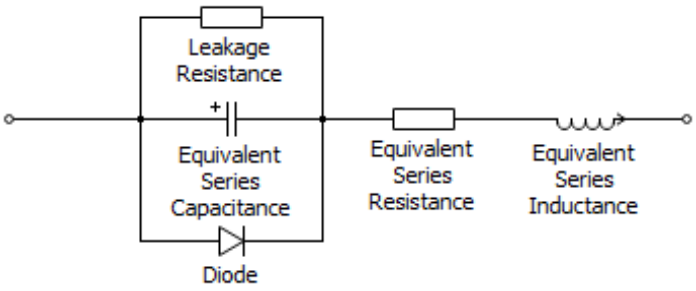


Fig2.2 – Equivalent series representation of a capacitor, based on Fig2.1

An equivalent series inductance (ESL) is shown, representing the inductive contributions from the aluminium foil layers within the capacitor case as well as the terminals and metallic contacts outside the case. The ESR is shown, representing the resistive contributions described in (2.3). The equivalent series capacitance (or net capacitance) is shown, representing the capacitance provided due to choices of foil purity, foil etching, and paper pores, as well as surface area, foil spacing and choice of electrolytic liquid as described in (2.2). Also shown are a leakage resistance and a diode.

As was previously described, the presence of the diode is due to the unidirectional flow of current caused by the presence of the layer of dielectric medium on the anode, where the diode represents flow of current from the anode to cathode. In the specific representation in Fig2.2, the diode is actually redundant because the symbol for the capacitor indicates that the capacitor is polarised.

The presence of the leakage resistance is used to represent the leakage current between the anode and cathode shown in Fig2.1. As was described in (2.3), the electrolytic liquid has a certain resistive contribution. The resistivity of the electrolyte may also be considered in terms of conductivity, where a high conductivity leads to the electrolyte allowing a large amount of leakage current to flow as a forward bias voltage is applied across the capacitor, and a low conductivity leads to the flow of a small amount of leakage current. As leakage current is inversely proportional to the resistive contribution of the electrolyte, the electrolytic capacitor may fail if the resistive contribution of the electrolyte decreases as this would lead to a dangerous amount of leakage current flowing from anode to cathode.

Overall, the choice of electrolytic liquid affects both the ESR due to the contribution via resistive contributions in the physical structure according to (2.3); and the leakage resistance via leakage current.

Fig2.2 may be simplified to Fig2.3 by ignoring the redundant diode due to the understanding that the capacitor is already polarised, as well as the ESL due to the interest in the influence of the more dominant reactance of the capacitor.

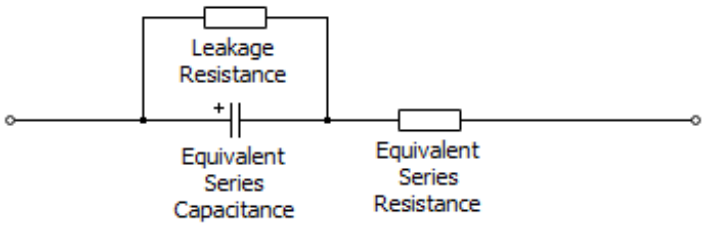


Fig2.3 – Equivalent series representation of a capacitor, simplified from Fig2.2

Using Fig2.3, the transfer function of the ideal capacitor reactance described by (2.1) may be amended to the more realistic transfer function described by (2.4), where the presence of the leakage resistance in the equivalent series representation is acknowledged but still omitted from (2.4) due to the leakage resistance being very large compared to the other two impedances:

$$\bar{Z}(s) = \frac{1}{sC} + ESR \equiv \frac{1+(ESR \cdot sC)}{sC} \tag{2.4}$$

where $\bar{Z}(s)$ refers to the impedance of a capacitor in the Laplace domain; C refers to the capacitance of a capacitor; where ESR refers to the equivalent series resistance of an electrolytic capacitor; and where s refers to the Laplace operator.

2.3 – Variation of capacitor impedance

Based on the equivalent series representation of a capacitor shown in Fig2.3, there are two circuit components that may vary and therefore affect the capacitor impedance.

2.3.1 – Variation in ESR

The dependencies of the capacitor ESR, whose components were described in (2.3), on frequency and temperature are well documented in manufacturer datasheets. An example of datasheet information is shown in Fig2.4 where the manufacturer provides graphs [36] showing the frequency characteristics of ESR (top graph) and the variation of impedance with frequency (bottom graph).

In the graph showing variation in ESR, each of the curves represent a capacitor of a different core temperature; and in the graph showing variation in impedance, ESR is

shown to dominate the frequency response of each capacitor beyond approximately 2kHz.

Unfortunately, these curves are best used as a rule-of-thumb as capacitor ESR varies according to the amount of DC bias voltage across the capacitor; according to the magnitude of AC ripple current through the capacitor; and according to the frequency spectrum of the AC ripple current. Additionally, the datasheet graphs show that in-situ temperature measurement of the capacitor core would be necessary if making direct use of the plotted curves.

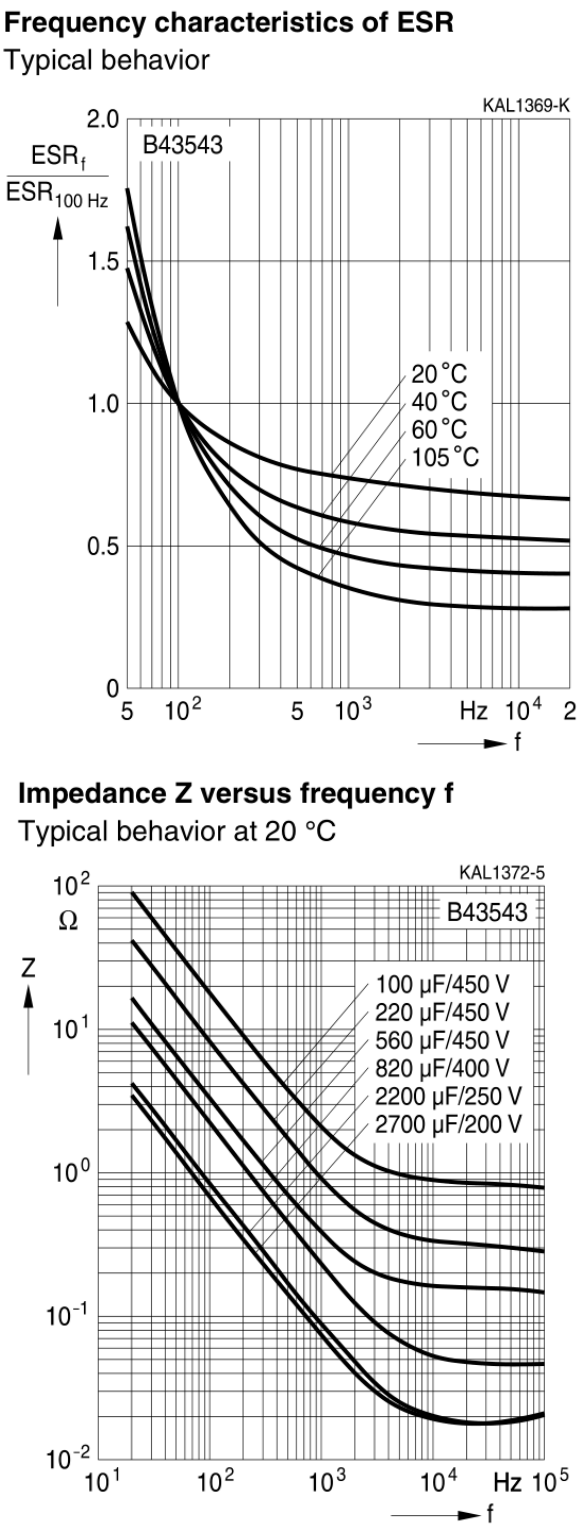


Fig2.4 – Datasheet information showing dependency of ESR on frequency and temperature *[36]*

Furthermore, [37] and [38] expand upon (2.3), stating that the net ESR of the aluminium electrolytic capacitor is dependent on temperature and frequency as the

electrolyte-dependent resistance is a function of temperature, and the dielectric-dependent resistance is a function of frequency. This is shown in (2.5):

$$ESR = R_O + R_E(T) + R_D(f) \tag{2.5}$$

where ESR refers to the equivalent series resistance of an electrolytic capacitor; where R_O refers to the ohmic resistive contribution of the aluminium foil inside the capacitor casing and the metallic contacts outside the casing; where $R_E(T)$ refers to the temperature-dependent resistive contribution of the electrolyte; and where $R_D(f)$ refers to the frequency-dependent resistive contribution of the dielectric medium.

Considering (2.5), this would mean that (2.4) would need to be amended to include the dependency of ESR on frequency and temperature, as is shown in (2.6):

$$\bar{Z}(s) = \frac{1}{sC} + ESR(s,T) \tag{2.6}$$

where $\bar{Z}(s)$ refers to the impedance of a capacitor in the Laplace domain; C refers to the capacitance of a capacitor; where $ESR(s,T)$ refers to the temperature-dependent and frequency-dependent equivalent series resistance of an electrolytic capacitor; and where s refers to the Laplace operator.

2.3.2 – Variation in capacitance

Considering the explanation of Fig2.1 that was presented in section **2.2**, the capacitance of an aluminium electrolytic capacitor is dependent primarily on the choice of liquid electrolyte; the porosity of the paper; and the increase in surface area of the aluminium foil achieved through etching processes.

These three dependencies are impractical to directly assess without destructive testing of a capacitor. Additionally, manufacturer information is not provided on variation of capacitance via datasheets. However, as it is has been made clear that the properties of the liquid electrolyte and the dielectric medium cause dependencies on frequency and temperature, (2.6) may be amended to (2.7):

$$\bar{Z}(s) = \frac{1}{sC(s,T)} + ESR(s,T) \tag{2.7}$$

where $\bar{Z}(s)$ refers to the impedance of a capacitor in the Laplace domain; $C(s,T)$ refers to the temperature-dependent and frequency-dependent capacitance of a capacitor; where $ESR(s,T)$ refers to the temperature-dependent and frequency-

dependent equivalent series resistance of an electrolytic capacitor; and where s refers to the Laplace operator.

2.3.3 – Variation in circuit models

The general equivalent series representation of a capacitor was shown in Fig2.3, showing a capacitor in series with an equivalent series resistor. This model is a simplification based on Fig2.1, and is not the only possible equivalent model of a capacitor.

As electrolytic capacitors are electrochemical devices, measurement of their impedances may be taken using electrochemical impedance spectroscopy (EIS) [39] [40]. Although EIS is more suited to measurements related to batteries, supercapacitors, and fuel cells, the same general measurement techniques may be used with electrolytic capacitors. Examples of two general measurement techniques include galvano-static EIS (GEIS) and potentio-static EIS (PEIS), where GEIS uses small amounts of controlled impulses of current and PEIS uses small amounts of controlled impulses of voltage [41].

EIS is well suited for generating equivalent circuits based on curve-fitted frequency responses of test electrochemical devices. As a result, the equivalent circuits of electrolytic capacitors may be made more complex according to EIS-measured frequency responses, usually due to EIS measurements primarily being interpreted through Nyquist plots. An example of an equivalent circuit of a capacitance and the corresponding Nyquist plot found via EIS are shown in Fig2.5.

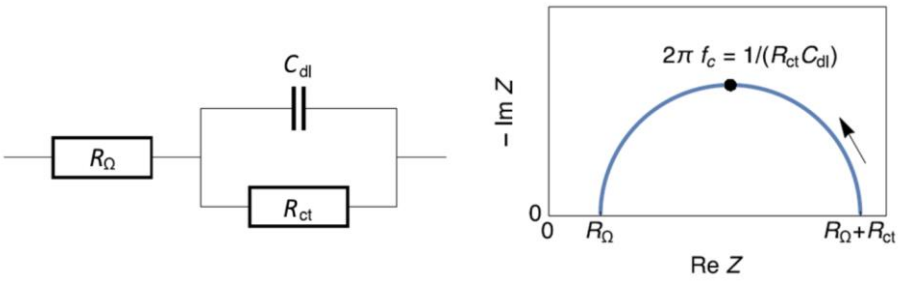


Fig2.5 – A circuit (left) and the corresponding Nyquist representation of impedance (right) *[41]*

Generating equivalent circuits is not a recent innovation, and this dates back to at least 1981 [42], where the authors state that curve-fitted Nyquist plot frequency responses may be used to generate at least third-order equivalent circuit models to better

quantify the effect of dielectric mediums. This work carried on in [43], where the term EIS was defined and the author focused more closely on advising on how to generate better curve-fits to improve equivalent circuit models. Fig2.6 shows an example taken from [43], where the author shows that four different second-order circuits can be used to exhibit the same impedance response.

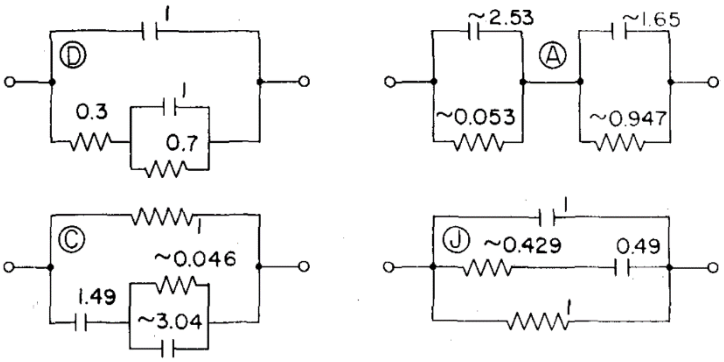


Fig2.6 – Four different second-order circuits with the same impedance response *[43]*

More recently, [44] showed that it was possible to take the frequency response of an electrochemical device and split the full frequency response into separate sections where it could be considered that each section would have its own equivalent circuit model. By splitting the experimentally derived full frequency response into smaller sections, a more accurate model would be generated for the equivalent circuit model of the electrochemical device. Fig2.7 shows an example of this sectional split of the frequency response.

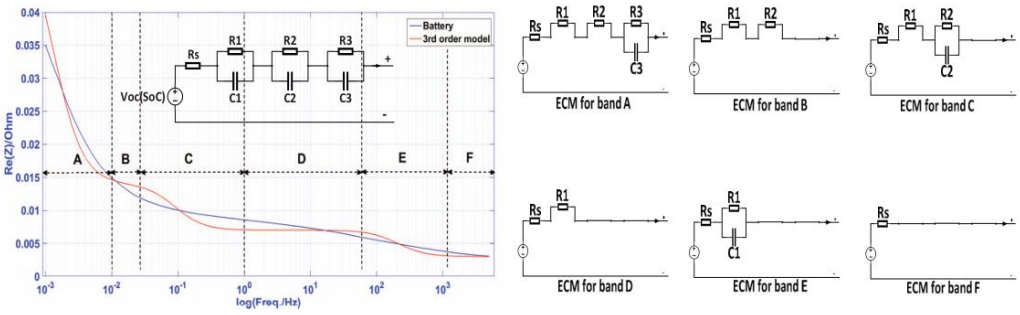


Fig2.7 – A fitted curve which is split into six different sections *[44]*

[45] went in a different direction, demonstrating that some improvements may be made on the curve-fitted equivalent circuit models by making use of mathematical components in addition to the traditional electrical components (resistor, inductor, capacitor). It was shown that by making use of additional mathematical components,

improved curve-fits of Nyquist plots may be found and therefore more accurate equivalent circuit models may be generated. Fig2.8 shows an example of an equivalent circuit model which makes use of a constant phase element (CPE) along with the more familiar capacitors and resistors, where CPEs are mathematical components which may be used to represent non-ideal capacitors [43].

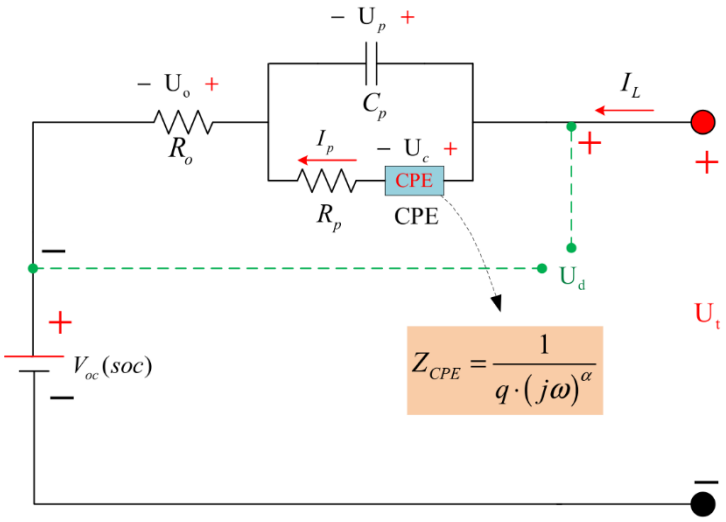


Fig2.8 - Example of an equivalent circuit model using a “constant phase angle element” [45]

One problem with splitting frequency responses into smaller sections of frequency responses as was shown in [44] was that many higher-order circuits may be generated depending on the frequency range of interest, resulting in complex equivalent circuits. Similarly, making use of mathematical components as was shown in [45] would also result in highly complex circuits, although arguably the specific problem in this case would be in interpreting data from Nyquist plots instead of comparing magnitudes of impedances directly against frequency.

2.4 – Failure modes caused by degradation

Failure in electrolytic capacitors may be caused by a variety of reasons. For example, [37] described deterioration characteristics of aluminium electrolytic capacitors, stating that increases in capacitor core temperatures lead to evaporation of liquid electrolyte and this reduction in electrolyte would mean a reduction in effective surface area of the capacitor, thereby causing a decrease in capacitance. Additionally,

an increase in ESR would be observed due to a reduction in the amount of electrolyte between the layers of foil.

[46] stated that evaporation of liquid electrolyte occurs when a capacitor is placed under a forward bias voltage and a high ambient temperature. Fig2.9 shows the variation in impedances as a capacitor is placed under a constant DC voltage and high temperature. Cathode depassivation is also listed as a cause of failure, where this involves a breakdown in the surface layer of the cathode aluminium foil over long periods of time. Voltage derating is also mentioned, where the maximum permissible voltage that may be maintained by a capacitor varies according to the capacitor core temperature. This is understandable when considering (2.7), which states that both capacitance and resistance of a capacitor are functions of temperature due to the behaviour of the liquid electrolyte.

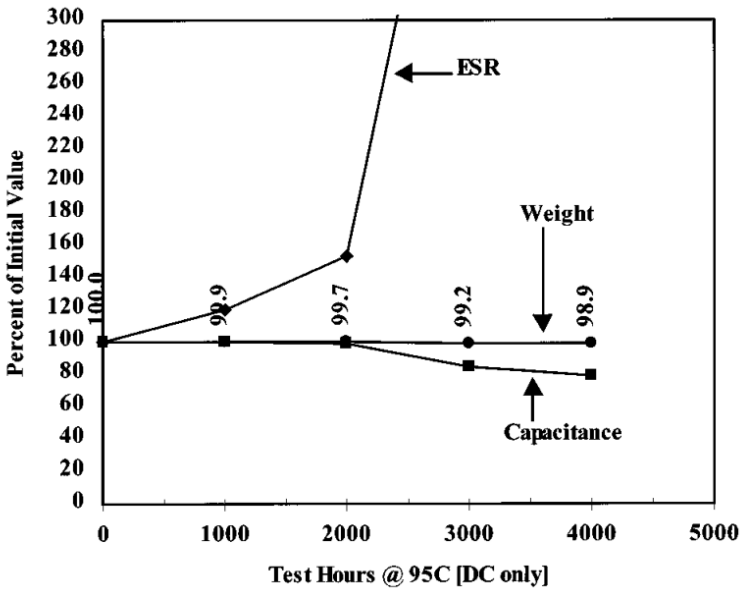


Fig2.9 - Drift in capacitor impedance due to evaporation of electrolyte [46]

[47] investigated failure mechanisms by looking at the effect of inrush currents on capacitor leakage resistances, showing that current pulses to the capacitor core coupled with a hot core temperature caused irreparable damage to leakage resistance whereas a hot core temperature alone did not. This meant that the volume of liquid electrolyte in a capacitor can would be reduced as a result of application of a current pulse and hot core temperature, whereas simply varying the core temperature would not cause a permanent effect on the leakage resistance.

Separately, [48] and [49] stated that common failure modes include faults due to short circuits and open circuits. Short circuit failures are stated to be caused by breakdown of the dielectric medium due to manufacturing defects in the dielectric material layer, whereas open circuit failures are stated to be caused by drying of the electrolyte, especially due to long-term operation of the capacitor in high temperature environments.

[50] stated that on a material level, thermal cycling of capacitors leads to crystal defects and degradation of the dielectric oxide layer, with repeated application of electrical stress leading to localised breakdowns in the dielectric oxide layer, further leading to reductions in capacitance.

A common theme of [46] [47] [48] [49] was that reducing the amount of electrolyte in a capacitor can via application of high temperature is an effective way of inducing a failure mode. [50], on the other hand, spoke of the dielectric oxide layer specifically, mentioning that placing a repeated stress upon the dielectric medium would lead to an alternative failure mechanism.

2.5 – Acceleration of degradation

To demonstrate detection of degradation in electrolytic capacitors, it is necessary to have capacitors of various stages of degradation. As a result, it is vital to understand and develop methods of degrading capacitors in a controlled manner.

As previously shown in Fig2.9, [46] used the method of placing test capacitors under a high DC voltage of 450V with a high ambient temperature of 95°C for 4000 hours. Changes in resistance were noticed after 1000 hours, with sharper increases in measured resistance at 2000 and then 3000 hours. Noticeable changes in capacitance, however, required much longer. The step change in measured resistance at 3000 hours coincided with the decrease in capacitance, and this was probably due to evaporation of liquid electrolyte causing an open circuit failure.

[51] also looked at accelerating the ageing of a batch of electrolytic capacitors, except here the electrolytic capacitors that were used were of much lower rated voltages than the electrolytic capacitors used in DC-links. Here, a batch of capacitors were subjected to voltage stresses by alternating between applying a DC voltage greater than the rated voltage and applying an AC square-wave ripple of very low frequency (<1Hz) and an

amplitude greater than the rated voltage. The electrical stressing occurred for many thousands of hours, with results being shown in Fig2.10. In addition to electrical stressing, [51] also looked at making use of thermal stressing. For more than 2000 hours, capacitors were placed in a thermal chamber at a temperature of 125°C and allowed to rest at that temperature for the duration of the experiment, with results being shown in Fig2.11. Based upon the experimental data gathered using these two sets of stress tests, a prognostics algorithm was devised using a control technique where the algorithm would determine how close a capacitor would be to end-of-life.

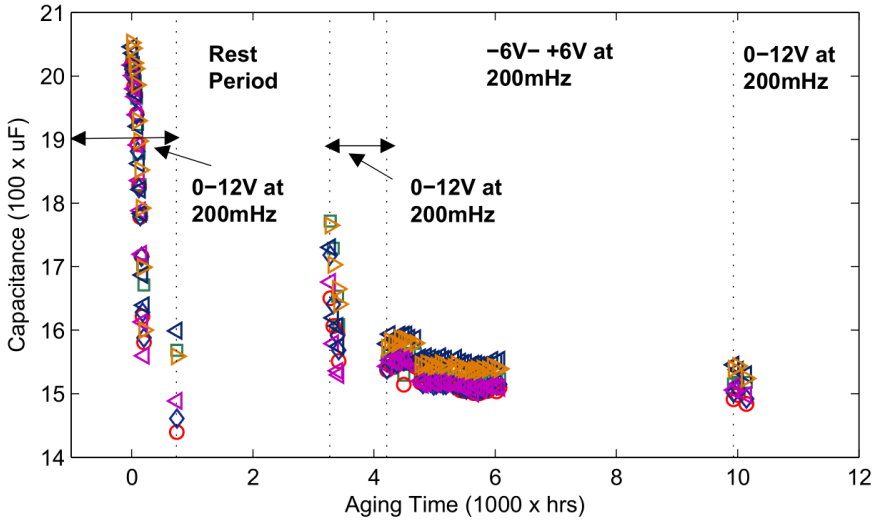


Fig2.10 - Electrical stressing results [51]

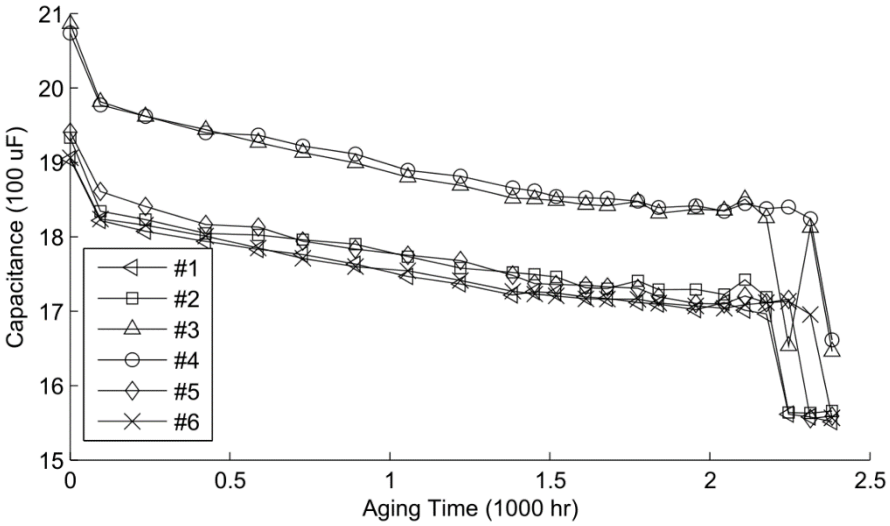


Fig2.11 - Thermal stressing results [51]

Whilst [51] injected current pulses of very low frequency, [52] instead injected current pulses of frequencies between 2kHz and 15kHz into capacitors held at high ambient

temperatures. Here, the authors chose this frequency range due to the frequency response of the test capacitors showing that the gain was flat in this frequency range. As a result of looking exclusively at this frequency range, and by heating test capacitors for prolonged periods of time, the effect of the ageing process upon the test capacitors could be easily observed in terms of change in ESR alone.

[53] looked at tampering with the capacitor directly on a physical level, where the capacitor lid was punctured and then the capacitor was placed in a high ambient temperature for a number of hours. The heating of the capacitor would cause the temperature of the liquid electrolyte to increase, and eventually a small volume of electrolyte would be lost through evaporation. The vapour would be easily dissipated through the introduction of the puncture in the capacitor lid. Fig2.12 shows a graph of change in ESR over time. The one clear downside of this method was that puncturing the capacitor lid would mean that the dissipation of heat in the capacitor would be much less predictable and would result in an increase in the risk of an explosive failure of the capacitor. This meant that this method was considered to be unsuitable for ageing capacitors for this study.

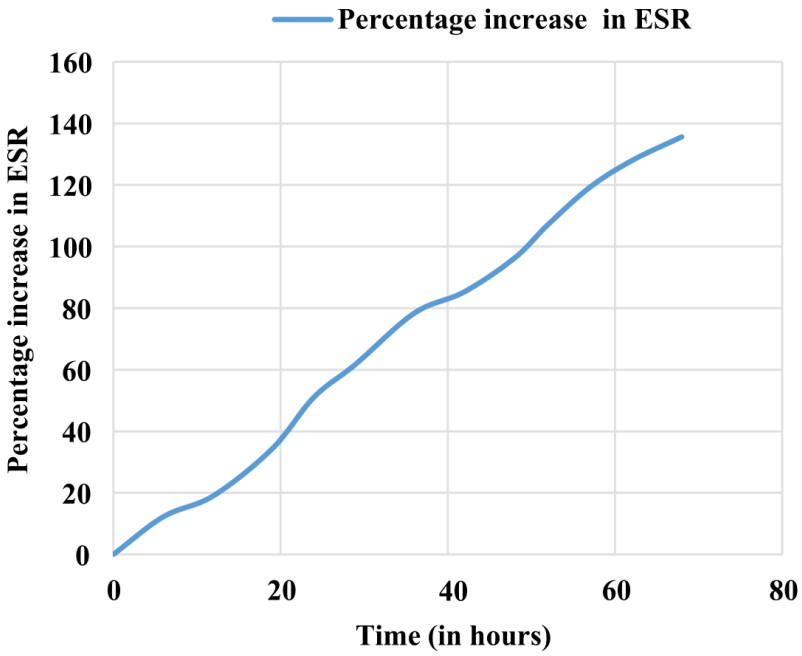


Fig2.12 - Change in ESR over time using a punctured capacitor [53]

[54] investigated ageing under a range of conditions, including where test capacitors were either held at a high temperature; under a forward bias voltage at a high temperature; or held subject to a square wave ripple at a high temperature. ESR and

capacitance were measured over the course of a few thousand hours, using a batch of 26 test capacitors. [54] did not delve into specifics beyond observing for changes in impedance over time as this was the stated aim of the paper. However, consideration was given to the Arrhenius rule [55] in terms of relating capacitor life to temperature.

In [56], a test setup was devised where the setup was used to accelerate the ageing process of test capacitors. The DC-link of a motor drive was used in conjunction with an isolated AC ripple power supply so test capacitors would be subjected to a large DC forward bias voltage and a constant ripple current. The test bench schematic is shown in Fig2.13. The DC bias voltage and AC ripple current were placed across the capacitors for 5000 hours (approximately 208 days) before capacitance and ESR were measured.

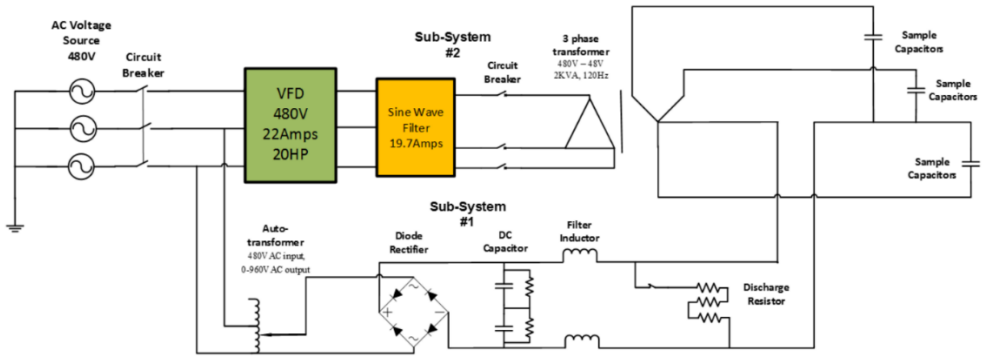


Fig2.13 - Electrical test bench setup [56]

Although the prognostics algorithm was interesting as a standalone topic – and is very relevant to section **2.6.3** – the accelerated ageing processes presented in [51] shared a similarity with [56] where they both made use of electrical stressing of the capacitor through maintaining an AC ripple current through the capacitor for an extended amount of time, although [51] took this a step further by making use of a ripple frequency of less than 1Hz. Additionally, [51] made use of thermal stressing for extended amounts of time: this would rapidly cause a change in the amount of liquid electrolyte within the capacitor can. However, a clear problem with the methods presented in [46], [56] and [51] is the extended amount of time required for ageing of capacitors, where 4000 hours is approximately 166 days; 2000 hours is approximately 83 days; and 5000 hours is approximately 208 days.

[57] went in a different direction altogether, starting with a physics-of-failure (POF) model – where the concept of POF models is best described in [58] – and then looking instead at applying a reverse bias voltage of 12V and a maximum current of 18mA to

electrolytic capacitors. An increase in ESR of approximately 80% was achieved within 50 hours, as shown in Fig2.14. The rest of the paper went on the describe error statistics involved in mean-time-to-failure calculations, which is a component-specific issue.

As the authors of [57] noticed, and as was described in section **2.2**, the dielectric medium effectively acts as a diode and current will not flow if a reverse bias voltage is applied until the reverse bias voltage meets and exceeds a threshold voltage, normally of 1.5V. By applying a reverse bias voltage and allowing current to flow from cathode to anode, a layer of the dielectric medium developed on the cathode. The development of this layer was an exothermic process, causing an increase in temperature of the electrolytic liquid. As this increase in temperature caused an increase in conductivity which meant more current flowed through the electrolyte from cathode to anode, the temperature of the electrolytic liquid kept increasing. To try to regulate the temperature, the maximum current was limited to 18mA, although the reasoning behind this specific value was not explained. In this manner, the dielectric medium was made use of in a different way as described in [50] for the purpose of degrading the capacitor impedance. Overall, this method was considered to be very interesting in principle but also impractical due to the fact that an assumption would have to be made that all test capacitors would be perfectly identical and able to maintain the same reverse bias voltage and maximum current. Perhaps for this reason, [57] only used two test capacitors.

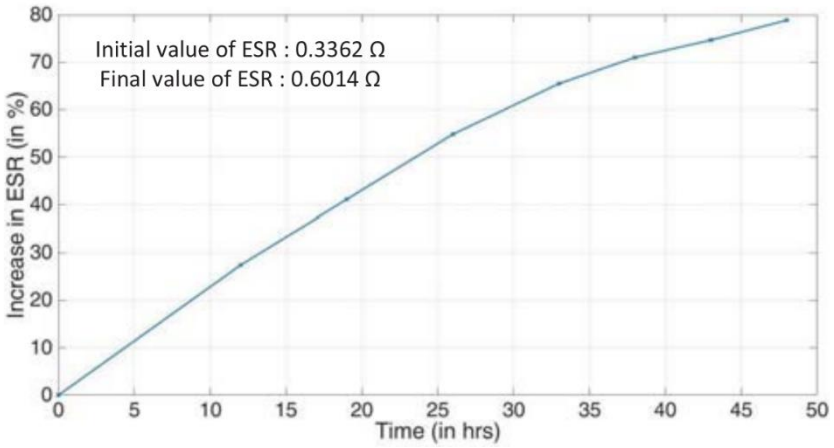


Fig2.14 - Increase in ESR using a reverse bias voltage [57]

2.6 – Detection of degradation in-situ in power converters

In the context of motor drives, different methods exist to estimate the impedance of the equivalent circuit representation shown in Fig2.3. These schemes vary in complexity and also in terms of how impedance identification is carried out, with some methods focusing on monitoring frequencies in electrical waveforms whilst others consider changes in capacitor core temperature arising from the chemical reactions within the capacitor. For example, [59] is an excellent review of many general methods which may be used to determine the impedance of an electrolytic capacitor. However, these general methods are not necessarily directly implementable in power converters.

In this section, it is assumed that detection of degradation would take place in-situ within a power converter. Examples of relevant impedance estimation schemes will be presented.

2.6.1 – Impedance estimation using measurement of DC-link capacitor current

Typically, vector-controlled motor drives with diode-rectifier bridge input stages do not make use of the measurement of DC-link capacitor current as it is only the measurement of DC-link capacitor voltage which is necessary for use in motor control [1]. As a result, an impedance estimation scheme making use of this additional sensor would be impractical. Regardless, it is worth examining some examples of schemes which do use the additional sensor.

Separately in [60] [61] [62], authors proposed measuring capacitor voltage and current for the purpose of finding the integral of power and the integral of the square of the measured current, where these two calculated values would be used to find an estimate of ESR; this process is shown in Fig2.15. In [61], it was pointed out that the integration step would effectively act as a low-pass filter, meaning that specific filtering of frequencies through use of bandpass filters would not be required to extract specific frequencies of interest. Additionally, it was pointed out that digital implementation of the repetitive small-time integrations would be trivial, meaning that this method would be practical and computationally cheap.

Ignoring the dependency on measuring the capacitor current, this method seemed quite interesting as it considered finding average power losses in an attempt to find an estimate of average ESR. However, when it is considered that ESR is frequency and temperature dependent, it is clear that this method is mathematically interesting but

it would be difficult to show the usefulness of this method in practice using a current with high harmonic content and a varying core temperature.

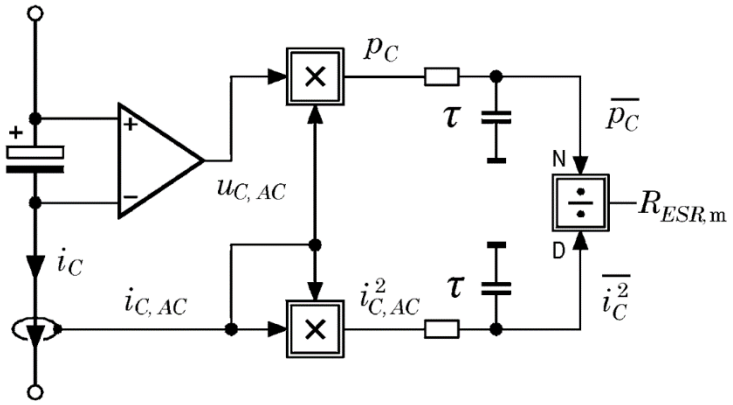


Fig2.15 - Proposed calculation of ESR via power losses [61]

In [63], a batch of capacitors had their capacitance measured as core temperatures were varied in a controlled manner. Estimates of capacitance were generated based on measured values of capacitor voltage and current, after which estimates of core temperature were made by comparing the estimated capacitances with the measured capacitances. The estimated core temperature was then compared with the measured core temperature to give an idea of the error in estimate of capacitance. The schematic and estimation procedure are shown in Fig2.16.

Ignoring the dependency on measuring the capacitor current, this method seemed quite interesting as it initially considered finding the variation of capacitance with temperature using a batch of capacitors, and then looked at finding accurate estimates of capacitance by comparing the measurement of temperature with the estimate of temperature. However, the dependency on having an additional temperature measurement meant that this method was limited in practice.

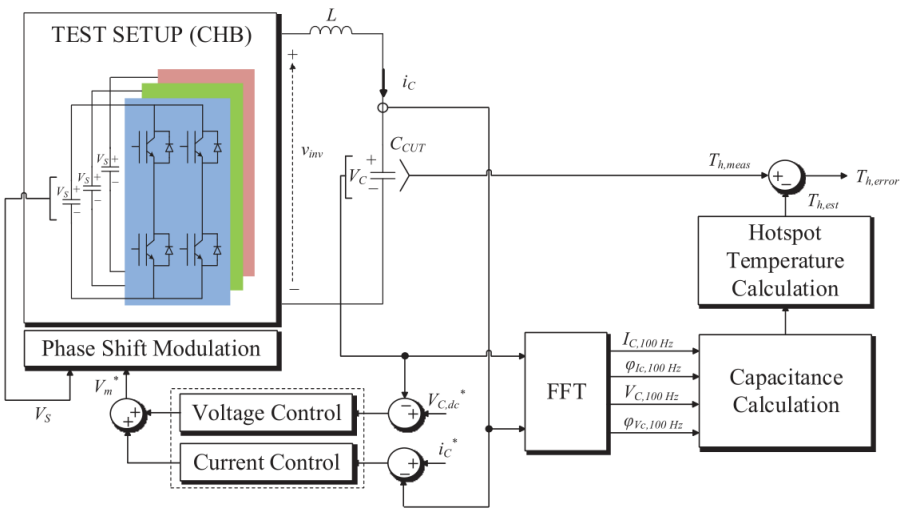


Fig2.16 - Schematic and hotspot temperature estimation procedure [63]

[38] considered estimating ESR using two methods: the first being through making use of peaks at the third harmonic of switching frequency, and the second being through measuring capacitor voltage, capacitor current, and then calculating the phase difference between these two quantities. The voltage across the ESR would be calculated by multiplying the cosine of the phase difference with the capacitor voltage, and finally the ESR would be estimated by dividing the calculated ESR voltage by the measured current. The method which was chosen was the second, which made use of measurements of capacitor voltage and capacitor current. Fig2.17 shows the block diagram representation of the ESR presentation scheme.

Variations of this method are common in literature, where the shared problem is that this method depends on measuring the current through the capacitor. In an industrial motor drive, this would be impractical: typically, control schemes of vector-controlled motor drives require only a measurement of at least one phase of the motor current [1], meaning introducing an additional current sensor to monitor the current through the capacitor would incur additional cost.

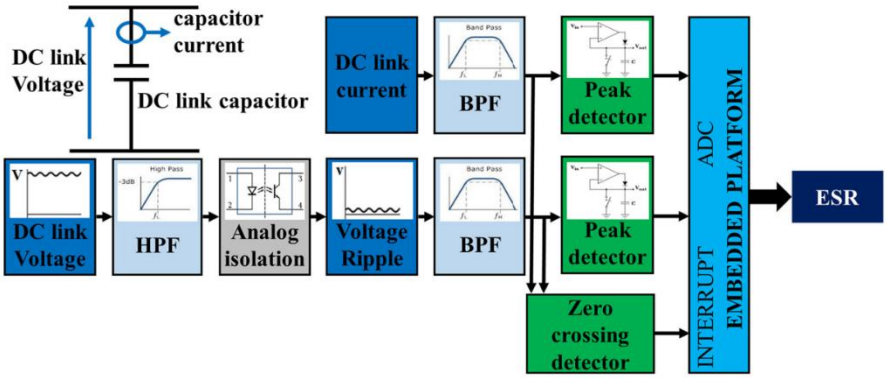


Fig2.17 - ESR estimation scheme using bandpass filtering [38]

The same authors from [38] continued their work in [64], where a method was described which made use of a Foster network [65] [66] representation of the capacitor thermal impedance, shown in Fig2.18. Using a DC-link capacitor within a motor-drive, the AC components of the DC-link capacitor were used in conjunction with the capacitor case temperature to compute an estimate of core power loss. An equivalent thermal model was fitted using the estimates of power loss and measured case temperature, after which estimates of core temperature and ESR were calculated.

As was noted for [38], this paper required measurements of the capacitor current to find estimates of ESR, which meant that this method depended on the presence of an additional current sensor. Additionally, this method also relied on attaching a thermocouple to the exterior of the capacitor can. The choice of type of thermocouple was not mentioned, which is a problem as the specific choice of thermocouple affects precision of temperature measurements. As the method required the use of a manually attached thermocouple, this method would only be practical as a proof-of-concept.

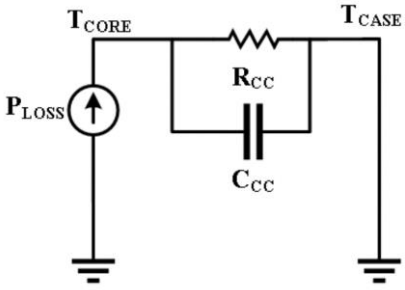


Fig2.18 - Foster network representation of the capacitor thermal impedance [64]

Other examples of relevant works in terms of impedance estimation of electrolytic capacitors in converters include [67], which looked at capacitor sizing for an electric-

vehicle motor drive and also presented an iterative ESR-estimation scheme as part of first a power-loss model and then a capacitor thermal model.

[68] also explored thermal modelling, looking at estimating the sum of power losses across a range of frequencies. The current used to estimate power losses is itself estimated using measured values of capacitor voltage and known values of input power from a photovoltaic (PV) panel. The sum of the power loss across a range of frequencies would then be used as an input in a thermal model, where instantaneous capacitor core temperature would be estimated.

In [69] [70] [71], the authors first made use of the application of Short Time Least Squares Prony's transform and then a Short-Time Fourier Transform, where each transform was applied to capacitor voltage and current. Frequency content was extracted, specifically switching frequency content as well as rectifier frequency content, with the switching frequency content being used to estimate ESR and the rectifier frequency content being used to estimate capacitance. [70] also extended into proposing a method for use in condition monitoring of capacitor health.

2.6.2 – Impedance estimation using signal injection

[72] made use of the known relation between capacitor current and the rate of change of capacitor voltage, showing that estimates of ESR and capacitance may be found through waiting until the motor at the output of the inverter is not in use and then injecting a constant duty-cycle DC voltage to the stator winding. Fig2.19 shows the equivalent circuit of the drive and attached motor during DC injection. Impedance estimation would take place using the average capacitor voltage; the duty ratio and switching period of the inverter; and the DC component of the inverter current. Specifically, this method would be used at moments when the drive rectifiers would not be conducting as the inverter current could be used as an approximation of the capacitor current.

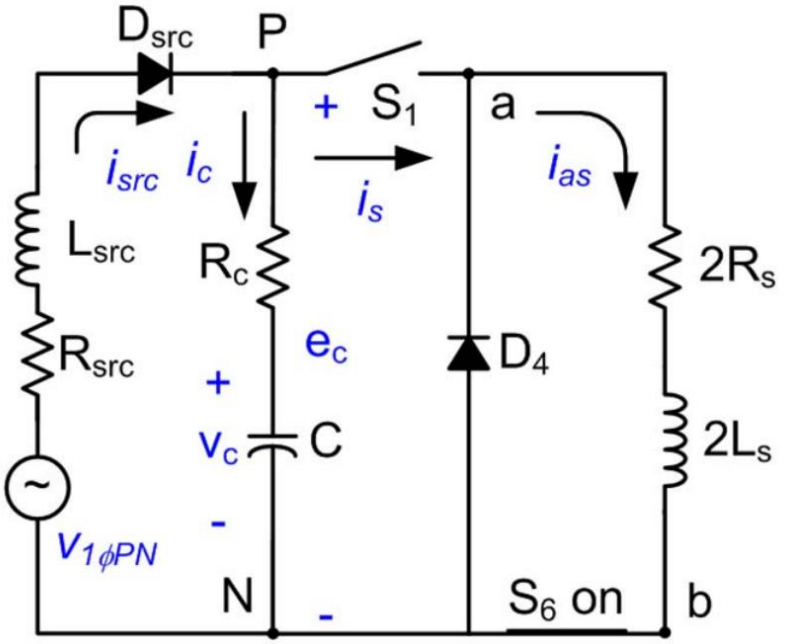


Fig2.19 - Equivalent circuit during DC injection [72]

This method made use of an estimate of capacitor current and measured capacitor voltage, as well as duty ratio and switching period time. No additional sensor was required to measure the capacitor current. Due to this reason, this method seemed very feasible to implement on an industrial motor drive. However, one immediate problem with this method is the reliance on waiting until the motor is not in use, as this would pose a problem in applications where the motor is in constant use whilst the motor drive is powered. Otherwise, this was considered to be a very interesting and straightforward method to avoid having to measure the capacitor current directly.

[73] approached the problem of detecting changes in DC-link capacitance through a control perspective, considering very simply a converter connected via an active-front end rectifier to a three-phase mains supply as shown in Fig2.20. An AC ripple was injected into the reference quadrature current and the ripple was allowed to perpetuate through the capacitor voltage and current. A recursive least squares algorithm was used to estimate ESR based on measurement of capacitor voltage and estimate of capacitor current. This ESR estimate via electrical means would then be compared with thermal and datasheet values of ESR for error-checking.

This method relied only on a converter with a DC-link; a controlled switching stage; and a three-phase controlled voltage source. As a result, the method outlined in [73] can be interpreted to have shown that if the motor at the output of the converter is considered to be simplified into a voltage source (back-emf) and lumped impedances,

and if only vector control of currents are considered, then the capacitor current may then be estimated using only knowledge of currents and switching states.

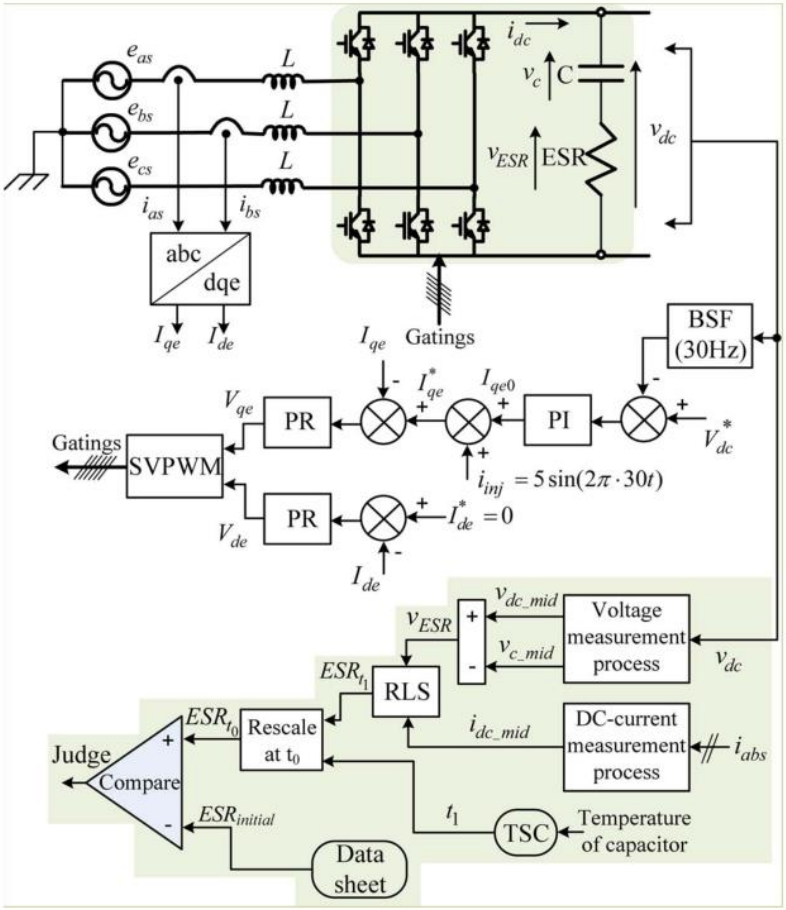


Fig2.20 - Schematic and injection procedure of an active front-end [73]

Authors from [73] continued on in [74], where they again approached the problem of detecting changes in DC-link capacitance through a control perspective, looking here at injecting an AC ripple into the reference stator quadrature current and allowing the ripple to perpetuate through the reference motor voltage into the motor electric torque. The injection signal would be triggered during the regeneration period as motor speed reduced. Inverter current would be calculated using knowledge of switching states and motor currents, and the calculated inverter current would be used as an estimate of capacitor current. Using the estimate of capacitor current and a measurement of capacitor voltage, a recursive least squares algorithm would be applied to generate an estimate of capacitance. The schematic and injection procedure are shown in Fig2.21.

This method made use of measured capacitor voltage, switching states, and measured motor currents. No additional sensor was required to measure the capacitor current. Due to this reason, this method seemed very feasible to implement on an industrial motor drive. However, this method could be improved by making use of a AC ripple injection during normal motor operation instead of specifically during regeneration periods. The reason given for limiting the injection period to regeneration periods was to prevent current flow into the DC-link from the diode rectifier bridge, assuming similar frequencies as the injection may be conducted and show up as disturbances.

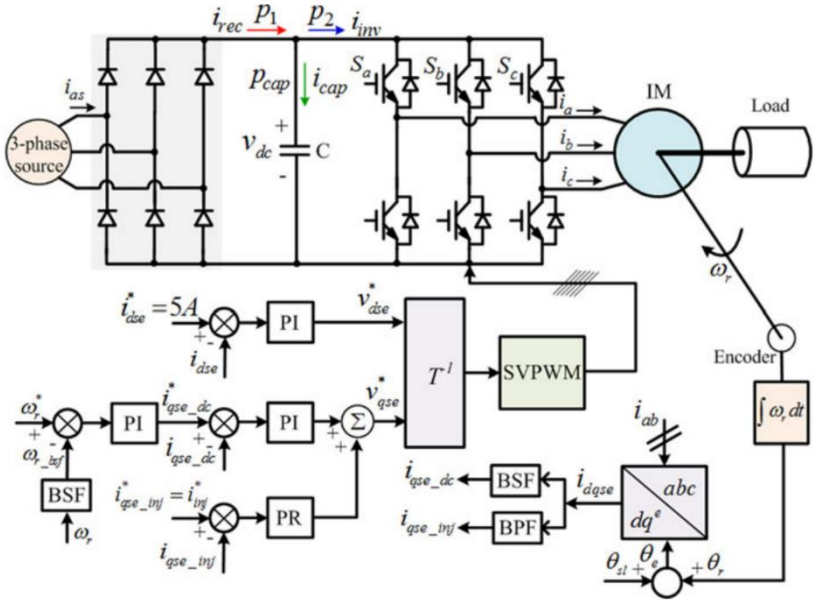


Fig2.21 - Schematic and injection procedure of the motor drive system *[74]*

[75] made use of injection of low-frequency signals using a boost converter for a PV system instead of a motor drive. Here, a low-frequency perturbation signal was injected into the switching duty cycle, causing a ripple in PV voltage and current, as well as inductor current; this is shown in Fig2.22. This PV and inductor currents would be used to calculated the capacitor current, and the impedance of the capacitor would be estimated using the PV voltage and calculated capacitor current at the frequency of perturbation. As the method made use of a boost converter, discussion was made on the effect of sampling quantities whilst the converter was operating in continuous or discontinuous current modes. Discussion was also made on the monitoring of capacitor health over time.

Relying on the injection of a low-frequency perturbation signal, this method was interesting as it demonstrated the use of signal injection in converters other than

AC/DC/AC converters as seen with drives. Additionally, the discussion that was made of ongoing monitoring of capacitor health as perturbations were injected over time was interesting on its own as it would be useful to judge state of health based on the frequency response of a known and controlled frequency independent of converter dynamics.

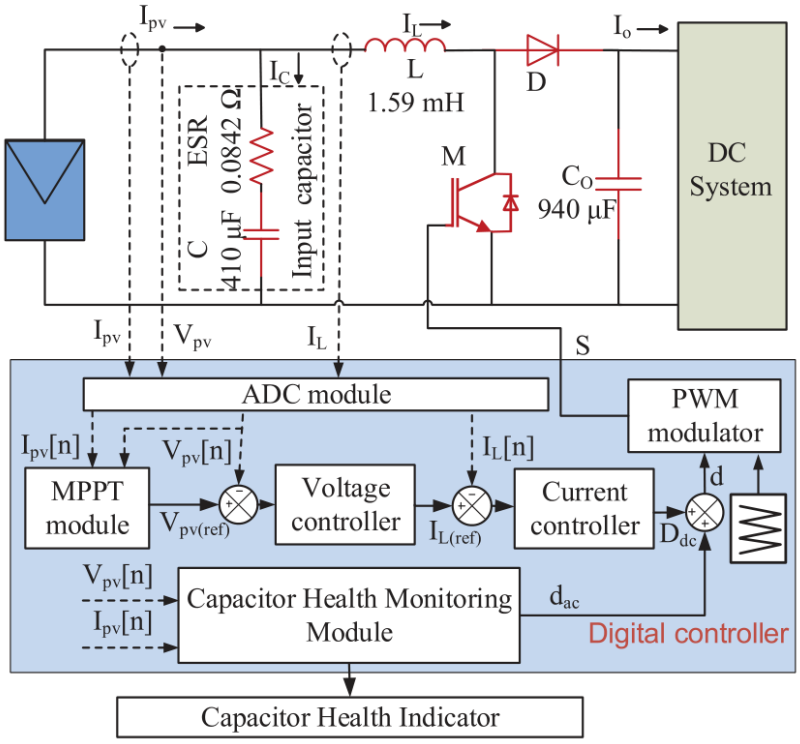


Fig2.22 - Schematic of the boost converter system [75]

Whilst [74] considered a system making use of injection of a ripple where a diode rectifier bridge was used at the input stage of the motor drive, [76] considered making use of injection of a ripple in a system where a PWM rectifier bridge was used instead. Here, control of the PWM rectifier switching states was used to inject a low-frequency ripple into the reference direct voltage and then also inject another low-frequency ripple into the direct current. The direct current (with a ripple imposed upon it twice) and the quadrature current (without a ripple imposed upon it) would be used by the PWM rectifier to maintain a voltage across the DC-link capacitor, where a specific low-frequency ripple would be present in the voltage. The capacitor current would be calculated using measured rectifier and inverter current measurements. Estimates of capacitance would be generated using calculated capacitor current and measured voltage across the capacitor, specifically at the frequency of the injected ripple. The drive schematic is shown in Fig2.23.

This method was unconventional when considering a typical industrial motor drive which may not make use of PWM rectifiers but would instead make use of a diode rectifier bridge at the input stage of the drive. However, the common theme between [74] and [76] was injection of a ripple signal into the system and using the ripple frequency for estimation of DC-link capacitance. [74] limited itself to periods of motor regeneration, and [76] made use of an injection into the DC-link but made use a capacitor current that was calculated using the rectifier current which would not necessarily be available within a normal drive. Overall, both methods relied on only making use of measurements that were available to the drive, meaning that each method had merits.

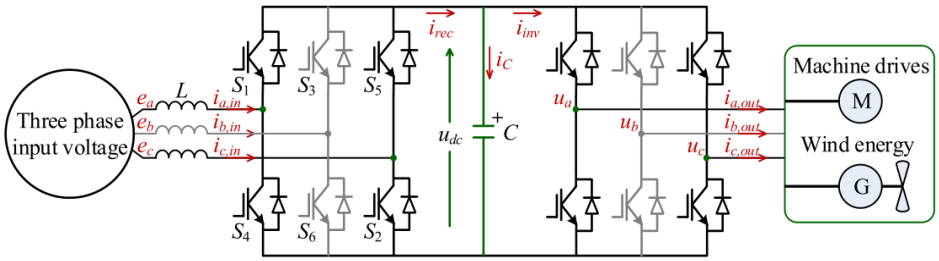


Fig2.23 - Schematic of the motor drive system [76]

2.6.3 – Impedance estimation as part of an intelligent system

As the stated aim of the project involved devising a strategy to be used to monitor impedance over time, it is useful to understand some of the variety of on-line monitoring systems described in the literature.

[77] and [78] are examples of methods which are popular in the literature where intelligent systems such as artificial neural networks [79] (ANN) are employed to solve specific problems. [80] states that ANN are used where it is best to minimise the use of specific current sensors, which in this case would mean eliminating the use of a current sensor measuring the current through the electrolytic capacitor. [77] describes a method which measures three voltages in a power converter and uses an ANN to estimate the capacitances of the DC-bus capacitors, with an alarm triggering if estimates pass a threshold value. Similarly, [78] makes use of an ANN which takes in values of grid currents and voltages, DC-link voltage, and also motor currents and voltages and then outputs an estimate of capacitance.

Incidentally, and in the larger context of motor drives, ANN may also be used for monitoring the drive system for faults related to the motor, with examples such as [81]

and [82] setting out to provide some ANN design considerations and [83] building upon these ideas to show the use of ANN in monitoring for changes in the motor current vectors and classifying state of health based upon the current vector arcs. Additionally, and still in context of motor drives, ANN has been commonly used in literature to estimate machine impedance during motor commissioning, as shown in examples such as [84] [85] [86] [87] [88].

The main problem with making use of methods such as the ANN is the training time required on a desktop computer to train the model to generate acceptable answers, as well as the complexity of producing a model which may be deployed in real-time on an industrial drive with limited computing power [89]. Another issue with ANN models is that the range of possible models vary according to number of layers and nodes, as well as the choice of input variables. Fig2.24 shows an example of a structure of an ANN with many nodes and three layers. As models have to be trained to produce correct outputs, ANN models have many different levels of complexity compared to traditional circuit phenomena based models. Otherwise, methods such as the ANN are very interesting if considering exporting data to a desktop computer for further processing and analysis.

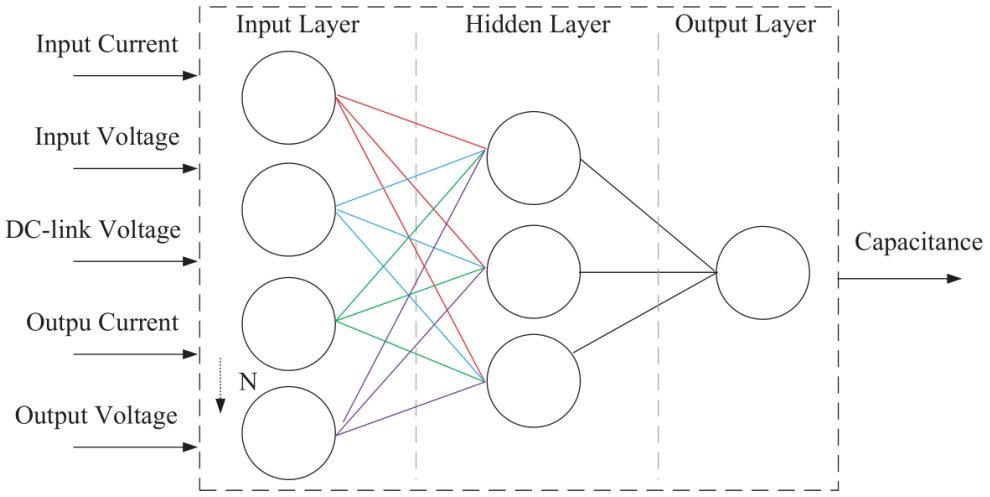


Fig2.24 - Example of the structure of an ANN [78]

An example of a more circuit-phenomena-oriented system capable of providing an outlook on capacitor prognostics was [51], where an accelerated ageing scheme was defined for use with a prognostic system. Here, a Kalman filter [90] was applied to digitally filter and predict the potential end-of-life of capacitors, where the end-of-life was defined as a loss of 20% of capacitance, through the use of the Kalman filter as a

forecasting algorithm. Fig2.25 shows an example of the usage of a capacitance loss forecasting algorithm. The accelerated ageing scheme made use of a DC-DC converter to provide a nominal 5VDC to the test capacitor, along with a configured ripple and noise [91], and the state-space models used by and implemented as part of the forecasting Kalman filter were described as part of a prior work [92]. Overall, the method shown in [51] provided a remaining useful life prediction could be made for a DC-bus as part of an overall health monitoring system.

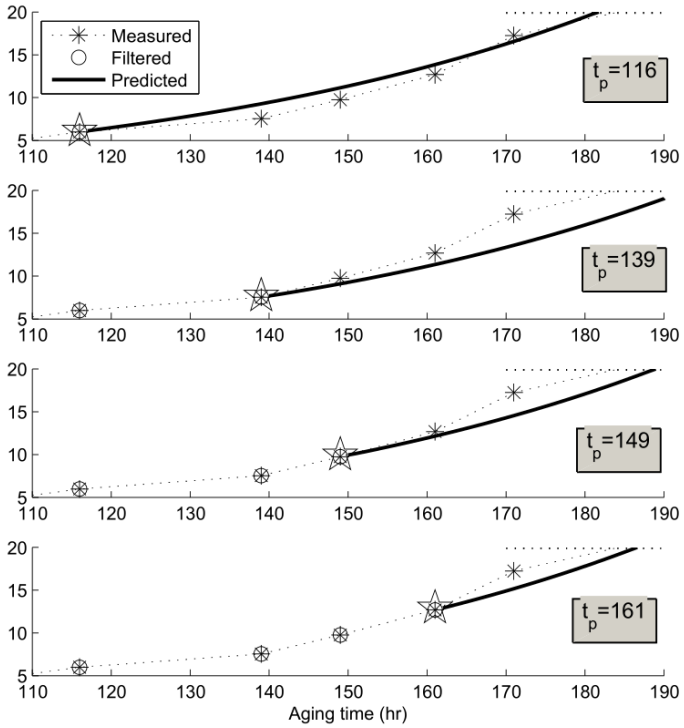


Fig2.25 - Example of the usage of a capacitance loss forecasting algorithm *[51]*

[93] also made use of a digital filter, where it was proposed that the Goertzel algorithm - stated to be computationally efficient compared to the DFT and FFT, with the full theoretical explanation being presented in [94] – would be used to extract specific harmonics from the capacitor current and voltage for use in separately estimating ESR and capacitance. After this extraction, a measurement of capacitor case temperature would be used with the estimate of capacitance to estimate core temperature. The estimated values of resistance, capacitance, and core temperatures would be saved for ongoing learning, and used to generate estimates of present health status for use as part of an expert system. The diagram of the proposed system is shown in Fig2.26.

This method shared the problems of requiring an additional temperature measurement sensor and an additional capacitor current measurement sensor, with the difference being the use of a digital filter to computationally extract specific harmonics from electrical waveforms for use in a health monitoring scheme. In the context of using intelligent systems with motor drives, [93] clearly laid out the problems involved in developing a health monitoring scheme capable of generating and making use of accurate estimates of impedance.

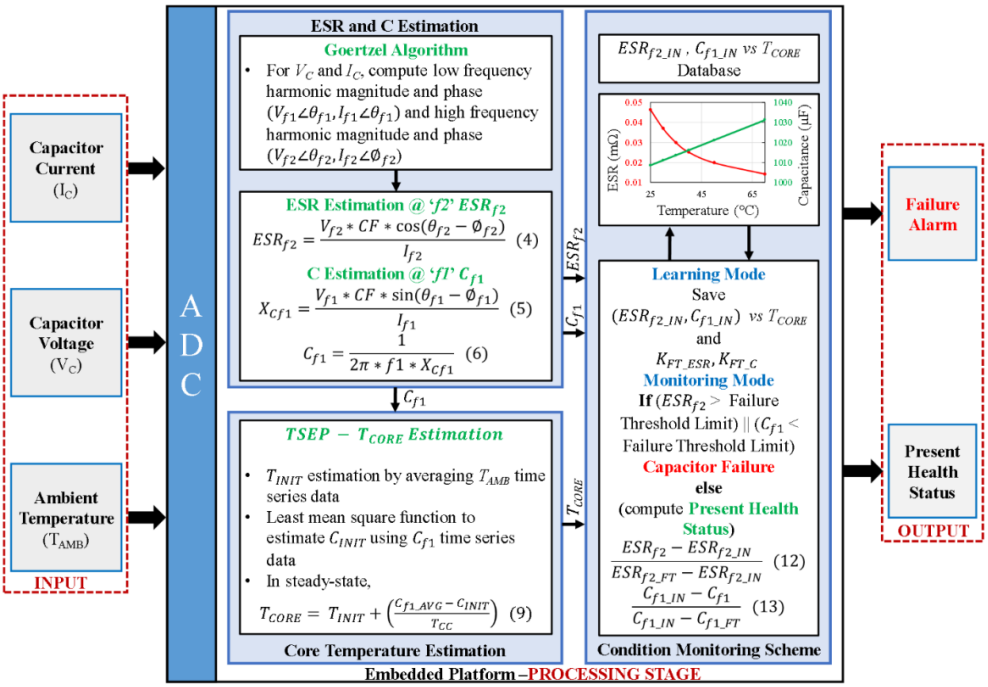


Fig2.26 - Diagram of the proposed conditioning monitoring scheme [93]

In terms of monitoring schemes, it is worth referring back to [70] where a method was proposed for generating estimates of impedance for use in condition monitoring of capacitor health. As shown in Fig2.27, a thermal model was used in conjunction with an electrical model to allow an ongoing comparison of estimates derived from the electrical model with threshold values derived from the thermal model. [70] was unclear, however, on how the thermal model coefficients are derived.

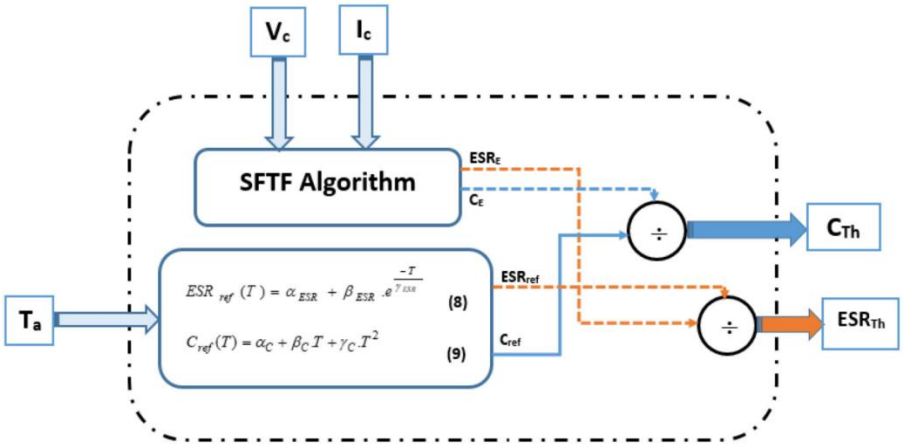


Fig2.27 - Diagram of the proposed capacitor health monitoring scheme [70]

As a slightly different example of working towards the goal of understanding variation in capacitor impedance using intelligent systems, [13] looked at modelling the full power converter system by taking into account the capacitor's equivalent circuit; the model of the motor drive; the heat transfer model [95]; and also the life model. A flowchart of the proposed method for predicting expected life is shown in Fig2.28. The purpose of this work was to provide a framework for building a model of prediction of life for electrolytic capacitors, with the only drawback being that a deeper understanding of capacitors would be required to fully test and implement the heat and lifetime models as described. Throughout, the author was interested in building POF models which involved looking into the physical phenomena involved in failure beyond just the electrical.

The heat model described in [95] drew upon an investigation of heat dissipation in capacitor cans as presented in [96]. [96] considered an electrolytic capacitor as two concentric cylinders, looking at first the heat loss from a bare can and then examining the effect of varying thicknesses of sleeving on the heat flow. It was shown how the presence of sleeving can have a beneficial effect on the heat dissipation in the capacitor, and how this is useful when considering the ripple current of a capacitor. In context of monitoring the degradation of a capacitor, capacitor heat models are interesting as they are not well understood due to the unknowability of specific manufacturing methods, and in this context [96] attempted to quantify the effect of heat dissipation in electrolytic capacitors and then later [95] and [13] attempted to work in this knowledge into an POF model relating to heat.

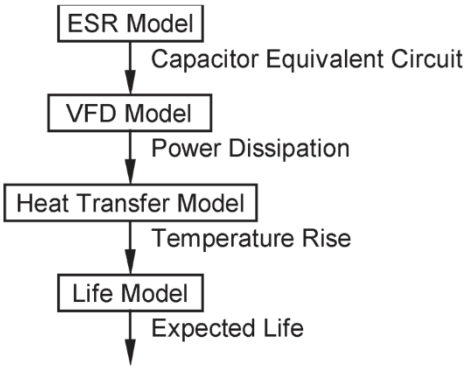


Fig2.28 - Flowchart of the proposed method for predicting expected life, considering POF *[13]*

Another interesting approach to developing a system for use in degradation detection was shown in [97], where the authors produced an algorithm which took into account the changes in capacitance and resistance of a capacitor bank as a function of time; temperature stress; surface area and distance between plates of the test capacitors; and also permittivity of the liquid electrolyte. This algorithm was continually updated over time until a criterion was met where this POF model could report an estimate of time-to-failure. Fig2.29 shows the proposed flowchart of this algorithm.

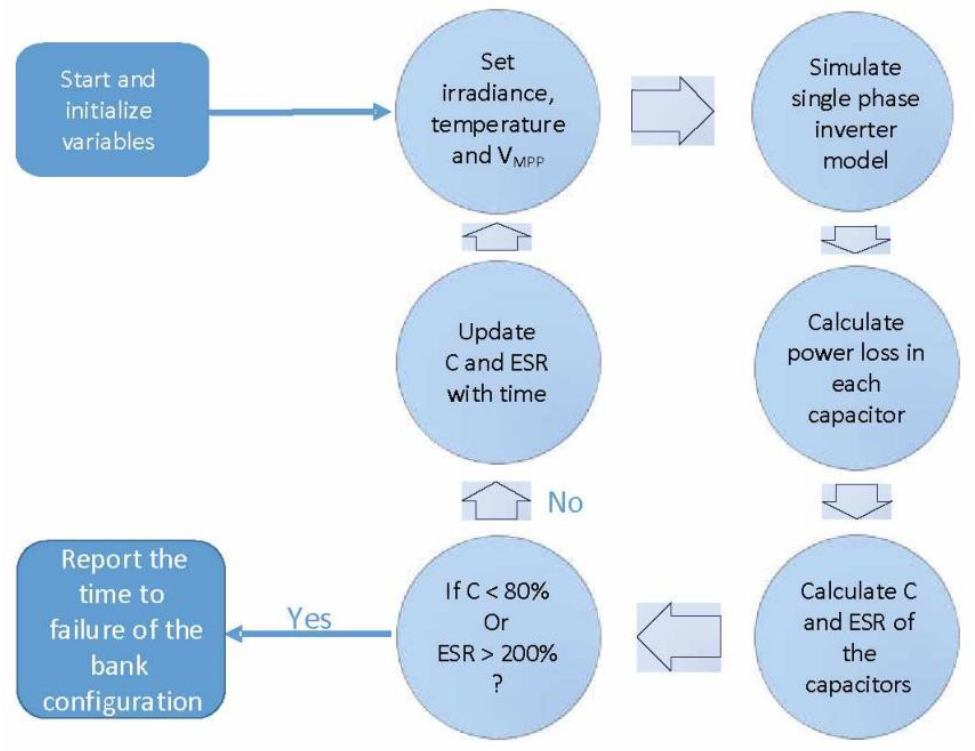


Fig2.29 - Flowchart of the proposed POF model in [97]

2.7 – Detection of degradation using chemical characterisation

Electrolytic capacitors are widely used to maintain DC voltages in electrical power converters but are clearly electrochemical devices. As a result, chemical characterisations may be taken of test capacitors to better understand changes in the capacitor on a physical level.

For example, [34] made use of ripple currents and heat to accelerate the ageing of batches of capacitors. Scanning electron microscopy (SEM) was used to identify damage in the dielectric layer, and infrared spectroscopy (IR) was used to compare the spectra of liquid electrolyte taken from damaged and undamaged capacitors. An example of the spectra is shown in Fig2.30, generated using IR, where the frequency responses of four different capacitors are shown. One capacitor was undamaged, whilst the other three had been damaged via application of temperature or voltage or ripple current.

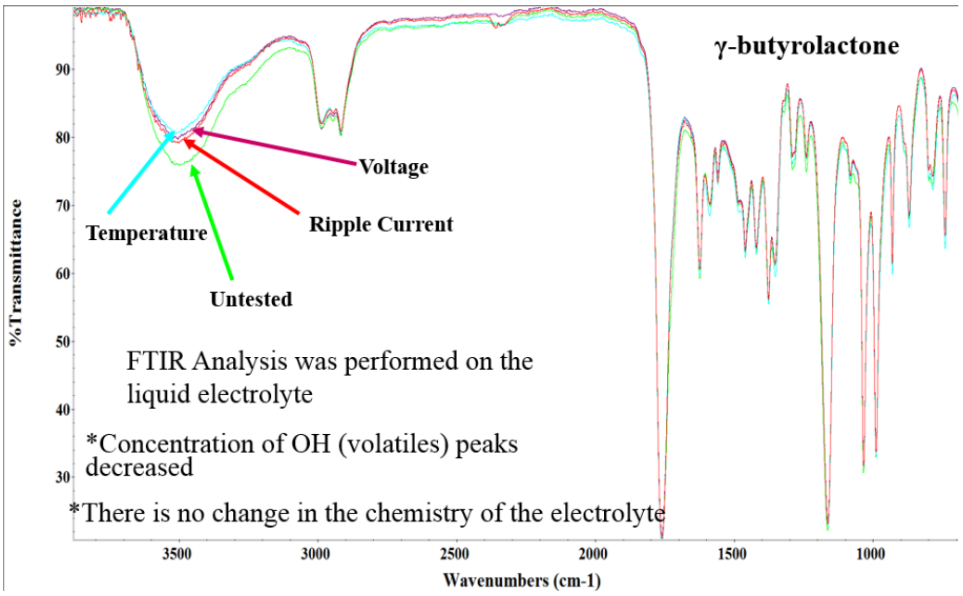


Fig2.30 - Chemical analysis of liquid electrolyte taken from different capacitors [34]

[98] also made use of the application of heat and ripple currents to batches of capacitors, except here the authors made use of energy dispersive X-ray (EDX) spectroscopy and nuclear magnetic resonance (NMR) spectroscopy. EDX was used to examine the anode and cathode layers as part of an investigation into effects of defects upon capacitance; and NMR was used to identify the type of liquid electrolyte by comparing the spectra against the spectra of known chemicals, as shown in Fig2.31.

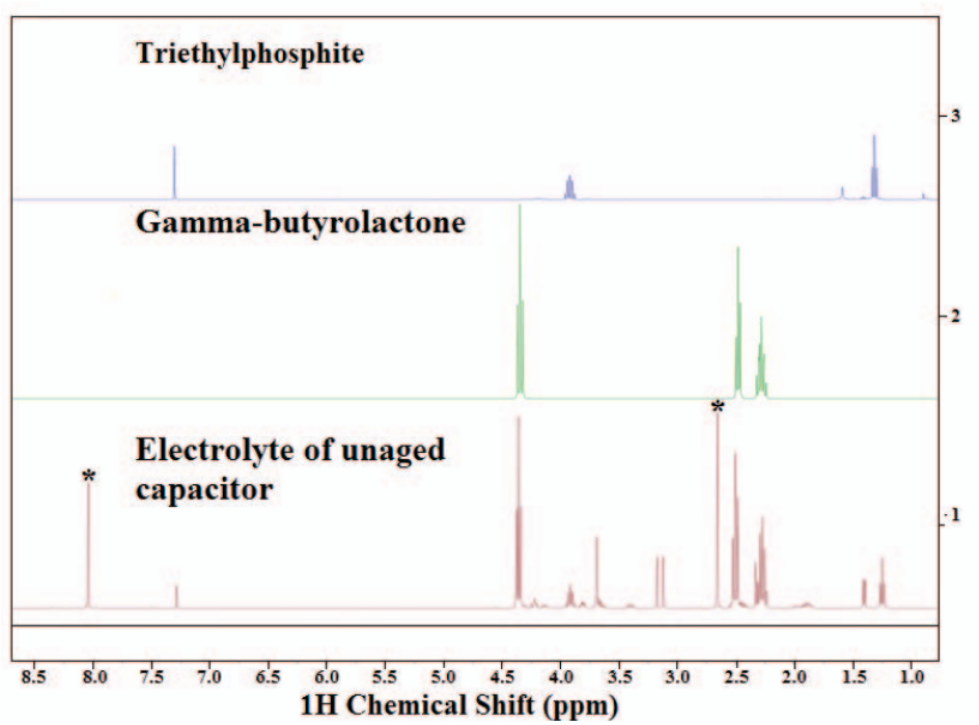


Fig2.31 - Comparisons of measured spectra with spectra of known chemicals [98]

As the motivation of this project had a clearly electrical context, only a very shallow reading was taken of the detection of degradation using chemical characterisation. However, considering [34] and [98], alternative methods to the electrical are clearly available for failure analysis through considering the chemical aspect of electrolytic capacitors. Although the methods used were clearly destructive tests carried out in laboratory settings outside of a power converter, they considered the specific material phenomena that were considered as part of POF models in examples such as [13] [95] [97].

2.8 – Detection of degradation in terms of reliability engineering

POF models have been mentioned as the basis of some methods which make use of an understanding of fundamental physical mechanisms to gauge changes in relevant system parameters.

Much literature exists on the subject of reliability across ranges of applications [99] [100] [101], with an example in literature of a mathematical model relating reliability to electrolytic capacitors being the Arrhenius model [55]. This model relates lifetime of a component to temperature, and is often cited when considering mean-time-to-failure (MTTF) of electronic components. According to the example of the model

shown in [55], this model is best used as a general rule-of-thumb as it generally only considers variation in temperature in determining MTTF.

However, the Arrhenius model may be adjusted to account for more variables such as applied voltage, and the effect of derating the capacitor in terms of life multipliers due to ambient temperature, ripple current frequency, as well as air speed cooling may be found as shown in [102]. In context of motor drives, the concepts developed in [102] were used in [103] to help evaluate the lifetime of electrolytic capacitors placed within a low power regenerative motor drives, where it was confirmed that capacitor lifetimes decrease during operation and high ambient temperatures. Overall, however, the Arrhenius model is dependent on temperature and so it is primarily used where variations in capacitor core temperature are taken into account; of course, this requires measurement of capacitor core temperature or at least a very accurate estimate of capacitor core temperature. Examples of the usage of the Arrhenius model specifically due to variations in core temperatures may be observed in varied sources such as [104] [105] [106] [107] [108].

In terms of general reliability engineering for the purpose of health monitoring and prognostics, statistical methods may be used to forecast likelihood of failure according to historically gathered empirical data. One such statistical method is survival analysis, which relies upon having a knowledge of moments of past failure events and their specific times over a life in order to build a model of MTTF, where an explanation of survival analysis in relation to reliability engineering is presented in [109] and where a rigorous mathematical explanation of the subject is presented in [110].

As the motivation of this project had a clearly electrical context, only a very shallow reading was taken of the detection of degradation in terms of reliability engineering. Additionally, the dependency on having an accurate measurement or estimate of capacitor core temperature is a limiting factor given that a standard industrial drive may not have access to this variable. However, this section has been included in this chapter to emphasise the overall context of reliability engineering in relation to this project.

2.9 – Summary

Starting with an overview of the fundamental physical mechanisms of aluminium electrolytic capacitors, an equivalent circuit and a transfer function were defined for these types of capacitors. Equivalent circuit models additional to the originally defined equivalent circuit were also mentioned, showing that the frequency response of a specific capacitor may be interpreted to different levels of complexity as needed.

Issues regarding degradation were investigated, starting with failure modes of capacitors. Failure modes of capacitors were stated in terms of physical mechanisms, and it was mentioned how short circuits and open circuits manifest due to different aspects of the physical structure of the aluminium electrolytic capacitor. Evaporation of the liquid electrolyte; cathode depassivation; and voltage derating were also stated as other possible causes of failures. Clearly, each of these failure modes and causes of failures would show slightly differently in terms of electrical response in a power converter.

For the purpose of speeding up degradation of test capacitors to be used in this project, methods related to acceleration of degradation were understood, with the two common methods used involving application of thermal stress via high ambient temperature, and application of electrical stress via high DC voltage with a ripple current.

Using methods capable of estimating impedances of capacitors in-situ in power converters, detection of degradation was reviewed. Methods were shown which required additional current or temperature sensors to be fitted within a motor drive, where the presence of an additional current sensor was deemed to not necessarily be practical and the presence of an additional thermocouple was also questioned. Injection of a controlled ripple was also discussed using motor drives with two different types of input stages, where it was shown that the injection of a controlled ripple was interesting due to not requiring an additional current sensor to be fitted to the drive. The possibility of the use of intelligent systems was also discussed, describing briefly examples of various methods such as the usage of an ANN; digital filtering schemes capable of reporting estimates of present health status and learning using past knowledge; and also the use of POF models which are based on knowledge of physical mechanisms within the electrolytic capacitor.

The possibility of detection of degradation via chemical characterisation was also briefly acknowledged, although the methods that were mentioned were destructive tests that are interesting but impractical for use in-situ in a power converter. Mathematical models stemming from the field of reliability engineering were also briefly discussed.

Reflecting on the survey of literature in this chapter, it is worth reiterating the main research objectives, which were previously stated to have been:

1) To determine an appropriate technique for condition monitoring of electrolytic capacitors in an operational drive utilising an impedance estimation method.
2) To investigate the effect of accelerated ageing on electrolytic capacitors used in an operational drive.
3) To investigate the usage of the impedance estimation method applied to a drive in a laboratory setting.
4) To investigate the usage of the impedance estimation method applied to a drive considering practical measurement limitations.

In relation to objective 1) and 4), this chapter discussed various techniques that may be used to estimate the impedance of DC-link electrolytic capacitors in-situ within a drive. The reliance of many techniques on measurement of capacitor current was stated to be a problem due to the need for a current sensor which would not necessarily be present in the DC-link, whereas techniques relying on injecting signals into the DC-link were shown to rely instead on AC currents that would be measured as part of converter control schemes. Specifically, [74] was considered to be the most interesting of the works involving signal injection due to its usage of a uncontrolled diode rectifier at the input stage as opposed to the other works which made use of PWM rectifier input stages, where the use of an uncontrolled diode rectifier input stage is common in commercial motor drives. The main limitation of [74] was stated to be the restriction of injection to motor regeneration periods instead of allowing signal injection during normal motor operation, as any given motor powered and controlled by a motor drive may run in motoring mode indefinitely.

In relation to objective 2), this chapter presented different works which discussed methods of accelerating the ageing of electrolytic capacitors. Heating batches of capacitors for prolonged lengths of time at high temperatures were found to be the

most efficient in terms of time scales versus reduction in measured capacitor impedances, as shown in [51]. The main limitation of these methods was the prolonged length of time requiring many thousands of hours for each batch of capacitors, as such long timescales may not be feasible for rapidly producing batches of aged capacitors for use in operational drives.

Considering these two limitations observed in methods found in the academic literature, work was undertaken looking first at impedance estimation of electrolytic capacitors within motor drive DC-links in both simulation and practice, and then at speeding up the accelerated ageing process for use of aged capacitors in operational drives.

Work undertaken after having surveying relevant literature is presented in Chapter 3, and continues on in Chapters 4 and 5 to fulfil objectives 3) and 4).

Chapter 3 specifically addresses the main limitation of [51] – which was stated to be the prolonged length of time required for thermal stressing of batches of capacitors at fixed temperature – by mitigating the issue by heating capacitors at temperatures far exceeding their rated operating temperatures. As the intention of thermal stressing was to induce drying of the liquid electrolyte and therefore change capacitor impedance characteristics, this method was found to be a simple and straightforward mitigant.

Chapter 5 specifically addresses the main limitation of [74] – which was stated to be the restriction of signal injection to solely motor regeneration periods – by showing that a signal injection scheme may be used whilst a motor-under-test is operating in motoring mode, given an accurate estimate of the inverter current at the frequency of the injected signal. Whilst the authors relied on a motor regeneration period causing the inverter current and the capacitor current to be equal, the chapter showed that the limitation may be disregarded as the inverter current may be estimated using knowledge of the motor stator currents and transistor switching states.

Chapter 3 – DC-Link Impedance Estimation

3.1 – Introduction

This chapter will discuss impedance estimation using mathematical transforms, making use of measured capacitor voltages and currents. Equivalent electrical and thermal models of capacitors will be presented and discussed. Simulations and experimental work will be presented to better understand relevant estimation problems.

3.2 – Electrical analysis

3.2.1 – Overview

There are at least two forms of analyses that may be applied to electrical signals when dealing with impedance estimation: time-domain analysis, and frequency-domain analysis. To initially explore these techniques, a model of an inverter driven induction motor was created, where the model included a simplified representation of an AC grid supply and a drive DC-link.

The motor-drive simulation was created using the PLECS power-electronics simulation package [111]. Starting with a simplified model of the motor-drive, waveforms from the simulated drive were used to provide data for the methods developed in this work to estimate the capacitance and equivalent series resistance (ESR) of the DC-link. The next section describes the simplified drive model.

3.2.2 – Simulation of electrical models

A simplified model of an electrolytic capacitor was specified as shown in Fig3.1. This model had a capacitor in parallel with a very large leakage resistance, where the capacitor was placed in series with an ESR. The equivalent series inductance (ESL) was neglected as the inductive contribution to impedance would be very small in the frequency range of interest (<<1MHz), assuming an ESL in the low nano-Henries.

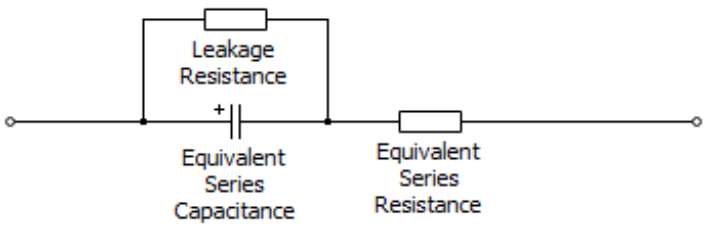


Fig3.1 – Simplified representation of an electrolytic capacitor

The outline of a motor-drive was designed and simulated using the PLECS power electronics simulation package. This motor-drive was designed to be powered by a 415V, 50Hz, 3ph source with a very small supply impedance and a very small cable impedance. A switching frequency of 4kHz was used, as was a 12kHz anti-aliasing filter, and a 100kHz sampling frequency.

The circuit shown in Fig3.2 is of a motor-drive with three stages: an input stage, where a rectifier is fed from a balanced three-phase voltage supply; a DC-link, where capacitors are in parallel with bleed resistors; and an output stage, where an inverter provides power to a vector-controlled induction motor. The resistors are used in a real drive to speed up capacitor discharge when the power supply is disconnected.

Fig3.2 does not include the high-frequency bypass capacitors which are placed in parallel with the network of DC-link capacitors and bleed resistors. The high-frequency bypass capacitors are part of the physical circuit, but their effect on the frequency analysis is limited as the value of the capacitances affect frequencies in the range >1MHz.

Specific component values are listed in Table3.1 and are from a G120C drive [112], where the specific values are listed and were simulated based on the original G120C circuit schematic [113].

In these circuits, each electrolytic capacitor is connected in series with a resistor used to represent its individual ESR, whilst each electrolytic capacitor is also connected in parallel with a large leakage resistance.

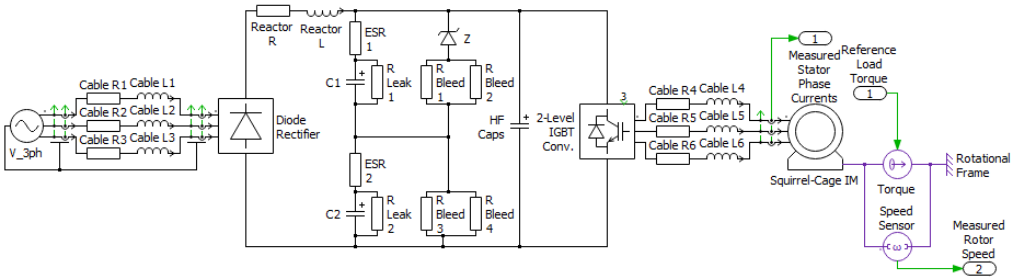


Fig3.2 – Circuit diagram of the simulated motor drive

C1, 2	Nominally 270uF, measured via EIS
ESR1, 2	Nominally 160mΩ, measured via EIS
Rleak1, 2	100kΩ
Rbleed1, 2, 3, 4	300kΩ
HF Caps	111nF
Reactor R	100mΩ
Reactor L	1mH
Cable R1,2,3,4,5,6	100mΩ
Cable L1,2,3,4,5,6	10uH

Table3.1 – Values used in Fig3.2

Resistive-inductive (RL) combinations are used to represent wire impedances: this is necessary for modelling the effect of stray inductances and power drops found in real-world cables and tracks. RL combinations were placed immediately before and after the rectifier. These RL combinations are normally included to reduce the harmonic content of the supply current [114]. In most cases, if a DC reactor is present in a drive, specific DC inductors are housed in the casing. Sometimes, it is assumed that the supply impedance is large enough to provide this filtering, or even cable and connection impedance in the drive itself.

Overall, a 4% reactor – meaning a maximum voltage drop of 4% between the point-of-common-coupling (PCC) and the drive, as advised by the project sponsors – was consistently assumed in this work, with the value of the reactor calculated by (3.1).

$$L_{reactor} = \frac{v_{phase}}{i_{max}\omega_{grid}} \cdot \frac{4}{100} = \frac{240}{23 \cdot 2\pi 50} \cdot \frac{4}{100} \approx 1.33mH \qquad (3.1)$$

where $L_{reactor}$ refers to the DC-link reactor; where v_{phase} refers to the RMS grid voltage; where i_{max} refers to the maximum grid current; and where ω_{grid} refers to the grid angular frequency.

Practically, the value of 4% is nominal, where the assumption of a maximum drop in voltage of 4% between the PCC and drive is subject to factors such as grid stability; cable sizing and/or length; and temperature and/or humidity. This may be observed in Fig3.3, where the DC reactors of a commercial motor drive - which were stated to be nominally 4% reactors - had their impedances measured over a frequency range of DC to 10kHz. The measured resistance of the DC reactors increased linearly as frequency increased, and the measured inductance decreased as frequency increased.

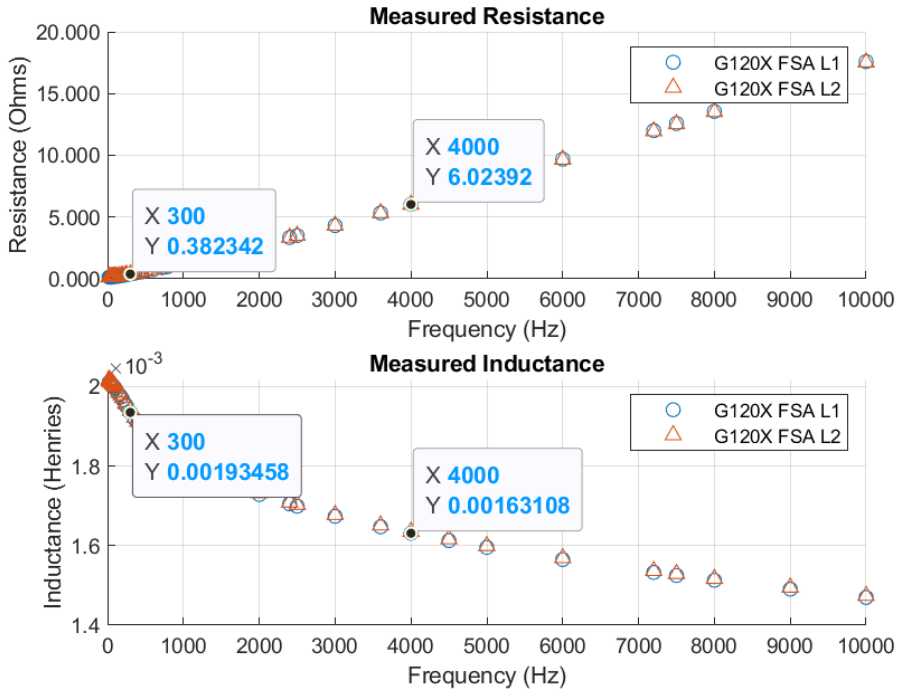


Fig3.3 – Measured impedances of a commercial DC reactor over a frequency range

As the resistance and inductance clearly varied significantly over the frequency range in Fig3.2, the nominal values included in the drive schematic [113] were simulated and have been listed in Table3.1.

The output of the simulated drive was connected to a 2.2kW induction motor with a controllable load torque profile, where closed-loop current and speed control were maintained through vector-control, specifically via the use of simulated current sensors and a rotary speed encoder. In practice, the commercial drives produced by the project sponsor are capable of encoder-less speed control, but the control algorithms implemented within these commercial drives are sufficient to provide a very accurate speed feedback to the speed controller. As a result, an encoder-less speed control method was considered to be unnecessary in this simulation. An RC low-pass filter of 12kHz was used to mitigate the effect of aliasing [115].

The motor load torque profile was varied to provide a 2Hz periodic load to the motor. The choice of a 2Hz periodic load was due to a few reasons, such as: a 2Hz signal would be far removed from any signals that arise in the electrical quantities due to normal machine or drive behaviour and so the effect of the 2Hz perturbation would not be “drowned” by existing harmonic content; a perturbation every 0.5s is sufficient for observing the motor response to loading and unloading; and in context of industrial

drives, typically induction motors do not act as servo motors and so do not require a high dynamic performance, hence the choice of a low rate of perturbation.

It was also considered that the use of a different loading torque profile – in terms of the "shape" of the applied loading - would not necessarily be useful to investigate at this stage as the harmonics induced in the motor as a result of periodic loading would increase the complexity of the estimation process in terms of choosing harmonics to monitor. Incidentally, the choice of finding harmonics to monitor is further discussed in Chapter 4.

A problem worth addressing regarding the simulated 2Hz loading is that in practice, a motor rapidly being fully loaded and fully unloaded would face significant shearing forces and the rapid rises and falls in DC-link voltage may cause issues for the motor drive. Practically, this method would be destructive for the motor and/or the motor drive, but it is used here in simulation for investigative purposes.

The values of the capacitors C1 and C2 in Fig3.2 were set to 270μF for a total capacitance of 135μF, and simulations were run in the cases where ESR1 was equivalent to ESR2, where both were set at values of 0.5*[1mΩ, 10mΩ, 100mΩ, 500mΩ, 1Ω]. The values assigned to C1, C2 were selected to match the capacitances of the electrolytic capacitors within the drive under test; and the range of values assigned to ESR1, ESR2 was selected to look for changes in waveform behaviour or estimation accuracy as ESR increased from the minimum of 1mΩ to 1Ω.

The motor load torque profile was varied between no load and rated load: five sets of recordings were made of voltage across and current through the DC-link capacitors. The periodic load torque reference signal is shown in Fig3.4. The reference load torque alternated between maximum torque and zero torque, allowing the motor transients to be observed before allowing the motor currents and speed to rapidly settle at steady-state before the load was again alternated.

Over the course of the simulation, the motor was brought to a speed of 40Hz, and an alternating reference load torque of 27Nm was applied at a frequency of 2Hz, starting from a time of 1s. This is shown in Fig3.5.

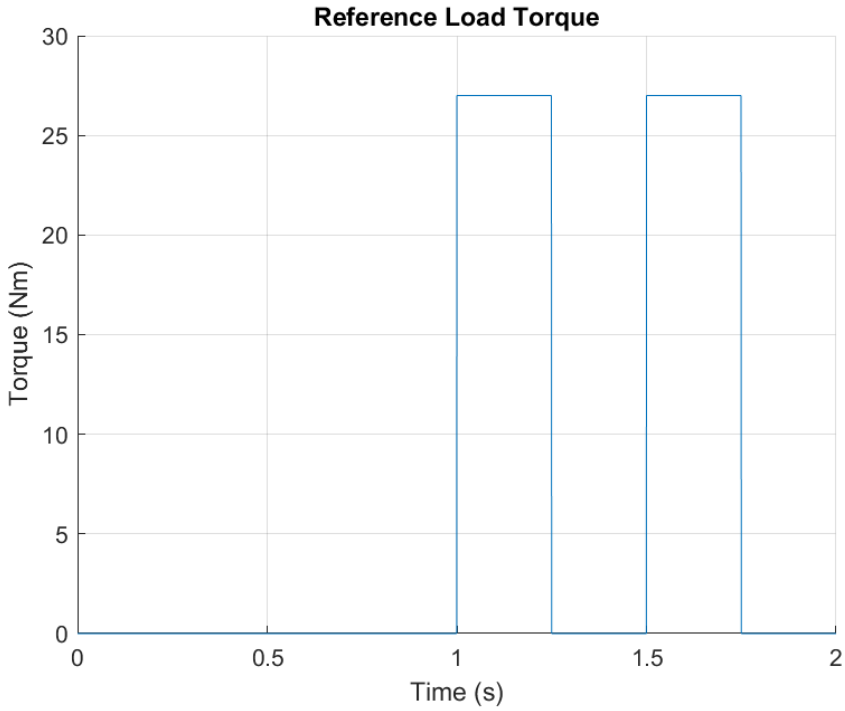


Fig3.4 – Simulated reference load torque

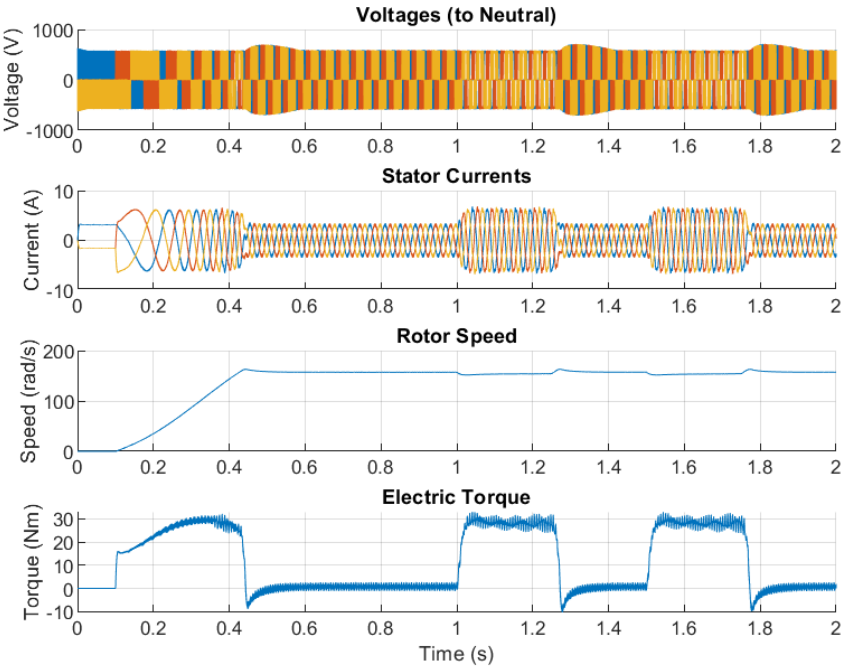


Fig3.5 – Simulated motor drive waveforms: a) voltages; b) currents; c) speed; d) torque

Fig3.4 shows the 2Hz periodic load torque reference signal, where the signal was switched on at 1s and the load torque applied to the motor followed the reference signal.

Fig3.5 shows four graphs: the first graph shows the PWM voltages applied across the stator rails; the second graph shows the stator currents; the third graph shows the measured motor speed in radians per second; and the last graph shows the electric torque created by the motor-under-test. Specifically looking at the simulated PWM voltages, the first 0.1s of the simulation shows transients in the voltage. These very high voltages were due to quirks of simulation behaviour, where differential equations are solved at the simulation start-up, and they are not representative of reality. The motor is provided a controlled three-phase current starting from 0.1s. However, the first 0.1s are left in the graph to allow comparison of motor current versus motor speed and electric torque for the length of the simulation.

Fig3.5c shows the motor speed, where the speed was controlled via a motor speed controller. As the mechanical load torque applied upon the motor alternated as shown in Fig3.4, the motor changed how much electric torque was provided in order to maintain the reference motor speed, as shown in Fig3.5d. As the amount of electric torque provided by the motor adjusted, so did the electric current drawn by the motor due to the relationship between electric torque and quadrature current. This is shown in Fig3.5b. Finally, voltage is shown in Fig3.5a, where the PWM voltage applied between the stator rails changed according to changes in motor speed.

3.2.3 – Time domain analysis

By measuring the voltage across the capacitors and the current through the capacitors, it was possible to extract the waveforms seen in Fig3.6, and further zoom in to the waveform in Fig3.7.

Fig3.6,7 show the voltage across and the current through the simulated DC-link capacitors, where Fig3.6 shows data measured over 20ms: the six pulses of 300Hz current contributed by the rectifier can clearly be seen. Fig3.7 shows one pulse of rectifier contribution. Both figures show the rectifier contribution, as well as the high-frequency switching component, where the switching component is very clearly seen in the noisy jagged edges of the capacitor current.

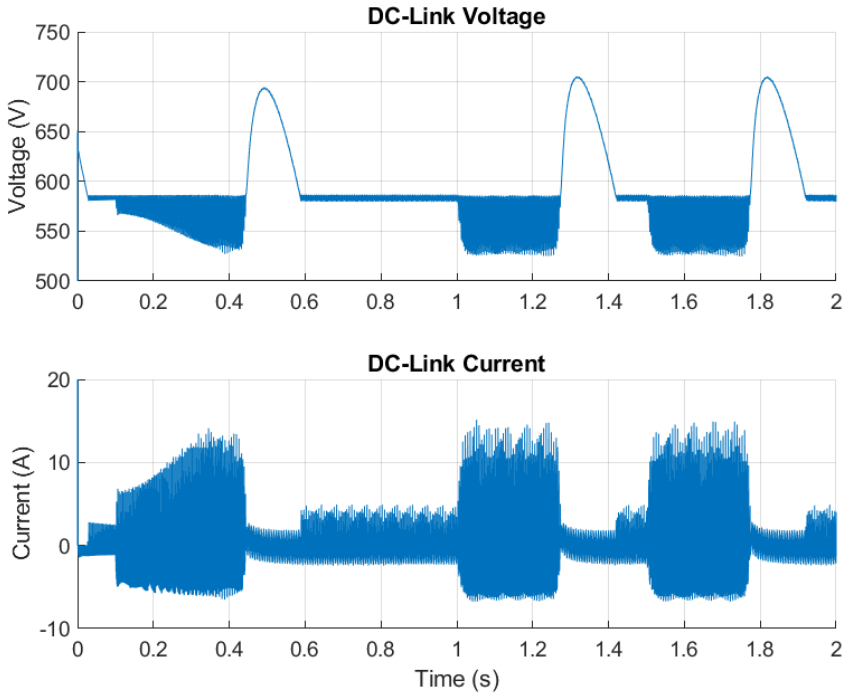


Fig3.6 – Simulated DC-link capacitor waveforms

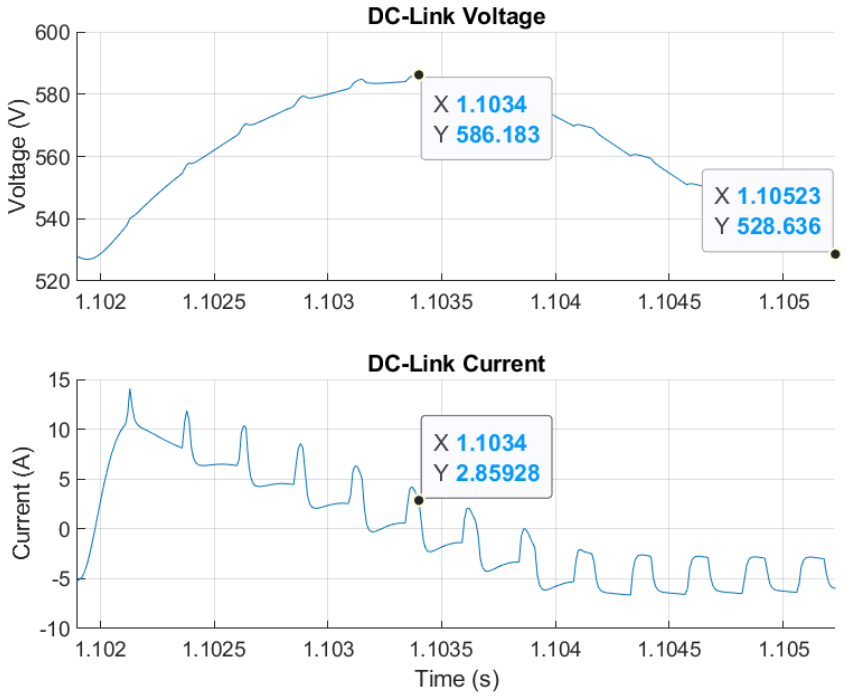


Fig3.7 – Simulated DC-link capacitor waveforms (zoomed)

Applying (3.2) to Fig3.7, it is possible to make use of measurements of voltage and current at two moments in time and then find an estimate of capacitance.

$$\hat{C} = \left|\frac{I}{\frac{dV}{dt}}\right| \equiv \left|\frac{2.85928}{\frac{586.183-528.636}{1.10523-1.1034}}\right| \approx 91uF \qquad (3.2)$$

The values of the voltages and current used to estimate the DC-link electrolytic capacitance were chosen according to the moments in time where the diode rectifier bridge was commutating and where it stopped commutating. These two moments in time relate to where the voltage across the DC-link was at a maximum and at a minimum in one commutation period. Using the values of voltage and time at these moments, a rate of change of voltage may be calculated, and the value of current at the maximum point may be used with the rate of change to produce the estimate of capacitance shown in (3.2).

As the actual value of the capacitance set in the simulation was 135uF, the error between the simulated and the estimated capacitances was roughly 33%. Although the waveforms were taken from an ideal simulation, an error was present between the measured and estimated values of the DC-link electrolytic capacitance due to the presence of the impedances in the rest of the DC-link as well as the impedances on the grid-side of the rectifier. The impedances prior to the rectifier may be combined to give a simplified lumped impedance in the DC-link, and as (3.2) did not consider the effect of these impedances, an error was to be expected between estimated and simulated values.

There are a few issues with this result: firstly, this estimated capacitance assumes the ESR is negligible. Additionally, this method is dependent on looking for voltage maxima and minima: this is a straightforward task in simulation, where waveforms may be inspected and exact datapoints selected, but is difficult to automate in practice due to the presence of both random and system noise causing difficulty in differentiating signals [4].

Additionally, this method makes use of only the 300Hz components of the electrical signals in the DC-link, which means that much information that may provide a more precise insight into the impedance of the DC-link is ignored. Furthermore, this method would be likely to break-down in the case of motor mechanical transients, where currents and voltages would change rapidly and unpredictably.

3.2.4 – Frequency domain analysis

In the frequency domain, there are many transforms that may be used for the purpose of analysing signals through spectral decomposition. For this work, three frequency

transforms were compared: the Fast Fourier Transform (FFT); the Short Term Fourier Transform (STFT); and the Continuous Wavelet Transform (CWT).

3.2.4.1 – Fast Fourier Transform (FFT)

The FFT was initially chosen for this work to inspect the frequency response of a motor-drive DC-Link across a chosen frequency range of [300, 1800] Hz. The frequencies in this range were chosen because they are integer multiples of the sixth-harmonic of the grid frequency where the frequency of the grid is 50Hz. The FFT is subject to a choice of window and window length, where a higher resolution spectrogram may be obtained through a longer sampling period [2]. The implication is that the FFT may produce a coarser resolution output where the sampling period is small. This situation may matter in cases where motor-drive output transients occur quickly, and the sampling period is long enough that it includes the transient and produces an erroneous output calculation.

The Discrete Fourier Transform, from which the FFT is derived and implemented, is described in (3.3) [116]:

$$X(k) = \frac{1}{\mathrm{N}} \sum_{n=0}^{N-1} x(n) \cdot e^{\frac{-j2\pi kn}{N}} \quad where\ k = 0,1,2 \dots N-1 \tag{3.3}$$

where $X(k)$ refers to a set of values in the frequency domain; and $x(n)$ refers to a set of values in the time domain.

3.2.4.2 – Short Term Fourier Transform (STFT)

In order to gain a better snapshot of very rapid transients, the Short Term Fourier Transform (STFT) was employed. The frequency resolution of the output of the STFT is dependent on window length as well as choice of the window function [117], where a well-chosen window length may provide a lot of information about the frequencies of interest in a given time-window. However, the implication then is that an optimal window length would need to be chosen, where the chosen window would have to deal with electrical signals that may vary massively depending on the motor load torque profile. The STFT may be beneficial for cases where monitoring of steady-state signals may not provide enough information about intermittent lower-amplitude, higher frequency signals, where such signals might indicate change in long-term behaviour, i.e. degradation.

The discrete STFT is described in (3.4) [116]:

$$X(t,\omega) = \int_{-\infty}^{\infty} x(t) \cdot w(t-\tau) \cdot e^{-j\omega t} \cdot dt \quad (3.4)$$

where $X(t,\omega)$ refers to a set of values in the frequency domain; $x(\mathrm{t})$ refers to a set of values in the time domain; and $w(t-\tau)$ refers to a windowing function.

3.2.4.3 – Continuous Wavelet Transform (CWT)

Both the FFT and STFT are frequency transforms, where each transform is provided with time-varying data; a snapshot of the data is taken and analysis is performed; and a frequency-vs-amplitude response is returned, where frequency is the independent variable and amplitude and phase are the dependent variables.

Related to frequency transforms are time-frequency transforms, where time is the independent variable, and frequency and amplitude the dependent variables – i.e. changes in amplitude and frequency may be observed with change in time, as opposed to the FFT, where the input data is taken as a snapshot in time and thereafter time is disregarded.

An example of a time-frequency transform is the Continuous Wavelet Transform (CWT) [116] [118] [119] [120], which is suited to motor-drive applications where variation is to be expected in electrical signals due to change in the mechanical load torque profile. This transform may also be applied to the motor-side electrical quantities, allowing for detection of motor issues [121].

Wavelet transforms rely upon choice of the mother wavelets, which are mathematical functions that are used to split the input signal into smaller signals of different frequencies and amplitudes [9]. The choice of mother wavelet is a restriction similar to the choice of window for the STFT, where a poorly chosen mother wavelet may lead to undesirable transform outputs. In practice, this means that a poor choice of mother wavelet may result in a spectral leakage, similar to when a poor choice of window function is chosen, where choosing a window function that does not coincide with integer number of periods of the signal in the time-domain leads to leakage in the frequency-domain.

There are any number of ways to express a mother wavelet mathematically, causing more issues in choosing an exact mother wavelet. However, there are a number of predefined mother wavelets in the literature from which to choose, due in part to the popularity of the wavelet transform for frequency analysis [122]. These mother

wavelets are available in pre-written library forms in different languages and for different platforms, such as Python or MATLAB [123] [124].

The general CWT is described in (3.5) [116]:

$$X(\omega_a, t) = \int_{-\infty}^{\infty} x(t+\tau) \cdot \varphi(a, p) \cdot d\tau \tag{3.5}$$

where $X(\omega_a, t)$ refers to a set of values in the time-frequency domain; $x(\mathrm{t})$ refers to a set of values in the time domain; and $\varphi(\tau, a, p)$ refers to the mother wavelet function which is dependent on a scaling and shifting.

(3.5) states that the output signal of the CWT is the sum over time of the input signal scaled and shifted by the mother wavelet. A shift in frequency means that the mother wavelet must have a centre frequency and room within which to shift, i.e. a bandwidth. Similarly, the presence of a scaling factor means that the mother wavelet must change in size at different frequencies, increasing or decreasing as the frequency changes compared to the centre frequency.

As an example, the frequency responses of specific frequencies were found using the complex Morlet wavelet through the implementation of (3.6) [125], where f_c is the cut-off frequency of choice for the mother wavelet – here, 2Hz; f_s is the sampling frequency – here, 1MHz; and a is the scaling factor used to find the frequency f_{bw} of interest. Here, the bandwidth of the mother wavelet was chosen to be 10Hz.

$$f_{bw} = \frac{f_c f_s}{a} \tag{3.6}$$

Fig3.8 shows an example of a complex Morlet mother wavelet where a 10Hz bandwidth was chosen with a 2Hz cut-off frequency. The choice of bandwidth is affected by how much knowledge is available about the signal that is being analysed, where a signal which is known to be at an exact frequency at all moments in time might not need a mother wavelet of a large bandwidth whereas a signal which may be of varying frequencies due to circuit behaviour might need a large bandwidth. Additionally, a mother wavelet of a wider bandwidth in the time domain allows for a sharper peak in the frequency domain.

The top two graphs in Fig3.8 show the real and imaginary parts of the mother wavelet, and the bottom graphs show the complex modulus of the wavelet and the associated phase angle. The bandwidth of 10Hz is observed by looking at the amplitude of the complex modulus falling off to zero below -5Hz and above +5Hz.

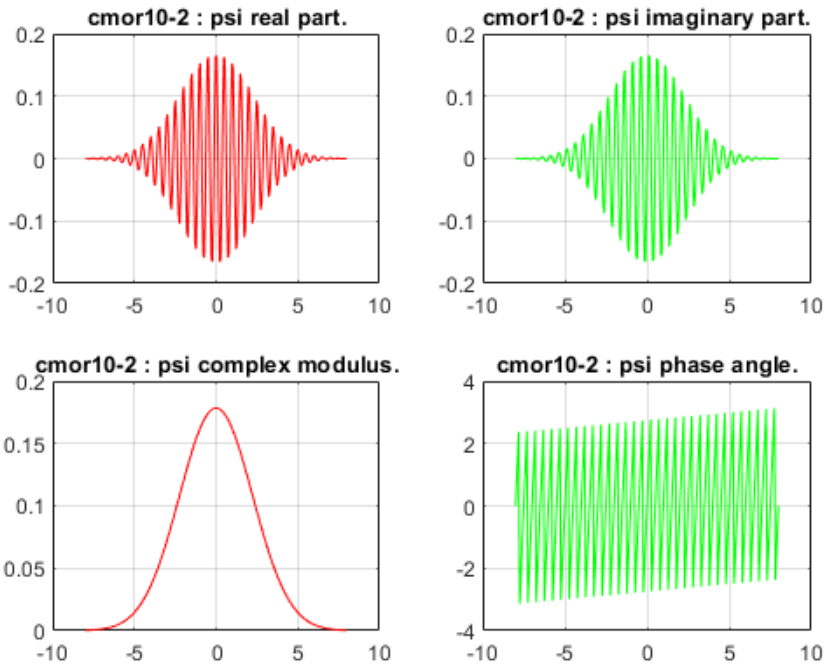


Fig3.8 – Mother wavelet using a complex Morlet with a 10Hz bandwidth

After some preliminary testing with different wavelets and simple test-cases using the MATLAB platform, two specific mother wavelets were chosen: the complex Morlet wavelet [116] and the bump wavelet [126], which had been chosen as a test wavelet against which to compare the complex Morlet wavelet.

The complex Morlet wavelet, defined in (3.7) [127], is shown in literature to be useful for impedance estimation [125] [128]:

$$\varphi(x) = \frac{1}{\sqrt{\pi f_{bw}}} \cdot e^{(j2\pi f_c x)} \cdot e^{\left(\frac{x^2}{f_{bw}}\right)} \tag{3.7}$$

where f_{bw} refers to bandwidth; and f_c refers to cut-off frequency.

The bump wavelet, defined in (3.8) [126], makes use of a mother wavelet from a pre-written toolbox which was used to compare estimated values of impedance against estimates produced via the complex Morlet wavelet:

$$\varphi(x) = e^{\left(1-\frac{1}{1-\frac{(ax-f_{bw})^2}{f_c^2}}\right)} \tag{3.8}$$

where f_{bw} refers to bandwidth; and f_c refers to cut-off frequency.

3.2.4.4 – Comparison of estimates

The MATLAB platform was used to import and process data to find the DC-link impedances for each of the five simulations, all of which used a time-varying mechanical load. Making use of known frequency transform relations, the input voltage and current data were used to find impedance as shown in (3.9), where F represents a mathematical function [129].

$$F\big(z(t)\big) = \frac{F(v(t))}{F(i(t))} \tag{3.9}$$

where $z(t)$ refers to time-varying impedance; where $v(t)$ refers to time-varying voltage; and where $i(t)$ refers to time-varying current.

Scripts were written to import and process one second of data from each PLECS simulation. To replicate the sample-and-hold behaviour of a real microprocessor with an ADC, a zero-order hold of 100kHz was used, as was a 12kHz anti-aliasing filter. For the choice of type of window, a Blackman window was used. There was no noticeable difference observed here between uses of a Blackman or Hamming window.

For each value of ESR, the different transforms were used to provide estimates of capacitance and resistance at the frequencies of [300Hz, 600Hz, 900Hz, 1200Hz, 1500Hz, 1800Hz]. The frequencies in this range were chosen because they are integer multiples of the sixth-harmonic of the grid frequency where the frequency of the grid is 50Hz.

Examples of the estimates generated are shown in Fig3.9 and Fig3.10, which show estimates found when the total ESR was set at 1Ω.

Fig3.9 shows the estimates of capacitance found using the four transforms described above, where the simulation made use of electrolytic capacitors which contributed a total ESR of 1Ω. Estimates of reactance are shown on the first graph; estimates of capacitance are shown on the second graph.

Fig3.10 shows the estimates of resistance found using the four transforms described above, where the simulation made use of electrolytic capacitors which contributed a total ESR of 1Ω.

For both figures, the solid line is the reference, where reactance of a capacitor was expected to decrease as frequency increased whilst resistance was expected to stay

constant as the simulated resistance was not time-varying. The marker shapes each represent estimates found via a different transform.

Looking at the estimates of reactance and capacitance in Fig3.9, the graphs show that the markers showing estimates found via the STFT, the FFT, and one of the wavelet transforms were consistently close to the expected values shown by the reference solid line. However, the estimates found via the complex Morlet wavelet transform were not as consistent as estimates via the other transforms.

Looking at the estimates of resistance in Fig3.10, the same trend may be observed: again, estimates found via the complex Morlet wavelet transform were not as consistent as estimates via the other transforms. However, these estimates were still seen to fall within a 10% error band, which was considered to be acceptable.

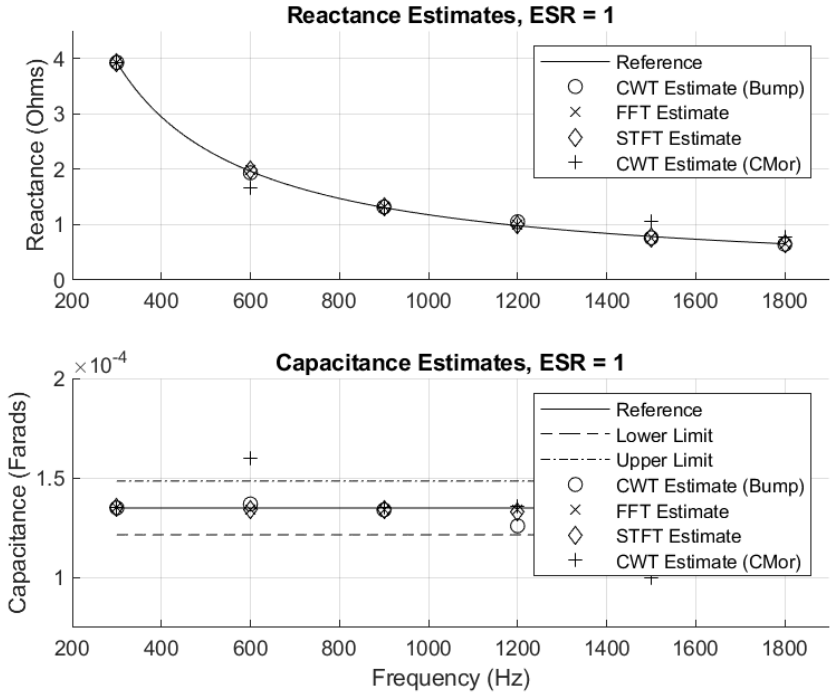


Fig3.9 – Estimates of impedance when ESR = 1Ω, comparing estimates using different transforms

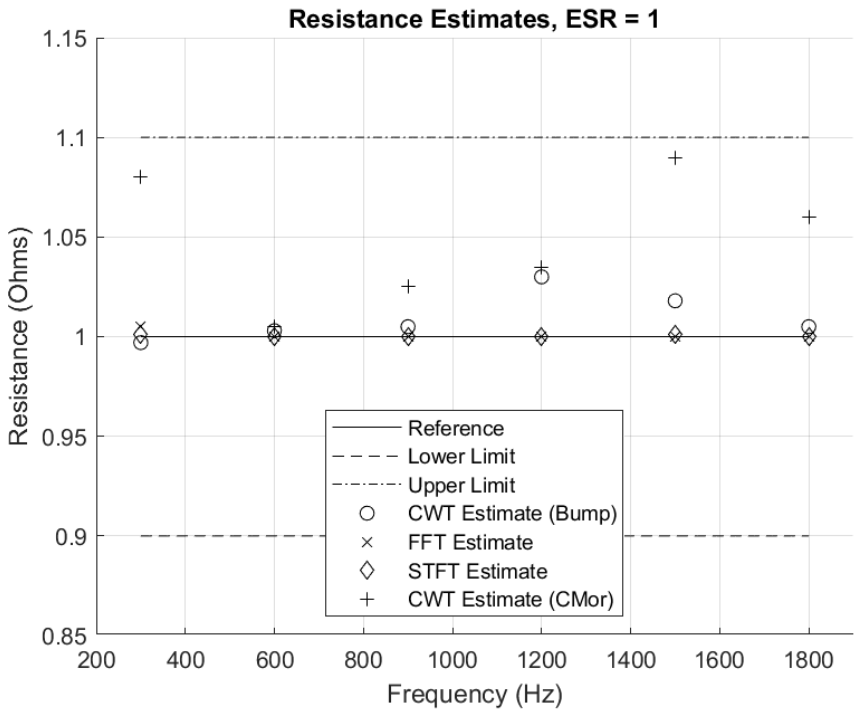


Fig3.10 – Estimates of resistance when ESR = 1Ω, comparing estimates using different transforms

After generating and tabulating the estimates for values of ESR between 1mΩ and 1Ω, regression analysis [130] was then used to find influential outliers through measuring abnormally large Cook's distances, where frequencies associated with large Cook's distances were neglected in the next step.

Cook's distances [131] were calculated to investigate the influence of amplitudes over the given frequency range on the fit, and overly influential amplitudes were removed according to a defined tolerance of deviation of an individual amplitude from the mean of amplitudes for each fit, thereby removing the influential amplitude and the associated frequency from the fit and from the plotted estimates.

Cook's distances may be calculated through adaptation of (3.10) [132]:

$$t_i = \frac{y_i - x_i\hat{\beta}}{s\sqrt{1-v_i}} \qquad D_i = {t_i}^2 \cdot \frac{V(\hat{y}_i)}{V(r_i)} \tag{3.10}$$

where t_i is referred to as a studentised residual, which is a normalised estimate of error found at one point in a regression fit, where the normalisation factor in the denominator helps provide further indication of error as a function of the standard deviation and variance of the estimated regression; and D_i is a product of the square of this normalised error and the ratio of the variance of the estimated dependent

values found via the regression to the variance of the error found at each of the original dependent values found via the regression.

Across a range of values of ESR, the results of the estimation schemes are shown in Fig3.11. Fig3.12 shows the absolute percentages of error associated with the estimates.

The previous two figures – Fig3.9 and Fig3.10 – used frequency as the independent variable, while the next two figures – Fig3.11 and Fig3.12 – use the value of the simulated resistance as the independent variable.

Fig3.11 shows estimates of impedance as resistance (ESR) varies between 1mΩ and 1Ω. As was observed with the previous two figures, the estimates of impedance between the transforms are not too different, but estimates found via the complex Morlet transform are noticeably greater in error compared to the reference value.

Fig3.12 shows the absolute values of error of the estimates shown in Fig3.11. Notably, estimates of capacitance found via the complex Morlet wavelet had less than 10% error as the simulated resistance varied, but the same transform produced estimates which were very high in error when the simulated resistance was small whilst the error reduced as resistance increased.

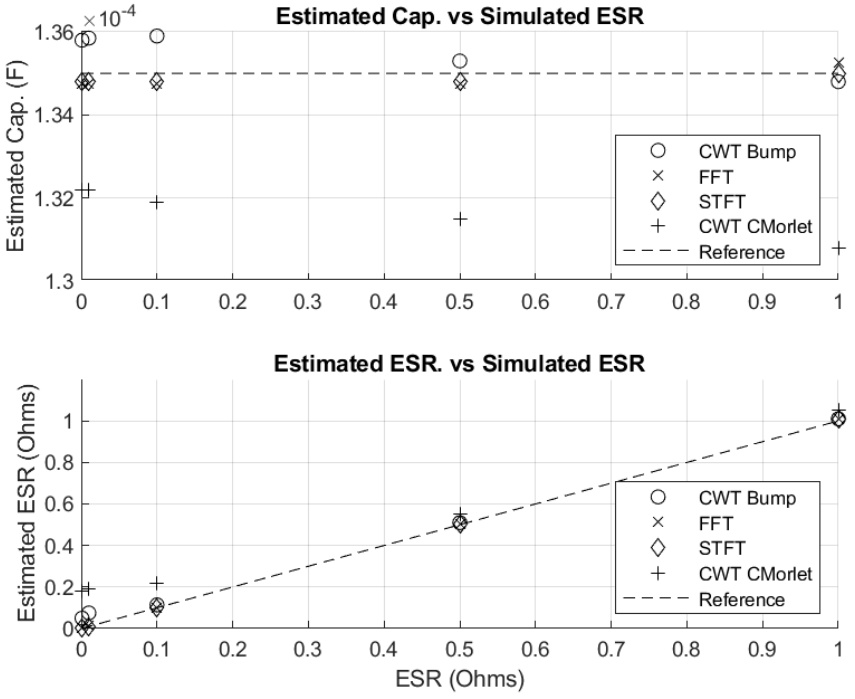


Fig3.11 – Comparison of impedance estimates as ESR varies

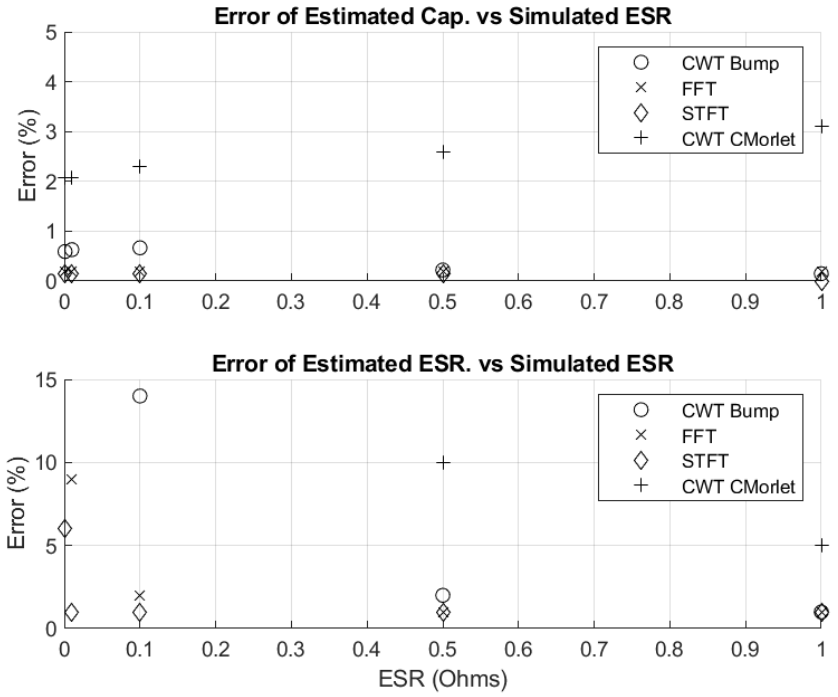


Fig3.12 – Comparison of error of impedance estimates as ESR varies

When estimating capacitance, the FFT and STFT produced estimates that were very close to the true value of capacitance, with a very low absolute error between the reference and estimated values. This was also true for the CWT bump wavelet, which had been chosen as a test wavelet against which to compare the complex Morlet wavelet. The complex Morlet wavelet was found to produce estimates of capacitance which increased in error as the value of the simulated resistance increased, as opposed to the other transforms where estimates of capacitance became more precise as the value of the simulated resistance.

When estimating resistance, the estimates of the four transforms quickly converged to the simulated value of resistance as the resistance increased, but the STFT gave the most precise results. The FFT and the bump wavelet had the most comparable results, and the complex Morlet wavelet converged slowly to the reference value of resistance.

As the estimates of the resistance found via the complex Morlet waveform became more accurate, the estimates of the capacitance found via the same transform became less accurate. It was assumed that a phase-shift issue was present during estimation, where a real element dominated the imaginary element of the impedance and the estimate was skewed towards the real impedance as resistance increased.

It was decided that the STFT should be discounted due to issues involved in deciding an optimal window length that may suit multiple real-world applications, where transients may be unpredictable. In practice, many discrete samples taken via the STFT plotted along time and frequency would effectively resemble the output of a time-frequency transform such as the wavelet transform. However - at this stage - the use of the STFT was rejected as the frequencies of interest in the motor drive system for impedance estimation purposes had not been investigated, and so it was considered that it would be better to make use of a time-frequency transform that was slightly more frequency agnostic than the STFT. As further work in this document does proceed to identify very specific frequencies of interest, it is clear in hindsight that the STFT is acceptable in practice assuming an optimal window length is chosen for the identified frequencies.

Choosing between the FFT and one of the wavelets, both are suitable for estimation of capacitance and ESR, but it is probable that having knowledge of estimated capacitance and ESR variation with finer resolution in time may be useful for diagnostic and maintenance purposes, and therefore the wavelet transform may be chosen as more optimal for monitoring the condition of a DC-link.

However, it must be stated that the clear downside in the use of wavelets is the higher computational cost in implementing the more exotic wavelet transform compared to the many cheaper, optimised, and readily available implementations of the FFT on embedded platforms. For research and investigative purposes, the wavelet transform may be implemented on commercial embedded platforms, but this may be more difficult for industrial applications where financial cost is a constraint and it would be preferable to make use of cheaper computational costs as this would translate into cheaper financial costs for the embedded platform.

As a result, a trade-off must be made between accuracy and computation expense. As has been stated previously, no frequencies of interest had been decided at this stage in the work; also, work at this stage had expected to make use of a mathematical processing using a laboratory computer where the issue of computational costs would be negligible, and so the use of the wavelet transform was preferred over the FFT.

Between the two wavelets used, it is actually more useful to make use of the complex Morlet wavelet despite the phase-shift error flaws mentioned, and this is due to the

fact that this wavelet is well defined in literature across a range of topics and code libraries, whereas the bump wavelet is best used as an exemplar wavelet.

As a result, if this test were to be reproduced on a platform outside simulation, it would be easier to make use of easily accessible pre-existing complex Morlet wavelet functions.

3.3 – Thermal analysis

As noted in [133], a thermal model can provide a secondary estimate of ESR to be used for comparison with estimates found via an electrical model. In this case, it is necessary to understand the effect of temperature on the capacitor.

3.3.1 – Structure of an electrolytic capacitor

An ideal capacitor would not be resistive, and so would not incur a power loss when conducting current. However, real electrolytic capacitors incur a power-loss which may be detected through changes in the temperatures around the structure of the capacitor.

The exact structure of an electrolytic capacitor varies between the type of electrolyte used, and variability may be introduced depending on electrolyte composition; incongruencies due to differences in material structure; or simply manufacturing tolerances [26].

The compositions and distributions of the electrolyte within capacitors are manufacturers' secrets, but the primary compound of electrolytes may be found via material data-sheets: for example, for a TDK B43547 aluminium electrolytic capacitor, the active substance within the capacitor electrolyte may be seen to be ethyl glycol [32] [134].

Alternatively, experimental methods may be used, such as spectroscopy or X-ray tomography [34]. For example, Gas Chromatography - Flame Ionisation Detection (GC-FID) [135] is recommended for identification or confirmation of the presence of ethyl glycol within an electrolyte [33] based upon the viscosity of the substance under test; this method was inconclusive when attempted for this project, due to the large sampling time required to detect peaks within the process response.

The mechanical part of the capacitor is more easily understood than the chemical: a typical electrolytic capacitor may be considered to essentially comprise a metal can within which sits a tightly wound strip of anodised aluminium foil, where the foil would be impregnated with electrolytic fluid acting as a dielectric [26]. The permittivity of the dielectric helps dictate the nominal capacitance of the capacitor [136].

When such an electrolytic capacitor is used in an electrical circuit, power-losses occur along the aluminium foil. Unfortunately, it is difficult to model a power-loss model of a realistic capacitor due to imperfections in the manufacturing process leading to anisotropic distributions in heat [137], even when provided an electrical steady-state. As a result, making use of the hottest part of the capacitor internals may be used as a benchmark for the temperature around the rest of the internal structure: this temperature is referred to as the core temperature.

In order to fully understand power-loss of a component, the component casing must be considered; as the component case has a capacity for heat just as does the internals of the component, the component case must also have an associated temperature. Knowledge of the temperature differential between the two given temperatures may then be used to provide a knowledge of the power-loss within the capacitor.

3.3.2 – Thermal network model

The following will assume that an industrial motor-drive will have make use of forced air-flow within its enclosure, typically via a low-voltage internal fan [138].

The capacitor can be considered as a thermal network, as shown in Fig3.13, where the capacitor case is represented as a first-order RC network [64]. The internal hotspot of the capacitor, which is considered to be the capacitor core, would lose power in the form of heat due to imperfections in the manufacturing process, as well as due to the presence of resistive elements internal to the device. This power loss would bleed from the capacitor core to the capacitor case, and thereafter to the ambient environment.

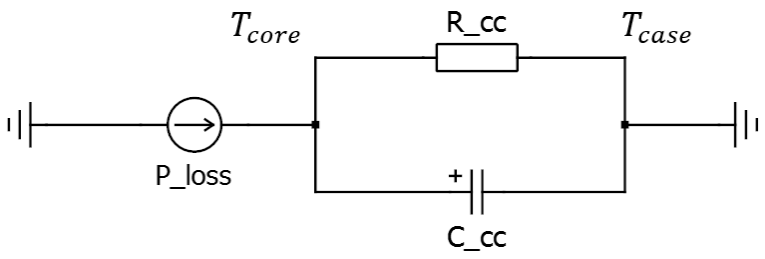


Fig3.13 – Simplified thermal representation of an electrolytic capacitor

(3.11) may be used to explain Fig3.13:

$$T_{core} - T_{case} = P_{loss} \cdot R_{cc} \cdot \left(1 - e^{\frac{-t}{R_{cc} \cdot C_{cc}}}\right) \quad (3.11)$$

where T refers to temperature; where P refers to power; where R refers to thermal resistance; where C refers to thermal capacitance; and where cc refers to the junction between the capacitor core and capacitor case.

A first-order model is presented here; a second-order model may be derived and have parameters fitted using empirical data, making use of temperatures of the core and the case. Whilst it is relatively straightforward to find the temperature of the case - requiring only a thermocouple to be firmly attached to the external sides of the capacitor casing - it is difficult to accurately measure the temperature of the capacitor core.

3.3.3 – Variations in ESR

Usually, resistance is a quantity that is a function of temperature but not a function of frequency unless the temperature were to increase due to a contribution from the skin effect. However, the impedance of an electrolytic capacitor is different, where the effective ESR reduces with frequency of the input signal, but increases with the temperature of the capacitor core [27] [28].

3.3.3.1 – Variations along frequency

Fig3.14 shows resistances measured for capacitors of two different brands: the TDK B43547 [36] for the upper graph, and the Nippon Chemi-Con ESMQ451VSN331MA30S [139] for the lower graph.

Electrochemical impedance spectroscopy (EIS) [140] was used to take impedance measurements making use of a dedicated EIS measurement device, a BioLogic SP-150 [141], shown in Appendix A, in FigA.1. To capture accurate EIS measurements, sine-wave currents in the order of milli-Amps were injected with varied frequencies into the capacitor by the finely calibrated measurement device, and the corresponding potential difference between the legs were measured. Impedances were then calculated based on measured currents and voltages. Multiple samples were taken for each frequency, with an average found for the frequency from the multiple samples. Frequencies are shown using a logarithmic scale.

The use of EIS measurements for the purpose of measuring capacitor impedance has limitations when considering the fact that the laboratory test measurement may only be conducted within the voltage range of the built-in potentiostat of the measurement device, which is typically in the low tens of volts. As a potential difference is placed across the two terminals of an electrolytic capacitor, a measurement may be taken – but that measurement is only valid for the range of volts at which it is taken, meaning that the measured impedance may change noticeably when placing a greater voltage across the terminals. This would mean that the measurement is only valid for the exact conditions under which it was taken.

This means that whilst an EIS measurement may provide a good idea of the impedance of the capacitor in low-voltage laboratory test conditions, the impedance should only be considered to be a benchmark when considering the impedance of the same capacitor in an actual motor-drive, where voltage across the DC-link would be held in the hundreds of volts [142] before taking temperature into account [143].

Interestingly, considering the usage of EIS, the model of a capacitor seen in Fig3.1 does not need to be the only capacitor model; with further analysis of the frequency response of an electrolytic capacitor, a multi-component model may be produced in order to give a more accurate fit of either the real or reactive components of the capacitor frequency response [44].

Fig3.14 shows two graphs showing the measured resistance in the frequency range between DC and 4kHz. The top graph shows six plots where measurements were taken using TDK capacitors, and the bottom graph shows six plots where measurements were taking using Nippon capacitors. One of each of the six plots is an average of the other five sets of measurements at each frequency. Both graphs from this figure show an inverse relationship between resistance and frequency for both sets of capacitors.

Using the same capacitors, Fig3.15 shows two graphs showing the measured capacitance in the frequency range between DC and 4kHz. The top graph shows six plots where measurements were taken using TDK capacitors, and the bottom graph shows six plots where measurements were taking using Nippon capacitors. One of each of the six plots is an average of the other five sets of measurements at each frequency.

The two sets of capacitors are of different brands but all capacitors are electrolytic capacitors of roughly the same rated capacitance and rated voltages and

temperatures. It is noticeable that the TDK capacitors had a much lower average resistance and much higher capacitance across the frequency range shown; this is due to differences in manufacturing, not experimental or measurement causes.

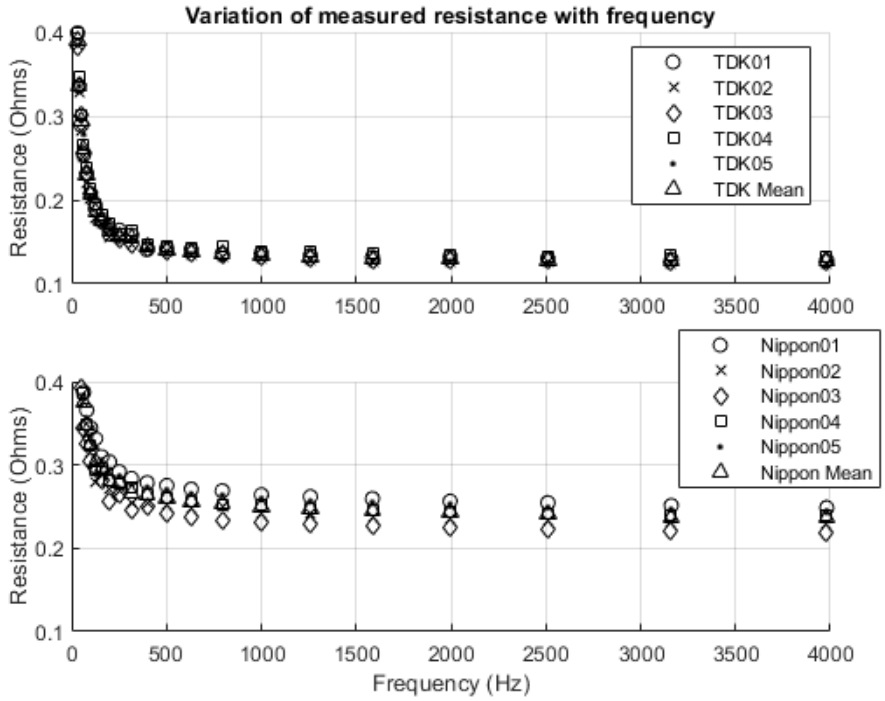


Fig3.14 – Comparison of variation of resistance with frequency between TDK, Nippon capacitors

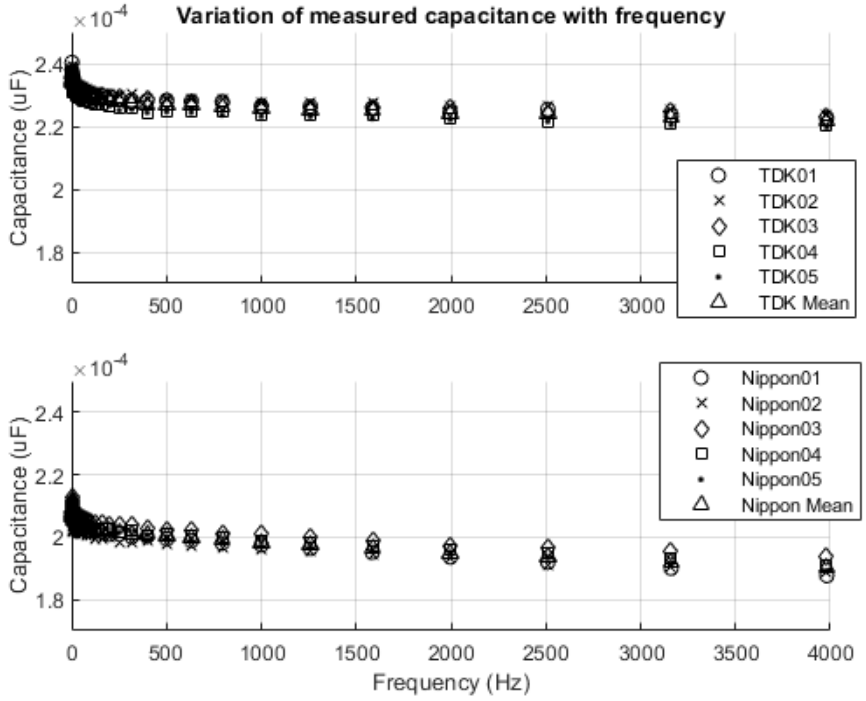


Fig3.15 – Comparison of variation of capacitance with frequency between TDK, Nippon capacitors

Using the mean values of each brand, it is possible to find that the mean TDK ohmic reactive contribution was roughly 0.35Ω at 2kHz, and 0.18Ω at 4kHz. Meanwhile, the mean TDK ohmic real contribution was roughly 0.127Ω at 2kHz, and 0.124Ω at 4kHz.

Similarly, the mean Nippon ohmic reactive contribution was roughly 0.41Ω at 2kHz, and 0.21Ω at 4kHz. Meanwhile, the mean Nippon ohmic real contribution was roughly 0.24Ω at 2kHz, and 0.235Ω at 4kHz.

Over the frequency range of DC to 4kHz, reactance dominates the complex impedance and the capacitance is relatively consistent. This is true for the frequency range of DC to 4kHz, whilst the resistance starts to dominate over extended frequency ranges such as DC to 100kHz, as shown in Fig3.16,17. These electrolytic capacitors are intended for usage with relatively low switching-frequencies, as can be observed by noting that frequency ranges where resistances dominate are not useful for energy storage purposes, and the frequency ranges where reactance dominates are in below approximately 10kHz.

The reasoning behind the discontinuities in the measured resistances and capacitances at frequencies above 10kHz – as shown in Fig3.16,17 – could be due to a number of reasons: resonance points being located above 10kHz, at the approximate frequencies

at which discontinuities in the impedance measurements occur; measurement current pulses at high frequencies becoming smaller and smaller to the point of being tending towards approximately zero and so any measurement data over a certain frequency range may not be trusted; or even the evaporation of liquid electrolyte (due to usage or storage of the capacitors) causing an effect on the measured frequency response of capacitor impedance, where change in volume of liquid electrolyte may manifest as change in measured signals.

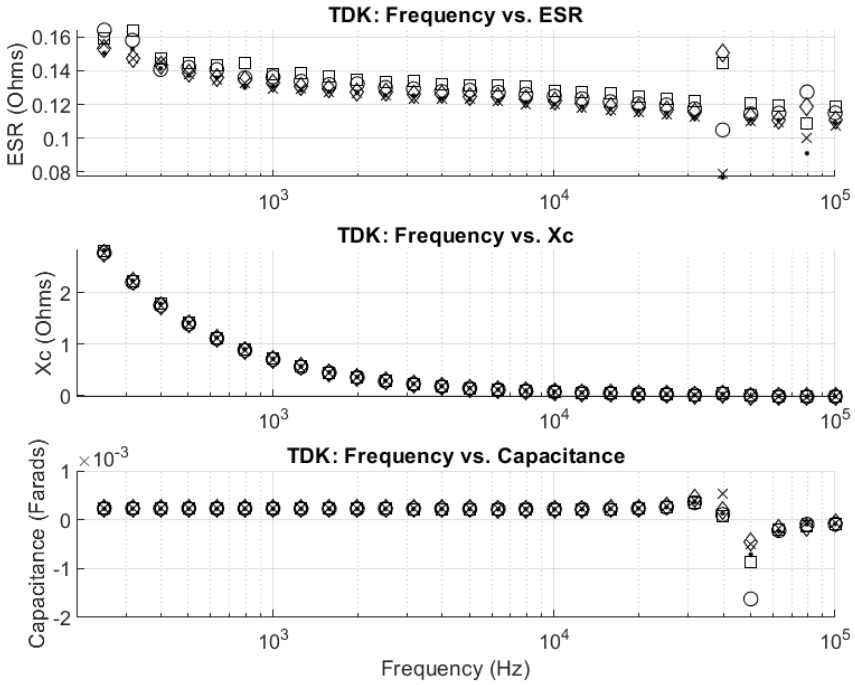


Fig3.16 – Frequency response of TDK capacitors over a larger frequency range

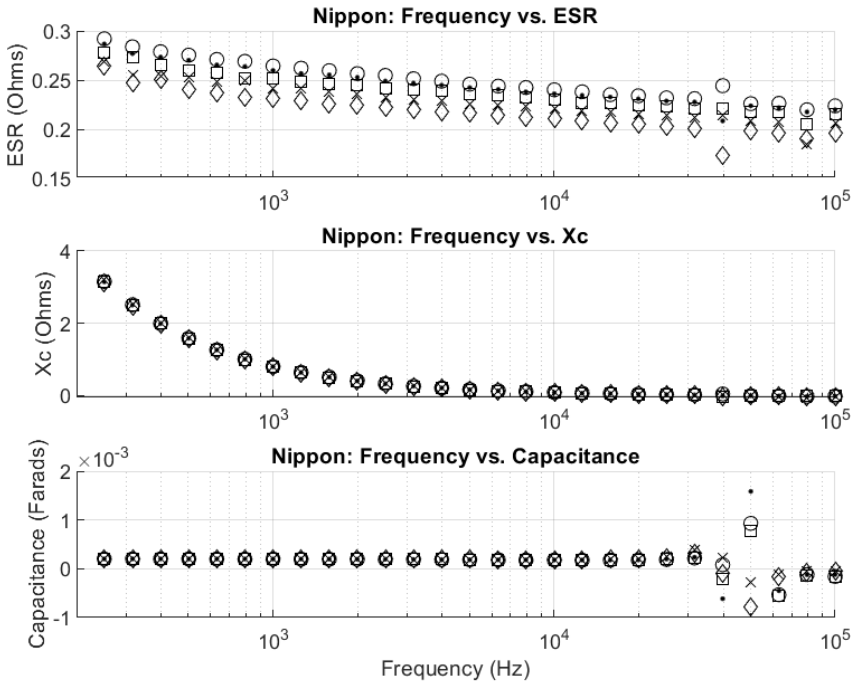


Fig3.17 – Frequency response of Nippon capacitors over a larger frequency range

3.3.3.2 – Variations with frequency and temperature

Unlike ideal components, real capacitors incur power-losses. However, power-loss is not the only non-ideal behaviour exhibited by real electrolytic capacitors.

Fig3.18 was generated using data measured using one of the previously mentioned TDK B43547 capacitors. This capacitor was one of a batch of capacitors which the manufacturer had impregnated with Type-K thermocouples, allowing for measurement of temperature at the core of the capacitor.

EIS measurements had previously been taken to find impedance over a range of frequencies. The EIS scans used in this next section used the same method of measurement as before, but through a different device: a N4L PSM1735 [144] shown in Appendix A, in FigA.2.

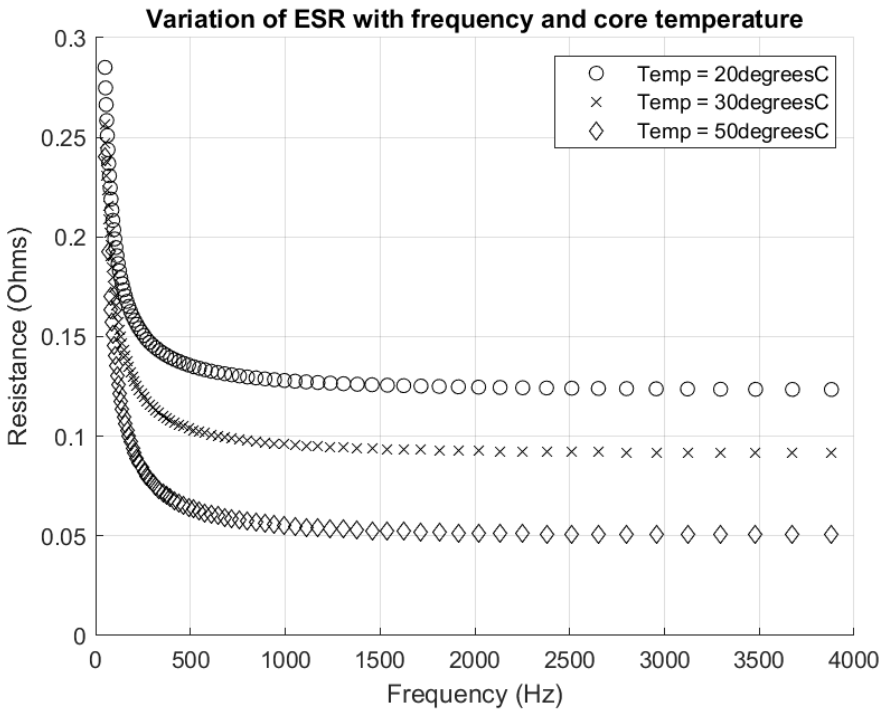


Fig3.18 – Variation of resistance of a TDK capacitor with varied frequency and temperature

Fig3.18 shows three traces showing the measured resistance of the capacitor measured when the core of the capacitor was held at first 20°C, and then 30°C, and then 50°C. The core was maintained at this temperature using a thermal chamber and a hysteretic current control was used to turn on and off heating of the chamber. EIS scans were rapidly undertaken while the measured temperature of the core was within 0.2°C absolute error of the target temperature.

As has been previously shown, the resistance of the electrolytic capacitor varies with frequency. Additionally, the resistance is shown here to vary according to core temperature, where an increase in core temperature of 30°C caused the measured resistance at 500Hz to decrease from roughly 140mΩ to 60mΩ.

Physically, the inversely proportional relationship between change in ESR and change in temperature is due to the effect of the capacitor core temperature on the properties of the electrolytic liquid solution: higher temperatures cause the solutes suspended within the solvent to more easily conduct electrical current, and so the effective resistance contributed by the electrolytic liquid solution reduces.

Interestingly, the same behaviour was not observed in the capacitance, as seen in Fig3.19.

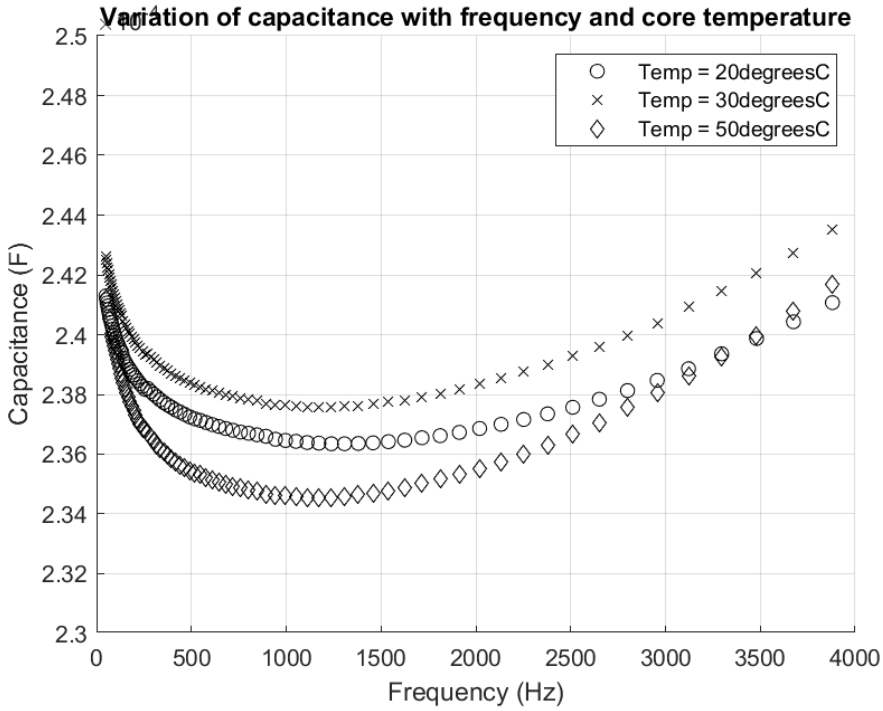


Fig3.19 – Variation of capacitance of a TDK capacitor with varied frequency and temperature

Fig3.19 shows two phenomena. The first was that as temperature increased, measured capacitance increased, seemed to reach a knee-point, and then decreased. This was confirmed after carrying out the test again with more than one thermocouple-impregnated capacitor.

The second phenomenon observed was that the measured capacitance sharply increased as frequency increased. It was not clear if this was a measurement error, so some testing was undertaken to address this issue, as seen in Fig3.20,21.

Fig3.20 shows the ten different EIS measurements taken using one capacitor, as well as the average of the ten measurements. Both resistance and capacitance can be seen to double between 1kHz and 10kHz, which is contradictory when considering Fig3.15 or Fig3.16,17, which all show that measurements of capacitance past 1kHz should be mostly flat: there should be an inverse mathematical relationship between reactance and frequency.

It was found that one of the causes for the increase in capacitance as frequency increased was the lack of an adequate contact between the EIS measurement clips and the electrical pins protruding out of the capacitor. Despite the clips being firmly connected to the pins, layers of dirt would build up and provide enough of a parasitic

impedance that frequency measurement would be affected. This was shown to be the most likely case after making use of different EIS measurement tools; varying between different capacitors with known and unknown measured impedances; and consulting with equipment manufacturers.

After cleaning the dirt from the pins, the measured resistance decreased uniformly by roughly 120mΩ across the frequency range, as shown by comparing Fig3.20,21. Additionally, the difference between the biggest and smallest values of measured capacitance across the frequency range was much smaller, as shown by comparing Fig3.20,21.

These two figures are included solely to demonstrate that accuracy of impedance measurements may be affected by otherwise mundane sources of error such as dirt, which may contribute parasitic impedances to the impedance of the device under test. Additionally, these figures called into question the accuracy and reliability of the EIS measurement tools, where troubleshooting was required to sanity-check and validate the measurements taken using the EIS measurement tools.

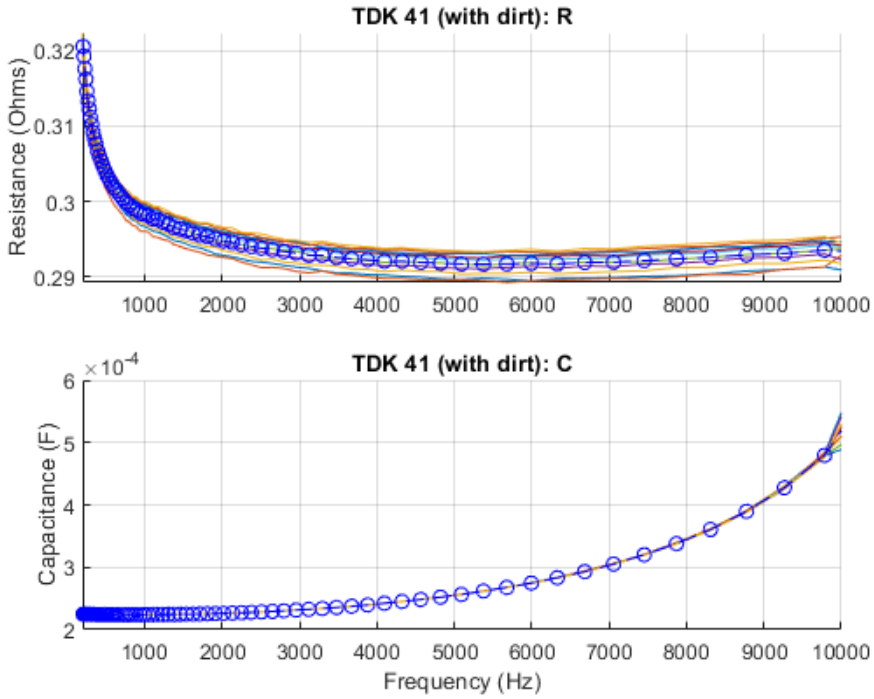


Fig3.20 – Measured impedances of one capacitor with dirty contacts/pins

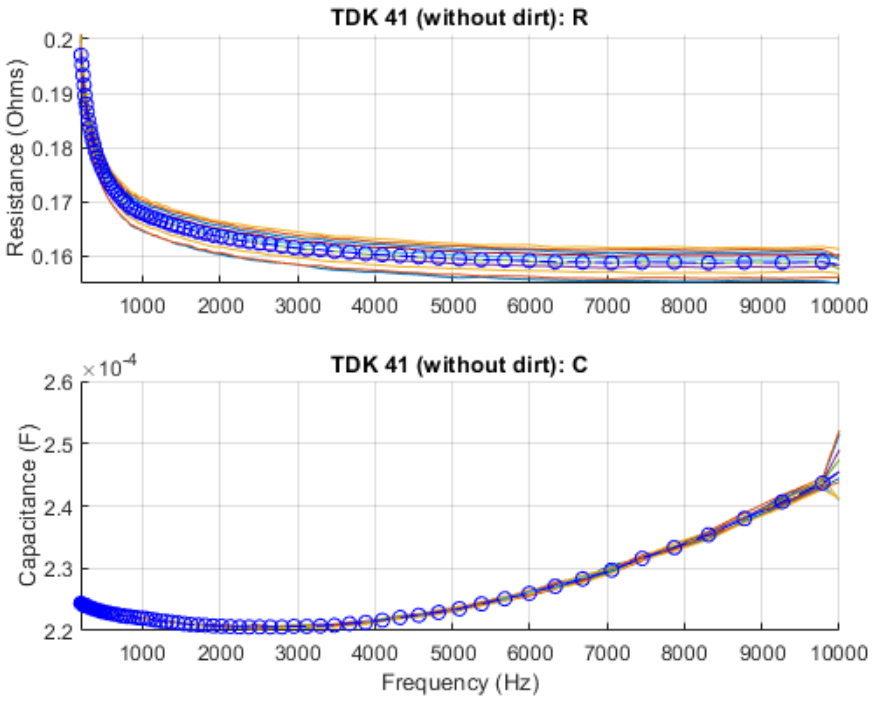


Fig3.21 – Measured impedances of one capacitor with cleaned contacts/pins

3.4 – Experimental implementation of the impedance estimation methods

Having discussed electrical and thermal models that may be used for impedance estimation purposes, the next step was to test the models using some of the aged capacitors to see if the impedance estimation schemes were useable.

3.4.1 – Estimation using the electrical method

The circuit diagram for the experimental system is shown in Fig3.22 and has two stages. On the left of the red line, a rectified three-phase mains voltage was used to provide a DC voltage source, where the rectifier stage and the capacitor maintaining the DC voltage were provided by a standard Siemens motor-drive [145]. On the right of the red line, a PCB-mounted test circuit had been assembled where a controlled AC voltage source provided current of a controlled frequency to two sets of capacitors, where the capacitors are labelled TDK01,02 and TDK07,08. The AC power-supply unit used was the GW Instek 7100E [146]. RL combinations are included in the circuit diagram to represent cable or wire impedances.

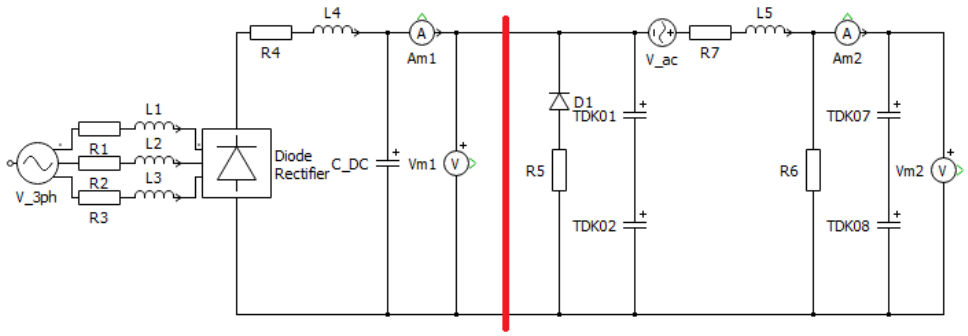


Fig3.22 – Test circuit to be used for estimation using the electrical method

The experimental rig is shown in Appendix A, in FigA.3. This figure shows a cabinet used to house a motor drive and a PCB mounted within a box. Four cables are pointed out, with the first cable used for measuring capacitor current; the second cable used for providing DC voltage to the PCB, where this voltage was also measured; the third cable used for provided AC voltage to the PCB; and the fourth cable used for providing AC voltage to the drive.

Before the four capacitors were mounted on a PCB, the impedances of these capacitors (on the right-hand side of the red line) were first measured via EIS, where the frequency progression of measurements was along a logarithmic scale. The BioLogic SP-150 was used for impedance measurement [141]. Using these measurements, curve-fitted impedances were found at 300Hz with these specific measurements being shown in Table3.2. The last column of the table includes the total value of the "lower leg" of the capacitor arrangement, and the individual impedances of TDK07 and TDK08 are also included. For the first test, brand new capacitors were used.

TDK01	**TDK02**	**TDK07**	**TDK08**	**TDK07, TDK08**	**Mode Est. of TDK07, TDK08**
149.4mΩ	144.5mΩ	156.6mΩ	154.3mΩ	310.9mΩ	407.6mΩ
228.7uF	229.7uF	228.4uF	227.3uF	113.925uF	113.17uF

Table3.2 – Curve fitted impedances at 300Hz from EIS measurement

Once the EIS measurements had been taken, the capacitors were mounted onto the PCB and arranged as shown in the circuit of Fig3.22, and a DC bias voltage and 30VAC 300Hz AC ripple voltage were applied as shown in Fig3.23. This figure shows

waveforms for five periods of the applied signal. On the left of the red line, the drive DC-link voltage was measured, as was the current from the rectifier output. On the right of the red line, the voltage across the lower leg of the PCB capacitors was measured, as was the current through these capacitors.

Fig3.23 shows waveforms for five periods of the applied signal, where the waveforms are the voltage across and current through the lower leg of the capacitor arrangement. An analogue RC low-pass filter was used at the input of the data-acquisition unit (DAQ), with a cut-off frequency of 12kHz. The DAQ was made up of a NI cDAQ-9174 [147] and NI-9222 [148]. The DAQ sample rate chosen was 500kHz. Sampling windows of 30s were used. Voltage and current were measured across TDK07,08 after applying rectified three-phase mains supply and a controlled 30V 300Hz AC voltage source to the capacitors.

As a 300Hz AC signal was present, the time-domain data was passed through a complex Morlet transform function to find estimates of impedance as described in section **3.2.4.3**, looking specifically at 300Hz. Fig3.24 shows the estimates, where magnitudes are plotted over a period of time. Measured values are plotted in orange, and estimated values are plotted in blue.

Using the electrical estimation scheme, there was an error of less than 10% between the values of the reference and the estimated capacitances, where a maximum error of 10% was chosen to place a hard limit on the maximum acceptable error of the output of the estimation process. However, an absolute error of 31% was detected between the reference and estimated resistances.

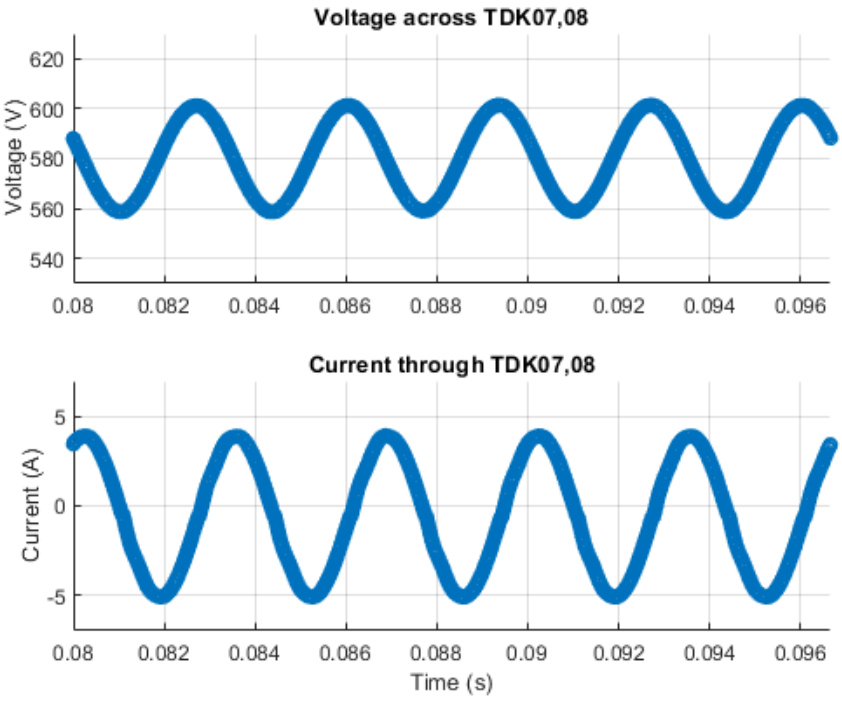


Fig3.23 – Voltage and current through the PCB lower leg: TDK07,08

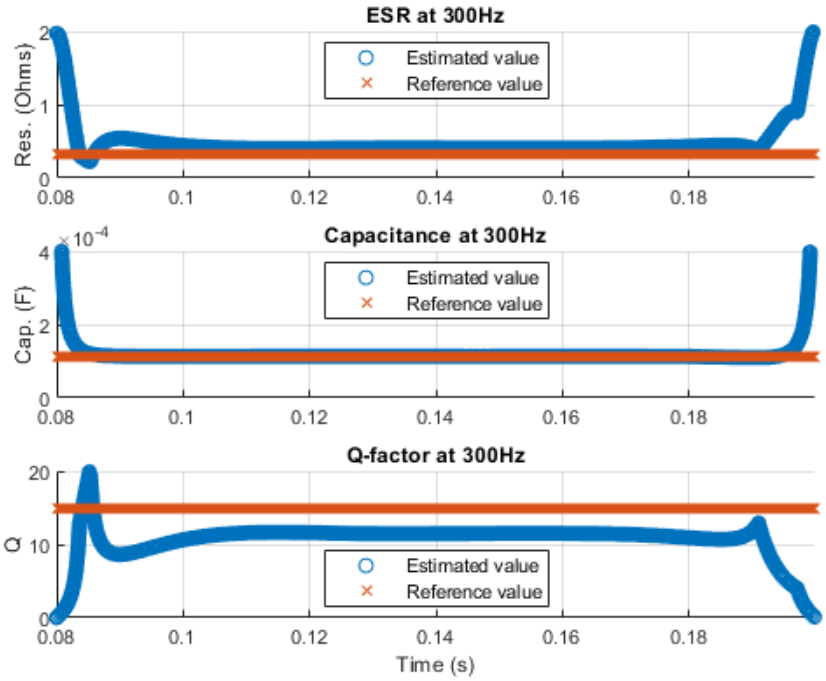


Fig3.24 – Impedance estimation using voltage and current through the PCB lower leg: TDK07,08

For the second test, a slightly artificially aged set of capacitors (TDK51-54) were used. The aging process of the capacitors is shown in Appendix B. The capacitors had been

subject to roughly a cumulative ten hours of heating. Table3.3 lists the relevant measurements of these “aged” capacitors taken using the BioLogic SP-150 [141].

TDK51	TDK52	TDK53	TDK54	TDK53, TDK54	Mode Est. of TDK53, TDK54
135.4mΩ	133.2mΩ	140.5mΩ	125.8mΩ	266.3mΩ	377.1mΩ
225.6uF	229.0uF	223.0uF	226.1uF	112.269uF	112.75uF

Table3.3 – Curve fitted impedances at 300Hz from EIS measurement

Fig3.25 shows the voltage and current across and through the lower leg of the capacitor arrangement. An analogue RC low-pass filter was used at the input of the data-acquisition unit (DAQ), with a cut-off frequency of 12kHz. The DAQ was made up of a NI cDAQ-9174 [147] and NI-9222 [148]. The DAQ sample rate chosen was 500kHz. Sampling windows of 30s were used. Voltage and current were measured across TDK53,54 after applying rectified three-phase mains supply and a controlled 30V 300Hz AC voltage source to the capacitors.

As a 300Hz AC signal was present, the time-domain data was passed through a complex Morlet transform function to find estimates of impedance as described in section **3.2.4.3**, looking specifically at 300Hz. Fig3.26 shows the estimates, where magnitudes are plotted over a period of time. Measured values are plotted in orange, and estimated values are plotted in blue.

Again, there was an error of less than 10% between the values of the EIS measured and the estimated capacitances. However, an absolute error of 42% was detected between the EIS measured and estimated resistances.

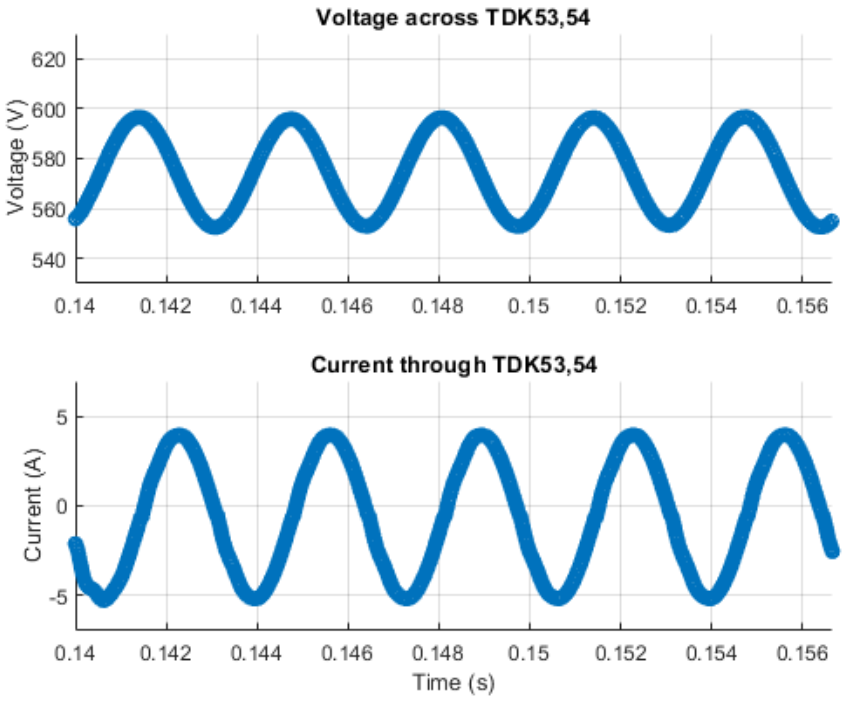


Fig3.25 – Voltage and current through the PCB lower leg: TDK53,54

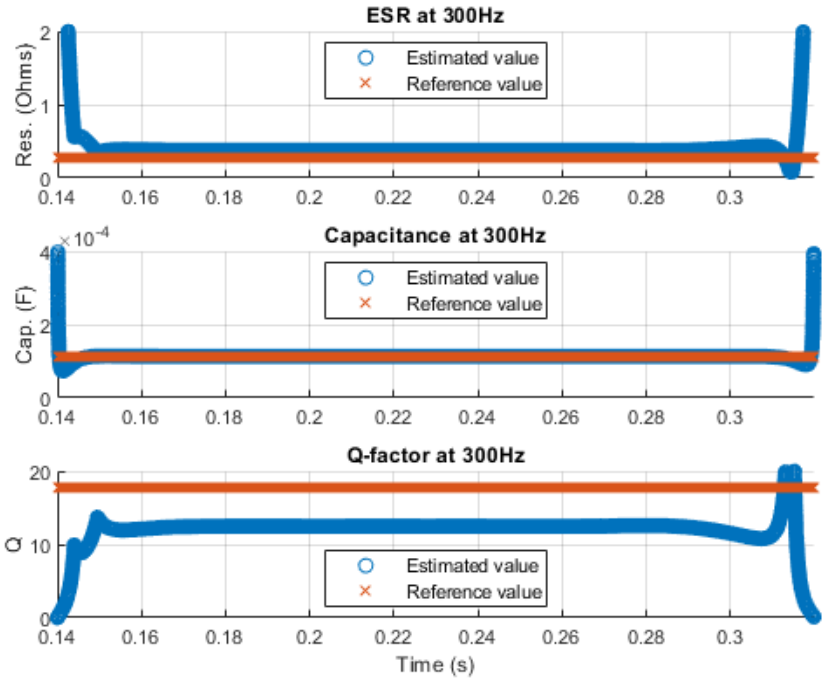


Fig3.26 – Impedance estimation using voltage and current through the PCB lower leg: TDK53,54

In both Fig3.24 and Fig3.26, there was a low error between the measured and estimated values of capacitance, whereas estimates of resistance were outside of a

10% error band. This may be due to the original EIS measurements not being taken at the temperature at which the capacitor later operated. Whilst connected as part of the circuit, the capacitor had a bias voltage and a ripple voltage placed across it in-situ, resulting in a thermal stress upon the capacitor, resulting in a difference between the measured EIS resistance and the estimated resistance due to differences in core temperature during measurement.

Alternatively, the explanation could be due to the lengths of cable which were crimped and connected to the physical PCB using brass screws and nuts. As an oversight, the impedance of the lengths of the cables connecting each capacitor terminal the physical PCB track were not measured, and neither were the brass screws and nuts. Retrospectively, the impedances of these extra lengths of cable and brass would have contributed to the increased resistance.

Fig3.27 shows a trace of the PCB, created using the KiCAD PCB design software [149]. The red box in Fig3.27 (which was not actually part of the PCB) is used to show the six holes used to mount each capacitor, where each capacitor had one pin for the positive terminal and two pins for the negative terminal. When the PCB had been designed, it was intended that test capacitors would be directly soldered onto the board. However, once it was understood that repeatedly heating the capacitor legs to hundreds of degrees Celsius may cause unintentional changes in capacitor impedance, capacitors were connected to the PCB using brass screws and nuts with fork terminals attached to the end of lengths of cables soldered onto capacitor legs.

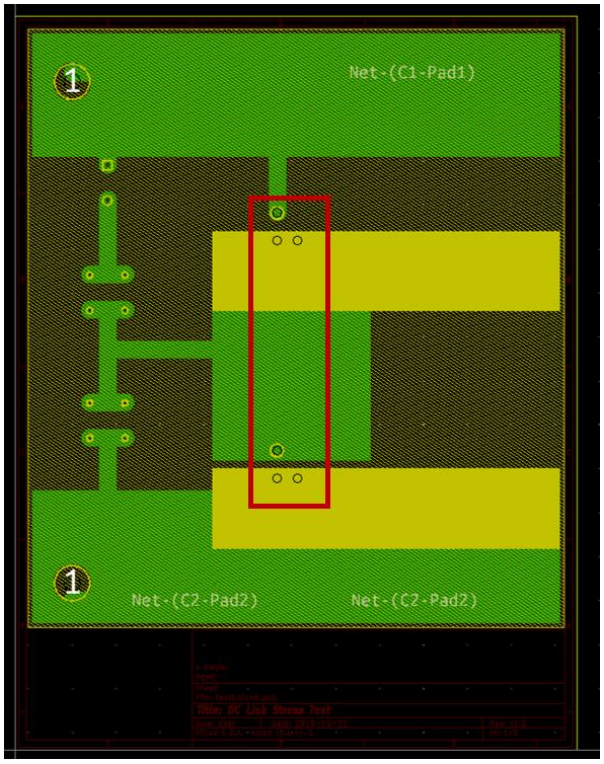


Fig3.27 – Example of the trace of the PCB under test

Overall, the reactance estimation method was shown to work in practice.

Incidentally, a simple calculation of the Q-factor values found via the EIS measured values would show that the capacitors from the first test (capacitors labelled TDK07,08) had a Q-factor value of 15.00 and the capacitors from the second test (capacitors labelled TDK53,54) had a Q-factor value of 17.74. These values are included as a visual indication of how tracking one variable may be easier than looking for changes in two variables.

3.4.2 – Estimation using the thermal method

When an electrolytic capacitor is held at a constant DC voltage and has a constant AC current passing through it, the core of the capacitor can be expected to be at a higher temperature than the external casing of the capacitor, neglecting the presence of cooling acting on the external casing. This is true over a range of temperatures, where the movement of heat is exothermic.

If the ambient temperature around a capacitor is held at a constant value via the use of a heating chamber, and a DC voltage is applied across the capacitor legs whilst an AC ripple current is passed through the capacitor, then the capacitor casing temperature may be measured and compared to the temperature of the capacitor

core. Using the difference in temperatures (ΔT), and assuming a simple first order thermal network comprising of a power-loss source (P_{loss}) and a thermal resistance ($R_{th,cc}$) – where the thermal capacitance shown in Fig3.13 is neglected in order to only consider temperatures at steady-state – it is possible to make use of the AC ripple current RMS value to find an estimate of electrical resistance ($\widehat{R_{th,elec}}$) through (3.12):

$$\Delta T = P_{loss} R_{th}$$

$$P = i^2 R \tag{3.12}$$

$$\widehat{R_{th,elec}} = \frac{\Delta T}{R_{th} i^2}$$

Thermal resistances may sometimes be found via manufacturer literature and can be assumed to be roughly constant for most of the operational range of temperatures. Here, the value of thermal resistance was stated to be 1.3K/W [150].

The difficulty comes in calculating ΔT, where the best method of finding the exact core temperature is through procuring thermocouple-impregnated capacitors from the manufacturer. For this test, the thermocouple measuring the core temperature was a Type K, while the thermocouple measuring the casing temperature was a Type T.

Thermocouples were connected to capacitors placed within a heating chamber, with a DC bias voltage of 20VDC and a 300Hz 100mA AC ripple current applied to the capacitor-under-test. The temperature of the chamber was maintained via hysteretic current control. Temperature was recorded at a sample rate of one measurement per second. The DC bias was chosen to be very low as EIS measurements were constantly taken to by injecting the low-level AC voltage which was used to find $\widehat{R_{th,elec}}$, and the EIS measurement device had strict limits on what voltage levels could safely be measured by its internal potentiostat.

The ambient temperature was controlled, and the voltage across and current through the capacitor were measured when the two temperatures had reached steady-state. The estimated $\widehat{R_{th,elec}}$ was then compared with the $\widehat{R_{elec}}$ found via usage of EIS.

For an ambient temperature of 25°C, the values listed in Table3.4 were measured:

Cap #	ΔT	i	$\widehat{R_{elec}}$	$\widehat{R_{th,elec}}$	Abs. Error (%)
1	0.37	1.04	0.170	0.263	54.71
2	0.66	1.04	0.147	0.469	219
3	0.29	1.04	0.162	0.206	27.16
4	0.33	1.04	0.158	0.235	48.73
5	0.23	1.04	0.151	0.164	8.61
6	0.23	1.04	0.152	0.164	7.89
7	0.27	1.04	0.156	0.192	23.08
8	0.5	1.04	0.158	0.356	125
9	0.34	1.04	0.150	0.242	61.30
10	0.32	1.04	0.156	0.228	46.15

Table3.4 – Estimates using an ambient temperature of 25°C

For an ambient temperature of 40°C, the values listed in Table3.5 were measured:

Cap #	ΔT	i	$\widehat{R_{elec}}$	$\widehat{R_{th,elec}}$	Abs. Error (%)
1	1.06	2.1	0.157	0.185	17.83
2	0.97	2.1	0.149	0.169	13.42
3	3.18	2.1	0.155	0.555	258
4	0.7	2.09	0.152	0.123	19.08
5	0.3	1.05	0.147	0.209	42.18
6	0.25	1.05	0.162	0.174	7.41
7	-	-	-	-	-
8	0.49	1.05	0.159	0.342	115
9	0.23	1.05	0.159	0.160	0.63
10	0.16	1.05	0.158	0.112	29.11

Table3.5 – Estimates using an ambient temperature of 40°C

In the 25°C test, it was noticed that when ΔT was close in value to 0.23K, the values found via the electrical model was similar to values found via the thermal model, with larger calculated values of ΔT leading to high errors between the two estimates of resistance. The discrepancy between the thermocouples was found to be the issue: the Type T thermocouple, being very sensitive to small changes in temperature within the heating chamber, produced constantly varying readings of the casing temperature,

even after filtering measurements taken at steady-state; whereas the Type K thermocouple, being impregnated within the core, produced readings that were already low-pass filtered. This meant that it was difficult to take reliable estimates of ΔT, even after post-processing.

In the 40°C test, capacitor #7 failed prematurely, and so it was neglected from the table. This test had a roughly 1A current applied to five capacitors, and a roughly 2A current applied to the other four. In this case, the previously observed phenomena were again observed: where RMS current was at roughly 1A, there was a low error between the two estimates when ΔT was close in value to 0.23K, compared to when current was increased to roughly 2A and when ΔT was close in value to 0.8K.

Fig3.28 shows two snapshots of one sample of thermocouple-measured capacitor casing temperature over the course of 2000 seconds, or 30 minutes. This portion of data was measured during the second test, where the target temperature of the 40°C was maintained through hysteretic current control.

The first graph of Fig3.28 indicates that this form of control caused issues in precise maintaining the temperature of the heating chamber on a macro scale: between the instants in time where the hysteretic controller turned on or off the heating element, both the temperature of the chamber and of the capacitor casing varied by at least 1°C.

The second graph of Fig3.28 indicates that problems are also present in temperature measurement on a micro scale: at the flattest part of the curve in the measured temperatures (600s), a great deal of variation is present even when the average temperature of the capacitor casing is 39°C. A line of best fit is provided so the trajectory of the temperature can be compared with the variation in the measured temperature data.

The third graph of Fig3.28 makes this problem much clearer: when looking at only 60s of data and plotting the same line of best fit as from the second graph, it is clear visually that there is a great deal of variation in temperature over measurement increments of one second. This variation in the measurements is effectively noise contributed from compounding errors which arose from the use of the Type-T thermocouple and the temperature data-logger, as well as potentially the natural variation of ambient temperature and air pressure conditions directly outside the heating chamber.

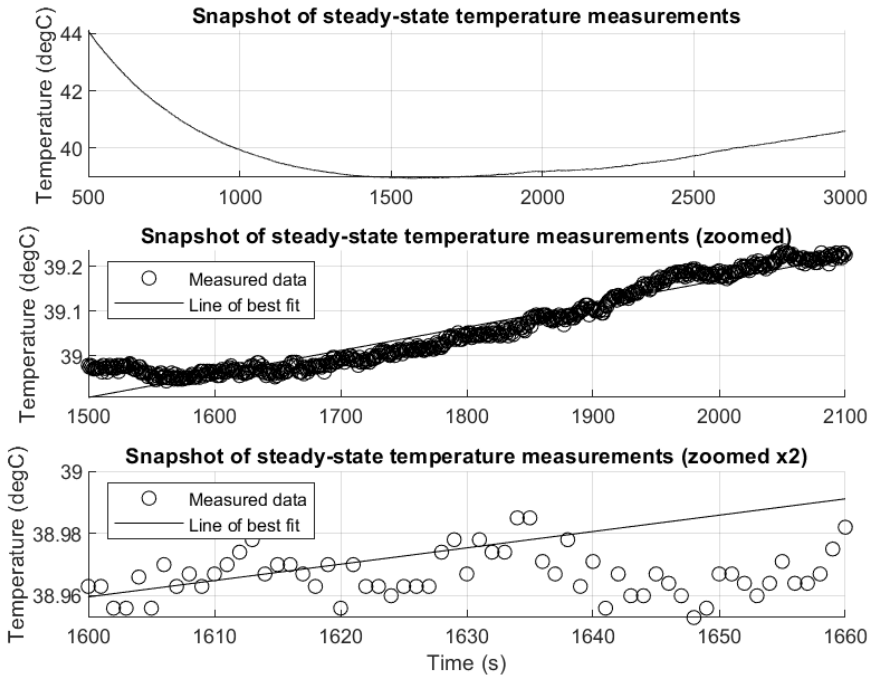


Fig3.28 – Variation in measured capacitor casing temperature

In terms of impedance estimation, this method relies upon three factors: knowledge of core temperature, or at least an expected ΔT at a given bias voltage and ripple current; casing temperature readings with a slow time-constant; and an acceptable estimate of resistance via frequency analysis.

If the estimate via frequency analysis is assumed to be acceptable, the issues of core and casing temperatures must be addressed via laboratory testing of thermocouple-connected capacitors under a range of bias voltages, ripple currents and casing temperatures, and finding average ΔT values in each condition; this would allow for the casing temperature to be measured in practice, and the appropriate ΔT value chosen for estimation purposes.

Clearly, noisy thermal measurements would be a source of error that would cause poor estimates and therefore the fitted thermal model would be inaccurate. As a result of the difficulty in finding estimates of the relevant thermal variables, the capacitor thermal model would therefore have to be considered to be too unreliable for further use in estimating any electrical quantities.

This is not a practical method for finding estimates of impedance in practice, and with the absence of existing temperature measurements of capacitor casing, it may not be appropriate for an industrial drive given the difficulty of trialling the method using

individual capacitors in ideal laboratory environments. This approach was therefore abandoned.

3.5 – Aging of capacitors

A major challenge with this project was to obtain capacitors which had been "naturally aged" through use in a standard industrial drive. Therefore, in order to provide samples of capacitors which exhibited different levels of degradation, a series of tests were performed on a set of brand-new capacitors in order to degrade them, and provide a set of devices to experimentally evaluate any impedance estimation techniques devised. Thermally stressing batches of capacitors was employed to mimic degradation of electrolytic capacitors by way of heat.

3.5.1 – Lifetime curves

Exposure to heat alone does not result in the same type of stress placed upon an electrolytic capacitor operating in a motor-drive as the capacitors also see cycles in their current levels. In addition, stressing capacitors is caused by many thousands of hours operation.

An example of expected lifetime of a typical capacitor used within motor-drives is shown in Fig3.29, where the lifetime curves are plotted of a capacitor subject to a 300Hz fundamental signal, extrapolated based upon manufacturer datasheets [36] [151] [150].

Fig3.29 plots temperature against thousands of hours, showing lifetime of a capacitor would be lower if it were to operate continually at a higher temperature. The circular markers plotted on the graph are taken from the TDK lifetime calculations, whilst the straight lines are the extrapolated curves based on a tool produced and suggested by the manufacturer to understand lifetime of the capacitors under different operating conditions [150].

The second plot in Fig3.29 has no circular markers. This is because the capacitor is not expected to operate this close to its rated temperature of 105°C. However, these high temperatures allowed the capacitors to be cycled to failure within a timescale reasonable for this project.

Lifetime can be seen to vary according to magnitude of signal current, as well as according to temperature of the capacitor. Fig3.29 shows that keeping the capacitor-

under-test at a high temperature whilst pushing currents of large magnitude through should lead to low expected lifetimes. In practice, this is difficult to attain, due to the fact that – for example – holding a capacitor at 100°C and passing a 300Hz 6A current through the capacitor would require a month and a half of continuous cycling in order to reach expected end-of-life.

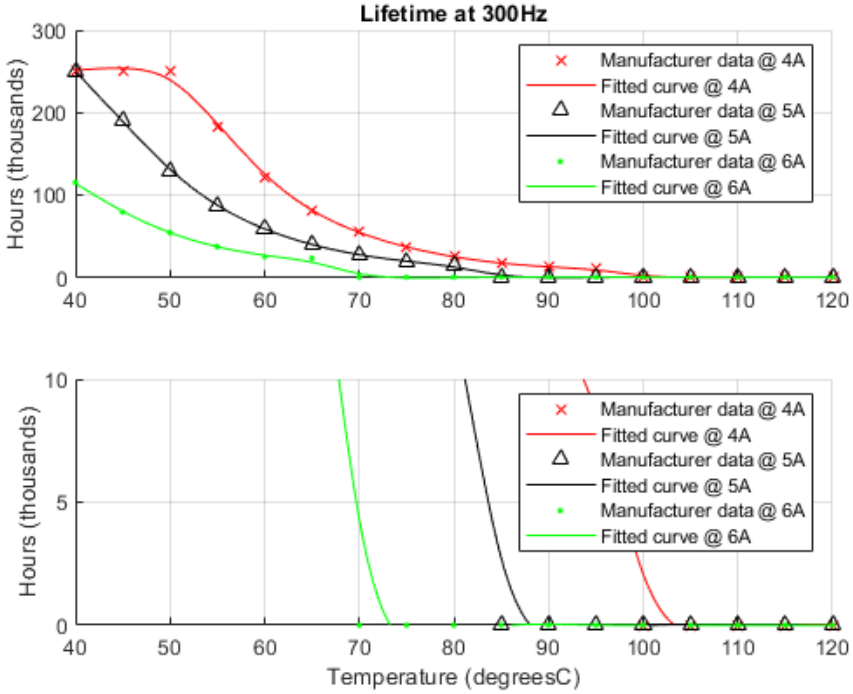


Fig3.29 – Extrapolated lifetime curves where TDK capacitor is subject to a fundamental 300Hz signal

To speed up the ageing process, it was decided that very high levels of stress would be placed upon electrolytic capacitors through at least two methods: placing a bias voltage across the terminals so the bias voltage would either significantly exceed the rated voltage or would be less than zero volts, which would typically result in a violent breakdown of the capacitor; or placing the capacitor in situations such that the capacitor leakage current would increase [26].

If the leakage current is increased, the capacitor breaks down slowly, depending on the method used. For example, electrolytic capacitors left in storage may suffer variations in ambient temperature, resulting in variations in conductivity of the electrolyte, which would then slowly cause changes in the leakage current of the capacitor [26]. For this reason, it is suggested by manufacturers that electrolytic capacitors are stored within an approved range of temperatures and humidity [152],

in order to minimise change in state of the electrolyte, so the capacitor itself does not suffer from a breakdown.

For this project, a third method was considered for accelerating ageing: exposing a capacitor to temperatures exceeding its rated temperature for periods of time, after which the capacitor would be cooled and impedances would be measured via EIS. This thermal cycling would be used to find a replicable method of degrading capacitors, for use with testing future impedance estimation schemes. This method would explicitly affect the electrolyte in the capacitor cans, causing a loss of electrolyte by way of evaporation via sustained heat.

A fourth method was also used, where changes in impedance were forced through causing damage to the dielectric medium present on the layers of aluminium foil. This method made use of application of reverse bias voltages to the capacitor terminals.

3.5.2 – Using a high ambient temperature

Two tests were undertaken using a high temperature to change the impedance of the capacitors. The first involved heating the ambient temperature of a batch of capacitors to 175°C for a relatively short amount of time as part of a fact-finding task, and the second involved heating a batch of capacitors to 150°C for a relatively longer time with corrections applied based upon the findings of the first task.

3.5.2.1 – Using a high ambient temperature for a short time

The first thermal cycling trial was effectively used to find sources of error and uncertainty within the method itself.

The first set of EIS measurements were taken using ten capacitors and looking across a range of frequencies, where a mean of the measured impedances was found. These ten capacitors were placed within a metal tin placed within a thermal chamber, where the chamber temperature was set at 175°C. After one hour of heating, the tin was removed from the chamber and the capacitors were left to cool to room temperature, after which the EIS measurements were taken again. This cycle was repeated over a number of hours.

Fig3.30 shows the mean impedances of the ten capacitors over a number of hours, plotting impedances at five frequencies.

The first four frequencies are multiples of an expected fundamental signal of 300Hz, and the fifth frequency is a frequency in the expected switching frequency range. At

times, the tin was left in the oven for a period of time longer than one hour, although the procedure of cooling and measuring impedances via EIS was kept the same.

Mean resistances are shown in the first plot, where the mean resistances increase from roughly 160mΩ to 500mΩ after a cumulative total of 30 hours of heating. Mean capacitances are shown in the second plot, where there is little change observed in the mean capacitances over the duration of the test. Mean phase angles are calculated, where the value of phase angle can be used to sanity-check the changes in the resistance and capacitance.

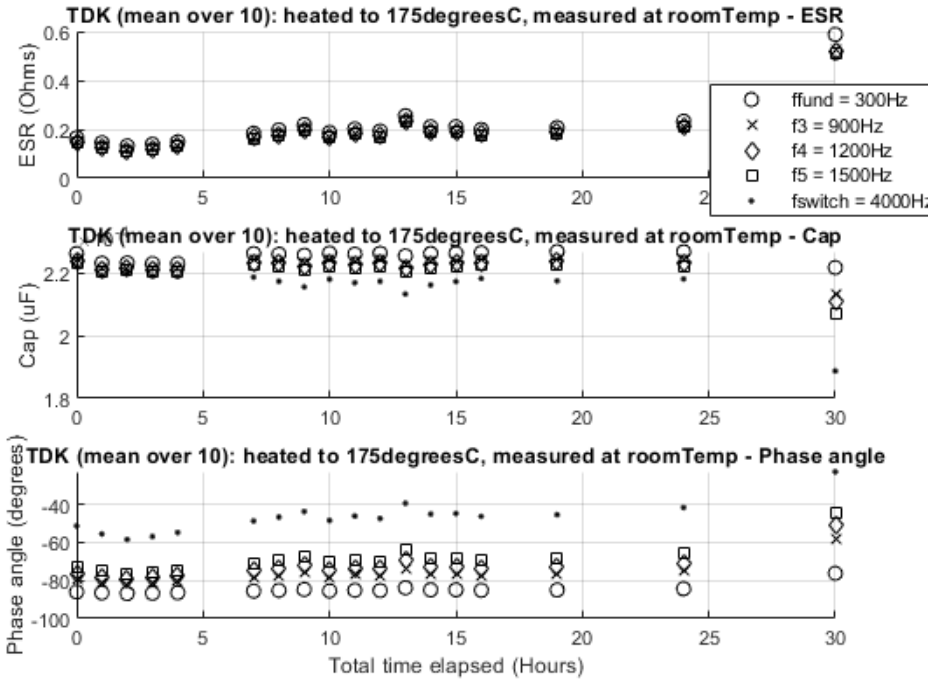


Fig3.30 – First thermal cycling trial

A few problems were noticed with this method, for example: build-up of dirt caused erroneous EIS measurements due to improper contact between pin and measurement clip, resulting in measurement error.

The difference between “clean” capacitor contacts may be seen in Fig3.31, where the capacitor on the bottom left of the image is in pristine condition, allowing for easy contact between pin and clip. The other capacitors in the image are shown to be in various states of damage, resulting from leaking electrolyte; burnt solder; burnt debris; or just charred contact pins due to exposure to high temperature.



Fig3.31 – Dirt on surface of the capacitor contacts

A second problem was that it was noticed that whilst measurements were being taken, the capacitors were not all held at a uniform internal temperature. This discrepancy of internal temperatures caused a variation in impedances between the ten capacitors, which in turn caused variation in the mean impedances taken from the ten capacitors. This is shown in the fluctuation in plotted impedances.

A third problem was noticed, which is very clear when looking at Fig3.30: leaving the capacitors sitting in the thermal chamber for a short amount of time did not cause much change in measured impedances, whereas allowing the capacitors to sit for a long amount of time did cause a noticeable change in measured impedance, specifically the resistive component.

3.5.2.2 – Using a high ambient temperature for a long time

Looking at the sources of error from the first test, a FLIR i7 thermal camera [153] was used to monitor capacitor internal temperatures – as seen in Fig3.32 – so EIS measurements could be taken when the capacitors were at roughly equal temperatures. Internal temperature of the core is not directly measured, but as the metal pins protruding from the base of the capacitor are connected to the capacitor core and are also good conductors of both electricity and heat, the temperature of the pins can be a good indicator of the temperature of the capacitor core.

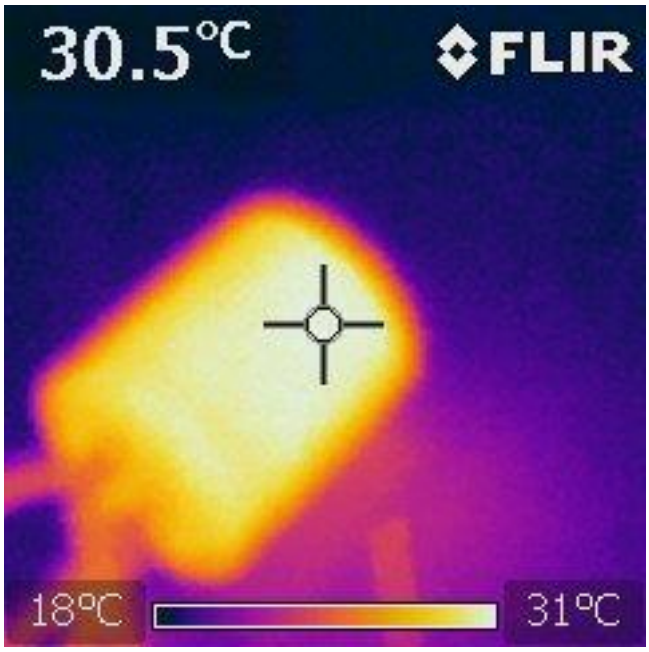


Fig3.32 – Measurement of capacitor internal temperature

As before, the first set of EIS measurements were taken using ten capacitors at a range of frequencies, where a mean of the measured impedances was found. These ten capacitors were placed within a metal tin placed within a thermal chamber, where the chamber temperature was set at 150°C. The temperature had been lowered from 175°C, to try to reduce the number of capacitors damaged to a state where they became unusable. After a number of hours, the tin was removed from the chamber and the capacitors were left to cool to room temperature, after which EIS measurements were taken again. Measurements may be seen plotted in Fig3.33.

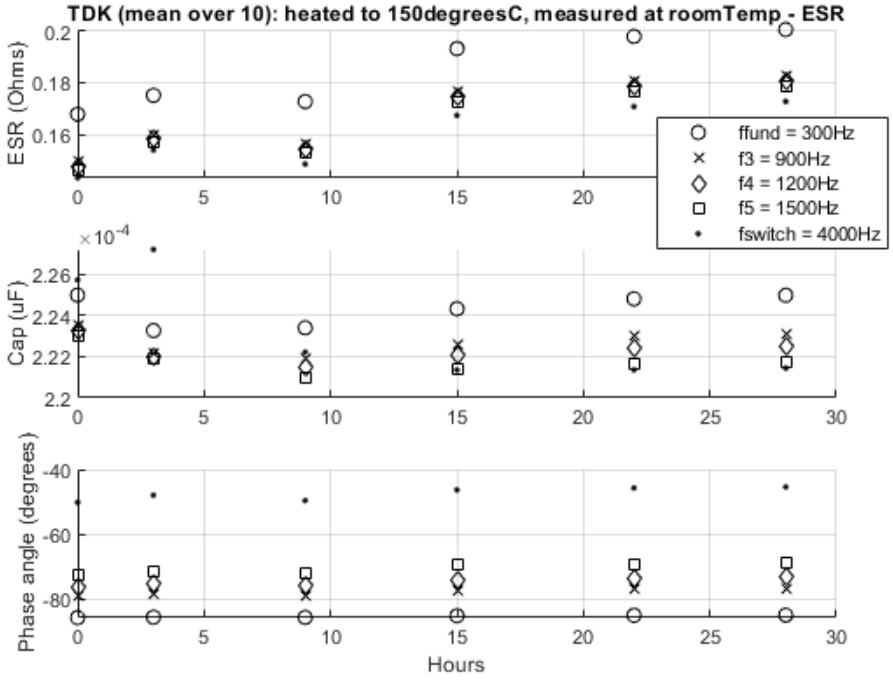


Fig3.33 – Second thermal cycling trial

Fig3.33 shows plots taken from the second thermal cycling trial. Although lacking as many data-points as the first trial, there is a clear increase in the mean resistive component of the capacitors. Although the capacitances did not noticeably change, there was enough of a phase-shift due to an increase in the resistances to show that the dissipation factor of the capacitors had changed, where dissipation factor is defined below in (3.13).

After examining the results, the Q-factor may be calculated. Q-factor has many definitions, with the definition used here being the ratio of energy stored to the amount lost per cycle [154]. Based on the defined expression of the Q-factor of a parallel RC circuit in [4], the Q-factor of the series RC circuit considered here is as follows:

$$Q_C = \frac{1}{\omega C R_C} = \frac{1}{DF} \tag{3.13}$$

where Q refers to Q-factor; where ω refers to angular frequency; where R refers to resistance; where C refers to capacitance; and where DF refers to the dissipation factor.

The implication is that the change in state of the capacitor may be seen discretely either through looking for clear changes in resistance or capacitance, or the ratio of

energy stored to energy lost may be observed for a definition of change of usefulness at a given frequency. This is shown in Fig3.34, where the Q-factor is calculated using (3.13) and the specific RC values over time are found from measured values shown in Fig3.32.

Following on from Fig3.33 and making use of (3.13), Fig3.34 summarises the behaviour of both the real and imaginary impedances in one variable. This graph shows that as time progresses, the energy in the 300Hz component reduces, either as a reduction in energy storage capability for a fixed amount of energy lost, or as an increase in energy lost for a fixed amount of energy stored.

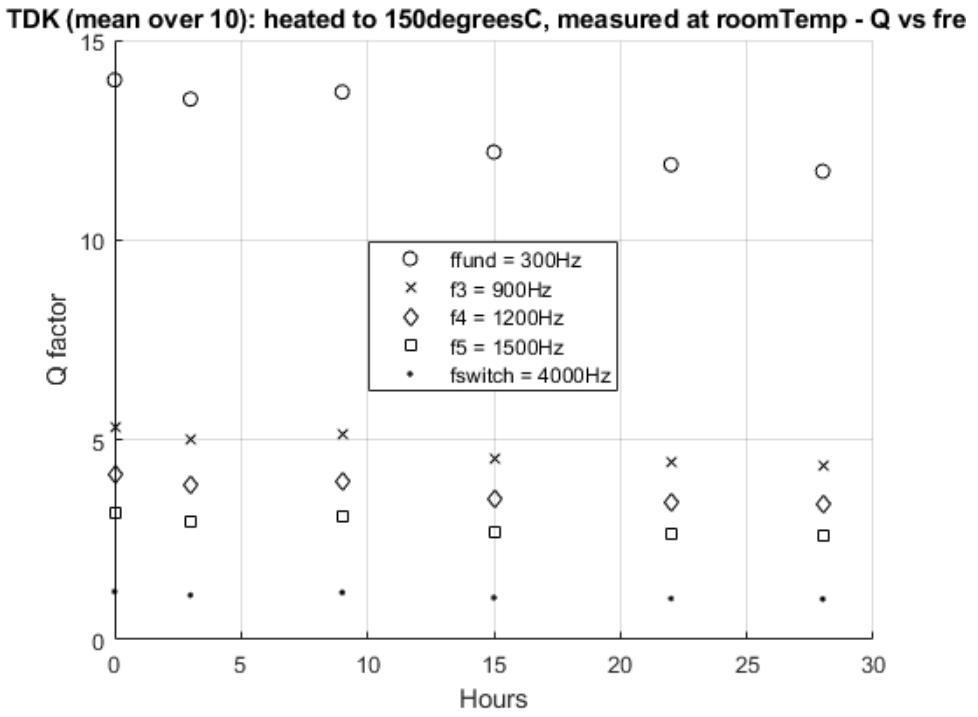


Fig3.34 – Q-factors calculated from the second thermal cycling trial

As frequency increases, there is less of a change in Q-factor: this is to be expected, as an ideal capacitor behaves as a high-pass filter in terms of its frequency response, where high-frequency signals face little loss of energy compared to low-frequency signals passing through the same filter. On the other hand, the -3dB frequency knee-point of a real capacitor shifts depending on the capacitor ESR and capacitance, meaning that as ESR increases as a capacitor ages, the amount of energy stored and lost at higher frequencies is unlikely to vary by too much until a capacitor starts to fail, whereas the amount of energy stored and lost at lower frequencies would decrease.

As a result, it is expected that a change in resistance would predominantly cause an observable effect at lower frequencies than around the switching frequency.

Looking forward, a possible rule-of-thumb when tracking changes in estimated capacitor impedance would be to reduce the number of variables tracked. In this case, the Q-factor may be tracked over time, looking for indications where the Q-factor consistently falls outside of an acceptable range. This would indicate failure of the capacitor, based on both components of its estimated impedance.

3.5.3 – Using a reverse bias voltage

The second method which was tested involved causing changes in capacitor impedance through causing migration of the dielectric medium present on the layers of the anode foil to layers of the cathode foil. This method made use of application of reverse bias voltages to the capacitor terminals. A variation of this method was described in [57].

Two particular issues in this task involved finding acceptable limits on the value of voltage applied across the terminals, as well as the amount of current allowed to flow through the cathode to the anode. The limitation on current and voltage were achieved through connecting test capacitors to a GW Instek PSH-2018A [155] DC power supply unit capable of operating in constant-current mode, where the maximum output voltage was limited along with the maximum output current.

Impedances of test capacitors were measured using a Rohde & Schwarz HM8118 [156] - shown in Appendix A, in FigA.4 - at intervals of approximately 1.5 hours. Measurements were taken at approximately the same core temperatures, using a handheld thermal camera, and this was to mitigate the effect of variation of impedance with core temperature as a source of measurement error. After some trial-and-error in finding suitable levels of voltage and current, two specific sets of results were found and presented here.

Fig3.35 and Table3.6 were produced where they show and list measured impedances taken after applying -20VDC and 50mA to a test capacitor. The table lists impedances at 300Hz, which is not in the linear region for measurements of both capacitance and resistance; most of the variation in voltage and current would be seen at harmonics of this frequency.

A 50mA current was found to be unsuitable for causing small changes in impedance after increments of 1.5 hours as the application of even a small current of 50mA was found to cause a rapid change in measured resistance of at least five times the original resistance, as well as a rapid decrease in capacitance which resulted in measured capacitances of almost half the rated value. This is seen in Fig3.35 and listed in Table3.6.

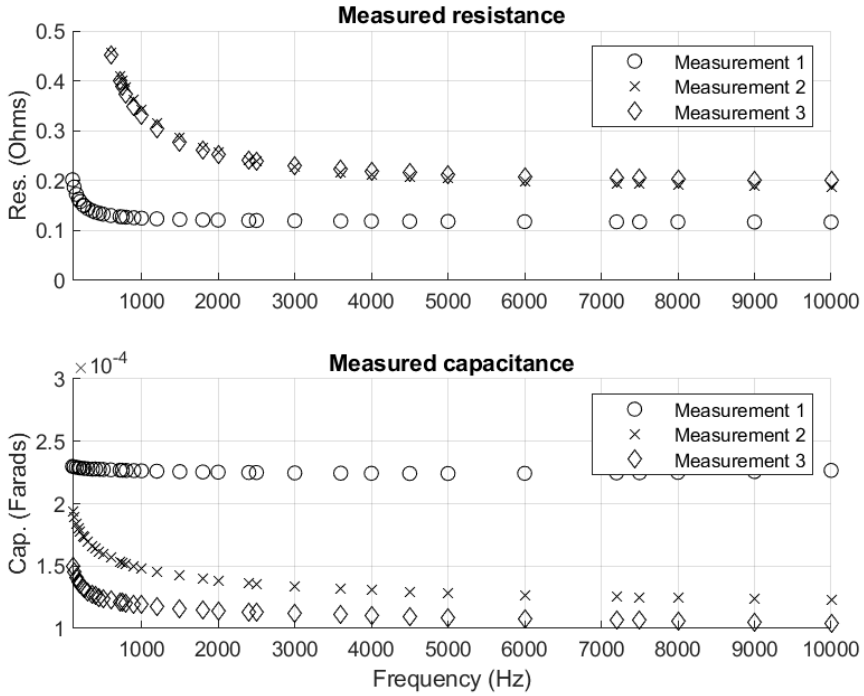


Fig3.35 – Measured impedances found using -20VDC and 50mA

	Measured Resistance (mΩ)	**Measured Capacitance (uF)**
Measurement 1	143.98	227.96
Measurement 2	723.14	169.32
Measurement 3	824.90	129.37

Table3.6 – Measured impedances found using -20VDC and 50mA, all at 300Hz

Fig3.36 and Table3.7 were produced where they show and list measured impedances taken after applying -20VDC and 10mA to a test capacitor. Again, the table lists impedances at 300Hz. Looking specifically at Measurement 4 in Fig3.36, the measurements after 2kHz were inaccurate due to the improper contact between measurement clips and the capacitor terminals: this was due to leaking electrolyte

preventing a solid contact between clips and terminals. This problem was corrected in the subsequent measurements.

A 10mA current was found to be suitable for causing small changes in impedance after increments of 1.5 hours. After each measurement, the resistance was found to increase by anywhere between approximately 5% and 50% of each previous measured resistance. Also, the capacitance was found to decrease by approximately 5% of each previous measured capacitance. This is seen in Fig3.36 and listed in Table3.7.

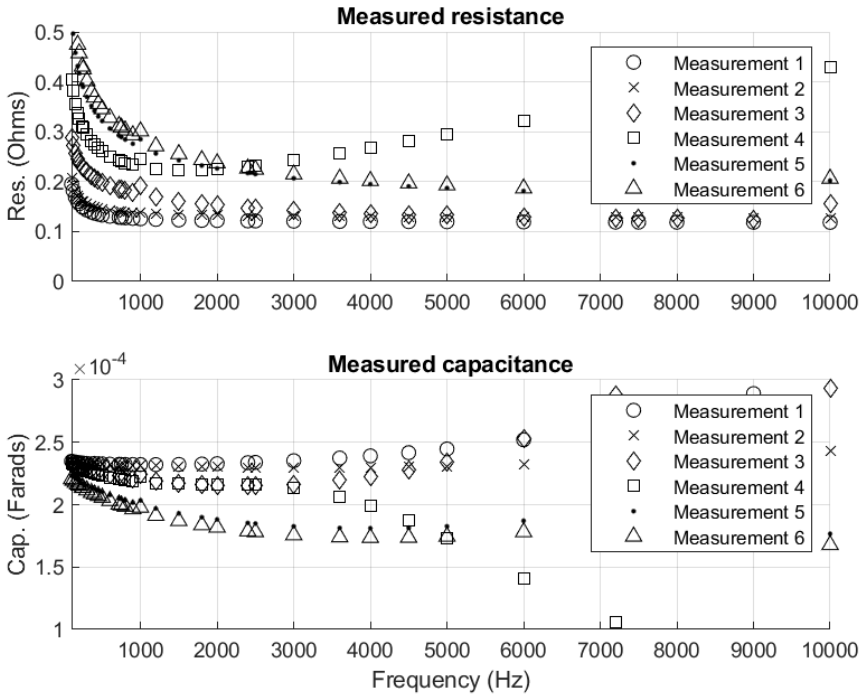


Fig3.36 – Measured impedances found using -20VDC and 10mA

	Measured Resistance (mΩ)	**Measured Capacitance (uF)**
Measurement 1	143.05	233.11
Measurement 2	154.88	232.87
Measurement 3	220.11	228.36
Measurement 4	294.14	226.89
Measurement 5	369.95	215.53
Measurement 6	401.87	211.62

Table3.7 – Measured impedances found using -20VDC and 10mA, all at 300Hz

Comparing Table3.6 with Table3.7, it was clear that application of -20VDC across the capacitor terminals with a small flow of current could cause a change in impedance of the capacitors. The difference between the two tables was the amount of current flowing through the capacitors, where permitting 50mA of current to flow caused a rapid change in measured capacitor impedance and permitting 10mA of current to flow slowed down the rate of change of impedance over time.

This specific method of aging batches of capacitors allowed impedances to be changed rapidly compared to the process of aging reliant on maintaining high core temperatures, which is desirable when attempting to produce many batches of aged test capacitors. However, this method relies upon causing migration of the dielectric medium from the anode layer to the cathode layer through application of a reverse bias voltage to a capacitor. As migration of the dielectric layer is considered to be unlikely in practice in a power converter due to its dependency on the reverse bias voltage, this specific failure mechanism was understood to be appropriate for causing controlled changes in impedance but was not pursued further in this project due to this failure mechanism being unlikely in practice, as well as the uncertainty of the effects of causing changes in the arrangement of the dielectric medium on the aluminium layers.

3.6 – Summary

Impedance estimation was investigated using time-domain, frequency-domain, and time-frequency-domain transforms, making use of measured capacitor voltages and currents. A benchmark comparison was made using the transforms and the benefits and drawbacks of each transform were discussed.

Having taken a benchmark comparison, the CWT was found to be appropriate for observing changes in estimates of capacitance and resistance. The specific impedance estimation technique used in further chapters will make use of the complex Morlet mother wavelet as was described in section **3.2.4**. Using this frequency transform, simulations and experimental work were presented with insights to clarify both the behaviour of the estimation and reasons for discrepancy between expected results and obtained results. This was to ensure that this frequency transform may be used to find accurate estimates of capacitance before making use of capacitors within an operational drive, where a drive will be used for further testing in the next chapter.

Thermal issues were explored, where a method was devised for intentionally accelerating the age of batches of capacitors. The specific aging mechanism used to produce batches of aged capacitors for work in the next chapter will make use of prolonged heating as described in section **3.5.2.2**. This is because this method rapidly reduces the lifetime of capacitors in a controlled manner, which should allow experimental work to be completed in the lifetime of the project. A method of rapidly aging capacitors through causing migration of the dielectric medium from anode to cathode was also presented, but rejected due to the uncertainty of the effect of varying the dielectric medium on the aluminium layers.

A thermal model was described, and the difficulty of accurately estimating the value of the resistive component was shown, as well as the reasons for this difficulty. The thermal model was found to be impractical based on laboratory testing. As a result, the impedance estimation based on the electrical model was found to be of more use to this project.

One issue which must be addressed is the following: as the rate of change of the capacitor ESR would be accelerated via application of high temperature, the question would be how to determine the effect on the instantaneous ESR estimate between either the high capacitor core temperature or the effect of the accelerated ageing process upon the capacitor impedance.

There are at least two possible answers, with the first answer specifically addressing measurement issues: external factors *such as high temperature* acting upon the capacitor core can be neglected if all measurements/estimates of the capacitor impedance were to be taken at the same capacitor core temperature, as well as by extension at the same bias voltage, altitude, humidity levels, etc. Regardless of external factors, variations in the capacitor core temperature are the main limiting factor in accurate impedance estimation. Although measurements or estimates of capacitor impedance would clearly vary as core temperature varies – as was established in **Chapter 2** – it would be possible to obtain repeatably consistent measurements or estimates of the same impedance assuming the core temperature were to be constant.

Alternatively, the second answer: an understanding of the structure of the electrolytic capacitor is required as was described in section **2.2**, where the contributions of the different parts of the capacitor were addressed. If the high temperature were to be

correctly and successfully applied as part of the accelerated ageing process, the volume of liquid electrolyte within the capacitor can would reduce and the impregnated paper would dry up, thereby leading to an increase in ESR and eventual shorts between the aluminium foil anodes and cathodes. On the other hand, if the high temperature were to be incorrectly or unsuccessfully applied, the capacitor would otherwise risk failure due to damage instead being limited to, for example: the metal contacts protruding outside of the insulation; damage to the outer layer of insulation and therefore potentially causing damage to the inner layers of insulation; or damage to the aluminium oxide dielectric layers, which would lead to catastrophic damage due to increased leakage current through the capacitor.

Chapter 4 – DC-Link Impedance Estimation via Capacitor Current

4.1 – Introduction

The previous chapter discussed equivalent electrical and thermal models of capacitors, as well as mathematical transforms which may be used to produce estimates of capacitor impedance. This chapter expands upon these ideas, considering the use of these ideas experimentally.

This chapter will discuss identifying frequencies relevant to the operational motor drive, as well as propose tests for achieving accurate impedance estimation under a range of conditions of load torques, injection frequencies, switching frequencies, motor frequencies, and capacitor core temperatures. A brief comparison study will be undertaken examining a batch of aged capacitors used in an operational drive.

4.2 – Identification of frequencies of interest

A specific industrial drive was chosen for experimental use: the Siemens G120C PN FSAA 2.2kW. Fig4.1, 2 were taken from the drive schematic, showing the connections of the input and output stages of the motor-drive in relation to the electrolytic capacitors in question.

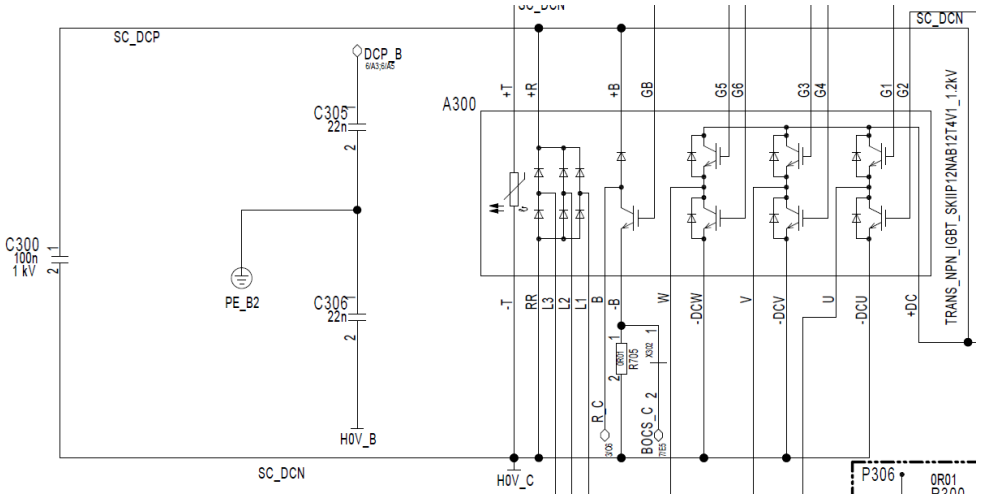


Fig4.1 - FSAA schematic, power module circuit diagram

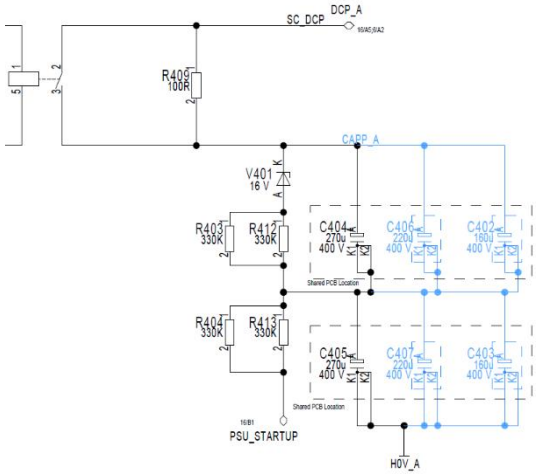


Fig4.2 - FSAA schematic, DC-link circuit diagram

The simplified circuit diagram of the DC-link is presented in Fig4.3, assuming a lumped 4% (approximately 1mH) reactor on the input of the DC-link. This value is taken as a "typical" value for input reactance, as recommended by the project sponsors.

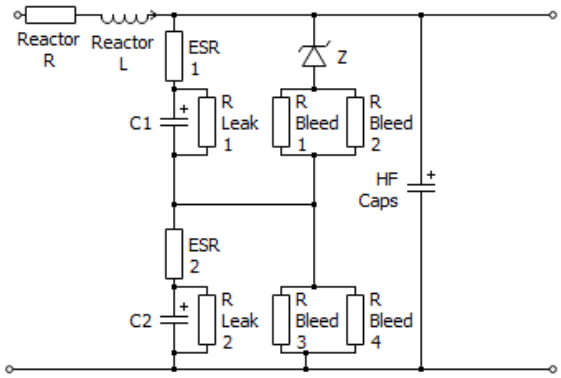


Fig4.3 - Simplified DC-link circuit

The circuit shown in Fig4.3 has been shown in the previous chapter. A lumped 4% reactor is present on the top left of the circuit, and high-frequency capacitors were present on the right of the circuit. Bleed resistors were included to rapidly discharge the capacitors, and the capacitors themselves were modelled as having a capacitance and an equivalent series resistance (ESR) in series, with a leakage resistance placed in parallel across the capacitance. Table4.1 lists the values used in Fig4.3, where values of capacitance and ESR were measured using an electrochemical impedance spectroscopy (EIS) tool.

C1, 2	Nominally 270uF, measured via EIS
ESR1, 2	Nominally 160mΩ, measured via EIS
Rleak1, 2	100kΩ
Rbleed1, 2, 3, 4	300kΩ
HF Caps	111nF
Reactor R	100mΩ
Reactor L	1mH

Table4.1 – Values used in Fig4.3 to produce Fig4.4

Through finding the transfer function of circuit shown in Fig4.3 (looking at the ratio of voltage out to voltage in) and using the values shown in Table4.1, Fig4.4 can be obtained.

Fig4.4 shows the Bode plot magnitude and phase response representations of the circuit shown in Fig4.3 for two capacitors of different levels of ageing; these capacitors were real capacitors, i.e., practical measurements were used to generate Fig4.4. The Bode plots were generated using experimentally derived data. The method of ageing the capacitors has been described in the previous chapter, specifically making use of prolonged heating of batches of capacitors as described in section **3.5.2.2**.

The different levels of damage referred to in Fig4.4 refer to one capacitor which has been subject to extended periods of accelerated ageing in comparison to another capacitor which has not been subject to the same ageing process, instead being taken directly from a factory-sealed box of capacitors. It is worth noting that the effect of natural ageing of a capacitor due to being placed in storage prior to usage is not considered here.

It can be seen from the top plot of Fig4.4 that change in the magnitude of the DC-link impedance may be observed at frequencies in the range of 10kHz to 10MHz, denoted by the arrow spanning between the red dashed line (middle line) and the purple dashed line (right-hand-side line); and it can be seen in the bottom plot of Fig4.4 that change in the phase of the DC-link may be observed at frequencies in the range of roughly 400Hz to 10kHz, denoted by the arrow spanning between the blue dashed line (left-hand-side line) and the red dashed line (middle line).

The flat region between 10kHz and 10MHz shows suggests that the impedance is not frequency dependent and is dominated by resistance, or poles and zeroes cancel.

Additionally, the curved region between 400Hz and 10kHz shows that an effect is seen here of poles or zeroes in the frequency domain, meaning the effect of a capacitor or inductor is more influential. As the phase in this region is in the range of 0° and -90°, the dominant reactive element here is a capacitor. As a result of the dominance of the resistance and capacitance in these two frequency ranges, it was inferred that it would be best to separately estimate resistance and capacitance at these ranges.

The graphs do not indicate that only resistance may be estimated in the flat region (right-hand-side) or that only capacitance may be estimated in the curved region (left-hand-side). However, as the actual impedance of an electrolytic capacitor varies with the potential across the terminals of the capacitor, the Bode plot in Fig4.4 was used to provide a rough rule of thumb on which to base further work estimating resistive and reactive elements individually.

Many of the frequencies in these ranges, such as DC to 10kHz, may be measured in the motor phase currents and voltages, as well as in the drive electrolytic capacitor currents and voltages. Here, the challenge was to identify specific frequencies of interest and extract as much information as possible in as few steps as possible.

This stage of the work was theoretical, and so measurement accuracies relating to signals at frequencies between 10kHz and 1MHz were not considered. Practically, it would be expected that it would be difficult to accurately measure very high frequency content as electrolytic capacitors are generally designed to be used for the “low” frequency range, i.e., well below 1MHz.

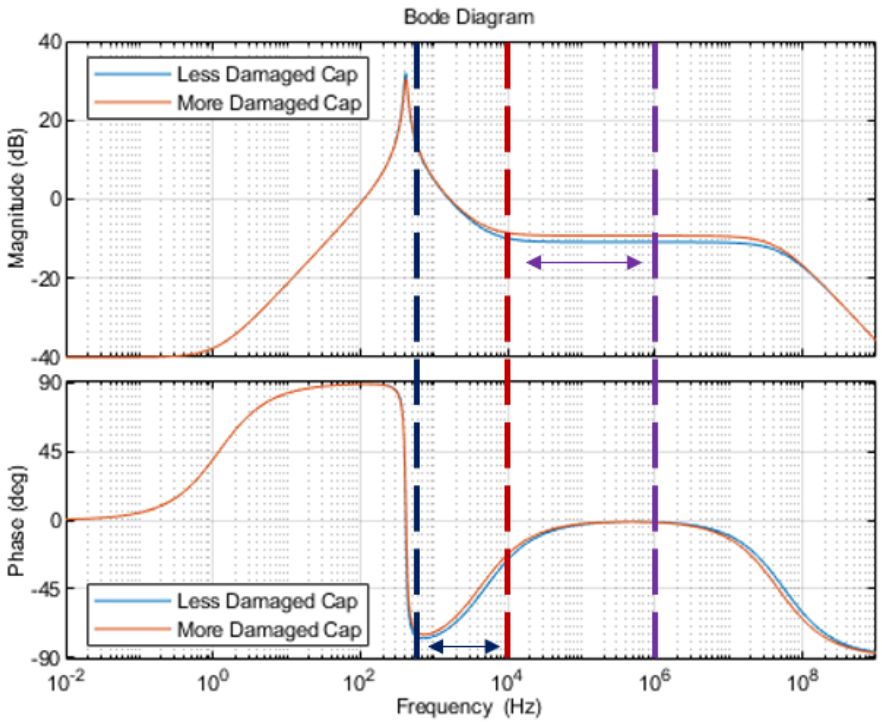


Fig4.4 - Bode plot of simplified DC-link circuit

4.3 – Drive DC-Link frequency spectrum

4.3.1 – Measurement of inverter quantities

To characterise the frequency content of the DC-link voltage and currents, experimental measurements were taken of the voltages across and currents through the electrolytic capacitors with the drive driving a loaded motor and the load being varied between 0% and 90%. The drive switching frequency was set at 4kHz, and the motor speed reference was 40Hz. The values of the relevant components in the DC-link are presented in Table4.1.

To access the DC-link current for measurement, the power module was removed from the drive casing and opened out, as shown in Fig4.5. The control unit was connected to a desktop PC via RS232-to-USB communication; the control unit itself was powered via the DC-link voltage through a transformer and converter which provided 24V to the control unit circuitry.

An external table-top fan was used to provide forced airflow to the PCB and the Semikron switching module; this was to prevent the on-board temperature sensors from reporting overtemperature conditions which would otherwise cause the drive to trip to a FAULT state. A side effect of using the forced cooling was that the drive-

mounted electrolytic capacitors were held at room temperature whilst the drive was powered, and the attached motor was in operation; temperature variation of the capacitor casing was minimal.

The voltage across the DC-link was measured using a Pico Technology differential 25MHz 700V probe [157], and a Fluke i30s 100kHz current clamp [158] was used to measure current through the electrolytic capacitors. An analogue RC low-pass filter was used at the input of the data-acquisition unit (DAQ), with a cut-off frequency of 12kHz as an anti-aliasing filter. The DAQ was made up of a NI cDAQ-9174 [147] and NI-9222 [148]. The DAQ sample rates chosen for this section was 50kHz. Sampling windows of 10s were used, providing a 0.1Hz frequency resolution. A space-vector modulation (SVM) modulation scheme was used [159], with the inverter switching at 4kHz. The practical arrangement of the drive under test (DUT) is shown in Fig4.5.

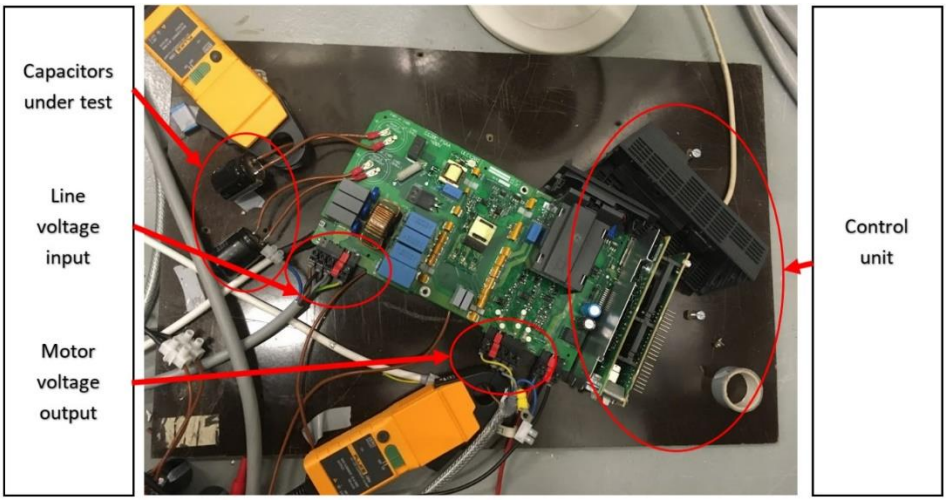


Fig4.5 - Practical arrangement of DUT

Fig4.5 shows the drive PCB outside of the protective casing; access to line voltages were provided through the tabs on the lower left-hand side of the PCB, and access to the motor voltages is provided through the tabs on the lower right-hand side of the PCB. The capacitors under test, on the upper left-hand side of the PCB, were attached to the PCB through use of brass bolts and nuts threading the holes on the PCB usually reserved for the capacitor through-hole legs. The legs of the capacitors were soldered to short lengths of 1.5mm^2 multi-stranded copper wire cables which were in turn crimped using fork terminals, where the brass bolts and nuts were used to secure the capacitors via fork terminations to the board. The short lengths of copper wire cables act as sources of parasitic resistance and inductance, but the contributory impedances

of the cables were found to be small enough to not influence the net capacitive contributions of the two in-series capacitors.

This arrangement of securing capacitors to the board was considered to be less damaging to the PCB and to the capacitors in the long term, as the capacitor connection holes were found to be placed upon sizeable copper pads, which would have meant a large amount of heat would have been required for capacitor solder joints in order to remove capacitors.

4.3.2 – The loading system

The inverter being tested was loaded using a motor under encoder-less speed control. The load drive used in this work was a Control Techniques UNI2402 7.5kW drive [160], where the load motor was controlled using encoder-fed torque control. This drive is shown in Fig4.6.



Fig4.6 - Load drive

The motors used in this work are shown in Fig4.7. These induction motors were coupled via a shared shaft, and the motors were identical. The motors' nameplate is summarised in Table4.2.



Fig4.7 - MUT (left) and load motor (right)

Grid Frequency (Hz)	50
Power Rating (kW)	2.2
Line Voltage (V)	415 (Y)
Line Current (A)	4.9 (Y)
Rated Speed (rpm)	1415
Power Factor	0.80

Table4.2 – Induction motor nameplate values

The drives and motors were connected together as indicated in Fig4.8, with the system under test being enclosed in the red box.

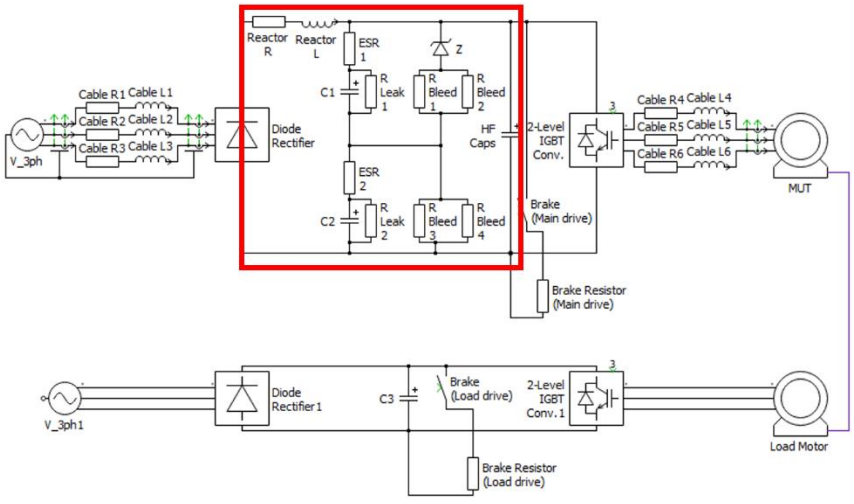


Fig4.8 - Circuit arrangement with test motor and drive and load motor and drive

4.3.3 – Experimental results

Fig4.9,10 show the last 100ms of voltages and currents captured during steady state operation with two different torque levels imposed upon the motor under test. There were no obvious differences when analysed in the time domain. This data was therefore also analysed in the frequency domain.

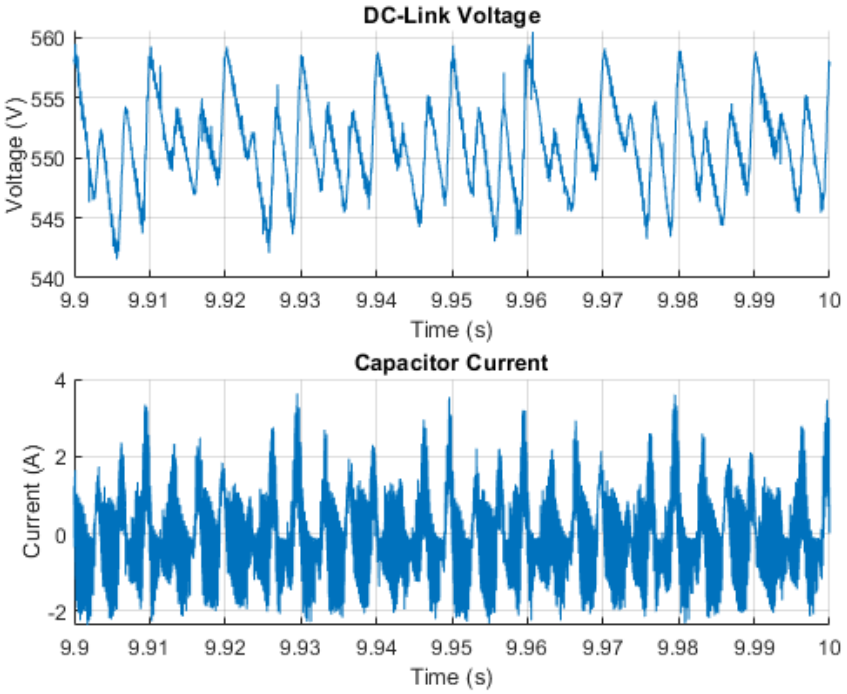


Fig4.9 - Drive waveforms with motor load torques of 00%

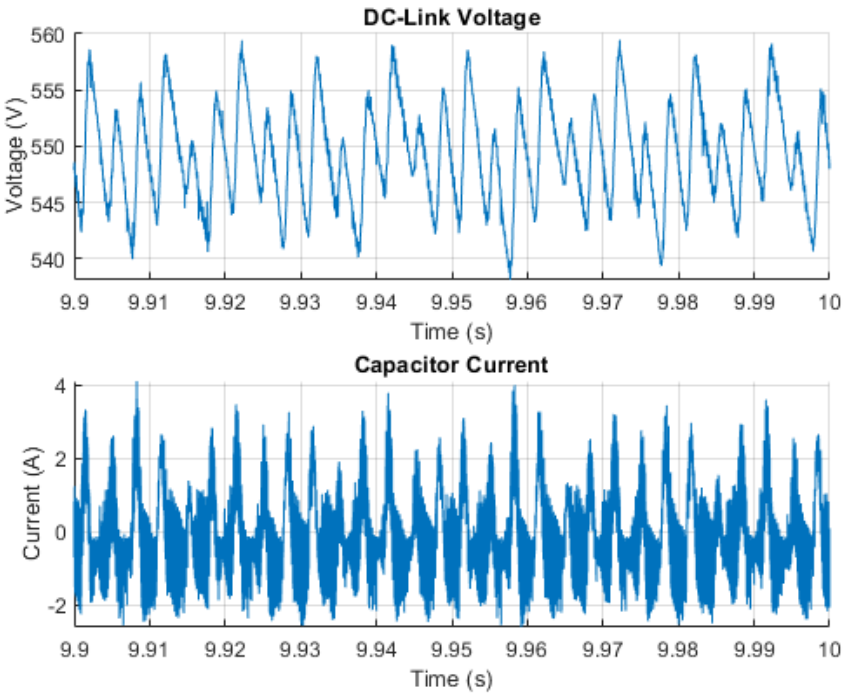


Fig4.10 - Drive waveforms with motor load torques of 90%

Graphs showing the FFT outputs based upon the recorded quantities were generated, where magnitudes seen in the FFT graphs were taken from the absolute values of the complex output of the FFT. Blackman windows were used in each case.

Particular attention was paid to three frequency ranges: 0Hz - 1kHz (Range 1); 3.6kHz - 4.4kHz (Range 2); and 7.6kHz – 8.4kHz (Range 3). These three particular frequency ranges were chosen based on the knowledge that frequencies of interest in motor current would typically be at frequencies below 1kHz, or would be grouped around harmonics of the inverter switching frequency. Here, only the first two harmonics of switching frequency were considered.

Frequencies above 10kHz were not considered, where this was due in large part to the knowledge that the signals passing through electrolytic capacitors within a motor-drive would have most of their energy content located in the low-frequency region; as a result, 10kHz was chosen as an arbitrary cut-off point. Conveniently, choosing a cut-off point of 10kHz meant that the second harmonic of a switching-frequency of 4kHz would fall within the frequency range of interest.

Referring back to the Bode plot in Fig4.4, discussion of the graph stated that 400Hz – 10kHz would be a suitable range for tracking changes in reactance, i.e., due to changes in the phase in this frequency range. For this reason, Range 1 and Range 2 would ideally

be used for estimation of reactance. The same discussion stated that resistance would ideally be estimated using a minimum frequency of 10kHz based on the positioning of dashed line placed according to differences between magnitude responses of two capacitors (the orange line and blue line), i.e., due to changes in the magnitude in this frequency range. However, the magnitude responses actually start to differ before 10kHz, with a difference of 1dB and approximately 5 degrees in the phase between the two responses being observable at as low as approximately 4kHz, meaning that Range 2 and Range 3 may be used for estimation of resistance.

To further investigate the frequency ranges of interest, the FFT was applied to measured capacitor voltage and current, specifically to look at changes in distribution of frequency peaks. Specifically, the aim was to look at existing peaks in the frequency spectrum before tampering with capacitors or injecting signals from outside the motor drive system. Whilst it was expected from prior knowledge that certain peaks would exist in the capacitor voltage and current frequency spectra – such as the frequency content induced by the six-pulse diode rectifier bridge, as well as a pair of sideband peaks around the multiples of switching frequency – it was speculated that other peaks must exist within the frequency spectra, and that it would be best to investigate the feasibility of making use of these existing peaks for any further estimation purposes.

Fig4.11,12 show the FFT graphs based upon measured capacitor voltage, and Fig4.13,14 show the FFT graphs based upon measured capacitor current. Voltages and currents were measured whilst the motor was either unloaded or loaded at 90% of rated load torque. The change in loading conditions was to examine the frequency spectra for changes due to loading conditions.

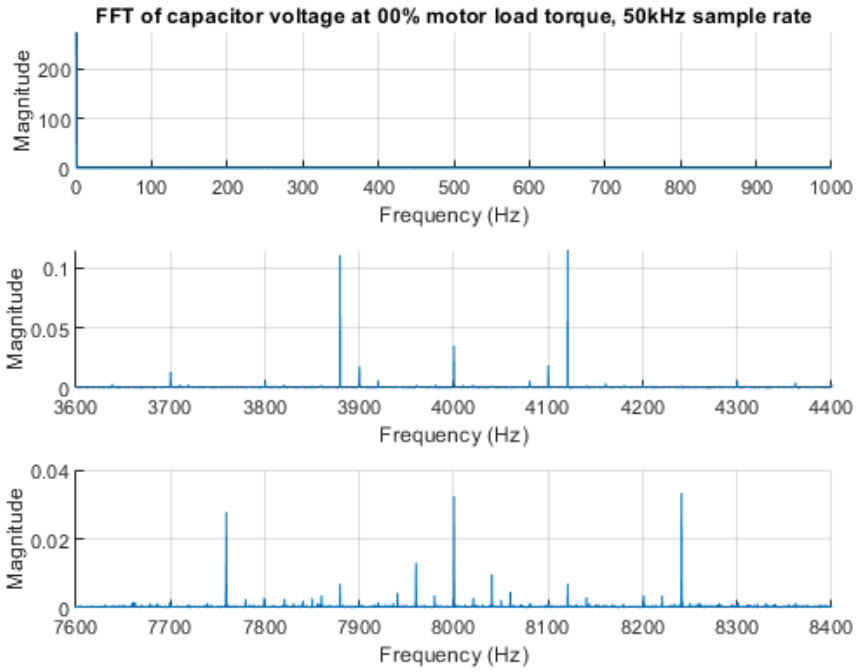


Fig4.11 - FFT of measured capacitor voltage with motor load torques of 00%

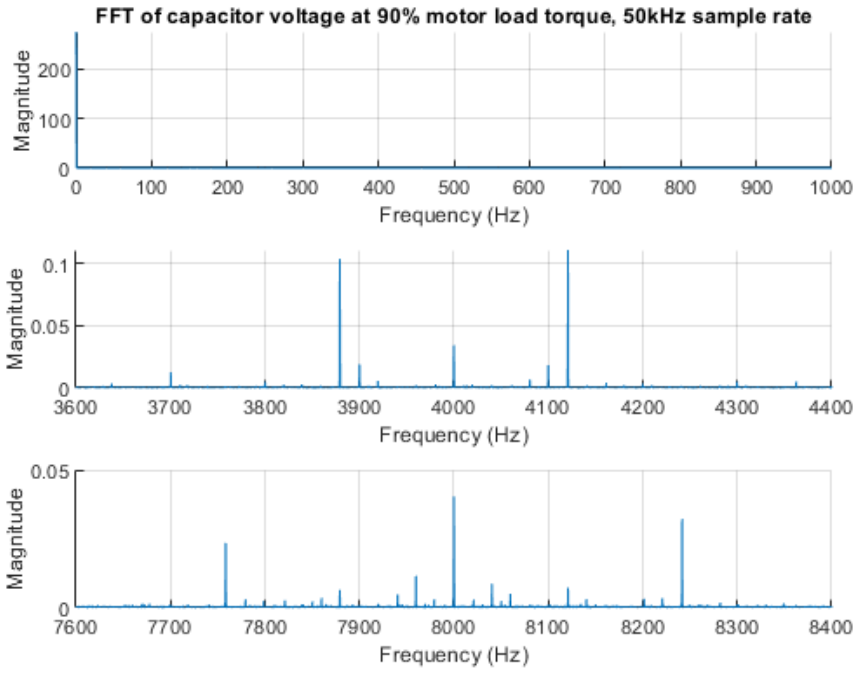


Fig4.12 - FFT of measured capacitor voltage with motor load torques of 90%

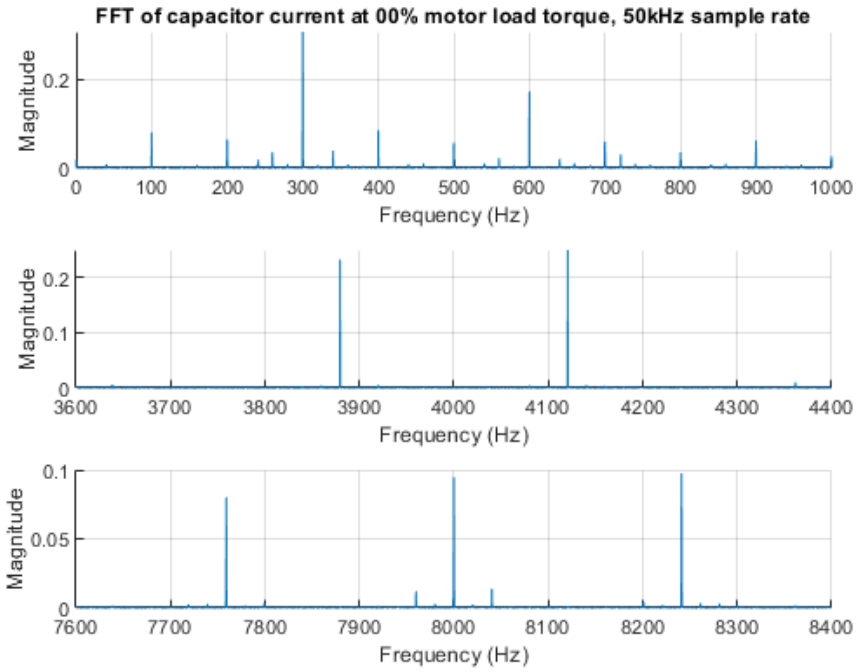


Fig4.13 - FFT of measured capacitor current with motor load torques of 00%

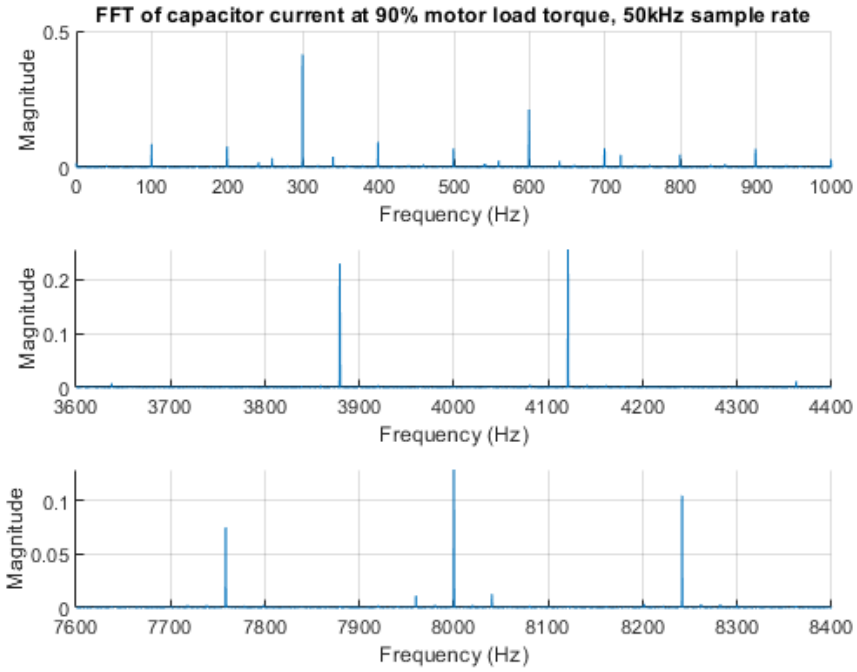


Fig4.14 - FFT of measured capacitor current with motor load torques of 90%

It can be seen from Fig4.13,14 that in the frequency range below 1kHz, the dominant frequencies were multiples of 300Hz, frequencies associated with the six-pulse diode rectifier. Additionally, the stator frequency f_{stat} (40Hz) was present, as well as

harmonics of the stator frequency. The stator frequency itself increased slightly with increases in load.

In the frequency range around the first switching harmonic ($f_{sw} \pm 400$), the main frequencies of note were found at

$$f_{sw} \pm 3f_{stat} \qquad (4.1)$$

where f_{sw} refers to the switching frequency; and where f_{stat} refers to the stator frequency.

In the frequency range around the second switching harmonic ($2f_{sw} \pm 400$), the main frequencies of note were found at the second switching harmonic itself as well as at

$$2f_{sw} \pm 6f_{stat} \qquad (4.2)$$

where f_{sw} refers to the switching frequency; and where f_{stat} refers to the stator frequency.

In the case of the second switching harmonic, the magnitude of the peak of the second switching harmonic itself was greater in magnitude than the peak of the first switching harmonic, but the peak of the second switching harmonic was found to increase in magnitude as the load torque applied to the motor increased.

Neglecting the presence of the frequency content contributed by the six-pulse diode rectifier, some frequencies of note are listed in Table4.3, captured from the FFT spectrums seen in Fig4.12,14:

Frequency (Hz)		**Voltage (V)**	**Current (A)**
40.3	f_{stat}	0.3071	0.0070
403	$10f_{stat}$	0.0015	9.8210e-15
4000	f_{sw}	0.0342	0.0014
4120.8	$f_{sw} + 3f_{stat}$	0.1111	0.2559
3879.2	$f_{sw} - 3f_{stat}$	0.1039	0.2295
8000	$2f_{sw}$	0.0404	0.1286
8241.6	$2f_{sw} + 6f_{stat}$	0.0322	0.1043
7758.4	$2f_{sw} - 6f_{stat}$	0.0235	0.0747

Table4.3 – Noteworthy frequencies, taken from Fig4.12,14

Table4.3 shows noteworthy frequencies found using (4.1) and (4.2), specifically harmonics of the switching frequency and harmonics of the stator frequency. Some of the frequencies presented in Table4.3 show magnitudes that are comparatively higher than the frequencies in the surrounding frequency regions; these frequencies were tabulated due to the prominence of the peaks graphically at these frequencies, as well as due to the fact that the sensors used to measure voltages and currents have limits to their sensitivity. It was considered better to ignore frequencies with negligibly low magnitude peaks due to the difficulty in distinguishing "legitimate" frequency content from artefacts caused by either quantisation noise or system noise.

From Table4.3, it was clear that without any modifications having been made, the motor-drive frequency spectrum presented noticeable peaks at heterodyne frequencies, where each frequency could be located through combinations of sums of switching frequency integer harmonics and stator frequency integer harmonics. A short explanation of the heterodyning process is briefly described in **Appendix C**.

Referring to Fig4.4, the frequencies surrounding the first two switching harmonics may be seen to be close to or within the frequency region that was suggested as suitable for finding estimates of resistance.

Similarly, the sub-1kHz frequencies may be seen to be close to or within the frequency region that was suggested as suitable for finding estimates of reactance. However, as much of the sub-1kHz region is dominated by the six-pulse diode rectifier, and as it is unlikely to easily make use of the six-pulse diode rectifier frequency components, all frequencies which are integer harmonics of $6f_{grid}$ must be disregarded. Based on Fig4.11,12,13,14, these frequencies would be 300Hz, 600Hz, 900Hz in the range below 1kHz, and – even with these frequencies being intentionally ignored – these frequencies would dominate in this frequency range due to their comparatively large magnitudes.

4.3.4 – Conclusions from initial tests

The tests presented in this section show that the frequency content found via experimental measurements of the DC-link quantities (capacitor voltage and capacitor current) were small and were unlikely to give sufficient signal-to-noise ratio to allow calculation of capacitor values.

It would be advantageous to make use of existing frequency content as drive and motor behaviour may be easily tracked via measurement of electrical signals.

However, with the SNR of existing signals being a limiting factor, it was considered inappropriate to try to make use of the existing frequency content as any error due to poor SNR would simply compound and impedance estimation accuracy would suffer as a result.

Therefore, the next sections examine methods to increase the SNR by creating specific signals to “inject” into the DC capacitor.

4.4 – Improving the SNR of DC-link measurements through signal injection

4.4.1 – Introduction to signal injection

The previous section clearly demonstrated that under normal operating conditions, the frequency content (and signal strength) of the measured capacitor current and voltage were not good enough to provide a reliable estimate of the impedance of the DC-link capacitor. This section will show that this can be addressed by specifically injecting a signal into the DC-link at a suitable frequency. Results will demonstrate that the parameters of the DC-link capacitor can be identified with sufficient accuracy. Subsequent sections will show how a similar injection can be achieved in a more realistic way for a real drive.

4.4.2 – Proposed signal injection approach

Fig4.15 shows the proposed experimental system, where a controlled AC source has been connected into the DC-link capacitor circuit. This AC source is connected via “bypass capacitors” C3 and C4, which block the DC component of the DC-link voltage (set up by the diode rectifier) from damaging the AC supply. This leads to some attenuation of the actual AC voltage imposed, compared to its reference value, and this also limits the maximum frequency which can be injected.

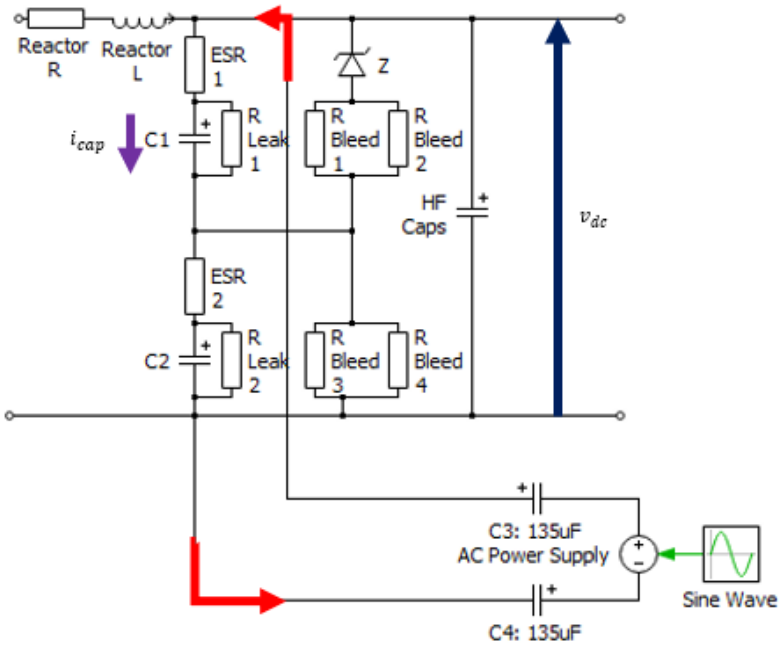


Fig4.15 - Circuit diagram of injection arrangement

A GW Instek APS-7100E AC power supply [146] - capable of outputting sine-wave signals of controllable voltages and frequencies in the range of 45Hz-500Hz – was used as shown in Fig4.16. The yellow box to the left of the image is the single-phase isolating transformer which isolates the AC power supply from the DC-link of the inverter. For safety, the inverter was also floating through use of a three-phase isolating transformer at the input of the diode rectifier.



Fig4.16 - AC power supply used for injection, and isolating transformer

To test the feasibility of injection of controlled signals directly into the DC-link and attempting to find estimates of DC-link impedance, the drives and motors were connected as shown in Fig4.17. The red box is used to show the circuit under test.

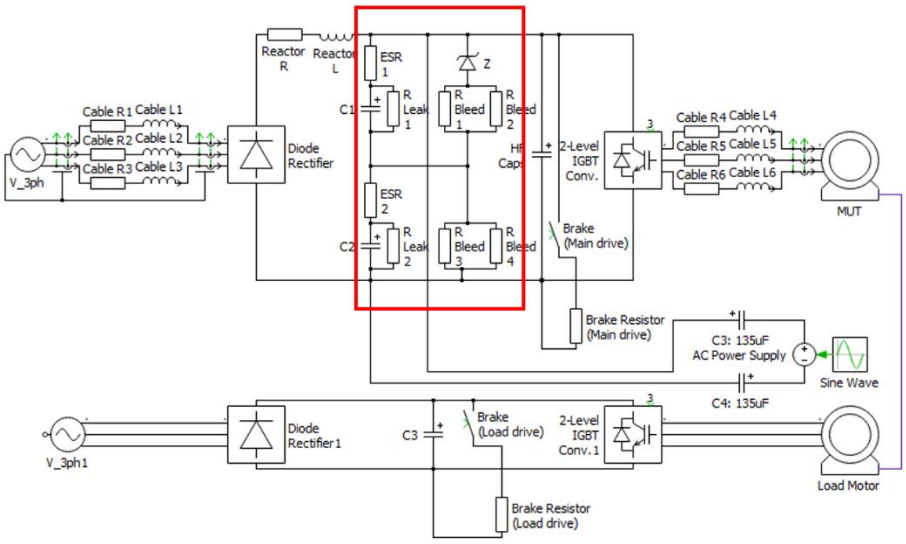


Fig4.17 - Circuit arrangement with test motor and drive and load motor and drive, with injected signal

The two commercial drives were enabled initially to operate the drive to a similar way used in the previous section. The AC power supply was then enabled, and its frequency/amplitude adjusted to perform an injection test.

4.4.3 – Data capture and data processing

For this series of tests, one pair of capacitors was taken from a factory-sealed box of capacitors and subject to a set of tests: these capacitors can be considered to be a control set. This was to ensure that no ageing process had been applied to the capacitors as part of this work, to provide a good baseline to compare capacitors which had been subject to the same tests after being aged.

Test conditions were varied to determine whether the estimated capacitor parameters varied as a function of operating conditions.

The following measurements were taken at steady-state. Ten sets of samples were taken for each individual measurement point. The first set of measurements were taken as a benchmark. The values in bold show which variable was changed in each test.

Frequencies of 233Hz and 487Hz were chosen for use with signal injection due to the fact that the AC power supply unit used to provide the injected signals had a maximum frequency limit of 500Hz, as well as due to the fact that both of the frequencies 233Hz and 487Hz are located at prime numbers that would not arise naturally in the frequency spectrum due to effects involving integer multiples of existing frequency content.

- Motor speed **40Hz**, switching frequency **4kHz**, injection voltage ripple **10Vrms**
    - Sampling at 50kHz
        - No injection or injection at 233Hz or 487Hz
            - Load torques of 0%, 25%, 50%, 75%, 90%
- Motor speed 40Hz, switching frequency **6kHz**, injection voltage ripple 10Vrms
    - Sampling at 50kHz
        - No injection or injection at 233Hz or 487Hz
            - Load torques of 0%, 25%, 50%, 75%, 90%
- Motor speed **10Hz**, switching frequency 4kHz, injection voltage ripple 10Vrms
    - Sampling at 50kHz
        - No injection or injection at 233Hz or 487Hz
            - Load torques of 0%, 25%, 50%, 75%, 90%
- Motor speed 40Hz, switching frequency 4kHz, injection voltage ripple **2.5Vrms**
    - Sampling at 50kHz
        - No injection or injection at 233Hz or 487Hz
            - Load torques of 0%, 25%, 50%, 75%, 90%

A total of 600 samples were taken for the six test cases listed above. Oversampling was used in this test, both in terms of number of samples and sampling frequency, for the following reasons:

- The voltage supply of the drive was imperfect, meaning the DC-link voltage was seen to fluctuate noticeably when random sample measurements were taken. To smooth out variations in the mean DC voltage without applying phase-altering filtering techniques, a mean of 10 measurements were taken for each sample point, giving a clearer, less noisy picture of the frequency components of the various recorded quantities.
- The maximum sampling rate available for the DAQ is 500kHz. However, a sample frequency of 50kHz adequately represents the data captured without

incurring significant processing costs. 50kHz is high for a current commercial drive, but allows us to investigate a significant range of frequencies present. A resolution of 0.1Hz has been used by using sample windows of 10s worth of data.

Taking ten samples of data for each of the four tests using a sample rate of 50kHz and a sample window of 10s meant a large amount of data was generated and would need to be parsed for useful datapoints.

FFTs were taken of each data sample, and specific heterodyne frequencies of interest were identified. These frequencies were calculated as described in (4.3), based on knowledge of the effect of interactions between the motor switching frequency and the motor stator frequency, and where the injection frequency term is also considered:

$$f = \pm x f_{sw} \pm y f_{stat} \pm z f_{inj} \qquad (4.3)$$

$$x, y, z, = 0, 1, 2, \dots, maximum\ harmonic$$

where f_{sw} refers to the switching frequency; where f_{stat} refers to the stator frequency; and where f_{inj} refers to the injection frequency.

Based on calculations using (4.3), frequencies that were not considered were those calculated to be below 0Hz; frequencies smaller than the stator frequency; and frequencies that were integer multiples of the 300Hz contributed by the diode rectifier.

After identifying specific frequencies of interest, the DC-link voltage and capacitor current were passed through a wavelet transform and an FFT. The frequency responses of voltage and current were found at each identified frequency, and estimates of resistance and capacitance found for each frequency using the wavelet transform. The FFT was applied to the same voltages and currents to look for peaks in the frequency spectrum at the identified frequencies.

As noted in section **4.3.3**, the frequency content of the original DC-link voltage and electrolytic capacitor current included frequencies that were sums and differences of combinations of integer harmonics of switching frequencies and stator frequencies. With an additional frequency signal introduced to the DC-link via signal injection, it was hypothesised that additional peaks may be generated due to sums and differences

of integer harmonics of switching frequencies, stator frequencies, and now also injection frequencies, as indicated in (4.3).

An attempt was made to generate a list of possible frequencies of interest - further extending the list of frequencies seen in Table4.3 - to find an ideal set of frequencies arising from motor operation that may be used for impedance estimation within the motor drive. This was achieved by calculating all of the heterodyne frequencies using one constant stator frequency, one constant switching frequency, one constant injection frequency, and a range of integer harmonics.

Fig4.18 shows the frequency content of the DC-link capacitor current in the range of 0-1kHz whereas Fig4.19 shows the capacitor current for frequency ranges above 1kHz. While the peaks at the exact injection frequencies were found to be high in magnitude at frequencies below 1kHz - as seen in Fig4.18 - the peaks associated with the injected frequencies above 1kHz were found to be very low in magnitude, as seen in Fig4.19 which looks at the frequencies local to the switching frequency ($f_{sw} \pm 233$ and $f_{sw} \pm 487$).

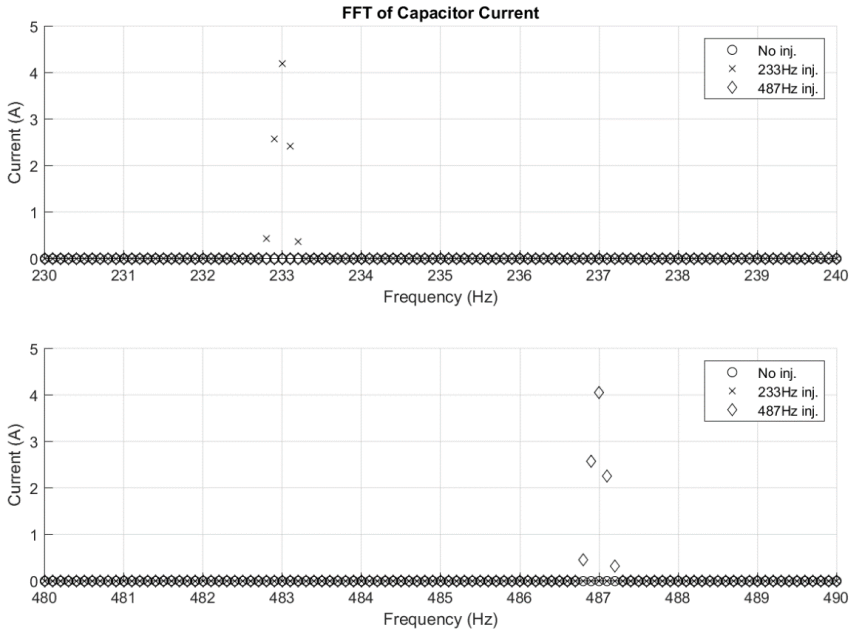


Fig4.18 - FFT of capacitor current below 1kHz where injection signals are present (Test #1)

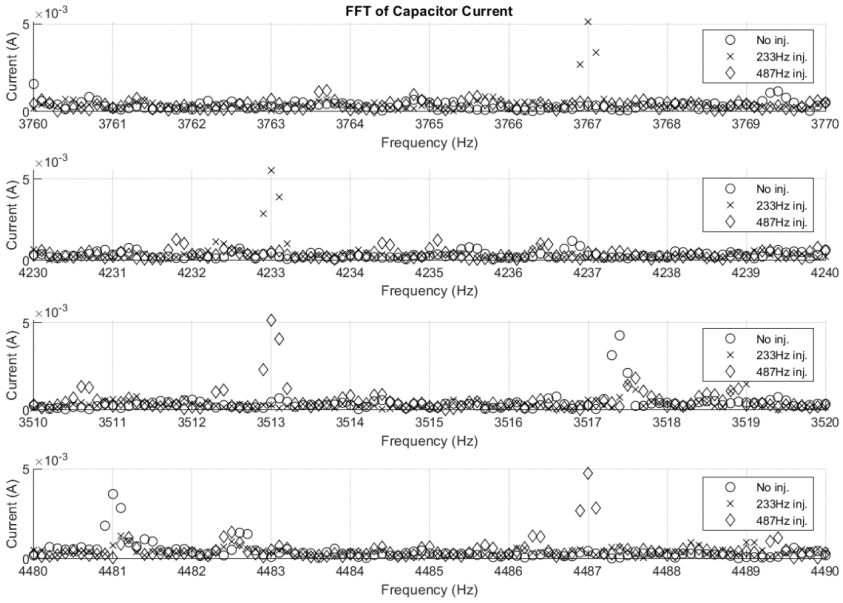


Fig4.19 - FFT of capacitor current around switching frequency where injection signals are present (Test #1)

Fig4.19 shows the presence of injection frequencies local to the switching frequency ($f_{sw} \pm 233$ and $f_{sw} \pm 487$). This figure shows that whilst the signal injection was low in magnitude above 1kHz, it was present as a result of sums and differences of switching frequency and injection frequency, meaning that it was correct to search for these frequencies – the heterodyne frequencies were indeed present in the frequency spectrum, although the problem was that their magnitudes were very low, being in the mA range.

Looking for peaks and impedance estimates at the other identified frequencies started to show the limitations of the lists of identified frequencies, as shown in Fig4.20:

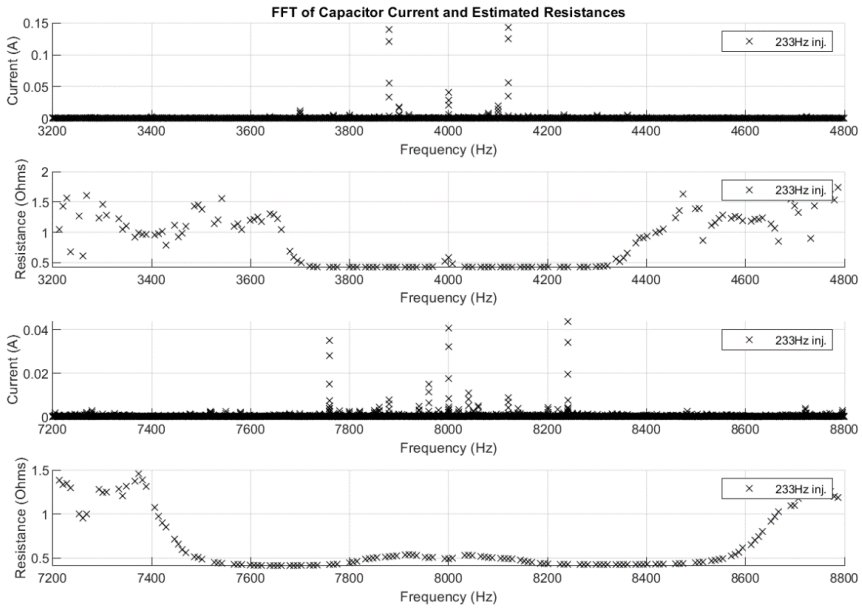


Fig4.20 - FFT of capacitor current and estimated resistances, using a 233Hz injection signal (Test #1)

The first and third graphs of Fig4.20 show the peaks in the frequency domain where an FFT had been applied to the capacitor current.

The first graph shows the frequency response around the first switching harmonic of 4kHz, between 3200Hz and 4800Hz. The third graph shows the frequency response around the second switching harmonic of 8kHz, between 7200Hz and 8800Hz. Peaks are observed at frequencies expressed by (4.1) and (4.2).

The second and last graphs of Fig4.20 show estimates of resistance found via use of the CWT at the frequencies shown in the first and third graphs. An injection signal of 233Hz was used with a switching frequency of 4kHz.

In the second graph of Fig4.20, there is a flat region of estimation of resistance from around 3700Hz and 4300Hz. Also, the last graph of Fig4.20 shows a flat region of estimation of resistance from around 7500Hz to 8500Hz. These frequency ranges correspond to the constraint defined by (4.4). This was predicted earlier in section **4.3.3**.

$$n(f_{sw} - 7f_{stator}) < nf_{sw} < n(f_{sw} + 7f_{stator}) \qquad (4.4)$$

$$n = 1, 2, \dots, maximum\ switching\ harmonic$$

where f_{sw} refers to the switching frequency; and where f_{stat} refers to the stator frequency.

The estimate of resistance deteriorated outside these frequency ranges because there was a reduction in the energy at these frequencies further away from the harmonics of the switching frequency. Other than the stator frequency, the harmonics of the switching frequency dominate in the time-domain waveform. As good estimation depends on use of signals with high energy content and high SNR, it is best in this case to look for a signal close to switching harmonics.

Additionally, observing the frequencies at which there were peaks seen in the FFT response in Fig4.20 turned out not to be useful: the peaks around the switching harmonics may be used to learn about the stator frequency, and by extension about the behaviour of the motor, but Fig4.20 shows that they were not the only useful frequencies for this estimation purpose.

As has been stated, this behaviour was seen to be true as the frequency of the injected signal was varied, as can be seen for the three values of injection frequency shown in Fig4.21. This figure shows that whether there was no injection or there was an injection of 233Hz or 487Hz, the same flat region was observed in the frequency ranges expressed by (4.4).

This did mean that for estimation of resistance at frequencies close to first two harmonics of the switching frequency, the presence of injection signals was unnecessary. However, this did not mean that injection signals were unnecessary for estimation of capacitance, where capacitance would have to be estimated at a much lower frequency.

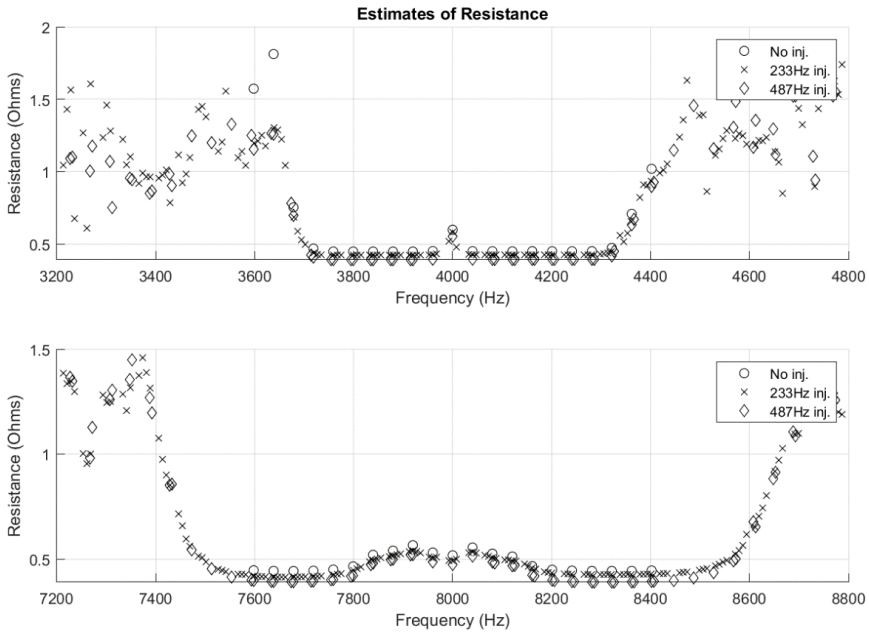


Fig4.21 - Estimated resistances with varied injected signal frequency (Test #1)

Following (4.4) as a rule of thumb, the linear regions in estimated resistance are between 3700Hz and 4300Hz (local to the first switching harmonic) and between 7500Hz and 8500Hz (local to the second switching harmonic).

Although these frequency ranges are approximate, the fact that the frequencies in the flat regions could be used to produce consistent values of estimates means that using (4.3) to produce many frequencies of interest was useful in this experiment, as it was not just the obvious frequencies found via (4.1) and (4.2) which may be used for estimation.

4.4.4 – Conclusions from signal injection tests

The tests presented in this section show that the injection of a signal into the capacitor current caused an effect in the measured DC-link quantities (capacitor voltage and capacitor current). By identifying a list of frequencies as expressed in (4.3) and setting constraints as expressed in (4.4), it is possible to find frequencies local to switching frequency harmonics which may be used for impedance estimation using the CWT. This method worked for a range of frequencies that would not have been immediately identified if looking for peaks in the FFT response of the capacitor current which meant that a wider range of frequencies to use for estimation were identified, meaning that more accurate estimates may be found.

Based on the results in section **4.4**, it was clear at this stage that low-frequency signals may be injected into the DC-link electrolytic capacitors and impedance could be estimated based using these injected signals. As frequencies of 233Hz and 487Hz had been used for injection in this section, further work was continued using these same frequencies.

4.5 – Sensitivity analysis of the identification of capacitor parameters

4.5.1 – Overview

A specific set of "aged" capacitors was chosen to evaluate the proposed test process. It was expected that the impedance of these capacitors would be significantly different from the new pair used previously.

The tests in this section were defined in **4.4.3**.

Before proceeding with the tests, it was necessary to calibrate the impedance for the capacitors to be used.

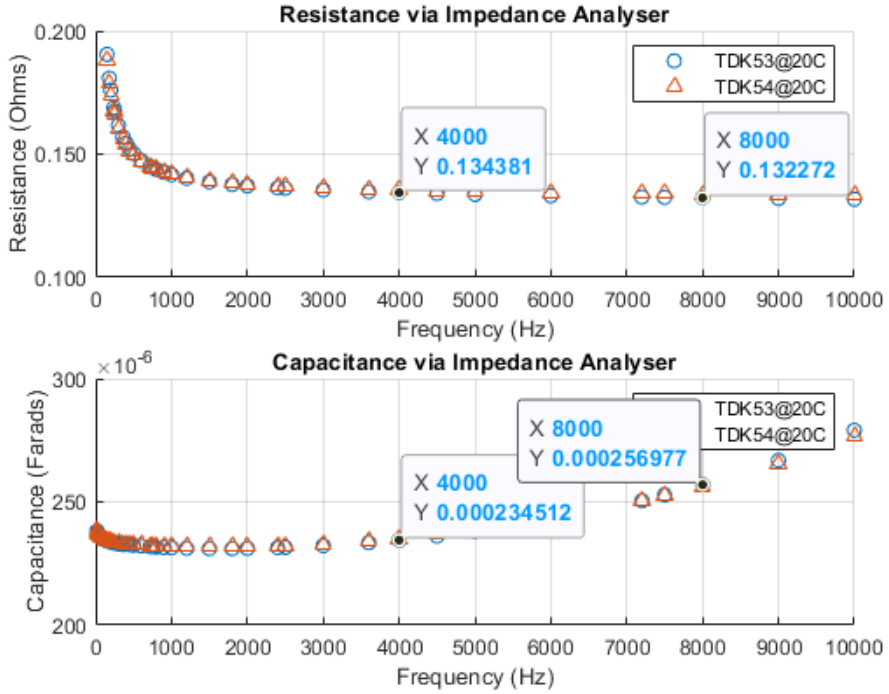


Fig4.22 - Measured impedance for the two test capacitors using the HM8118

Fig4.22 shows measurements taken of the RC values of each capacitor to be used in the sensitivity analysis using a Rohde & Schwarz HM8118 [156]. The measurement device took multiple samples at each frequency in the range of 0Hz and 200kHz, slowly

taking many snapshots of the capacitor response to an injected 1V signal of the set frequency. The measurements were taken at roughly room temperature.

The values of measured impedance at 4kHz and 8kHz are selected specifically in Fig4.22, showing that the capacitors connected in series would give an effective measured resistance of approximately 0.26Ω and an effective capacitance of approximately 117uF, both at 4kHz.

4.5.2 – Results of sensitivity analysis

4.5.2.1 - Test #1: Motor speed 40Hz, switching frequency 4kHz, injection voltage ripple 10Vrms

The first set of measurements were taken using a 40Hz rotor speed, 4kHz switching frequency, and a controlled 10Vrms sine-wave signal. These measurements were taken using a sampling frequency of 50kHz and the calculated values for resistance, capacitance and quality factor are shown in Fig4.23-25. Tables are provided following the graphs to allow for both graphical and numerical comparison of estimates with variations in frequencies.

Fig4.23 shows estimates (using the CWT) of resistance, capacitance, and quality factor where no injection signal was present. Fig4.24 shows estimates where a 233Hz injection signal was present, and Fig4.25 shows estimates where a 487Hz injection signal was present. Cook's distances, previously described in (3.9) as being used essentially as a filter capable of removing "undesirable" datapoints, were calculated to filter out overly influential datapoints from the data.

Using frequencies found using (4.4), resistance was estimated at frequencies around the first two harmonics of switching frequency. Capacitance was estimated at frequencies around the switching frequency and also at the injection frequency. This differs from the frequency ranges described in Fig4.4, where the Bode plot representation of an ideal circuit diagram was used to state that the frequency range between 10kHz and 10MHz would be used for estimating resistance and that the frequency range between 400Hz and 10kHz would be used for estimating reactance.

This change was due to differences observed between the experimental system and the ideal case, where the assumptions made based on the ideal case with Fig4.4 did not take into account the differences in magnitudes of signals at each frequency, whereas clearly the motor current spectrum has much variation in magnitudes of signals across the frequency spectrum. Due to the nature of the pulse-width

modulation (PWM) process, most of the energy of the switching frequencies would be found in the first two harmonics of the switching frequency, with a reduction in energy at each progressive switching harmonic. This means that if resistance should be estimated at "high" frequencies, then the most useful frequencies at which to estimate should be close to the first two switching harmonics.

Table4.4 tabulates the mean filtered estimates shown in Fig4.23 where no injection signal was present.

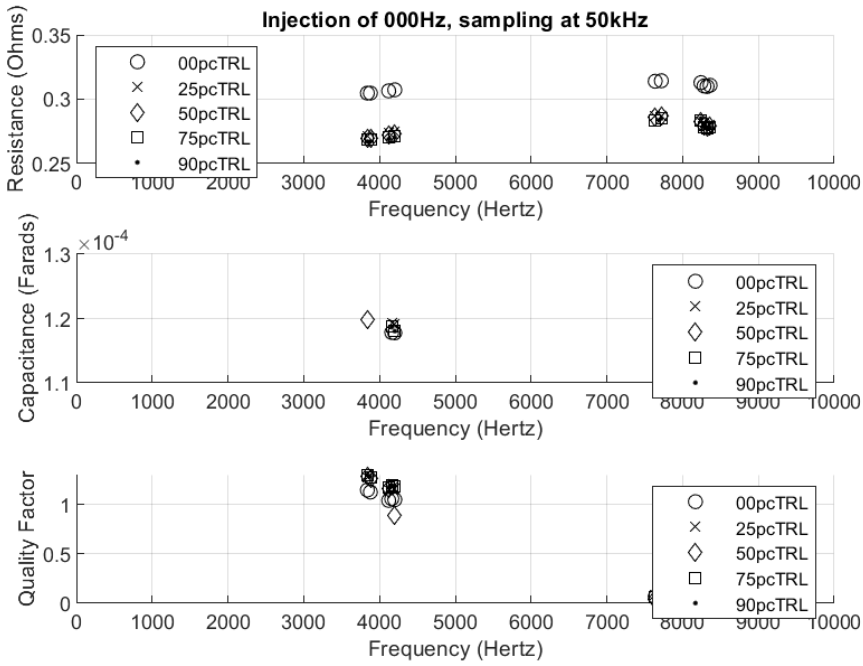


Fig4.23 – 40Hz, 4kHz, no injection, filtered

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	0.3059	0.3120	-	117.8
25% T_L	0.2734	0.2827	-	119.2
50% T_L	0.2710	0.2820	-	119.8
75% T_L	0.2696	0.2809	-	118.4
90% T_L	0.2684	0.2808	-	118.3

Table4.4 – Mean estimates using no injection signal, taken from Fig4.23

The mean values of resistance estimated local to 4kHz were close to the measured value of 0.26Ω, with a difference of approximately 0.04Ω between the estimate at

minimum load and maximum load. The mean values of resistance estimated local to 8kHz were also close to the measured value but had a increased mean error of 0.01Ω, with a difference of approximately 0.03Ω between estimate at minimum load and maximum load.

The mean values of capacitance estimated local to 4kHz did not vary linearly with load, with a difference of approximately 2uF between the largest estimate and the smallest estimate.

Table4.5 tabulates the mean filtered estimates shown in Fig4.24 where a 233Hz injection signal was present.

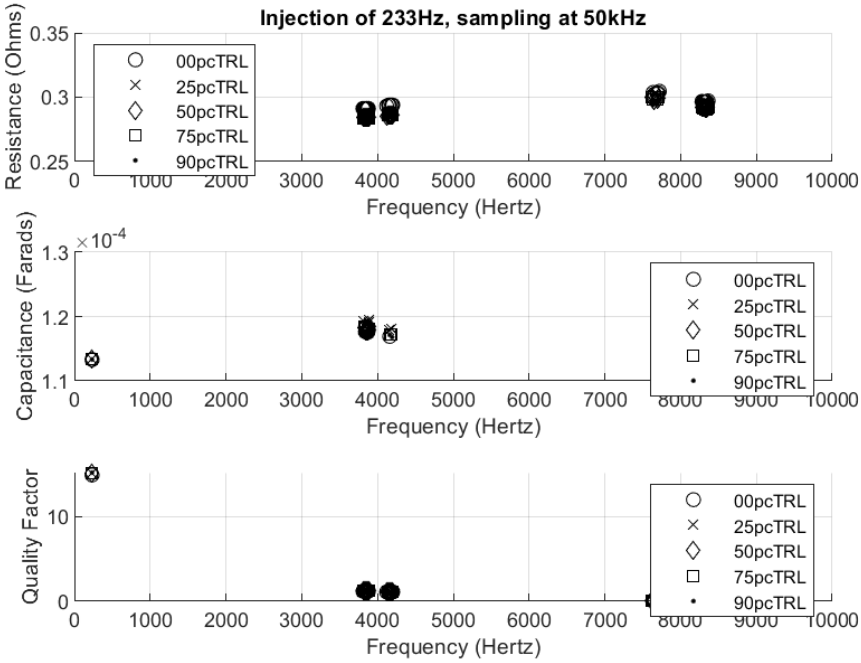


Fig4.24 – 40Hz, 4kHz, 10Vrms, 233Hz injected, filtered

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	0.2924	0.2994	113.3	117.5
25% T_L	0.2871	0.2955	113.3	118.6
50% T_L	0.2850	0.2948	113.3	117.9
75% T_L	0.2843	0.2939	113.3	117.8
90% T_L	0.2829	0.2928	113.3	117.6

Table4.5 – Mean estimates using a 233Hz injection signal, taken from Fig4.24

The mean values of resistance estimated local to 4kHz were close to the measured value of 0.26Ω, with a difference of approximately 0.01Ω between the estimate at minimum load and maximum load. The mean values of resistance estimated local to 8kHz were also close to the measured value but had a increased mean error of 0.01Ω, with a difference of approximately 0.01Ω between estimate at minimum load and maximum load.

The mean values of capacitance estimated local to 4kHz did not vary linearly with load, with a difference of approximately 1.1uF between the largest estimate and the smallest estimate. In contrast, the estimates of capacitance at 233Hz were seen to be load invariant.

Table4.6 tabulates the mean filtered estimates shown in Fig4.25 where a 487Hz injection signal was present.

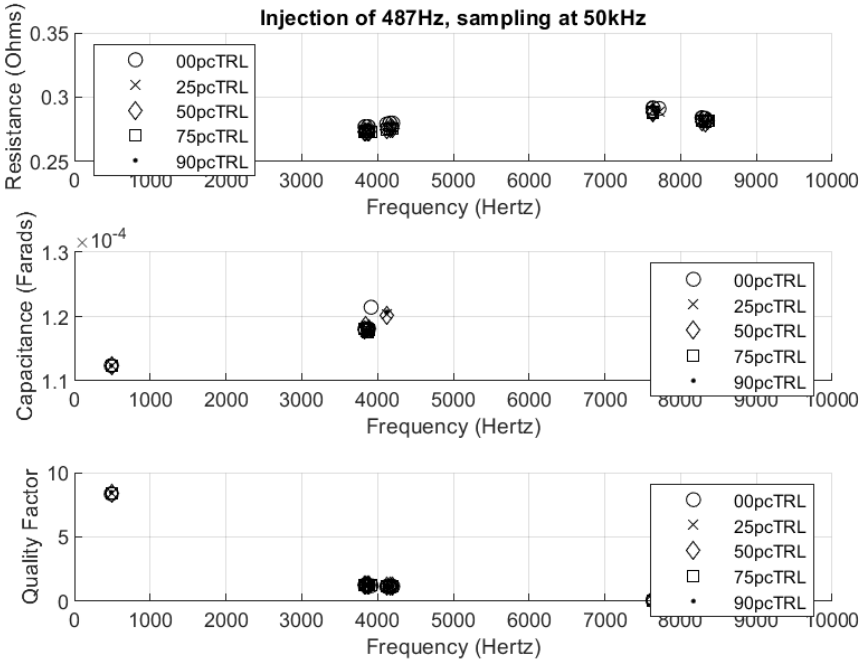


Fig4.25 – 40Hz, 4kHz, 10Vrms, 487Hz injected, filtered

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	0.2784	0.2871	112.4	118.9
25% T_L	0.2757	0.2850	112.4	118.2
50% T_L	0.2744	0.2829	112.3	118.7
75% T_L	0.2739	0.2831	112.3	117.8
90% T_L	0.2718	0.2845	112.4	119.0

Table4.6 – Mean estimates using a 487Hz injection signal, taken from Fig4.25

The mean values of resistance estimated local to 4kHz were close to the measured value of 0.26Ω, with a difference of approximately 0.01Ω between the estimate at minimum load and maximum load. The mean values of resistance estimated local to 8kHz were also close to the measured value but had an increased mean error of 0.01Ω, with a difference of approximately 0.00Ω between estimate at minimum load and maximum load.

The mean values of capacitance estimated local to 4kHz did not vary linearly with load, with a difference of approximately 1.2uF between the largest estimate and the smallest estimate. In contrast, the estimates of capacitance at 487Hz were seen to be load invariant.

Graphically, the estimates of resistance around 4kHz were tightly spaced whereas the estimates around 8kHz were more dispersed. Numerically, the estimates of resistance around 4kHz were both more precise and accurate than the estimates around 8kHz because there was little variation in estimate as load varied and also because the mean resistance estimated was closer to the measured resistance of 0.26Ω, the value which was stated in section **4.5.1**.

Using a higher injection frequency and looking at estimates local to 4kHz and 8kHz resulted in estimates across load levels that were closer to the measured value for resistance, i.e. estimates became more precise. However, increasing the load upon the motor with higher injection frequencies did not increase precision of the estimates of capacitance in the same frequency regions, as they can be seen to vary around the measured value of 117uF as load varies.

The variance of estimates with load at frequencies local to 4kHz and 8kHz can be understood as being due to the peak amplitudes around the switching frequency increasing in magnitude as the amount of current drawn by the motor increases, due to the motor providing more electric torque.

In contrast, the estimates of capacitance observed at 233Hz and 487Hz were seen to be load invariant. This is due to the fact that the signal at the injection frequency is fixed and the amount of current provided by the injection power supply is constant regardless of changes in the motor current as the amount of electric torque provided changes. As a result, if an injection signal were to be provided by an injection power supply in the way shown in Fig4.17, a constant high-amplitude signal could be used to find load invariant estimates of capacitance.

The data presented in Table4.4-6 show that capacitance may be estimated at frequencies local to the harmonics of switching frequency. Estimates may also be found at the injection frequency, and as these estimates had less variation over a range of applied load torques, they may be considered to be more precise. As it is desirable to obtain reliably repeatable results (i.e., low variation), it may be preferable to estimate capacitance based upon specifically the injected frequency instead of at heterodyne frequencies close to the switching harmonics.

The same data shows that an accurate estimate of resistance could be found across the frequency range used, although the precision of the estimate varied with the load applied to the motor.

4.5.2.2 - Test #2: Motor speed 40Hz, switching frequency 6kHz, injection voltage ripple 10Vrms

The second set of measurements were taken using a 40Hz rotor speed, 6kHz switching frequency, and a controlled 10Vrms sine-wave signal. These measurements were taken using a sampling frequency of 50kHz.

The purpose of this test was to try to judge the effect of varying switching frequency, if only by an increase of 2kHz. The drive-under-test provided by the sponsor was capable of switching at multiples of 2kHz between 4kHz and 16kHz. Dependent on the size of the motor at the output of the drive, an appropriate switching frequency would have to be chosen, with lower switching frequencies preferred as the power rating of a motor increases to keep switching losses at an appropriate level. For this reason, the

change in switching frequency was chosen to be small, and so a 6kHz switching frequency was selected.

	$\widehat{R}$ local to 6kHz (Ω)	$\widehat{R}$ local to 12kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 6kHz (uF)
00% T_L	0.3038	0.3533	-	345.9
25% T_L	0.2693	0.3237	-	314.8
50% T_L	0.2681	0.3257	-	305.7
75% T_L	0.2666	0.3354	-	316.5
90% T_L	0.2638	0.3416	-	498.2

Table4.7 – Mean estimates using no injection signal, after filtering

Table4.7 shows that where no injection signal was present, the mean values of resistance estimated local to 6kHz were close to the measured value of 0.26Ω, with a difference of approximately 0.04Ω between the estimate at minimum load and maximum load. The mean values of resistance estimated local to 12kHz were further away from the measured value and had a increased mean error of 0.06Ω.

	$\widehat{R}$ local to 6kHz (Ω)	$\widehat{R}$ local to 12kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 6kHz (uF)
00% T_L	0.2905	0.3402	113.1	465.2
25% T_L	0.2806	0.3333	113.2	432.0
50% T_L	0.2780	0.3400	113.2	415.4
75% T_L	0.2770	0.3429	113.2	352.5
90% T_L	0.2748	0.3518	113.2	422.1

Table4.8 – Mean estimates using a 233Hz injection signal, after filtering

Table4.8 shows that where a 233Hz injection signal was present, the mean values of resistance estimated local to 6kHz were close to the measured value of 0.26Ω, with a difference of approximately 0.02Ω between the estimate at minimum load and maximum load. The mean values of resistance estimated local to 12kHz were further away from the measured value and had a increased mean error of 0.06Ω.

	$\widehat{R}$ local to 6kHz (Ω)	$\widehat{R}$ local to 12kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 6kHz (uF)
00% T_L	0.2738	0.3292	112.2	552.5
25% T_L	0.2703	0.3260	112.2	510.1
50% T_L	0.2689	0.3365	112.2	667.7
75% T_L	0.2676	0.3356	112.2	434.9
90% T_L	0.2660	0.3441	112.2	837.6

Table4.9 – Mean estimates using a 487Hz injection signal, after filtering

Table4.9 shows that where a 487Hz injection signal was present, the mean values of resistance estimated local to 6kHz were close to the measured value of 0.26Ω, with a difference of approximately 0.01Ω between the estimate at minimum load and maximum load. The mean values of resistance estimated local to 12kHz were further away from the measured value and had a increased mean error of 0.07Ω.

4.5.2.3 - Test #3: Motor speed 10Hz, switching frequency 4kHz, injection voltage ripple 10Vrms

The third set of measurements were taken using a 10Hz rotor speed, 4kHz switching frequency, and a controlled 10Vrms sine-wave signal. These measurements were taken using a sampling frequency of 50kHz.

The purpose of this test was to try to judge the effect of varying motor speed. Whereas Test #1 chose a setpoint of 80% of the maximum motor speed, a 20% setpoint was chosen here. The higher speed setpoint was chosen to prevent effects of over-modulation in motor currents, and the lower setpoint was chosen to reduce the complexity of understanding how the DUT achieves zero- and low-speed control.

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	2.3665	0.3073	-	249.1
25% T_L	2.4425	0.2792	-	160.1
50% T_L	2.3920	0.2777	-	164.8
75% T_L	2.2512	0.2779	-	172.0
90% T_L	2.1411	0.2776	-	156.4

Table4.10 – Mean estimates using no injection signal, after filtering

Table4.10 shows that where no injection signal was present, the mean values of resistance estimated local to 4kHz were far from the measured value of 0.26Ω, with a mean error of 2Ω. However, estimates local to 8kHz were far more accurate, with a difference of approximately 0.03Ω between the estimate at minimum load and maximum load and a mean error of 0.01Ω compared to the measured value.

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	2.8402	0.2994	113.1	179.8
25% T_L	2.9020	0.2926	113.2	179.6
50% T_L	2.8642	0.2915	113.2	162.6
75% T_L	2.6665	0.2884	113.2	163.5
90% T_L	2.4920	0.2854	113.2	180.4

Table4.11 – Mean estimates using a 233Hz injection signal, after filtering

Table4.11 shows that where a 233Hz injection signal was present, the mean values of resistance estimated local to 4kHz were still highly inaccurate, with a mean error of 2Ω. Estimates local to 8kHz were still more accurate, with a difference of approximately 0.01Ω between the estimate at minimum load and maximum load and a mean error of 0.03Ω compared to the measured value.

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	2.2619	0.2836	112.3	181.2
25% T_L	2.2251	0.2803	112.3	145.3
50% T_L	2.1087	0.2772	112.2	225.4
75% T_L	2.0313	0.2739	112.2	170.0
90% T_L	1.9948	0.2730	112.3	162.7

Table4.12 – Mean estimates using a 487Hz injection signal, after filtering

Table4.12 shows that where a 487Hz injection signal was present, the mean values of resistance estimated local to 4kHz were still highly inaccurate, with a mean error of 2Ω. Estimates local to 8kHz were still more accurate, with a difference of approximately 0.01Ω between the estimate at minimum load and maximum load and a mean error of 0.01Ω compared to the measured value.

4.5.2.4 - Test #4: Motor speed 40Hz, switching frequency 4kHz, injection voltage ripple 2.5Vrms

The fourth set of measurements were taken using a 40Hz rotor speed, 4kHz switching frequency, and a controlled 2.5Vrms sine-wave signal. These measurements were taken using sampling frequencies of 50kHz.

The purpose of this test was to investigate the effect of reduction of the root-mean-square (RMS) value of the injected signal from 10Vrms to 2.5Vrms.

In the tests in this section, the output voltage of the injection power supply and the impedance across which the voltage is applied have both been kept constant. It was the frequency of the injected current which was altered from first there being no injection present; and then an injection of a 233Hz signal being present; and then an injection of a 487Hz signal.

Between Table4.4-7 and Table4.13-15, there is not much difference between the mean estimates of impedance in each case. This is desirable: ideally, an injection of a signal into a system in order to gauge system response would have little effect. This means that it is beneficial to make use of as low a level of current as possible whilst maintaining the same level of accuracy in system response, as has been observed by reducing the injection voltage from 10Vrms to 2.5Vrms.

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	0.3070	0.3113	-	118.3
25% T_L	0.2806	0.2886	-	117.6
50% T_L	0.2776	0.2836	-	117.2
75% T_L	0.2747	0.2826	-	116.9
90% T_L	0.2729	0.2829	-	119.0

Table4.13 – Mean estimates using no injection signal, after filtering

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	0.2891	0.2947	113.2	117.2
25% T_L	0.2829	0.2899	113.2	116.7
50% T_L	0.2793	0.2854	113.2	117.1
75% T_L	0.2768	0.2818	113.2	116.5
90% T_L	0.2755	0.2834	113.3	117.1

Table4.14 – Mean estimates using a 233Hz injection signal, after filtering

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	0.2828	0.2885	112.1	117.9
25% T_L	0.2795	0.2850	112.1	117.1
50% T_L	0.2765	0.2836	112.1	118.0
75% T_L	0.2748	0.2806	112.1	117.9
90% T_L	0.2738	0.2828	112.2	117.5

Table4.15 – Mean estimates using a 487Hz injection signal, after filtering

4.5.3 - Conclusions from sensitivity analysis tests

Undertaking a sensitivity analysis allowed specific test variables to be varied to observe the effects of controlled variables on estimation behaviour and accuracy.

The following points were observed:

1. Injecting a signal into the motor drive causes peaks to arise in the frequency spectra of the measured capacitor voltage and current which are functions of switching frequency, stator frequency, and injection frequency. This was expressed by (4.3).
2. Because use of (4.3) results in a large number of calculated frequencies to evaluate, filtering was required to remove “undesirable” frequencies from the mean aggregated magnitude estimate. This was achieved by use of statistical filtering through calculating Cook’s distances, as was described in section **3.2.4.4**, (3.10).
3. Frequencies found to be useful for estimation were found close to harmonics of switching frequencies. This was previously expressed by (4.4).

4. It was simpler to aggregate the frequency responses of frequencies found via (4.3) into mean values - as was shown starting with Table4.4 - than to focus on individual frequencies. The aggregation into groups of frequencies close to either the first or second switching harmonic – i.e., “local to” – was achieved using (4.4), where all of the frequencies within the boundaries of the calculated upper and lower limits of (4.4) were used to find a total mean value for the values within the range. This process was used because frequencies at which peaks arise within the range may vary with stator speed and loading [1]. As stator speed instantaneously changes, so do the heterodyne frequencies based on stator speed. By finding aggregates of frequency responses, the dependency of the estimation process on knowledge of the precise stator frequency is removed.
5. The injection frequency itself is very useful for finding estimates of capacitance. The presence of an injection frequency allows for a load-invariant estimate of capacitance to be obtained. This injection frequency is also speed-invariant.
6. Variation of the switching frequency can affect the estimation accuracy, because a motor may attenuate the switching component harmonics and sidebands enough that the useful frequency content is lost.
7. Low-speed can affect the estimation accuracy if making use of the first switching harmonic due to a reduction in magnitudes at the first switching harmonic at low modulation indices.
8. The RMS voltage at the output of the injection power supply may be small as long as a significant current is still being injected. Incidentally, the RMS current injected in Test #1 at 233Hz was approximately 1.6A, and the RMS current injected in Test #4 at 233Hz was approximately 0.4A, where the RMS voltage was reduced by 75% between the two tests. A reduction was not made beyond 75% of the original injection RMS voltage.

4.6 – Variation of capacitor core temperature

4.6.1 – Measurement of capacitor core temperature variations

Previous sections have shown that variation in capacitor core temperature leads to variation in estimated impedances. Therefore, it was necessary to investigate the variations in temperature of the capacitor core if additional signals were injected.

An increase in capacitor core temperature leads to a reduction in the effective series resistance of the capacitor. For this reason, a pair of capacitors identical to those used in this work were procured, where the capacitors had Type-K thermocouples impregnated within them during the manufacturing process. These capacitors were fitted to the inverter and the motor was operated at 40Hz under load, with a switching frequency of 4kHz, with the added task of measuring the capacitor core temperatures. These temperatures were measured using a Pico Technology TC-08 thermocouple data logger [161], using a sample rate of 1s. This sample rate was considered to be acceptable due to the very slow time-constant of the temperature of the capacitor cores.

The motor speed, motor loading, and frequency of injection were adjusted over time according to the routine shown in Table4.16.

Time (s)	Motor speed (Hz)	Load (%)	Freq. of injection (Hz)	Comment
0	0	0	N/A	Drive disabled
40	40	0	N/A	Drive enabled
277	40	0	233	Drive enabled
407	40	0	487	Drive enabled
531	40	0	N/A	Drive enabled
785	40	25	N/A	Drive enabled
933	40	0	N/A	Drive enabled
1182	40	50	N/A	Drive enabled
1310	40	0	N/A	Drive enabled
1557	40	75	N/A	Drive enabled
1685	40	0	N/A	Drive enabled
1936	40	90	N/A	Drive enabled
2071	40	0	N/A	Drive disabled

Table4.16 – Routine used to adjust motor and injection parameters

At the beginning of the test, the drive was powered on and the motor was kept inhibited and unloaded for a period of 40s. The end of this 40s period is marked by the dashed line labelled **(a)** on Fig4.26, where the conditions of the drive and the motor after 40s are shown in the second row of Table4.16. The table shows that after 40s, the unloaded motor was given a reference speed of 40Hz until the time indicated by

the dashed line labelled **(b)**, where a signal of 233Hz was injected until **(c)**, where a signal of 487Hz was injected until **(d)**. At **(d)**, the injection signal was removed and the system was allowed to rest until **(e)**, where cycles of loading and unloading the turning motor was repeated until **(l)**. At **(l)**, the load was removed from the motor and the drive switching was inhibited.

Following the routine set out in Table4.16, Fig4.26 may be understood.

Fig4.26 shows a graph of the measured core temperatures when a test was carried out according to Table4.16. Two lines are plotted: the blue line shows the core temperature of the electrolytic capacitor connected to the upper DC rail, and the orange line shows the core temperature of the electrolytic capacitor connected to the lower DC rail. The ambient temperature was 17°C, and the average temperature of the capacitor cores were low as the capacitors were not enclosed in the drive housing and were forcibly cooled using an external table-top fan.

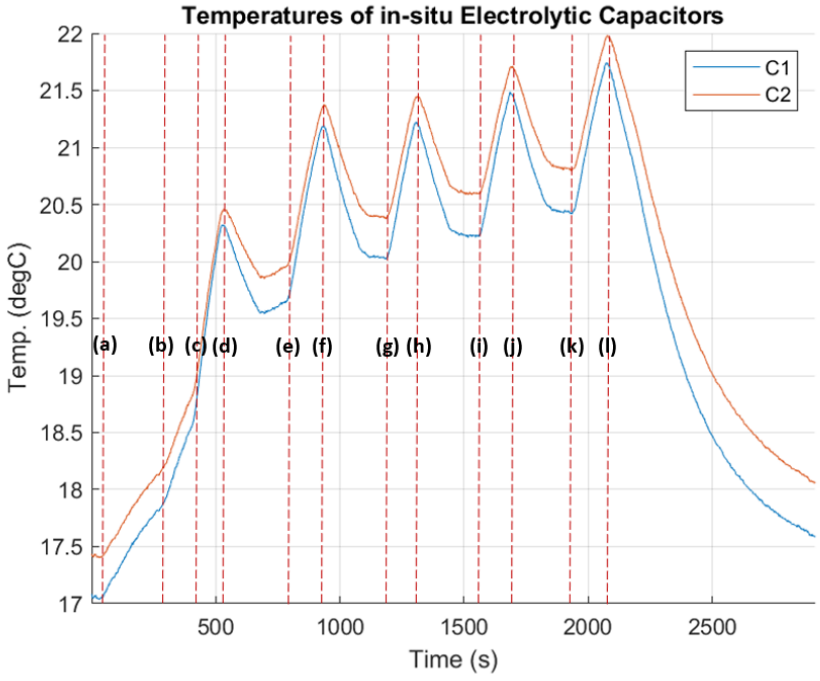


Fig4.26 - Variations in capacitor core temperatures using C1,C2 at an ambient temperature of approximately 17°C

Although it was originally expected that core temperatures would rapidly vary as signals were injected and removed, as well as when motor loading was increased, it was found that it was unnecessary to let the core temperatures settle at final values. Table4.16 shows that injection signals were applied for a maximum of 130s, and the

core temperatures shown in Fig4.26 did not vary much between signals being applied and removed. Similarly, there was little variation in core temperatures as motor loading was increased. This was because the rates of change in core temperatures were quite slow when compared to the time required to sample the capacitor voltage and current.

Rates of changes of capacitor core temperature over time were calculated using Fig4.26, looking for change in capacitor core temperature over periods of time when injection signals were present when the motor was unloaded, and then looking during periods of time when injection signals were not present but the motor was loaded. Table4.17 shows relevant values.

Time period	$\frac{dT_{C_1}}{dt}$ **(°C/s)**	$\frac{dT_{C_2}}{dt}$ **(°C/s)**	**Comment**
a-b	0.0034	0.0031	No injection, 0% load
b-c	0.0057	0.0052	233Hz injection, 0% load
c-d	0.0140	0.0131	487Hz injection, 0% load
e-f	0.0104	0.0095	No injection, 25% load
g-h	0.0092	0.0083	No injection, 50% load
i-j	0.0099	0.0086	No injection, 75% load
k-l	0.0097	0.0085	No injection, 90% load

Table4.17 – Rates of change of capacitor core temperature over time found using Fig4.26

The first three rows of Table4.17 show rates of change in core temperature when the motor was unloaded, first using no injection signal; and then using a 233Hz injection signal; and then using a 487Hz injection signal. The rate of change of temperature increased when an injection signal was applied to the capacitors, and then again when the frequency of the injection was increased. This was due to the increase in current flowing through the capacitors, where the capacitors would then experience higher internal I^2R ohmic power losses during each charge/discharge cycle.

The fourth to seventh rows of Table4.17 show rates of change in core temperature where an injection signal was not present, but instead the loading on the motor was increased. The table shows that the rates of change were fairly consistent for each capacitor core despite the higher load drawing more current.

The only difference between the two sets of rates of change in temperature was that the capacitor connected to the lower rail of the DC-link (C2) had a consistently higher temperature than the capacitor connected to the upper rail (C1).

There were two possible reasons for this: a calibration error in the Type-K thermocouple that was impregnated within the capacitor, or a slight imbalance in the DC voltage shared between C1 and C2.

The calibration error was considered and the test was repeated twice using two new sets of capacitors, but the temperature of the capacitor attached to the lower rail was always higher. An example of the temperatures of the other two sets of capacitors may be seen in Fig4.27, where C1 and C2 were first substituted for C3 and C4 and then C5 and C6 and the temperatures of the core of the lower capacitors (represented by the orange lines) was seen to be higher than the temperatures of the core of the upper capacitors (represented by the blue lines).

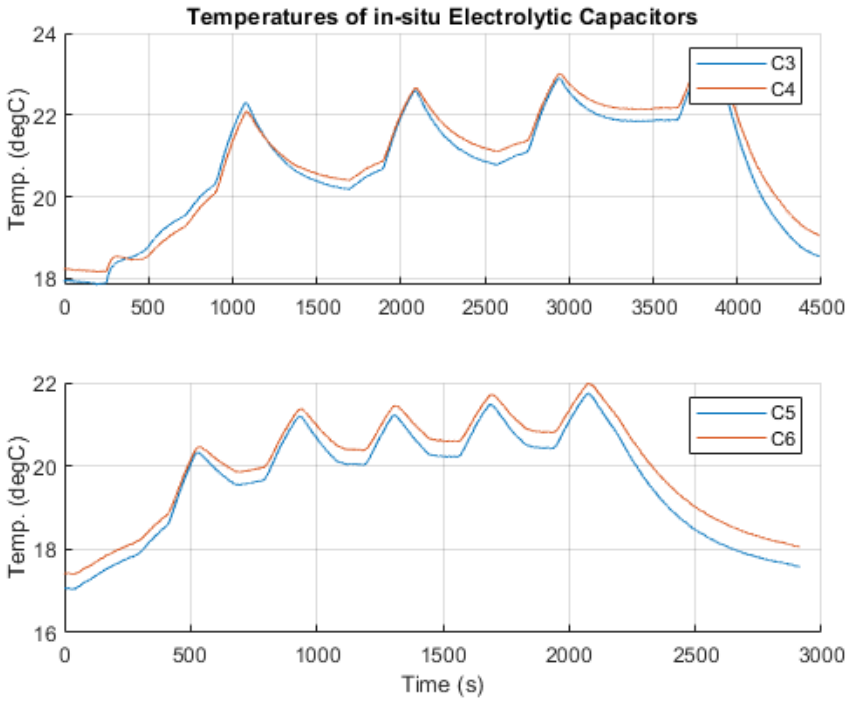


Fig4.27 - Variations in capacitor core temperatures using C3,C4 and C5,C6 at approximately 20°C

As the error in temperatures persisted after varying the capacitors, it was thought that the slight imbalance in the DC voltage shared between the upper and lower capacitor was the cause of the issue. The imbalances would be caused by extra impedances elsewhere in the test drive's circuitry contributing to the effective impedance of the

test electrolytic capacitors in the DC-link. As the project focused on the behaviour of the drive's DC-link and not contributory effects of peripherals such as the transformer which provided 24V to the control unit circuitry from the DC-link, the effect of the rest of the industrial drive's circuitry was not pursued.

As the core temperatures varied very little from room temperature whilst the routine listed in Table4.16 was carried out, it was considered that variation in capacitor core temperatures at an ambient room temperature would not be a probable source of error during impedance estimation.

In this section, the drive was operated whilst the capacitor core temperatures were initially at an ambient room temperature of 17°C. At this ambient temperature, signals were injected into the capacitors and then loading upon the motor was increased, but the changes in core temperatures were not large enough to affect the impedance estimation under the proposed conditions.

4.6.2 – Estimation of impedance at different capacitor core temperatures

Variations in core temperatures were investigated when the ambient temperature was 17°C; when the capacitors were not enclosed in the drive housing; and when the capacitors were forcibly cooled using an external table-top fan.

Realistically, electrolytic capacitors used in an operational drive would experience a higher ambient temperature. Therefore, the way that the drive was operated in section **4.6.1** was not very representative of actual drive operation: it would be best to repeat the test after increasing the ambient temperature of the capacitors.

As was described in section **3.3.3.2**, a N4L PSM1735 [144] was used to take EIS scans of two test thermocouple-impregnated capacitors, where the capacitors were first held at approximately 20°C and then approximately 60°C. Measured values are shown in Fig4.28.

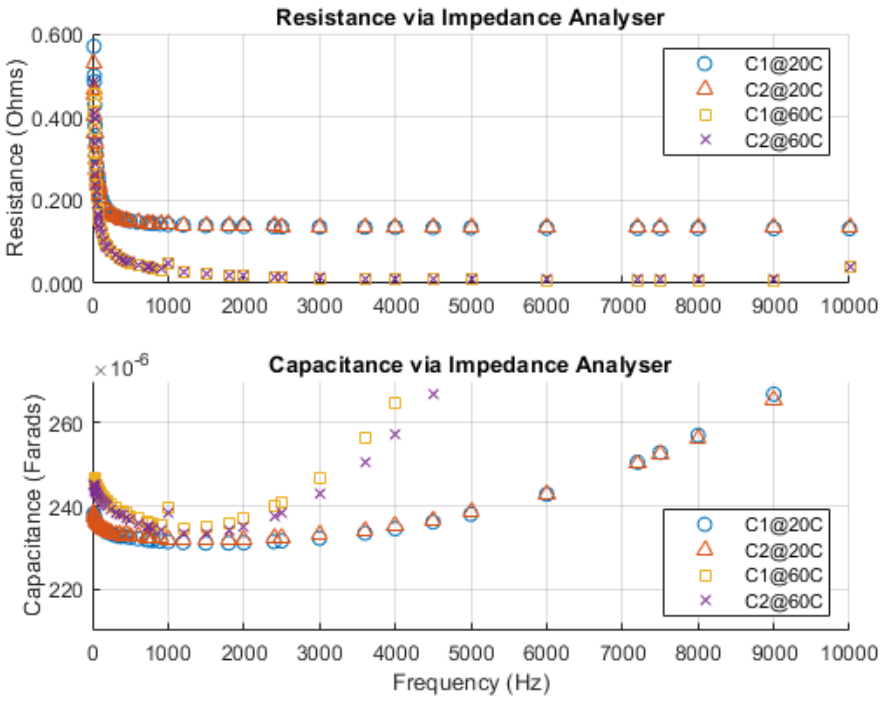


Fig4.28 - Variation of impedance with frequency and temperature

Fig4.28 confirms what was shown previously in section **3.3.3.2**, where an increase in the temperature of the capacitor cores results in a reduction in measured resistance across the frequency range shown, as well as a slight increase in the measured capacitance at the same frequencies.

When the drive is operated normally, with the capacitors enclosed in the drive enclosure, the capacitor cores would be heated in a non-isotropic manner and the core temperature would be approximately 60°C. As it would be difficult to access the drive cabling if the drive PCB were to be packed within the enclosure, some testing was undertaken to find the most efficient way of providing a constant heat source to the capacitors that would result in the core temperatures experiencing an ambient temperature of approximately 60°C, before turning on the motor.

The most efficient manner of heating the capacitors was found to be via using a 2kW Remington D3010 hairdryer [162], and allowing the focused stream of hot air to heat the capacitors until the cores were at an appropriate temperature.

The same thermocouple-impregnated capacitors were used to find estimates of impedance at room temperature and then at a temperature at which the drive would be likely to operate. Heat was provided to the capacitors as depicted in Fig4.29.

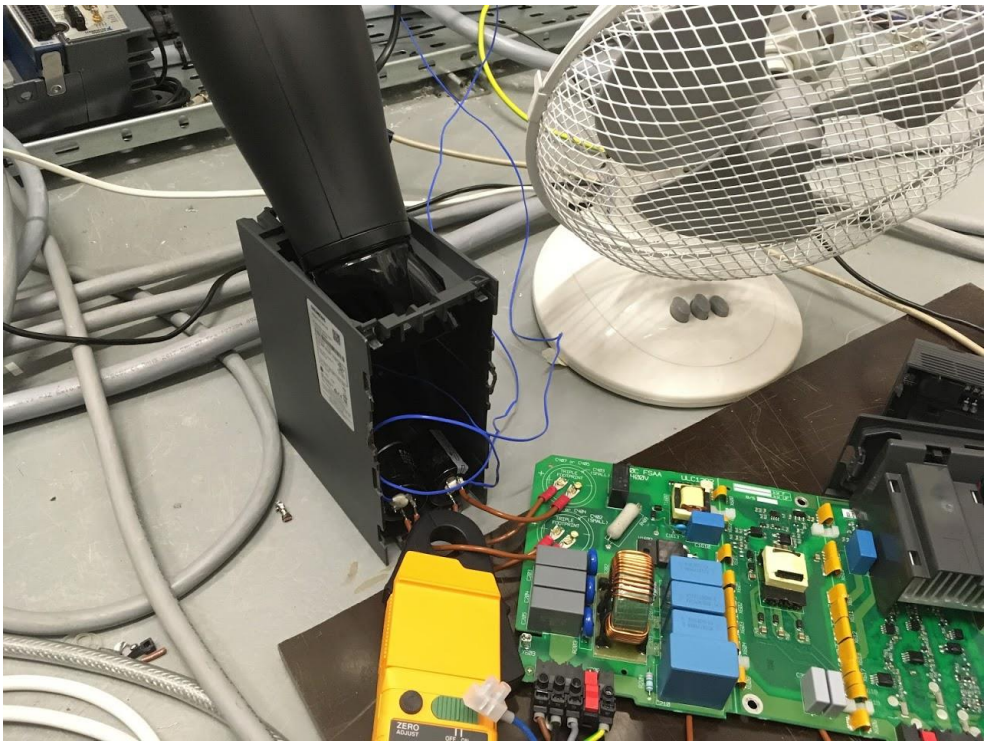


Fig4.29 - Heating of capacitors in operation, using the 2kW Remington D3010 hairdryer

Recorded temperatures are shown in Fig4.30, where three plateaus can be observed: the first plateau was recorded when the motor was operating at 40Hz with 25% of rated load torque applied on it; the second plateau with 50% load; and the third at 75% load. A 90% load was not applied to prevent the loading motor from overheating.

The graph shows that the motor was allowed to turn for at least 14000s, which was roughly four hours: this was to ensure that the capacitor core temperatures were as close to steady-state as possible before recording electrical quantities for estimation purposes.

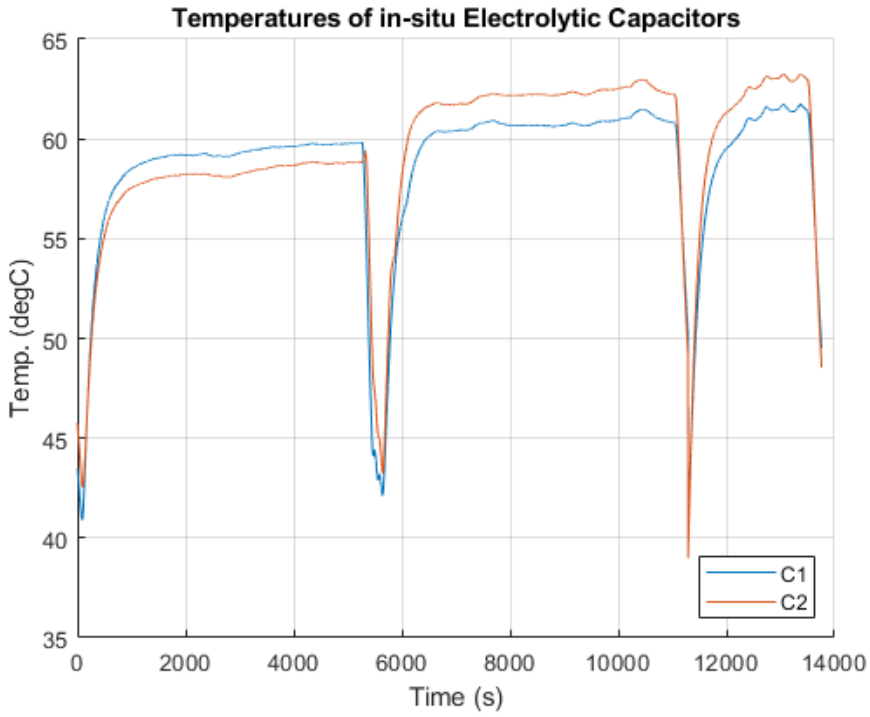


Fig4.30 - Variations in capacitor core temperatures using C1,C2 at approximately 60°C

Table4.18,19 show the mean estimates of impedance found where the motor was rotating at 40Hz; where no injection signal was present; and where measurements were taken when core temperatures were at steady-state: 20°C and 60°C, respectively.

It was found that mean estimates of resistance did decrease by roughly 50% as the ambient temperature around the capacitor casing was heated and the temperatures of the air within the drive enclosure during conventional operation was mimicked. This result agreed with the resistance-frequency curves shown in Fig4.28. The mean estimates of capacitance were also accurate when compared to the capacitance-frequency curves from Fig4.28.

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	0.3059	0.3120	-	117.8
25% T_L	0.2734	0.2827	-	119.2
50% T_L	0.2710	0.2820	-	119.8
75% T_L	0.2696	0.2809	-	118.4

Table4.18 – Mean estimates using no injection signal, with a core temperature of 20°C

	$\widehat{R}$ local to 4kHz (Ω)	$\widehat{R}$ local to 8kHz (Ω)	$\widehat{C}$ at injection frequency (uF)	$\widehat{C}$ local to 4kHz (uF)
00% T_L	0.1402	0.1561	-	133.5
25% T_L	0.1384	0.1548	-	133.7
50% T_L	0.1452	0.1575	-	132.5
75% T_L	0.1435	0.1568	-	133.6

Table4.19 – Mean estimates using no injection signal, with a core temperature of 60°C

4.6.3 - Conclusions on variation in capacitor core temperature

The tests presented in this section show that the impedance of a capacitor in an operational drive varies with the temperature of the capacitor core. Using thermocouple-impregnated capacitors, two tests were undertaken to investigate the effect of the variation of temperature on impedance estimation. It was found that estimation could still take place whether capacitors were used at laboratory temperature or at a temperature that would be expected in an operational drive.

However, as impedances vary with applied voltage and also very clearly vary with temperature, a good estimation scheme would require calibration of resistance and capacitance at both different levels of applied voltages and temperatures in order to account for varying impedance in practice.

As was addressed in section **3.6**, the impedance estimation process relies on consistency of capacitor core temperature, where the effect of external factors may be neglected assuming the capacitor core temperature were to be constant. Fig4.30 showed that the capacitor core temperature was held at approximately 60°C over a period of time whilst applied load torque was varied, and the impedance estimates taken over this time period across the respective frequency ranges were consistent, as was shown in Table4.18,19.

4.7 – Impedance estimation under transient conditions

While the work in section **4.4** looked at impedance estimation via injection of signals into the DUT DC-link during steady-state operation of a loaded motor, it is necessary

to investigate how impedance estimation is affected during dynamic changes in motor speed or loading.

Motors may be used for different applications, such as pump, fan, or paper-mill applications where the motor uses a continuous duty due to the application having an indefinite constant load torque, or conveyors and hoists applications where the motor would use a short-time or periodic intermittent duties due to applications requiring either power either in large bursts or periodically [1].

As was discussed in Chapter 3, a range of frequency transforms may be used to estimate capacitor impedance during steady-state operation of a motor. However, as this section shall show, the CWT may be useful for generating accurate estimates of impedance during transient conditions as opposed to frequency transforms such as the commonly used FFT.

4.7.1 – Overview

To test the effect of transients of speed and load torque upon the impedance estimation process, the working process was adjusted slightly, starting with creating the speed and load profile shown in Fig4.31.

Fig4.31 shows a loading profile where a step change is made in the speed of the motor from 10Hz to 40Hz at 15s, and a step change is made in the load torque imposed upon the motor from 0% to 75% at 35s. The moments of interest are primarily between 10-20s and 30-40s, where the transitions in speed and torque occur.

The measured value of resistance at the side lobes described by (4.1) were approximately 0.3Ω and the measured value of resistance at 233Hz was approximately 0.4Ω. The measured value of capacitance at these frequencies were approximately 117uF.

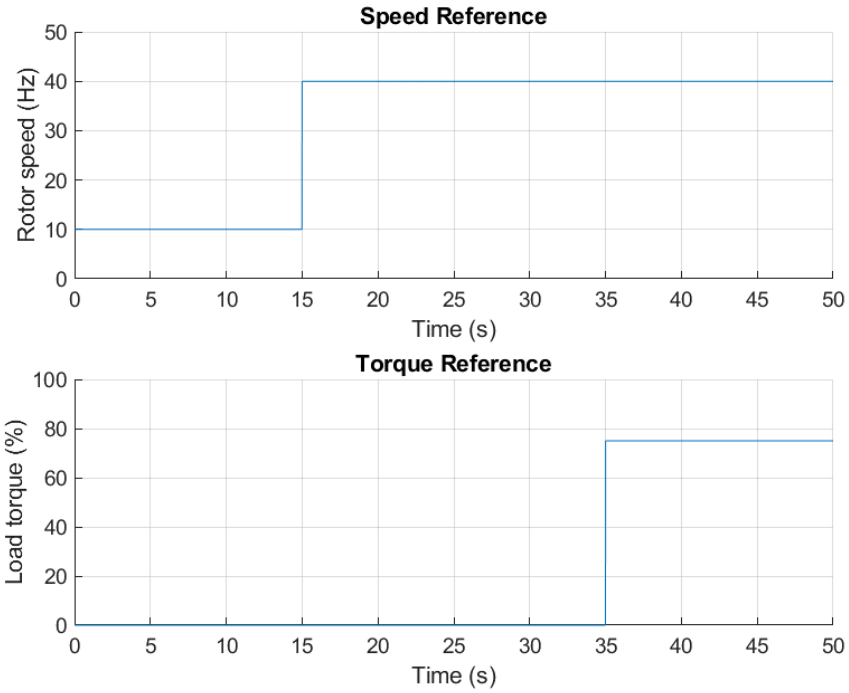


Fig4.31 - Proposed experimental loading profile

4.7.2 – Estimation via FFT

This section considers estimation under transient conditions where measurements are processed using the FFT. Measurements of voltages and currents were taken first when no injection signal was present, and then when a 233Hz injection signal was present.

The loading profile shown in Fig4.31 was emulated using the experimental rig, with measurements being taken for 50s using a sample frequency of 50kHz. Measurements are shown in Fig4.32 and Fig4.33 where the sampling period of 50s was sliced into five equal 10s windows. Each of the 10s were used to find individual sets of estimates. The moments of the two transients are indicated using red dashed lines.

Linking back to the sensitivity analysis in section **4.5**, Fig4.32 shows that when the motor was rotating at 10Hz, the estimates of impedance were high in error when looking at a frequency close to the switching frequency of 4kHz. In this case, the frequency of one of the switching side lobes was used, 4120.3Hz.

When the motor frequency was increased from 10Hz to 40Hz at the moment indicated by the first red dashed line, the average estimates of both resistance and capacitance stepped to values much closer to the measured values. Estimates at this motor frequency continues to be close to the measured values until the time window after

the load was applied to the motor at the moment indicated by the second red dashed line. Loading the motor introduced an error during and immediately after the transient, with the final ten seconds of the test showing that the electrical quantities at this frequency had not entered a steady-state by the time the measurements ended.

Fig4.33 repeats this test with the difference being the presence of a constant 233Hz signal. In contrast to the previous graph which looked at a frequency which was a function of both stator speed and load torque, the frequency monitored here was motor speed and load invariant. This meant that there was a negligible change in estimates during both steady-states and transients.

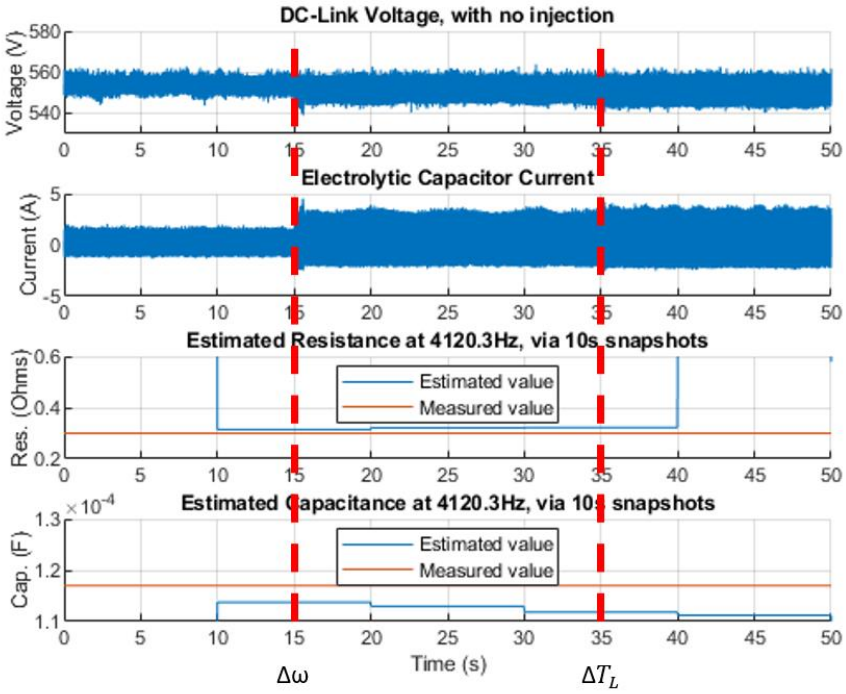


Fig4.32 - Estimation at a switching frequency side-lobe, with no injection, FFT

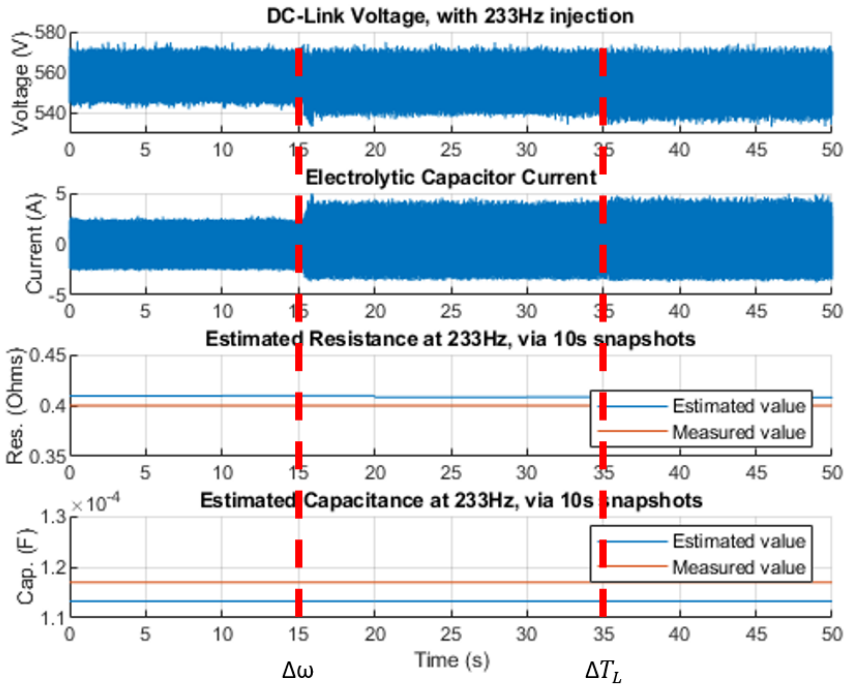


Fig4.33 - Estimation at the injection frequency, FFT

4.7.3 – Estimation via the continuous wavelet transform (CWT)

This section considers estimation under transient conditions where measurements are processed using the CWT. Measurements of voltages and currents were taken first when no injection signal was present, and then when a 233Hz injection signal was present.

The loading profile shown in Fig4.31 was emulated using the experimental rig, with measurements being taken for 50s using a sample frequency of 50kHz. Measurements are shown in Fig4.34 and Fig4.35. The moments of the two transients are indicated using red dashed lines.

The estimates found using the FFT had been found by splitting the 50s of data into five windows of 10s each, and this is because the FFT is a frequency transform where improving granularity in time resolution would either require making use of the STFT or using many smaller windows instead of one large window. In this case, many smaller windows were used. In contrast, estimates found using the CWT may make take advantage of the fact that the CWT is a time-frequency transform and the entire length of the large window may be used.

Fig4.34 shows estimation where no injection signal had been present. Over the length of the sampling window, the estimates showed a large amount of variance - or error -

in the estimates of resistance and capacitance of the DC-link when the motor operated at 10Hz, with the variance reducing as the motor speed was increased to 40Hz.

The reduction in variance in estimates is rapid after the transient begins. As the energy of the peaks at the side lobes of switching frequency are related to the motor speed, it was expected that an increase in the current and voltage magnitudes in this frequency range would cause more accurate estimates to be found if motor speed were to be increased.

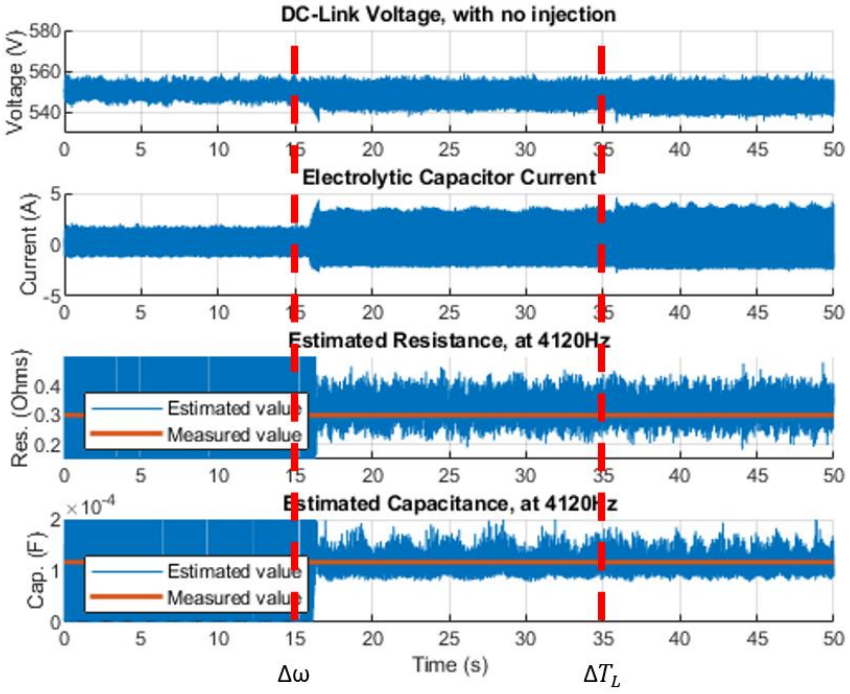


Fig4.34 - Estimation at a switching frequency side-lobe, with no injection, CWT

Fig4.35 shows estimation where a 233Hz injection signal was present. In contrast to Fig4.34, Fig4.35 shows a lot less variance in estimates regardless of motor speed or loading.

The reason behind the difference in variance in estimates due to the injection frequency being independent of the behaviour of the motor behaviour or control, and therefore was effectively load and speed invariant.

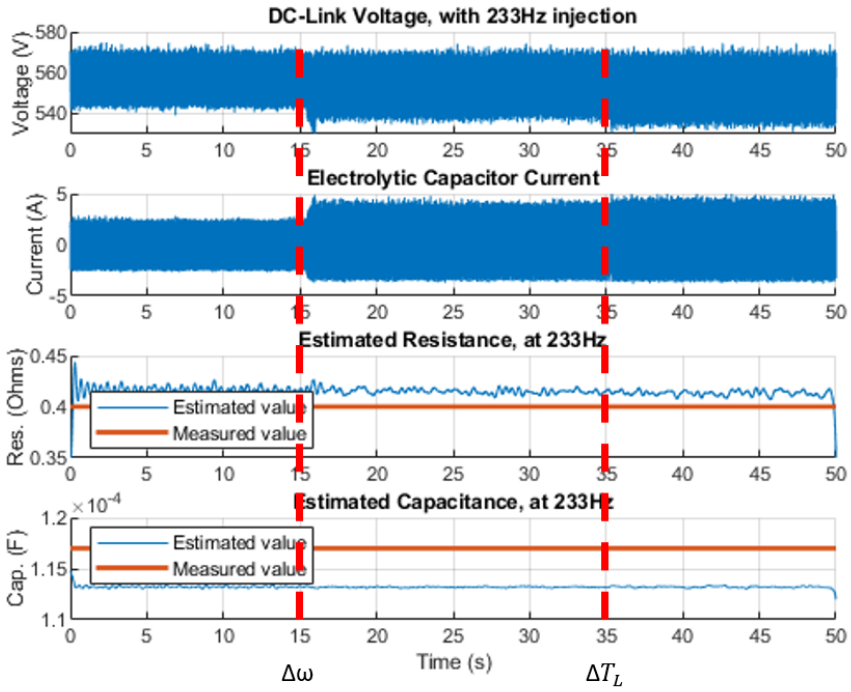


Fig4.35 - Estimation at the injection frequency, CWT

4.7.4 – Conclusions from transient responses tests

These two tests reiterated the findings of the sensitivity analysis, indicating that the use of FFT window "snapshots" for the purpose of impedance estimation can be appropriate. However, an issue would be the need of additional smoothing filters during moments of transients.

Conversely, an advantage of using a time-frequency transform such as the CWT is that a larger sample window may be used instead of many smaller window "snapshots", and so additional smoothing filters would be far less necessary.

4.8 – Comparison of estimates between new and aged capacitors

Previous sections separately looked at impedance estimation and accelerated ageing process. This section will investigate estimation where aged capacitors are used within the test drive.

4.8.1 – Measurement of and estimation of the impedance of "new" capacitors

Using the BioLogic SP-150 [141], EIS was used to measure impedances of two new test capacitors which were labelled TDK53 and TDK54. These measurements were taken when the capacitors had a 10V DC bias voltage and injected with <100mA sine-wave

pulses of variable frequency. The limitation of the DC bias voltage was due to the maximum limit of the potentiostat within the measurement device. Measurements were taken at room temperature.

Measurements are shown in Table4.20 and Table4.21 for a small selection of relevant frequencies.

	TDK53 (mΩ)	**TDK54 (mΩ)**	**Total (mΩ)**
100Hz	188.8	190.1	378.9
233Hz	146.8	147.1	293.9
300Hz	135.5	135.8	271.3
487Hz	120.3	120.8	241.1
4kHz	111.9	112.7	224.6
8kHz	110.4	111.0	221.4

Table4.20 – Measured resistances of two new test capacitors (TDK53,54), using EIS

	TDK53 (uF)	**TDK54 (uF)**	**Total (uF)**
100Hz	224.8	227.6	113.1
233Hz	223.9	226.7	112.7
300Hz	223.2	225.9	112.3
487Hz	223.4	226.1	112.4
4kHz	218.5	220.6	109.8
8kHz	216.2	218.1	108.6

Table4.21 – Measured capacitances of two new test capacitors (TDK53,54), using EIS

Using the same testing methodology described in Test #1 of section **4.5**, the two new test capacitors were connected to the drive and measurements were taken with and without injection signals being present when the motor rotated at 40Hz with first no load applied and then with 90% load applied.

Measurements are shown in Table4.22 and Table4.23 for relevant frequencies.

TL = 00%	000Hz	233Hz	487Hz
<1kHz	x	113.31uF	112.39uF
4kHz	117.81uF	117.51uF	118.69uF
8kHz	x	x	x

TL = 90%	000Hz	233Hz	487Hz
<1kHz	x	113.32u	112.36u
4kHz	118.35uF	117.63u	119.02u
8kHz	x	x	x

Table4.22 – Estimated capacitances of TDK53,54 using 00% and 90% load torque

TL = 00%	000Hz	233Hz	487Hz
<1kHz	x	x	x
4kHz	305.83mΩ	292.43mΩ	278.42mΩ
8kHz	312.04mΩ	299.37mΩ	287.07mΩ

TL = 90%	000Hz	233Hz	487Hz
<1kHz	x	x	x
4kHz	268.37mΩ	282.89mΩ	271.77mΩ
8kHz	280.78mΩ	292.77mΩ	284.46mΩ

Table4.23 – Estimated resistances of TDK53,54 using 00% and 90% load torque

There is an error between the measured and estimated values. This error was partly due to error in the process of measuring and estimating values in Table4.22,23, but was mostly due to the values in Table4.20,21 being obtained when the capacitors were under a much lower DC bias than the capacitors within the drive.

Compared to the EIS measurement process which used a precisely calibrated measurement device that used fixed low levels of voltage and injected current in the mA range, the cores of the capacitors within the drive were much warmer when capacitor electrical quantities were measured; the capacitors had a higher potential across the terminals; and the cores had more current flowing through them. These three reasons affected the frequency response of the capacitor impedances, and therefore the estimated impedances.

When the effect of the increased temperature and increased energy through the capacitors during measurement are accounted for, the measurements shown in Table4.20,21 can be seen to be the ideal values of impedance of the electrolytic capacitors within the drive, whereas the estimates shown in Table4.22,23 can be seen to be truly representative when the same capacitors are placed in an operational drive.

Realistically, the contribution of each capacitor towards the total impedance of the DC-link would not be perfectly divided between each capacitor. This is due to anything from manufacturing imperfections all the way to cumulative degradation due to storage life, or even due to the physics involved in the process of intentionally ageing capacitors.

4.8.2 – Estimation of the impedance of "aged" capacitors

In this section, a batch of capacitors were subjected to the accelerated ageing process described in section **3.5.2**. Ten specific capacitors are used in this section to demonstrate the variation in capacitor impedance after undergoing this ageing process. Pairs of capacitors were connected to the test inverter under the conditions described in Test #1 of section **4.5**. The ten capacitors used were identical to the capacitors used in the previous section, section **4.8.1**, and as they were taken from the same box, it was expected that they would be of the same age and manufacturing imperfections.

As ten capacitors were used in this section and pairs of capacitors had to be used, the total number of unique combinations when using only two capacitors at a time was calculated to be 45, as found via the use of (4.5):

$$\binom{n}{r} = \frac{n!}{(n-r)!r!} \equiv \frac{10!}{(10-2)!2!} = 45 \qquad (4.5)$$

where n refers to the total number of objects in the set; and where r refers to the number of objects to be picked from the set.

Tabulated values of estimated resistances and capacitances for each of these 45 combinations are included in **Appendix D**. An example of one of the tables is shown in Table4.24. Due to the number of unique combinations of pairs of capacitors found using a batch of ten capacitors, only ten capacitors are shown in this section to limit the amount of data presented. This is because an increase in the number of capacitors in the batch would increase the number of combinations, as was expressed by (4.5).

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	116.57u									
TDK33	116.14u	114.76u								
TDK34	116.86u	114.49u	117.99u							
TDK35	115.51u	113.84u	116.96u	116.9u						
TDK36	115.63u	114.02u	116.96u	117.47u	118.43u					
TDK37	115.01u	113.03u	116.44u	117.05u	116.60u	116.64u				
TDK38	x	x	x	x	x	x	x			
TDK39	115.59u	113.67u	117.10u	117.34u	117.38u	118.21u	117.24u	x		
TDK40	x	x	x	x	x	x	x	x	x	

Table4.24 – Example of a table from **Appendix D**: "TableD4.1 – Estimated capacitances with 00% load torque, with an injection of 233Hz"

The tables listed in **Appendix D** may be summarised as follows:

- Section 1 of the appendix (**Dx.1**) has four tables which list estimates of capacitance. Estimates were found at injection frequencies of 233Hz and 487Hz. These estimates were found at both no load and 90% load.
- Section 2 of the appendix (**Dx.2**) has twelve tables where the first six list estimates of capacitance and the next six list estimates of resistance. Estimates were found using no injection frequency, as well as injection frequencies of 233Hz and 487Hz. The frequencies which were used to generate estimates were frequencies identified local to the switching frequency, 4kHz, following (4.4). These estimates were found at both no load and 90% load.
- Section 3 of the appendix (**Dx.3**) has six tables which list estimates of resistance. Estimates were found using no injection frequency, as well as injection frequencies of 233Hz and 487Hz. The frequencies which were used to generate estimates were frequencies identified local to the second harmonic of the switching frequency, 8kHz, following (4.4). These estimates were found at both no load and 90% load.

4.8.3 – Analysis of estimates found using "aged" capacitors

The tables in section 1 of **Appendix D** contain estimates of specifically capacitance found using the aged capacitors. Comparing between the estimates of capacitance of the new and aged capacitors, there was no major difference between the two. For example, the measured values of capacitance listed in Table4.22 were consistent with the estimated values of capacitance listed in Table4.24: this meant that capacitances estimated using injection frequencies were very accurate.

The tables in section 2 of **Appendix D** contain estimates of both resistance and capacitance found using the aged capacitors. The frequency range in this section was around the switching frequency of 4kHz, and again the estimated values capacitances were accurate to the measured values of capacitance. However, the estimated values of resistance were up to four times the values of the measured resistances.

The tables in section 3 of **Appendix D** contain estimates of resistance found using the aged capacitors. Comparing between the estimates of resistance of the new and aged capacitors showed that the increased resistances seen in section 2 were seen at both the first and second switching harmonics. This indicated that the accelerated ageing process described in section **3.5.2** was successful, as the equivalent series resistance had been increased at two of the frequency ranges which were identified by (4.4).

Crucially, the increased electrical power loss exacerbate the thermal power losses, which would then mean that the estimation scheme would be better able to identify the increased equivalent series resistance of the capacitors as the capacitors get progressively aged.

Overall, the data in the tables in the appendix show that the ageing process was successful in increasing the effective resistance of the capacitor pairs from the measurements and estimates of the new capacitors, sometimes by only a few percentage points and sometimes by up to 300%. Examples of these may be seen by comparing the values of the new capacitors with TDK35,36 in TableD4.15 and TDK32,33 in TableD4.11, where the values are 277.13mΩ and 1173.90mΩ local to 4kHz, respectively.

The same data shows that there were negligible changes in the capacitance after ageing, apart from with one particular pair of capacitors, TDK31,38. The values of this pair are highlighted in orange in the tables in the appendix, and are also listed here in Table4.25.

TL = 00%	000Hz	233Hz	487Hz
<1kHz	x	x	x
4kHz	94.51uF	x	x
8kHz	x	x	x

TL = 00%	000Hz	233Hz	487Hz
<1kHz	x	x	x
4kHz	322.22mΩ	x	x
8kHz	307.81mΩ	x	x

Table4.25 – Estimated impedances of TDK31,38 using 00% load torque and where no injection signal was present

This specific pair of capacitors resulted in an explosive failure of TDK31 shortly after one 50kHz sample of currents and voltages were taken whilst the unloaded motor was rotating at 40Hz.

With this specific pair of capacitors, the estimated resistance was similar to the measured and estimated values of resistance found using the new pair of capacitors, with the error between the measurements of the new pair and aged pair being approximately 50%, which is far less than the 300% increase in resistance observed using other pairs of capacitors. This indicated that the change in resistance was the cause of the capacitor failure.

However, the estimated capacitance was seen to be approximately 18% smaller than the measured and estimated values of capacitance found using the new pair of

capacitors, which is a lot more than the negligible difference in capacitance observed using other pairs of capacitors. All else being equal, this indicated that the change in capacitance was the cause of the capacitor failure.

The 10s waveforms recorded for the capacitor pair TDK31,38 were examined for any obvious differences between them and other waveforms recorded for the pairs of TDK31 and 32-37. For reference, the estimated impedances of the pairs of capacitors are listed in Table 4.26; also listed are the errors of the estimated resistances and capacitances, which were calculated relative to the measured values of TDK53,54.

The mean values of measured voltages and measured currents are listed in Table4.27. The relevant values for capacitor pair TDK53,54 are also included to allow for comparison of values of pairs of aged capacitors with values of a pair of new capacitors.

The key point that this table shows is that the capacitor pair which resulted in a failure had both a reduced capacitance compared to the other capacitor pairs, as well as drew a lot more current compared to the others immediately before failure. This may be seen by comparing the mean currents through the capacitors.

	$\widehat{C}$ at injection frequency (uF)	Abs. error rel. to measured TDK53,54 (%)	$\widehat{C}$ local to 4kHz (uF)	Abs. error rel. to measured TDK53,54 (%)
TDK31,32	-	-	112.59	2.5
TDK31,33	-	-	117.83	7.3
TDK31,34	-	-	119.24	8.6
TDK31,35	-	-	116.88	6.4
TDK31,36	-	-	114.57	4.3
TDK31,37	-	-	117.46	7.0
TDK31,38	-	-	94.51	13.9
TDK31,39	-	-	117.04	6.6
TDK53,54	-	-	117.81	7.3
	$\widehat{R}$ local to 4kHz (mΩ)	Abs. error rel. to measured TDK53,54 (%)	$\widehat{R}$ local to 8kHz (mΩ)	Abs. error rel. to measured TDK53,54 (%)
TDK31,32	749.60	233.7	738.01	233.3
TDK31,33	627.60	179.4	620.86	180.4
TDK31,34	579.00	157.8	569.53	157.2
TDK31,35	567.00	152.4	561.00	153.4
TDK31,36	689.64	207.1	681.44	207.8
TDK31,37	647.58	188.3	641.24	189.6
TDK31,38	322.22	43.5	307.81	39.0
TDK31,39	692.54	208.3	683.65	208.8
TDK53,54	305.83	36.2	312.04	40.9

Table4.26 – Estimated impedances of a batch of pairs, using 00% load torque

	RMS Voltage (V)	RMS Current (A)	Power (VA)
TDK31,32	549.7780	1.0032	551.5487
TDK31,33	553.0088	1.0058	556.2150
TDK31,34	558.7250	1.0276	574.1567
TDK31,35	557.0635	1.0216	569.1115
TDK31,36	550.2580	1.0093	555.3646
TDK31,37	552.5549	1.0076	556.7581
TDK31,38	555.0200	1.1315	628.0211
TDK31,39	557.7973	1.0103	563.5504
TDK53,54	550.1582	0.9606	528.4560

Table4.27 – Averages of measured voltages, currents, and power, linked to Fig4.36

The mean power, measured in volt-amps, is shown in both this table as well as in Fig4.36.

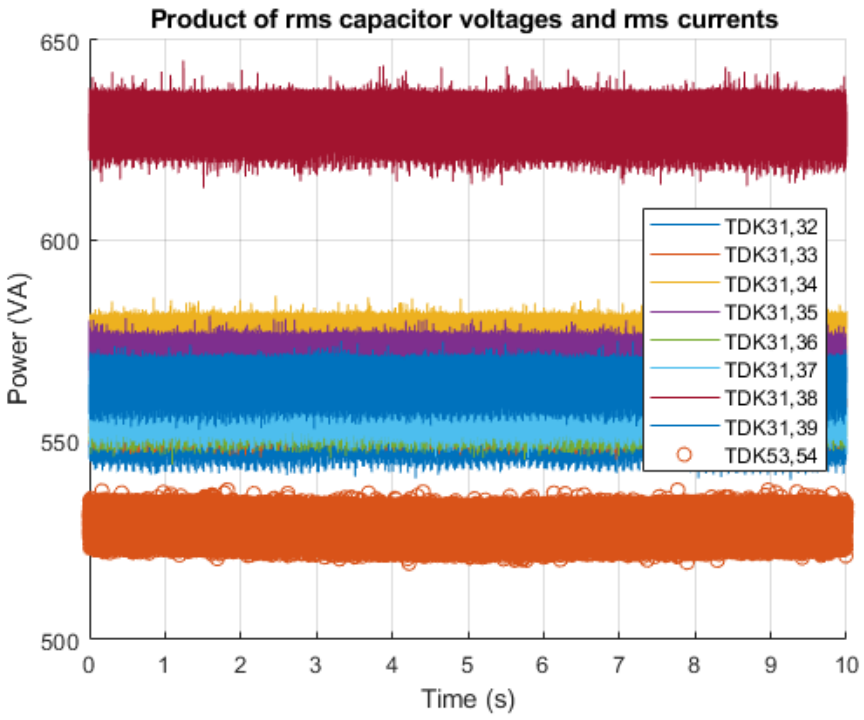


Fig4.36 - Power as a function of variable voltage and mean current, linked to Table4.27

Fig4.36 shows the product of RMS voltages and RMS currents taken from Table4.27. The unaged capacitors TDK53,54 have an average power throughput of approximately 530VA, whereas most of the aged capacitors have an average power throughput of

approximately 560VA. However, TDK31,38 was found to have a much larger power throughput, at approximately 630VA.

There were no failures when 300% increases in resistance were observed. The singular failure happened when a decrease in capacitance of more than 10% was observed. This suggests that increases in resistance would only result in increased thermal losses to the capacitor, instead of immediate failure. These increases may decrease the lifetime of the capacitor due to increased thermal cycling, but the more immediate cause of failure would be reduction in nominal capacitance provided by the component to an operational inverter.

The impedances of the new capacitor pair may be compared with the impedances of the capacitor pairs where the highest estimate of resistance was observed, as well as where the lowest estimate of capacitance was observed. This is shown in Fig4.37.

Fig4.37 shows the Bode plot generated from data of three sets of capacitors: TDK53,54 is used to show the “original”, frequency response of the DC-link using unaged capacitors; TDK32,33 is used to show the frequency response of a DC-link where aged capacitors result in the largest estimated resistance found in the tables in the appendix; and TDK31,38 is plotted to show the frequency response of a DC-link where aged capacitors result in the smallest estimated capacitance found in the same tables.

Contrasting Fig4.37 with the ideal Bode plot at the start of this chapter, Fig4.4, it can be seen that frequency regions were identified accurately for separately estimating resistance and capacitance.

Although it was previously stated that estimates of resistance should be made in the range of 10kHz to 10MHz, Fig4.37 shows that variation in the magnitude gain can be seen starting from 600Hz to at least 10kHz, meaning estimation may take place at lower frequencies.

Similarly, the previously stated frequency region for estimating capacitance was 400Hz to 10kHz, whereas Fig4.37 shows that as capacitor impedance varies, variations in phase may be observed as low as 300Hz. However, Fig4.37 also shows that as frequency decreases past the resonant frequency, phase changes from negative to positive, meaning that the effect of a reactor upon the DC-link would become more and more dominant at these frequencies, therefore potentially affecting accuracy of estimation.

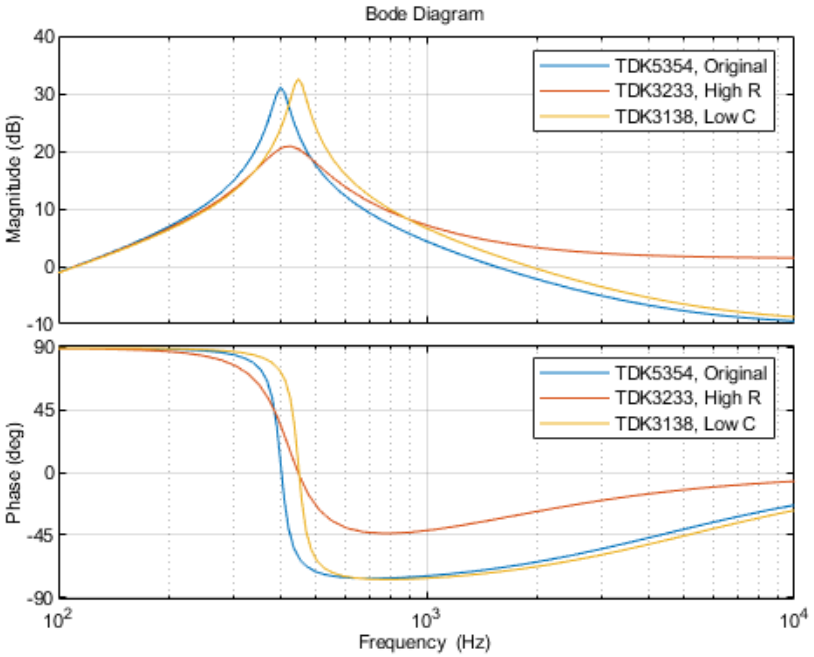


Fig4.37 - Bode plot comparison showing frequency responses of different capacitor pairs

4.8.4 – Conclusions from estimation using "aged" capacitors

This section compared impedance estimation where a pair of new capacitors were connected to the test inverter with estimation where the new capacitors were replaced with pairs of aged capacitors.

It was found that the ageing process was successful in increasing the equivalent series resistance of the capacitors, up to 300% of the resistance of the new capacitors. However, this did not result in a failure when the drive and the attached loaded motor were operated using the capacitor pairs where resistance was increased to that amount. Only one failure was achieved, and this was where the estimated capacitance of a capacitor pair was reduced by approximately 18% from the estimated capacitance of the new capacitor pair.

Data was provided to demonstrate how the amount of current through the failed capacitor increased so much compared to the other test capacitors, and a Bode plot was generated to compare against and validate the frequency regions chosen for separate estimates of resistance and capacitance at the start of the chapter.

4.9 - Summary

This chapter has investigated the feasibility of identifying capacitor impedance during drive operation for the purpose of detecting changes due to degradation. Impedance estimation using the DC-link electrolytic capacitors of an operational drive was investigated through a variety of methods.

As the previous chapter had discussed electrical and thermal models of capacitors, this chapter looked at placing test capacitors within an operational drive and operating the attached motor under a range of conditions of load torques, injection frequencies, switching frequencies, motor frequencies, and capacitor core temperatures.

The purpose of this range of tests was to verify that the equivalent electrical model of the capacitor, which was described in the previous chapter, could be identified using mathematical transforms applied to electrical quantities which vary as motor operation varies.

Using the particular test drive which was supplied by the project sponsor as well as a simple method which was developed in this chapter, it was shown that the equivalent electrical model of a capacitor may be identified under a range of conditions. Where it was not possible to identify the equivalent model satisfactorily, investigations were undertaken to find acceptable reasons for why identification was not possible.

A comparison study was undertaken using a batch of aged capacitors where the purpose was to look at the limits of using capacitors in an operational drive where the capacitors had been subjected to the accelerated ageing process described in the previous chapter. It was found that the equivalent series resistance of a batch of capacitors could be increased by a wide margin but the capacitors would still achieve their function of providing power to a loaded rotating motor. One singular failure was recorded where the capacitance of a pair of capacitors was seen to decrease by approximately 18% before the drive failed.

Throughout this chapter, signals of frequencies 233Hz and 487Hz were separately injected into the capacitor current and used to identify estimates of capacitance and resistance. As part of the comparison study, aged capacitors were used in the drive. From this study, the Bode plots Fig4.4 and Fig4.37 were compared, and it was stated that the frequency ranges shown in Fig4.4 for estimating capacitance and resistance could be reduced to consider only frequencies below 10kHz.

As the AC injection power supply unit was limited to a maximum injection frequency of 500Hz, these two specific frequencies were initially used as examples of prime numbers which may be injected into a drive in an ideal case. Fig4.37 showed that these frequencies actually happened to be appropriate choices as changes in the magnitude gain and phase were observed close to 500Hz as capacitor resistance and capacitance changed through the ageing process.

At the start of this chapter, the frequencies of 233Hz and 487Hz were used for injection and it had been expected that frequency peaks arising from interactions between harmonics of switching frequency and these injection frequencies may be used for estimation purposes. At the end of this chapter, section **4.8.3** demonstrated that aged capacitors may have their resistances and capacitances estimated at lower frequencies than expected. As a result, the conclusion could be drawn that since the estimation bandwidth was seen to be reduced, perhaps also the value of the injection frequencies may be reduced closer to a DC signal.

Some shortcomings were observed in this chapter, such as the use of the external power supply and use of DC-link current measurement. Use of the external power supply is impractical, and measuring the current of the DC-link is unlikely. As a result, work was undertaken as described in the next chapter, where an alternative approach to measuring DC-link currents was explored.

Chapter 5 – DC-Link Impedance Estimation via Motor Speed Perturbation

5.1 – Introduction

Chapter 4 demonstrated that the real and imaginary components of the DC-link impedance could be identified by injecting specific frequencies in the DC-link and measuring DC-link voltage and current through the electrolytic capacitors. The specific frequencies investigated were in the region 0-500Hz (limited by the injection device) but the sidebands created by interaction with the switching frequency and harmonics were in the regions indicated by the Bode plot shown in Fig4.4 to be suitable for capacitance and resistance identification.

This chapter will explore using the motor itself as the injection source, replacing the external AC power supply unit (PSU) of Chapter 4. It will also remove the need for the DC-link capacitor current measurement. This leads to two further issues which must be addressed:

1) The influence of the grid-connected impedance on the amount of signal injected into the DC-link, and the amount which goes to the grid directly.
2) The sample frequency of the commercial drive used in this work.

The chapter is therefore laid out into five sections as follows:

- Section **5.2** – explains the concept of using the motor to create the injection, and the mechanism for identifying the capacitor current. This includes a discussion of the influence of the grid-side reactance (DC reactor).
- Section **5.3** – presents simulation data to show that the injection frequencies used in Chapter 4 can be used with the motor providing the injection, taking into account a realistic grid-side impedance.
- Section **5.4** – explains the influence of converter sample frequency on the ability to inject a signal. A lower injection frequency is therefore employed, which means an unrealistically larger grid-side reactance must be used to ensure the capacitor current estimation works well. Simulations show the feasibility of this approach.
- Section **5.5** – attempts to experimentally validate the approach to capacitor impedance estimation. The inverter current is impossible to access, so it is reconstructed using the estimated rectifier current and measured capacitor current. The results show that the capacitance can be measured well, but there are issues with the resistance.

- Section **5.6** – discusses these results and draws conclusions to the chapter.

5.2 – Motor speed perturbation

Chapter 4 had previously looked at making use of an external AC PSU to inject controlled signals directly into the DC-link electrolytic capacitors, where the capacitor current would also be directly measured. Chapter 4 had then gone on to conclude that the developed method would be impractical due to the reliance on an external PSU, as well as on the reliance on measurement of the current through the electrolytic capacitors. As a result, an alternative method is required if making use of a drive outside of laboratory conditions.

5.2.1 – Basic concept

Fig5.1 shows the circuit diagram of the G120C motor-drive [113], where this drive was used in this project as the drive under test. Relevant values are provided in Table5.1. Power flows from the three-phase voltage source at the left of the diagram to the motor at the right of the diagram. Considering the influence of the motor transients on the transients in the DC-link currents, a constant controlled ripple injection signal may be overlaid onto the reference motor stator quadrature current to excite a ripple signal in the motor and therefore in the DC-link currents.

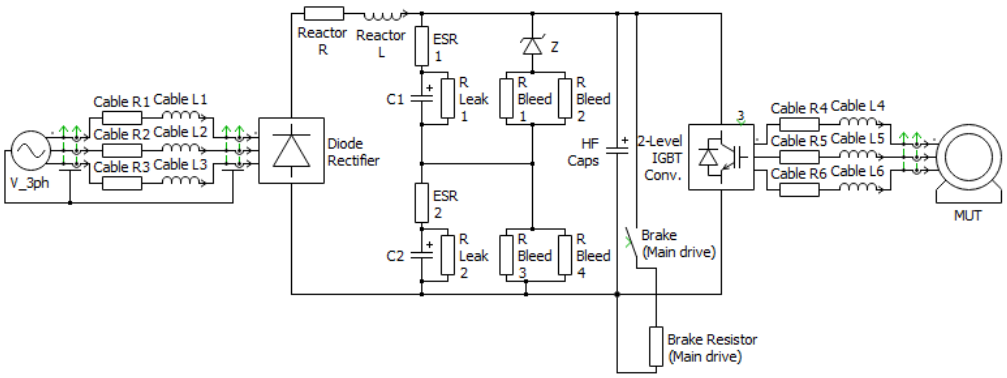


Fig5.1 - Circuit diagram of the G120C motor-drive, with the attached motor

C1, 2	Nominally 270uF, measured via EIS
ESR1, 2	Nominally 160mΩ, measured via EIS
Rleak1, 2	100kΩ
Rbleed1, 2, 3, 4	300kΩ
HF Caps	111nF
Reactor R	100mΩ
Reactor L	1mH

Table5.1 – Component values used in Fig5.1

In drives such as the G120C, direct and quadrature stator currents can be controlled using current feedback to maintain separate flux control and torque control. If the direct stator current is used solely to maintain the rated motor flux, the quadrature stator current may be adjusted according to equation (5.1) to excite a ripple of known frequency in the motor speed, motor electric torque, stator currents, and also the DC-link currents.

The equation to describe the reference stator quadrature current with an overlaid ripple signal would be as follows:

$$i^*{}_{sq_{amended}} = i^*{}_{sq} + \mathrm{A}\sin(\omega_{inj}t) \tag{5.1}$$

where $i^*{}_{sq_{amended}}$ refers to the reference stator quadrature current with the overlaid perturbation; where $i^*{}_{sq}$ refers to the reference stator quadrature current; and where ω_{inj} refers to the angular frequency of the ripple/perturbation/injection/disturbance.

Direct and quadrature quantities are calculated by mathematically transforming three-phase AC vectors to two orthogonal DC vectors, where the DC vectors rotate at a specified angular frequency [1].

To test the idea of injecting a controlled disturbance signal into the quadrature current for later measurement in the motor and DC-link currents, a preliminary simulation was ran. A sine wave was injected into the reference quadrature current of a motor whilst motor speed and currents were controlled using feedback. The simulation injected a signal for 10s whilst the motor loading was constant. The simulated stator, injection, and switching frequencies were as follows, making use of an arbitrary stator speed:

$$f_{st} = 21Hz;\ f_{inj} = 233Hz;\ A = 4;\ f_{sw} = 4kHz \tag{5.2}$$

Fig5.2 shows 0.1s of this 10s window. The first graph in Fig5.2 shows the measured stator direct and quadrature currents where the ripple is very evident in the quadrature current. Due to the mathematical relation between the two currents, the ripple is also present in the direct current but at a much lower magnitude. The second graph shows the three phases of motor stator current, where a certain ripple frequency is also present in the current waveforms. The third graph shows the DC-link capacitor and inverter currents, where a certain ripple frequency is again present.

Fig5.3 and Fig5.4 show FFT frequency spectra based on the currents in Fig5.2. Specifically, Fig5.3 shows frequencies between 0Hz and 300Hz for the purpose of showing the distribution of frequencies around the injection frequency, and Fig5.4 shows frequencies close to the switching frequency for the purpose of showing the distribution of frequencies around the switching frequency.

The magnitudes at key frequencies in Fig5.3 and Fig5.4 are summarised in Table5.2. These key frequencies are dependent on the stator, injection, and switching frequencies.

Four main points stand out from comparing the graphs of the FFT with the table:

1) At the frequency of injection, a peak arises in the FFT in the stator direct and quadrature currents, as well as in the DC-link capacitor and inverter currents. In the three phases of the stator currents, peaks arise instead at sidebands located at $f_{inj} \pm f_{st}$.
2) In the stator direct and quadrature currents, as well as in the DC-link capacitor and inverter currents, peaks arise sidebands located at $f_{sw} \pm f_{inj}$. However, the peaks are very low in magnitude compared to peaks at the injection frequency.
3) At the frequency of injection, a large current flows between the DC-link capacitor and inverter currents. This means that if the capacitor current cannot be directly measured, making use of the inverter current may be a suitable alternative in context of the overall aim of impedance estimation.
4) Between the DC-link capacitor and inverter currents, there is a discrepancy between the magnitudes of current at the injection frequency. This means that there is a loss in the current at this frequency, meaning that some of the current had been lost either as part of parasitic losses due to unforeseen converter circuit or PCB design, or through the grid.

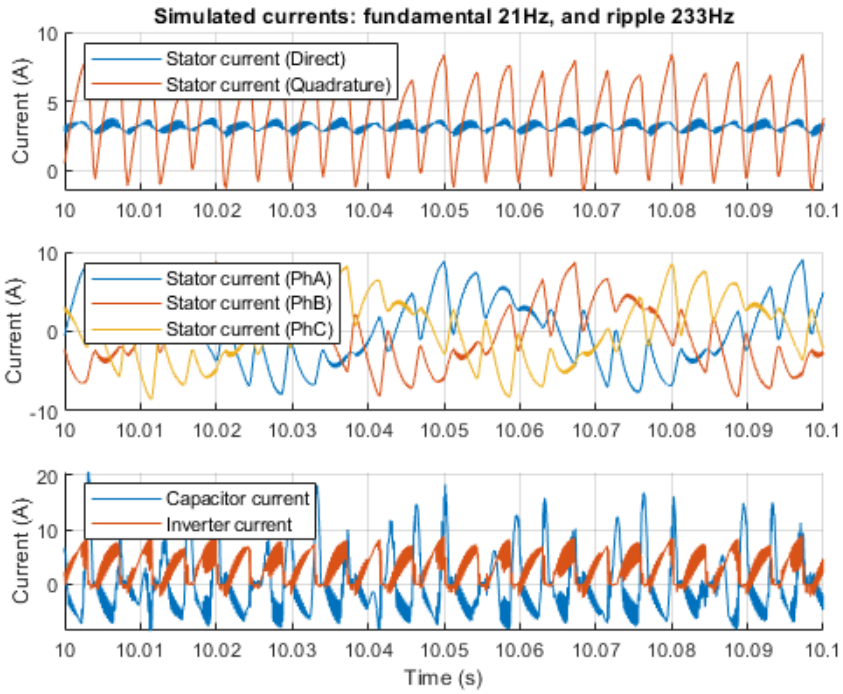


Fig5.2 - Preliminary simulated waveforms using a ripple in quadrature current

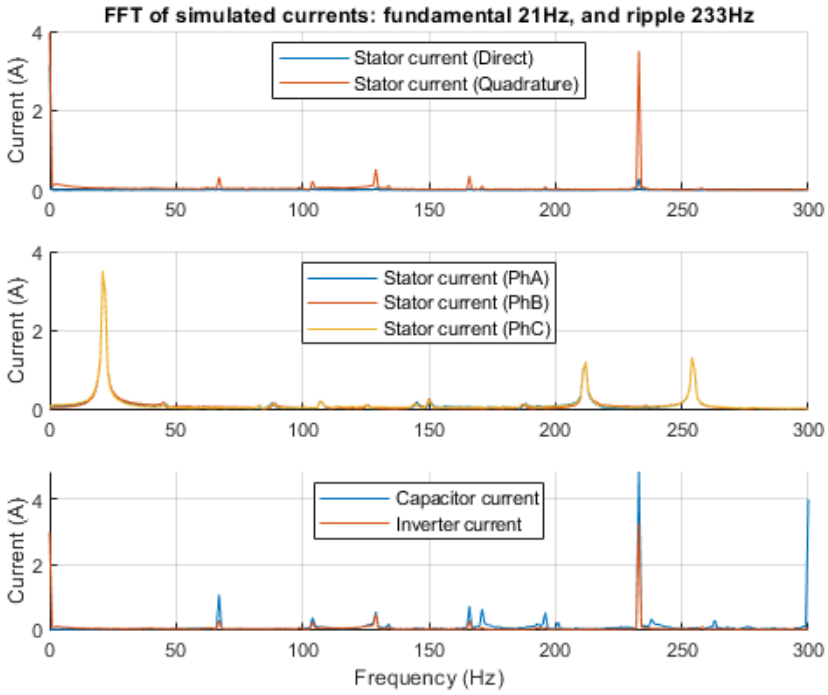


Fig5.3 - FFT of preliminary simulated waveforms, looking at injection frequency

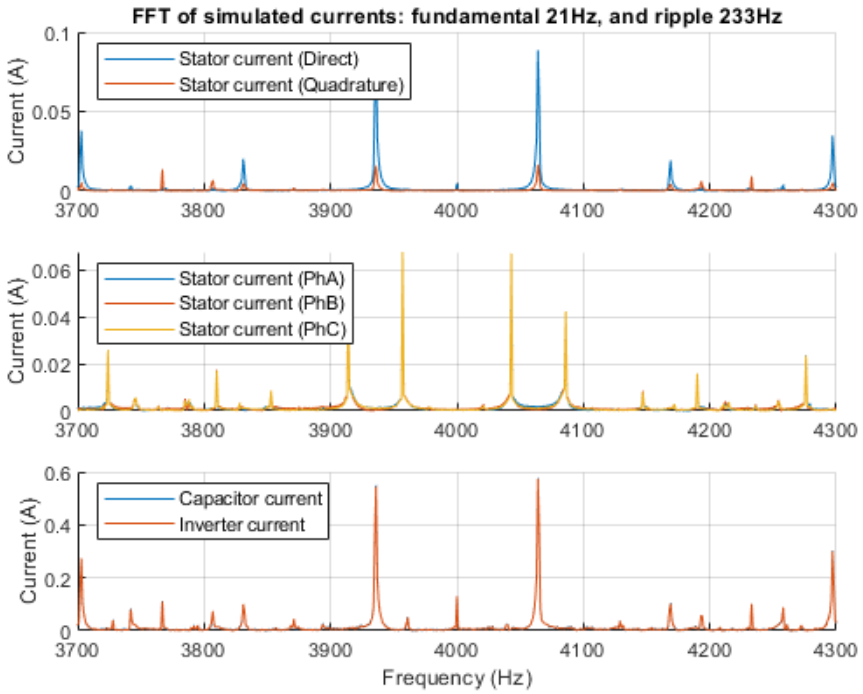


Fig5.4 - FFT of preliminary simulated waveforms, looking at switching frequency

	f_{st}	$f_{inj} - f_{st}$	f_{inj}	$f_{inj} + f_{st}$	$f_{sw} - f_{inj}$	f_{sw}	$f_{sw} + f_{inj}$
i_{sd}	0.0027 A	0.0023 A	0.2862 A	0.0020 A	0.0027 A	0.0046 A	0.0018 A
i_{sq}	0.0525 A	0.0218 A	3.4990 A	0.0116 A	0.0135 A	0.0011 A	0.0092 A
i_{sA}	3.4805 A	1.1518 A	0.0327 A	1.2875 A	0.0007 A	0.0004 A	0.0010 A
i_{sB}	3.4451 A	1.2036 A	0.0602 A	1.3057 A	0.0006 A	0.0006 A	0.0008 A
i_{sC}	3.5055 A	1.1956 A	0.0463 A	1.3034 A	0.0001 A	0.0004 A	0.0003 A
i_{cap}	0.0169 A	0.0119 A	4.8453 A	0.0474 A	0.1119 A	0.1304 A	0.1015 A
i_{inv}	0.0302 A	0.0079 A	3.2495 A	0.0228 A	0.1101 A	0.1300 A	0.1009 A

Table5.2 – Measured peak values of currents following injection of a disturbance signal

5.2.2 – Identifying the capacitor current

This section is used to justify the choice of using the inverter current as an alternative to using the capacitor current, based upon point 3) in section **5.2.1**.

In context of impedance estimation using a commercial drive, a key problem is that vector-controlled motor drives are usually designed to monitor one phase of the current going to the motor as that is all that is needed to maintain control over the motor when the three phases of the motor currents are assumed to be reasonably balanced.

Referring back to the circuit diagram in Fig5.1, the currents in the drive DC-link are related by (5.3):

$$i_{rect} = i_{electrolytic\ caps} + i_{HF\ caps} + i_{inv} \tag{5.3}$$

where i_{rect} refers to the rectifier current; where $i_{electrolytic\ caps}$ refers to the current through the electrolytic capacitors; where $i_{HF\ caps}$ refers to the current through the high-frequency capacitors; and where i_{inv} refers to the inverter current.

In the DC-link, the contribution of high-frequency capacitors are at frequencies far higher than the 10th harmonic of the switching frequency, meaning they have very little effect on at or below switching frequency. Neglecting $i_{HF\ caps}$, it is possible to reconstruct the current flowing through the electrolytic capacitors using a knowledge of the rectifier current and/or the inverter current.

5.2.2.1 – Rectifier current estimation

Specifically referring to (5.3), the six-pulse diode rectifier at the input of the drive does not need current measurement feedback in order to operate: it is not an active front-end, and so rectifier current does not necessarily need to be measured. However, it is still possible to estimate the rectifier current and the estimation process shall be described here.

Based upon [163], (5.4) lists relations between the states of an uncontrolled diode rectifier and grid currents at the input of the rectifier, and Fig5.5 shows the process of reconstructing the rectifier currents based upon (5.4) using another short simulation:

$$S_a = \sum_{n=1}^{\infty} A_n \cos\left(n\omega_{grid}t\right)$$

$$n = 1,\ 5,\ 7,\ 11,\ \ldots, \tag{5.4}$$

$$A_n = \frac{4}{n\pi}\sin\left(\frac{n\pi}{3}\right), \qquad S_{b,c} = S_a\left(t \mp \frac{T}{3}\right), \qquad i_{rect} = \sum \frac{i_{a,b,c}}{S_{a,b,c}}$$

where $S_{a,b,c}$ refers to the switching states of each leg of the inverter phases; where $i_{a,b,c}$ refers to the phases of motor current; where ω_{grid} refers to the grid angular frequency; A_n refers to the odd-numbered coefficients, excluding coefficients that are multiples of three; where T refers to the displacement in time to achieve three balanced phases; and where i_{rect} refers to the rectifier current.

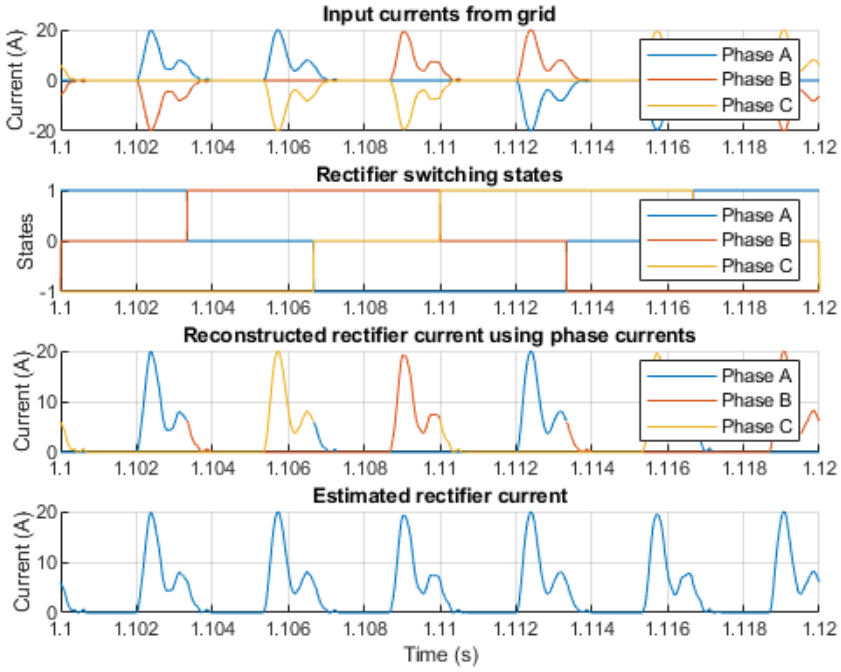


Fig5.5 - Rectifier current estimation

Fig5.5 shows 0.02 seconds of data, which is equal to one period of 50Hz. The first graph in Fig5.5 shows three currents flowing from the grid to the rectifier stage, as suggested by the characteristic “bunny ears” in the current peaks. The shape of these peaks are functions of the rectifier switching states as well as grid-side impedance. The second graph shows rectifier switching states calculated through use of the relations seen in (5.4). The values of the states vary in time in the range [-1,1] and are dependent on the maximum value of the limit, where a higher limit leads to a higher-order trigonometric function and therefore a sharper square wave which is then used to denote transitions in rectifier switching state.

Starting with finding the switching states for phase A of the grid current and then comparing the state and current components of phase A, the relations in (5.4) may be error-checked and used to find the states for phases B and C, as shown in the second graph of Fig5.5.

The third graph in Fig5.5 shows the contribution of each phase of the grid current to the rectifier current, considering at each moment the state of the diode commutations. The overlap/non-overlap periods – which are described in [164] - are not considered in this case, and this is because the intention of this section is to provide a simplified model of the rectifier for use in looking at low-frequency content (<1kHz),

where the effect of the time-domain diode commutations would be apparent at in the frequency-domain at frequencies much higher than 1kHz.

The fourth graph shows the calculated rectifier current. This graph is used more for illustrative purposes than any other, as it allows for a visual inspection in the time-domain to see if the periodic swells in the capacitor current magnitude coincide with the estimated swells and sags in the rectifier current. In this case, this periodic low-frequency shape is seen to be accurate.

As Fig5.5 shows, use of (5.4) with measurements of grid current can provide estimates of the DC-link rectifier current.

5.2.2.2 – Inverter current estimation

Specifically referring to (5.3), inverter currents are not measured as part of the control schemes of typical drives, mostly due to the lack of a need for the measurements of these currents when controlling motor speed. However, it is still possible to estimate the inverter current and the estimation process shall be described here.

Provided a knowledge of at least one of the three balanced motor stator currents as well as the three sets of switching states, the DC-link inverter current may be estimated using the following:

$$i_{inv,estimated} = S_a i_a + S_b i_b + S_c i_c \tag{5.5}$$

where $i_{inv,estimated}$ refers to the estimated inverter current; where $i_{a,b,c}$ refers to the phases of motor current; and where $S_{a,b,c}$ refers to the switching states of each leg of the inverter phases.

The following is then assumed to be true, amending (5.3):

$$\begin{aligned} i_{rect} &= i_{electrolytic\ caps} + i_{HF\ caps} + i_{inv} \\ &\approx i_{electrolytic\ caps} + i_{HF\ caps} + i_{inv,estimated} \end{aligned} \tag{5.6}$$

where i_{rect} refers to the rectifier current; where $i_{electrolytic\ caps}$ refers to the current through the electrolytic capacitors; where $i_{HF\ caps}$ refers to the current through the high-frequency capacitors; where i_{inv} refers to the measured inverter current; and where $i_{inv,estimated}$ refers to the estimated inverter current.

This assumption may be tested through use of another short simulation, as seen in Fig5.6.

Fig5.6 shows three graphs over the period of 4ms. The first graph shows instantaneous motor stator currents; the second graph shows instantaneous switching states which led to each of the transitions in the motor stator currents; and the third graph shows the measured rectifier, inverter, and capacitor currents, together with the inverter current estimated using (5.5).

The bottom graph is the most interesting. The purple line clearly shows a rise in rectifier current which can be seen in a commensurate rise in capacitor current, which is outlined in blue. The inverter currents – shown here as negative inverter currents for to make comparison easier – show the same high-frequency content as seen in the capacitor current. The inverter currents also show that the estimated inverter current almost perfectly matches the measured inverter current.

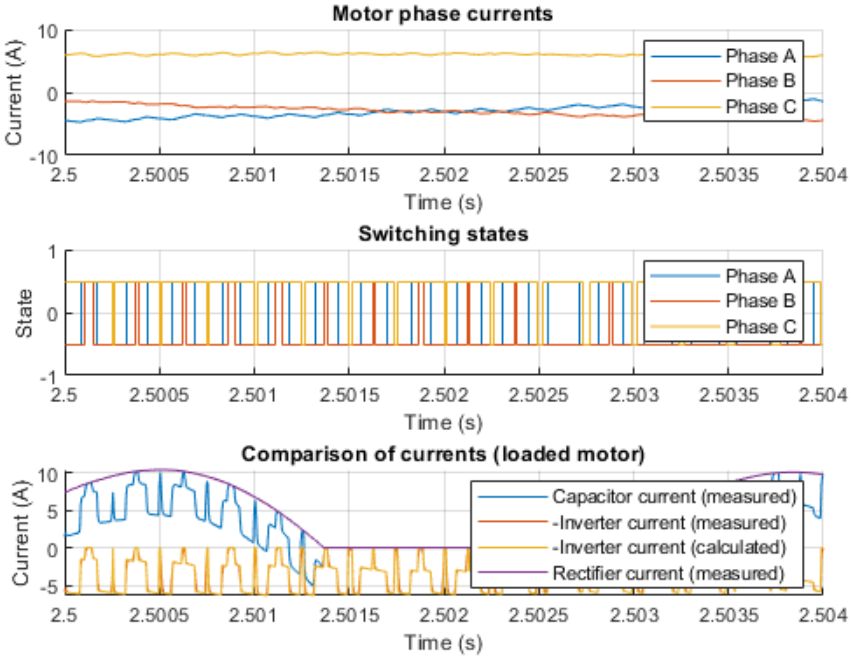


Fig5.6 - Inverter current estimation

As Fig5.6 shows, use of (5.5) with measurements of motor current and knowledge of inverter switching states can provide estimates of the DC-link inverter current.

5.2.2.3 – Conclusions on capacitor current identification

This section showed that although direct measurement of capacitor current may not be feasible, it is still possible to estimate both DC-link rectifier and inverter currents. The estimated rectifier current, containing frequency content from the grid as well as by-products of the six-pulse-diode rectification process, would require measurement of at least one phase of grid currents to provide an accurate estimate. The estimated inverter current, containing frequency content from the motor as well as by-products of the inverter switching process, would require measurement of at least one phase of motor currents as well as inverter switching states to provide an accurate estimate.

If estimating both DC-link rectifier and inverter currents, then the DC-link capacitor current may be calculated, taking into account both the effect of the grid and the motor upon the capacitor current. However, as it is unnecessary to measure the grid current when using an uncontrolled six-pulse diode rectifier, it is therefore infeasible to make use of an estimate of the rectifier current. By process of elimination, the estimated inverter current must then be used in place of the directly measured capacitor current.

Both in theory and in simulation, there would be a vanishingly small error (milli-percentages, or ~0%) between the measured and estimated currents. In practice as part of this work, the error was noticeable in both the time and frequency domains, as discussed in section **5.5.2**.

5.2.3 – The influence of grid-side impedance

This section is used to discuss the effect of the grid upon the currents in the DC-link, based upon point 4) in section **5.2.1**.

The aim here is to understand what injection frequency contained in the motor current can be considered to flow only in the DC-link capacitor. At higher frequencies, or higher values of grid inductance, the injection frequencies are “blocked” for entering the grid by the high grid impedance, and can therefore be assumed only to flow in the DC-link capacitor, and can be used for impedance estimation purposes.

5.2.3.1 – DC reactor

Previously, Fig5.1 showed the circuit diagram of the motor-drive used in this work. Specifically, resistive-inductive (RL) combinations were placed immediately before and after the rectifier. These RL combinations are normally included to reduce the harmonic content of the supply current [114]. In most cases, if a DC reactor is present

in a drive, specific DC inductors are housed in the casing. Sometimes, it is assumed that the supply impedance is large enough to provide this filtering, or even cable and connection impedance in the drive itself.

Overall, a 4% reactor – meaning a maximum voltage drop of 4% between the point-of-common-coupling (PCC) and the drive, as advised by the project sponsors – has consistently been assumed in this work, with the value of the reactor calculated by (5.7):

$$L_{reactor} = \frac{v_{phase}}{i_{max}\omega_{grid}} \cdot \frac{4}{100} = \frac{240}{23 \cdot 2\pi 50} \cdot \frac{4}{100} \approx 1.33mH \qquad (5.7)$$

where $L_{reactor}$ refers to the DC-link reactor; where v_{phase} refers to the RMS grid voltage; where i_{max} refers to the maximum grid current; and where ω_{grid} refers to the grid angular frequency.

(5.7) may be used to design a reactor with a specific maximum volt-drop in mind. However, as the cabling may contribute to a small proportion of volt-drops between the PCC and the drive, the total impedance due to cabling and reactor may be expressed as so:

$$L_{lumped} \approx L_{reactor} + 2L_{cabling} \qquad (5.8)$$

$$R_{lumped} \approx R_{reactor} + 2R_{cabling}$$

where $L_{reactor}$ refers to the inductance of the DC-link reactor; where $L_{cabling}$ refers to the cable inductance; where $R_{reactor}$ refers to the resistance of the DC-link reactor; and where $R_{cabling}$ refers to the cable resistance.

The fact here is that despite a design point being chosen for the reactor, the total impedance at the input of the DC-link will exceed the impedance of the reactor alone, resulting in slightly different frequency response of the DC-link.

5.2.3.2 – Effect of the DC reactor

An issue with the sizing of a DC reactor is the effect of the reactor on the shape of the time-domain waveform. The use of a very small reactor would allow high frequency content to move between the motor and the grid, whereas a very large reactor would effectively block the movement. These effects would be seen in the currents being supplied to the drive from the grid, whereas a small reactor would result in sharp

transitions in rectified current whilst a large reactor would smooth out the rectified current to a more sinusoidal form.

Taking this into account, and also considering (5.8), the effect of a varied grid impedance should be considered when choosing the frequency of injection for DC-link impedance estimation purposes, as is illustrated in Fig5.7.

Fig5.7 is a Bode plot based on the circuit diagram shown in Fig5.1, relating the voltage at the output of the drive (at the inverter stage) to the voltage at the input of the drive (at the rectifier stage). Four plots are presented, where reactor sizing is varied for each plot.

The smallest reactor chosen is essentially zero, with the input represented by cable resistance only. The next reactor is sized as a 1mH inductor, which is close in value to the 4% sizing criterion. The resonant point in the frequency range shown is at roughly 450Hz. Above 450Hz, the capacitive elements dominate the impedance of the DC-link. The next two reactors are sized at 10mH and 100mH, respectively. These inductances are unrealistically large but are used to illustrate a point, which is that as the value of the reactor inductance increases, the resonant frequency decreases and therefore a lower and lower frequency may be used to estimate the impedance of the DC-link electrolytic capacitors. This is because the higher supply inductance is preventing motor injected currents from entering the grid. The full motor injection signal flows into the DC-link capacitor at lower injection frequencies. The motor injection current can be assumed to be equal to the associated component of capacitor current.

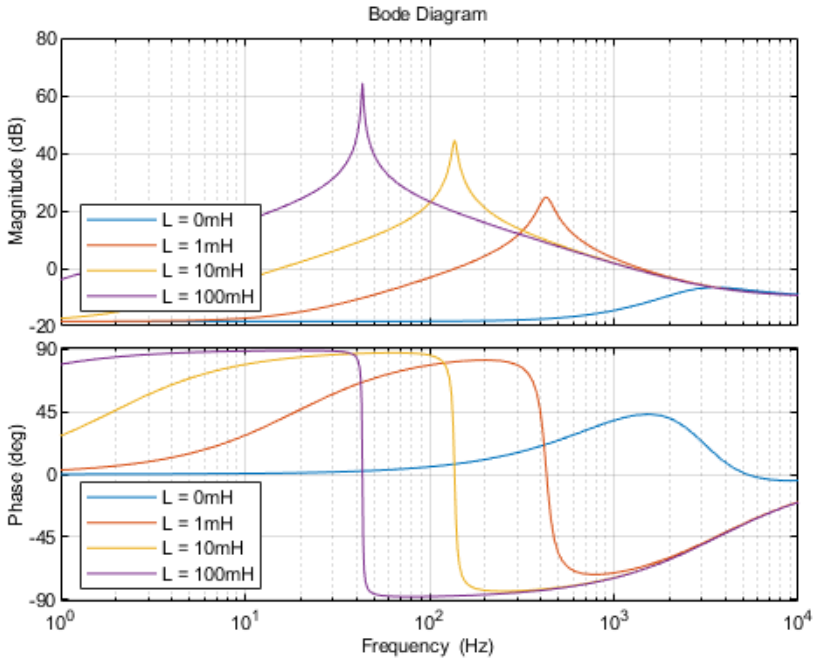


Fig5.7 - Bode plot relating inverter and rectifier voltages

Fig5.7 related voltage at the output of the DC-link (inverter stage) to the voltage at the input of the DC-link (rectifier stage). It is useful for understanding at which frequencies the electrolytic capacitors or the reactor start to dominate the frequency response. If making use of direct measurements of capacitor current, Fig5.7 could be used to identify specific frequencies at which to inject signals as reactor sizing varies.

However, the previous section described the need to use the inverter current instead of the capacitor current. As variation of the DC reactor sizing can affect how much of the injection signal can flow into from the inverter current to the rectifier current, a different Bode plot would be required to identify the relationship between these two currents.

Fig5.8 is a Bode plot based on the circuit diagram shown in Fig5.1, relating the rectifier current to the inverter current. Four plots are presented, where reactor sizing is varied for each plot. The transfer function is presented in (5.9):

$$\frac{i_{rect}}{i_{inv}} = \frac{Z_C}{Z_C+Z_L} \tag{5.9}$$

$$Z_C = 2\left(\frac{\frac{R_{Bleed}}{2}\left(ESR+\frac{X_C R_{Leak}}{X_C+R_{Leak}}\right)}{\frac{R_{Bleed}}{2}+\left(ESR+\frac{X_C R_{Leak}}{X_C+R_{Leak}}\right)}\right)$$

$$Z_L = R_{Reactor} + L_{Reactor}$$

Based on Fig5.7 and Fig5.8, Table5.3 is used to list the resonant frequencies observed as DC reactor sizing varies. At frequencies lower than the resonant frequency, the DC reactor dominates the frequency response, and at frequencies higher than the resonant frequency, the DC-link capacitors dominate the frequency response. This is shown by the immediate change in phase at each resonant frequency.

Comparing the Bode plots with the resonant frequencies, it is clear that the choice of the injection frequency relative to the location of the resonant frequency can affect estimation accuracy. As an example, this means that if (5.7) is used to choose a 1mH reactor with a 100Hz injection frequency, then this injection frequency would be conducted from the inverter current to the rectifier current because it would be blocked from conducting into the capacitor. On the other hand, if using a 1mH reactor and a 1000Hz signal, then this injection frequency would be conducted primarily to the capacitor current instead of the rectifier current because it would be blocked from conducting easily into the inductor.

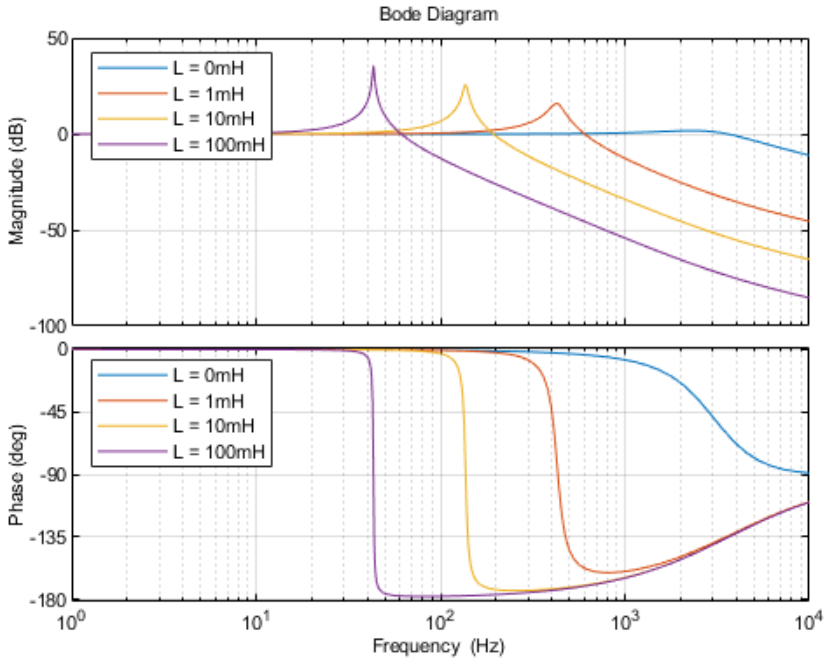


Fig5.8 - Bode plot relating rectifier and inverter currents, based on (5.9)

DC reactor and cabling (mH)	Resonant frequency (Hz)
0.02	2430
1.02	426
10.02	137
100.02	43.3

Table5.3 – Resonant frequencies as DC reactor sizing varies, based on Fig5.7 and Fig5.8

Summarising this discussion, (5.10) can be used to define an ideal frequency range for injection of a signal, dependent on the DC-link resonant frequency. (5.10) is based specifically on Fig5.8, which is in turn based on the DC-link circuit diagram, where Fig5.8 shows that at frequencies higher than the resonant frequency, the inverter current conducts less to the rectifier current and instead conducts more to the capacitor current.

$$f_{inj} > f_{res} \tag{5.10}$$

No other practical limitations were considered here.

5.2.3.3 – Conclusions on the influence of grid-side impedance

This section looked at the transfer functions of the DC-link circuit diagram in context of the effect of the DC reactor. The DC reactor sizing is a function of the cabling impedance as well as the stated percentage voltage drop between the PCC and the drive, and the DC reactor sizing can have a substantial effect on the choice of the injection frequency.

As DC reactor size is varied, the effect is primarily observed in the change in the resonant frequency, and secondarily in the change in the frequency range at which to inject to estimate capacitor impedance. The limitation based upon DC reactor size is expressed by (5.10).

5.2.4 – Conclusions on injection via motor speed perturbation

Based upon the limitations of the work in Chapter 4, this section has discussed injecting a signal via motor speed perturbation.

The variable to control for injecting a signal was identified as the motor stator quadrature current as this specific current directly affects the motor speed without compromising the ability to maintain the rated motor flux.

In context of the currents in the DC-link, estimation of the rectifier current and the inverter current was discussed. However, it was pointed out that the best alternative to making use of the measured capacitor current would simply be to use the estimated inverter current, where the inverter current would be found through knowledge of motor stator currents and inverter switching states.

Having decided that the inverter current would be used for estimation of the DC-link capacitor impedance, the influence of the DC-link reactor was discussed, pointing out that the size of the DC reactor can have a substantial effect on choosing an appropriate injection frequency.

5.3 – Estimation via simulated motor speed perturbation

Chapter 4 had previously used an external AC PSU to inject two specific injection frequencies: either 233Hz or 487Hz. These frequencies had been chosen at the time as they were prime numbers unrelated to any other peak in the drive frequency spectrum.

Continuing with these two frequencies, simulations were run where an signal at either of these frequencies was injected into the stator quadrature current as in (5.1). The DC reactor was set at 4%, or approximately 1mH. The switching and stator frequencies from (5.2) were used again in these simulations. The magnitude of the ripple signal was 2A. Impedance estimation was then carried out using the simulated capacitor and inverter currents.

5.3.1 – Outline of simulated motor speed perturbation

The same simulation used in section **5.2.1** was used again, with the difference being that here that a second step of estimating DC-link capacitor impedance at the injection frequency using both the capacitor current and the inverter current. Fig5.9 shows the simulation diagram for injection into the reference stator quadrature current, where the signal is kept active for a controlled length of time.

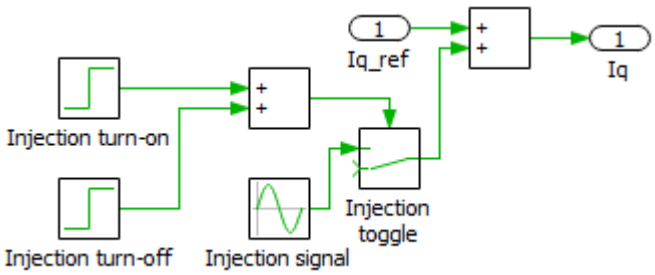


Figure 0-9 - Simulated injection of a signal into reference quadrature current

In addition to the previously used 233Hz and 487Hz, four more frequencies were also used in this section: 677Hz, 1033Hz, 4064.4Hz, and 8kHz. The first two are prime numbers; the third is located at a peak at the sideband of the inverter switching frequency; and the fourth is the second harmonic of the inverter switching frequency. Two more prime numbers, 677Hz and 1033Hz, were used in this section due to Fig5.8 and Table5.3 showing that 487Hz is very close to the resonant frequency where a 1mH reactor is used, meaning that an otherwise unexpected gain might affect the 487Hz signal which is close to the 1mH resonant frequency. Additionally, the two frequencies related to the inverter switching frequency were used because they are expected to be independent of any injection phenomena.

Data was captured from the simulation using a 10s window, where a sample frequency of 20kHz was used. When the motor was loaded, 75% of the rated load was applied. The inverter switching frequency was 4kHz.

5.3.2 – Estimates found via simulated motor speed perturbation

Based on the simulated waveforms shown in Fig5.10 and Fig5.11, the impedance estimation method used in Chapter 4 was used again to estimate values of resistance and capacitance at each individual frequency. Estimates and the related values of absolute error are found in Table5.4 and Table5.5. The most relevant values are then plotted in Fig5.12 and Fig5.13.

Fig5.10 and Fig5.11 show simulated waveforms, specifically the DC-link voltage, capacitor current, and inverter current. Four lines are plotted in each graph, representing changes in the waveforms as injection frequencies are either absent or present in the DC-link quantities. Fig5.10 plots data taken from a simulation where a constant load was placed upon the motor, and Fig5.11 plots data taken from a simulation where a varied 2Hz load was placed upon the motor.

The simulation made use of a 1mH DC reactor (neglecting cabling). Based on the magnitude plot for a 1mH reactor in Fig5.8, any injection signal between approximately 1Hz to 1kHz would flow from the inverter to the rectifier. This would mean that any estimate of the resistance of the DC-link capacitance based on the inverter current in this frequency range would be inaccurate, and that estimation accuracy would be worse at frequencies lower than the resonant frequency.

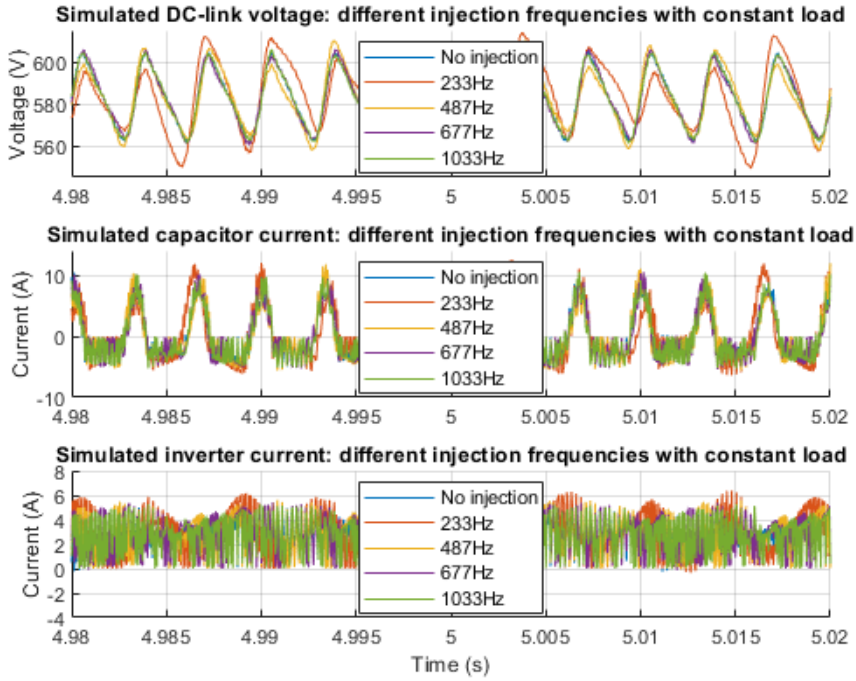


Fig5.10 - Simulations using different injection frequencies with constant load

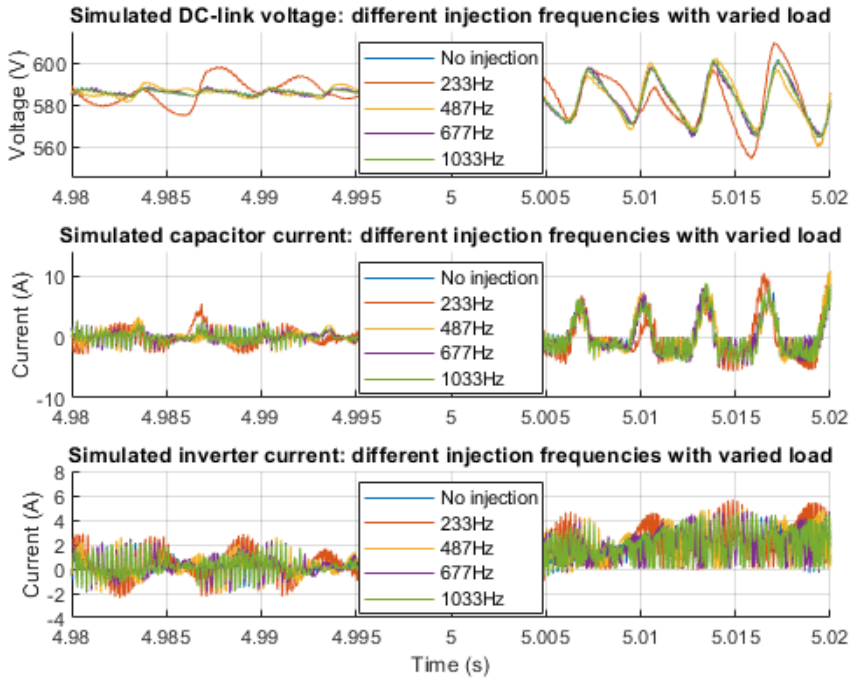


Fig5.11 - Simulations using different injection frequencies with varied load

The impedance estimation method used in Chapter 4 was used to estimate values of resistance and capacitance at each individual frequency plotted in Fig5.10 and Fig5.11. Estimates and the related values of absolute error are listed in Table5.4 and Table5.5.

Through Table5.4, Table5.5, and later in Fig5.13, the error of the estimates made via inverter current at 233Hz, 487Hz, 677Hz, and 1033Hz may be observed. The errors were calculated as described in (5.11):

$$\boldsymbol{\varepsilon}\left(\widehat{\boldsymbol{R}}_{\boldsymbol{i}_{cap}}\right) = \left|\frac{\boldsymbol{R}_{sim}-\widehat{\boldsymbol{R}}_{\boldsymbol{i}_{cap}}}{\boldsymbol{R}_{sim}}\right| \qquad (5.11)$$

$$\boldsymbol{\varepsilon}\left(\widehat{\boldsymbol{R}}_{\boldsymbol{i}_{inv}}\right) = \left|\frac{\boldsymbol{R}_{sim}-\widehat{\boldsymbol{R}}_{\boldsymbol{i}_{inv}}}{\boldsymbol{R}_{sim}}\right|$$

$$\boldsymbol{\varepsilon}\left(\widehat{\boldsymbol{C}}_{\boldsymbol{i}_{cap}}\right) = \left|\frac{\boldsymbol{C}_{sim}-\widehat{\boldsymbol{C}}_{\boldsymbol{i}_{cap}}}{\boldsymbol{C}_{sim}}\right|$$

$$\boldsymbol{\varepsilon}\left(\widehat{\boldsymbol{C}}_{\boldsymbol{i}_{inv}}\right) = \left|\frac{\boldsymbol{C}_{sim}-\widehat{\boldsymbol{C}}_{\boldsymbol{i}_{inv}}}{\boldsymbol{C}_{sim}}\right|$$

Using (5.11), it may be seen that in each table, and also in Fig5.13, the absolute errors of estimates made via inverter current decrease as injection frequency increases. In fact, whether using capacitor current or inverter current, estimating resistance in the frequency range below 1kHz leads to an error of greater than 10%.

This follows what was shown in Chapter 4, where section **4.8.3** stated that a range of 600Hz to 10kHz could realistically be used for estimating resistance. As 233Hz and 487Hz are below this range, and 677Hz and 1033Hz are at the lower end of this range, resistance would ideally be estimated at a higher frequencies, perhaps related to switching harmonics.

Related to switching harmonics, estimates were made at 4064.4Hz and 8kHz where the former was a sideband of the switching frequency and the latter was the second harmonic of the switching frequency, and so these frequencies should be independent of any injection phenomena. Estimates made at these frequencies using either capacitor current or inverter current during steady-state or transients were found to have less than 10% absolute error when compared to the reference values of impedance.

	$f_{inj} = 233Hz$	$f_{inj} = 487Hz$	$f_{inj} = 677Hz$	$f_{inj} = 1033Hz$	$f_{sw} + 3f_{st} = 4064.4Hz$	$2f_{sw} = 8kHz$
v_{cap}	4.2799 V	1.1046 V	0.7257 V	0.3772 V	0.1261 V	0.1952 V
i_{cap}	0.8306 A	0.4311 A	0.4064 A	0.3131 V	0.2917 A	0.5711 A
i_{inv}	0.6037 A	0.3828 A	0.3343 A	0.2912 V	0.2903 A	0.5693 A
R_{sim}	0.3200 Ω	0.3200 Ω	0.3200 Ω	0.3200 Ω	0.3200 Ω	0.3200 Ω
C_{sim}	135 uF	135 uF	135 uF	135 uF	135 uF	135 uF
$\widehat{R}_{i_{cap}}$	0.4458 Ω	0.5237 Ω	0.5371 Ω	0.5713 Ω	0.3249 Ω	0.3078 Ω
$\widehat{C}_{i_{cap}}$	133.2 uF	130.4 uF	138.0 uF	145.2 uF	137.4 uF	133.6 uF
$\widehat{R}_{i_{inv}}$	4.7811 Ω	2.2484 Ω	0.9228 Ω	0.6754 Ω	0.3283 Ω	0.3091 Ω
$\widehat{C}_{i_{inv}}$	130.4 uF	180.7 uF	119.7 uF	139.4 uF	137.7 uF	133.8 uF
$\varepsilon(\widehat{R}_{i_{cap}})$	39.23 %	63.66 %	67.84 %	78.53 %	1.531 %	3.813 %
$\varepsilon(\widehat{C}_{i_{cap}})$	1.3111 %	3.437 %	2.185 %	7.556 %	1.778 %	1.074 %
$\varepsilon(\widehat{R}_{i_{inv}})$	>100 %	>100 %	>100 %	>100 %	2.594 %	3.406 %
$\varepsilon(\widehat{C}_{i_{inv}})$	3.430 %	33.84 %	11.36 %	3.237 %	2.007 %	0.8593 %

Table5.4 – Relevant DC-link magnitudes, simulated values, impedance estimates, and absolute errors of estimates – based on Fig5.10, which used constant loading

	$f_{inj} = 233Hz$	$f_{inj} = 487Hz$	$f_{inj} = 677Hz$	$f_{inj} = 1033Hz$	$f_{sw} + 3f_{st} = 4064.4Hz$	$2f_{sw} = 8kHz$
v_{cap}	2.9711 V	0.6726 V	0.4414 V	0.2195 V	0.0346 V	0.1103 V
i_{cap}	0.5837 A	0.2734 A	0.2534 A	0.1895 V	0.0799 A	0.3188 A
i_{inv}	0.4856 A	0.2692 A	0.2191 A	0.1768 V	0.0795 A	0.3179 A
R_{sim}	0.3200 Ω	0.3200 Ω	0.3200 Ω	0.3200 Ω	0.3200 Ω	0.3200 Ω
C_{sim}	135 uF	135 uF	135 uF	135 uF	135 uF	135 uF
$\widehat{R}_{i_{cap}}$	0.4273 Ω	0.4897 Ω	0.4795 Ω	0.5047 Ω	0.3263 Ω	0.3119 Ω
$\widehat{C}_{i_{cap}}$	134.7 uF	135.4 uF	140.2 uF	147.6 uF	137.4 uF	133.1 uF
$\widehat{R}_{i_{inv}}$	3.2403 Ω	1.6338 Ω	0.8499 Ω	0.6049 Ω	0.3298 Ω	0.3132 Ω
$\widehat{C}_{i_{inv}}$	131.3 uF	172.3 uF	128.4 uF	142.0 uF	137.8 uF	133.4 uF
$\varepsilon(\widehat{R}_{i_{cap}})$	33.448 %	53.031 %	49.844 %	57.72 %	1.9687 %	2.5313 %
$\varepsilon(\widehat{C}_{i_{cap}})$	0.2444 %	0.3259 %	3.8741 %	9.348 %	1.8000 %	1.4370 %
$\varepsilon(\widehat{R}_{i_{inv}})$	>100 %	>100 %	>100 %	89.03 %	3.0625 %	2.1250 %
$\varepsilon(\widehat{C}_{i_{inv}})$	2.7185 %	27.659 %	4.9037 %	5.215 %	2.0815 %	1.2000 %

Table5.5 – Relevant DC-link magnitudes, simulated values, impedance estimates, and absolute errors of estimates – based on Fig5.11, which used varied loading

Section **4.8.3** stated that 300Hz to 10kHz would be an acceptable range for estimating capacitance, also stating that the effect of the reactor-dependent resonance may affect estimation accuracy. This is true here, where the injection frequency of 487Hz was closest to the resonant frequency of 426Hz and also had the higher percentage of error in estimated capacitance compared to the estimates of capacitance found via the other three injection frequencies.

Interestingly, the estimates of resistance found via capacitor current and inverter current at both steady-state and transient operation become approximately equal in magnitude as well as error starting at 1kHz. This indicates that 1mH DC reactor starts to block higher-frequency components and these components flow to the capacitor current from the inverter current, meaning that ideally these higher frequencies components would be used in place of lower frequency components during current estimation.

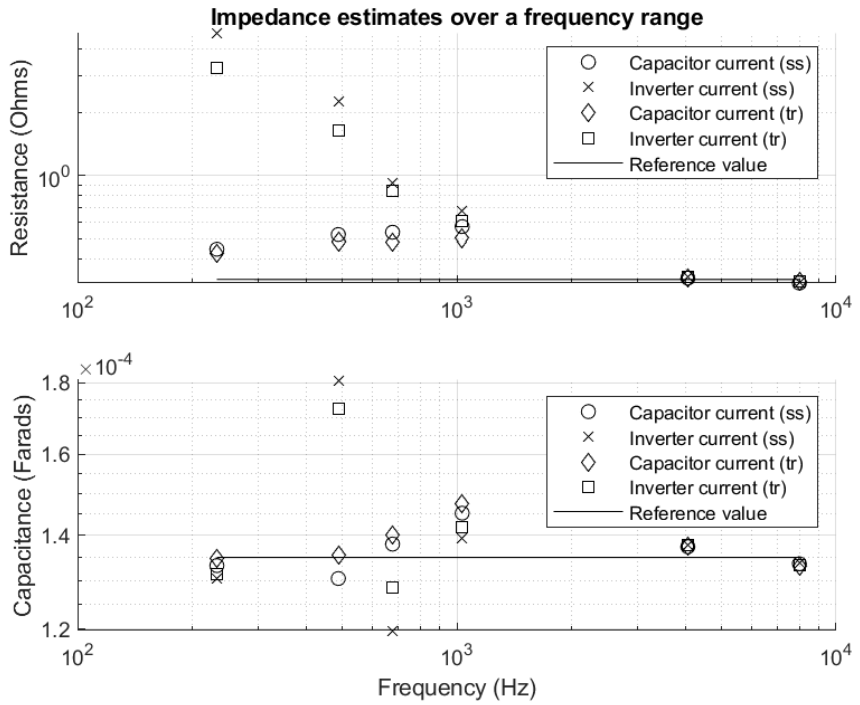


Fig5.12 - Impedance estimates, based on motor steady-state (ss) and transients (tr)

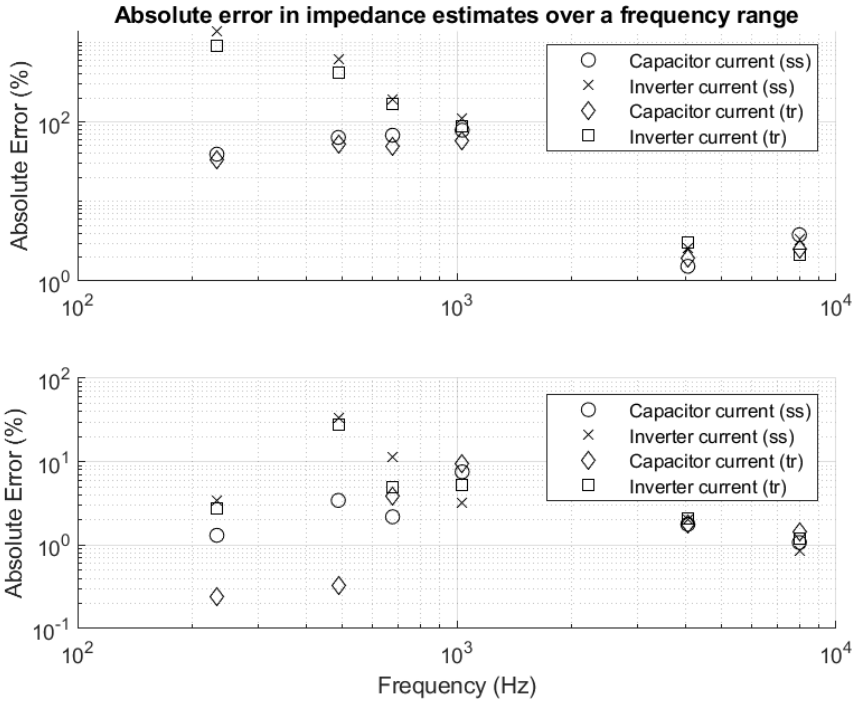


Fig5.13 - Error of impedance estimates, based on Fig5.12

5.3.3 – Conclusions on estimation via simulated motor speed perturbation

Based upon the limitations of the work in Chapter 4, this section has discussed making use of simulation to estimate impedance via motor speed perturbation, taking into account a realistic grid-side impedance.

In context of the currents in the DC-link, the transfer function of the rectifier current and the inverter current was taken into account where DC-link reactor affects the DC-link resonant frequency, and therefore the choice of an appropriate injection frequency if looking for an accurate estimate of either resistance or capacitance.

Taking into account the findings of Chapter 4, section **4.8.3**, the frequency range at which signals were injected in this section was criticised as being too low for finding accurate estimates of resistance. Simply put, estimation of resistance at frequencies below at least 1kHz was shown to produce estimates which were high in error, especially if the inverter current were to be used for estimation.

However, this section did verify via simulation an observation which was made in section **4.8.3**, where empirical data was used as evidence to suggest that capacitance should be estimated in the frequency range of approximately 300Hz to 1000Hz.

Overall, increasing the frequency of injection whilst using a 1mH reactor led to the estimates found via inverter current to be closer and closer in value to the estimates found via capacitor current. This was true for both estimates of resistance and capacitance.

5.3.4 – Limitations on experimental validation

Having devised a method to inject a signal of a known frequency into the DC-link via motor speed perturbation, and having undertaken a series of simulations to look at the effect of varying grid-side impedance on the accuracy of estimates, the next step was to experimentally validate the specific process. However, the COVID pandemic and illness in the supervisory team limited the ability to build or procure a custom research converter.

As a result, experimental validation of the method shown in this section was attempted using the same G120C drive previously used in Chapter 4.

5.4 – Experimental test rig limitation: sampling frequencies

The drive used in this section was arranged as shown in Fig5.14, as was also shown in the previous chapter. The figure shows the drive PCB outside of its case, with the DC-link capacitors on the left-hand-side of the image and the control unit on the right-hand-side of the image.

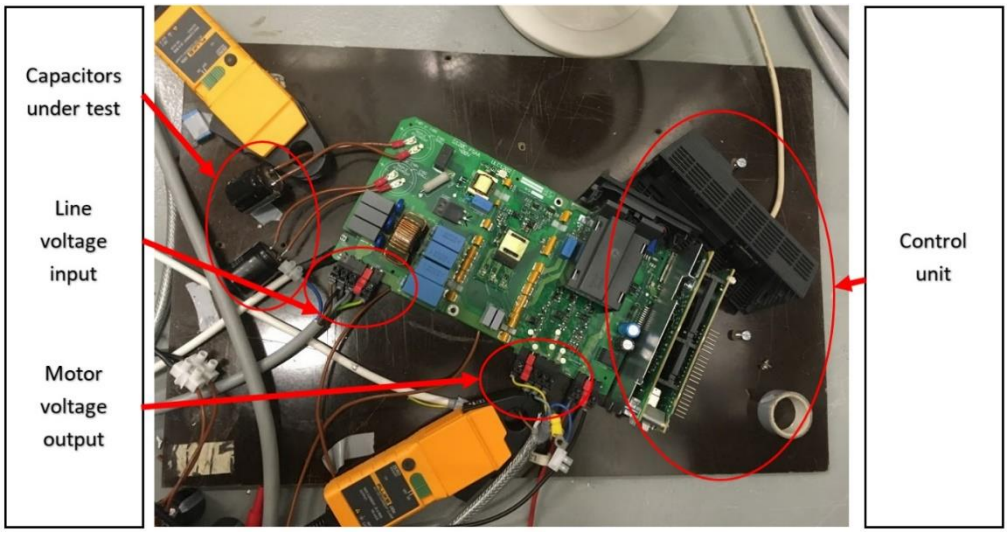


Fig5.14 - Experimental test rig

5.4.1 – Outline of the limitation

As a commercial drive, there are limitations on the functionality of the drive. For example, the previous section made use of a simulation where the sampling frequency was 20kHz, whereas the commercial drive is limited to sampling the motor stator current and the DC-link voltage at a sampling frequency of 2kHz.

Whilst problems were observed in the previous section related to motor speed perturbation – such as capacitor current estimation, grid-side impedance, and choice of injection frequencies - the sampling frequency of 20kHz did not have a major impact on the injection or estimation processes. At the maximum injection frequency of approximately 1kHz, the sampling frequency ratio would be 20:1; and at the minimum injection frequency of approximately 200Hz, the sampling frequency ratio would be 100:1. As a result, making use of a sampling frequency of 2kHz would result in a reduction in the sampling frequency ratios across the injection frequency range.

The project sponsor suggested that the constraint a 2kHz sampling frequency should be accepted in this work as it is the maximum possible rate at which the internal drive

software can sample, and so the constraint of the 2kHz sampling frequency was applied from this stage onwards.

Additionally, a further constraint was applied in terms of communicating with the drive externally. As the converter source code is intellectual property which the project sponsor was unable to share, the method of communicating with the drive was reliant on the drive analogue-to-digital (ADC) input/output terminals.

As the reference stator quadrature current variable could not be directly accessed, an injection signal would have to be supplied to the reference motor speed instead via the input terminals. The schematic for the ADC input/output terminals is shown in Fig5.15.

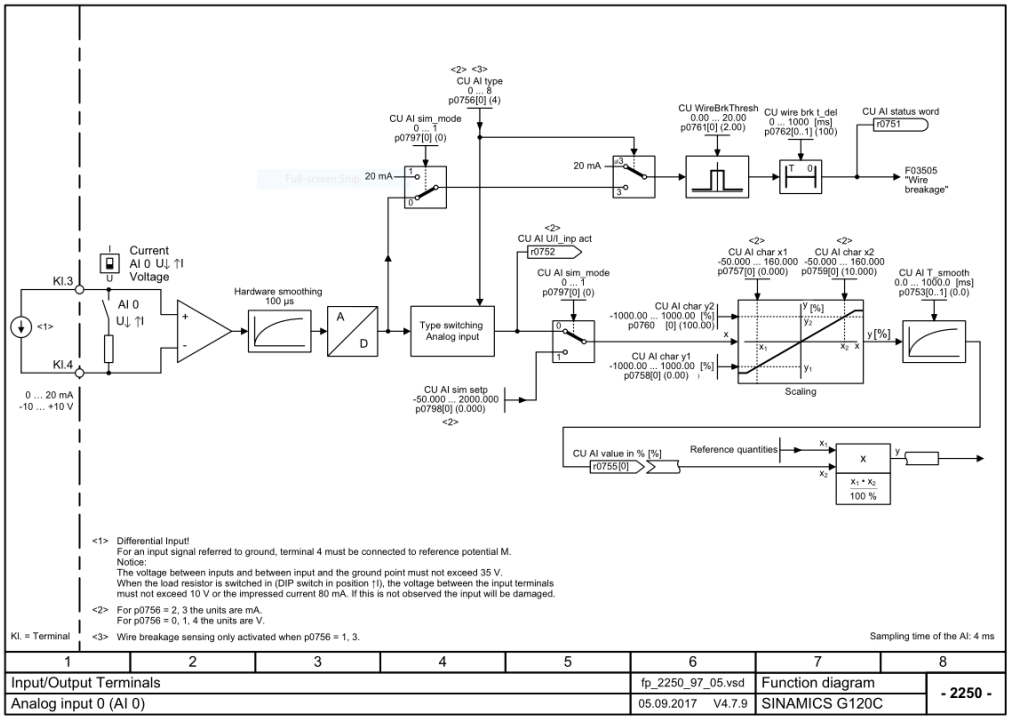


Fig5.15 - ADC input/output terminals

Fig5.15 is taken from the G120C List Manual [112], showing the mechanism between the analogue input terminals and the digital sampler. Of particular note are the two rates mentioned relating to the smoothing of any input signal: there is a smoothing filter present on the analogue side, where the filter has a cut-off frequency of 10kHz. The signals are then sampled at a rate of 250Hz.

Overall, this meant that there were effectively two constraints to be applied in further experimental work:

1) The maximum sampling frequency would be limited to a maximum of 2kHz
2) The maximum injection signal would be limited to a maximum of 250Hz

5.4.2 – Effect of the limitation on estimation accuracy

The immediate issue with reducing the sampling frequency from 20kHz to 2kHz was the restriction on accurately estimating resistance. As was stated in the previous section as well as the previous chapter, estimates of resistance should be found at frequency ranges above 1kHz, meaning that using a 2kHz sampling frequency would immediately prevent finding an accurate estimate of resistance due to the Nyquist frequency limiting sampled signals to a maximum of 1kHz [115]. As a result, using this sampling frequency would mean that only estimates of capacitance may be found.

To understand the effect of the sampling frequency upon capacitance estimation accuracy, the same simulation from the previous section was used again, except the sampling frequency was now changed to 2kHz. The DC reactor was still set at a value of 1mH. Additionally, as the sampling frequency constraint meant that frequencies above 1kHz were unable to be sampled, two frequencies below 1kHz were used here: 59Hz and 157Hz.

Fig5.16 shows the plots of capacitance estimates, and the absolute error of the capacitance estimates compared to the reference capacitance value. Specifically, estimates found at 2kHz are plotted alongside estimates found at 20kHz. The frequencies at which estimates were found are: 59Hz, 157Hz, 233Hz, 487Hz, and 677Hz.

Estimates of capacitance using the capacitor current sampled at a high sampling frequency should be more accurate than estimates of capacitance using the capacitor current sampled at a low sampling frequency. The second graph shows this to be true, where comparison of the yellow cross (20kHz capacitor current) with the blue circle (2kHz capacitor current) shows that errors via capacitor current at 20kHz are lower than at 2kHz. This is also generally true for inverter current, where the error at the purple triangle (20kHz inverter current) is lower than at the orange cross (2kHz inverter current), although this is not true at 157Hz. However, errors via inverter current at 157Hz are well over 1000% anyway so any further comparison would be meaningless.

Overall, Fig5.16 shows - by comparison of estimates found via the motor speed perturbation method - that reducing the sampling frequency from 20kHz to 2kHz would reduce the accuracy of estimation using both capacitor and inverter currents.

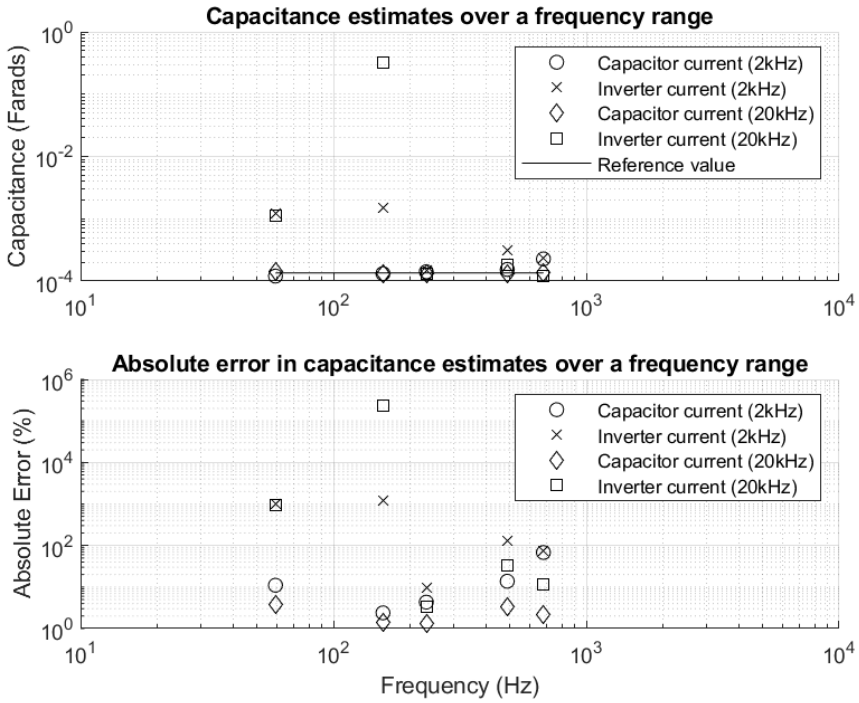


Fig5.16 - Capacitance estimates and absolute errors with varied sampling frequencies, based on motor steady-state

5.4.3 – Effect of the limitation on the choice of the DC reactor

In context of the limitation of the 2kHz sampling frequency, sampling frequency ratios have been mentioned. It was also stated that the following frequencies were used in Fig5.16: 59Hz, 157Hz, 233Hz, 487Hz, and 677Hz. The reason for introducing 59Hz and 157Hz was that it was thought that if the maximum possible injection frequency were to be limited to 1kHz, then it would make sense to inject at much lower frequencies, ideally close to 100Hz.

Section **5.2.3** also discussed the effect of the DC reactor sizing on choice of injection frequencies. As the proposed injection frequencies stretch across almost a decade, it would make sense to compare the estimation accuracy at each frequency.

Fig5.17 shows plots of capacitance estimates and estimate errors when using a 20kHz sampling frequency and when the size of the DC reactor is varied. Fig5.18 shows the same, except using a 2kHz sampling frequency.

Using a sampling frequency of 20kHz, a signal of 677Hz would have a sampling frequency ratio of approximately 30:1. This means that a 677Hz signal would be well sampled and attenuation of the signal would not be a problem. Additionally, a 677Hz signal is has a higher value of frequency than the resonant frequencies listed in

Table5.3, which means that a signal of 677Hz would flow primarily from the inverter current to the capacitor current. Fig5.17 shows that this is true, where estimates found via both capacitor and inverter currents sampled at 20kHz have errors of less than 10%, i.e. they are very accurate regardless of the reactor size.

This logic is also generally true for an injection signal of 487Hz, where estimates have errors of less than 10% when using capacitor current with a 1mH, 10mH, or 100mH reactor; or when using inverter current with a 10mH or 100mH reactor. The one problem here is the estimate via inverter current with a 1mH reactor, where the 487Hz signal is very close to the resonant frequency of 426Hz.

Using injection frequencies of 233Hz, 157Hz, and 59Hz, the variation in estimate errors starts to increase. Estimates made using a larger DC reactor have less error than estimates made using a smaller DC reactor, but a noticeable difference is present between estimates made via capacitor current and estimates made via inverter current. This indicates that even when using a 20kHz sampling frequency, there is a limit on the minimum injection frequency that may be used for estimation if using the inverter current.

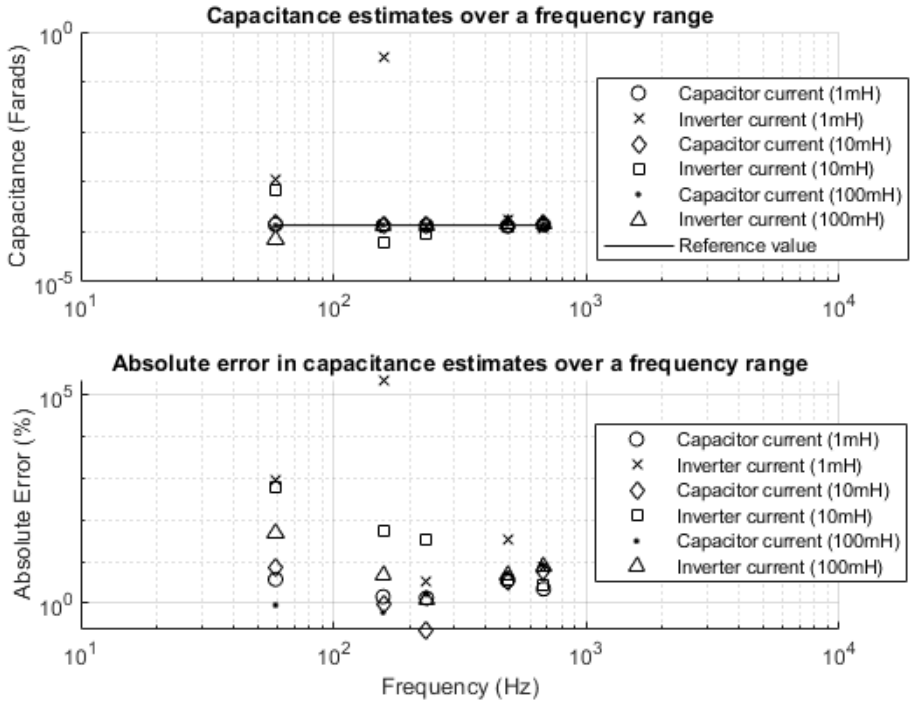


Fig5.17 - Capacitance estimates and absolute errors with varied DC reactor sizing (20kHz)

Fig5.17 used a large sampling frequency (20kHz) and showed that some problems arise when choosing an appropriate injection frequency according to the DC reactor size. On the other hand, Fig5.18 shows that a small sampling frequency (2kHz) severely limits the range of possible injection frequencies.

Looking at Fig5.18, all estimates made at 677Hz had an error of approximately 100%. This was regardless of the choice of the DC reactor or even of the choice of current. In contrast, sampling a 677Hz signal at 20kHz led to errors of less than 10%. This relatively high error was also observed at 487Hz, where errors of approximately 40% were seen despite varying the DC reactor size.

Much the same as before, reducing the frequency of injection led to more variation in the estimate errors, although a larger DC reactor led to a reduced error compared to error from a smaller DC reactor. This was true for both capacitor and inverter currents.

The middle ground between low variation, consistent error and high variation, inconsistent error was found at 233Hz. Here, the estimation errors were generally around 10%, which is not ideal but desirable when looking for consistency across a range of DC reactor sizes. Interestingly, this frequency seemed to provide estimates which were low in error compared to other injection frequencies despite varying sampling frequency or DC reactor.

Overall, Fig5.17 and Fig5.18 both showed that the choice of an appropriate injection frequency is affected by the chosen sampling frequency, and that choosing a low injection frequency would require the use of progressively larger DC reactors to maintain estimation accuracy. The choice of DC reactor would be critical if using a 2kHz sampling frequency, where the ideal injection frequency would be around 100Hz.

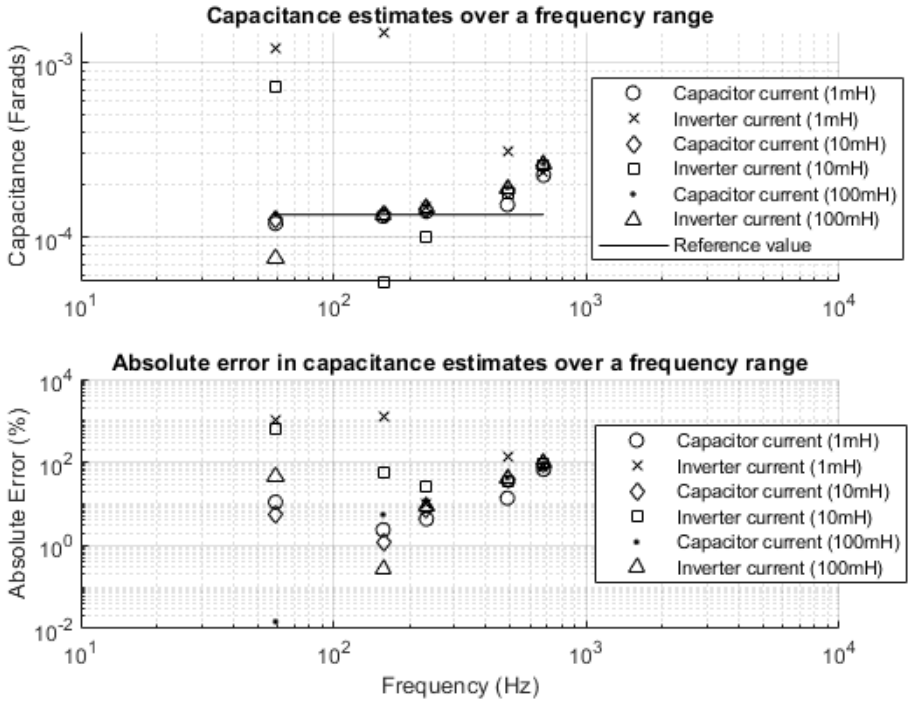


Fig5.18 - Capacitance estimates and absolute errors with varied DC reactor sizing (2kHz)

5.4.4 – Effect of the limitation on the choice of injection frequency

The previous section discussed the effect of the DC reactor size on the choice of injection frequency, in context of sampling waveforms using a sampling frequency of 2kHz. This was because one of the stated constraints was that the test drive can sample waveforms at a maximum of 2kHz.

The other constraint was that the ADC terminals on the test drive can only sample at a maximum frequency of 250Hz. If the problem were to be simplified and it were assumed that an ideally large DC reactor were to be used, the previous section concluded that using injection frequencies higher than 233Hz led to low variation, consistent error whereas using injection frequencies lower than 233Hz led to high variation, inconsistent error. As a result, 233Hz would be the only appropriate choice of all the injection frequencies listed so far, especially with a 2kHz sample rate. However, the close proximity of 233Hz to the 250Hz ADC limit would be expected to lead to attenuation of any injected 233Hz signal.

5.4.5 – Conclusions on the effect of the limitation on sampling frequencies

Due to the internal workings of the test drive, the ideal sampling frequency of 20kHz was reduced to 2kHz. In terms of the effect on estimation accuracy, it was shown that

sampling at 2kHz led to a reduction in accuracy whether using capacitor current or inverter current.

The effect of the reduced sampling frequency on the need for a larger DC reactor was also discussed, where a reduced sampling frequency would then require the use of a lower injection frequency and therefore a larger DC reactor if making use of the inverter current for estimation. The injection frequency of 233Hz was identified as being the only suitable frequency out of the few frequencies discussed, due in large part to the relative lack of variation in estimation accuracy despite varying DC reactor size.

The issue of the ADC 250Hz sample rate was also briefly discussed, where it was stated that a further attenuation issue would affect any 233Hz injection signal applied to the drive.

5.5 – Experimental test rig limitation: inverter current estimation

The drive shown in Fig5.14 was used for experimental testing. The previous section described a limitation of the drive, specifically the issue of sampling frequencies, and how sampling at 2kHz would affect capacitance estimation accuracy – specifically looking at comparisons of estimation using both capacitor current and inverter current. Another limitation found with this drive was the inability to estimate or access the inverter current.

5.5.1 – Outline of the limitation

Referring back to (5.5), inverter current may be estimated using both measurements of motor stator phase currents and knowledge of inverter switching states.

Being capable of closed-loop vector control, the drive makes use of one measurement of motor stator phase current and reconstructs the other two phases; and since the drive clearly makes use of an inverter, switching states are used to control the inverter switches. However, the inability to access the drive source code or the switching states meant that it was impossible to produce estimates of the inverter current via (5.5).

A hardware-based approach was attempted, looking at measuring the inverter current from the surface of the drive PCB. However, it was difficult to measure the inverter current due to the PCB track arrangements, where the SEMIKRON SKiiP module [165] had the rectifier and inverter directly connected together with only capacitor tracks

carrying current away from the module: this meant that the inverter current was effectively inaccessible in the drive without tampering with the SKiiP module.

Fig5.19 is used to illustrate how the rectifier and inverter are directly connected on G120C drives: the three pads to the left of the module footprint are the input phases, where they are each connected to the rectifier; the upper IGBT gates are connected to the pads directly above the rectifier pads; and the lower IGBT gates are connected to the pads directly below the rectifier pads. As a result, it becomes difficult to access the rectifier and inverter currents without either causing an accidental short-circuit, or a disconnect between the pads and the module and therefore an open-circuit.

The task required the use of the inverter current, but the inverter current was inaccessible. As a result, an alternative method had to be devised for estimating inverter current.

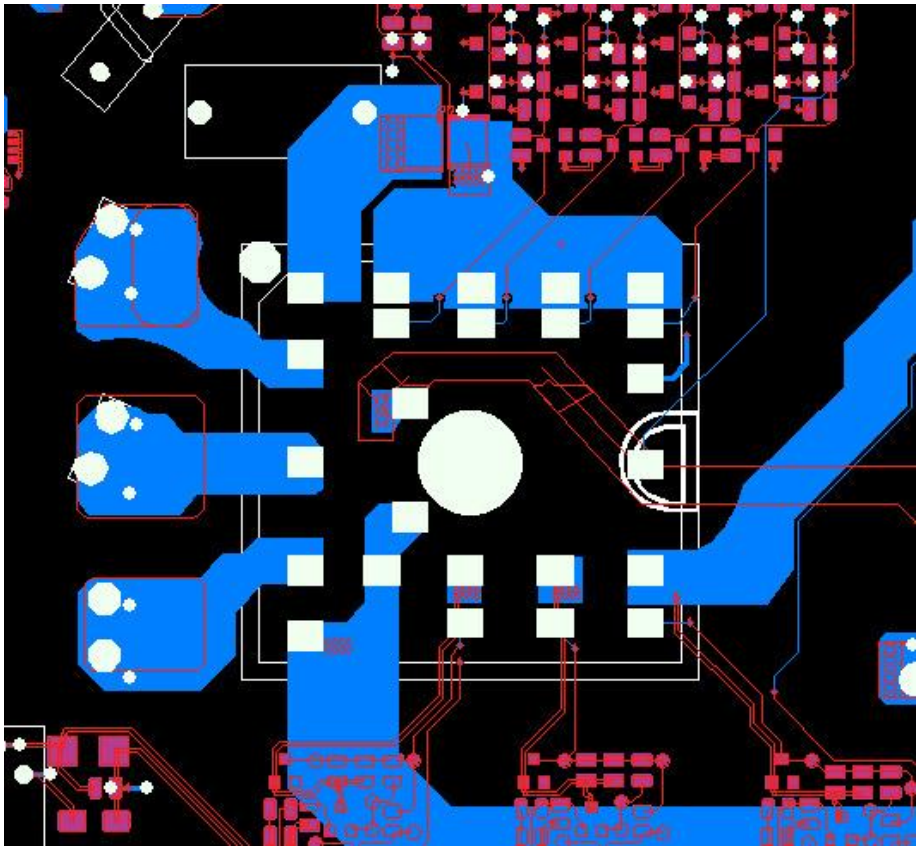


Fig5.19 - Example of in-situ SEMIKRON module with directly connected rectifier/inverter

5.5.2 – Inverter current estimation within the limitation

At the start of this chapter, (5.3) described the relation between rectifier, inverter, and capacitor currents; (5.4) was used to describe the process of estimating the rectifier current; and (5.5) was used to describe the process of estimating the inverter current.

The test drive did not provide access to switching states or the inverter current, and Chapter 4 had stated that any impedance estimation scheme could not rely on using capacitor current measurements for estimation as it would be infeasible to measure the capacitor current in practice.

Although the inverter current was inaccessible, and although the capacitor current could not be used for estimation, it was still possible to measure two phases of the current flowing from the grid to the input of the rectifier, and it was possible to measure the capacitor current. Using the two measured grid currents and the calculated third grid current, rectifier current was estimated using (5.4). Thereafter, the estimated rectifier current and the measured capacitor current were used as in (5.3) to estimate the inverter current.

This meant that the estimated inverter current was itself based on an estimate of rectifier current, meaning that it was imprecise. Fig5.20 shows the three currents where the rectifier current was estimated, the capacitor current was measured, and the inverter current was estimated. The rectifier current estimation was imprecise because only two phases of grid current were measured using two separate current clamps as opposed to three phases, where small offsets in the measurements of each separate clamps contributed towards errors when calculating the third phase. This error then propagated forward into the estimation of the inverter current.

As the rectifier current was imperfectly estimated, the magnitudes of the peaks at the lower frequencies in the frequency spectrum of the inverter current should be assumed to differ slightly to the actual inverter current within the drive. However, as the capacitor current was directly measured, the higher frequencies in the inverter current should be assumed to be almost exactly the same as in the capacitor current. This can be observed in Fig5.20, where the capacitor current follows the rectifier current during the 300Hz pulses but otherwise follows the (negative) inverter current.

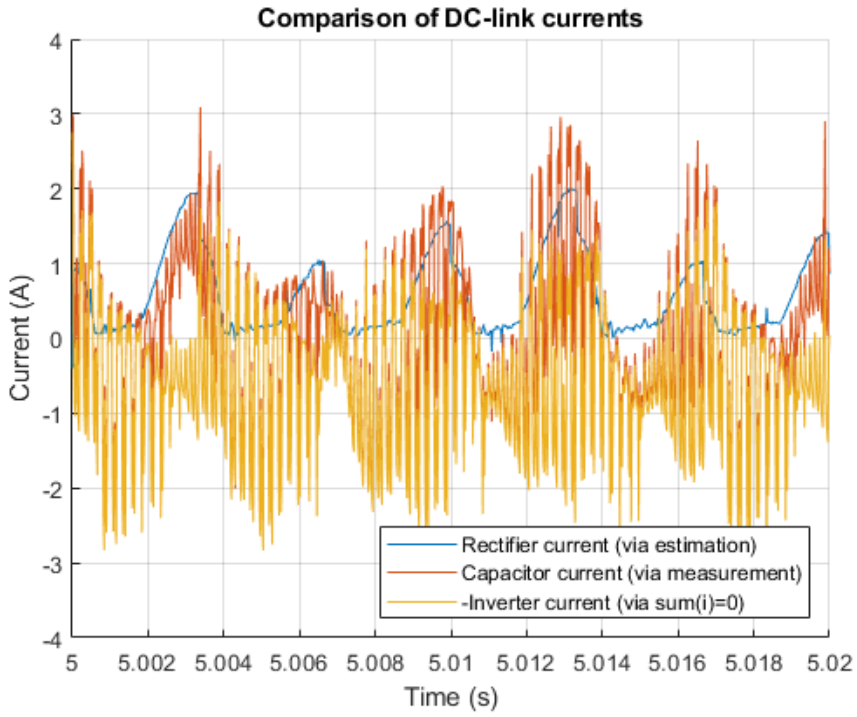


Fig5.20 - Estimated rectifier current, measured capacitor current, and negative estimated inverter current

The estimated rectifier current, being estimated using two measured grid currents, was not a perfect reconstruction of the rectifier current. This is shown in Fig5.21 and Table5.6, which plot and list the magnitudes of the first three harmonics induced by the six-pulse diode bridge rectifier within the rectifier, capacitor, and inverter currents.

The rectifier current was estimated using two phases of the grid current, and it was an imperfect estimate. In hindsight, estimation accuracy could have been improved by measuring all three phases of the grid current, regardless of the fact that only two out of three (balanced) grid phases are theoretically required to estimate the third phase.

The imperfection in estimate may be easily observed in Table5.6, where the table shows that the six-pulse diode rectifier bridge correctly contained harmonics at multiples of 300Hz (or harmonics of six times the grid frequency of 50Hz). The same table states that the estimated value of current at 300Hz in the rectifier current was 0.696A whereas the measured capacitor current had a peak of 0.711A at 300Hz.

Overall, this was not a significant issue as this chapter does not focus on making use of harmonic content at 300Hz. Additionally, the table and the graph show that the "trend" of currents at 600Hz and 900Hz were as expected, where higher peaks were observed in the estimated rectifier current at these two frequencies than in the

measured capacitor current: this meant that frequency content at higher frequencies could be expected to be accurate.

However, the implication was that since the fundamental (low-) frequency content of the estimated rectifier current was affected by a small but non-zero amount of error, then frequency content at similarly low frequencies may be affected. In context of this work, this would then mean that use of any low-frequency harmonic content such as injected signals would also carry a small but non-zero amount of error.

In this way, an error would be expected to be present in estimates if using the practical methods laid out in this chapter, due to the error involved in estimating the rectifier current and then also due to the error involved in estimating the inverter current using the estimated rectifier current.

Frequency (Hz)	**Estimated rectifier current (A)**	**Measured capacitor current (A)**	**Estimated inverter current (A)**
300	0.696	0.711	0.017
600	0.384	0.375	0.010
900	0.120	0.110	0.013

Table5.6 – Comparison of the magnitudes of the first three harmonics induced by the six-pulse diode bridge rectifier within the rectifier, capacitor, and inverter currents

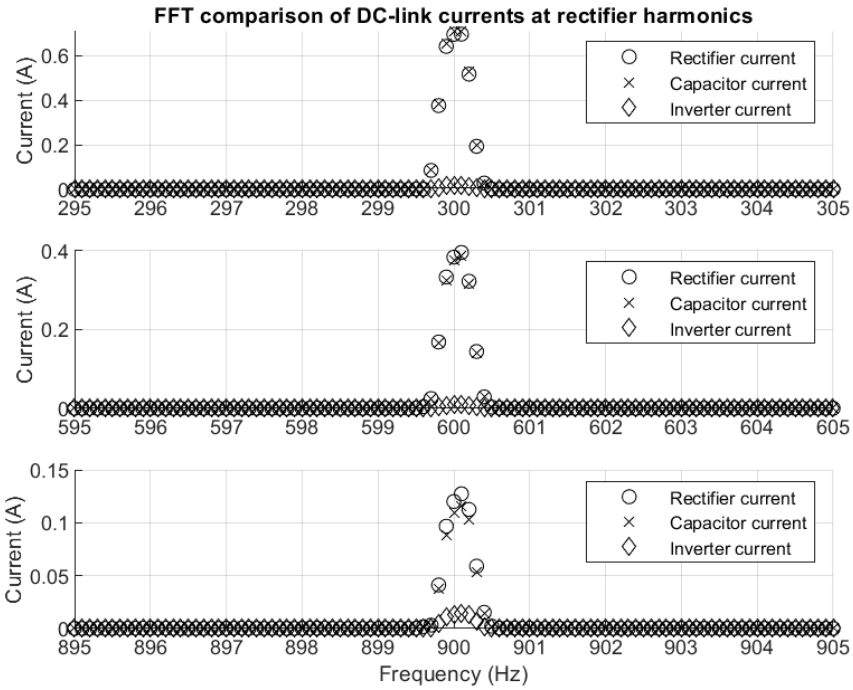


Fig5.21 - Comparison of the magnitudes of the first three harmonics induced by the six-pulse diode bridge rectifier within the rectifier, capacitor, and inverter currents, linked to Table5.6

5.5.3 – Impedance estimation within the limitation

Using the drive ADC terminals shown in Fig5.15, the reference motor speed was provided with a speed setpoint with a ripple signal overlaid on top, where the ripple signal was of a chosen injection frequency. This is shown in Fig5.22.

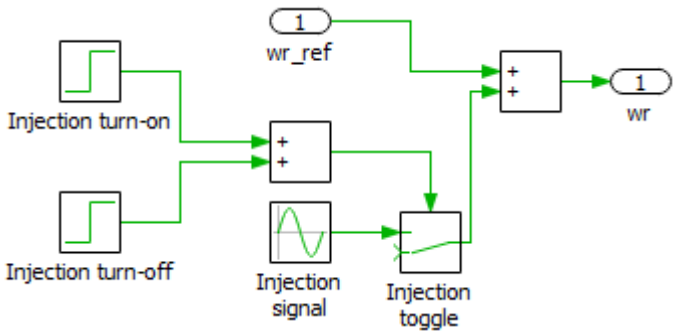


Fig5.22 - Simulated injection of a signal into reference motor speed

The project sponsor had advised that a 4% DC reactor be assumed (approximately 1mH) and a 2kHz sampling frequency be used.

However, considering that section **5.4** had shown that the use of both a 2kHz sampling frequency and a 1mH DC reactor would lead to wildly inaccurate estimates, the

sampling frequency was instead kept at a high value, and was in fact increased to 50kHz to try to further mitigate issues observed when sampling at 20kHz. The 250Hz ADC constraint was still observed and so signals were injected at frequencies of 59Hz, 157Hz, and 233Hz.

Signals were provided to the drive ADC via an NI 9263 [166] digital-analogue converter (DAC) module and an NI cDAQ 9174 [147] chassis, where they were controlled via a MATLAB scripted interface. Measurements of DC-link voltage and the stator and capacitor currents were made via an NI 9222 [148] ADC module, a Pico Technology differential 25MHz 700V probe [157], and three Fluke i30s 100kHz current clamps [158].

Three sets of tests were run using the drive. Within a window of 10s, measurements were taken of the DC-link voltage, the capacitor current, and two grid currents for the purpose of estimating the rectifier current. A sampling frequency of 50kHz was used, with an anti-aliasing filter of 12kHz. Within the 10s window, the drive was constantly passed a speed reference comprised of 40Hz with a ripple frequency for the entire duration of the window. During this time, the motor was under a constant load of 50% of rated load torque.

The motor correctly followed the provided speed reference, where the reference signal had a ripple signal overlaid on top. However, the frequency spectra of the currents showed that the peaks which should have been exactly at the frequencies of injection consistently shifted by a few Hertz as shown in Table5.7.

Table5.7 shows measured peak values of current prior to and following injection of a signal, where the injected frequency is stated as well as the frequency at which the signal was observed. Two observations are to be made: the first, that the there was a larger shift in frequency as the injected frequency approached 250Hz; and the second, that as injection frequency increased, more current at the (observed) injection frequency flowed from the inverter current to the capacitor current.

The project sponsor advised that the shift in frequency should be assumed to be due to an anti-aliasing issue related to the terminal hardware, probably caused by the very close proximity of the injection frequencies to the 250Hz sampling rate of the drive ADC.

Injected Frequency (Hz)	Observed Frequency (Hz)	Rectifier Current (A)	Capacitor Current (A)	Inverter Current (A)
No injection	59	188.3u	189.9u	178.2u
59	59	13.7m	3.71m	13.8m
No injection	161.1	524.7u	653.5u	160.7u
157	161.1	1.17m	1.08m	1.21m
No injection	241.6	966.9u	587.6u	620.7u
233	241.6	3.87m	7.38m	6.83m

Table5.7 – Measured peak values of current prior to and following injection

At the frequencies of the observed injection frequencies, impedance estimation was carried out, with estimation made using both the directly measured capacitor current and also the estimated inverter current. Results are shown in Table5.8, Fig5.23 and Fig5.24.

Table5.8 lists the measured values of resistance and capacitance of the test capacitors (taken via the Rohde & Schwarz HM8118 [156]) as well as the estimated values found through use of capacitor current and inverter current. Fig5.23 and Fig5.24 show plots of impedance estimates and estimate errors based on Table5.8.

Table5.8 shows that increasing the frequency of the injection signal leads to reduced errors in estimates of both resistance and capacitance, and this can be linked to Table5.7, where it was shown that increasing the frequency of the injection signal resulted in more of the inverter current flowing to the capacitor current. As more current flows from the inverter to the capacitors, the frequency spectrum of the inverter current is more representative of the capacitor current, resulting in higher accuracy of impedance estimation.

The previous simulation study had been concluded that frequencies below 1kHz would be unsuitable for estimating resistance, and the error would be especially pronounced if estimating via inverter current. This was reiterated again in Table5.8, Fig5.23 and Fig5.24, where the error of the estimated resistance via capacitor current was at least approximately 30% and the error via inverter current was at least approximately 1000%.

The simulation study had further identified 233Hz as the most suitable of a list of frequencies due to a lack of variation in the estimation accuracy as the DC reactor size varied. During the simulation study, this was true whether using capacitor current or inverter current. Again, this was reiterated by Table5.8, Fig5.23 and Fig5.24, where the errors of the estimated capacitance via both capacitor and inverter currents are below 10% at 233Hz.

Whilst some of the error in the estimates found using the inverter current were due to the fact that the estimated inverter current is not a perfect alternative to the measured capacitor current, a contribution to this error was also due to the fact that the inverter current was an estimate based upon another estimate, as was stated in section **5.5.2**.

As was shown in the simulation study, estimates of both resistance and capacitance made at frequencies above 1kHz via inverter current were of low error when compared to the reference value and also when compared to the estimates via capacitor current. To show this, a switching frequency sideband as well as the second switching harmonic are both included in Table5.8, Fig5.23 and Fig5.24, where Fig5.24 plots absolute error of estimates for ease of visualisation and visualisation of the error at each frequency.

These two switching-related frequencies are included to reiterate the constraint of the 2kHz sampling frequency: the motor speed perturbation method is shown to work at 233Hz for accurately estimating capacitance via the capacitor or inverter currents, but the use of a higher frequency is required for accurately estimating resistance via the inverter current.

	Using capacitor current		Using inverter current	
	Mean Resistance (Ω)	**Mean Capacitance (F)**	**Mean Resistance (Ω)**	**Mean Capacitance (F)**
Measurement via LCR meter at 300Hz	0.30	115u	0.30	115u
Estimation at 59Hz	0.71	123.03u	6.53	3856u
Estimation at 161.1Hz	0.08	113.87u	6.14	291.4u
Estimation at 241.6Hz	0.40	115.35u	3.48	124.15u
Estimation at $f_{sw} + 3f_{st}$, 4123Hz	0.23	117.11u	0.23	117.46u
Estimation at $2f_{sw}$, 8kHz	0.22	124.60u	0.22	125.55u

Table5.8 – Measured values and mean estimated values of impedance using capacitor and inverter currents

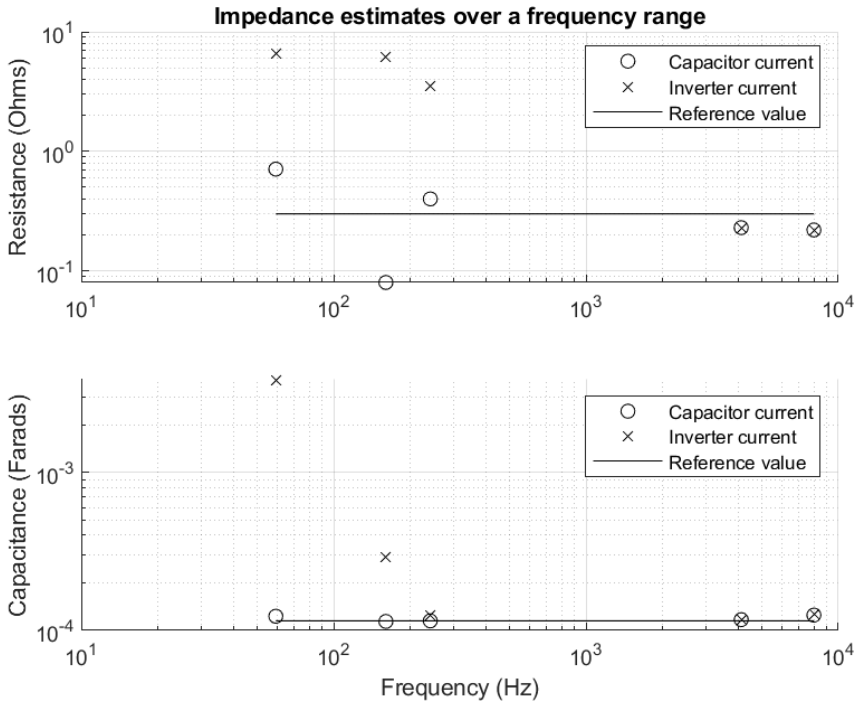


Fig5.23 - Impedance estimates found using the test drive

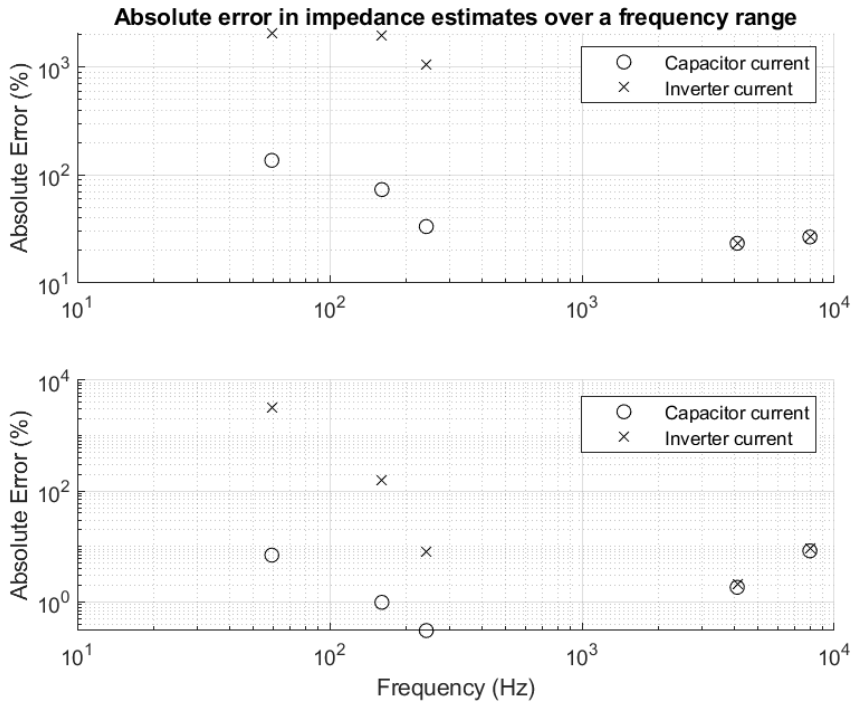


Fig5.24 - Absolute errors of impedance estimates found using the test drive

5.5.4 – Conclusions on the effect of the limitation on inverter current estimation

Inverter current was estimated using an alternative method to what was proposed, where the inverter current would ideally be estimated using switching states whereas the method here made use of the estimated rectifier current.

Using a commercial test drive, impedance estimation was at the chosen injection frequencies of 59Hz, 157Hz, and 233Hz. The choice of these frequencies followed the constraint of the 2kHz sampling frequency, as well as the constraint of the 250Hz ADC limit.

As indicated by the simulation study, the estimation errors were high at the lower frequencies and low at 233Hz. The simulation study had indicated that at 233Hz, estimation would be ideal using both capacitor and inverter currents regardless of the size of the DC reactor. Incidentally, the DC reactor was stated to be 1mH for this drive.

Using the inverter current, estimation of resistance at 233Hz was very high in error. This was to be expected, as it had previously been stated that resistance should be estimated at higher frequencies. This was verified by finding that estimates of resistance at switching-related frequencies were low in error compared to the measured value of resistance.

Using the inverter current, an accurate estimate of capacitance at 233Hz was possible. However, the injection itself was not ideal as the input 233Hz signal was not found at the exact frequency of 233Hz when looking at the current frequency spectra, but instead the signal was found to have shifted to 241.6Hz due to the interaction of the signal with the drive ADC terminal. This shift in frequency was understood to be due to limitations of the practical system; overall, the injection of a signal for use in estimation purposes was successful.

5.6 – Summary

The previous chapter showed that impedance estimation of the DC-link capacitors was possible via signal injection, where an external AC power supply unit was used to inject the signal into the DC-link and where capacitor current was directly measured for use in the estimation process. These two dependencies were noted as being infeasible in practice.

This chapter described a method of injecting a signal into the DC-link via motor speed perturbation where the estimated inverter current was used as an alternative to making use of the capacitor current. A simulation study was used to compare the accuracy of estimates of impedance via capacitor and inverter currents, where the two currents were used to verify that estimates made via inverter current would be comparable to estimates made via capacitor current. Injection of a range of frequencies was considered, where estimation accuracy according to frequency range was noted; and the effect of the size of the DC reactor upon the estimation process was also discussed, where it was shown that injection of low frequency signals would require progressively larger DC reactors.

This chapter also described the steps taken towards validating the idea of injection via motor speed perturbation, as well as impedance estimation via use of the estimated inverter current. Within the limitations of the drive provided by the project sponsor, it was shown that - in principle – impedance estimation of the DC-link capacitors was possible by making use of an estimated inverter current.

This method was found to be less than ideal because of the following limitations:

- Due to the effect of the COVID pandemic on the project timeline, a bespoke research converter could not be procured for use with this project.

- Due to lack of access to the commercial drive controller, motor speed perturbation could not be implemented via adjusting the reference stator quadrature currents.
- Due to lack of access to the commercial drive controller, inverter switching states could not be accessed for use with estimation of the inverter current.
- Due to the design of the drive PCB, the inverter current could not be easily accessed without disrupting the operation of either the rectifier or the inverter.
- Due to the 2kHz sampling frequency constraint, nominally ideal injection signal frequencies were limited to below 1kHz.
- Due to the 250Hz ADC terminal sample rate constraint, nominally ideal injection signal frequencies were limited to below 250Hz.

However, despite the limitations listed above, the experimental work did still validate the simulation study which stated that using a 1mH DC reactor and using a 2kHz sampling frequency, it would be possible to inject a signal of 233Hz and find an accurate estimate of capacitance using the estimated inverter current.

Additionally, it was also shown that if the sampling frequency of the commercial drive were to be increased to at least 20kHz, it would be possible to use the switching-related frequencies in the estimated inverter current to find an accurate estimate of both capacitance and resistance without requiring additional current sensors or motor speed perturbation.

A proposed increase in sampling frequency may also potentially allow for further monitoring of issues in the quality of the grid, as well as for online-monitoring of issues relating to motor failure modes where symptoms of motor failure may present at frequencies which are a function of switching frequency or where monitoring of grid quality issues may benefit from a high sampling frequency ratio.

Chapter 6 – Conclusion

6.1 – Summary

In this work, an impedance estimation method based on signal injection was presented and tested using a series of tests involving a injection of a ripple into the DC-link of a motor drive via an external power supply unit, and then using a more realistic test involving injection of a ripple into the DC-link of a motor drive via reference motor speed. Capacitors were aged using an accelerated ageing process for use with the presented impedance estimation method.

6.1.1 – Impedance estimation

The first series of tests were primarily used to test the sensitivity of the presented impedance estimation method to variations in the motor electrical operating conditions, where measurements were taken directly of the current through the DC-link electrolytic capacitors.

The second test was used to verify that the same method would work in practice using the limitations of an industrial drive, where access to the specific DC-link electrolytic capacitor current measurement may not be guaranteed.

Injection of a ripple signal was considered as suitable for this work after looking into literature on relevant impedance estimation schemes, where [74] and [76] implemented impedance estimation schemes based on signal injection using no additional sensor to measure the DC-link capacitor current. This specific current measurement was ultimately a limiting factor in this work, where the project sponsor directed that direct measurement of this specific current was impractical.

Within the scope of the needs of the project sponsor, it was shown that in principle it is possible to estimate DC-link capacitor impedance using a 2kHz sample speed and an estimate of the inverter current. Outside of this scope, it was also shown that the same method may be used to estimate impedance using other frequency components present in the inverter current.

6.1.2 – Accelerated ageing

An accelerated ageing process was devised for producing batches of aged capacitors for use in testing the impedance estimation method, where electrolytic capacitors used in the DC-link had their impedances measured using laboratory impedance measurement units and then had their impedances estimated using in-situ measurements of voltage and currents. Taking a measurement of impedance as well

as estimating impedance allowed for estimation accuracy to be compared as test conditions varied. This method was considered to be very “realistic” for the purpose of irreversibly changing the impedance of electrolytic capacitors, although in hindsight it had not taken into account the issue of damage to capacitor insulation where the pins and the sleeving of the capacitors were also subject to damage in addition to the dielectric-impregnant foil and fluid [32].

An accelerated ageing process was used to produce batches of aged capacitors after taking into account methods in the literature relating to impedance estimation as well as causes of failure modes. For example, [48] described very clearly the causes of open and short circuit failure modes, where it was shown that changes in the state of the dielectric medium or the electrolytic liquid contribute to capacitor failure with the change in state being observable in capacitor impedance.

In terms of implementing an accelerated ageing process to be applied to test capacitors, [56] described setting up a test bench for injecting an AC ripple injection signal into test capacitors placed under a forward bias voltage, and [51] showed the possibility of usage of both electrical and thermal stress tests to induce degradation in capacitors.

6.2 – Research contributions

This section summarises the main contributions presented in this thesis:

1) Investigating and developing an impedance estimation scheme appropriate for an industrial drive operating under a range of conditions, as shown in sections **4.5**-**4.7** and sections **5.4**-**5.5**.
2) Investigating and developing a simple and repeatable accelerated ageing scheme to rapidly age batches of test capacitors for use in validation of the impedance estimation scheme, as shown in section **3.5** and section **4.8**.

6.3 – Future recommendations

6.3.1 – Impedance estimation

Reflecting on the second test which involved injecting a signal into a drive via reference motor speed, limitations were faced due to the presence of the filtering effect of the drive ADC. In practice, ripple injection would more ideally be introduced through the

use of a vector control scheme, where the motor quadrature current control would be used to perpetuate the ripple [1].

6.3.2 – Accelerated ageing

Reflecting on the accelerated ageing process used in this work, the ageing process and the measurement of the capacitor impedances could be improved by more precisely controlling capacitor core temperatures whilst sweeping frequencies via EIS.

Ideally, it would be preferable to measure the impedances of test capacitors whilst they are held under the same nominal voltage as the drive DC-link, but this is impractical using laboratory EIS measurement devices due to device voltage limits being limited to below 20V. Additionally, it would be interesting to see if a repeatable method of controlled degradation could be further carried out as described in [57], for the purpose of reducing time taken to age batches of capacitors.

In context of the industrial theme of the project, the accumulated results would be used as test-data inputs for an "intelligent" motor-drive condition-monitoring system, where the system would be developed and implemented making use of knowledge of past failures by way of a statistical scheme using concepts based on reliability engineering theory to provide estimates of likelihood of impending capacitor failure.

6.4 – References

[1] W. Leonhard, Control of Electrical Drives, Berlin, Germany: Springer, 1996.

[2] R. Dorf and R. Bishop, Modern Control Systems, Upper Saddle River, NJ, United States of America: Prentice Hall, 2017.

[3] P. Vas, Sensorless Vector and Direct Torque Control, Oxford, United Kingdom: Oxford University Press, 1998.

[4] P. Horowitz and W. Hill, The Art of Electronics, New York, NY, United States of America: Cambridge University Press, 2016.

[5] B. K. Bose, Power Electronics and Variable Frequency Drives, Piscataway, NJ, United States of America: IEEE Press, 1997.

[6] B. K. Bose, Power Electronics and Motor Drives: Advances and Trends, Burlington, MA, United States of America: Elsevier, 2006.

[7] P. Wheeler, J. Rodriguez, J. Clare, L. Empringham and A. Weinstein, “Matrix converters: a technology review,” *IEEE Transactions on Industrial Electronics,* vol. 49, no. 2, pp. 276-288, 2002.

[8] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran and P. Tavner, “An Industry-Based Survey of Reliability in Power Electronic Converters,” *IEEE Transactions on Industry Applications,* vol. 47, no. 3, pp. 1441-1451, 2011.

[9] P. Tavner, L. Ran, J. Penman and H. Sedding, Condition Monitoring of Rotating Electrical Machines, London, United Kingdom: The Institution of Engineering and Technology, 2008.

[10] S. Nandi, H. Toliyat and X. Li, “Condition Monitoring and Fault Diagnosis of Electrical Motors - A Review,” *IEEE Transactions on Energy Conversion,* vol. 20, no. 4, pp. 719-729, 2005.

[11] M. Eleffendi and C. Johnson, “In-Service Diagnostics for Wire-Bond Lift-off and Solder Fatigue of Power Semiconductor Packages,” *IEEE Transactions on Power Electronics,* vol. 32, no. 9, pp. 7187-7198, 2017.

[12] M. Gleissner and M. Bakran, “Identification of module condition (degradation) by means of an on-line Tj-monitor during converter operation,” ECPE, Bayreuth, Germany, 2021.

[13] M. Gasperi, “Life prediction modeling of bus capacitors in AC variable-frequency drives,” *IEEE Transactions on Industry Applications,* vol. 41, no. 6, pp. 1430-1435, 2005.

[14] H. Wang and F. Blaabjerg, “Reliability of Capacitors for DC-Link Applications in Power Electronic Converters - An Overview,” *IEEE Transactions on Industry Applications,* vol. 50, no. 5, pp. 3569-3578, 2014.

[15] J. Shi, R. Wang, M. Xian and T. Wo, “A Cloud-edge Collaborative Architecture for Data-driven Health Condition Monitoring of Machines,” in *2021 IEEE International Conference on Joint Cloud Computing*, Oxford, United Kingdom, 2021.

[16] C. Bhargava, P. Sharma, M. Senthilkumar, S. Padmanaban, V. Ramachandaramurthy, Z. Leonowicz, F. Blaabjerg and M. Mitolo, “Review of Health Prognostics and Condition Monitoring of Electronic Components,” *IEEE Access,* vol. 8, pp. 75163-75183, 2020.

[17] Digital Factory, “MindSphere white paper,” Siemens AG, Plano, TX, United States of America , 2017.

[18] ABB, “Data-driven Maintenance Planning for Variable Speed Drives,” *Bodo's Power Systems,* pp. 30-33, July 2020.

[19] P. Evans and M. Annunziata, “Industrial Internet: Pushing the Boundaries of Minds and Machines,” General Electric Co., 2012.

[20] Oracle Cloud, “Driving Real-Time Insight: The Convergence of Big Data and the Internet of Things,” Oracle, 2016.

[21] A. Raqib, H. Jahanger, M. Sumner, T. Cox and C. Klumpner, “Comparison of Frequency Transform Methods for Condition Monitoring of a DC-Link Capacitor,” in *The 10th International Conference on Power Electronics, Machines and Drives*, Nottingham, United Kingdom, 2020.

[22] W. Sarjeant, J. Zirnheld and F. MacDougall, “Capacitors,” *IEEE Transactions on Plasma Science,* vol. 26, no. 5, pp. 1368-1392, 1998.

[23] J. Kolar, U. Drofenik, J. Biela, M. Heldwein, H. Ertl, T. Friedli and S. Round, “PWM Converter Power Density Barriers,” *IEEJ Journal of Industry Applications ,* vol. 128, no. 4, pp. 468-480, 2008.

[24] “Military Handbook - Reliability Prediction of Electronic Equipment,” Department of Defense, Washington DC, United States of America, 1991.

[25] S. Parler, “Improved Spice models of aluminum electrolytic capacitors for inverter applications,” *IEEE Transactions on Industry Applications,* vol. 39, no. 4, pp. 929-935, 2003.

[26] P. Deeley, Electrolytic Capacitors, Plainfield, NJ, United States of America: The Cornell-Dubilier Electric Corp., 1938.

[27] Nichicon, “General Descriptions of Electrolytic Capacitors,” Nichicon Corporation, Kyoto, Japan, 2019.

[28] TDK, “Aluminium electrolytic capacitors - General technical information,” TDK Electronics AG, Szombathely, Hungary, 2019.

[29] Device Solutions Business Division, “Technical Guide - Aluminium Electrolytic Capacitor,” Panasonic, Osaka, Japan, 2019.

[30] H. Chen and B. Ou, “Effects of trace silver on etching of aluminum electrolytic capacitor foil,” *Journal of Materials Science: Materials in Electronics,* vol. 15, pp. 297-301, 2004.

[31] A. Amaral and A. Cardoso, “Condition monitoring of electrolytic capacitors,” *International Journal of System Assurance Engineering and Management,* vol. 2, no. 4, pp. 352-332, 2011.

[32] TDK, “B43547 Material Data Sheet,” TDK Electronics AG, Szombathely, Hungary, 2019.

[33] National Center for Biotechnology Information, USA, “Ethylene Glycol,” [Online]. Available: https://pubchem.ncbi.nlm.nih.gov/source/hsdb/5012. [Accessed May 2020].

[34] A. Shrivastava, Reliability Evaluation of Liquid and Polymer Aluminium Electrolytic Capacitors, College Park, MD, United States of America: University of Maryland, 2014.

[35] R. Alwitt and R. Hills, “The Chemistry of Failure of Aluminum Electrolytic Capacitors,” *IEEE Transactions on Parts, Materials and Packaging,* vol. 1, no. 2, pp. 28-34, 1965.

[36] TDK, “Aluminium electrolytic capacitors - B43547,” TDK Electronics AG, Szombathely, Hungary, 2019.

[37] K. Harada, A. Katsuki and M. Fujiwara, “Use of ESR for deterioration diagnosis of electrolytic capacitor,” *IEEE Transactions on Power Electronics,* vol. 8, no. 4, pp. 355-361, 1993.

[38] P. Sundararajan, M. Sathik, F. Sasongko, C. Tan, M. Tariq and R. Simanjorang, “Online Condition Monitoring System for DC-Link Capacitor in Industrial Power Converters,” *IEEE Transactions on Industry Applications,* vol. 54, no. 5, pp. 4775-4785, 2018.

[39] A. Lasia, Electrochemical Impedance Spectroscopy and its Applications, New York City, NY, United States of America: Springer, 2014.

[40] J. Macdonald and E. Barsoukov, Impedance Spectroscopy: Theory, Experiment, and Applications, Hoboken, NJ, United States of America: John Wiley & Sons, 2005.

[41] N. Murer, J. Diard and B. Petrescu, “The effects of time-variance on impedance measurements: examples of a corroding electrode and a battery cell,” *Journal of Electrochemical Science and Engineering,* vol. 10, no. 2, pp. 127-140, 2020.

[42] J. Macdonald and W. Kenan, “Interface Effects in the Electrical Response of Non-Metallic Conducting Solids and Liquids,” *IEEE Transactions on Electrical Insulation,* vol. 16, no. 2, pp. 65-82, 1981.

[43] J. Macdonald, “Impedance Spectroscopy,” *Annals of Biomedical Engineering,* vol. 20, pp. 289-305, 1992.

[44] A. Fares, C. Klumpner and M. Sumner, “Development of a battery energy loss observer based on improved equivalent circuit modelling,” in *18th European Conference on Power Electronics and Applications*, Karlsruhe, Germany, 2016.

[45] S. Yuan, H. Wu, X. Zhang and C. Yin, “Online estimation of electrochemical impedance spectra for lithium-ion batteries via discrete fractional order model,” in *2013 IEEE Vehicle Power and Propulsion Conference*, Beijing, China, 2013.

[46] J. Stevens, J. Shaffer and J. Vandenham, “The service life of large aluminum electrolytic capacitors: effects of construction and application,” *IEEE Transactions on Industry Applications,* vol. 38, no. 5, pp. 1441-1446, 2002.

[47] A. Imam, D. Divan, R. Harley and T. Habetler, “Electrolytic Capacitor Failure Mechanism Due to Inrush Current,” in *2007 IEEE Industry Applications Annual Meeting*, New Orleans, LA, United States of America, 2007.

[48] W. Lifeng, Z. Shihong, D. Yinyu, G. Yong and P. Wei, “Research on failure analysis method of the key components in SMPS,” in *Prognostics and System Health Managment Conference*, Shenzhen, China, 2011.

[49] Y. Chen, H. Liao and J. Chen, “Life Prediction of Aluminum Electrolytic Capacitors under Normal Operation,” in *2019 IEEE 4th International Future Energy Electronics Conference*, Singapore, 2019.

[50] Y. Rana, S. Banerjee, T. Singh and P. Varde, “Experimental program for physics-of-failure modeling of electrolytic capacitors towards prognostics and health management,” *Life Cycle Reliability and Safety Engineering,* vol. 6, pp. 179-185, 2017.

[51] J. Celaya, C. Kulkarni, S. Saha, G. Biswas and K. Goebel, “Accelerated aging in electrolytic capacitors for prognostics,” in *2012 Proceedings Annual Reliability and Maintainability Symposium*, Reno, NV, United States of America, 2012.

[52] S. Khan, N. Khera, T. Islam and A. Agarwala, “An online method for condition based maintenance of aluminum electrolytic capacitors,” in *2014 Recent Advances in Engineering and Computational Sciences*, Chandigarh, India, 2014.

[53] R. Shukla, M. Ahmad, N. Agarwal and S. Anand, “Accelerated Ageing of Aluminum Electrolytic Capacitor,” in *Proceedings of the 7th National Power Electronics Conference*, Mumbai, India, 2015.

[54] D. Hewitt, J. Green, J. Davidson, M. Foster and D. Stone, “Observation of electrolytic capacitor ageing behaviour for the purpose of prognostics,” in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, Italy, 2016.

[55] G. Hartler, “Parameter Estimation for the Arrhenius Model,” *IEEE Transactions on Reliability,* vol. 35, no. 4, pp. 414-418, 1986.

[56] X. Wang, R. Tallam, A. Shrivastava and G. Morris, “Reliability Test Setup for Liquid Aluminum Electrolytic Capacitor Testing,” in *2019 Annual Reliability and Maintainability Symposium*, Orlando, FL, United States of America, 2019.

[57] S. Narale, A. Verma and S. Anand, “Accelerated Aging Method and Lifetime Evaluation of Aluminum Electrolytic Capacitors for Power Electronic Application,” in *2020 IEEE Energy Conversion Congress and Exposition*, Detroit, MI, United States of America, 2020.

[58] H. Wang, M. Liserre, F. Blaabjerg, P. Rimmen, J. Jacobsen, T. Kvisgaard and J. Landkildehus, "Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 2, no. 1, pp. 97-114, 2014.

[59] P. Venet, F. Perisse, M. El-Husseini and G. Rojat, "Realization of a smart electrolytic capacitor circuit," *IEEE Industry Applications Magazine,* vol. 8, no. 1, pp. 16-20, 2002.

[60] E. Aeloiza, J. Kim, P. Ruminot and P. Enjeti, "A Real Time Method to Estimate Electrolytic Capacitor Condition in PWM Adjustable Speed Drives and Uninterruptible Power Supplies," in *2005 IEEE 36th Power Electronics Specialists Conference*, Dresden, Germany, 2005.

[61] M. Vogelsberger, T. Wiesinger and H. Ertl, "Life-Cycle Monitoring and Voltage-Managing Unit for DC-Link Electrolytic Capacitors in PWM Converters," *IEEE Transactions on Power Electronics,* vol. 26, no. 2, pp. 493-503, 2011.

[62] H. Matsumori, T. Kosaka, N. Matsui, K. Onda, M. Ozawa and K. Toda, "Loss evaluation of aluminum electrolytic capacitor under power electronics converter excitation," in *2020 IEEE Applied Power Electronics Conference and Exposition*, New Orleans, LA, USA, 2020.

[63] H. Jedtberg, G. Buticchi, M. Liserre and H. Wang, "A method for hotspot temperature estimation of aluminum electrolytic capacitors," in *2017 IEEE Energy Conversion Congress and Exposition*, Cincinnati, OH, United States of America, 2017.

[64] P. Sundararajan, M. Halick, M. Sathik, F. Sasongko, T. Seng, P. Yaxin and R. Simanjorang, "Condition Monitoring of Electrolytic Capacitor based on ESR Estimation and Thermal Impedance model using Improved Power Loss Computation," in *2018 International Power Electronics Conference*, Niigata, Japan, 2018.

[65] K. Murthy and R. Bedford, "Transformation between Foster and Cauer equivalent networks," *IEEE Transactions on Circuits and Systems,* vol. 25, no. 4, pp. 239-239, 1978.

[66] J. Davidson, D. Stone and M. Foster, "Required Cauer network order for modelling of thermal transfer impedance," *IET Electronics Letters,* vol. 50, no. 4, pp. 260-261, 2014.

[67] H. Wen, W. Xiao, X. Wen and P. Armstrong, "Analysis and Evaluation of DC-Link Capacitors for High-Power-Density Electric Vehicle Drive Systems," *IEEE Transactions on Vehicular Technology,* vol. 61, no. 7, pp. 2950-2964, 2012.

[68] Y. Yang, K. Ma, H. Wang and F. Blaabjerg, "Instantaneous thermal modeling of the DC-link capacitor in PhotoVoltaic systems," in *2015 IEEE Applied Power Electronics Conference and Exposition*, Charlotte, NC, USA, 2015.

[69] K. Laadjal, M. Sahraoui, A. Cardoso and A. Amarai, “On-line estimation of aluminum electrolytic-capacitor parameters using a modified Prony's method,” in *2017 IEEE 11th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives*, Tinos, Greece, 2017.

[70] K. Laadjal, M. Sahraoui and A. Cardoso, “On-Line Fault Diagnosis of DC-Link Electrolytic Capacitors in Boost Converters Using the STFT Technique,” *IEEE Transactions on Power Electronics,* vol. 36, no. 6, pp. 6303-6312, 2021.

[71] K. Laadjal, F. Bento, I. Jlassi and A. Cardoso, “Online Condition Monitoring of Electrolytic Capacitors in DC-DC Interleaved Boost Converters, Adopting a Model-Free Predictive Controller,” in *2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering*, Florence, Italy, 2021.

[72] K. Lee, M. Kim, J. Yoon, S. Lee and J. Yoo, “Condition Monitoring of DC-Link Electrolytic Capacitors in Adjustable-Speed Drives,” *IEEE Transactions on Industry Applications,* vol. 44, no. 5, pp. 1606-1613, 2008.

[73] X. Pu, T. Nguyen, D. Lee, K. Lee and J. Kim, “Fault Diagnosis of DC-Link Capacitors in Three-Phase AC/DC PWM Converters by Online Estimation of Equivalent Series Resistance,” *IEEE Transactions on Industrial Electronics,* vol. 60, no. 9, pp. 4118-4127, 2013.

[74] T. Nguyen and D. Lee, “Deterioration Monitoring of DC-Link Capacitors in AC Machine Drives by Current Injection,” *IEEE Transactions on Power Electronics,* vol. 30, no. 3, pp. 1126-1130, 2015.

[75] M. Ahmad, N. Agarwal, P. Kumar and S. Anand, “Low-Frequency Impedance Monitoring and Corresponding Failure Criteria for Aluminum Electrolytic Capacitors,” *IEEE Transactions on Industrial Electronics,* vol. 64, no. 7, pp. 5657-5666, 2017.

[76] T. Li, J. Chen, P. Cong, X. Dai, R. Qiu and Z. Liu, “Online Condition Monitoring of DC-Link Capacitor for AC/DC/AC PWM Converter,” *IEEE Transactions on Power Electronics,* vol. 37, no. 1, pp. 865-878, 2022.

[77] T. Kamel, Y. Biletskiy and L. Chang, “Capacitor aging detection for the DC filters in the power electronic converters using ANFIS algorithm,” in *2015 IEEE 28th Canadian Conference on Electrical and Computer Engineering*, Halifax, Canada, 2015.

[78] H. Soliman, H. Wang, B. Gadalla and F. Blaabjerg, “Condition monitoring for DC-link capacitors based on artificial neural network algorithm,” in *2015 IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives*, Riga, Latvia, 2015.

[79] P. Picton, Introduction to Neural Networks, London: Palgrave, 1994.

[80] H. Soliman, H. Wang and F. Blaabjerg, “A Review of the Condition Monitoring of Capacitors in Power Electronic Converters,” *IEEE Transactions on Industry Applications,* vol. 52, no. 6, pp. 4976-4989, 2016.

[81] M. Chow, R. Sharpe and J. Hung, “On the application and design of artificial neural networks for motor fault detection. I,” *IEEE Transactions on Industrial Electronics,* vol. 40, no. 2, pp. 181-188, 1993.

[82] M. Chow, R. Sharpe and J. Hung, “On the application and design of artificial neural networks for motor fault detection. II,” *IEEE Transactions on Industrial Electronics,* vol. 40, no. 2, pp. 189-196, 1993.

[83] H. Nejjari and M. Benbouzid, “Monitoring and diagnosis of induction motors electrical faults using a current Park's vector pattern learning approach,” *IEEE Transactions on Industry Applications,* vol. 36, no. 3, pp. 730-735, 2000.

[84] M. Wishart and R. Harley, “Identification and control of induction machines using artificial neural networks,” in *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*, Toronto, Canada, 1993.

[85] H. Yang, K. Huang and C. Huang, “An ANN based identification and control approach for field-oriented induction motor,” in *1993 2nd International Conference on Advances in Power System Control, Operation and Management*, Hong Kong, China, 1993.

[86] W. Dazhi, W. Zhenlei and G. Shusheng, “Identification and control of induction motor using artificial neural networks,” in *ICEMS'2001. Proceedings of the Fifth International Conference on Electrical Machines and Systems*, Shenyang, China, 2001.

[87] V. Tipsuwanporn, W. Piyarat and C. Tarasantisuk, “Identification and control of brushless DC motors using on-line trained artificial neural networks,” in *Proceedings of the Power Conversion Conference-Osaka 2002*, Osaka, Japan, 2002.

[88] R. Kumar, R. Gupta and A. Bansal, “Identification and Control of PMSM Using Artificial Neural Network,” in *2007 IEEE International Symposium on Industrial Electronics*, Vigo, Spain, 2007.

[89] C. Aggarwal, Neural Networks and Deep Learning, Cham, Switzerland: Springer, 2018.

[90] R. Kalman, “A New Approach to Linear Filtering and Prediction Problems,” *Journal of Basic Engineering,* vol. 82, no. 1, pp. 35-45, 1960.

[91] C. Kulkarni, G. Biswas, X. Koutsoukos, J. Celaya and K. Goebel, “Experimental Studies of Ageing in Electrolytic Capacitors,” in *Annual Conference of the Prognostics and Health Management Society*, Portland, OR, United States of America, 2010.

[92] J. Celaya, C. Kulkarni, G. Biswas and K. Goebel, “Towards Prognostics of Electrolytic Capacitors,” in *AIAA Infotech@Aerospace 2011*, St. Louis, MO, United States of America, 2011.

[93] P. Sundararajan, M. Sathik, F. Sasongko, C. Tan, J. Pou, F. Blaabjerg and A. Gupta, “Condition Monitoring of DC-Link Capacitors using Goertzel Algorithm for Failure Precursor Parameter and Temperature Estimation,” *IEEE Transactions on Power Electronics,* vol. 35, no. 6, pp. 6386-6396, 2020.

[94] G. Goertzel, “An Algorithm for the Evaluation of Finite Trigonometric Series,” *The American Mathematical Monthly,* vol. 65, no. 1, pp. 34-35, 1958.

[95] M. Gasperi and N. Gollhardt, “Heat transfer model for capacitor banks,” in *Conference Record of 1998 IEEE Industry Applications Conference*, St. Louis, MO, United States of America, 1998.

[96] F. Hayatee, “Heat Dissipation and Ripple Current Rating in Electrolytic Capacitors,” *Electrocomponent Science and Technology,* vol. 2, pp. 109-114, 1975.

[97] S. Narale, P. Kumar, M. Ahmad, A. Verma and S. Anand, “Reliability Comparison of DC Link Capacitor Bank for Different Configurations,” in *2019 IEEE International Conference on Industrial Technology*, Melbourne, Australia, 2019.

[98] C. Lachkar, M. Kadi, J. Kouadio, M. Presle, S. Yousfi, J. Goupy and P. Eudeline, “Failure analysis of aluminum electrolytic capacitors based on electrical and physicochemical characterizations,” in *2017 IEEE International Reliability Physics Symposium*, Monterey, CA, United States of America, 2017.

[99] D. Kececioglu, Reliability Engineering Handbook, Lancaster, PA, United States of America: DEStech Publications, 2002.

[100] A. Goel and R. Graves, “Electronic system reliability: collating prediction models,” *IEEE Transactions on Device and Materials Reliability,* vol. 6, no. 2, pp. 258-265, 2006.

[101] D. Hirschmann, D. Tissen, S. Schroder and R. Doncker, “Reliability Prediction for Inverters in Hybrid Electrical Vehicles,” *IEEE Transactions on Power Electronics,* vol. 22, no. 6, pp. 2511-2517, 2007.

[102] S. Parler, “Deriving Life Multipliers for Electrolytic Capacitors,” *IEEE Power Electronics Society Newsletter,* vol. 16, no. 1, pp. 11-12, 2004.

[103] S. Maddula and J. Balda, “Lifetime of Electrolytic Capacitors in Regenerative Induction Motor Drives,” in *2005 IEEE 36th Power Electronics Specialists Conference*, Dresden, Germany, 2005.

[104] B. Kirisken and H. Ugurdag, “Cost-benefit approach to degradation of electrolytic capacitors,” in *2014 Reliability and Maintainability Symposium*, Colorado Springs, CO, USA, 2014.

[105] N. Khera, S. Khan, T. Islam and A. Agarwala, “An intelligent technique for condition based self-maintenance of aluminum electrolytic capacitors,” *International Journal of System Assurance Engineering and Management,* vol. 7, no. 1, pp. 25-34, 2016.

[106] J. Xue, L. Wang, X. Wei and S. Yang, “Remaining useful life prediction of aluminum electrolytic capacitors used in wind turbines,” in *2017 2nd International Conference Sustainable and Renewable Energy Engineering*, Hiroshima, Japan, 2017.

[107] S. Huang, S. Xiong, D. Zeng, L. Qu, L. Nie and G. Zhu, “Accurate Lifetime Predication of Aluminum Electrolytic Capacitor Considering Equivalent Series Resistance Variations,” in *2018 IEEE International Power Electronics and Application Conference and Exposition*, Shenzhen, China, 2018.

[108] Z. Hao, Y. Liu, J. Gong, M. Huang, Y. Yu, X. Zha and X. Li, “Lifetime Estimation for Aluminum Electrolytic Capacitors in Active Power Filter,” in *2020 IEEE 9th International Power Electronics and Motion Control Conference*, Nanjing, China, 2020.

[109] Z. Ma and A. Krings, “Survival Analysis Approach to Reliability, Survivability and Prognostics and Health Management (PHM),” in *2008 IEEE Aerospace Conference*, Big Sky, MT, United States of America, 2008.

[110] D. Kleinbaum and M. Klein, Survival Analysis, New York, NY, United States of America: Springer, 2012.

[111] “PLECS Standalone,” [Online]. Available: https://www.plexim.com/products/plecs_standalone. [Accessed May 2020].

[112] Motion Control, “Sinamics G120C List Manual,” Siemens AG, Nuremberg, Germany, 2017.

[113] Motion Control, “G120C Power Board Schematic,” Siemens AG, Congleton, United Kingdom, 2014.

[114] Motion Control, “G120X Power Board Schematic,” Siemens AG, Congleton, United Kingdom, 2017.

[115] G. Franklin, D. Powell and M. Workman, Digital Control of Dynamic Systems, Boston, MA, United States of America: Addison-Wesley Longman Publishing Co., Inc., 1997.

[116] A. Vistnes, Physics of Oscillations and Waves, Oslo, Norway: Springer, 2018.

[117] M. Portnoff, “Time-frequency representation of digital signals and systems based on short-time Fourier analysis,” *IEEE Transactions on Acoustics, Speech, and Signal Processing,* vol. 28, no. 1, pp. 55-69, 1980.

[118] A. Abusorrah, The Application of the Continuous Wavelet Transform to Power System Identification and Protection, Nottingham, United Kingdom: University of Nottingham, 2006.

[119] W. Burger and M. Burge, Digital Image Processing, Ithaca, NY, United States of America: Springer, 2016.

[120] L. Cohen, Time-Frequency Analysis, Upper Saddle River, NJ, United States of America: Prentice Hall, 1995.

[121] A. Sinha, Wavelet Transform and ANN Based Fault Diagnosis Scheme for Simultaneous Detection of Broken Rotor Bars and Bearing Damages In Squirrel Cage Induction Motor, Dhanbad, India: Indian Institute of Technology, 2018.

[122] K. Rana and S. Thakur, “Comparisons of wavelets and algorithms based on wavelets and comparing the results with JPEG,” in *International Conference on Energy, Communication, Data Analytics and Soft Computing*, Chennai, India, 2017.

[123] “Continuous Wavelet Transform (CWT),” [Online]. Available: https://pywavelets.readthedocs.io/en/latest/ref/cwt.html. [Accessed May 2020].

[124] “Wavelet Toolbox,” [Online]. Available: https://uk.mathworks.com/products/wavelet.html. [Accessed May 2020].

[125] K. Jia, Impedance based fault location in power distribution systems, Nottingham, United Kingdom: University of Nottingham, 2012.

[126] “Bump Wavelet,” [Online]. Available: https://uk.mathworks.com/help/wavelet/ref/cwtft.html#buu64ch. [Accessed May 2020].

[127] “Complex Morlet Wavelets,” [Online]. Available: https://www.mathworks.com/help/wavelet/ug/wavelet-families-additional-discussion.html. [Accessed July 2021].

[128] H. Jahanger, A Practical Investigation of Wideband Impedance Based Fault Location Technologies, Nottingham, United Kingdom: University of Nottingham, 2019.

[129] K. Jia and B. Liu, “Comparison of system impedance estimating methods,” in *International Conference on Advanced Power System Automation and Protection*, Beijing, China, 2011.

[130] M. Bonamente, Statistics and Analysis of Scientific Data, Huntsville, AL, United States of America: Springer, 2017.

[131] W. Duivesteijn, A. Feelders and A. Knobbe, “Different slopes for different folks: mining for exceptional regression models with cook's distance,” in *Proceedings of the 18th ACM SIGKDD international conference on Knowledge discovery and data mining*, New York, USA, 2012.

[132] R. Cook, “Detection of Influential Observation in Linear Regression,” *Technometrics,* vol. 19, no. 1, pp. 15-18, 1977.

[133] M. Gasperi, “Life prediction model for aluminum electrolytic capacitors,” in *IEEE Industry Applications Conference Thirty-First IAS Annual Meeting*, San Diego, CA, United States of America, 1996.

[134] National Center for Biotechnology Information, USA, “1,2-Ethanediol,” [Online]. Available: https://pubchem.ncbi.nlm.nih.gov/compound/1_2-Ethanediol. [Accessed May 2020].

[135] J. Gross, Mass Spectrometry, Heidelberg, Germany: Springer, 2017.

[136] A. Macchi, G. Moruzzi and F. Pegoraro, Problems in Classical Electromagnetism, Pisa, Italy: Springer, 2017.

[137] W. Demtroder, Mechanics and Thermodynamics, Kaiserslautern, Germany: Springer, 2017.

[138] B. Drury, The Control Techniques Drives and Controls Handbook, London, United Kingdom: The Institution of Engineering and Technology, 2009.

[139] Nippon Chemi-Con, “SMQ Series Specifications,” United Chemi-Con, 2021.

[140] C. Lefrou, P. Fabry and J.-C. Poignet, Electrochemistry, Saint Martin d'Heres Cedex, France: Springer, 2012.

[141] BioLogic, “SP-150,” [Online]. Available: https://www.biologic.net/products/sp-150/. [Accessed May 2020].

[142] P. Kulsangcharoen, C. Klumpner, M. Rashed and G. Asher, “Characterization of energy storage devices for constant power applications,” in *36th Annual Conference on IEEE Industrial Electronics Society*, Glendale, AZ, United States of America, 2010.

[143] P. Kulsangcharoen, C. Klumpner, M. Rashed, G. Asher, G. Chen and S. Norman, “Assessing the accuracy of loss estimation methods for supercapacitor energy storage devices operating under constant power cycling,” in *16th European Conference on Power Electronics and Applications*, Lappeenranta, Finland, 2014.

[144] N4L, “PSM1735 – 10uHz to 35MHz Frequency Response Analyzer,” [Online]. Available: https://www.newtons4th.com/products/frequency-response-analyzers/psm1735-frequency-response-analyzer/. [Accessed May 2020].

[145] Digital Factory, “Sinamics G120 Inverters - PM230 Power Modules, IP55,” Siemens AG, Nurnberg, Germany, 2016.

[146] GW Instek, “APS 7000E,” [Online]. Available: https://www.gwinstek.com/en-GB/products/detail/APS-7000E. [Accessed October 2021].

[147] National Instruments, “cDAQ-9174,” [Online]. Available: https://www.ni.com/en-gb/support/model.cdaq-9174.html. [Accessed April 2021].

[148] National Instruments, “NI-9222,” [Online]. Available: https://www.ni.com/en-gb/support/model.ni-9222.html. [Accessed April 2021].

[149] KiCad, “KiCAD,” [Online]. Available: https://www.kicad.org/. [Accessed October 2021].

[150] TDK, “AlCap Useful Life Calculation Tool - Web-based Application,” TDK Electronics AG, [Online]. Available: https://www.tdk-electronics.tdk.com/en/180482/design-support/design-tools/alcap-useful-life-calculation-tool. [Accessed May 2020].

[151] TDK, “B43547 - Frequency and temperature multipliers,” TDK Electronics AG, Szombathely, Hungary, 2019.

[152] TDK, “Aluminium electrolytic capacitors - Cautions and Warnings,” TDK Electronics AG, Szombathely, Hungary, 2019.

[153] FLIR, “FLIR i3, i5, i7, Extech IRC30 User's manual,” FLIR Systems, Stockholm, Sweden, 2011.

[154] M. Capek, L. Jelinek and P. Hazdra, “On the Functional Relation Between Quality Factor and Fractional Bandwidth,” *IEEE Transactions on Antennas and Propagation,* vol. 63, no. 6, pp. 2787-2790, 2015.

[155] GW Instek, “PSH-Series Programmable Switching D.C. Power Supply,” [Online]. Available: https://www.gwinstek.com/en-global/products/detail/PSH-Series. [Accessed November 2021].

[156] Rohde & Schwarz, “HM8118 LCR Bridge/Meter,” [Online]. Available: https://www.rohde-schwarz.com/uk/product/hm8118-productstartpage_63493-44101.html. [Accessed April 2021].

[157] Pico Technology, “25 MHz 700 V differential oscilloscope probe 10:1/100:1,” [Online]. Available: https://www.picotech.com/accessories/active-differential-high-voltage/25-mhz-700-v-differential-probe. [Accessed October 2021].

[158] Fluke, “Fluke i30s AC/DC Current Clamp,” [Online]. Available: https://www.fluke.com/en-gb/product/accessories/current-clamps/fluke-i30s. [Accessed October 2021].

[159] D. G. Holmes and T. A. Lipo, Pulse Width Modulation For Power Converters, New Jersey, United States of America: IEEE Press, 2003.

[160] Control Techniques, User Guide - Unidrive - Model sizes 1 to 5, Control Techniques Drives Limited, 2003.

[161] Pico Technology, “TC-08 thermocouple data logger,” [Online]. Available: https://www.picotech.com/data-logger/tc-08/thermocouple-data-logger. [Accessed October 2021].

[162] Remington, “Power Dry 2000,” [Online]. Available: https://uk.remington-europe.com/products/d3010-power-dry-2000. [Accessed April 2021].

[163] D. Basic, “Input Current Interharmonics of Variable-Speed Drives due to Motor Current Imbalance,” *IEEE Transactions on Power Delivery,* vol. 25, no. 4, pp. 2797-2806, 2010.

[164] J. Li, M. Sumner, J. Padilla and H. Zhang, “Fault Signal Propagation Through the PMSM Motor Drive Systems,” *IEEE Transactions on Industry Applications,* vol. 53, no. 3, pp. 2915-2924, 2017.

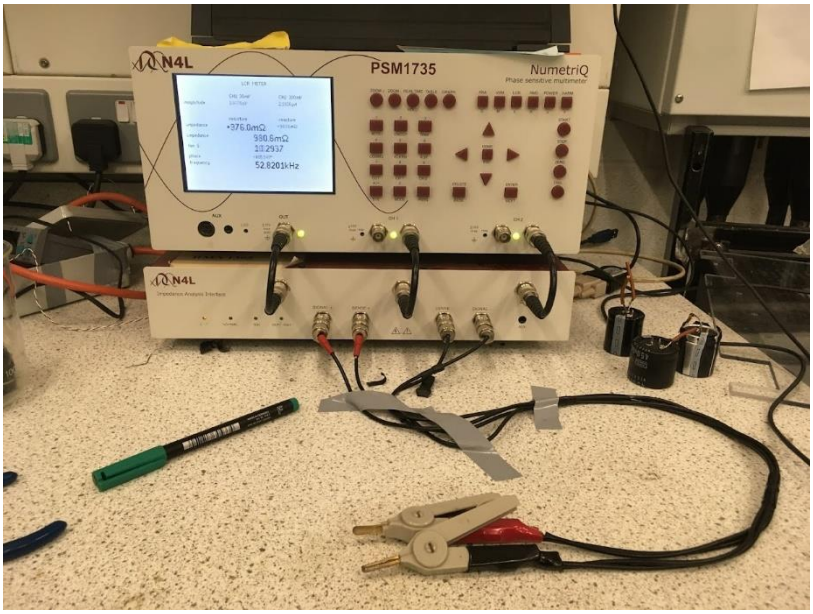
[165] SEMIKRON, “SKiiP 12NAB12T4V1,” [Online]. Available: https://www.semikron.com/products/product-classes/igbt-modules/detail/skiip-12nab12t4v1-25231440.html. [Accessed April 2021].

[166] National Instruments, “NI-9263,” [Online]. Available: https://www.ni.com/en-gb/support/model.ni-9263.html. [Accessed April 2021].

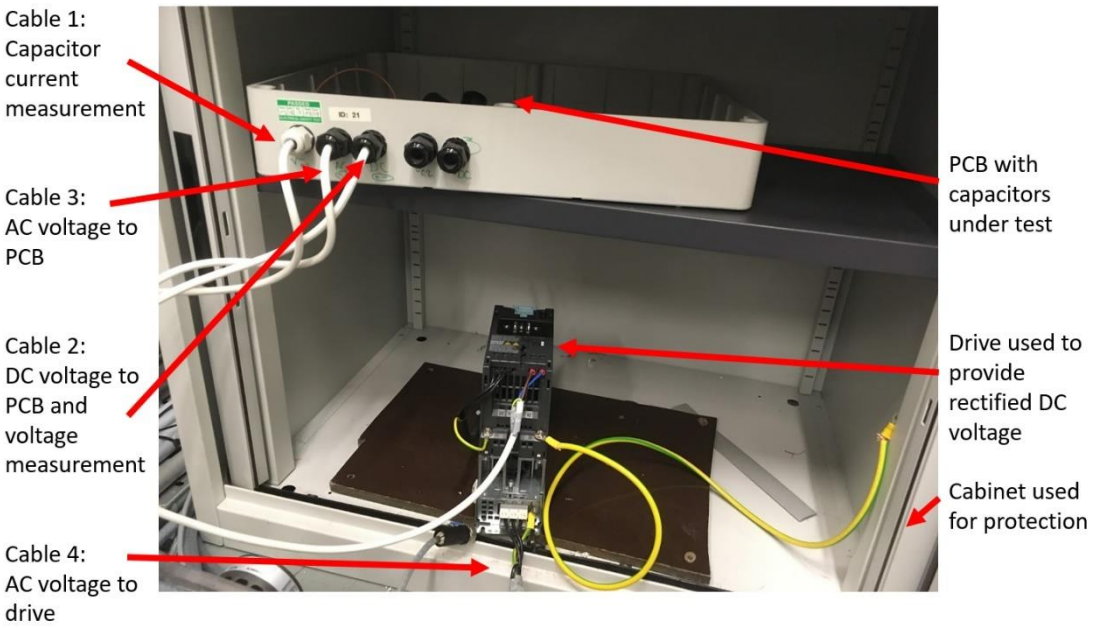
Appendix A



FigA.1 – Biologic SP-150 used in section **3.3.3.1**



FigA.2 – N4L PSM1735 used in section **3.3.3.2**

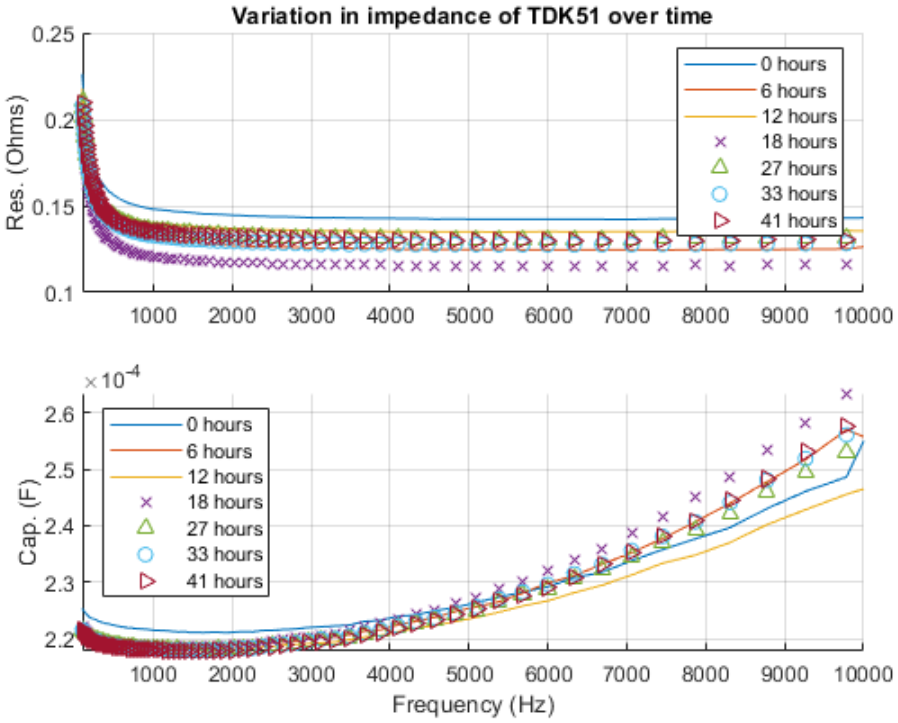


FigA.3 – Test rig used in section **3.4.1**, based on Fig3.21

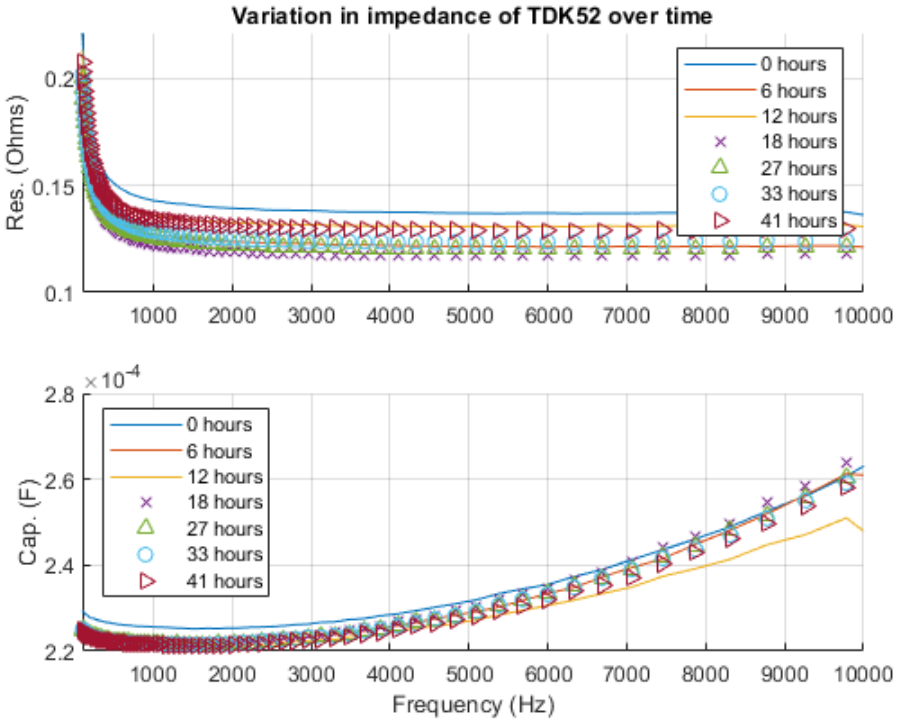


FigA.4 – Rohde & Schwarz HM8118 used in section **3.5.3**

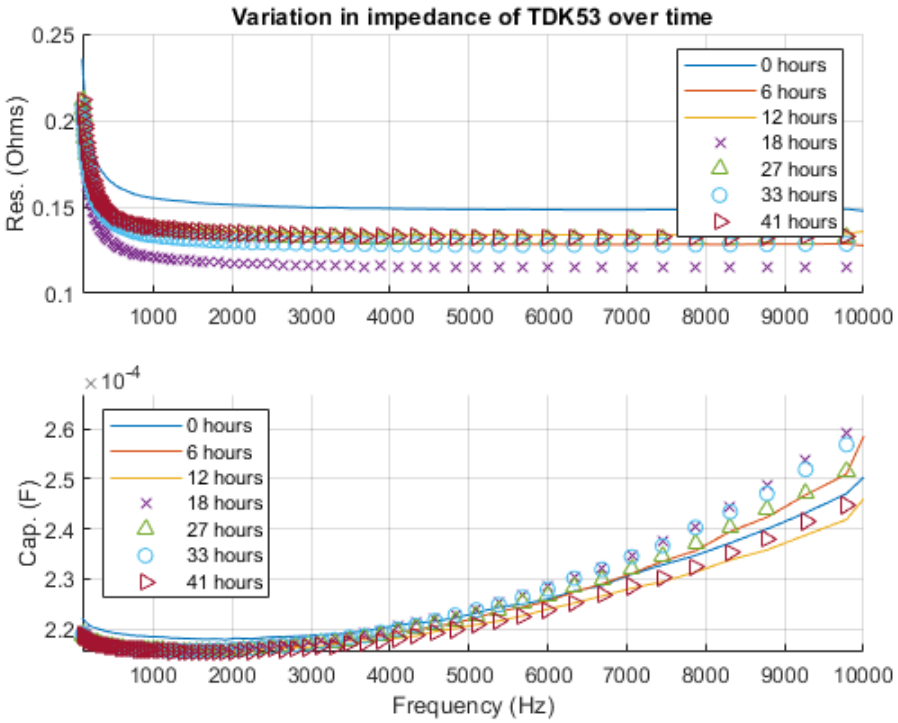
Appendix B



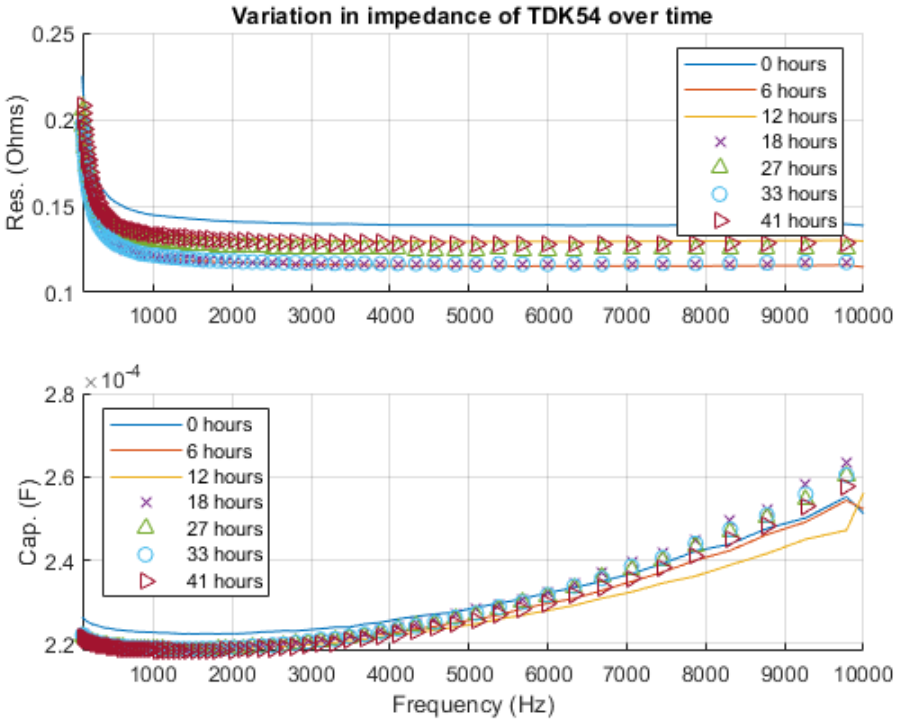
FigB.1 – Variation in impedance of the aged capacitor TDK51 over time



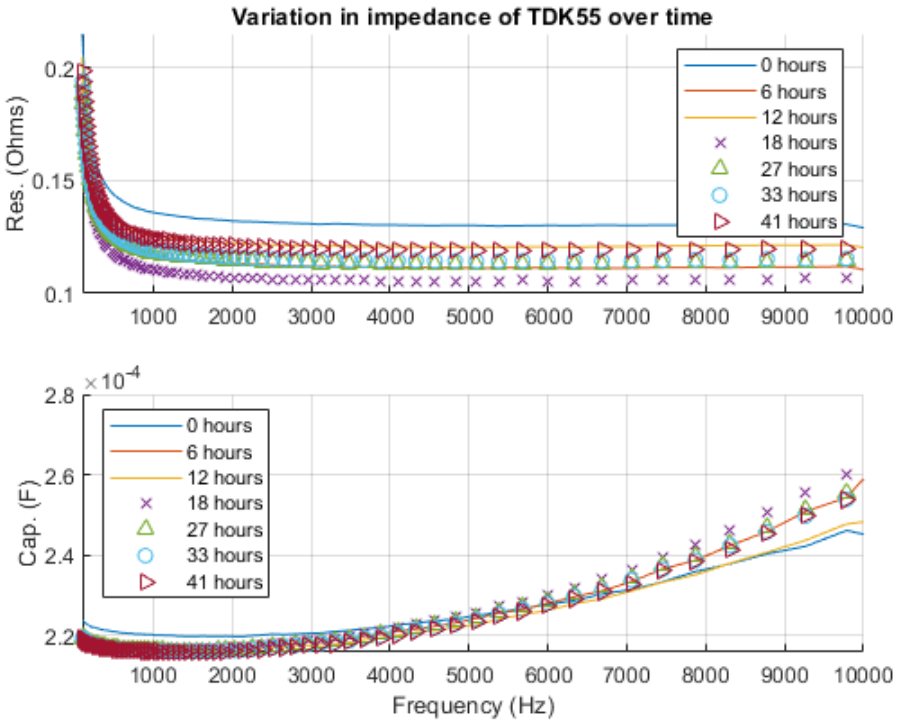
FigB.2 – Variation in impedance of the aged capacitor TDK52 over time



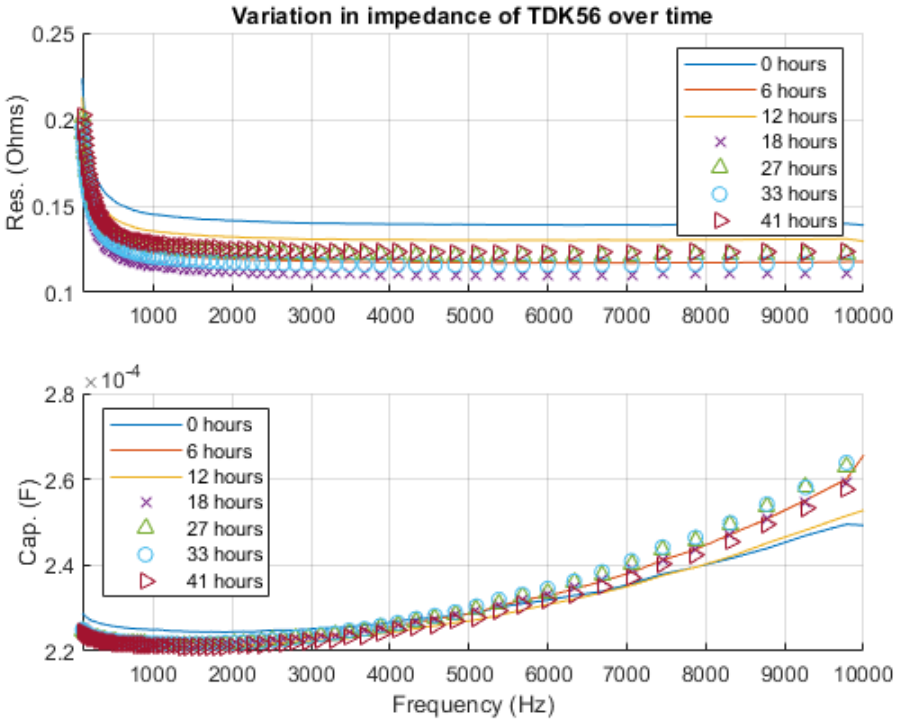
FigB.3 – Variation in impedance of the aged capacitor TDK53 over time



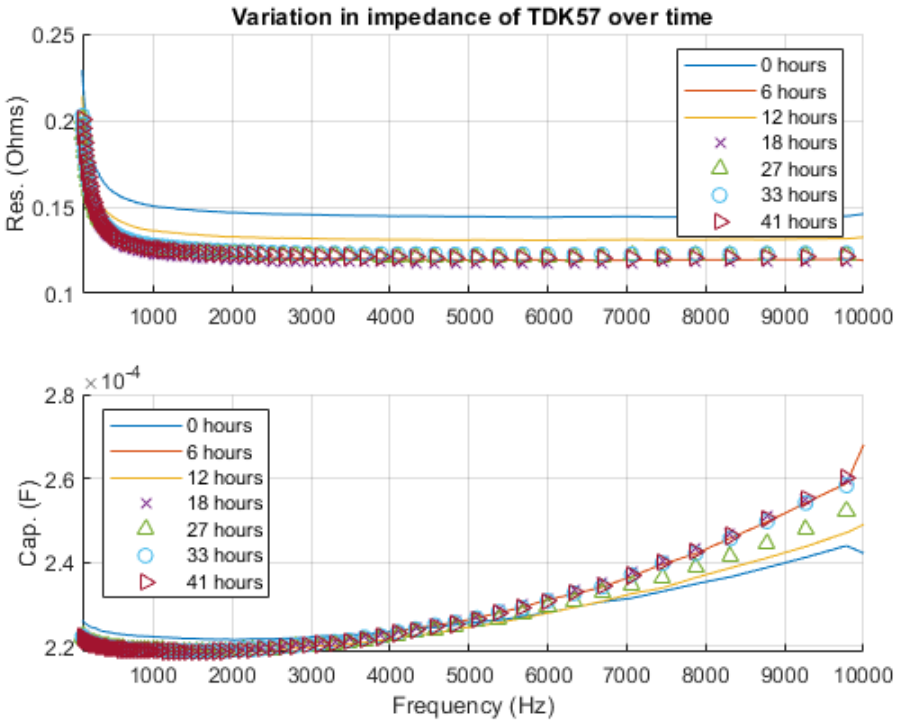
FigB.4 – Variation in impedance of the aged capacitor TDK54 over time



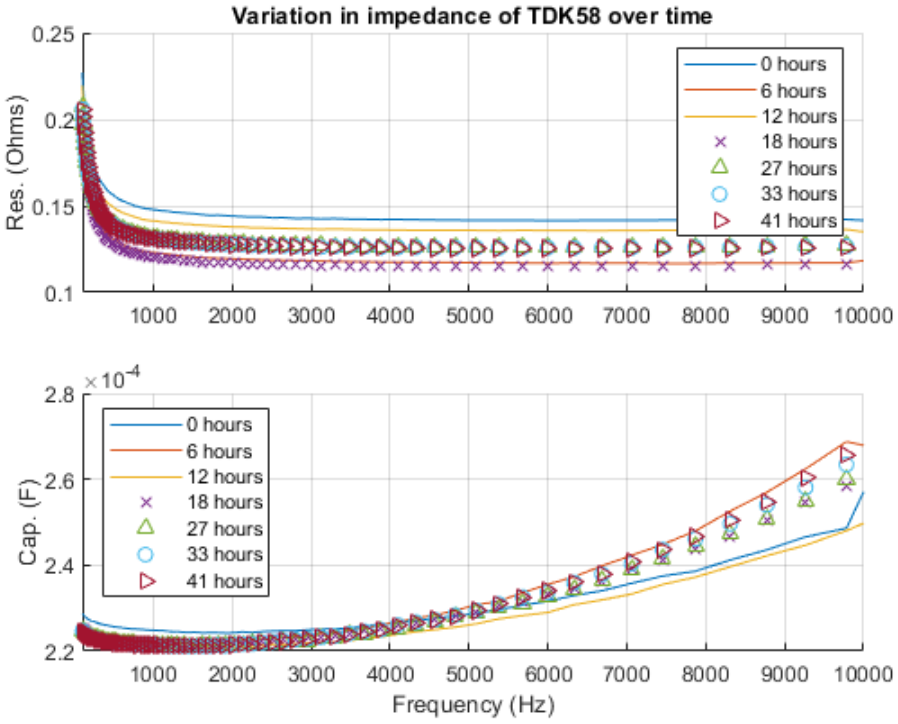
FigB.5 – Variation in impedance of the aged capacitor TDK55 over time



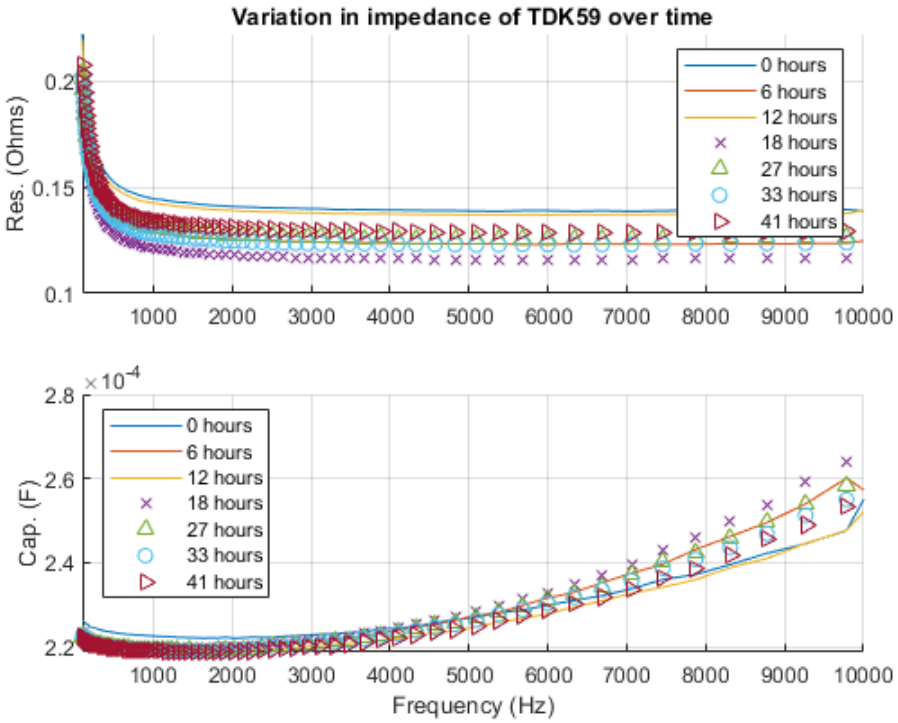
FigB.6 – Variation in impedance of the aged capacitor TDK56 over time



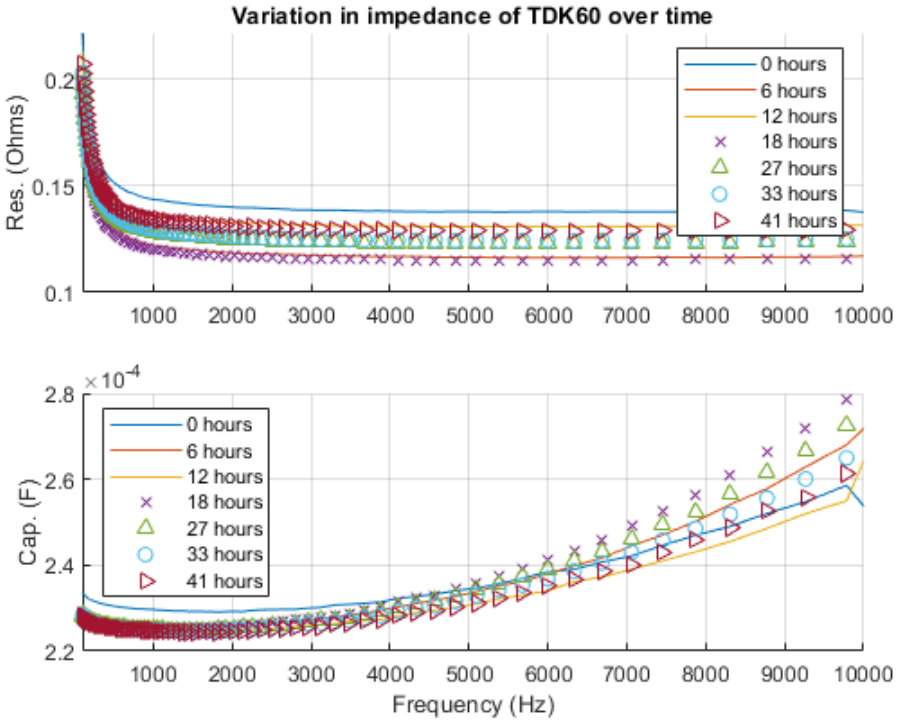
FigB.7 – Variation in impedance of the aged capacitor TDK57 over time



FigB.8 – Variation in impedance of the aged capacitor TDK58 over time



FigB.9 – Variation in impedance of the aged capacitor TDK59 over time



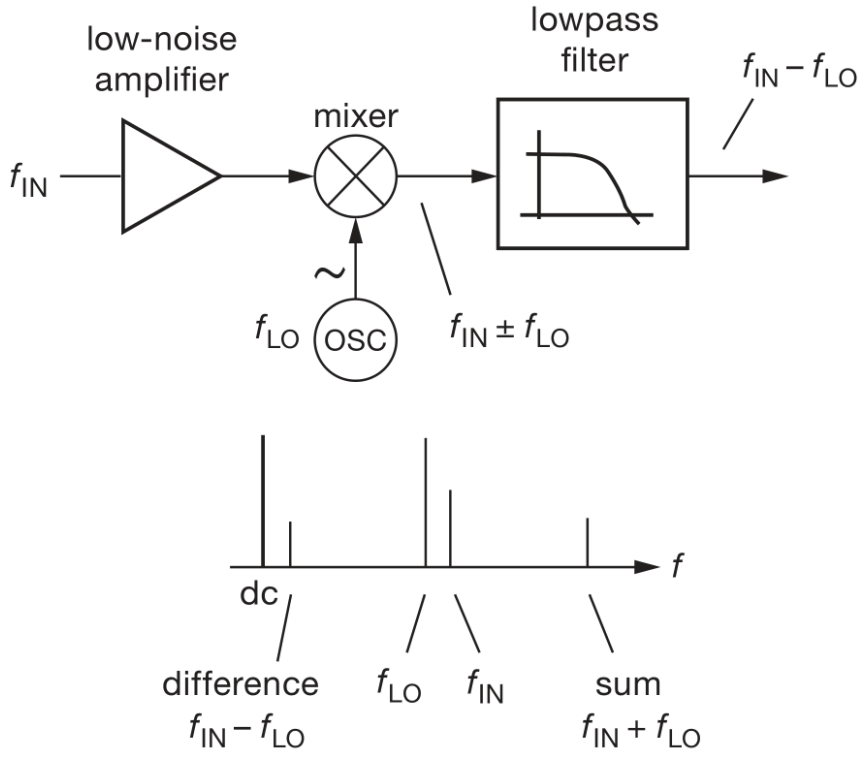
FigB.10 – Variation in impedance of the aged capacitor TDK60 over time

Appendix C

Heterodyning can be summarised as shown in FigC.1, where the diagram is copied from a textbook for illustrative purposes [4]. The diagram shows that if an input frequency is mixed with a local oscillator (LO) provided frequency, the frequency spectrum of the output waveform will cause peaks to arise at sums and differences of the input and LO frequencies. This diagram considers only two frequencies.

In this chapter, (4.3) considered three frequencies: injection, switching, and stator. Without the injection frequency, the input frequency and the LO frequency may be replaced with the stator frequency and the switching frequency, resulting in a normal motor current spectrum with peaks arising at frequencies related to multiples of stator speed. With the injection frequency, the same happens again, except this time with an additional mixer stage to include the injection frequency.

The lowpass filter shown in FigC.1 can be neglected according to which frequencies in the waveform are of interest to the task.



FigC.1 – Heterodyne frequency shifting, copied from [4]

Appendix D

Appendix D.1 – <1kHz range

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	116.57u									
TDK33	116.14u	114.76u								
TDK34	116.86u	114.49u	117.99u							
TDK35	115.51u	113.84u	116.96u	116.9u						
TDK36	115.63u	114.02u	116.96u	117.47u	118.43u					
TDK37	115.01u	113.03u	116.44u	117.05u	116.60u	116.64u				
TDK38	x	x	x	x	x	x	x			
TDK39	115.59u	113.67u	117.10u	117.34u	117.38u	118.21u	117.24u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.1 – Estimated capacitances with 00% load torque, with an injection of 233Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	115.09u									
TDK33	116.32u	115.82u								
TDK34	116.71u	115.39u	118.15u							
TDK35	115.54u	114.60u	116.95u	116.92u						
TDK36	115.65u	114.77u	116.58u	117.26u	118.78u					
TDK37	115.37u	114.17u	116.78u	117.37u	116.58u	116.72u				
TDK38	x	x	x	x	x	x	x			
TDK39	116.06u	115.06u	117.42u	117.64u	117.37u	117.57u	117.58u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.2 – Estimated capacitances with 90% load torque, with an injection of 233Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	115.33u									
TDK33	115.25u	113.97u								
TDK34	116.00u	113.74u	117.61u							
TDK35	114.72u	113.00u	116.31u	116.20u						
TDK36	114.73u	112.95u	115.88u	116.46u	118.13u					
TDK37	114.22u	112.06u	115.70u	116.43u	116.23u	116.10u				
TDK38	x	x	x	x	x	x	x			
TDK39	114.76u	112.76u	116.29u	116.81u	117.11u	117.64u	116.71u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.3 – Estimated capacitances with 00% load torque, with an injection of 487Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	113.24u									
TDK33	115.20u	114.41u								
TDK34	115.74u	114.08u	117.59u							
TDK35	114.39u	113.08u	116.21u	116.01u						
TDK36	114.26u	113.04u	115.38u	116.00u	117.17u					
TDK37	114.34u	112.63u	115.85u	116.54u	116.11u	115.95u				
TDK38	x	x	x	x	x	x	x			
TDK39	114.97u	113.45u	116.43u	116.92u	116.97u	116.88u	116.89u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.4 – Estimated capacitances with 90% load torque, with an injection of 487Hz

Appendix D.2 – 4kHz range

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	112.59u									
TDK33	117.83u	106.90u								
TDK34	119.24u	107.65u	123.63u							
TDK35	116.88u	107.97u	121.16u	121.21u						
TDK36	114.57u	107.98u	120.30u	120.97u	118.79u					
TDK37	117.46u	106.65u	123.27u	122.52u	119.36u	120.68u				
TDK38	94.51u	x	x	x	x	x	x			
TDK39	117.04u	104.82u	124.90u	122.09u	126.59u	123.18u	126.80u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.5 – Estimated capacitances with 00% load torque, local to 4kHz, with no injection

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	113.51u									
TDK33	118.84u	113.81u								
TDK34	120.94u	119.66u	125.39u							
TDK35	125.40u	117.84u	124.31u	123.72u						
TDK36	118.63u	114.51u	121.73u	121.45u	121.15u					
TDK37	116.75u	111.86u	123.74u	136.6u	122.21u	119.47u				
TDK38	x	x	x	x	x	x	x			
TDK39	118.91u	112.05u	127.42u	129.32u	125.84u	126.17u	124.22u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.6 – Estimated capacitances with 90% load torque, local to 4kHz, with no injection

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	113.06u									
TDK33	117.67u	111.07u								
TDK34	118.90u	112.76u	123.33u							
TDK35	117.73u	111.90u	121.23u	122.15u						
TDK36	115.55u	110.80u	119.86u	120.80u	119.50u					
TDK37	115.24u	110.16u	120.56u	120.74u	119.76u	120.50u				
TDK38	x	x	x	x	x	x	x			
TDK39	117.19u	106.42u	123.98u	121.84u	121.16u	122.78u	122.45u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.7 – Estimated capacitances with 00% load torque, local to 4kHz, with an injection of 233Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	111.96u									
TDK33	118.19u	113.33u								
TDK34	118.45u	114.23u	124.44u							
TDK35	117.64u	112.96u	121.29u	122.04u						
TDK36	114.96u	111.49u	118.65u	119.50u	120.16u					
TDK37	115.92u	111.87u	122.5u	122.74u	120.95u	118.43u				
TDK38	x	x	x	x	x	x	x			
TDK39	118.08u	111.68u	124.79u	123.20u	122.76u	121.73u	123.41u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.8 – Estimated capacitances with 90% load torque, local to 4kHz, with an injection of 233Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	114.84u									
TDK33	118.90u	113.93u								
TDK34	119.91u	116.40u	125.44u							
TDK35	119.31u	114.22u	122.31u	124.74u						
TDK36	120.43u	111.87u	122.20u	122.20u	121.66u					
TDK37	117.24u	112.48u	122.14u	123.32u	120.99u	122.86u				
TDK38	x	x	x	x	x	x	x			
TDK39	118.71u	113.24u	125.84u	125.23u	122.75u	124.94u	123.82u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.9 – Estimated capacitances with 00% load torque, local to 4kHz, with an injection of 487Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	112.61u									
TDK33	118.40u	116.91u								
TDK34	120.43u	115.90u	127.61u							
TDK35	118.06u	115.36u	124.70u	122.72u						
TDK36	115.79u	113.23u	120.70u	121.49u	119.96u					
TDK37	117.1u	111.83u	123.06u	125.16u	121.99u	119.78u				
TDK38	x	x	x	x	x	x	x			
TDK39	120.6u	112.32u	128.38u	123.08u	124.37u	122.54u	123.42u	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.10 – Estimated capacitances with 90% load torque, local to 4kHz, with an injection of 487Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	749.60m									
TDK33	627.60m	1173.90m								
TDK34	579.00m	1167.60m	486.09m							
TDK35	567.00m	975.28m	432.80m	419.34m						
TDK36	689.64m	1050.90m	636.98m	595.02m	419.38m					
TDK37	647.58m	990.56m	500.00m	484.84m	442.82m	661.45m				
TDK38	322.22m	x	x	x	x	x	x			
TDK39	692.54m	1152.60m	503.91m	468.27m	452.17m	683.03m	493.52m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.11 – Estimated resistances with 00% load torque, local to 4kHz, with no injection

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	578.50m									
TDK33	475.10m	625.23m								
TDK34	458.11m	554.15m	360.55m							
TDK35	384.11m	486.74m	354.63m	317.21m						
TDK36	414.55m	525.47m	471.17m	416.28m	214.18m					
TDK37	485.1m	618.92m	382.07m	369.92m	355.67m	488.10m				
TDK38	x	x	x	x	x	x	x			
TDK39	462.41m	605.41m	369.63m	344.68m	334.42m	483.58m	400.42m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.12 – Estimated resistances with 90% load torque, local to 4kHz, with no injection

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	633.86m									
TDK33	589.15m	963.68m								
TDK34	558.94m	931.87m	417.73m							
TDK35	484.27m	763.77m	416.71m	377.63m						
TDK36	586.33m	861.08m	584.79m	532.62m	334.65m					
TDK37	602.19m	890.15m	471.63m	446.3m	421.92m	607.56m				
TDK38	x	x	x	x	x	x	x			
TDK39	601.63m	947.82m	458.17m	422.46m	401.76m	586.78m	448.59m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.13 – Estimated resistances with 00% load torque, local to 4kHz, with an injection of 233Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	625.93m									
TDK33	511.02m	682.21m								
TDK34	479.23m	656.28m	387.02m							
TDK35	402.20m	523.75m	370.46m	331.36m						
TDK36	437.83m	566.16m	502.97m	439.43m	232.27m					
TDK37	511.89m	671.77m	398.98m	386.04m	370.80m	512.56m				
TDK38	x	x	x	x	x	x	x			
TDK39	486.99m	658.65m	384.78m	361.63m	348.70m	502.44m	415.92m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.14 – Estimated resistances with 90% load torque, local to 4kHz, with an injection of 233Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	546.44m									
TDK33	525.93m	748.62m								
TDK34	506.66m	717.46m	376.55m							
TDK35	414.76m	590.21m	381.99m	344.89m						
TDK36	491.52m	680.25m	515.45m	468.67m	277.13m					
TDK37	537.65m	733.30m	429.44m	407.48m	382.80m	537.90m				
TDK38	x	x	x	x	x	x	x			
TDK39	528.89m	743.76m	421.29m	389.53m	370.64m	520.18m	414.44m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.15 – Estimated resistances with 00% load torque, local to 4kHz, with an injection of 487Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	611.00m									
TDK33	495.51m	644.00m								
TDK34	463.07m	605.68m	367.42m							
TDK35	396.23m	508.57m	360.04m	326.57m						
TDK36	436.76m	557.87m	481.18m	429.52m	245.12m					
TDK37	496.11m	639.17m	389.39m	375.64m	361.52m	495.64m				
TDK38	x	x	x	x	x	x	x			
TDK39	472.82m	622.66m	377.63m	355.67m	341.50m	483.32m	390.29m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.16 – Estimated resistances with 90% load torque, local to 4kHz, with an injection of 487Hz

Appendix D.3 – 8kHz range

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	738.01m									
TDK33	620.86m	1158.10m								
TDK34	569.53m	1153.80m	481.17m							
TDK35	561.00m	963.44m	429.58m	416.83m						
TDK36	681.44m	1037.90m	631.27m	587.62m	414.35m					
TDK37	641.24m	978.70m	496.45m	481.79m	439.34m	655.91m				
TDK38	307.81m	x	x	x	x	x	x			
TDK39	683.65m	1132.20m	501.79m	464.39m	450.05m	673.36m	489.78m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.17 – Estimated resistances with 00% load torque, local to 8kHz, with no injection

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	568.89m									
TDK33	473.53m	618.03m								
TDK34	459.30m	549.96m	368.10m							
TDK35	389.42m	484.70m	362.70m	326.82m						
TDK36	415.41m	519.00m	470.14m	420.90m	225.81m					
TDK37	483.81m	612.64m	388.81m	377.93m	362.03m	492.16m				
TDK38	x	x	x	x	x	x	x			
TDK39	463.29m	598.02m	379.32m	353.58m	342.38m	485.51m	401.28m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.18 – Estimated resistances with 90% load torque, local to 8kHz, with no injection

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	623.05m									
TDK33	583.83m	951.45m								
TDK34	552.25m	921.45m	417.61m							
TDK35	480.22m	754.00m	416.09m	377.64m						
TDK36	578.74m	849.24m	580.25m	529.08m	334.60m					
TDK37	595.23m	878.79m	468.93m	445.40m	420.07m	602.05m				
TDK38	x	x	x	x	x	x	x			
TDK39	596.38m	931.09m	458.81m	422.99m	402.44m	581.86m	447.04m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.19 – Estimated resistances with 00% load torque, local to 8kHz, with an injection of 233Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	615.17m									
TDK33	508.35m	674.57m								
TDK34	476.61m	651.46m	391.64m							
TDK35	404.55m	517.45m	375.73m	338.02m						
TDK36	433.19m	557.28m	500.21m	440.61m	242.05m					
TDK37	506.22m	662.88m	402.32m	390.28m	371.70m	512.62m				
TDK38	x	x	x	x	x	x	x			
TDK39	485.13m	647.94m	390.07m	366.39m	355.23m	501.56m	414.84m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.20 – Estimated resistances with 90% load torque, local to 8kHz, with an injection of 233Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	536.44m									
TDK33	521.93m	736.94m								
TDK34	500.21m	710.48m	378.72m							
TDK35	413.08m	581.14m	382.89m	348.87m						
TDK36	486.53m	669.74m	512.10m	465.5m	280.52m					
TDK37	530.26m	723.41m	428.62m	407.59m	382.59m	534.21m				
TDK38	x	x	x	x	x	x	x			
TDK39	524.61m	729.83m	423.13m	390.43m	371.86m	516.52m	414.81m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.21 – Estimated resistances with 00% load torque, local to 8kHz, with an injection of 487Hz

	TDK31	TDK32	TDK33	TDK34	TDK35	TDK36	TDK37	TDK38	TDK39	TDK40
TDK31										
TDK32	602.74m									
TDK33	492.65m	636.89m								
TDK34	461.09m	600.08m	372.81m							
TDK35	395.97m	503.80m	364.98m	333.34m						
TDK36	435.37m	548.53m	478.86m	430.67m	252.70m					
TDK37	490.30m	631.61m	391.85m	379.77m	365.70m	495.95m				
TDK38	x	x	x	x	x	x	x			
TDK39	471.37m	613.33m	383.97m	360.33m	346.89m	484.03m	391.73m	x		
TDK40	x	x	x	x	x	x	x	x	x	

TableD4.22 – Estimated resistances with 90% load torque, local to 8kHz, with an injection of 487Hz