A Modular Isolated AC/AC Matrix Converter

Usman Nasir, B.Sc., M.Sc.

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To my mother

- for her unconditional and immeasurable love -

Abstract

With the advancements in the semiconductor device technologies and computational power, the Solid State Transformer (SST) has emerged as a key research topic due to potential benefits in power density and controllability when compared to line-frequency transformers. However, in the applications where the power density is a key priority, for example traction and space limited grid applications, the conventional AC to AC SST solution is not suitable because the DC-link capacitors put a constraint on further improvements in the power density. A compact single-stage AC to AC SST solution can be achieved by eliminating the intermediate DC-link stages.

This thesis investigates the feasibility of a new single-stage AC to AC SST based three-phase Modular Isolated Matrix Converter (MIMC) topology. The MIMC topology, proposed in this thesis, is obtained by using single-phase Medium Frequency (MF) isolated AC to AC converters as a cell. The arrangement of the cells in the MIMC is derived from the concept of the Direct Matrix Converter. The MIMC achieves structural modularity due to the repetition of the single-phase isolated AC to AC converters. The modularity within the converter is advantageous in terms of hardware implementation, maintenance and it also opens up possibilities of stacking cells based on the required power level. However, as each cell in the MIMC is isolated via a MF transformer, this causes challenges in modulation and commutation.

In this thesis, both scalar and vector type of modulation methods are developed respecting the presence of MF transformers in the MIMC. The standard commutation approach which assumes voltage source at one side and current source at the other is no longer applicable in the presence of practical transformers with non-negligible leakage inductance. Therefore, a leakage tolerant current commutation method which guarantees safe current commutation, without an auxiliary clamp circuit or high band-width measurements, is also proposed. The proposed commutation method is experimentally validated on a single cell and then applied along with the Venturini Modulation method to the MIMC. The experimental results from a 6kW proof of concept prototype validate the proposed operating modes and feasibility of the MIMC.

Thesis Contribution

This thesis has resulted in two journal and three conference paper publications. The published papers are as listed:

1. U. Nasir, A. Costabeber, P. Wheeler, M. Rivera and J. Clare, "A Three-Phase Modular Isolated Matrix Converter," in IEEE Transactions on Power Electronics, vol. 34, no. 12, pp. 11760-11773, Dec. 2019.

2. U. Nasir, A. Costabeber, M. Rivera, P. Wheeler and J. Clare, "A Leakage-Inductance-Tolerant Commutation Strategy for Isolated AC/AC Converters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 1, pp. 467-479, March 2019.

3. U. Nasir, M. Rivera, A. Costabeber and P. Wheeler, "A Venturini based modulation technique for a new isolated AC/AC power converter," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 6243-6248.

4. U. Nasir, A. Costabeber, P. Wheeler and M. Rivera, "A new AC/AC power converter," 2017 IEEE Southern Power Electronics Conference (SPEC), Puerto Varas, 2017, pp. 1-6.

5. U. Nasir, M. Rivera, S. Toledo, A. Costabeber and P. Wheeler, "A review of power converter topologies with medium/high frequency transformers for grid interconnection systems," 2016 IEEE International Conference on Automatica (ICA-ACCA), Curico, 2016, pp. 1-8.

6. M. Rivera, S. Toledo, U. Nasir, A. Costabeber and P. Wheeler, "New configurations of power converters for grid interconnection systems," 2016 IEEE International Conference on Automatica (ICA-ACCA), Curico, 2016, pp. 1-8.

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List of Terms

Abbreviations

SCR	Silicon Controlled Rectifier
MOSFET	Metal Oxide Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
SiC	Silicon Carbide
GaN	Galium Nitride
LV	Low Voltage
MV	Medium Voltage
SST	Solid State Transformer
PET	Power Electronic Transformer
MF	Medium Frequency
HF	High Frequency
MIMC	Modular Isolated Matrix Converter
PR	Proportional Resonant
MPC	Model Predictive Control
M2PC	Modulated Model Predictive Control
DAB	Dual Active Bridge
CBM	Cycloconverter Based Module
MS	Modulation State
VM	Venturini Modulation
DVM	Double Venturini Modulation
DOVM	Double Optimum Venturini Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion

FFT	Fast Fourier Transform
2QSH-bridge	Two Quadrant Switches based H-Bridge
4QSH-bridge	Four Quadrant Switches based H-Bridge
CS	Commutation State
FSM	Finite State Machine
FPGA	Field-Programmable Gate Array
VHDL	VHSIC Hardware Description Language
PCB	Printed Circuit Board
DSP	Digital Signal Processor
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
RMS	Root Mean Square
PLL	Phase-Locked Loop
VCO	Voltage Controlled Oscillator

Nomenclature

MS_{Kij}	Input bridge modulation state matrix
MS_{Koj}	Output bridge modulation state matrix
f_i	Input frequency
f_o	Output frequency
D_{Kj}	Duty cycle
V_{Ki}	Three-phase input voltage
V_{jo}	Three-phase output voltage
ϕ_K, φ_K	Phase of the input voltage
ϕ_j	Phase of the output voltage
V_m	Input voltage amplitude
q	Voltage transfer or regulation ratio
f_{sw}	Switching frequency

T_S	Switching period
V_{TKj}	Transformer voltage
A_c	Core area of transformer
${A_c}^{MIN}$	Minimum core area of transformer
B^{MAX}	Maximum flux density of transformer
ω_i	Input frequency in Radians per second
ω_o	Output frequency in Radians per second
ω_s	Switching frequency in radian per second
V_{Koj}	Cell output voltage
I_{jo}	Three-phase output current
I_{Ki}	Three-phase input current
Z_{load}	Load impedance
ϕ_o	Load angle
R	Load resistance
L	Load inductance
I_{Kij}	Cell input current
$\bar{\mathbf{v}}_{\mathbf{o}}$	Output voltage vector
$\bar{\mathbf{I}}_{\mathbf{i}}$	Input current vector
$\bar{\mathbf{v}}_{\mathbf{o_rotating}}$	Rotating output voltage vector
r_1	Radius of inner hexagon vectors
r_2	Radius of outer hexagon vectors
α_o	Output voltage vector angle
β_i	Input current vector angle
Z	Zero output voltage vector
$\hat{\alpha}_o$	Angle from sector's bisecting line to output voltage vector
K_v	Output voltage sector number
δ	Space vector modulation duty cycle
$\hat{\beta}_i$	Angle from sector's bisecting line to input current vector

K_i	Input current sector number
φ_i	Input power factor angle
T_{comm}	Commutation step
T_{OFF}	Semiconductor turn-OFF time
T_{ON}	Semiconductor turn-ON time
L_{leak}	Transformer leakage inductance
I_L	Leakage inductance current
I_{out}	Output current
I_{out}	Output voltage
V_{in}	Input voltage
V_{PK}	Peak of the voltage spike
V_T	Transformer voltage
C_{clp}	Clamp capacitor
V_{clp}	Clamp capacitor voltage
V_{clp1}	Input clamp capacitor voltage
V_{clp2}	Output clamp capacitor voltage
R_{clp}	Clamp circuit resistance
I_{clp}	Clamp circuit current
L_o	Load inductance
V_{in}^{MIN}, V_{TH}	Minimum input voltage for safe commutation
I_{out}^{MAX}	Peak output current
CS_i	Input bridge commutation state matrix
CS_o	Output bridge commutation state matrix
V_{in}^{MAX}	Peak input voltage
V_{clp}^{MAX}	Maximum clamp capacitor voltage
V_{igbt}^{MAX}	IGBT rated voltage
V_{rec_h}	Half-wave rectified voltage
V_{rec}	Full-wave rectified voltage

V_{th}	Voltage threshold detector circuit voltage
V_{dir}	Current direction detector circuit voltage
$s(t)$	Periodic square wave function
$\Phi_{TK}(t)$	Transformer flux
${\Phi_{TK}}^{MAX}$	Maximum transformer flux
C_F	Input filter capacitor
S	State change variable
T_n	Commutation timer
$Q(t)$	Clamp capacitor charge
$E(t)$	Energy lost per commutation
$\bar{P}(t)$	Average power loss per switching period
I_{ao_open}	Open-loop output current
$G_{PR}(s)$	PR controller s-domain transfer function
I_{ao_PR}	Output current with PR controller
$G_{PR}(z)$	PR controller z-domain transfer function
I_{ao_ref}	Output reference current
$I_{ao_err_lin}$	Output current error with PR controller
g_{Aa}, g_{Ba}, g_{Ca}	Model predictive control cost functions
D_{Aa}^{lin}, D_{Ba}^{lin}, D_{Ca}^{lin}	Linear duty cycles
D_{Aa}^{n-lin},D_{Ba}^{n-lin},D_{Ca}^{n-lin}	Non-linear duty cycles
$I_{ao_MPC_n_lin}$	Output current with non-linear M2PC
$I_{ao_MPC_lin}$	Output current with linear M2PC
$I_{ao_err_lin}$	Output current error with non-linear M2PC
$I_{ao_err_n_lin}$	Output current error with linear M2PC
${V_{Ki}}'$	Unbalanced three-phase input voltage
P_1, P_2, P_3	Phases of positive, negative and zero sequences, respectively
K_1, K_2, K_3	Magnitude of positive, negative and zero sequences, respectively
$[M]$	Modulation matrix

$[M']$	Compensation modulation matrix
S_{in}	Input apparent power
α_1, α_2	Constants for controlling the input power factor

Contents

1 Introduction **1**

1.1 Background 1

1.2 Objectives of the Project 5

1.3 Thesis Structure 8

2 Evolution of the Modular Isolated Matrix Converter (MIMC) **10**

2.1 Three-stage AC/DC/DC/AC SST Architecture 11

2.2 Two-stage AC/DC/AC SST Architecture 12

2.3 Single-stage AC/AC SST Architecture 14

2.3.1 A Modular Isolated Matrix Converter (MIMC) 19

2.4 Conclusions 22

3 Modulation Methods **23**

3.1 Introduction 23

3.2 Venturini Modulation 27

3.3 Double Venturini Modulation 44

3.4 Double Optimum Venturini Modulation 53

3.5 Space Vector Modulation 54

3.6 Comparison of the Modulation Methods 73

3.7 Conclusions 79

4 The Commutation Method **80**

4.1 Introduction and Requirement 80

4.2 Standard 4-Step Current Commutation Method 83

4.2.1 Current Based 4-step Current Commutation Method 83

4.2.2 Voltage Based 4-step Current Commutation Method 86

4.3 Impact of Transformer's Leakage Inductance on Standard 4-step Current Commutation Method 91

4.4 A Source Based Leakage Inductance Tolerant Current Commutation Method 98

4.4.1 Basic Principle 98

4.4.2 Source Based Leakage Tolerant Current Commutation Method For the MIMC 101

4.4.3 Theoretical Commutation Waveforms 108

4.4.4 Commutation Paths 110

4.5 Conclusions 114

5 Experimental Validation of the Commutation Method 115

5.1 Experimental Setup 115

5.1.1 Control Platform 117

5.1.2 4QSH-bridge and Clamp Circuit 118

5.1.3 Gate Driver Board 121

5.1.4 Voltage Polarity and Threshold Detection 122

5.1.5 Current Direction Detector Circuit 124

5.1.6 The Medium Frequency (MF) Transformer 126

5.1.7 Experimental Rig and Prototype 132

5.2 Experimental Results 133

5.2.1 Standard 4-step Current Commutation Method 134

5.2.2 Source Based Leakage Tolerant Current Commutation Method 139

5.3 Comparison of Losses 147

5.3.1 Leakage Inductance Related Losses with Standard 4-step Current Commutation Method 148

5.3.2 Switching Losses with Standard 4-Step Current Commutation Method 150

5.3.3 Switching Losses with Proposed Current Commutation Method 151

5.4 Conclusions 156

6 Experimental Validation and Control of Modular Isolated Matrix Converter (MIMC) 157

6.1 Introduction 157

6.2 Open-loop Validation of the MIMC 162

6.2.1 Simulation Results 162

6.2.2 Experimental Setup and Results 168

6.3 Closed-loop Control of the MIMC 176

6.3.1 Proportional-Resonant (PR) Controller 177

6.3.2 Modulated Model Predictive Control (M2PC) 184

6.4 Conclusions 193

7 An Insight into Reactive Power Capability of the Modular Isolated Matrix Converter (MIMC) 194

7.1 Introduction 194

7.2 Reactive Power Capability 195

7.3 Conclusions 199

8 Conclusions and Future Work **200**

8.1 Future Work 204

8.1.1 Converter Topology Extension For High Voltage 205

8.1.2 Converter Topology Extension For High Current 205

A Schematics **225**

B States for Space Vector Modulation(SVM) **228**

List of Figures

1.1 Architecture of a three-stage AC/AC Solid State Transformer (SST) . 2

1.2 Architecture of a single-stage AC/AC SST 3

1.3 A single-phase AC/AC converter topology based on single-stage SST architecture 4

1.4 A three-phase Modular Isolated AC/AC Matrix Converter (MIMC) based on single-stage SST architecture 6

2.1 Architecture of a three-stage AC/DC/DC/AC SST 11

2.2 Single-phase AC/AC converter topology based on three-stage SST architecture 12

2.3 Architecture of a two-stage AC/DC/AC SST 13

2.4 Single-phase AC/AC converter topology based on two-stage SST architecture 13

2.5 Architecture of a single-stage AC/AC SST 15

2.6 Single-phase AC/AC converter topology based on single-stage SST architecture 16

2.7 Three-phase single-stage SST based AC/AC converter topology with half-bridges at input side [1] 17

2.8 Three-phase single-stage SST based AC/AC converter topology with full-bridges at input side [2] 18

2.9 Three-phase single-stage SST based AC/AC converter topology with reduced switch count [3–5] 19

2.10 A three-phase Modular Isolated AC/AC Matrix Converter (MIMC) based on single-stage SST architecture 20

3.1 A three-phase to three-phase Modular Isolated Matrix Converter (MIMC) 24

3.2 A three-phase to three-phase Direct Matrix Converter 25

3.3 A generalised three-phase to single-phase section of the MIMC 26

3.4 The relationship between the duty cycle of the voltage waveform at MF transformer and the core area A_c of the MF transformer 30

3.5 The arrangement of the duty cycles defined by the Venturini Modulation method 31

3.6 Theoretical voltage waveforms in the top-cell as a result of the Venturini Modulation (a) Input voltage V_{Ai} (b) Transformer voltage V_{TAa} (c) Output voltage V_{Aoa} 32

3.7 A zoomed view of Figure 3.6, focussing on a single switching period T_S (a) Input voltage V_{Ai} (b) Transformer voltage V_{TAa} (c) Output voltage V_{Aoa} 33

3.8 Theoretical voltage waveforms in the three-phase to three-phase MIMC as a result of the Venturini Modulation. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Total output voltage V_{ao}. (e) Phase-phase output voltage V_{ab}. 35

3.9 A single switching period T_S of voltages at the output of MIMC, showing the arrangement of duty cycles D_{Ka}. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Total output voltage V_{ao} of (3.7). 36

3.10 Harmonic spectrum of the cell's output voltage V_{Koa} as a result of the Venturini Modulation 40

3.11 Harmonic spectrum of the final voltage V_{ao} as a result of the Venturini Modulation 41

3.12 Harmonic spectrum of the cell's input current I_{Aij} as a result of the Venturini Modulation 42

3.13 Harmonic spectrum of the total input current I_{Ai} as a result of the Venturini Modulation 42

3.14 Theoretical voltage waveforms in the top-cell as a result of the Double Venturini Modulation: (a) Input voltage V_{Ai}. (b) Transformer voltage V_{TAa}. (d) Output voltage V_{Aoa}. 46

3.15 A zoomed view of Figure 3.14, focussing on a single switching period T_S (a) Input voltage V_{Ai}. (b) Transformer voltage V_{TAa}. (d) Output voltage V_{Aoa}. 47

3.16 Theoretical voltage waveforms in the three-phase to three-phase MIMC as a result of the Double Venturini Modulation. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Output voltage V_{ao}. (e) Phase-phase output voltage V_{ab}. 48

3.17 A single switching period T_S of voltages at the output of MIMC, showing the arrangement of duty cycles D_{Ka}. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Total output voltage V_{ao} of (3.37). 49

3.18 Harmonic spectrum of the cell's output voltage V_{Koa} as a result of the Double Venturini Modulation 50

3.19 Harmonic spectrum of the final voltage V_{ao} as a result of the Double Venturini Modulation 51

3.20 Harmonic spectrum of the cell's input current I_{Aij} as a result of the Double Venturini Modulation 52

3.21 Harmonic spectrum of the total input current I_{Ai} as a result of the Double Venturini Modulation 52

3.22 A generalised three-phase to single-phase MIMC 55

3.23 Space vector representation of the output phase voltages 58

3.24 Fixed direction output voltage vectors 60

3.25 Space vectors diagram showing the 54 fixed direction voltage and current vectors 62

3.26 Output voltage vector $\bar{\mathbf{v}}_\mathbf{o}$ in Sector 1 65

3.27 Input current vector $\bar{\mathbf{I}}_\mathbf{i}$ in Sector 1 68

3.28 Single-sided pattern for a switching period T_S 71

3.29 Theoretical voltage waveforms in the top-cell as a result of SVM method: (a) Input voltage V_{Ai}. (b) Transformer voltage V_{TAa}. (d) Output voltage V_{Aoa}. 72

3.30 Theoretical voltage waveforms in the three-phase to three-phase MIMC as a result of the SVM method. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Phase output voltage V_{ao}. (e) Phase-phase output voltage V_{ab} 72

3.31 Harmonic spectrum of phase output voltage V_{ao} comparing vector modulation method i.e. Space Vector Modulation (SVM) with the equivalent scalar modulation method i.e. the Double Optimum Venturini Modulation (DOVM). 73

3.32 State transitions (per-cell) required for the implementation of the Venturini Modulation method 74

3.33 Commutation sequence in a switching period T_S with the Venturini Modulation method 75

3.34 State transitions (per-cell) required for the implementation of the Double Venturini Modulation or Double Optimum Venturini Modulation method 76

3.35 Commutation sequence in a switching period T_S with the Double Venturini or Double Optimum Venturini Modulation method 76

3.36 Commutation sequence in a switching period T_S (when both current and voltage vectors are in sector 1) with the Space Vector Modulation method 77

3.37 Commutation sequence in a switching period T_S (when both current and voltage vectors are in sector 2) with the Space Vector Modulation method 77

4.1 2QSH-bridge with a current source on AC side and a voltage source on DC side 81

4.2 Timing diagram of the commutation process in 2QSH-bridge 82

4.3 4QSH-bridge with AC current source on output side and AC voltage source on input side 82

4.4 Illustration of steady-states MS_1 and MS_2 84

4.5 Steps in the current based 4-step current commutation method for moving from S_0, S_1, S_2, S_3 ON $(MS_1)$to S_4, S_5, S_6, S_7 ON (MS_2) when $I_{out} > 0$ 85

4.6 Steps in the voltage based 4-step current commutation method for moving from S_0, S_1, S_2, S_3 ON (MS_1) to S_4, S_5, S_6, S_7 ON (MS_2) when $V_{in} > 0$ 87

4.7 Timing diagrams of current and voltage based 4-step commutation process in 4QSH-bridge for moving from S_0, S_1, S_2, S_3 ON (MS_1) to S_4, S_5, S_6, S_7 ON (MS_2) 89

4.8 A single-cell of the MIMC 90

4.9 A single-cell of the MIMC with a non-ideal transformer 91

4.10 4-step current commutation method with non-negligible leakage inductance of transformer for moving from $S_{0o}, S_{1o}, S_{2o}, S_{3o}$ ON (MS_1) to $S_{4o}, S_{5o}, S_{6o}, S_{7o}$ ON (MS_2) when $V_T > 0, I_{out} > 0$ 93

4.11 Clamp circuit configuration 94

4.12 Equivalent circuits highlighting the activation of clamp with standard 4-step current based commutation of the output bridge from MS_1 to MS_2 for the case $V_T > 0, I_{out} > 0$ 95

4.13 Timing diagram showing the activation of clamp circuit when standard 4-step commutation method is used. (a)-(d) switching signals during standard 4-step current commutation of the output side 4QSH-bridge (e) transformer leakage inductance current I_L (f)-(h) currents in the clamp circuit corresponding to Figure 4.12. 96

4.14 Illustration of basic principle of the proposed source based leakage tolerant current commutation method 99

4.15 States (1-3) of proposed commutation strategy for single-phase AC/AC converter when $V_{in} > 0$, $I_{out} > 0$ and moving from MS_1 MS_1 to MS_2 MS_2 102

4.15 (Cont.) States (4-6) of proposed commutation strategy for single-phase AC/AC converter when $V_{in} > 0$, $I_{out} > 0$ and moving from MS_1 MS_1 to MS_2 MS_2 105

4.15 (Cont.) States (7-9) of proposed commutation strategy for single-phase AC/AC converter when $V_{in} > 0$, $I_{out} > 0$ and moving from MS_1 MS_1 to MS_2 MS_2 107

4.16 Theoretical commutation waveforms for moving from MS_1 MS_1 to MS_2 MS_2 when $V_{in} > 0$, $I_{out} > 0$. (a) With standard 4-step commutation (b) With proposed source based leakage tolerant current commutation method. 109

4.17 Generalised commutation paths for single-phase AC/AC converter (single-cell of the MIMC) to move between the steady states of Table 4.1 . . 112

4.17 (Cont.) Generalised commutation paths for single-phase AC/AC converter (single-cell of the MIMC) to move between the steady states of Table 4.1 113

5.1 Experimental setup diagram for the validation of proposed current commutation method on a single-cell of the MIMC 116

5.2 Typical rectifier-based-clamp circuit for protection against the current commutation failures 117

5.3 Photo of the DSP/FPGA based control platform with 16 optical transmitters and 3 optical receivers 118

5.4 Photo of the input side 4QSH-bridge based on SEMIKRON IGBT modules (SKM150GM12T4G) 119

5.5 Photo of the common-emitter configuration based four-quadrant switch - SEMIKRON SKM150GM12T4G 120

5.6 Block diagram of the isolated gate driver circuit 121

5.7 Photo of the isolated supply gate driver board 122

5.8 Input voltage V_{in} polarity detector circuit 123

5.9 Input voltage V_{in} threshold detector circuit 124

5.10 Output current I_{out} direction detector circuit 125

5.11 Photo of the sensing circuit - V_{in} polarity and threshold detector circuit 125

5.12 Illustration of function $s(t)$ implemented by input side 4QSH-bridge . 127

5.13 Time-domain plot of $|\cos(m\omega_s t)\sin(\omega_i t + \varphi_K)|$ and $|\sin(m\omega_s t)\cos(\omega_i t + \varphi_K)|$ - with $m = 1$, $\varphi_K = 0$, $f_i = 50$Hz, $f_{sw} = 500$Hz- showing when one term is at its peak value of unity, the other term is zero 129

5.14 Photo of the MF transformer 131

5.15 Photo of the experimental rig of the MIMC's cell built for the validation of proposed source based leakage tolerant current commutation method 133

5.16 The single-phase to single-phase AC/AC converter showing the points at which voltages and currents were measured in the experiment . . 134

5.17 Voltages and currents at the terminal of the single-phase isolated AC/AC converter with the standard 4-step current commutation 135

5.18 Transformer voltage V_T, leakage current I_L and voltages of the clamp circuits (input clamp voltage V_{clp1}, output clamp voltage V_{clp2} - in AC coupling - showing only ripples) with the standard 4-step current commutation 136

5.19 Triggering of clamp circuit during the reversal of leakage current I_L happening every commutation in the standard 4-step current commutation method 137

5.20 Expanded view of the region highlighted in Figure 5.19, showing current through the output clamp circuit during the reversal of leakage current after the transition from state 3 to state 4 in the standard 4-step current commutation - output clamp voltage V_{clp2} in AC coupling 138

5.21 Moore type Finite-State Machine (FSM) implemented in FPGA using VHDL to test the proposed source based leakage tolerant current commutation method 139

5.22 Voltages and currents at the terminal of the single-phase isolated AC/AC converter with the proposed current commutation method 142

5.23 Transformer voltage V_T, leakage current I_L and voltages of the clamp circuits (input clamp voltage V_{clp1}, output clamp voltage V_{clp2} -in AC coupling - showing only ripples) with the proposed current commutation method 142

5.24 Clamp circuit not triggering during the reversal of leakage current I_L with the proposed current commutation method 143

5.25 Expanded view of the region highlighted in Figure 5.24, showing current through the clamp circuit is zero during the reversal of leakage current with the proposed current commutation method 144

5.26 Comparison between simulated and experimented waveforms of input voltage V_{in}, output voltage V_o, transformer voltage V_T and leakage current I_L with the proposed current commutation method for the commutation from MS_1MS_1 to MS_2MS_2 when $V_{in} > 0$, $I_{out} > 0$. . . 145

5.27 Comparison between simulated and experimented waveforms of voltage across four-quadrant switch $s01$, its current i_5 in relation with the transformer voltage V_T and current I_L during the commutation from MS_1MS_1 to MS_2MS_2 when $V_{in} > 0$, $I_{out} > 0$. 146

5.28 Waveform of current flowing into the output clamp circuit due to transition from step 3 to step 4 in standard 4-step current commutation method 149

5.29 Leg current I_5 and voltage vs_{01} across switches S_{0o}, S_{1o} showing the hard turn-OFF of switch S_{0o} 150

5.30 Leg current I_5 and voltage vs_{01} across switches S_{0o}, S_{1o} showing the soft turn-OFF (ZCS) of switch S_{0o} 152

5.31 Simulated losses with standard and proposed current commutation methods: semiconductor switching loss with standard method (Sw Loss-Standard), semiconductor switching loss with proposed method (Sw Loss-Proposed), semiconductor conduction loss with standard method (Cond Loss-Standard), semiconductor conduction loss with proposed method (Cond Loss-Proposed), clamp circuits loss with standard method (SimClp Loss-Proposed), predicted clamp loss, using (5.23), with standard method (Pred Clp Loss-Standard) and clamp circuits loss with proposed method (SimClp Loss-Proposed) 154

5.32 Experimental and simulation-predicted losses with standard 4-step current commutation method and proposed current commutation method in a single cell of the MIMC 155

6.1 State transitions (per-cell) required for the implementation of the Venturini Modulation method 158

6.2 Finite State Machine (FSM) for implementing the Venturini Modulation on a cell of the MIMC 160

6.3 Equivalent Common-emitter configuration of a four-quadrant switch 161

6.4 Open-loop simulated waveforms at the terminals of the proposed three-phase to three-phase MIMC with Venturini Modulation and leakage tolerant commutation method (a) Three-phase input voltages V_{Ki} (b) Three-phase output currents I_{jo} 163

6.5 Open-loop simulated waveforms in the second cell of Figure 3.3 (a) Transformer voltage V_{TBa} (b) Transformer current I_{TBa} and output current I_{ao} (c) Output voltage V_{Boa} 163

6.6 Zoomed view of the highlighted region in Figure 6.5, showing non-ideal commutations (f) Transformer voltage V_{TBa} (g) Transformer current I_{TBa} (h) Output voltage V_{Boa} 164

6.7 Example of an ideal transformer current in a single cell when operated with the 50% Venturini Modulation – zero leakage transformer (a) Transformer voltage V_{TBa} (b) Transformer current I_{TBa} (c) Output voltage V_{Boa} 165

6.8 Cell output voltages V_{Koa} and final output phase voltage V_{ao} when operated with non-ideal (leakage tolerant) commutation and 50% Venturini Modulation. (a) Output voltage V_{Aoa}. (b) Output voltage V_{Boa}. (c) Output voltage V_{Coa}. (d) Output phase voltage V_{ao}. 166

6.9 Switching frequency vs. Total Harmonic Distortion (THD) with a fixed commutation time T_{comm} and filter inductor L =10 mH in the open-loop MIMC 167

6.10 Block diagram of the experimental setup for the three-phase to single-phase MIMC topology 168

6.11 Three-phase to single-phase version of the MIMC topology - showing the points where voltages and currents were measured in experiment 169

6.12 Photo of the DSP/FPGA based control platform with 48 optical transmitters and seven optical receivers 170

6.13 Structure of the Phase-Locked Loop (PLL) system 171

6.14 Photo of the experimental rig for three-phase to single-phase MIMC topology 172

6.15 Three-phase input voltages V_{Ki} at 50 Hz and single-phase output current I_{ao} at 60 Hz in open-loop three-phase to single-phase MIMC . . 174

6.16 Individual cell voltages V_{Koa} and the final output voltage V_{ao} in open-loop three-phase to single-phase MIMC 175

6.17 Zoomed view of Figure 6.16 showing several switching periods T_S of the individual cell voltages V_{Koa} and the final output voltage V_{ao} in open-loop three-phase to single-phase MIMC 175

6.18 Harmonic spectrum of the open loop output current I_{ao_open} in the MIMC (simulation) 176

6.19 Block diagram of PR based current-controller for MIMC 177

6.20 Bode diagram of the loop gain $\frac{G_{PR}(s)}{Ls+R}$ in the PR based current-controller with $\omega_c = 250\pi$ and $\omega_o = 120\pi$ 178

6.21 The output current I_{ao} in the MIMC when PR controller is activated at t=0.3ms (simulation) 179

6.22 Harmonic spectrum of the closed-loop output current I_{ao_PR} in the MIMC (simulation) 179

6.23 The open-loop output current I_{ao_open} in the MIMC (experiment) . . . 180

6.24 The closed-loop output current with PR controller I_{ao_PR} in the MIMC (experiment) 181

6.25 Harmonic spectrum of the open-loop output current I_{ao_open} in the MIMC (experiment) 181

6.26 Harmonic spectrum of the closed-loop output current I_{ao_PR} in the MIMC (experiment) 182

6.27 Experimental waveforms during step response of the closed-loop output current as a result of a PR controller (a) Step change in current reference I_{ao_ref} from 7A to 4A at t=0s (b) Zoomed view of Figure 6.27 showing transient response 183

6.28 M2PC based current controller for the MIMC (simulation) (a) closed-loop output current with linear ($I_{ao_MPC_lin}$) and non-linear ($I_{ao_MPC_n_lin}$) duty-cycles approach (b) Steady-state error - with linear ($I_{ao_err_lin}$) - with non-linear ($I_{ao_err_n_lin}$) 187

6.29 Harmonic spectrum of the output current with linear ($I_{ao_MPC_lin}$) and non-linear ($I_{ao_MPC_n_lin}$) duty-cycles approach of M2PC (simulation) 187

6.30 The closed-loop output current $I_{ao_MPC_n_lin}$ in the MIMC (experiment) 188

6.31 Harmonic spectrum of the closed-loop output current $I_{ao_MPC_n_lin}$ in the MIMC (experiment) 188

6.32 Experimental waveforms during step response of the closed-loop output current as a result of a non-linear M2PC controller (a) Step change in current reference I_{ao_ref} from 7A to 4A at t=0s (b) Zoomed view of Figure 6.32(a) showing transient response 190

6.33 Harmonic spectrums of the experimental output current with and without closed-loop systems in the MIMC. (a) open-loop current I_{ao_open} (b) PR based closed-loop current I_{ao_PR} (c) M2PC based closed-loop current $I_{ao_MPC_n_lin}$ 191

7.1 Relationship between the input side reactive power, α_2 and output power factor angle ϕ_o in the Venturini based modulated MIMC 196

7.2 Relationship between the input side reactive power, voltage regulation ratio q and output power factor angle ϕ_o with $\alpha_2 = 0$ in the Venturini based modulated MIMC 197

7.3 Relationship between the input side reactive power, voltage regulation ratio q and output power factor angle ϕ_o with $\alpha_2 = 1$ in the Venturini based modulated MIMC 198

7.4 Relationship between the active power, voltage regulation ratio q and output power factor angle ϕ_o in the Venturini based modulated MIMC 198

8.1 Extension of the three-phase Modular Isolated Matrix Converter (MIMC) for high voltage 206

8.2 Extension of the three-phase Modular Isolated Matrix Converter (MIMC) for high current 207

A.1 Schematic of an isolated driver for a 4-quadrant switch 225

A.2 Schematic of a 4QSH-bridge power board 226

A.3 Schematic of voltage polarity, voltage threshold and current direction detection board 227

B.1 State of the switches in the MIMC corresponding to the active vectors listed in Table 3.2 229

B.1 (Contd.) State of the switches in the MIMC corresponding to the active vectors listed in Table 3.2 229

B.1 (Contd.) State of the switches in the MIMC corresponding to the active vectors listed in Table 3.2 230

B.2 State of the switches in the MIMC corresponding to the zero vectors 231

B.3 Definitions of the 54 voltage and current vectors which generate $V_{TKj} = V_{Ki}$ 232

B.4 Definitions of the 54 complimentary voltage and current vectors which generate $V_{TKj} = -V_{Ki}$ 233

List of Tables

2.1 Comparison of the three-phase single-stage isolated AC/AC converter topologies 21

3.1 PLECS simulation parameters 40

3.2 Definition of the vectors for SVM 63

3.3 Vector configurations for the combinations of the output voltage and input current sectors 64

3.4 Comparison of the modulation methods 78

4.1 Steady states of a single-phase AC/AC converter (single-cell of the MIMC) 110

5.1 Parameters of the MF Transformer 131

5.2 Parameters of the experimental prototype 132

5.3 Input variables of FSM 140

5.4 Comparison of switch transitions in standard standard 4-step and proposed current commutation methods for all possible scenarios of V_{in} and I_{out} when converter moves between MS_1MS_1 and MS_2MS_2 . . . 153

6.1 Input variables of FSM 159

6.2 PLECS simulation parameters for validation of the MIMC 162

6.3 Experimental test parameters for validation of the MIMC 173

Chapter 1

Introduction

1.1 Background

The era of modern power electronics began at the Bell Laboratories in 1957 when the concept of Silicon Controlled Rectifier (SCR) was introduced [6–8]. The introduction of the SCRs acted as a trigger in the field of power electronics. This is because within the next two decades of SCR two faster switching devices, the Silicon Metal Oxide Field Effect Transistor (MOSFET) and the Silicon Insulated Gate Bipolar Transistor (IGBT), were introduced [9,10]. Revolutionary improvements in the device switching speed and power ratings are being achieved in the beginning of twenty-first century as wide-band gap technology based semiconductor devices are becoming commercially available in form of a Silicon Carbide (SiC) Schottky diodes [11, 12] and MOSFETs. Recent research has shown that further improvements in the device switching speed can be made possible by Galium Nitride (GaN) technology [13, 14]. In the past two years, reliability of the high speed device technologies has been the focus of research [15–17] as the successful operation of the wide-band gap devices can lead to significant reduction in the size of converters specifically for the AC/AC applications requiring galvanic isolation. This is because not only the filtering requirements but also the size of isolation stage reduces when operated with the higher frequency [18, 19].

The emerging isolated AC/AC applications include traction and interconnection of Low Voltage (LV) or Medium Voltage (MV) AC grids that require galvanic isolation to prevent the propagation of fault coming from one AC side to the other [20, 21]. These applications can greatly benefit in terms of size from the advancement in the switching speed of the devices. In such applications, power electronic devices can be used to increase the operating frequency at the isolation stage to achieve a compact size [22]. In this way the conventional, heavy and bulky line frequency transformer [23] can be avoided.

Despite a large variety of ratings, applications and topologies, converters that embed an isolation stage to replace line frequency transformers are usually referred to as Solid State Transformers (SSTs) [22, 24]. In addition to compact size, SSTs also offer increased control capabilities including voltage regulation and reactive power compensation when compared with conventional line frequency transformers [25, 26]. Due to these benefits SSTs are one of the most researched topics in power electronics with an exponential increase in the number of publications over that last two decades and seven-hundred publications in a single year of 2015 [27].

The basic architecture of a single-phase SST or Power Electronic Transformer (PET) [20,28] is shown in Figure 1.1 where the isolation stage is embedded in the power converter to generate a Medium Frequency (MF) or High Frequency (HF) AC waveform at the transformer.

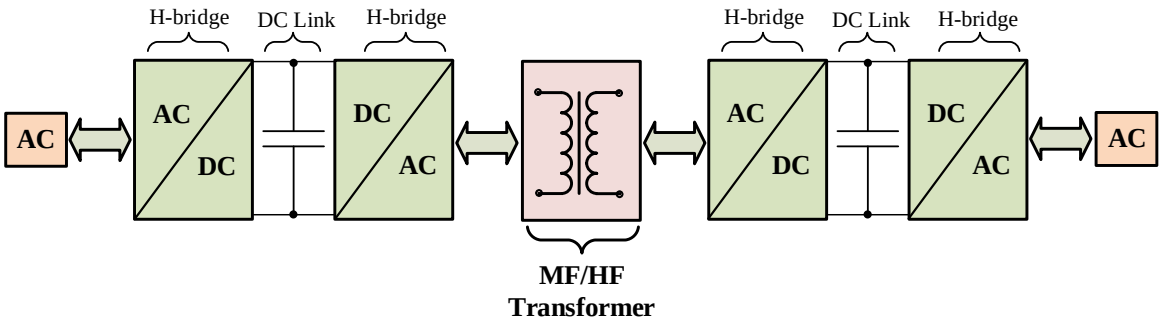


Figure 1.1: Architecture of a three-stage AC/AC Solid State Transformer (SST)

In the SST architecture, as shown in Figure 1.1, the low frequency AC is rectified to DC which is then converted to a transformer suitable medium or high frequency AC waveform. Note that this SST architecture is a three-stage architecture, including AC to DC, DC to DC and DC to AC stages, out of which there are two DC-link stages. In applications where space is expensive and a key limitation, for example in city centres, highly populated areas [19] and traction applications [21], the DC-link capacitors in the SST architecture are a major constraint in the improvements of the power density [19, 29]. For the improvement in the power density, both DC-links in the SST architecture, shown in Figure 1.1, can be eliminated to provide a compact single-stage AC/AC SST solution as, shown in Figure 1.2.

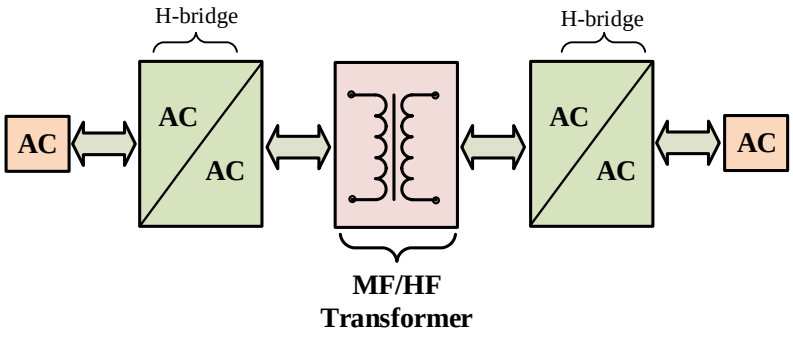


Figure 1.2: Architecture of a single-stage AC/AC SST

In comparison to the single-stage architecture, the three-stage architecture can suffer from reduced efficiency due to multiple power conversion stages [30] and lower reliability due to environmental degrading of the DC-link capacitors [3, 31, 32]. The single-stage SST, unlike three-stage SST, requires four-quadrant switches to transform low frequency AC directly to a transformer suitable MF or HF AC waveform without DC-link capacitors as shown in Figure 1.3. However, the absence of DC-link capacitors or energy storage in the single-stage SST makes it more suitable for applications where control capabilities, for example grid decoupling in case of imbalance and reactive power compensation [24], have lesser priority than the power density.

A potential example of such an application is a 400V LV mid-feeder compensator [33], where achieving a high power density isolated converter design and voltage regulation are the key requirements while the ability to operate under heavy imbalance or faults

is not a critical requirement. In fact, the converter can provide regulation services during normal grid operation but it will not be expected to respond to abnormal conditions.

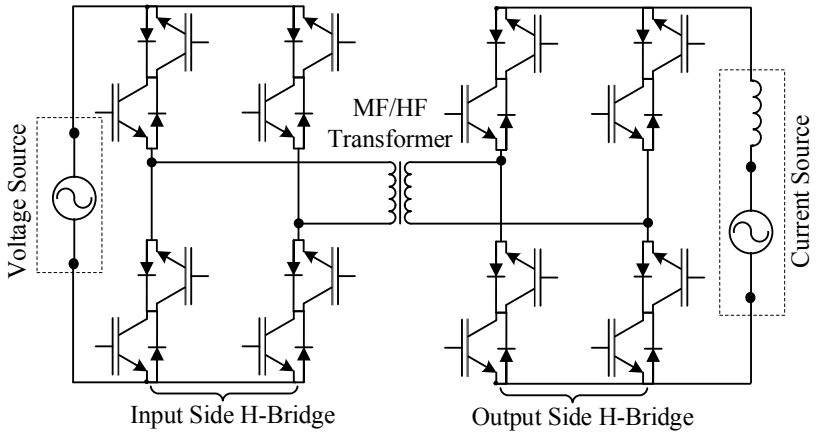


Figure 1.3: A single-phase AC/AC converter topology based on single-stage SST architecture

The single-phase single-stage isolated AC/AC converter, shown in Figure 1.3, has limited applications because the output frequency and the phase is locked to the input. For example, the single-phase single-stage isolated AC/AC converter will fail to find application in drive systems where the output frequency is different than the input frequency and in the interconnection of two AC systems operating at different frequencies. An example of interconnection of grids operating at two different frequencies can be found in Japan which uses both 50Hz and 60Hz AC systems [34]. The reason why the frequency and the phase at the output is locked to the input is because the single-phase single-stage isolated AC/AC converter has a single-phase sine-wave input and a single-phase sine-wave output.

In the past few years, various single-stage isolated AC/AC converter topologies have been proposed [1–5, 35–41] which can achieve input-output frequency decoupling by using a three-phase input. Out of these topologies, the topology in [35–37, 39] received more attention due to the reduced switch count, but the disadvantage of these topologies is that they lack a modular structure and thus scalability to higher power levels in not obvious [27, 42]. Recently, a modular single-stage topology has also been studied [43], but the key limitations are volume and weight since the proposed iso-

lation stage is at a low frequency. Therefore, there is very limited research on the single-stage isolated AC/AC solutions that are modular and flexible.

1.2 Objectives of the Project

This thesis investigates a single-stage modular isolated three-phase AC/AC topology that has been named as the Modular Isolated Matrix Converter (MIMC). The MIMC topology is derived considering the key requirements of future electrical networks [20, 28, 42] including isolation, compact design, modularity and flexibility. The topology uses single-phase isolated AC/AC converters as a basic building block or cell and keeps the modularity by repetition of these cells. The advantage of using single-phase isolated AC/AC converters as a cell is that the MIMC will have cell-level modularity because, within the cell, the two H-bridges on either side of the transformer are identical thus, offering additional benefits such as ease of hardware implementation and maintenance because all the four-quadrant switch based H-bridges are identical in the MIMC. The modularity can be further exploited by stacking multiple cells based on the desired power level. To achieve input-output frequency decoupling, the arrangement of the cells in the MIMC is derived from the concept of Direct Matrix Converters. The three-phase proposed MIMC topology is shown in Figure 1.4.

One of the key challenges in the practical implementation of the single-phase isolated AC/AC converter as a cell is the current commutation. This is because the four-quadrant or bidirectional switches used in the single-phase isolated AC/AC converter lacks free-wheeling paths and therefore a multi-step commutation approach is required unlike a dead-time approach that is used in a standard two-level inverter. The current commutation process becomes further challenging in the presence of practical transformer with non-negligible leakage inductance. This is because the output side of the cells in the MIMC have a filter inductance which can be seen as a current source and in the presence of the transformer leakage inductance, the output H-bridge of the cell, shown in Figure 1.3, will have current sources at both sides. Therefore whenever the

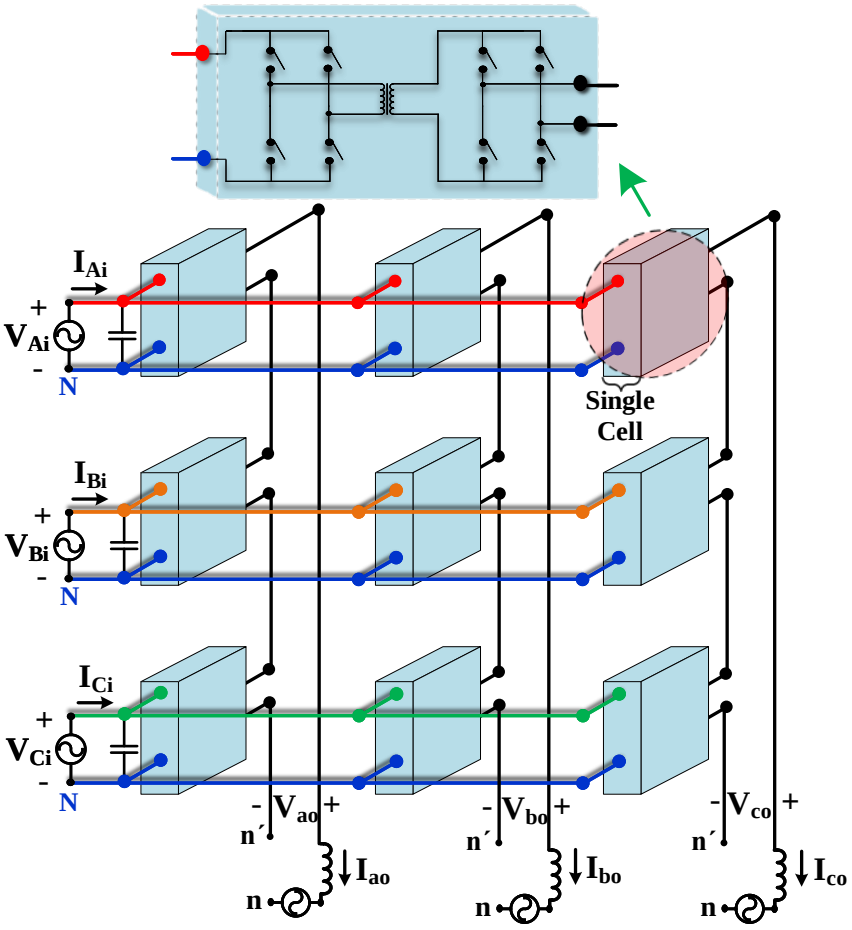


Figure 1.4: A three-phase Modular Isolated AC/AC Matrix Converter (MIMC) based on single-stage SST architecture

output side H-bridge of the cell changes state, the current through the transformer leakage inductance is forced to change which as a result will cause voltage spikes across the semiconductor devices. These voltage spikes can lead to permanent damage of the semiconductor devices and therefore, will threaten the practical success of the MIMC. Therefore the aim of this thesis is to study the practical feasibility of the proposed MIMC by investigating the key factors, including commutation, modulation and control, which are essential for the practical implementation of the MIMC.

It is the belief of the author that the study presented in this thesis will help in better understanding of isolated single-stage AC/AC converter solutions as well in increasing their competitiveness compared to other topologies.

The primary aim of this work has been met by achieving a number of research objectives which are summarised as follows:

- Proposing an isolated AC/AC single-stage conversion solution that achieves input-output frequency decoupling and also possesses a modular structure.
- Development and applications of modulation methods, including both scalar and vector approaches, for the proposed single-stage Modular Isolated Matrix Converter (MIMC).
- Design of a current commutation method that can work in practical scenarios with a non-ideal transformer which has non-zero leakage inductance.
- Practical implementation and demonstration of the effectiveness of the proposed commutation method and selection of the suitable modulation method which complies with the requirements of the commutation method.
- Experimental application of the selected modulation method along with the designed commutation method on the proposed topology for open-loop operation validation.
- Closed-loop control and compensation of the harmonics generated due to non-ideal commutations using multi-resonant approach of the Proportional-Resonant (PR) controller.
- Investigation into the suitability of Model Predictive Control (MPC) for the proposed topology and comparison of the practical performance of the PR control and MPC for the proposed converter.
- Study of the proposed converter in terms of reactive power compensation capability when operated with the Venturini modulation method.

Although the first single-stage isolated AC/AC SST architecture was proposed in 1968 by McMurray [44], it is only recently that the single-state SST architecture is receiving attention. This is due to the advancements in the computation power of control platforms and the availability of high-speed, high-power semiconductor devices. As the power electronics goes hand-in-hand with these technologies, complex and new single-stage SST topologies will emerge in near future for various applications. Therefore the work presented in this thesis is technology-driven in nature and not focussed on adaptation to specific applications.

1.3 Thesis Structure

The thesis is organised as follows;

- **Chapter 1** presents motivation, background and research objectives emphasising the challenges associated with the development of a single-stage isolated AC/AC conversion solution.
- **Chapter 2** provides a background on the conventional SST architectures and also discusses the evolution of a single-stage architecture based Modular Isolated Matrix Converter (MIMC) topology.
- **Chapter 3** presents the development, mathematical analysis and application of the modulation strategies, including both scalar and vector approaches, for the proposed MIMC.
- **Chapter 4** discusses the requirement of a commutation method for the MIMC and the drawbacks of using standard 4-step commutation solution. This chapter also presents a new leakage inductance tolerant commutation strategy which overcomes the drawback of the standard commutation approach.
- **Chapter 5** presents the experimental validation of the proposed leakage inductance tolerant commutation method on a single cell of the MIMC. The complete

development and operation of the experimental rig comprising a single cell of the MIMC is also discussed in this chapter.

- **Chapter 6** discusses the extension of the experimental rig from a single cell to a three-phase to single-phase MIMC. This chapter shows the open-loop experimental results that validate the application of the Venturini Modulation method and the leakage inductance tolerant commutation method for the MIMC. In addition to these, this chapter also demonstrates the feasibility of the closed-loop current control of the MIMC using Proportional-Resonant (PR) control as well as Modulated Model Predictive Control (M2PC).

- **Chapter 7** gives an insight into the reactive power capabilities of the MIMC when operated with Venturini modulation method. The parameters which define the reactive power limitations in a Venturini modulated MIMC are also discussed briefly.

- **Chapter 8** gives concluding remarks for the work presented in this thesis.

Chapter 2

Evolution of the Modular Isolated Matrix Converter (MIMC)

The idea of using semiconductor devices to operate the transformer with a MF or HF waveform leads to the concept of Power Electronic Transformer (PET) or Solid State Transformer (SST). The key benefit of a SST based converter topology is that a potential reduction in volume and weight can be achieved in comparison to the conventional line frequency transformer [22]. This is mainly because the size of magnetic components is inversely proportional to the frequency of operation. In addition to low volume and weight, the SST based converters have increased control capabilities. This is due to the presence of semiconductor devices, with the help of which the input and output side voltages, can be modulated and controlled as desired. Currently, the drawback of the SST based converters is that the short-circuit current and maximum voltage capability is limited by the semiconductor device [22, 24]. However, with the reliable operation of wide-band gap devices SiC and GaN, SST based converters are getting more and more attention [30, 45–47].

The SST based converter can be fundamentally categorised into the three types:

- Three-stage AC/DC/DC/AC
- Two-stage AC/DC/AC
- Single-stage AC/AC

2.1 Three-stage AC/DC/DC/AC SST Architecture

The three-stage AC/DC/DC/AC architecture converts from AC to DC, DC to DC using MF or a HF isolation stage and then DC back to AC. The three-stage architecture comprises of two DC-link stages, as shown in Figure 2.1. The simplest single-phase converter topology based on the three-stage AC/DC/DC/AC SST architecture is shown in Figure 2.2.

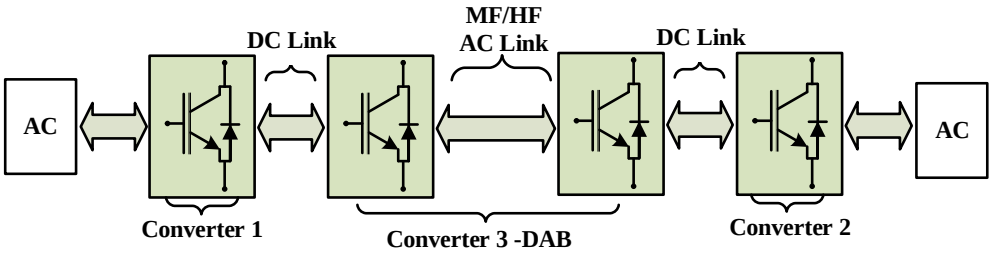


Figure 2.1: Architecture of a three-stage AC/DC/DC/AC SST

The principal operation of the single-phase, three-stage converter is carried out by the DC/DC conversion stage, also known as Dual Active Bridge (DAB). The DAB is composed of two voltage source converters connected via transformer. In terms of transformer design in the DAB, a sufficient amount of the leakage inductance is required for the power flow between the two DC voltage sources to be controlled. By changing the sign of the phase shift between the primary and secondary side voltage of the transformer, the direction of the current through the leakage inductance can be controlled. The amount of phase shift between the primary and secondary voltage of the transformer determines the amount of current through the leakage inductance

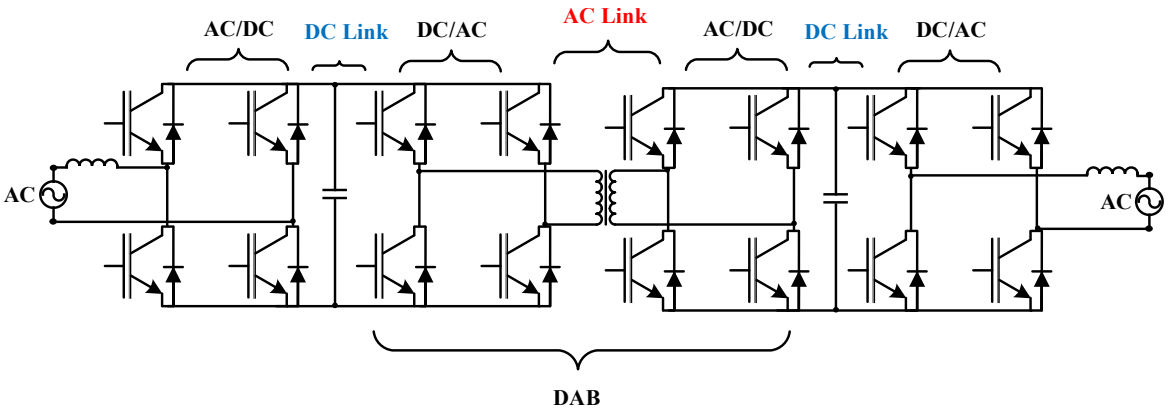


Figure 2.2: Single-phase AC/AC converter topology based on three-stage SST architecture

of the transformer [48]. Therefore, the direction of active power is defined by the sign of the phase shift, whereas its magnitude depends on the amount of phase shift [49].

The AC side H-bridges in the single-phase three-stage converter, shown in Figure 2.2, carry out the voltage regulation. Since the devices in the DAB operate in a range of kilohertz frequency, the semiconductor devices can undergo high switching losses [50]. Soft-switching methods are being successfully employed on the DAB converters to reduce the switching losses and increase the overall efficiency of the three-stage AC/DC/DC/AC SST based converter [51, 52] as otherwise the multiple-stage conversion can cause reduced efficiency [3, 31, 32]. A two-stage SST approach was studied in 2002 by Norrga [53, 54] which comprises only one DC-link stage in the AC/AC solution, therefore making an AC/DC/AC architecture.

2.2 Two-stage AC/DC/AC SST Architecture

In a two-stage AC/DC/AC architecture, one side of the SST utilizes a four-quadrant switch based H-bridge to convert low frequency AC to a waveform suitable for passing through a MF/HF transformer. The architecture for this SST approach is shown in Figure 2.3.

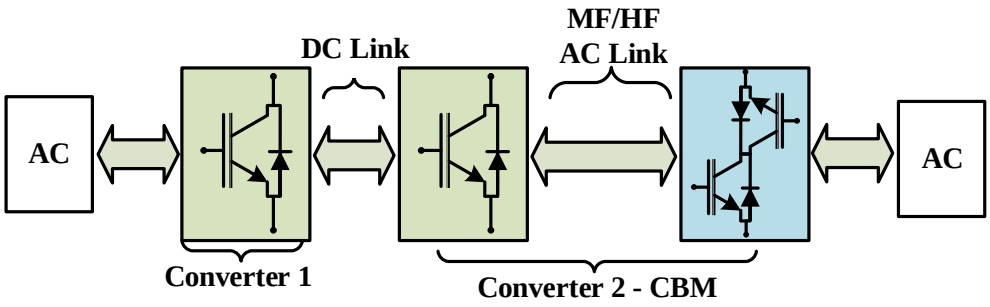


Figure 2.3: Architecture of a two-stage AC/DC/AC SST

A single-phase converter topology based on the two-stage AC/DC/AC SST architecture is shown in Figure 2.4. The single-phase two-stage converter topology, which uses a single DC-link stage, contains a Cycloconverter Based Module (CBM).

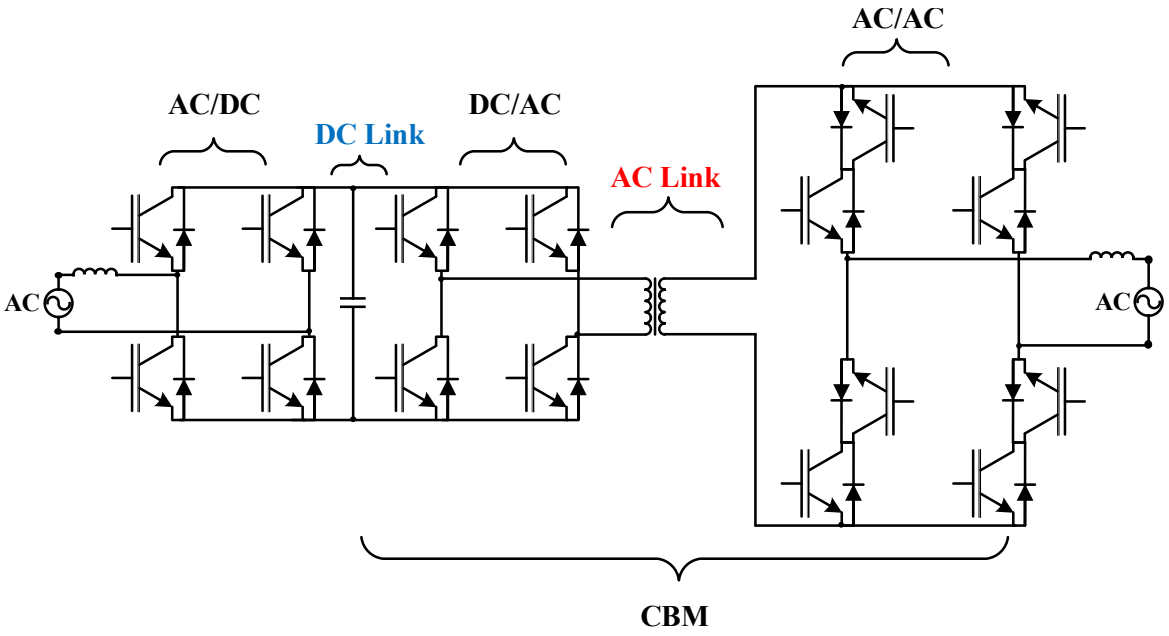


Figure 2.4: Single-phase AC/AC converter topology based on two-stage SST architecture

The CBM controls the power flow of the AC/AC system and operates at a medium or a high frequency [55–58]. The key challenge with this type of converter is the current commutation in the CBM because the four-quadrant switch based H-bridge used in the CBM lacks free-wheeling paths and therefore, a multi-step commutation approach is required. However, the standard multi-step commutation method is no longer valid

in the presence of the transformer leakage inductance because in this case, both sides of the CBM behave as current sources whereas the standard commutation method assumes voltage source on one side and a current source on the other. The standard commutation method can only be applied if the transformer leakage inductance is minimised. Therefore, the specifications of the transformer in this type of converter topology are different as opposed to the DAB in the three-stage topology, shown in Figure 2.2, where a sufficient amount of the leakage inductance is required for the power flow control between the two DC voltage sources. The four-quadrant switch based H-bridge in the two-stage converter topology can achieve complete soft-switching therefore, reducing the switching losses [53, 54]. However, to reduce the conduction losses, only two switches in the four-quadrant switch based H-bridge can be turned on during the zero voltage state [59].

A third type of AC/AC SST architecture is also possible in which no DC-link stage is required. This therefore allows achieving a compact design by undergoing a direct single-stage AC/AC conversion in comparison to the other two SST architectures.

2.3 Single-stage AC/AC SST Architecture

The single-stage AC/AC SST architecture, also known as matrix-type SST [42], directly generates the medium or high frequency AC waveform at the transformer from a low frequency AC waveform with the help of four-quadrant switches. The architecture of the single-stage AC/AC SST is shown in Figure 2.5.

The concept of the single-stage AC/AC SST architecture was introduced first by McMurray in 1968 [44]. In late seventies, Espelage presented analysis and design of 50kW thyristor based isolated single-stage AC/AC conversion system [60]. However, due to semiconductor technological limitations, the idea gained limited research attention at that time. The large turn-off times of the thyristors caused restricted frequency at the transformer eventually leading to only limited improvements in size and weight of the transformer.

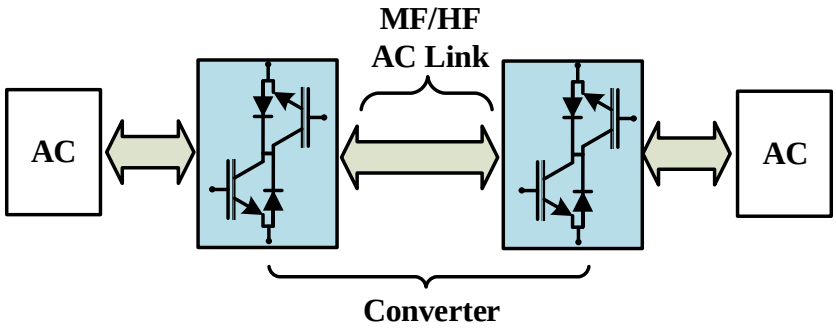


Figure 2.5: Architecture of a single-stage AC/AC SST

With the availability of MOSFETs and IGBTs, a 20kHz isolated single-stage AC/AC conversion was made possible in 1986 [61]. In the subsequent decades, various isolated single-phase AC/AC topologies based on single-stage SST architecture were presented [33, 41, 62–67]. Out of these topologies the single-phase AC/AC, also referred as full bridge-full bridge type [62, 66], is particularly attractive due to symmetrical nature which can be helpful in scalability of the power level. Figure 2.6 shows the single-phase AC/AC converter topology based on the single-stage AC/AC SST architecture.

The work on the single-phase AC/AC converter topology has received contributions in the modulation methods with voltage mode uni-polar and bi-polar modulation methods presented in [63] and [64], respectively and a current mode modulation method presented in [62]. With voltage source at the one side of the converter and current source at the other side, the transformer has to have minimum leakage inductance. In this regard, previous research on the commutation method for single-phase single-stage AC/AC converter assumes zero-leakage inductance in the transformer [65, 66]. However this assumption is not valid in reality as even with interleaved windings [68] it is not always possible to have adequate control over the leakage inductance of the transformer due to cost and design constraints. In this thesis, a practical current commutation is proposed for the single-phase single-stage AC/AC converter which does not rely on zero leakage inductance in the transformer, thus allowing standard transformer designs with non-negligible leakage inductance.

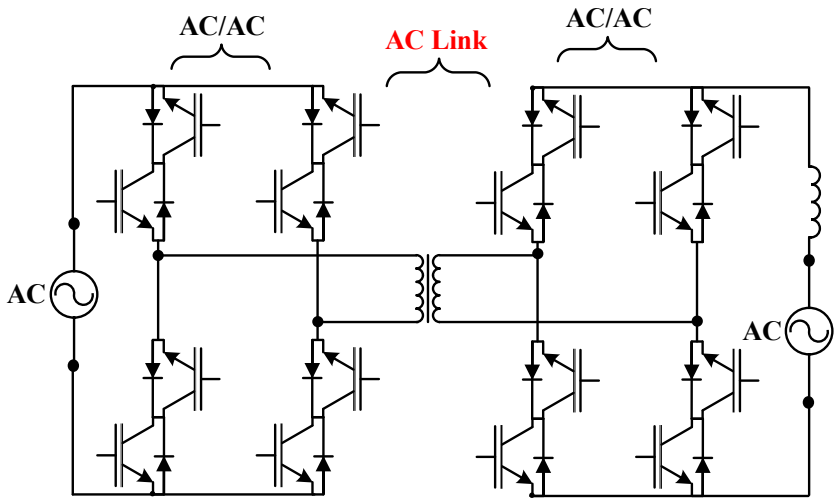


Figure 2.6: Single-phase AC/AC converter topology based on single-stage SST architecture

The single-phase single-stage AC/AC converter has restricted applications as the output frequency must always match the input one [24, 42]. For example, with the single-phase AC/AC converter [65, 66] it is impossible to generate 60Hz output from 50Hz input. Intuitively, the reason why the single-phase AC/AC converter fails to achieve the output frequency adaptation, is that the voltage that can be generated at the output is limited by the instantaneous value of the input voltage. This problem can be solved by using the concept of Direct Matrix Converter that achieves output frequency decoupling by utilising a three phase balanced voltage supply at the input side such as presented in a three-phase AC/AC converter topologies [1–5, 32, 38–41]. The three-phase single-stage converter topology, presented in [2], is referred to as the *push-pull topology* in literature. The *push-pull topology* suffers from the current commutation problem in the presence of transformer leakage inductances and requires clamp circuits at the input side to dissipate the energy stored in leakage inductances whenever current commutation occurs [38].

An improved version of the *push-pull topology*, which does not require clamp circuits, was presented in [1] and is shown in Figure 2.7. The three-phase single-stage topology, shown in Figure 2.7, operates by generating 50 % duty HF waveform at the transformer with the help of input side switches S_j and S_{j1}, where $j = a, b, c$. The

switches S_j, S_{j1} operate in complementary manner. Note that the switches S_s and S_{s1} are double pole single throw switches which operate synchronously with the input switches S_j, S_{j1}. The secondary sides of the transformers are connected to a Direct Matrix Converter which uses the pulse-width modulation to generate a three phase output. The voltage transfer ratio in this topology is limited to 0.866N, where N is the turns-ratio of the transformer.

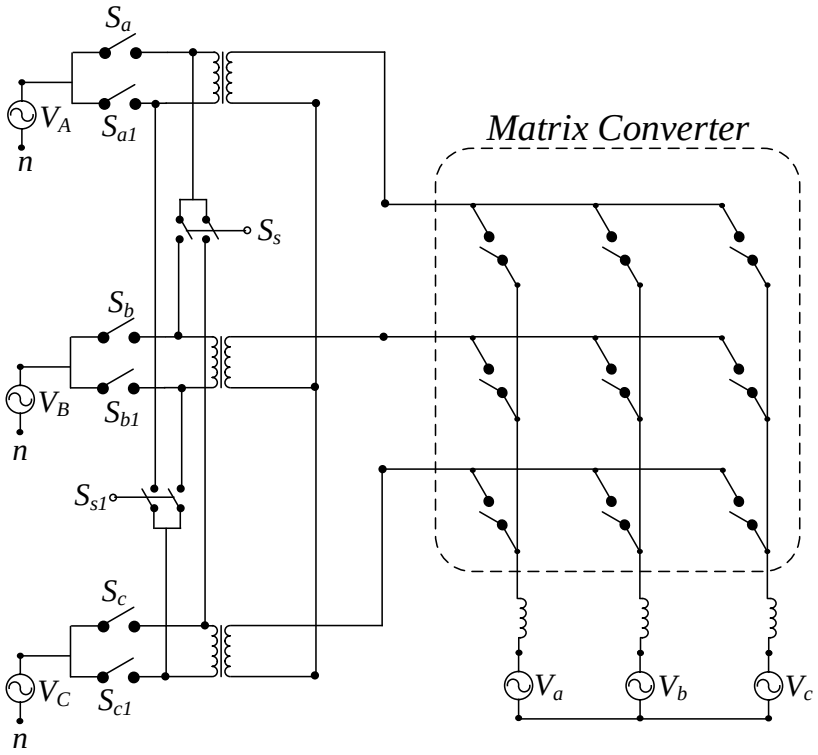


Figure 2.7: Three-phase single-stage SST based AC/AC converter topology with half-bridges at input side [1]

Another three-phase single-stage AC/AC converter topology, shown in Figure 2.8, which uses full bridges on the input side to generate a 50 % duty HF waveform was also presented [2]. The secondary sides of the transformers in the topology, shown in Figure 2.8, are connected to a Direct Matrix Converter and operates similarly to the topology shown in Figure 2.7. However, in this topology the total number of switches increase to 42 switches which is higher than that of the topology, shown in Figure 2.7. The voltage transfer ratio of the topology, shown in Figure 2.8, is 1.5N where N represents the transformer turns-ratio.

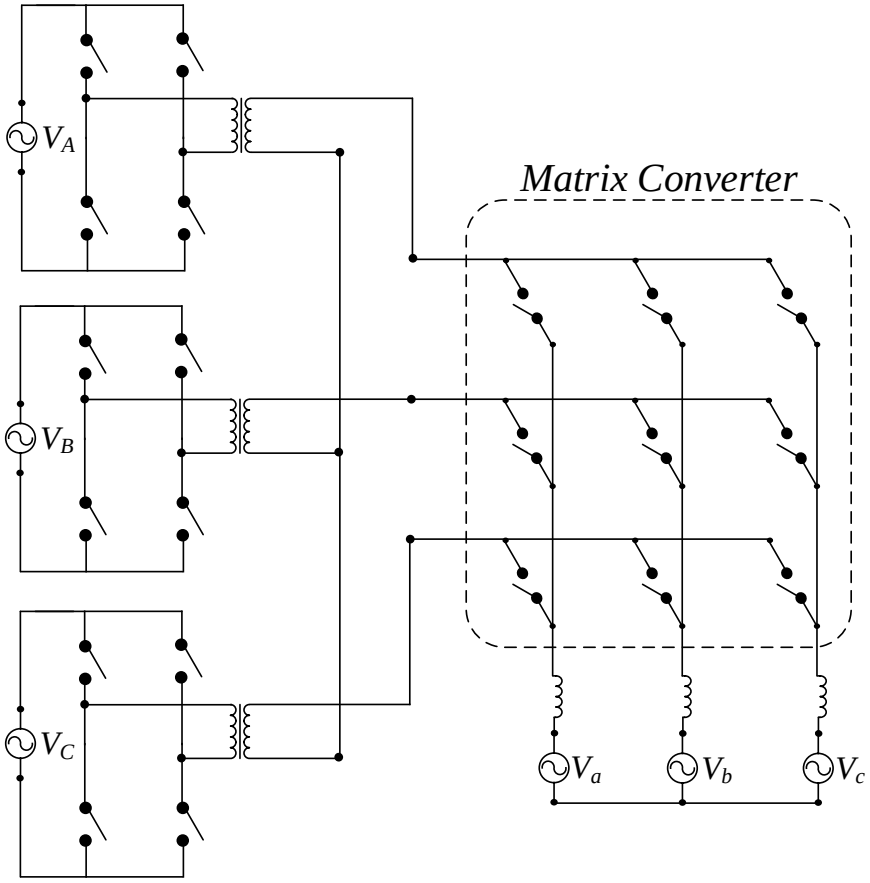


Figure 2.8: Three-phase single-stage SST based AC/AC converter topology with full-bridges at input side [2]

In order to achieve three-phase to three-phase single-stage AC/AC conversion with a reduced number of switches, a three-phase single-stage AC/AC converter topology, shown in Figure 2.9, was presented [4]. This topology uses a HF single-phase transformer and the main benefit of this topology is reduced switch count because the total number of switches is 24. In addition to this, there is a possibility of achieving a loss-less current commutation in presence of the transformer leakage inductance [3]. A parallel-resonant version of the topology, shown in Figure 2.9, has also been studied [5] by addition of a capacitor in parallel to the secondary winding of the transformer. However, the key disadvantage of the topologies, presented in [2–5, 38, 39], is the lack of a modular, flexible and symmetrical structure and thus, the scalability to higher power levels is not obvious which will compromise the requirements of the future power network including scalability, flexibility and redundancy [28, 42].

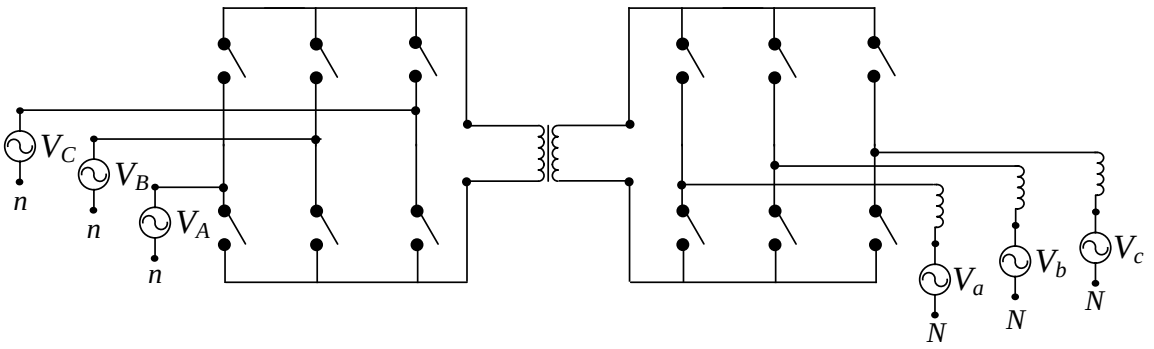


Figure 2.9: Three-phase single-stage SST based AC/AC converter topology with reduced switch count [3–5]

2.3.1 A Modular Isolated Matrix Converter (MIMC)

A modular three-phase single-stage AC/AC conversion solution can be achieved by exploiting the symmetrical nature of the single-phase AC/AC converter. This thesis proposes a three-phase modular single-stage AC/AC SST solution, as shown in Figure 2.10, which is obtained with an arrangement of nine independent single-phase single-stage AC/AC converters. The proposed converter uses the single-phase single-stage AC/AC converter as a basic building block or a cell. In this way, the proposed converter gains modularity within the structure because each cell is symmetrical. The proposed converter topology has higher switch count but increased redundancy, flexibility and modularity is expected to compensate for the potential disadvantage. Each cell in the proposed converter is connected in series at the output side to achieve the input-output frequency decoupling using Direct Matrix Converter modulation methods. Based on the concept of the evolution, proposed converter has been named as Modular Isolated Matrix Converter (MIMC). The comparison of the MIMC with the other isolated AC/AC conversion solutions in presented in Table 2.1.

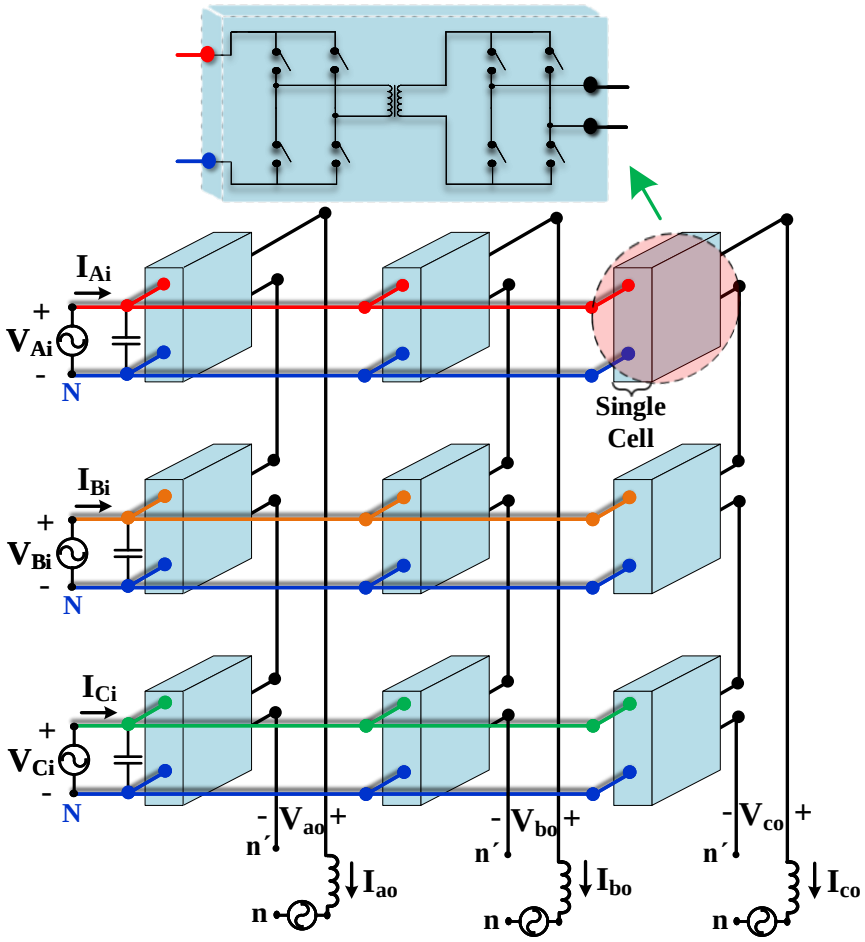


Figure 2.10: A three-phase Modular Isolated AC/AC Matrix Converter (MIMC) based on single-stage SST architecture

Table 2.1: Comparison of the three-phase single-stage isolated AC/AC converter topologies

Converter Topology	Push-pull [2]	Half-bridges [1]	Full-bridges [2]	Low switch [4]	MIMC
Primary side switches	2	20	24	12	72
Secondary side switches	18	18	18	12	72
Total switch count	20	38	42	24	144
No. of transformers	3	3	3	1	9
Fault propagation	Medium	Medium	Medium	High	Low [1]
Power-level adaptation	No	Difficult	Difficult	No	Easy
Cell-level modularity	No	No	No	No	Yes
Source-based commutation	Not possible	Possible	Possible	Possible	Possible
Max voltage regulation ratio [2]	0.86N	0.86N	1.5N	0.86N	1.73N

[1] All three phases at the input side of the MIMC are isolated from each other and so as phases at the output side
[2] The number 'N' represents turn-ratio of the transformers

2.4 Conclusions

The concept of embedding the isolation stage within the power electronic converter to achieve high power density and controllability, despite the wide range of applications and ratings, is referred universally to as a Solid State Transformer (SST). Based on the architecture, the AC/AC SST solutions can be divided into a total of three types including three-stage AC/DC/DC/AC, two-stage AC/DC/AC and single-stage AC/AC. The single-stage AC/AC, also known as matrix-type SST, can achieve a high power density and reliability when compared with the other two SST approaches due to the absence of DC-link capacitors. Within the single-stage architecture, the single-phase single-stage AC/AC converter is particularly important due to symmetrical nature that be exploited by using it as the basic building block in obtaining an isolated modular AC/AC solution. This chapter proposes a new Modular Isolated Matrix Converter (MIMC) topology formed by an arrangement of the single-phase single-stage AC/AC converters in accordance with the concepts of Direct Matrix Converter.

Chapter 3

Modulation Methods

3.1 Introduction

The MIMC topology, shown in Figure 3.1, is an extension of Direct Matrix Converter to an isolated case with additional switching states. To clearly show this, the Direct Matrix Converter comprising nine four-quadrant switches is shown in Figure 3.2. At any time each of the output phases can be directly connected to any of the input phases therefore, giving only three possible switching states per output generating either $V_{jo} = V_{Ai}$ or $V_{jo} = V_{Bi}$ or $V_{jo} = V_{Ci}$. The MIMC can also generate these voltages at its output just like the Direct Matrix Converter however, additionally it can generate the inverse of the input voltages as well i.e. $V_{jo} = -V_{Ai}$ or $V_{jo} = -V_{Bi}$ or $V_{jo} = -V_{Ci}$ this is because a single-cell in the MIMC is analogous to a four-quadrant switch in the Direct Matrix Converter. The series connection on the output side of the MIMC further increases the possible output voltages.

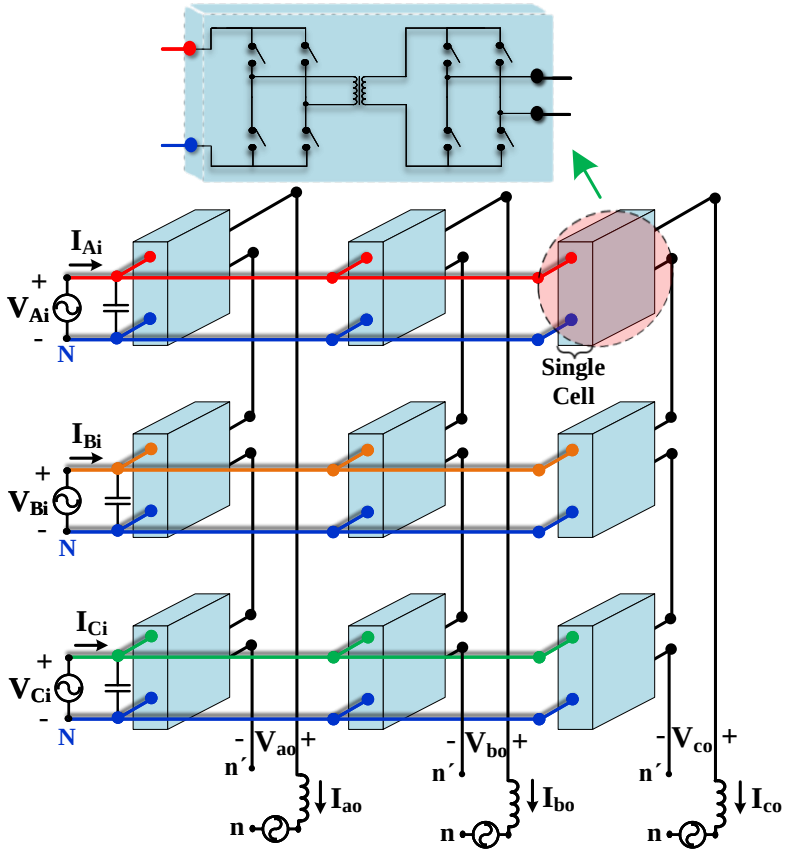


Figure 3.1: A three-phase to three-phase Modular Isolated Matrix Converter (MIMC)

Similar to the Direct Matrix Converter, it is assumed that one side in the MIMC behaves as a voltage source while the other side behaves as a current source. Therefore the modulation strategies of the standard Direct Matrix Converter can be adapted for the MIMC.

The first step in development of the modulation techniques is the identification of all the possible switch states available in the MIMC topology which means that all the states must respect the following two constraints. In case either of the listed constraints are not valid, the semiconductor devices can undergo catastrophic damage [69, 70] which will eventually lead to converter failure.

- Input voltage source must not be short circuited.
- Output current source must not open circuited.

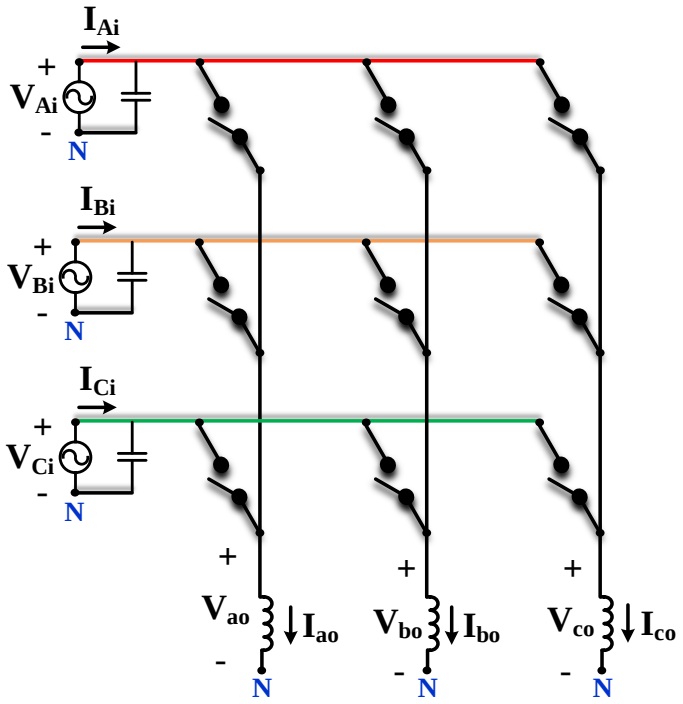


Figure 3.2: A three-phase to three-phase Direct Matrix Converter

To be able to determine all the possible switch states for the MIMC shown in Figure 3.1, consider a generalised three-phase to single-phase section of the MIMC, as shown in Figure 3.3. The three-phase to single-phase section of the MIMC has a voltage source at the input side, current source at the output side and an ideal MF transformer. The generic Modulation State (MS) matrices for the input and output side bridges can be defined as:

$$MS_{Kij} = \begin{bmatrix} S_{WKij} & S_{YKij} \\ S_{ZKij} & S_{XKij} \end{bmatrix} \tag{3.1}$$

$$MS_{Koj} = \begin{bmatrix} S_{WKoj} & S_{YKoj} \\ S_{ZKoj} & S_{XKoj} \end{bmatrix} \tag{3.2}$$

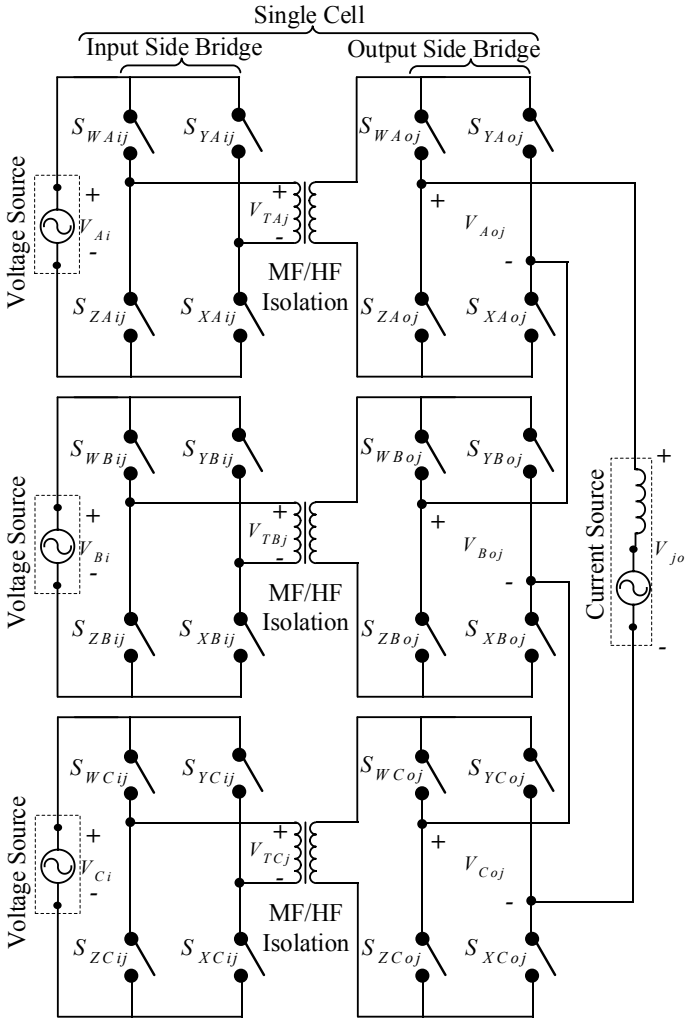


Figure 3.3: A generalised three-phase to single-phase section of the MIMC

In (3.1) and (3.2), 'i' denotes the input side, 'o' the output side, 'K' the three input phases with $K = A, B, C$ and 'j' the three output phases with $j = a, b, c$. Subsequently, to respect the mentioned constraints, i.e. the input voltage sources cannot be short circuited and that the output current sources cannot be open circuited during operation [71], the feasible MS matrices can be expressed as shown in (3.3) and (3.4), respectively. MS_1 and MS_2 are two active MS matrices whereas MS_0 is a zero MS matrix. It is important to mention that the zero state can be implemented with two different MS matrices however either of these have the same effect on the modulation waveforms.

$$MS_1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, MS_2 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{3.3}$$

$$MS_0 = \begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix} or \begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix} \tag{3.4}$$

Most of the modulation techniques, including both scalar and vector modulations, can be derived by using the listed three basic modulation states i.e. MS_1, MS_2 and MS_0 given in (3.3)-(3.4). For example when the modulation state matrix MS_1 is applied to both the input and the output bridges of a generic cell of the MIMC then the cell's output voltage in terms of its input voltage can be written as $V_{Koj} = V_{Ki}$. Although, the modulation methods which are applicable to a Direct Matrix Converter can be extended in order to be applicable to the MIMC. However, for the sake of simplicity the Venturini Modulation Method, which is a type of scalar modulation method, will be applied to the MIMC first.

3.2 Venturini Modulation

The *Venturini Modulation* method [72], presented in 1988 by Alesina and Venturini, was an early solution for solving the problem of modulation in direct AC/AC converters. The method formulates the expressions for the duty cycles of the switches of a Matrix Converter to generate, from a three-phase sine-wave input with a fundamental frequency of f_i, a three-phase output with a frequency of f_o [72]. This method solved the modulation problem by formulating the duty cycle D_{Kj} expression given in (3.5). The maximum value of the voltage regulation ratio achieved with this method is limited to 0.5 however, the voltage regulation ratio can be increased by third-harmonic injection scheme which was also presented by Alesina and Venturini and has been discussed in Section 3.4.

Note that the duty cycle D_{Kj} expression, shown in (3.5), is valid for a fixed input power factor of unity, however the input power factor can be varied by using another

modulation solution which will be presented in Chapter 7. When duty cycle D_{Kj}, given in (3.5), is applied to the topology, shown in Figure 3.3, V_{Ki} with $K = A, B, C$ are the three-phase input voltages and V_{jo} with $j = a, b, c$ are the three-phase output voltages. These can be expressed by (3.6) and (3.7), respectively where V_m is the input voltage amplitude and q is the voltage transfer ratio.

$$D_{Kj} = \frac{1}{3}\left(1 + \frac{2\ V_{Ki}V_{jo}}{{V_m}^2}\right) \tag{3.5}$$

$$V_{Ki} = V_m \sin\left(\omega_i t + \phi_K\right) \tag{3.6}$$

$$V_{jo} = qV_m \sin\left(\omega_o t + \phi_j\right) \tag{3.7}$$

Due to the presence of MF transformers in the MIMC, the basic operation of the converter can be achieved by first converting the low frequency input voltage V_{Ki} into a 50% duty cycle MF frequency voltage waveform at the transformers and then modulating the output side bridges to generate a low frequency output voltage V_{jo} by implementing the duty cycle (3.5). The Matrix Converter duty cycle, given in (3.5), can be directly applied to the MIMC because, similar to the Direct Matrix Converter, any one of the three phase input voltages can be selected for any duration to appear at the output.

The 50% duty cycle MF frequency voltage waveform at the transformer can be achieved by simply flipping the input voltage at the switching frequency f_{sw}. This is equivalent to implementing the switching function (3.8) on all the input side bridges of the MIMC. In equation (3.8), T_S is the switching period where n represents the number of the switching period, thus $n = 0, 1, 2, ..., \infty$. Considering the first period with $n = 0$, the steady-state MS_1 will be applied for the first half of the switching period, from 0 to $0.5T_S$, making $V_{TKj} = V_{Ki}$ true. Whereas steady-state MS_2 for the other half of switching period, from $0.5T_S$ to T_S, making $V_{TKj} = -V_{Ki}$ true and therefore generating a 50% duty cycle MF waveform at the transformer. Note that (3.8) is applicable to all the input side bridges of the MIMC, therefore all the input side bridges of the MIMC are switched synchronously. However, this is not a strict

requirement and different phases could be flipped at different times without affecting the average components of the modulated waveforms.

V_{TKj}	MS_{Kij}	$Interval$
V_{Ki}	MS_1	$nT_S \leq t \leq 0.5(T_S + nT_S)$
$-V_{Ki}$	MS_2	$0.5(T_S + nT_S) < t \leq (T_S + nT_S)$

(3.8)

A 50% duty cycle waveform at the transformer has been selected as it minimises the peak flux and will eventually reduce the core area A_c of the MF transformer. The required core area A_c is related to the transformer voltage V_{TKj} by the expression given in (3.9) where N is the number of turns and B^{MAX} is the maximum flux density. The core area A_c for various duty cycle voltage waveforms at the transformer were computed and the corresponding value of required core area A_c is shown in Figure 3.4. It can be seen from Figure 3.4 that the core area A_c is higher for duty cycles other than 0.5. The reason for increased core area requirement at the duty cycles other than 0.5 is presence of the low-frequency components in the transformer voltage $V_{TKj}(t)$ leading to increased flux-swing when moving away from the duty cycle of 0.5. Note that in Figure 3.4 the core area A_c is normalised with respect to the minimum value of core area ${A_c}^{MIN}$, which is at a duty cycle of 0.5. Therefore, a 50% duty cycle voltage waveform was selected as it minimises the size of the MF transformers.

$$A_c = \frac{1}{NB^{MAX}} \int V_{TKj}(t)dt \tag{3.9}$$

Note that the harmonic spectrum of the 50% duty cycle MF voltage waveform is essential for the practical design of MF transformer as the core area of the MF transformer A_c must be capable of accommodating the fundamental as well as harmonics present in the voltage applied to it. The expression for the transformer voltage $V_{TKj}(t)$, shown in (3.10), can be obtained as a product of the square-wave function (3.8) and the input voltage $V_{Ki}(t)$ (3.6). A detailed discussion on the determination of the core area A_c from the transformer voltage V_{TKj} is shown in Section 5.1.6 of Chapter 5

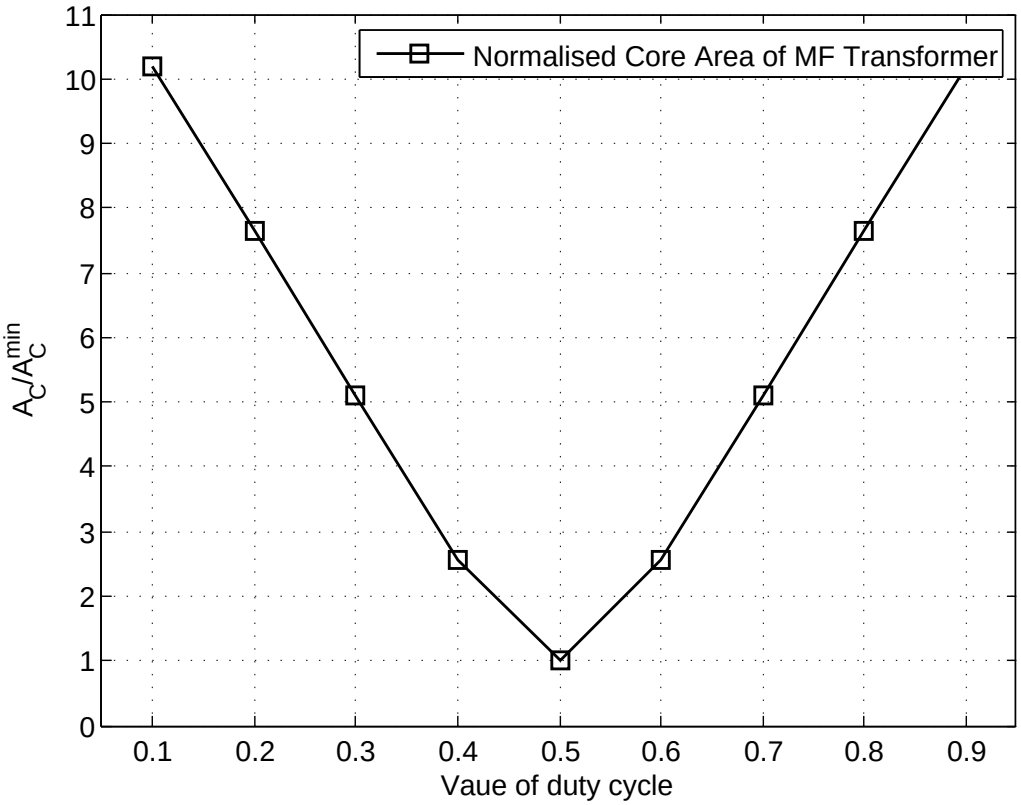


Figure 3.4: The relationship between the duty cycle of the voltage waveform at MF transformer and the core area A_c of the MF transformer

because the core area A_c is not required from the modulation's perspective which assumes an ideal-transformer.

$$V_{TKj}(t) = \frac{2V_m}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \left(\cos\left(n\omega_s t - \omega_i t - \phi_K\right) - \cos\left(n\omega_s t + \omega_i t + \phi_K\right)\right) \quad (3.10)$$

In order to generate the voltage V_{jo} (3.7) at the output of the MIMC, the output side bridges must be modulated to implement equation (3.5) and the duty cycles D_{Kj} must be arranged in the pattern shown in Figure 3.5, as defined by the Venturini Modulation method. This arrangement of the duty cycles can be achieved by implementing the switching functions shown in (3.11)-(3.13) on the top, middle and bottom cells of the topology shown in Figure 3.3. Note that these switching functions are generalised expressions that are valid for the complete three-phase to three-phase MIMC.

The switching functions for the three-phase output can be obtained by substituting $j = a, b, c$ in (3.11)-(3.13) for output phase a, phase b and phase c, respectively.

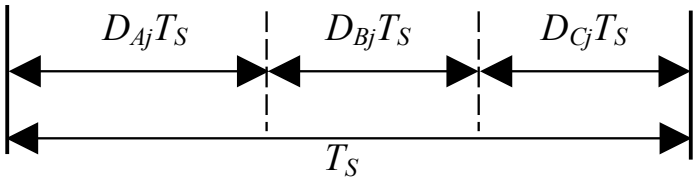


Figure 3.5: The arrangement of the duty cycles defined by the Venturini Modulation method

V_{Aoj}	MS_{Aoj}	*Interval*	*Condition*
V_{Ai}	MS_1	$nT_S \leq t \leq D_{Aj}(T_S + nT_S)$	$D_{Aj} \leq 0.5$
0	MS_0	$D_{Aj}(T_S + nT_S) < t \leq (T_S + nT_S)$	
V_{Ai}	MS_1	$nT_S \leq t \leq 0.5(T_S + nT_S)$	
V_{Ai}	MS_2	$0.5(T_S + nT_S) < t \leq D_{Aj}(T_S + nT_S)$	$D_{Aj} > 0.5$
0	MS_0	$D_{Aj}(T_S + nT_S) < t \leq (T_S + nT_S)$	

(3.11)

V_{Boj}	MS_{Boj}	*Interval*	*Condition*
0	MS_0	$nT_S \leq t \leq D_{Aj}(T_S + nT_S)$	
V_{Bi}	MS_1	$D_{Aj}(T_S + nT_S) < t \leq 0.5(T_S + nT_S)$	$D_{Aj} \leq 0.5$
V_{Bi}	MS_2	$0.5(T_S + nT_S) < t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	$\leq (D_{Aj} + D_{Bj})$
0	MS_0	$(D_{Aj} + D_{Bj})(T_S + nT_S) < t \leq (T_S + nT_S)$	
0	MS_0	$nT_S \leq t \leq D_{Aj}(T_S + nT_S)$	$0.5 \leq D_{Aj}$
V_{Bi}	MS_2	$D_{Aj}(T_S + nT_S) < t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	
0	MS_0	$(D_{Aj} + D_{Ba})(T_S + nT_S) < t \leq (T_S + nT_S)$	
0	MS_0	$nT_S \leq t \leq D_{Aj}(T_S + nT_S)$	$(D_{Aj} + D_{Bj})$
V_{Bi}	MS_1	$D_{Aj}(T_S + nT_S) < t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	≤ 0.5
0	MS_0	$(D_{Aj} + D_{Bj})(T_S + nT_S) < t \leq (T_S + nT_S)$	

(3.12)

V_{Coj}	MS_{Coj}	*Interval*	*Condition*
0	MS_0	$nT_S \leq t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	$(D_{Aj} + D_{Bj})$
V_{Ci}	MS_1	$(D_{Aj} + D_{Bj})(T_S + nT_S) < t \leq 0.5(T_S + nT_S)$	≤ 0.5
V_{Ci}	MS_2	$0.5(T_S + nT_S) < t \leq (T_S + nT_S)$	
0	MS_0	$nT_S < t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	$(D_{Aj} + D_{Bj})$
V_{Ci}	MS_2	$(D_{Aj} + D_{Bj})(T_S + nT_S) < t \leq (T_S + nT_S)$	> 0.5

(3.13)

To show the waveforms as a result of the switching functions shown in (3.8), (3.11)-(3.13), the theoretical voltage waveforms within the top-cell are shown in Figure 3.6. It can be seen from Figure 3.6(b) that the low frequency input voltage V_{Ki} is converted to a transformer-suitable 50% duty-cycle MF voltage waveform as a result of implementation of function (3.8) on input side bridge of top-cell.

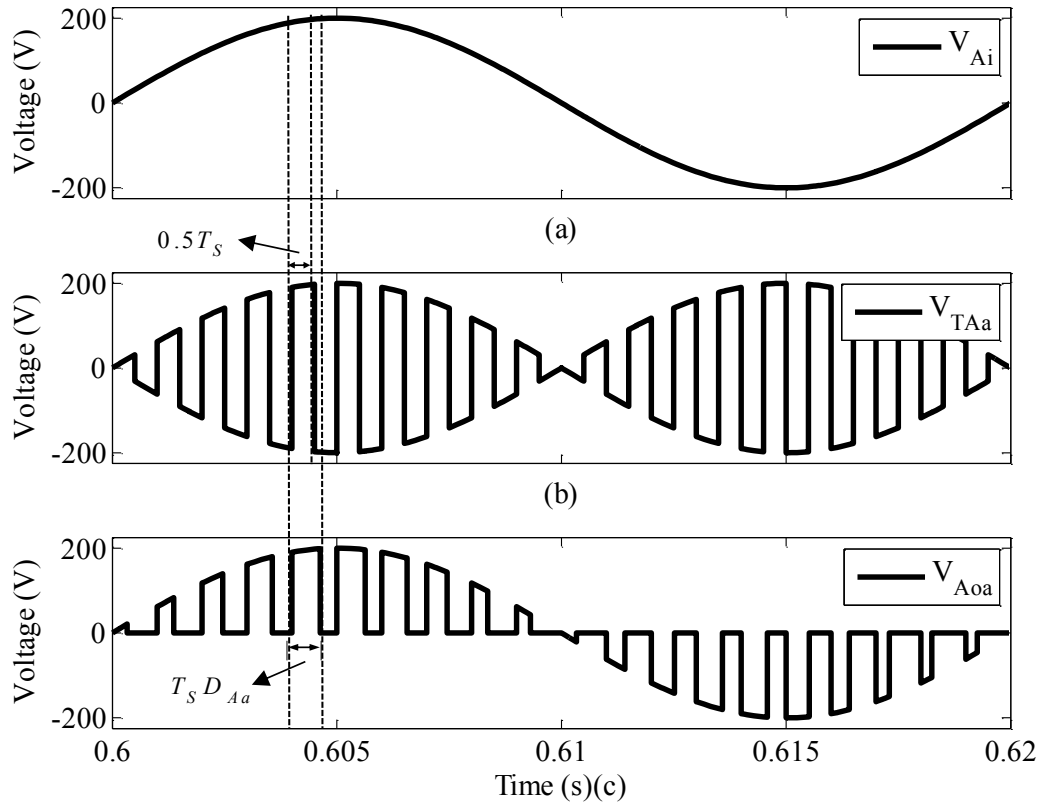


Figure 3.6: Theoretical voltage waveforms in the top-cell as a result of the Venturini Modulation (a) Input voltage V_{Ai} (b) Transformer voltage V_{TAa} (c) Output voltage V_{Aoa}

The output voltage V_{Aoa}, shown in Figure 3.6(c), is obtained by applying (3.11) to the output side bridge of the cell. To demonstrate how the modulation states can be applied using (3.11), a zoomed view of Figure 3.6, focussing on several switching periods T_S, is shown in Figure 3.7. In Figure 3.7, the modulation states have been represented by input and output MS matrices in form $MS_{Kij}MS_{Koj}$ where $K = A$ and $j = a$ therefore making $MS_{Aia}MS_{Aoa}$. It can be seen from the single switching period T_S, highlighted in Figure 3.7, that the value of duty cycle $T_S D_{Aa} > 0.5T_S$ which satisfies the condition $D_{Aa} > 0.5$ of the switching function (3.11) for output bridge of the top-cell. As the condition $D_{Aa} > 0.5$ is true in (3.11), there are three intervals within the said condition.

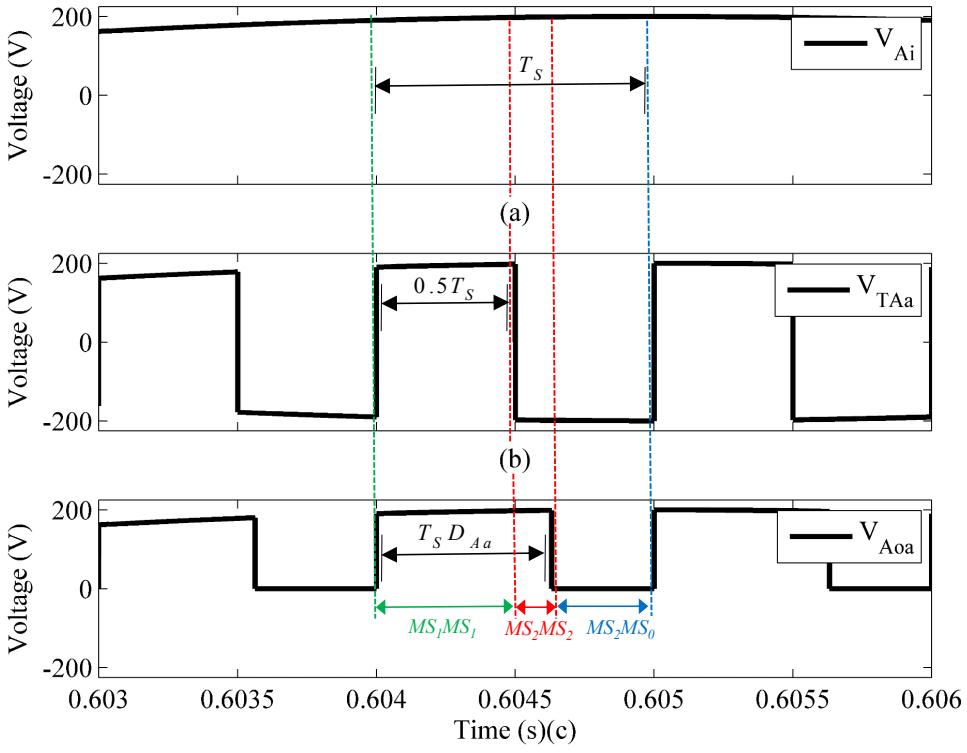


Figure 3.7: A zoomed view of Figure 3.6, focussing on a single switching period T_S (a) Input voltage V_{Ai} (b) Transformer voltage V_{TAa} (c) Output voltage V_{Aoa}

For the first interval $0 \leq t \leq 0.5T_S$, the modulation state of the output bridge is $MS_{Aoa} = MS_1$ while during the same interval i.e. $0 \leq t \leq 0.5T_S$, the modulation state of the input bridge using (3.8) is $MS_{Aia} = MS_1$ therefore the top-cell is applying the modulation states $MS_{Aia}MS_{Aoa} = MS_1MS_1$. For the second interval

$0.5T_S < t \leq D_{Aj}T_S$, the modulation state of the output bridge becomes $MS_{Aoa} = MS_2$ and that of the input bridge becomes $MS_{Aia} = MS_2$ therefore, the modulation states $MS_{Aia}MS_{Aoa} = MS_2MS_2$ are being applied. For the third interval $D_{Aj}T_S < t \leq T_S$, the output side bridge applies the zero state i.e. $MS_{Aoa} = MS_0$ while the modulation state of the input side bridge is $MS_{Aia} = MS_2$ according to (3.8). Thus the top-cell is applying the modulation states $MS_{Aia}MS_{Aoa} = MS_2MS_0$ in the third interval. The same sequence of modulation states of input and output bridges which is MS_1MS_1 (first interval), MS_2MS_2 (second interval), MS_2MS_0 (third interval) can also be seen in Figure 3.7, confirming that the theoretical waveforms are in accordance with the defined switching functions given in (3.8) and (3.11).

In a similar manner, the switching function (3.12) will be applied to the output bridge of the middle-cell. For instance if the first condition $D_{Aa} \leq 0.5 \leq (D_{Aa} + D_{Ba})$ is true in (3.12) then there a total of 4 possible intervals within this condition. The steady-state MS_0 will be applied for the first interval $0 \leq t \leq D_{Aa}T_S$ making $MS_{Boa} = MS_0$ and the steady-state MS_1 will be applied for the second interval $D_{Aa}T_S < t \leq 0.5T_S$ making $MS_{Boa} = MS_1$. The steady-state MS_2 for the third interval $0.5T_S < t \leq (D_{Aa} + D_{Ba})T_S$ making $MS_{Boa} = MS_2$ and again MS_0 for fourth interval $(D_{Aa} + D_{Ba})T_S < t \leq T_S$ making $MS_{Boa} = MS_0$. The other conditions and interval of all the switching functions in (3.11)-(3.13) can be interpreted following the discussed approach. The theoretical voltage waveforms at the terminals of the three-phase to single-phase MIMC, as a result of discussed switching functions, are shown in Figure 3.8.

Figure 3.8(a)-(c), shows the output voltages V_{Koa} of individual cells where $K = A, B, C$ for the top, middle and bottom cell, respectively. It is important to note that the final output voltage V_{ao}, shown in Figure 3.8(d), is the sum of cell output voltages V_{Koa} due to a series connection at the output side of the MIMC as shown in Figure 3.3 and follows equation (3.14). This can be validated by observing a single switching period T_S shown in Figure 3.9. In addition to this, it can also be seen from Figure 3.9 that the duty cycles D_{Aa}, D_{Ba}, D_{Ca} are arranged in the pattern shown in Figure 3.5 and are therefore in accordance with the Venturini Modulation.

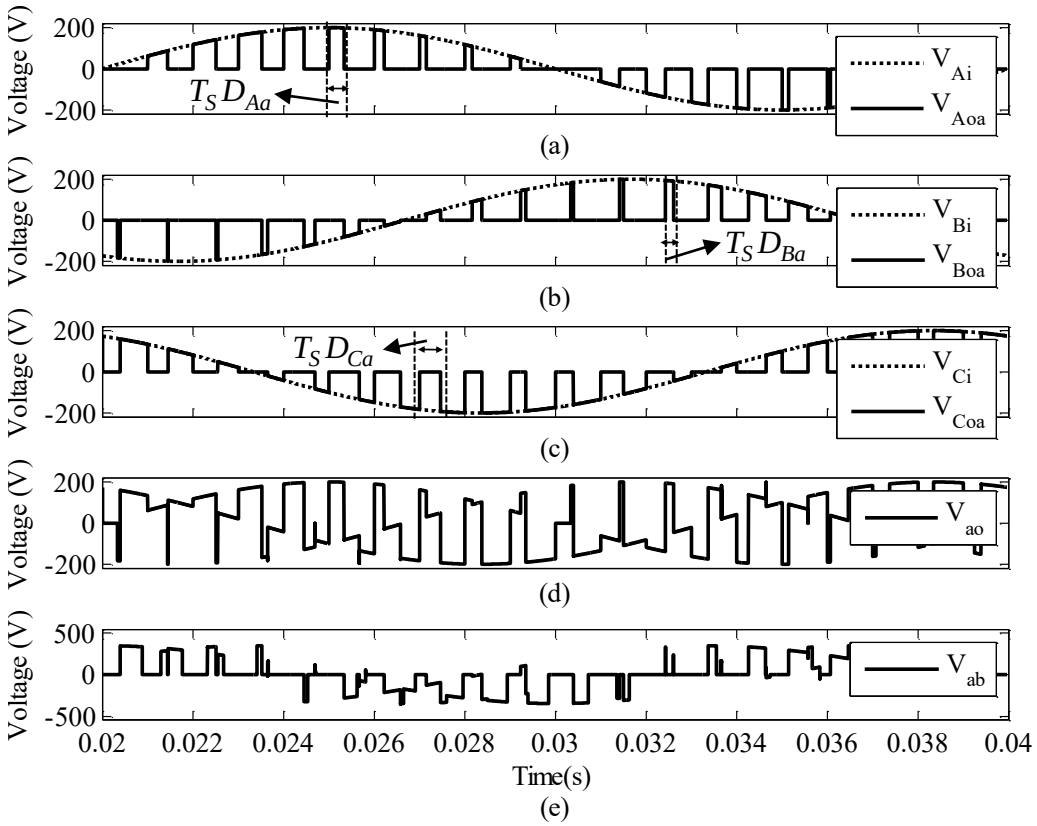


Figure 3.8: Theoretical voltage waveforms in the three-phase to three-phase MIMC as a result of the Venturini Modulation. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Total output voltage V_{ao}. (e) Phase-phase output voltage V_{ab}.

$$V_{jo} = \sum_{K=A,B,C} V_{Koj} = V_{Aoj} + V_{Boj} + V_{Coj} \tag{3.14}$$

It can be seen from Figure 3.9 that output voltage of the top-cell V_{Aoa} equals the input voltage V_{Ai} for the interval $0 \leq t \leq D_{Aa}T_S$ and is zero for the rest of the switching period i.e. $D_{Aa}T_S < t \leq T_S$. Therefore the switching function of the final output voltage V_{jo} can be expressed as (3.15), where $n = 0, 1, 2, ..., \infty$ is the number of switching period and $j = a, b, c$ represents the output phases of the MIMC.

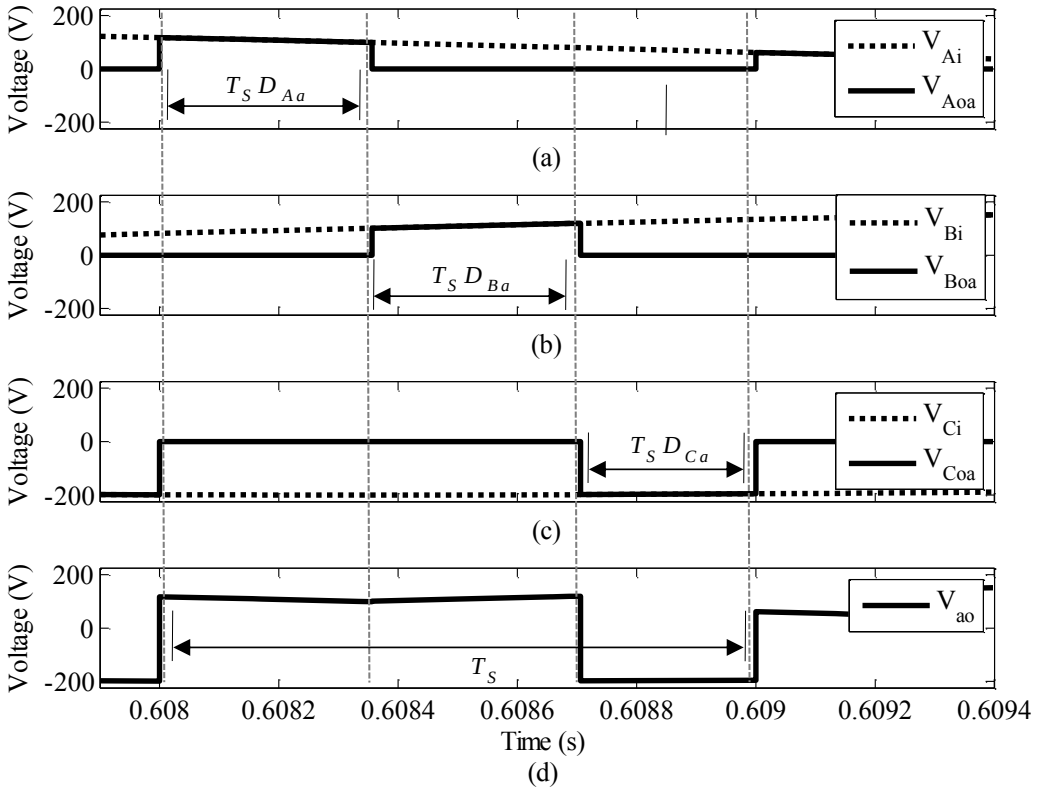


Figure 3.9: A single switching period T_S of voltages at the output of MIMC, showing the arrangement of duty cycles D_{Ka}. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Total output voltage V_{ao} of (3.7).

$$V_{jo} = \left\{ \begin{array}{c|c} Voltage & Interval \\ \hline V_{Ai} & nT_S \leq t \leq D_{Aj}(T_S + nT_S) \\ V_{Bi} & D_{Aj}(T_S + nT_S) < t \leq (D_{Aj} + D_{Bj})\,(T_S + nT_S) \\ V_{Ci} & (D_{Aj} + D_{Bj})\,(T_S + nT_S) < t \leq (T_S + nT_S) \end{array} \right\} \tag{3.15}$$

Note that harmonic spectrum of the final output voltage V_{jo} is same as of a standard Direct Matrix Converter which can be obtained by following the analytical approach discussed in [73]. However, to validate the application of the Venturini Modulation it is essential to determine how the individual cells are contributing towards generating a single frequency f_o sinusoidal waveform given in (3.7). This can simply be achieved by neglecting the switching components and determining time domain expressions for the cell's output voltage $V_{Koj}(t)$.

The output voltage $V_{Koj}(t)$ of the cell which connects K^{th} input with j^{th} output can be denoted as a function of corresponding duty cycle $D_{Kj}(t)$ and the input voltage $V_{Ki}(t)$, as shown in (3.16). Substitution of $V_{ki}(t)$ and $D_{Kj}(t)$ from (3.6) and (3.5), respectively into (3.16), results in equation (3.17). After trigonometric simplification, (3.17) can be expressed as (3.18). Since, $\phi_K = 0, -\frac{2\pi}{3}, -\frac{4\pi}{3}$ for $K = A, B, C$. For a balanced three-phase system the cell's output voltage $V_{Koj}(t)$ can then finally be expressed as shown in (3.19).

$$V_{Koj}(t) = V_{Ki}(t) D_{Kj}(t) \tag{3.16}$$

$$V_{Koj}(t) = \frac{V_m}{3} \sin(\omega_i t + \phi_K) \left[1 + 2\, q \sin(\omega_i t + \phi_K) \sin(\omega_o t + \phi_j)\right] \tag{3.17}$$

$$\begin{aligned} V_{Koj}(t) =& \frac{qV_m}{3} \sin(\omega_o t + \phi_j) + \frac{V_m}{3} \sin(\omega_i t + \phi_K) + \\ & \frac{qV_m}{6} \left[\sin(2\omega_i t + 2\phi_K - \omega_o t - \phi_j) - \sin(2\omega_i t + 2\phi_K + \omega_o t + \phi_j)\right] \end{aligned} \tag{3.18}$$

$$\begin{aligned} V_{Koj}(t) =& \frac{V_m}{3} \sin(\omega_i t + \phi_K) + \frac{qV_m}{3} \sin(\omega_o t + \phi_j) + \\ & \frac{qV_m}{6} \left[\sin(2\omega_i t - \omega_o t - \phi_K - \phi_j) - \sin(2\omega_i t + \omega_o t - \phi_K + \phi_j)\right] \end{aligned} \tag{3.19}$$

According to (3.14), the final output voltage is the sum of individual cell voltages, therefore the time domain expression for V_{Koj} can be summed for $K = A, B, C$ as shown in (3.22). From (3.22), it can be seen that the components are at frequencies of $\omega_i t$,$\omega_o t$, $2\omega_i t + \omega_o t$ and $2\omega_i t - \omega_o t$. Note that the components at frequencies $\omega_i t$, $2\omega_i t + \omega_o t$ and $2\omega_i t - \omega_o t$ have a phase difference of $\frac{2\pi}{3}$ and for a balanced system the components will be cancelled therefore leaving only a single component at ω_o, as shown in (3.23). Note that the equation (3.23) confirms that the applicability of the Venturini Modulation to the MIMC.

$$V_{jo}(t) = \sum_{K=A,B,C} V_{Koj}(t) \tag{3.20}$$

$$V_{jo}(t) = V_{Aoj}(t) + V_{Boj}(t) + V_{Coj}(t) \tag{3.21}$$

$$V_{jo}(t) = qV_m \sin(\omega_o t + \phi_j) + \frac{V_m}{3}\sin(\omega_i t) + \frac{V_m}{3}\sin\left(\omega_i t - \frac{2\pi}{3}\right) + \frac{V_m}{3}\sin\left(\omega_i t - \frac{4\pi}{3}\right) + \frac{qV_m}{6}\sin(2\omega_i t - \omega_o t - \phi_j) + \frac{qV_m}{6}\sin\left(2\omega_i t - \omega_o t - \frac{2\pi}{3} - \phi_j\right) + \frac{qV_m}{6}\sin\left(2\omega_i t - \omega_o t - \frac{4\pi}{3} - \phi_j\right) - \frac{qV_m}{6}\sin(2\omega_i t + \omega_o t - \phi_K + \phi_j) - \frac{qV_m}{6}\sin\left(2\omega_i t + \omega_o t - \frac{2\pi}{3} - \phi_j\right) - \frac{qV_m}{6}\sin\left(2\omega_i t + \omega_o t - \frac{4\pi}{3} - \phi_j\right) \quad (3.22)$$

$$V_{jo}(t) = qV_m \sin(\omega_o t + \phi_j) \quad (3.23)$$

Using the expression for the final output voltage $V_{jo}(t)$ (3.23), the time domain expressions for output current $I_{jo}(t)$ and input current $I_{Ki}(t)$ can also be derived. For an RL load at the output of the MIMC, the output current $I_{jo}(t)$ is given by (3.24). In equation (3.24), $|Z_{load}|$ and ϕ_o denote the impedance and phase of the output load respectively. In a analogous manner to the voltage, the input current $I_{Kij}(t)$ of single-cell which connects K^{th} input with j^{th} output can be denoted as a function of corresponding duty cycle $D_{Kj}(t)$ and the output current $I_{jo}(t)$ as shown in (3.29). The total input current $I_{Ki}(t)$ of phase K can be denoted by the sum of current $I_{Kij}(t)$ over $j = a, b, c$ as shown in (3.30). The expression for the input current $I_{Ki}(t)$, shown in (3.32), can be simplified as shown in (3.33) because the components at $\omega_o t$, $2\omega_o t - \omega_i t$, $2\omega_o t + \omega_i t$ cancel due to the phase difference of $\frac{2\pi}{3}$.

$$I_{jo}(t) = \frac{qV_m}{|Z_{load}|}\sin(\omega_o t + \phi_j - \phi_o) \quad (3.24)$$

$$|Z_{load}| = \sqrt{R^2 + (\omega_o L)^2}, \;\; \phi_o = \tan^{-1}\left(\frac{\omega_o L}{R}\right) \quad (3.25)$$

$$I_{Kij}(t) = I_{jo}(t)\, D_{Kj}(t) \quad (3.26)$$

$$I_{Kij}(t) = \frac{qV_m}{3\,|Z_{load}|}\sin(\omega_o t + \phi_j - \phi_o)\left[1 + 2q\sin(\omega_i t + \phi_K)\sin(\omega_o t + \phi_j)\right] \quad (3.27)$$

$$I_{Kij}(t) = \frac{qV_m}{3|Z_{load}|}\sin(\omega_o t + \phi_j - \phi_o) + \frac{q^2V_m}{3|Z_{load}|}\sin(\omega_i t + \phi_K)\cos(\phi_o) + \frac{q^2V_m}{6|Z_{load}|}\left[\sin(2\omega_o t - \omega_i t - \phi_K + 2\phi_j - \phi_o) - \sin(2\omega_o t + \omega_i t + \phi_K + 2\phi_j - \phi_o)\right] \tag{3.28}$$

$$I_{Kij}(t) = \frac{qV_m}{3|Z_{load}|}\sin(\omega_o t + \phi_j - \phi_o) + \frac{q^2V_m}{3|Z_{load}|}\sin(\omega_i t + \phi_K)\cos(\phi_o) + \frac{q^2V_m}{6|Z_{load}|}\left[\sin(2\omega_o t - \omega_i t - \phi_K - \phi_j - \phi_o) - \sin(2\omega_o t + \omega_i t + \phi_K - \phi_j - \phi_o)\right] \tag{3.29}$$

$$I_{ki}(t) = \sum_{j=a,b,c} I_{Kij}(t) \tag{3.30}$$

$$I_{ki}(t) = I_{Kia}(t) + I_{Kib}(t) + I_{Kic}(t) \tag{3.31}$$

$$\begin{aligned} I_{Ki}(t) = {} & \frac{q^2V_m}{|Z_{load}|}\sin(\omega_i t + \phi_K)\cos(\phi_o) + \frac{qV_m}{3|Z_{load}|}\sin(\omega_o t - \phi_o) + \\ & \frac{qV_m}{3|Z_{load}|}\sin\left(\omega_o t - \frac{2\pi}{3} - \phi_o\right) + \frac{qV_m}{3|Z_{load}|}\sin\left(\omega_o t - \frac{4\pi}{3} - \phi_o\right) + \\ & \frac{q^2V_m}{6|Z_{load}|}\left[\sin(2\omega_o t - \omega_i t - \phi_K - \phi_o) + \sin\left(2\omega_o t - \omega_i t - \phi_K + \frac{2\pi}{3} - \phi_o\right)\right] + \\ & \frac{q^2V_m}{6|Z_{load}|}\left[\sin\left(2\omega_o t - \omega_i t - \phi_K + \frac{4\pi}{3} - \phi_o\right) - \sin(2\omega_o t + \omega_i t + \phi_K - \phi_o)\right] - \\ & \frac{q^2V_m}{6|Z_{load}|}\left[\sin\left(2\omega_o t + \omega_i t + \phi_K + \frac{2\pi}{3} - \phi_o\right) + \sin\left(2\omega_o t + \omega_i t + \phi_K + \frac{4\pi}{3} - \phi_o\right)\right] \end{aligned} \tag{3.32}$$

$$I_{Ki}(t) = \frac{q^2V_m\cos(\phi_o)}{|Z_{load}|}\sin(\omega_i t + \phi_K) \tag{3.33}$$

The theoretical expressions for the cell's output voltage V_{Koj}, final output voltage V_{jo}, cell's input current I_{Kij} and final input current I_{Ki} must be validated. In order to validate that the expressions hold true, the switching functions shown in (3.8), (3.11)-(3.13) were implemented in PLECS and the harmonic spectrum of top-cell's output voltage V_{Koa} is shown in Figure 3.10. The parameters used in PLECS simulation are listed in Table 3.1. Note that in Figure 3.10, the magnitudes of the components are displayed as percentage of the peak value of the input voltage V_m. It can be seen

Table 3.1: PLECS simulation parameters

Parameter	Symbol	Value
Input Voltage Amplitude	V_m	200 $V(PEAK)$
Input Frequency	f_i	50 Hz
Output Frequency	f_o	60 Hz
Voltage Regulation Ratio	q	0.5
Transformer Turn Ratio	N	1
Load Resistance	R	10 Ω
Load Inductance	L	10 mH

from Figure 3.10 that the components are at 40 Hz ($2\omega_i - \omega_o$), 50 Hz (ω_i), 60 Hz (ω_o) and 160 Hz ($2\omega_i + \omega_o$) and are having magnitudes 8.25 % ($\frac{qV_m}{6}$), 33.3 % ($\frac{V_m}{3}$), 16.5 % ($\frac{qV_m}{3}$) and 8.25 % ($\frac{qV_m}{6}$), respectively. Therefore, the harmonic spectrum of the top-cell's output voltage V_{Koa} is in accordance with the expression shown in (3.19). The harmonic spectrum of all the cells in the MIMC are same to Figure 3.10.

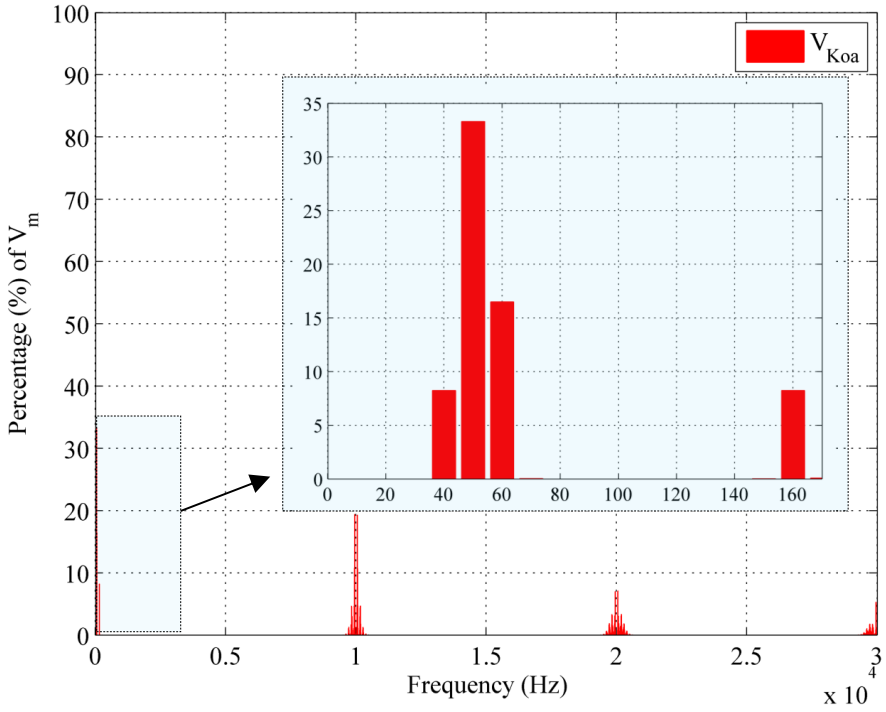


Figure 3.10: Harmonic spectrum of the cell's output voltage V_{Koa} as a result of the Venturini Modulation

The harmonic spectrum of the final output voltage V_{jo} must be observed to confirm that the components other than the component at ω_o are eliminated. In this regard, the spectrum of V_{ao} is shown in Figure 3.11. It can be clearly seen that the components, other than that at the output frequency f_o, are cancelled which validates (3.23) that frequency adaptation is achieved by employing the switching functions (3.8), (3.11)-(3.13) on the MIMC. It can also be seen from Figure 3.11 that the maximum voltage regulation ratio achieved using the Venturini Modulation method is 0.5 as the magnitude of the fundamental component at f_o=60 Hz is 50% of the peak value of the input voltage V_m.

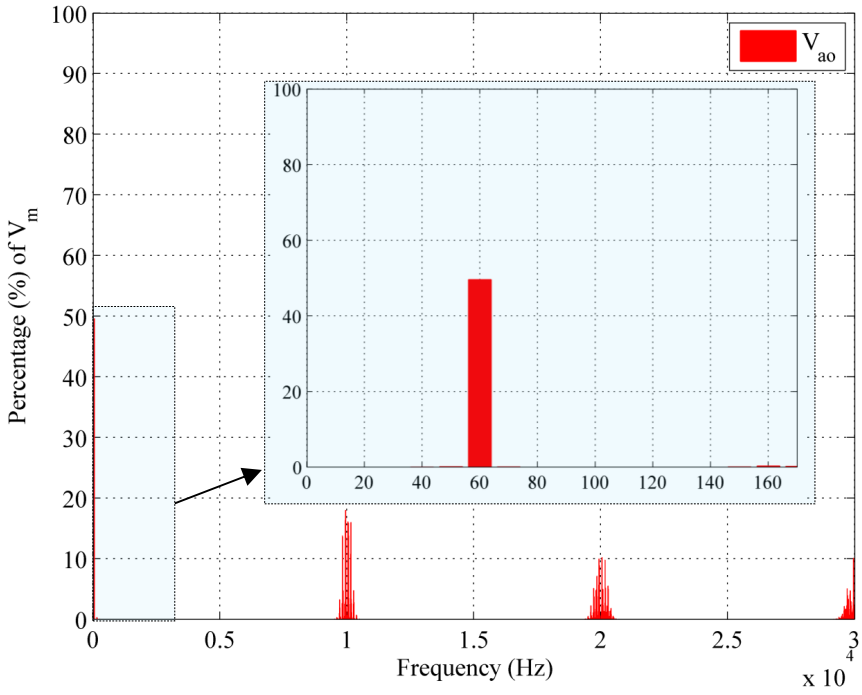


Figure 3.11: Harmonic spectrum of the final voltage V_{ao} as a result of the Venturini Modulation

The harmonic spectrum of the cell's input current I_{Aij} is shown in Figure 3.12 which validates that the components in current are in accordance with the expression shown in (3.29). All the components in Figure 3.12, except the one at the input frequency f_i, will be cancelled in the final input current I_{Ki}. To validate this, harmonic spectrum of final input current I_{Ki}, obtained through PLECS simulation, is shown in Figure 3.13.

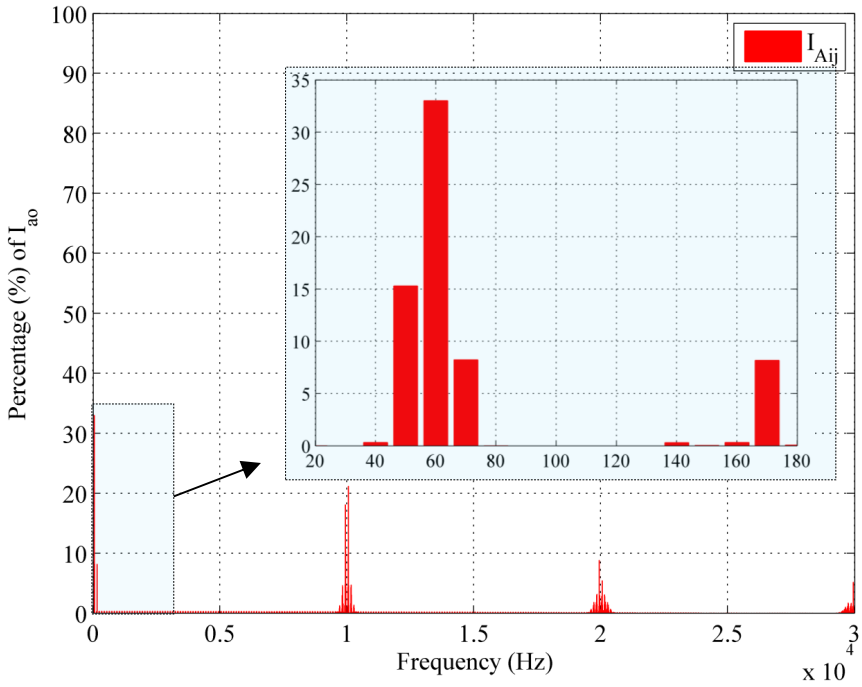


Figure 3.12: Harmonic spectrum of the cell's input current I_{Aij} as a result of the Venturini Modulation

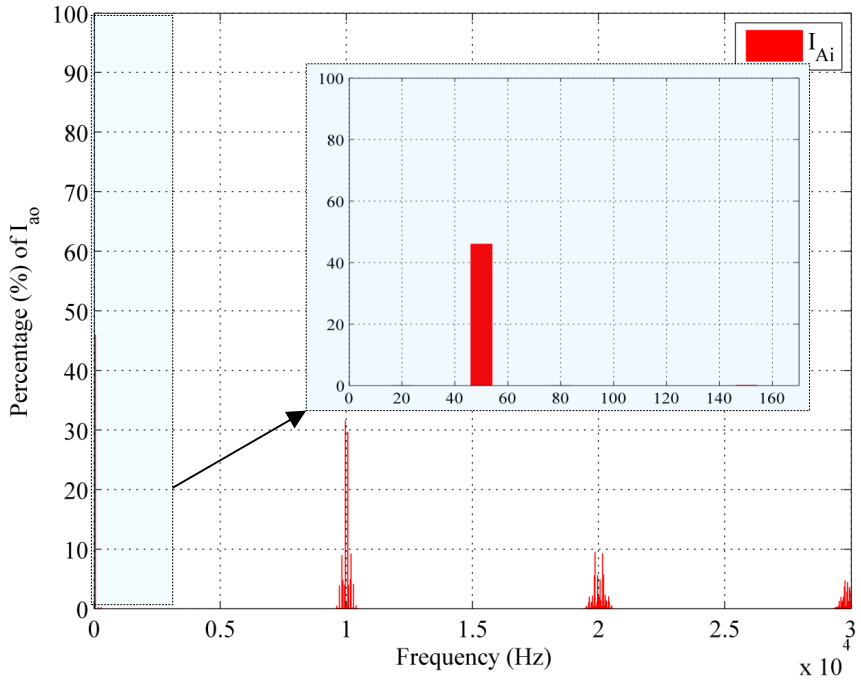


Figure 3.13: Harmonic spectrum of the total input current I_{Ai} as a result of the Venturini Modulation

The harmonic spectrums shown in Figure 3.10-3.13 have proved that the application of the Venturini Modulation method to the MIMC and that a voltage regulation ratio of 0.5 can be achieved. However, due to the availability of a large number of switches in the MIMC, the bridges can also be modulated in a way to increase voltage regulation ratio from 0.5 to unity. This will require a modification of the switching functions implementing the Venturini Modulation which will be explained in Section 3.3.

3.3 Double Venturini Modulation

The Venturini Modulation method applied to the MIMC can be extended to achieve a maximum voltage regulation ratio of unity. The extended version of the Venturini Modulation method, which will cause a two-fold increase in the voltage regulation ratio, has been named the *'Double Venturini Modulation'* method. Note that this two-fold increase in the voltage regulation is peculiar to the MIMC only and can not be achieved in the Direct Matrix Converter due to the limited number of possible output voltages.

From the Venturini Modulation method, it can be seen that at a time t only a single-cell is connected to the output. For example, if the top-cell of the MIMC, shown in Figure 3.3, is ON then the other two cells are being by-passed making the output voltage $V_{jo} = V_{Ai}$. However, if the middle and bottom cells are not by-passed and instead modulated to generate $-V_{Bi}$ and $-V_{Ci}$ in this case then the output voltage $V_{jo} = V_{Ai} - V_{Bi} - V_{Ci}$ will lead to $V_{jo} = 2V_{Ai}$ with a balanced system. Therefore, the Double Venturini Modulation method exploits the benefit of having a three-phase balanced system to increase the voltage transfer ratio. To implement Double Venturini Modulation on the MIMC, the switching functions of the output side bridges, shown in (3.11)-(3.13), require adaptation. The modified switching functions are shown in (3.34)-(3.36).

V_{Aoj}	MS_{Aoj}	*Interval*	*Condition*
V_{Ai}	MS_1	$nT_S \leq t \leq D_{Aj}(T_S + nT_S)$	
$-V_{Ai}$	MS_2	$D_{Aj}(T_S + nT_S) < t \leq 0.5(T_S + nT_S)$	$D_{Aj} \leq 0.5$
$-V_{Ai}$	MS_1	$0.5(T_S + nT_S) < t \leq (T_S + nT_S)$	
V_{Ai}	MS_1	$nT_S \leq t \leq 0.5(T_S + nT_S)$	
V_{Ai}	MS_2	$0.5(T_S + nT_S) < t \leq D_{Aj}(T_S + nT_S)$	$D_{Aj} > 0.5$
$-V_{Ai}$	MS_1	$D_{Aj}(T_S + nT_S) < t \leq (T_S + nT_S)$	

(3.34)

V_{Boj}	MS_{Boj}	*Interval*	*Condition*
$-V_{Bi}$	MS_2	$nT_S \leq t \leq D_{Aj}(T_S + nT_S)$	
V_{Bi}	MS_1	$D_{Aj}(T_S + nT_S) < t \leq 0.5(T_S + nT_S)$	$D_{Aj} \leq 0.5$
V_{Bi}	MS_2	$0.5(T_S + nT_S) < t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	$\leq (D_{Aj} + D_{Bj})$
$-V_{Bi}$	MS_1	$(D_{Aj} + D_{Bj})(T_S + nT_S) < t \leq (T_S + nT_S)$	
$-V_{Bi}$	MS_2	$nT_S \leq t \leq 0.5(T_S + nT_S)$	
$-V_{Bi}$	MS_1	$0.5(T_S + nT_S) < t \leq D_{Aj}(T_S + nT_S)$	$0.5 \leq D_{Aj}$
V_{Bi}	MS_2	$D_{Aj}(T_S + nT_S) < t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	
$-V_{Bi}$	MS_1	$(D_{Aj} + D_{Ba})(T_S + nT_S) < t \leq (T_S + nT_S)$	
$-V_{Bi}$	MS_2	$nT_S \leq t \leq D_{Aj}(T_S + nT_S)$	
V_{Bi}	MS_1	$D_{Aj}(T_S + nT_S) < t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	$(D_{Aj} + D_{Bj})$
$-V_{Bi}$	MS_2	$(D_{Aj} + D_{Bj})(T_S + nT_S) < t \leq 0.5(T_S + nT_S)$	≤ 0.5
$-V_{Bi}$	MS_1	$0.5(T_S + nT_S) < t \leq (T_S + nT_S)$	

(3.35)

V_{Coj}	MS_{Coj}	*Interval*	*Condition*
$-V_{Ci}$	MS_2	$nT_S \leq t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	$(D_{Aj} + D_{Bj})$
V_{Ci}	MS_1	$(D_{Aj} + D_{Bj})(T_S + nT_S) < t \leq 0.5(T_S + nT_S)$	≤ 0.5
V_{Ci}	MS_2	$0.5(T_S + nT_S) < t \leq (T_S + nT_S)$	
$-V_{Ci}$	MS_2	$nT_S \leq t \leq 0.5(T_S + nT_S)$	
$-V_{Ci}$	MS_1	$0.5(T_S + nT_S) < t \leq (D_{Aj} + D_{Bj})(T_S + nT_S)$	$(D_{Aj} + D_{Bj})$
V_{Ci}	MS_2	$(D_{Aj} + D_{Bj})(T_S + nT_S) < t \leq (T_S + nT_S)$	> 0.5

(3.36)

It is important to note that the waveforms for the Double Venturini Modulation method will be different than those obtained with Venturini Modulation. Figure 3.14 show the waveforms within a top-cell of the MIMC. From Figure 3.14, it can be seen that the output voltage of cell V_{Koa} is bipolar when compared with the waveform in Figure 3.6, which also indicates that the Double Venturini Modulation employs active steady-states only with no zero states. A zoomed view of Figure 3.14 is shown in Figure 3.15 to highlight which steady-states are employed and that these states are in accordance with the switching function shown in (3.34).

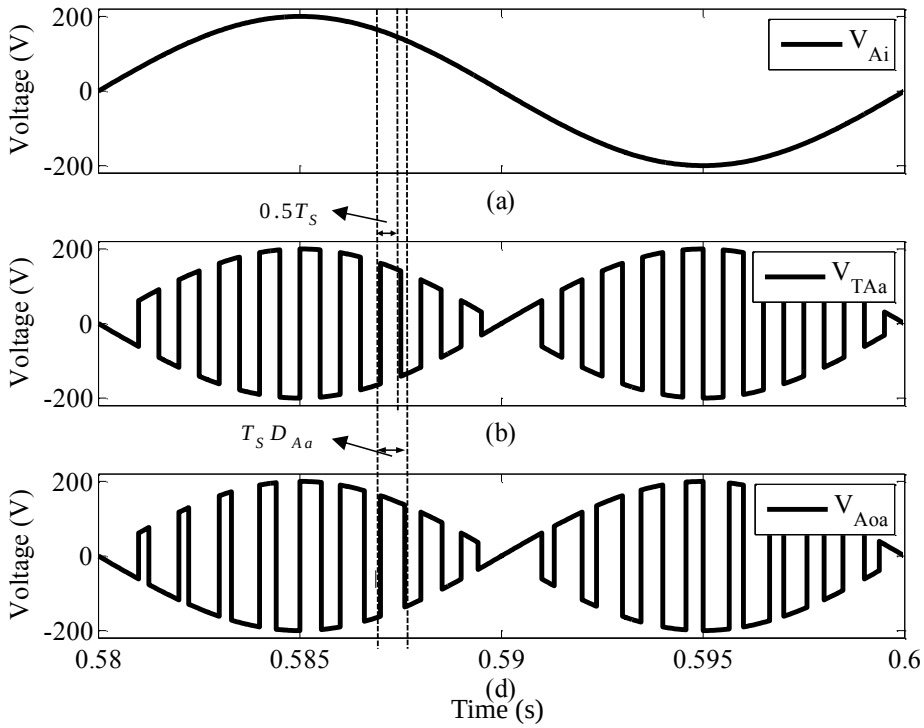


Figure 3.14: Theoretical voltage waveforms in the top-cell as a result of the Double Venturini Modulation: (a) Input voltage V_{Ai}. (b) Transformer voltage V_{TAa}. (d) Output voltage V_{Aoa}.

During the single switching period T_S, shown in Figure 3.15, the duty cycle $D_{Aa} < 0.5$. Therefore, the first condition of equation (3.34) becomes valid and the states MS_1, MS_2 and MS_1 are applied for intervals $0 \leq t \leq D_{Aj}T_S$, $D_{Aj}T_S < t \leq 0.5T_S$ and $0.5T_S < t \leq T_S$, respectively in the output bridge of the top-cell. Note that the switching functions of the input side bridges remain the same as defined in (3.8) for the Venturini Modulation $MS_{Kij} = MS_1$ for the interval $0 \leq t \leq 0.5T_S$ and $MS_{Aia} = MS_2$ for the remaining interval $0.5T_S < t \leq T_S$ therefore, the steady-state in form $MS_{Aia}MS_{Aoa}$ are applied in a sequence of MS_1MS_1, MS_1MS_2, MS_2MS_1. The same sequence can be seen in Figure 3.15, confirming that the top-cell is modulating the output voltage V_{Aoa} according to the switching function given in (3.34). In a similar manner, the waveforms for all the cells can be verified corresponding to their switching functions.

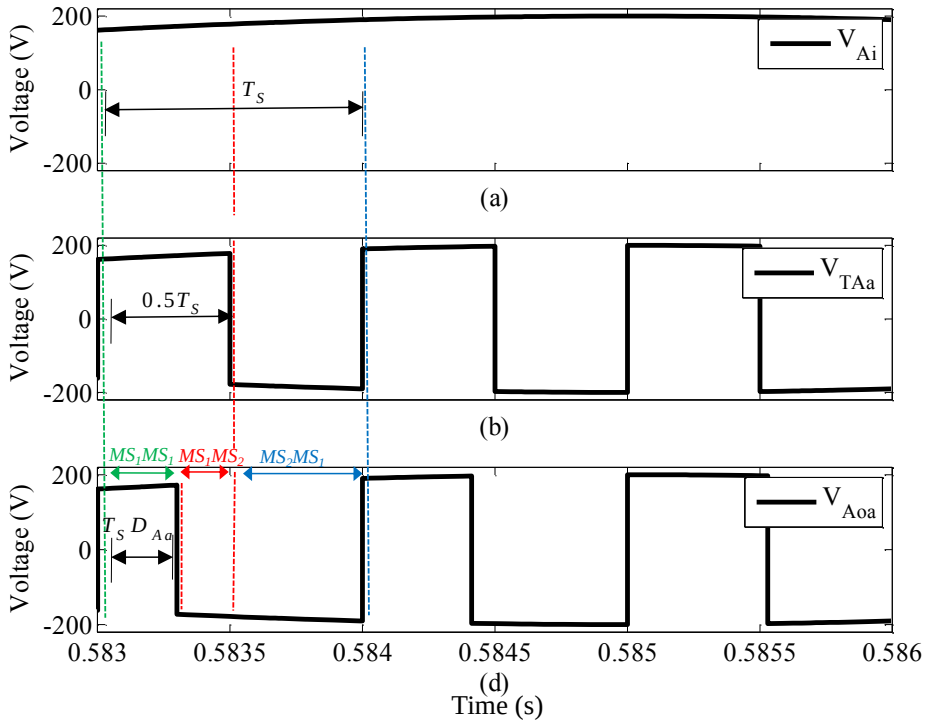


Figure 3.15: A zoomed view of Figure 3.14, focussing on a single switching period T_S (a) Input voltage V_{Ai}. (b) Transformer voltage V_{TAa}. (d) Output voltage V_{Aoa}.

Figures 3.16(a)-(c) shows the output voltages V_{Koa} of individual cells where $K = A, B, C$ for the top, middle and bottom cells, respectively. It is important to note that the amplitude of the final output voltage V_{ao}, shown in Figure 3.16(d) is doubled when compared with the Venturini Modulation shown in Figure 3.8(d).

To highlight that the waveform shown in Figure 3.16(d) follows (3.14), a single switching period T_S is shown in Figure 3.17. In Figure 3.17, consider the interval $0 \leq t \leq T_S D_{Aa}$ during which the output voltage of top-cell is $V_{Aoa} = V_{Ai}$ but meanwhile the output voltages of the other two cells are $V_{Boa} = -V_{Bi}$ and $V_{Coa} = -V_{Ci}$, respectively making the final output voltage $V_{ao} = 2V_{Ai}$. Therefore, the final output voltage obtained with the Double Venturini Modulation is double as that obtained with the Venturini Modulation as expressed in (3.37). Note that in equation (3.37) the maximum value of voltage transfer ratio q is 0.5.

$$V_{jo} = 2qV_m \sin(\omega_o t + \phi_j) \tag{3.37}$$

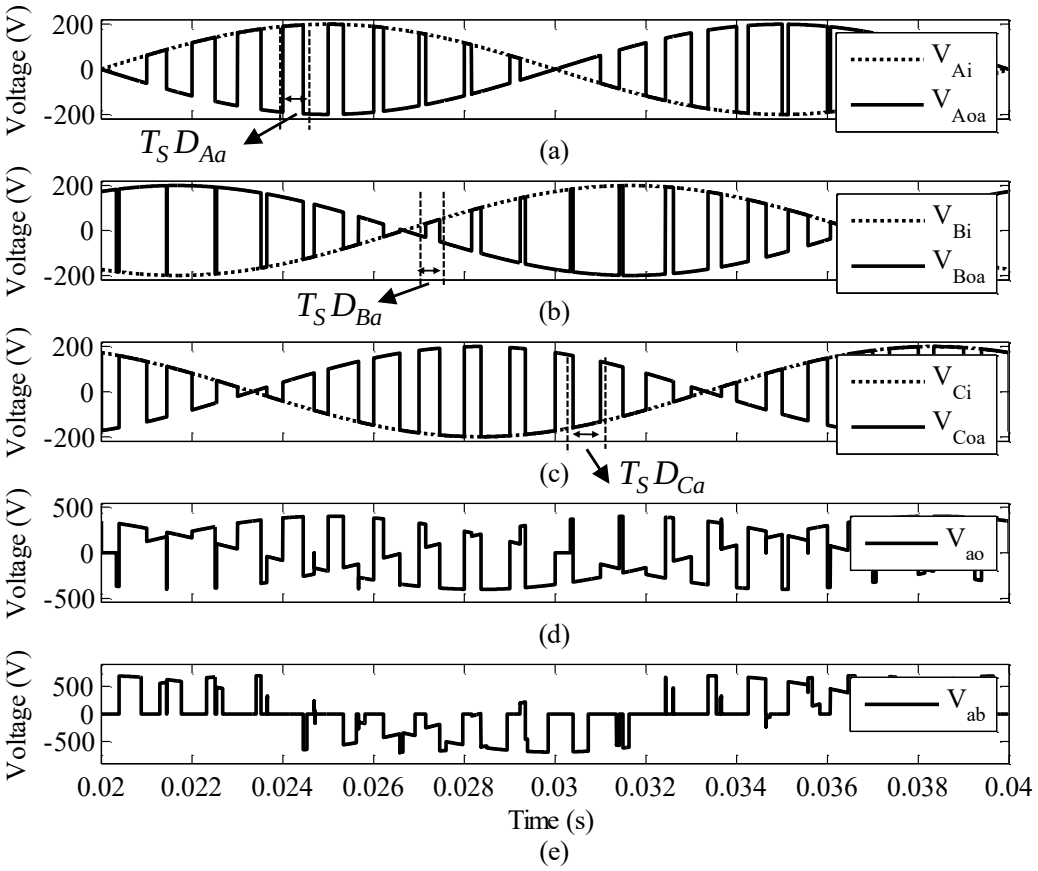


Figure 3.16: Theoretical voltage waveforms in the three-phase to three-phase MIMC as a result of the Double Venturini Modulation. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Output voltage V_{ao}. (e) Phase-phase output voltage V_{ab}.

The output voltage waveform for a single-cell V_{Koj} with the Double Venturini Modulation, shown in Figure 3.14(d), is not the same as that obtained with the Venturini Modulation. Therefore the time domain expression for the cell's output voltage $V_{Koj}(t)$ can be recalculated using (3.16), and simplified to a form as shown in (3.39).

$$V_{Koj}(t) = \frac{V_m}{3}\sin(\omega_i t + \phi_K)\left[1 + 4\,q\sin(\omega_i t + \phi_K)\sin(\omega_o t + \phi_j)\right] \tag{3.38}$$

$$\begin{aligned} V_{Koj}(t) =& \frac{V_m}{3}\sin(\omega_i t + \phi_K) + \frac{2qV_m}{3}\sin(\omega_o t + \phi_j) + \\ & \frac{qV_m}{3}\left[\sin(2\omega_i t - \omega_o t - \phi_K - \phi_j) - \sin(2\omega_i t + \omega_o t - \phi_K + \phi_j)\right] \end{aligned} \tag{3.39}$$

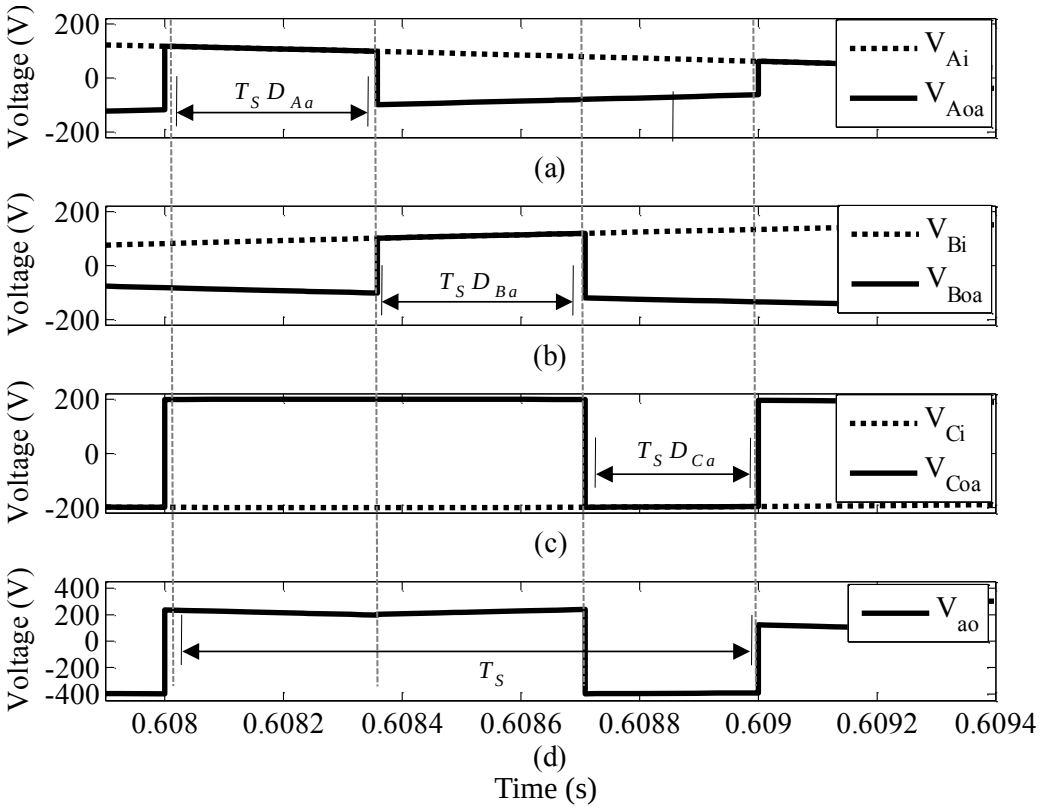


Figure 3.17: A single switching period T_S of voltages at the output of MIMC, showing the arrangement of duty cycles D_{Ka}. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Total output voltage V_{ao} of (3.37).

The output current $I_{jo}(t)$ for the Double Venturini Modulation as a result of final output voltage $V_{jo}(t)$ can be expressed using (3.40) and the input current of a single-cell I_{Kij} can be written as:

$$I_{jo}(t) = \frac{2qV_m}{|Z_{load}|} \sin(\omega_o t + \phi_j - \phi_o) \tag{3.40}$$

$$I_{Kij}(t) = \frac{2qV_m}{3|Z_{load}|} \sin(\omega_o t + \phi_j - \phi_o)\left[1 + 4q \sin(\omega_i t + \phi_K) \sin(\omega_o t + \phi_j)\right] \tag{3.41}$$

$$\begin{aligned} I_{Kij}(t) = & \frac{2qV_m}{3|Z_{load}|} \sin(\omega_o t + \phi_j - \phi_o) + \frac{4q^2V_m}{3|Z_{load}|} \sin(\omega_i t + \phi_K) \cos(\phi_o) + \\ & \frac{2q^2V_m}{3|Z_{load}|} \left[\sin(2\omega_o t - \omega_i t - \phi_K - \phi_j - \phi_o) - \sin(2\omega_o t + \omega_i t + \phi_K - \phi_j - \phi_o)\right] \end{aligned} \tag{3.42}$$

The total input current $I_{Ki}(t)$ of an input phase K, with $K = A, B, C$, can be written as:

$$I_{Ki}(t) = \frac{4q^2 V_m \cos(\phi_o)}{|Z_{load}|} \sin(\omega_i t + \phi_K) \tag{3.43}$$

In order to verify that the theoretical expressions for the cell's output voltage $V_{Koj}(t)$, input current $I_{Kij}(t)$, total output voltage $V_{jo}(t)$ and total input current $I_{Ki}(t)$ can be obtained from of the switching functions shown in (3.34)-(3.36), a PLECS simulation was performed. The parameters for the simulation were kept same as those used in the Venturini Modulation, as shown in Table 3.1. The harmonic spectrum of the output voltage of single-cell V_{Koj} is shown in Figure 3.18. In Figure 3.18 the magnitudes of the components are displayed as percentage of the peak value of the input voltage V_m. It can be seen from Figure 3.18 that the components are at 40 Hz, 50 Hz, 60 Hz and 160 Hz and are having magnitudes 16.7 % ($\frac{qV_m}{3}$), 33.3 % ($\frac{V_m}{3}$), 33.3 % ($\frac{2qV_m}{3}$) and 16.7 % ($\frac{qV_m}{3}$), respectively. Therefore, the harmonic spectrum of the cell's output voltage V_{Koa} is in accordance with the expression shown in (3.39).

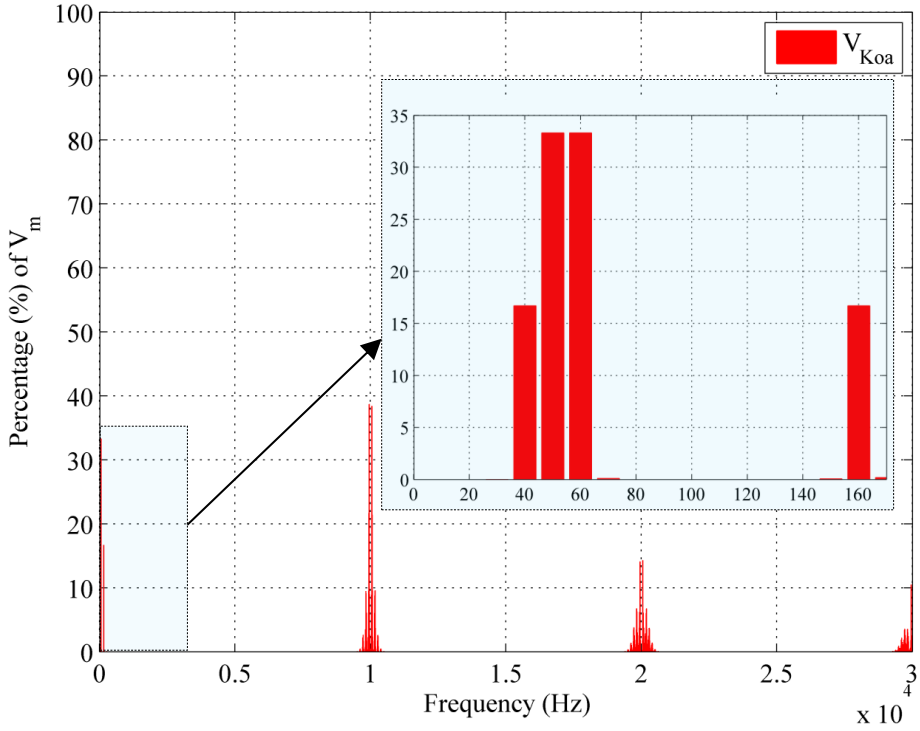


Figure 3.18: Harmonic spectrum of the cell's output voltage V_{Koa} as a result of the Double Venturini Modulation

In order to verify that the final output voltage has a single low frequency component at 60 Hz, and that all the the other components are cancelled the simulated harmonic spectrum of $V_{ao}(t)$ is shown in Figure 3.19. It is important to note that the magnitude of the component at 60 Hz shown in Figure 3.19 is double the magnitude of those obtained with the Venturini Modulation (Figure 3.11), this demonstrates that feasibility of the Double Venturini Modulation for the MIMC.

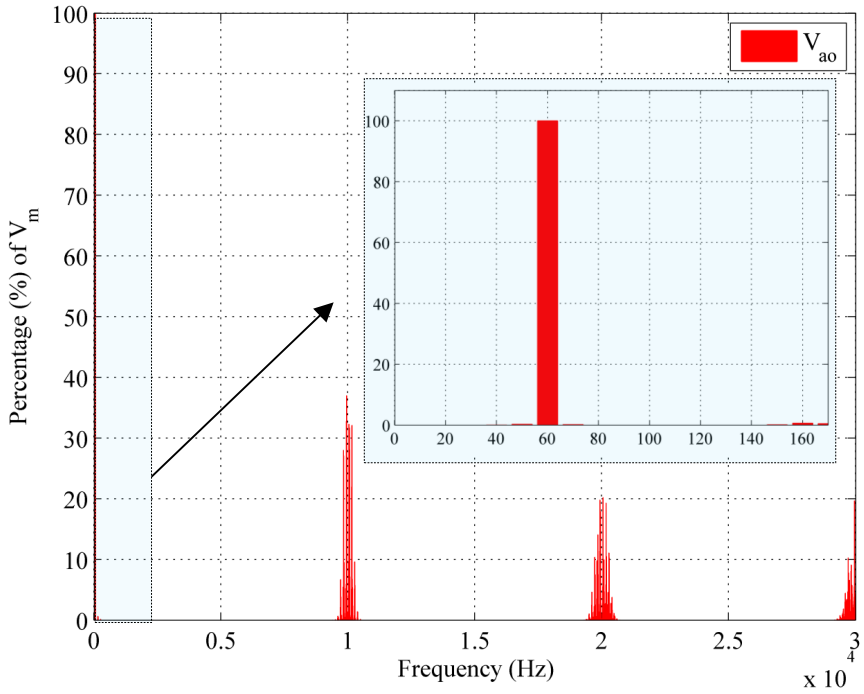


Figure 3.19: Harmonic spectrum of the final voltage V_{ao} as a result of the Double Venturini Modulation

Figure 3.20 shows the harmonic spectrum of cell's input current $I_{Kij}(t)$. The components in Figure 3.20 are plotted as a percentage of the peak output current. Note that the components and their magnitudes in Figure 3.20 are in accordance with (3.42). Finally, to validate that the final input current has a single low frequency component at 50 Hz and that all the other components are cancelled, simulated harmonic spectrum of final input current $I_{Ai}(t)$ is shown in Figure 3.21. The Double Venturini Modulation offers a two fold increase in the voltage regulation ratio, the magnitude of the total input current I_{Ki} will be twice that obtained with the Venturini Modulation, as seen by comparing Figure 3.21 with Figure 3.13.

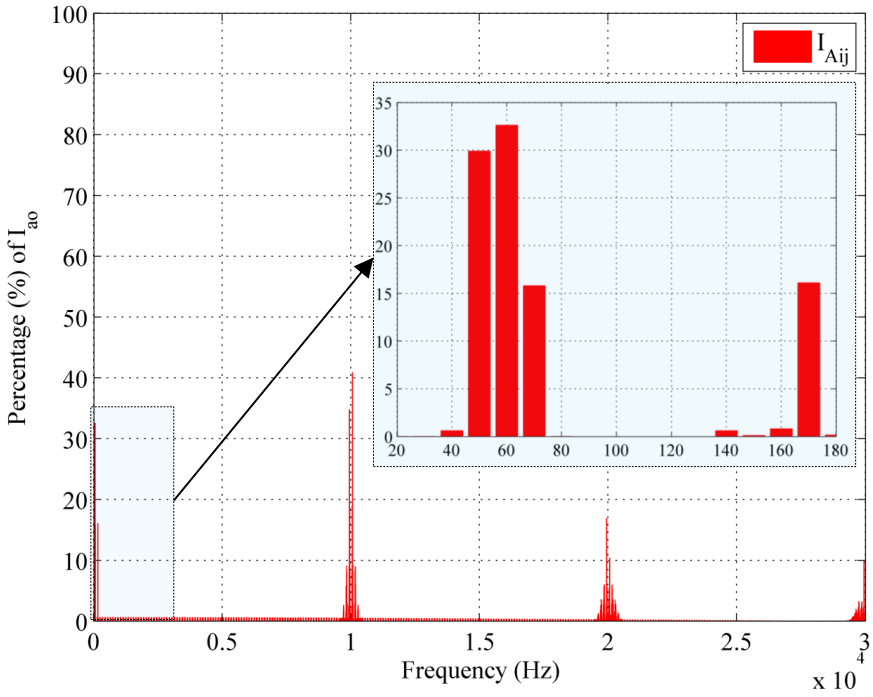


Figure 3.20: Harmonic spectrum of the cell's input current I_{Aij} as a result of the Double Venturini Modulation

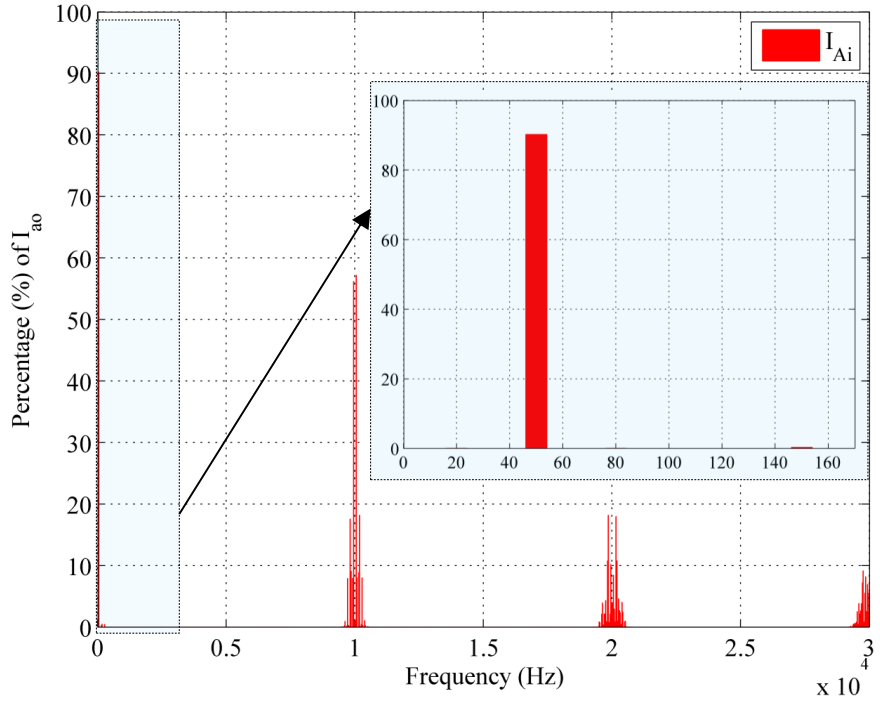


Figure 3.21: Harmonic spectrum of the total input current I_{Ai} as a result of the Double Venturini Modulation

3.4 Double Optimum Venturini Modulation

The maximum voltage regulation ratio obtained with the Double Venturini Modulation is unity but this can further be increased by employing a third harmonic injection scheme. The concept of third harmonic injection scheme was also introduced by Alesina and Venturini to increase the voltage regulation ratio of the standard Matrix Converter from 0.5 to 0.86 [74]. However when the same third harmonic injection scheme is applied to the MIMC, the voltage regulation ratio of the MIMC can be increased from unity to 1.73. The harmonics of both the input and the output frequencies are added in the output voltage V_{jo} to fully utilise the envelope of the input voltage V_{Ki}. In order to implement the *Double Optimum Venturini Modulation* on the MIMC, equations of duty cycle D_{Kj}, input voltage V_{Ki}, output voltage V_{jo} must be updated to (3.44)-(3.46) [75]. The third harmonic injection equation, shown in (3.44), is same as used in the Matrix Converters for a unity input power factor [74]. Note that the switching functions shown in (3.34)-(3.36) are still valid. These functions have already been validated by results obtained using PLECS simulation in Section 3.3. Therefore the switching waveforms are not shown in this Section for the sake of conciseness. However a PLECS simulated harmonic spectrum is shown in Section 3.6 (Figure 3.31) which validates that a voltage regulation ratio of 1.73 is achievable with the Double Optimum Venturini Modulation.

$$D_{Kj} = \frac{1}{3}\left(1 + \frac{2V_{Ki}V_{jo}}{{V_m}^2} + \frac{4q\sin\left(\omega_i t + \phi_K\right)}{3\sqrt{3}}\right) \tag{3.44}$$

$$V_{Ki} = V_m \cos\left(\omega_i t + \phi_K\right) \tag{3.45}$$

$$V_{jo} = qV_m[\cos\left(\omega_o t + \phi_j\right) - \frac{1}{6}\cos\left(3\omega_o t\right) + \frac{1}{2\sqrt{3}}\cos\left(3\omega_i t\right)] \tag{3.46}$$

The discussed modulation methods, including Venturini Modulation, Double Venturini Modulation and Double Optimum Venturini Modulation are a type of scalar modulation techniques. Due to a large number of semiconductor devices and a series connection at the output side in the MIMC, there are more possible switching combinations that can be explored using a more sophisticated approach known as the *Space Vector Modulation (SVM).*

3.5 Space Vector Modulation

The SVM of the MIMC can be developed by following the similar approach used for the SVM of the Matrix Converter [76]. To describe the development of the SVM method the generalised three-phase to single-phase MIMC can be considered as shown in Figure 3.22. The three-phase to single-phase MIMC has 24 bidirectional switches. The number of bidirectional switches will increase to 72 for the complete three-phase to three-phase MIMC system and with each switch having two states, either ON(1) or OFF(0), giving a total of 2^{72} combinations. For such a large number of switch state combinations the determination of possible states and their corresponding space vectors, when done manually, can be laborious. However, the possible states can easily be determined with a help of the computer programs such as MATLAB.

In order to compute the space vectors using MATLAB, the first step is to generate a model of the MIMC. The MIMC circuit, shown in Figure 3.22, can be modelled using equations which relate the output voltages to the input voltages and the input currents to the output currents. The equations relating the transformer voltage V_{TKj} with the respective input voltage V_{Ki} can be written as:

$$V_{TAj} = (S_{WAij}S_{XAij} - S_{YAij}S_{ZAij})V_{Ai} \tag{3.47}$$

$$V_{TBj} = (S_{WBij}S_{XBij} - S_{YBij}S_{ZBij})V_{Bi} \tag{3.48}$$

$$V_{TCj} = (S_{WCij}S_{XCij} - S_{YCij}S_{ZCij})V_{Ci} \tag{3.49}$$

The relation between the cell output voltage V_{Koj} and the input voltage V_{Ki} can be expressed using equations (3.50)-(3.52) and the final output voltage V_{jo} can be expressed as shown in (3.53).

$$V_{Aoj} = (S_{WAoj}S_{XAoj} - S_{YAoj}S_{ZAoj})(S_{WAij}S_{XAij} - S_{YAij}S_{ZAij})V_{Ai} \tag{3.50}$$

$$V_{Boj} = (S_{WBoj}S_{XBoj} - S_{YBoj}S_{ZBoj})(S_{WBij}S_{XBij} - S_{YBij}S_{ZBij})V_{Bi} \tag{3.51}$$

$$V_{Coj} = (S_{WCoj}S_{XCoj} - S_{YCoj}S_{ZCoj})(S_{WCij}S_{XCij} - S_{YCij}S_{ZCij})V_{Ci} \tag{3.52}$$

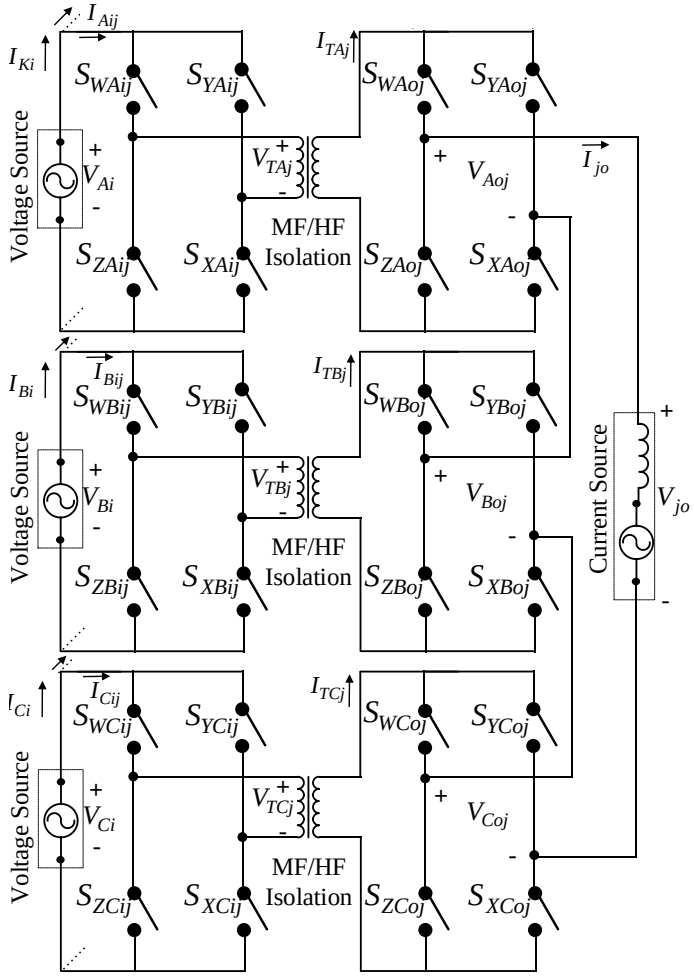


Figure 3.22: A generalised three-phase to single-phase MIMC

$$\begin{aligned} V_{jo} =&(S_{WAoj}S_{XAoj} - S_{YAoj}S_{ZAoj})(S_{WAij}S_{XAij} - S_{YAij}S_{ZAij})V_{Ai} \\ &+(S_{WBoj}S_{XBoj} - S_{YBoj}S_{ZBoj})(S_{WBij}S_{XBij} - S_{YBij}S_{ZBij})V_{Bi} \\ &+(S_{WCoj}S_{XCoj} - S_{YCoj}S_{ZCoj})(S_{WCij}S_{XCij} - S_{YCij}S_{ZCij})V_{Ci} \end{aligned} \tag{3.53}$$

In a similar manner, transformer current I_{TKj} can be expressed as function of output current I_{jo} (3.54)-(3.56).

$$I_{TAj} = (S_{WAoj}S_{XAoj} - S_{YAoj}S_{ZAoj})I_{jo} \tag{3.54}$$

$$I_{TBj} = (S_{WBoj}S_{XBoj} - S_{YBoj}S_{ZBoj})I_{jo} \tag{3.55}$$

$$I_{TCj} = (S_{WCoj}S_{XCoj} - S_{YCoj}S_{ZCoj})I_{jo} \tag{3.56}$$

The cell input current I_{Kij} and the final input current I_{Ki} can be expressed as shown in (3.57)-(3.59) and the final input current, due to a parallel connection of the cells at the input side, can be expressed as given by (3.60).

$$I_{Aij} = (S_{WAij}S_{XAij} - S_{YAij}S_{ZAij})(S_{WAoj}S_{XAoj} - S_{YAoj}S_{ZAoj})I_{jo} \tag{3.57}$$

$$I_{Bij} = (S_{WBij}S_{XBij} - S_{YBij}S_{ZBij})(S_{WBoj}S_{XBoj} - S_{YBoj}S_{ZBoj})I_{jo} \tag{3.58}$$

$$I_{Cij} = (S_{WCij}S_{XCij} - S_{YCij}S_{ZCij})(S_{WCoj}S_{XCoj} - S_{YCoj}S_{ZCoj})I_{jo} \tag{3.59}$$

$$\begin{aligned} I_{Ki} =& (S_{WKia}S_{XKia} - S_{YKia}S_{ZKia})(S_{WKoa}S_{XKoa} - S_{YKoa}S_{ZKoa})I_{ao} \\ &+(S_{WKib}S_{XKib} - S_{YKib}S_{ZKib})(S_{WKob}S_{XKob} - S_{YKob}S_{ZKob})I_{bo} \\ &+(S_{WKic}S_{XKic} - S_{YKic}S_{ZKic})(S_{WKoc}S_{XKoc} - S_{YKoc}S_{ZKoc})I_{co} \end{aligned} \tag{3.60}$$

Equations (3.47)-(3.60) define the switching model of the MIMC circuit only and do not indicate the presence of voltage and current sources in the circuit. The information that the input side in the MIMC behaves as a voltage source while the output side behaves as a current source is essential in determining the possible space vectors which neither short circuit the voltage source nor open circuit the current source. These conditions for the input and output side bridges can be described as:

- **Conditions for input side bridge(s):** For a generic input side bridge, only two diagonal switches can be in the ON state at any given time. This constraint can be represented by equations (3.61)-(3.62). Note that the condition in (3.61) means only active states will be allowed, however zero states can also be considered. An example of a zero state is when all the switches in the input side bridge are OFF resulting in a zero voltage at the MF transformer. The zero states in the input side bridge have been avoided to maintain voltage balance across transformer in a simple manner, by generating a 50% duty cycle waveform using the active states.

$$\begin{gathered} [S_{WKij} = S_{XKij} = 1, S_{YKij} = S_{ZKij} = 0] \\ OR \\ [S_{WKij} = S_{XKij} = 0, S_{YKij} = S_{ZKij} = 1] \end{gathered} \tag{3.61}$$

$$S_{WKij} + S_{XKij} + S_{YKij} + S_{ZKij} = 2 \tag{3.62}$$

- **Conditions for output side bridge(s):** For a generic output side bridge, two diagonal, top or bottom switches can be in the ON state. These constraints can be represented by (3.63). Note that the later constraints that either two top or two bottom switches can be ON, ensuring that the output side is never open circuit in case of a zero state.

$$\begin{aligned}
&[S_{WKoj} = S_{XKoj} = 1, S_{YKoj} = S_{ZKoj} = 0]OR \\
&[S_{WKoj} = S_{XKoj} = 0, S_{YKoj} = S_{ZKoj} = 1] \\
&\qquad OR \\
&[S_{WKoj} = S_{YKoj} = 0, S_{XKoj} = S_{ZKoj} = 1]OR \\
&[S_{WKoj} = S_{YKoj} = 1, S_{XKoj} = S_{ZKoj} = 0]
\end{aligned} \tag{3.63}$$

$$S_{WKoj} + S_{XKoj} + S_{YKoj} + S_{ZKoj} = 2 \tag{3.64}$$

Now that the constraints have been defined in equations (3.61)-(3.64), the three-phase output voltages, V_{jo} for $j = a, b, c$, can be represented as a vector in space $\bar{\mathbf{v}}_\mathbf{o}$ using equation (3.65), as shown in Figure 3.23.

$$\bar{\mathbf{v}}_\mathbf{o} = \frac{2}{3}\left(V_{ao} + V_{bo}e^{j\frac{2\pi}{3}} + V_{co}e^{-j\frac{2\pi}{3}}\right) \tag{3.65}$$

Substitution of the output voltage V_{jo} from (3.53) in (3.65) will result in output voltage vector $\bar{\mathbf{v}}_\mathbf{o}$ for the MIMC, as shown in (3.66). In an analogous manner, input current vector $\bar{\mathbf{I}}_\mathbf{i}$ (3.67) is expressed using (3.68).

$$\begin{aligned}
\bar{\mathbf{v}}_\mathbf{o} = \frac{2}{3}[&(S_{WAoa}S_{XAoa} - S_{YAoa}S_{ZAoa})(S_{WAia}S_{XAia} - S_{YAia}S_{ZAia})V_{Ai}+ \\
&(S_{WBoa}S_{XBoa} - S_{YBoa}S_{ZBoa})(S_{WBia}S_{XBia} - S_{YBia}S_{ZBia})V_{Bi}+ \\
&(S_{WCoa}S_{XCoa} - S_{YCoa}S_{ZCoa})(S_{WCia}S_{XCia} - S_{YCia}S_{ZCia})V_{Ci}+ \\
e^{j\frac{2\pi}{3}}&((S_{WAob}S_{XAob} - S_{YAob}S_{ZAob})(S_{WAib}S_{XAib} - S_{YAib}S_{ZAib})V_{Ai}+ \\
&(S_{WBob}S_{XBob} - S_{YBob}S_{ZBob})(S_{WBib}S_{XBib} - S_{YBib}S_{ZBib})V_{Bi}+ \\
&(S_{WCob}S_{XCob} - S_{YCob}S_{ZCob})(S_{WCib}S_{XCib} - S_{YCib}S_{ZCib})V_{Ci})+ \\
e^{-j\frac{2\pi}{3}}&((S_{WAoc}S_{XAoc} - S_{YAoc}S_{ZAoc})(S_{WAic}S_{XAic} - S_{YAic}S_{ZAic})V_{Ai}+ \\
&(S_{WBoc}S_{XBoc} - S_{YBoc}S_{ZBoc})(S_{WBic}S_{XBic} - S_{YBic}S_{ZBic})V_{Bi}+ \\
&(S_{WCoc}S_{XCoc} - S_{YCoc}S_{ZCoc})(S_{WCic}S_{XCic} - S_{YCic}S_{ZCic})V_{Ci})]
\end{aligned} \tag{3.66}$$

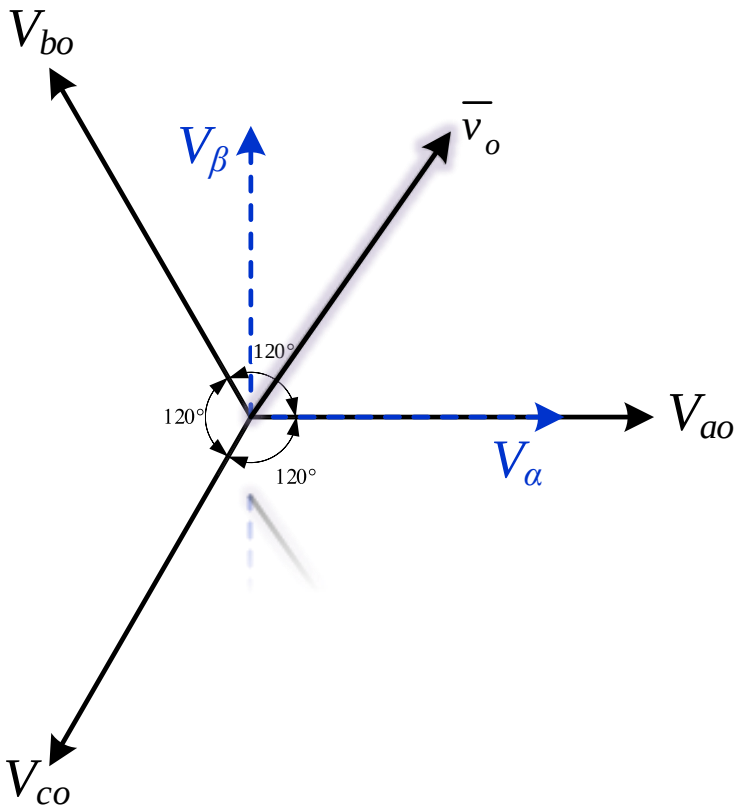


Figure 3.23: Space vector representation of the output phase voltages

$$\bar{\mathbf{I}}_\mathbf{i} = \frac{2}{3}\left(I_{Ai} + I_{Bi}e^{j\frac{2\pi}{3}} + I_{Ci}e^{-j\frac{2\pi}{3}}\right) \tag{3.67}$$

$$\begin{aligned}
\bar{\mathbf{I}}_\mathbf{i} = \frac{2}{3}[&(S_{WAia}S_{XAia} - S_{YAia}S_{ZAia})(S_{WAoa}S_{XAoa} - S_{YAoa}S_{ZAoa})I_{ao}+\\
&(S_{WAib}S_{XAib} - S_{YAib}S_{ZAib})(S_{WAob}S_{XAob} - S_{YAob}S_{ZAob})I_{bo}+\\
&(S_{WAic}S_{XAic} - S_{YAic}S_{ZAic})(S_{WAoc}S_{XAoc} - S_{YAoc}S_{ZAoc})I_{co}+\\
e^{j\frac{2\pi}{3}}&((S_{WBia}S_{XBia} - S_{YBia}S_{ZBia})(S_{WBoa}S_{XBoa} - S_{YBoa}S_{ZBoa})I_{ao}+\\
&(S_{WBib}S_{XBib} - S_{YBib}S_{ZBib})(S_{WBob}S_{XBob} - S_{YBob}S_{ZBob})I_{bo}+\\
&(S_{WBic}S_{XBic} - S_{YBic}S_{ZBic})(S_{WBoc}S_{XBoc} - S_{YBoc}S_{ZBoc})I_{co})+\\
e^{-j\frac{2\pi}{3}}&((S_{WCia}S_{XCia} - S_{YCia}S_{ZCia})(S_{WCoa}S_{XCoa} - S_{YCoa}S_{ZCoa})I_{ao}+\\
&(S_{WCib}S_{XCib} - S_{YCib}S_{ZCib})(S_{WCob}S_{XCob} - S_{YCob}S_{ZCob})I_{bo}+\\
&(S_{WCic}S_{XCic} - S_{YCic}S_{ZCic})(S_{WCoc}S_{XCoc} - S_{YCoc}S_{ZCoc})I_{co})]
\end{aligned} \tag{3.68}$$

The output voltage $\bar{\mathbf{v}}_{\mathbf{o}}$, shown in (3.66), was computed using a MATLAB program for all the switching combinations of 2^{72}. A total of 17576 possible voltage which respect the stated constrains of voltage and current source were found. Out of the total 17576 voltage vectors, 3649 are zero vectors, 2137 are fixed-direction active voltage vectors and the remainder are rotating vectors. An example of a fixed direction voltage vector is shown in (3.69) and of a rotating vector in (3.70). Note that the direction of the vector in (3.69) is not dependent on V_{Ai} or V_{Bi} and is fixed to 120°. On the other hand, the direction of the vector in (3.70) is dependant on V_{Ai} and V_{Bi} and is variable. The rotating vectors require high processing power [77] as the changing direction requires the DSP to compute the rotating vectors every switching period and are therefore not used commonly [78].

$$\bar{\mathbf{v}}_{\mathbf{o}} = \frac{2}{3}\left(V_{Ai} - V_{Bi}\right) e^{j\frac{2\pi}{3}} \tag{3.69}$$

$$\bar{\mathbf{v}}_{\mathbf{o_rotating}} = \frac{2}{3}\left(V_{Ai} - V_{Bi} e^{j\frac{-2\pi}{3}}\right) \tag{3.70}$$

A compass plot of 2137 fixed-direction voltage vectors is shown in Figure 3.24. From Figure 3.24, it can be seen that the there are two hexagons. The inner hexagon, highlighted in blue, is same as in a Direct Matrix Converter [76]. This because the fundamental concept of the MIMC is devised from the Direct Matrix Converter.

The outer hexagon, shown in Figure 3.24 have vectors with magnitude $\frac{4}{3}$ which is twice than the vectors in the inner hexagon. In scalar terms, the outer hexagon represents the voltage vectors for the Double Venturini Modulation method whereas the inner hexagon represents the voltage vectors for the Venturini Modulation method.

After the identification of the fixed direction output voltage vectors, the next step is to compute the input current vectors corresponding to the identified output voltage vectors. Using (3.68), a total of 2137 corresponding input current vectors can be found. Out of these 2137 input current vectors, only 502 active current vectors have a fixed direction. For example, the fixed direction output voltage vectors shown in red in Figure 3.24 have rotating input current vectors. This means that there are a total of 502 available active vectors in the MIMC. Out of the available 502 active vectors, 108 vectors lie in the outer hexagon, the rest lie in the inner hexagon.

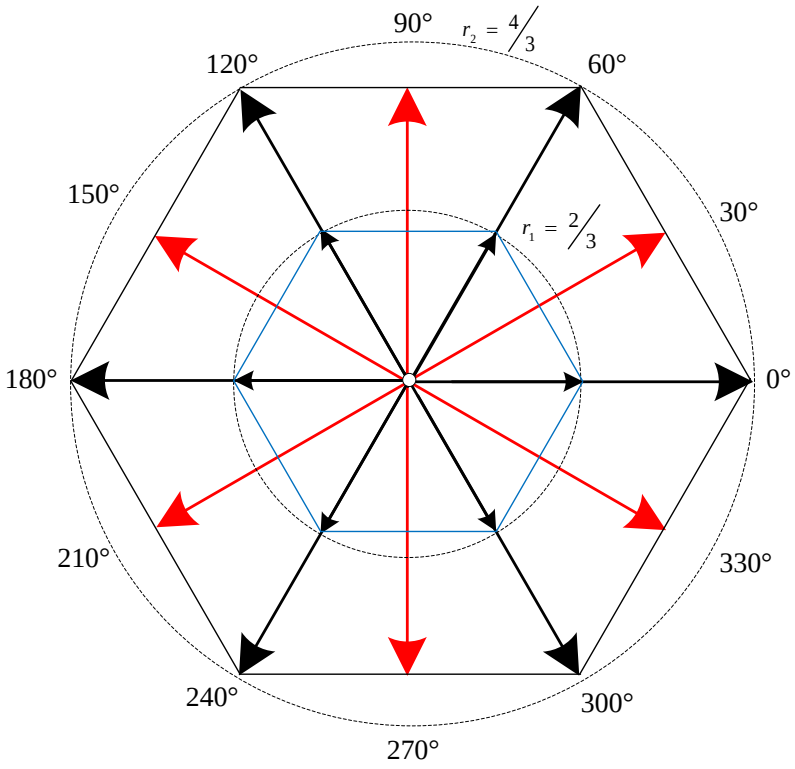


Figure 3.24: Fixed direction output voltage vectors

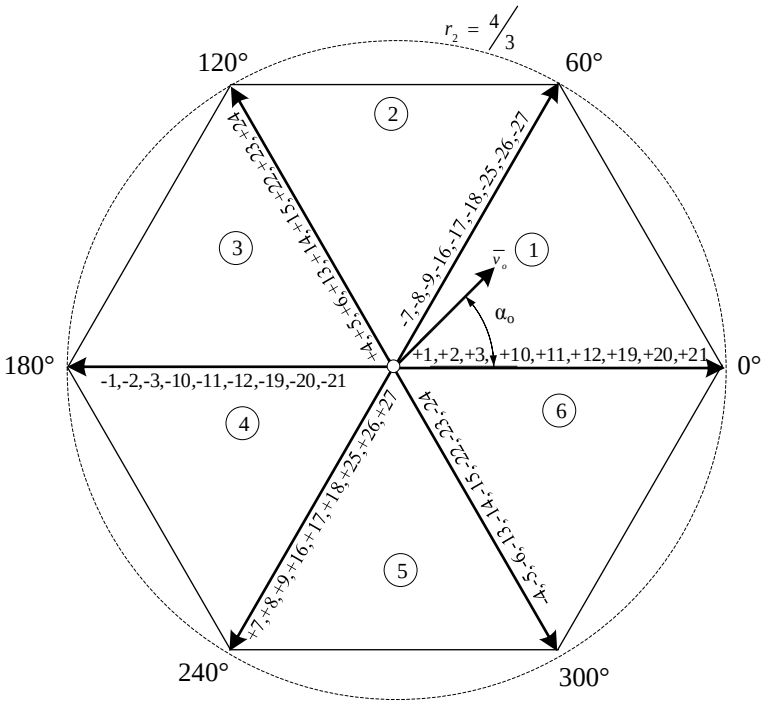
The vectors in the outer hexagon are preferred because a higher magnitude reference vector can be tracked, maximising the voltage transfer ratio of the MIMC. Therefore, only the vectors in the outer hexagon were considered in this study. 54 out of 108 vectors apply a voltage at the transformer equal to the input voltage, $V_{TKj} = V_{Ki}$; the other 54 reverse the voltage at the transformer, $V_{TKj} = -V_{Ki}$. Thus these vectors exist in complementary pairs in terms of voltage accross transformer but are same in terms of input current and output voltage vectors. These complementary vectors will be used to apply a balanced 50% duty voltage at the transformers, as discussed later in this section. Therefore, there are effectively 54 output voltage and input current available vectors, as shown in Figure 3.25. The 54 active vectors are represented using numbers ranging from -27 to $+27$, the sectors are numbered from 1 to 6, the angle of the output voltage vector $\bar{\mathbf{v}}_\mathbf{o}$ is α_o whereas that of the input current vector $\bar{\mathbf{I}}_\mathbf{i}$ is β_i.

The 54 active vectors can be sorted as shown in Table 3.2. By sorting these vectors, it can be seen from Table 3.2 that vectors 1, 10 and 19 generate the same output voltage

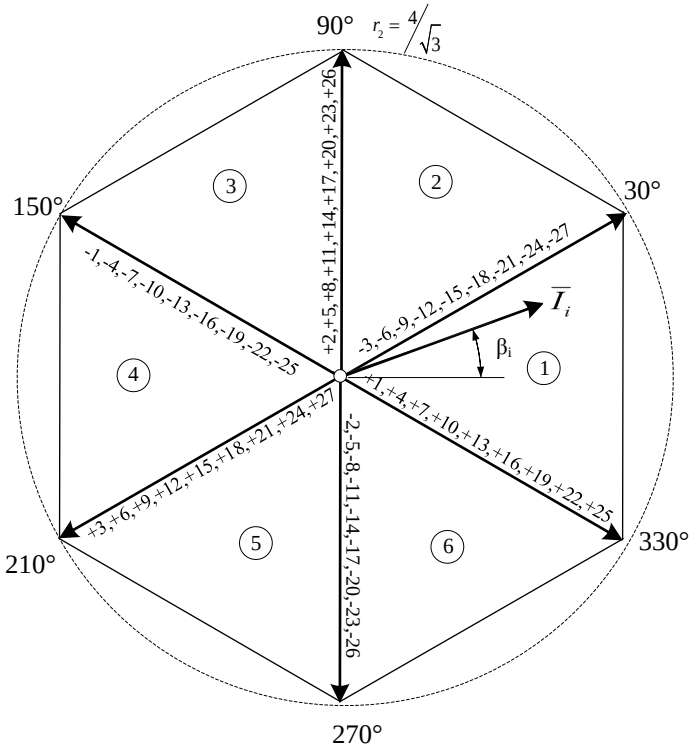
and input current, so in this case vector 10 and vector 19 are redundant. Similarly, it can also be seen that for each vector there are two redundant vectors, therefore there are 18 different active vectors. The selection between 18 different active vectors can be made based on the vector configuration, as presented in the SVM of the Matrix Converter [76], however the choice between the redundant vectors is usually made to achieve a certain target [79] for example reducing common-mode voltage [80, 81] or the number of commutations [82] and this has been discussed later in this section.
The vector configurations can be found by determining the common vectors available in each sector. To do this, it is assumed that both the voltage vector $\bar{\mathbf{v}}_\mathbf{o}$ and the current vector $\bar{\mathbf{I}}_\mathbf{i}$ are in the first sectors, as shown in Figure 3.25(a) and Figure 3.25(b), respectively. Then the vectors available in the first sector of voltage hexagon to generate $\bar{\mathbf{v}}_\mathbf{o}$ are +1,+2,+3,+10,+11,+12,+19,+20,+21 and -7,-8,-9,-16,-17,-18,-25,-26,-27 whereas those in the first sector of the current hexagon to generate $\bar{\mathbf{I}}_\mathbf{i}$ are +1,+4,+7,+10,+13,+16,+19,+22,+25 and -3,-6,-9,-12,-15,-18,-21,-24,-27. The vectors common in first sectors of voltage and current hexagons are +1,+10,+19,-3,-12,-21,+9,+18,+27,-7,-16,-25. The redundant vectors can then be grouped as:

- I=[+9, +18, +27]
- II=[-7, -16, -25]
- III=[-3, -12, -21]
- IV=[+1, +10, +19]

In this particular case, the first vector will be one of +9,+18,+27, second will be one of -7,-16,-25, third will be one of -3,-12,-21 and fourth will be one of +1,+10,+19. In a similar manner, the common vectors for all the sector combinations can be found and the vector configuration using 4 vectors (I,II,III and IV) per period [76] can be summarised, as shown in Table 3.3. Note that only positive vectors are shown in Table 3.3, the information about the sign will be discussed later in this section.



(a) Output voltage vectors with a maximum magnitude of $\frac{4}{3}$



(b) Input current vectors with a maximum magnitude of $\frac{4}{\sqrt{3}}$

Figure 3.25: Space vectors diagram showing the 54 fixed direction voltage and current vectors

Table 3.2: Definition of the vectors for SVM

Index	Vector Number	v_o	α_o	I_i	β_o
1	+1, +10, +19	$\frac{4}{3}(V_{Ai} - V_{Bi})$	0	$\frac{4}{\sqrt{3}}I_{ao}$	$-\frac{\pi}{6}$
2	-1, -10, -19	$\frac{4}{3}(V_{Ai} - V_{Bi})$	π	$\frac{4}{\sqrt{3}}I_{ao}$	$-\frac{7\pi}{6}$
3	+2, +11, +20	$\frac{4}{3}(V_{Bi} - V_{Ci})$	0	$\frac{4}{\sqrt{3}}I_{ao}$	$\frac{\pi}{2}$
4	-2, -11, -20	$\frac{4}{3}(V_{Bi} - V_{Ci})$	π	$\frac{4}{\sqrt{3}}I_{ao}$	$-\frac{\pi}{2}$
5	+3, +12, +21	$\frac{4}{3}(V_{Ci} - V_{Ai})$	0	$\frac{4}{\sqrt{3}}I_{ao}$	$\frac{7\pi}{6}$
6	-3, -12, -21	$\frac{4}{3}(V_{Ci} - V_{Ai})$	π	$\frac{4}{\sqrt{3}}I_{ao}$	$\frac{\pi}{6}$
7	+4, +13, +22	$\frac{4}{3}(V_{Ai} - V_{Bi})$	$\frac{2\pi}{3}$	$\frac{4}{\sqrt{3}}I_{bo}$	$-\frac{\pi}{6}$
8	-4, -13, -22	$\frac{4}{3}(V_{Ai} - V_{Bi})$	$-\frac{\pi}{3}$	$\frac{4}{\sqrt{3}}I_{bo}$	$-\frac{7\pi}{6}$
9	+5, +14, +23	$\frac{4}{3}(V_{Bi} - V_{Ci})$	$\frac{2\pi}{3}$	$\frac{4}{\sqrt{3}}I_{bo}$	$\frac{\pi}{2}$
10	-5, -14, -23	$\frac{4}{3}(V_{Bi} - V_{Ci})$	$-\frac{\pi}{3}$	$\frac{4}{\sqrt{3}}I_{bo}$	$-\frac{\pi}{2}$
11	+6, +15, +24	$\frac{4}{3}(V_{Ci} - V_{Ai})$	$\frac{2\pi}{3}$	$\frac{4}{\sqrt{3}}I_{bo}$	$\frac{7\pi}{6}$
12	-6, -15, -24	$\frac{4}{3}(V_{Ci} - V_{Ai})$	$-\frac{\pi}{3}$	$\frac{4}{\sqrt{3}}I_{bo}$	$\frac{\pi}{6}$
14	+7, +16, +25	$\frac{4}{3}(V_{Ai} - V_{Bi})$	$-\frac{2\pi}{3}$	$\frac{4}{\sqrt{3}}I_{co}$	$-\frac{\pi}{6}$
15	-7, -16, -25	$\frac{4}{3}(V_{Ai} - V_{Bi})$	$\frac{\pi}{3}$	$\frac{4}{\sqrt{3}}I_{co}$	$-\frac{7\pi}{6}$
16	+8, +17, +26	$\frac{4}{3}(V_{Bi} - V_{Ci})$	$-\frac{2\pi}{3}$	$\frac{4}{\sqrt{3}}I_{co}$	$\frac{\pi}{2}$
17	-8, -17, -26	$\frac{4}{3}(V_{Bi} - V_{Ci})$	$\frac{\pi}{3}$	$\frac{4}{\sqrt{3}}I_{co}$	$-\frac{\pi}{2}$
18	+9, +18, +27	$\frac{4}{3}(V_{Ci} - V_{Ai})$	$-\frac{2\pi}{3}$	$\frac{4}{\sqrt{3}}I_{co}$	$\frac{7\pi}{6}$
19	Z	0	0	0	0

Table 3.3: Vector configurations for the combinations of the output voltage and input current sectors

Sector of the input current vector	**Sector of output voltage vector**											
	1 or 4				**2 or 5**				**3 or 6**			
1 or 4	+9, +18, +27	+7 ,+16 ,+25	+3, +12, +21	+1 ,+10, +19	+6 ,+15, +24	+4, +13, +22	+9, +18, +27	+7, +16, +25	+3, +12, +21	+1, +10, +19	+6 ,+15, +24	+4, +13, +22
2 or 5	+8, +17, +26	+9, +18, +27	+2, +11, +20	+3, +12, +21	+5 ,+14, +23	+6 ,+15, +24	+8, +17, +26	+9, +18, +27	+2, +11, +20	+3, +12, +21	+5 ,+14, +23	+6 ,+15, +24
3 or 6	+7, +16, +25	+8, +17, +26	+1 ,+10, +19	+2, +11, +20	+4, +13, +22	+5 ,+14, +23	+7, +16, +25	+8, +17, +26	+1 ,+10, +19	+2, +11, +20	+4, +13, +22	+5 ,+14, +23
	I	II	III	IV	I	II	III	IV	I	II	III	IV

After the identification of the four different vectors to be applied in each switching period, the next step is to determine the times for which each of these vectors will be applied. To compute the time or duty cycle for each of the four vectors, assume that both the output voltage vector $\bar{\mathbf{v}}_\mathbf{o}$ and the input current vector $\bar{\mathbf{I}}_\mathbf{i}$ are in the first sector, as shown in Figure 3.26 and Figure 3.27, respectively.

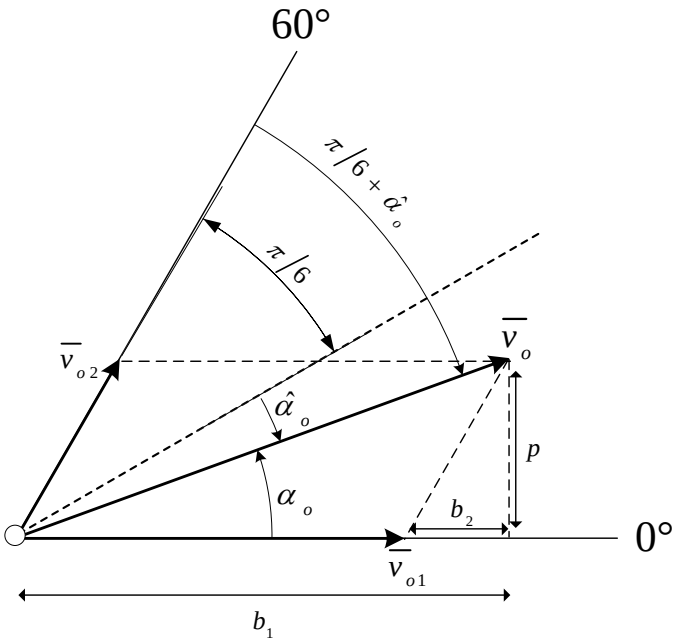


Figure 3.26: Output voltage vector $\bar{\mathbf{v}}_\mathbf{o}$ in Sector 1

In Figure 3.26, the angle from the sector's bisecting line to the voltage vector $\bar{\mathbf{v}}_\mathbf{o}$ is $\hat{\alpha}_o$ which can be expressed using (3.71) for the first sector. The output voltage vector $\bar{\mathbf{v}}_\mathbf{o}$ must be decomposed into two components $\bar{\mathbf{v}}_\mathbf{o1}$ and $\bar{\mathbf{v}}_\mathbf{o2}$. The magnitude of vector $\bar{\mathbf{v}}_\mathbf{o1}$ can then be evaluated by using (3.72).

$$\hat{\alpha}_o = \alpha_o - \pi/6 \quad Where \quad -\frac{\pi}{6} < \hat{\alpha}_o < \frac{\pi}{6} \tag{3.71}$$

$$|\bar{v}_{o1}| = b_1 - b_2 \tag{3.72}$$

$$b_1 = |\bar{v}_o| \cos\left(\hat{\alpha}_o + \frac{\pi}{6}\right) \tag{3.73}$$

$$b_2 = \frac{|\bar{v}_o|}{\sqrt{3}} \sin\left(\hat{\alpha}_o + \frac{\pi}{6}\right) \tag{3.74}$$

Substituting b_1 and b_2 from (3.73) and (3.74) into (3.72) will result in (3.75) which can be simplified to the form shown in (3.76). Similarly, the magnitude of vector $\bar{\mathbf{v}}_{\mathbf{o2}}$ can be found as shown in (3.79) using equations (3.78), (3.77) and (3.74).

$$|\bar{v}_{o1}| = |\bar{v}_o| \left[\cos\left(\hat{\alpha}_o + \frac{\pi}{6}\right) - \frac{1}{\sqrt{3}} \sin\left(\hat{\alpha}_o + \frac{\pi}{6}\right) \right] \tag{3.75}$$

$$|\bar{v}_{o1}| = \frac{2}{\sqrt{3}} |\bar{v}_o| \cos\left(\hat{\alpha}_o + \frac{\pi}{3}\right) \tag{3.76}$$

$$p = |\bar{v}_o| \sin\left(\hat{\alpha}_o + \frac{\pi}{6}\right) \tag{3.77}$$

$$|\bar{v}_{o2}| = \sqrt{{b_2}^2 + p^2} \tag{3.78}$$

$$|\bar{v}_{o2}| = \frac{2}{\sqrt{3}} |\bar{v}_o| \cos\left(\hat{\alpha}_o - \frac{\pi}{3}\right) \tag{3.79}$$

Note that equations (3.76) and (3.79) show the magnitudes of $\bar{\mathbf{v}}_{\mathbf{o1}}$ and $\bar{\mathbf{v}}_{\mathbf{o2}}$ respectively and the direction of these vectors depends on the sector. The generic expressions for these vectors, for all the sectors, are shown in (3.80) and (3.81) in which K_v denotes the sector number of voltage vector.

$$\bar{\mathbf{v}}_{\mathbf{o1}} = \frac{2}{\sqrt{3}} |\bar{v}_o| \cos\left(\hat{\alpha}_o + \frac{\pi}{3}\right) e^{j\left[\frac{\pi}{3}(K_v - 1)\right]} \tag{3.80}$$

$$\bar{\mathbf{v}}_{\mathbf{o2}} = \frac{2}{\sqrt{3}} |\bar{v}_o| \cos\left(\hat{\alpha}_o - \frac{\pi}{3}\right) e^{j\left[\frac{\pi}{3}(K_v - 1) + \frac{\pi}{3}\right]} \tag{3.81}$$

The vector $\bar{\mathbf{v}}_{\mathbf{o1}}$ can be generated using two vectors which are in the direction $e^{j\left[\frac{\pi}{3}(K_v-1)\right]}$ whereas the vector $\bar{\mathbf{v}}_{\mathbf{o2}}$ can be generated by two vectors in the direction $e^{j\left[\frac{\pi}{3}(K_v-1)+\frac{\pi}{3}\right]}$. The expressions for $\bar{\mathbf{v}}_{\mathbf{o1}}$ and $\bar{\mathbf{v}}_{\mathbf{o2}}$ can then be re-written as shown in equations (3.82) and (3.83). Note that the Roman numerals I,II,III and IV used in (3.82) and (3.83) denote the four vectors for the configurations shown in Table 3.3.

The two equations for voltage vectors, shown in (3.82) and (3.83), have four duty cycle variables δ^I, δ^{II}, δ^{III} and δ^{IV} but to compute the four duty cycles at least four equations are required. The two additional equations can be obtained from the input current vector.

$$\bar{\mathbf{v}}_{\mathbf{o1}} = \frac{2}{\sqrt{3}} |\bar{v}_o| \cos\left(\hat{\alpha}_o + \frac{\pi}{3}\right) e^{j\left[\frac{\pi}{3}(K_v - 1)\right]} = \bar{\mathbf{v}}_{\mathbf{o}}^{\mathbf{III}} \delta^{III} + \bar{\mathbf{v}}_{\mathbf{o}}^{\mathbf{IV}} \delta^{IV} \tag{3.82}$$

$$\bar{\mathbf{v}}_{\mathbf{o2}} = \frac{2}{\sqrt{3}} |\bar{v}_o| \cos\left(\hat{\alpha}_o - \frac{\pi}{3}\right) e^{j\left[\frac{\pi}{3}(K_v-1)+\frac{\pi}{3}\right]} = \bar{\mathbf{v}}_{\mathbf{o}}^{\mathbf{I}}\delta^I + \bar{\mathbf{v}}_{\mathbf{o}}^{\mathbf{II}}\delta^{II} \tag{3.83}$$

In order to obtain these equations, assume that the current vector $\bar{\mathbf{I}}_{\mathbf{i}}$ is in the first sector, as show in Figure 3.27. In Figure 3.27 the angle from the sector's bisecting line to the current vector $\bar{\mathbf{I}}_{\mathbf{i}}$ is $\hat{\beta}_i$ which, for the first sector, can be expressed using equation (3.84). Note that $\bar{\mathbf{v}}_{\mathbf{i}}$ is the input voltage vector and φ_i is the angle of the input power factor. Now the two equations can be obtained by imposing a vector in the direction $je^{j\hat{\beta}_i}$ which is perpendicular to the current vector $\bar{\mathbf{I}}_{\mathbf{i}}$. A dot product of two perpendicular vectors is zero therefore, therefore leading to equations (3.85) and (3.86). In (3.85) and (3.86), K_i denotes the sector number in which the input current vector $\bar{\mathbf{I}}_{\mathbf{i}}$ lies.

$$\hat{\beta}_i = \beta_i \qquad Where \qquad -\frac{\pi}{6} < \hat{\beta}_i < \frac{\pi}{6} \tag{3.84}$$

$$\left(\mathbf{I}^{\mathbf{I}}{}_{\mathbf{i}}\delta^I + \mathbf{I}^{\mathbf{II}}{}_{\mathbf{i}}\delta^{II}\right) \cdot je^{j\hat{\beta}_i} e^{j\left[\frac{\pi}{3}(K_i-1)\right]} = 0 \tag{3.85}$$

$$\left(\mathbf{I}^{\mathbf{III}}{}_{\mathbf{i}}\delta^{III} + \mathbf{I}^{\mathbf{IV}}{}_{\mathbf{i}}\delta^{IV}\right) \cdot je^{j\hat{\beta}_i} e^{j\left[\frac{\pi}{3}(K_i-1)\right]} = 0 \tag{3.86}$$

Using Table 3.3 and Table 3.2, the values of the voltage and current vectors can be expressed using equations (3.85)-(3.94). For the input voltages V_{Ki} of type (3.95), the vectors $\bar{\mathbf{v}}_{\mathbf{o1}}$ and $\bar{\mathbf{v}}_{\mathbf{o2}}$ can be simplified as shown in (3.96) and (3.97), respectively. Substitution of these vectors from (3.96) and (3.97) into (3.83) will result in (3.98) which can be simplified to the form shown in equation (3.101). Note that q is the voltage transfer ratio.

$$\bar{v}_o^I = \frac{4}{3}\left(V_{Ci} - V_{Ai}\right) e^{-j\frac{2\pi}{3}} \tag{3.87}$$

$$\bar{I}_i^I = \frac{4}{\sqrt{3}} I_{co} e^{j\frac{7\pi}{6}} \tag{3.88}$$

$$\bar{v}_o^{II} = \frac{4}{3}\left(V_{Ai} - V_{Bi}\right) e^{-j\frac{2\pi}{3}} \tag{3.89}$$

$$\bar{I}_i^{II} = \frac{4}{\sqrt{3}} I_{co} e^{-j\frac{\pi}{6}} \tag{3.90}$$

$$\bar{v}_o^{III} = \frac{4}{3}\left(V_{Ci} - V_{Ai}\right) \tag{3.91}$$

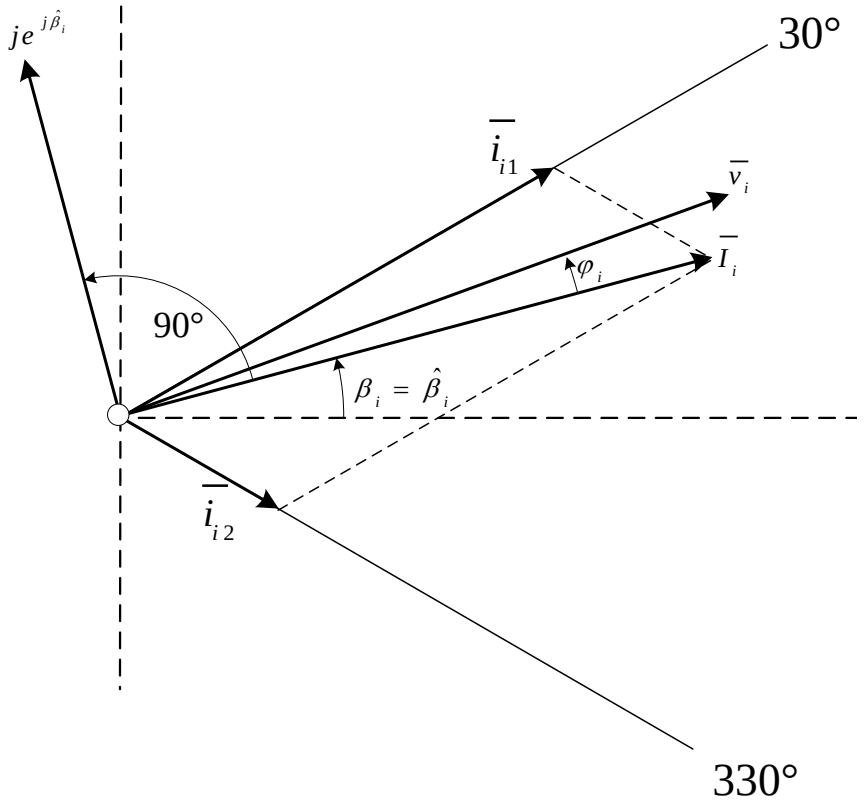


Figure 3.27: Input current vector $\bar{\mathbf{I}}_\mathbf{i}$ in Sector 1

$$\bar{I}_i^{III} = \frac{4}{\sqrt{3}} I_{ao} e^{j\frac{7\pi}{6}} \tag{3.92}$$

$$\bar{v}_o^{IV} = \frac{4}{3}\left(V_{Ai} - V_{Bi}\right) \tag{3.93}$$

$$\bar{I}_i^{IV} = \frac{4}{\sqrt{3}} I_{ao} e^{-j\frac{\pi}{6}} \tag{3.94}$$

$$V_{Ai} = V_m \cos\left(\alpha_i\right),\ V_{Bi} = V_m \cos\left(\alpha_i - \frac{2\pi}{3}\right),\ V_{Ci} = V_m \cos\left(\alpha_i + \frac{2\pi}{3}\right) \tag{3.95}$$

$$\begin{aligned} \bar{v}_o^I &= \frac{4}{3}\left(V_{Ci} - V_{Ai}\right) e^{-j\frac{2\pi}{3}} \\ &= \frac{4}{3} V_m \left[\cos\left(\alpha_i + \frac{2\pi}{3}\right) - \cos\left(\alpha_i\right)\right] e^{-j\frac{2\pi}{3}} \\ &= -\frac{4}{\sqrt{3}} V_m \sin\left(\alpha_i + \frac{\pi}{3}\right) e^{-j\frac{2\pi}{3}} \end{aligned} \tag{3.96}$$

$$\begin{aligned}\bar{v}_o^{II} &= \frac{4}{3}\left(V_{Ai} - V_{Bi}\right)e^{-j\frac{2\pi}{3}} \\ &= \frac{4}{3}V_m\left[\cos\left(\alpha_i\right) - \cos\left(\alpha_i - \frac{2\pi}{3}\right)\right]e^{-j\frac{2\pi}{3}} \\ &= -\frac{4}{\sqrt{3}}V_m \sin\left(\alpha_i - \frac{\pi}{3}\right)e^{-j\frac{2\pi}{3}}\end{aligned} \tag{3.97}$$

$$\bar{v}_o^I\delta^I + \bar{v}_o^{II}\delta^{II} = \frac{2}{\sqrt{3}}\left|\bar{v}_o\right|\cos\left(\hat{\alpha}_o - \frac{\pi}{3}\right)e^{j\frac{\pi}{3}} \tag{3.98}$$

$$-\frac{4V_m}{\sqrt{3}}e^{-j\frac{2\pi}{3}}\left[\sin\left(\alpha_i + \frac{\pi}{3}\right)\delta^I + \sin\left(\alpha_i - \frac{\pi}{3}\right)\delta^{II}\right] = \frac{2}{\sqrt{3}}\left|\bar{v}_o\right|\cos\left(\hat{\alpha}_o - \frac{\pi}{3}\right)e^{j\frac{\pi}{3}} \tag{3.99}$$

$$\left[\sin\left(\alpha_i + \frac{\pi}{3}\right)\delta^I + \sin\left(\alpha_i - \frac{\pi}{3}\right)\delta^{II}\right] = -\frac{\left|\bar{v}_o\right|}{2V_m}\cos\left(\hat{\alpha}_o - \frac{\pi}{3}\right)e^{j\pi} \tag{3.100}$$

$$\sin\left(\alpha_i + \frac{\pi}{3}\right)\delta^I + \sin\left(\alpha_i - \frac{\pi}{3}\right)\delta^{II} = \frac{q}{2}\cos\left(\hat{\alpha}_o - \frac{\pi}{3}\right) \tag{3.101}$$

In a similar manner, substituting current vectors $\bar{\mathbf{I}}_{\mathbf{i1}}$ and $\bar{\mathbf{I}}_{\mathbf{i2}}$ from (3.88) and (3.90) into (3.85) will result in equation (3.102) which can be simplified to the form shown in (3.108).

$$\left(\frac{4}{\sqrt{3}}I_{co}e^{j\frac{7\pi}{6}}\delta^I + \frac{4}{\sqrt{3}}I_{co}e^{-j\frac{\pi}{6}}\delta^{II}\right)\cdot je^{j\hat{\beta}_i} = 0 \tag{3.102}$$

$$\left(e^{j\frac{7\pi}{6}}\delta^I + e^{-j\frac{\pi}{6}}\delta^{II}\right)\cdot je^{j\hat{\beta}_i} = 0 \tag{3.103}$$

$$e^{j\frac{7\pi}{6}}\cdot je^{j\hat{\beta}_i}\delta^I + e^{-j\frac{\pi}{6}}\cdot je^{j\hat{\beta}_i}\delta^{II} = 0 \tag{3.104}$$

$$\cos\left(\frac{7\pi}{6} - \hat{\beta}_i - \frac{\pi}{2}\right)\delta^I + \cos\left(-\frac{\pi}{6} - \hat{\beta}_i - \frac{\pi}{2}\right)\delta^{II} = 0 \tag{3.105}$$

$$\cos\left(\hat{\beta}_i - \frac{2\pi}{3}\right)\delta^I + \cos\left(\hat{\beta}_i + \frac{2\pi}{3}\right)\delta^{II} = 0 \tag{3.106}$$

$$-\cos\left(\hat{\beta}_i + \frac{\pi}{3}\right)\delta^I - \cos\left(\hat{\beta}_i - \frac{\pi}{3}\right)\delta^{II} = 0 \tag{3.107}$$

$$\delta^{II} = \frac{-\cos\left(\hat{\beta}_i + \frac{\pi}{3}\right)\delta^I}{\cos\left(\hat{\beta}_i - \frac{\pi}{3}\right)} \tag{3.108}$$

Substituting this value of δ^{II} into (3.101) will result in (3.109) which can be simplified to the form shown in equation (3.112).

$$\sin\left(\alpha_i + \frac{\pi}{3}\right)\delta^I + \sin\left(\alpha_i - \frac{\pi}{3}\right)\left[\frac{-\cos\left(\hat{\beta}_i + \frac{\pi}{3}\right)\delta^I}{\cos\left(\hat{\beta}_i - \frac{\pi}{3}\right)}\right] = \frac{q}{2}\cos\left(\hat{\alpha}_o - \frac{\pi}{3}\right) \tag{3.109}$$

$$\frac{\sqrt{3}}{2}\delta^I\left[\cos\left(\alpha_i\right)\cos\left(\hat{\beta}_i\right)+\sin\left(\alpha_i\right)\sin\left(\hat{\beta}_i\right)\right]=\frac{q}{2}\cos\left(\hat{\alpha}_o-\frac{\pi}{3}\right)\cos\left(\hat{\beta}_i-\frac{\pi}{3}\right) \quad (3.110)$$

$$\delta^I\cos\left(\alpha_i-\hat{\beta}_i\right)=\frac{q}{\sqrt{3}}\cos\left(\hat{\alpha}_o-\frac{\pi}{3}\right)\cos\left(\hat{\beta}_i-\frac{\pi}{3}\right) \quad (3.111)$$

$$\delta^I=\frac{q}{\sqrt{3}}\frac{\cos\left(\hat{\alpha}_o-\frac{\pi}{3}\right)\cos\left(\hat{\beta}_i-\frac{\pi}{3}\right)}{\cos\left(\varphi_i\right)} \quad (3.112)$$

The value of δ^{II} can be obtained by substituting the value of δ^I from (3.112) into (3.108) which will result in equation (3.113). Note the duty cycle δ^{II} is negative because a positive sign is assumed in the analysis (See Table 3.3).

$$\delta^{II}=-\frac{q}{\sqrt{3}}\frac{\cos\left(\hat{\alpha}_o-\frac{\pi}{3}\right)\cos\left(\hat{\beta}_i+\frac{\pi}{3}\right)}{\cos\left(\varphi_i\right)} \quad (3.113)$$

In a similar manner, the duty cycles δ^{III} and δ^{IV} were also computed and the obtained generalised expressions of the duty cycles, for ${K_v}^{th}$ voltage and ${K_i}^{th}$ current sector, are shown in (3.114)-(3.117). From (3.114)-(3.117), it can be seen that the maximum voltage regulation ratio q that be achieved by the MIMC is $\sqrt{3}$, which is twice that of a Direct Matrix Converter [76].

$$\delta^I=(-1)^{K_v+K_i}\frac{q}{\sqrt{3}}\frac{\cos\left(\hat{\alpha}_o-\frac{\pi}{3}\right)\cos\left(\hat{\beta}_i-\frac{\pi}{3}\right)}{\cos\left(\varphi_i\right)} \quad (3.114)$$

$$\delta^{II}=(-1)^{K_v+K_i+1}\frac{q}{\sqrt{3}}\frac{\cos\left(\hat{\alpha}_o-\frac{\pi}{3}\right)\cos\left(\hat{\beta}_i+\frac{\pi}{3}\right)}{\cos\left(\varphi_i\right)} \quad (3.115)$$

$$\delta^{III}=(-1)^{K_v+K_i+1}\frac{q}{\sqrt{3}}\frac{\cos\left(\hat{\alpha}_o+\frac{\pi}{3}\right)\cos\left(\hat{\beta}_i-\frac{\pi}{3}\right)}{\cos\left(\varphi_i\right)} \quad (3.116)$$

$$\delta^{IV}=(-1)^{K_v+K_i}\frac{q}{\sqrt{3}}\frac{\cos\left(\hat{\alpha}_o+\frac{\pi}{3}\right)\cos\left(\hat{\beta}_i+\frac{\pi}{3}\right)}{\cos\left(\varphi_i\right)} \quad (3.117)$$

After the determination of the duty cycles, the next step is to define a switching pattern. The choice of the switching pattern is application specific and is usually done to achieve certain targets such as reduction in THD [79, 83] or common-mode voltages [80, 81] or number of commutations [84] . For the case of the MIMC, the priority is to reduce the number of commutations. This is because a multi-step commutation approach is required in the MIMC due to the absence of free-wheeling

path in the four-quadrant switches, therefore a significant amount of switching period would be lost with the increased number of commutations.

A double-sided switching pattern will cause higher number of commutations per switching period than single-sided pattern [76]. Therefore, a single-sided switching pattern was selected, as shown in Figure 3.28. Note that in Figure 3.28, the zero vectors are represented by Z.

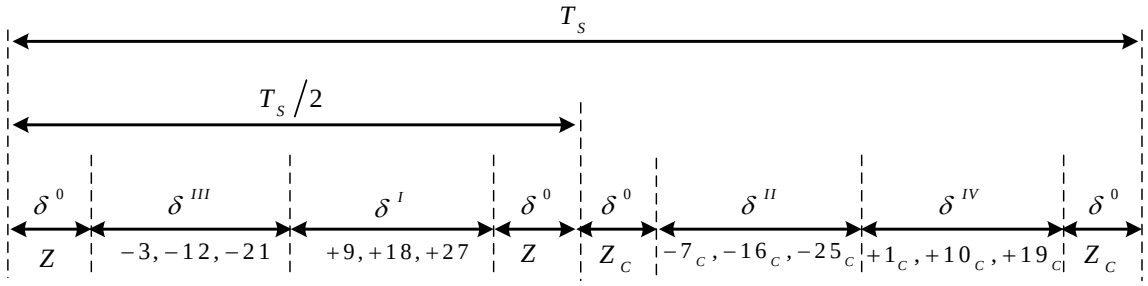


Figure 3.28: Single-sided pattern for a switching period T_S

Once the switching pattern is defined, the choice of zero vectors as well as the selection between the redundant vectors was made to achieve minimum number of commutations per-cell. For example, with the given switching pattern of [-3, -12, -21], [+9, +18, +27], [-7c, -16c,-25c], [+1c, +10c, +19c], the zero and active vectors which minimise the number of bridge commutations are Z^1,-3, +9, Z^2, ${Z_c}^3$, -7c, +1c, ${Z_c}^4$. Note that in Figure 3.28, c represents the complementary vectors which reverse the voltage at transformer. The switch-states of all the vectors including the zero vectors and the complimentary pairs are shown in Appendix B.

In order to validate the developed SVM method, ideal waveforms were obtained using the PLECS simulation toolbox and the results are shown in Figure 3.29 and Figure 3.30. Note the output cell voltage V_{Koa}, shown in Figure 3.30(a)-(c), is different to those obtained with the Venturini and the Double Venturini Modulation methods. The output cell voltages V_{Koa} obtained with SVM has a combination of both bi-polar and uni-polar waveforms. However with the Venturini Modulation method the waveform is uni-polar and with the Double Venturini Modulation method is bi-polar.

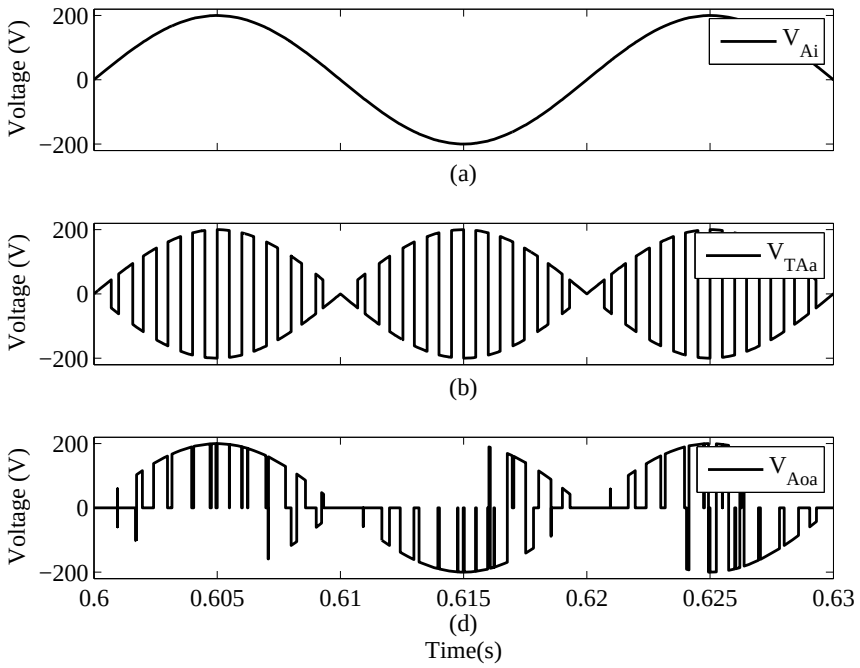


Figure 3.29: Theoretical voltage waveforms in the top-cell as a result of SVM method: (a) Input voltage V_{Ai}. (b) Transformer voltage V_{TAa}. (d) Output voltage V_{Aoa}.

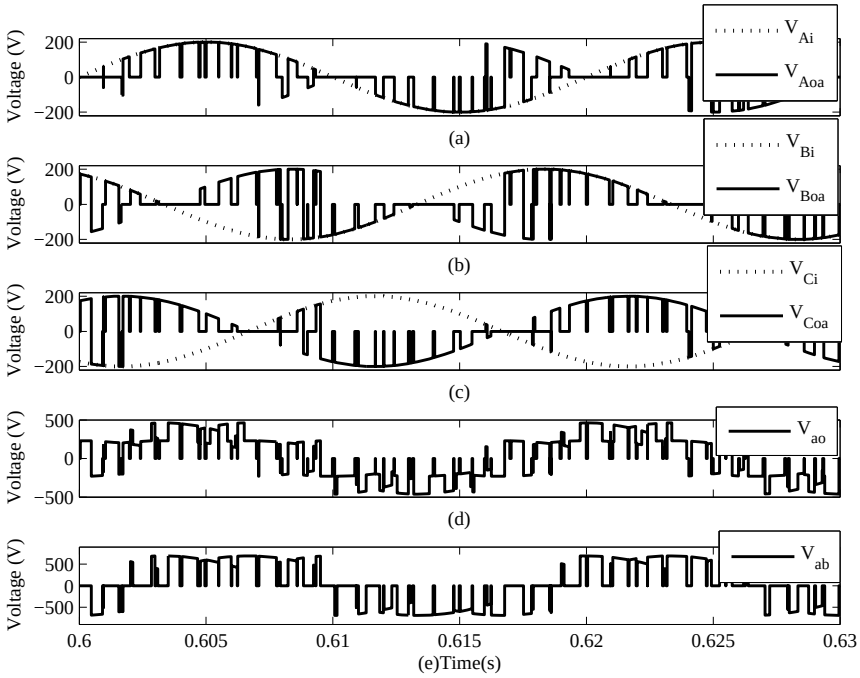


Figure 3.30: Theoretical voltage waveforms in the three-phase to three-phase MIMC as a result of the SVM method. (a)-(c) Input and output voltages of the cells V_{Ki} and V_{Koa}. (d) Phase output voltage V_{ao}. (e) Phase-phase output voltage V_{ab}

3.6 Comparison of the Modulation Methods

In this section, the SVM method is compared with the equivalent scalar modulation method, the Double Optimum Venturini Modulation (DOVM) method using a variety of parameters. A PLECS simulated harmonic spectrum of the phase output voltage V_{ao} is shown in Figure 3.31 which confirms the application of both scalar and vector modulation methods to the MIMC at 10kHz switching frequency. Note that same parameters are used for both methods to give a fair comparison, as given in Table 3.1. It can be seen from Figure 3.31 that a similar voltage regulation ratio is achieved with both methods, $\sqrt{3}$. Not only the magnitude of the fundamental component is the same but the harmonic spectrums are also similar.

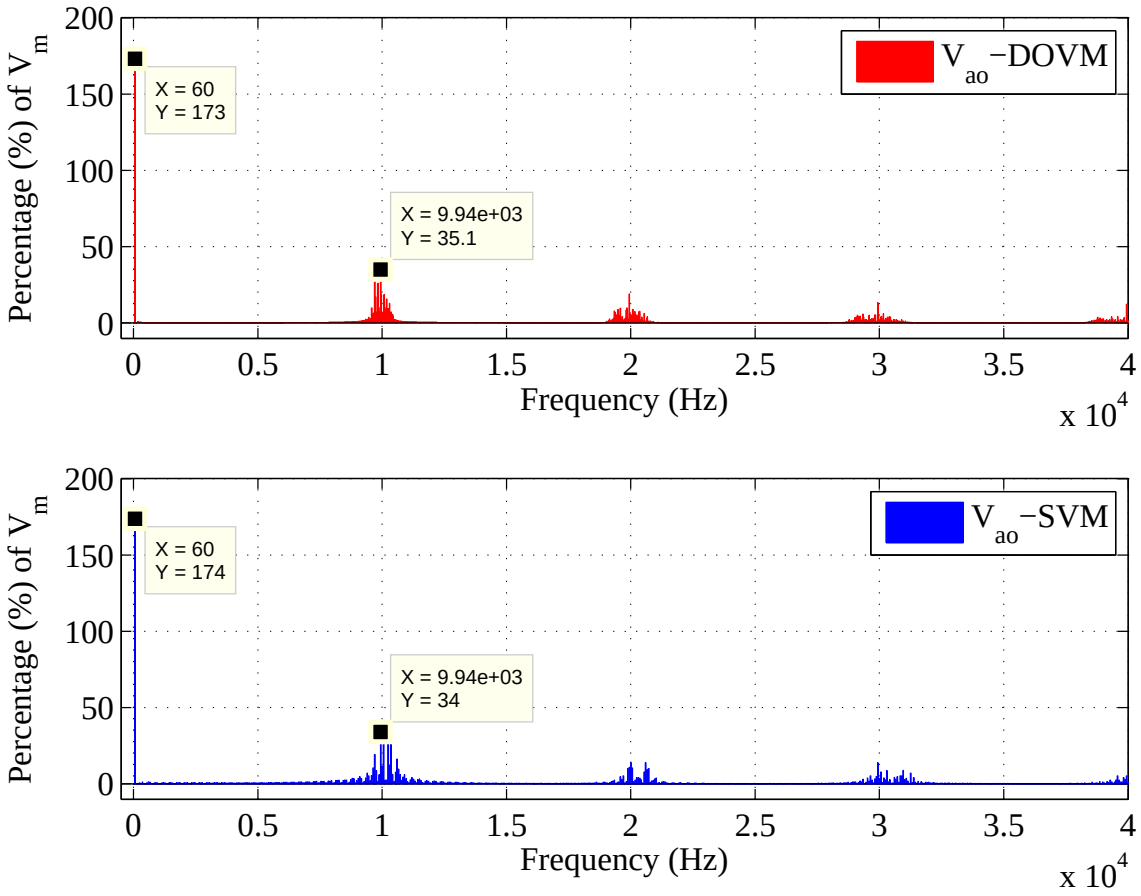


Figure 3.31: Harmonic spectrum of phase output voltage V_{ao} comparing vector modulation method i.e. Space Vector Modulation (SVM) with the equivalent scalar modulation method i.e. the Double Optimum Venturini Modulation (DOVM).

In order to see the number and sequence of commutations offered by the different methods, consider Figure 3.33, which shows the duty cycle arrangement in the Venturini Modulation. For example, the top-cell achieves the shown duty cycle arrangement D_{Aj}, D_{Bj}, D_{Cj} by implementing a state sequence which is $MS_{Kij}MS_{Koj} = [MS_1MS_1,\ MS_1MS_0,\ MS_2MS_0]$. Similarly, the two state sequences for the middle and bottom cells can be found in Figure 3.33. Note that these state sequences in the Venturini Modulation remain the same for every switching period. A total of four steady-states are required i.e. MS_1MS_1, MS_1MS_0, MS_2MS_2 and MS_2MS_0. The paths of movement between these steady-states, required to implement the Venturini Modulation method, are shown in Figure 3.32. A total of seven paths are required to implement the Venturini Modulation method. Note that the lower the number of required paths, the easier the practical implementation will become.

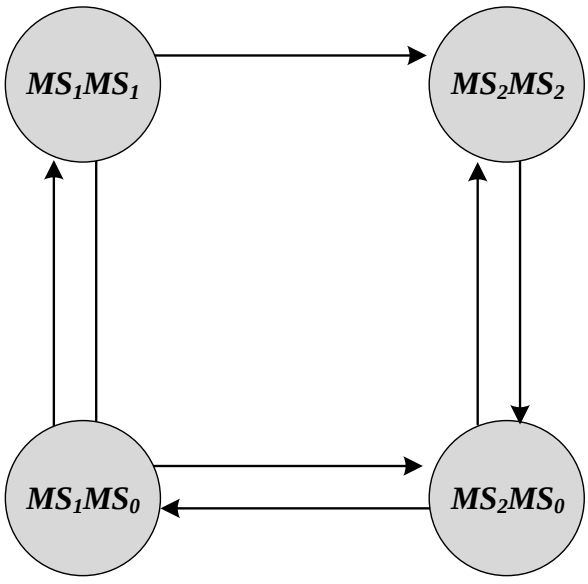


Figure 3.32: State transitions (per-cell) required for the implementation of the Venturini Modulation method

The commutation of a cell is marked by an arrow in Figure 3.33. The top and bottom cells will always have three commutations whereas the middle-cell will always have four commutations, therefore offering a total of ten cell-commutations in a three-phase to single-phase MIMC and thirty cell-commutations in a full MIMC.

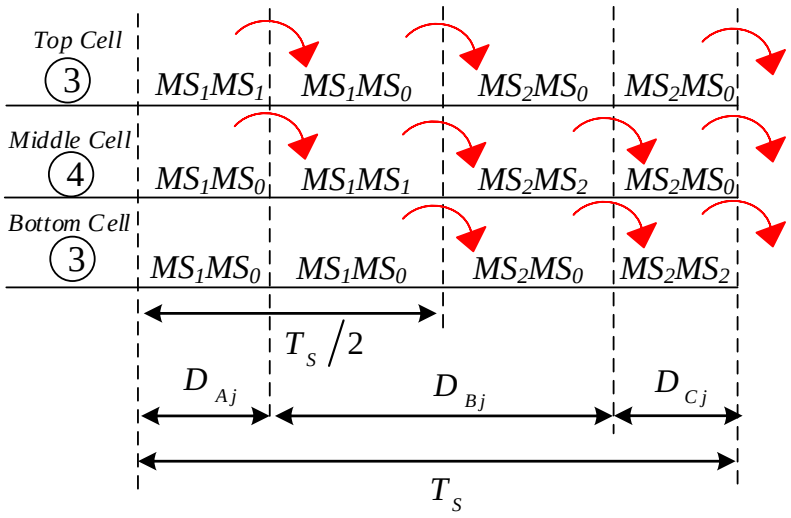


Figure 3.33: Commutation sequence in a switching period T_S with the Venturini Modulation method

The state change sequences required to implement the Double Venturini or Double Optimum Venturini Modulation are shown in Figure 3.35. Note that the shown state sequences do not change. The states required to implement the Double Venturini or Double Optimum Venturini Modulation method are MS_1MS_1, MS_1MS_2, MS_2MS_2, MS_2MS_1. The number of paths required for the implementation of the Double Venturini or Double Optimum Venturini Modulation method is nine which are shown in Figure 3.34 and found from Figure 3.35.

The state change sequences required to implement the SVM Modulation, when both the current and the voltage vectors are in sector 1, are shown in Figure 3.36. Note that state sequences for SVM is not fixed. These state sequences vary every switching period based on the sector of the input current output voltage. This can be seen by comparing the sequence for sector 2, shown in Figure 3.37, with the sequence for sector 1, shown in Figure 3.36. The minimum number of commutations that can be achieved with the SVM is same as offered by the scalar modulation methods however, a total of 6 steady-states, MS_1MS_1, MS_1MS_2, MS_2MS_2, MS_2MS_1,MS_1MS_0, MS_2MS_0, are required to implement the SVM. The total number of paths required to move between the 6 steady-states were found to be 30.

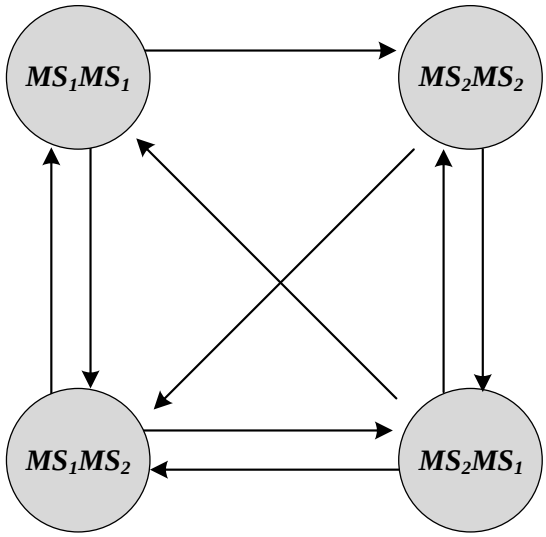


Figure 3.34: State transitions (per-cell) required for the implementation of the Double Venturini Modulation or Double Optimum Venturini Modulation method

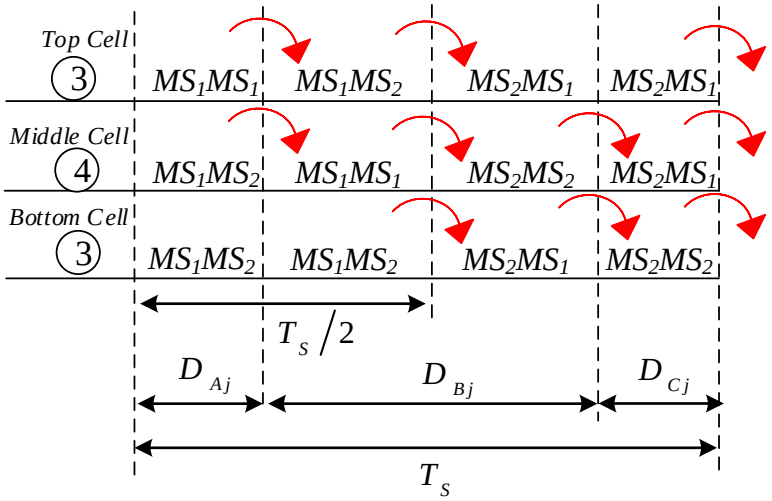


Figure 3.35: Commutation sequence in a switching period T_S with the Double Venturini or Double Optimum Venturini Modulation method

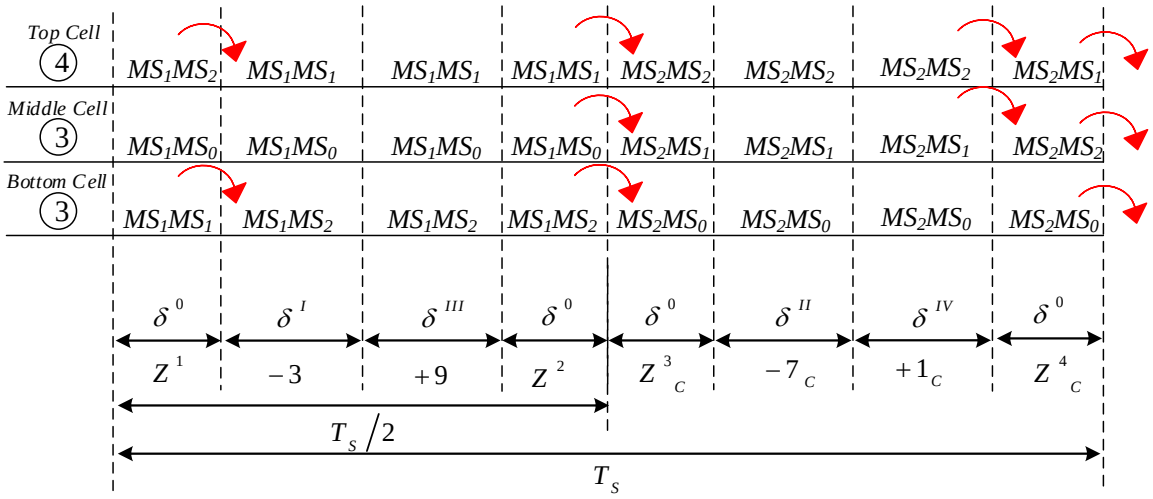


Figure 3.36: Commutation sequence in a switching period T_S (when both current and voltage vectors are in sector 1) with the Space Vector Modulation method

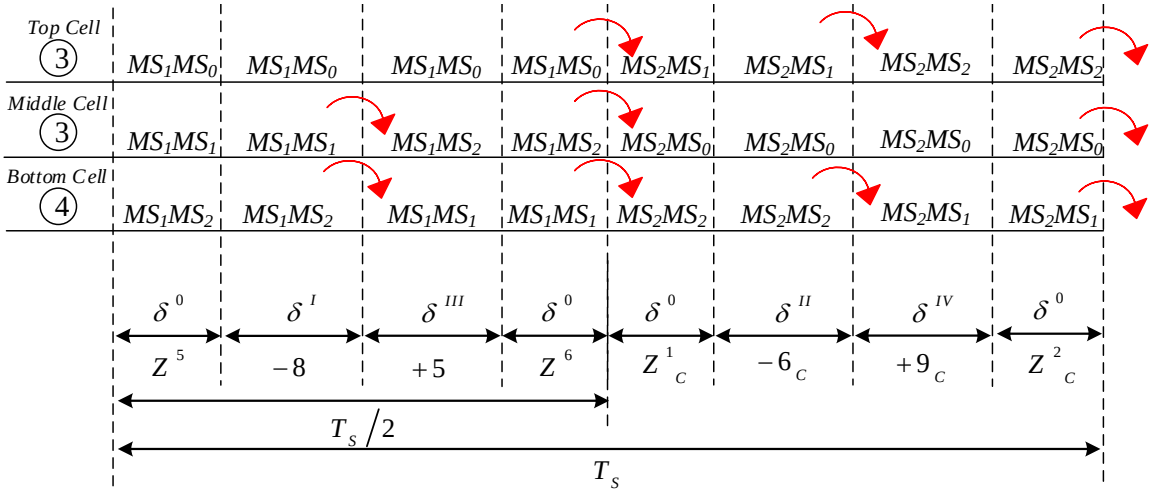


Figure 3.37: Commutation sequence in a switching period T_S (when both current and voltage vectors are in sector 2) with the Space Vector Modulation method

The scalar and vector modulation methods are compared for different parameters in Table 3.4. From Table 3.4, it can be seen that considering the power quality, the SVM shows slightly better performance than its scalar-equivalent, the Double Optimum Venturini Modulation (DOVM) but this comes at a cost of increased complexity in implementation due to a higher number of the commutation paths. Therefore, the choice of a modulation method is a trade-off between performance and complexity.

Table 3.4: Comparison of the modulation methods

	Vector Approach	**Scalar Approach**		
Parameter	SVM	DOVM	DVM	VM
Voltage Regulation Ratio (q)	1.73	1.73	1	0.5
THD in Input Current (I_{Ki}) [1]	61.9%	62.0%	110.6%	107.1%
THD in Output Voltage (V_{jo})	61.1%	61.5%	165.2%	161.7%
No. of Cell-Commutations	30	30	30	30
Commutation Sequence per-cell	Variable	Fixed	Fixed	Fixed
No. of Steady-States Required	6	4	4	4
No. of Commutation Paths	30	9	9	7
Implementation Complexity	High	Low	Low	Low

[1] Note that the THD of the input current was recorded without input filters

3.7 Conclusions

The Modular Isolated Matrix Converter (MIMC) is the extension of the Direct Matrix Converter to an isolated case. The Direct Matrix Converter uses a three-phase input to decouple the fundamental frequency of the output from that of the input. The input side, in the Direct Matrix Converter, behaves as a voltage source while the output side behaves as a current source. As the fundamental concept of the MIMC comes from the Direct Matrix Converter, these assumptions remain the same for the MIMC. Therefore, the Direct Matrix Converter modulation techniques can be applied to the MIMC after some adaptation.

If a scalar modulation method known as *Venturini Modulation (VM) Method* was implemented on the MIMC then a maximum voltage regulation ratio of 0.5 can be observed. Due to the presence of a series connection of the output side bridges in the MIMC, this voltage regulation ratio is increased to unity by using *Double Venturini Modulation (DVM) Method* which modifies the traditional VM method. A further increase in the voltage regulation, to $\sqrt{3}$, is also possible by using *Double Optimum Venturini Modulation (DOVM) Method* which is based on the third-harmonic injection scheme. More modulation possibilities were explored using a vector approach known as *Space Vector Modulation (SVM)*. It has been observed that power quality obtained with the SVM method was slightly better than its scalar-equivalent modulation method (DOVM), but this comes at a cost of increased complexity in implementation. This is because the SVM method will require a higher number of commutation paths to be implemented in the FPGA.

A higher control performance is possible with the SVM method due to the availability of a large number of redundant vectors but this will require higher processing power specifically when the selection between the redundant vectors is done online. Therefore, the choice of the modulation method, being a trade-off, is application specific which will be made after considering the commutation method for the MIMC.

Chapter 4

The Commutation Method

4.1 Introduction and Requirement

In power electronic converters, the commutation method defines the process through which safe-transition between switching states takes place. A transition is called *'safe-transition'* if neither the voltage source is short-circuited nor the current-source is open-circuited through the process of transition [69].

A short-circuit of a voltage source in power converter will result in catastrophic over-current through the semiconductor devices [85] whereas an open-circuit of a current source will cause voltage spikes across the semiconductor devices [70]. Therefore, the commutation failure can cause permanent damage to the semiconductor devices [69, 70]. To achieve a safe current commutation in the MIMC, is particularly challenging in the presence of practical transformers because the switches in the MIMC lack free-wheeling path for current. The problem of current commutation in the MIMC can be discussed in detail by understanding the concept of current commutation first.

A simple form of commutation as can be described using the case of a two-quadrant switch based H-bridge (2QSH-bridge) inverter, as shown in Figure 4.1, where the commutation method is a dead-time between in-coming and out-going switches [86–88]. Consider the timing diagram shown in Figure 4.2 where the commutation takes place from state S_0, S_1 ON to state S_2, S_3 ON and the commutation process can be summarised as:

- A short-circuit of the voltage source is prevented by using a dead-time T_{comm} between the OFF command of switches S_0, S_1 at t_1 and ON command of switches S_2, S_3 at t_3.
- An open-circuit of the current source is prevented by the presence of free-wheeling path provided by the anti-parallel diodes D_0, D_1, D_2 and D_3.

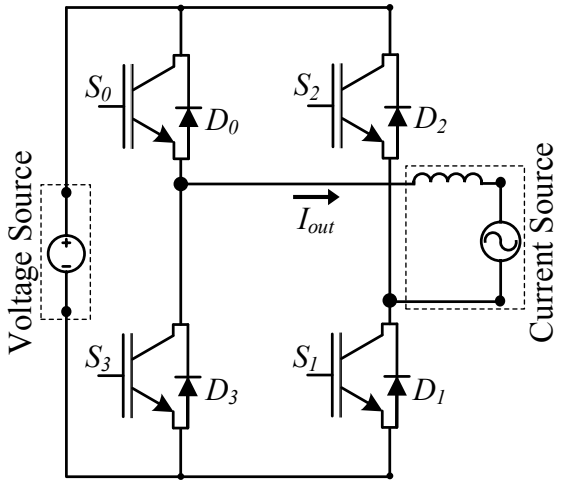


Figure 4.1: 2QSH-bridge with a current source on AC side and a voltage source on DC side

It can be noted that the simplicity of commutation process in 2QSH-bridge comes from the fact that, regardless of the state of the H-bridge, current source always has a conduction path. Thus the only requirement of the commutation process is the selection of appropriate dead-time T_{comm} based on the turn-OFF T_{OFF} and turn-ON T_{ON} times of the switches [88]. However, this is not true in case of a four-quadrant switches based H-bridge (4QSH-bridge) as it lacks natural free-wheeling path [89,90].

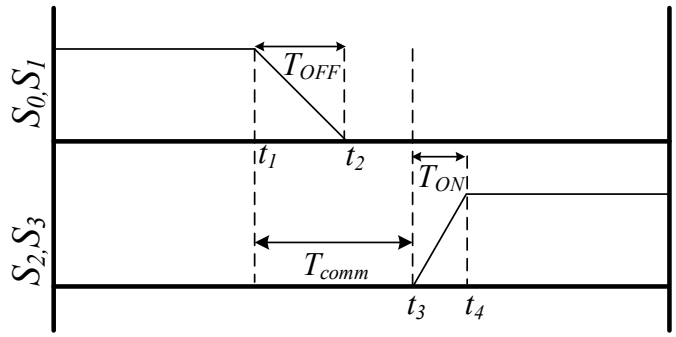


Figure 4.2: Timing diagram of the commutation process in 2QSH-bridge

For example, consider a 4QSH-bridge as shown in Figure 4.3 which also represents the output stage of the MIMC. If a commutation from S_0, S_1, S_2, S_3 ON to S_4, S_5, S_6, S_7 ON is required then a simple dead-time between in-coming and out-going switches, as shown in Figure 4.2, will cause all of the switches, $S_0, ..., S_7$, to be OFF which will interrupt the current, consequently causing an open-circuit commutation failure. This is because if all the switches of 4QSH-bridge are in OFF state there will be no free-wheeling path available [90] for the output current I_{out}. Note that this is true for an inductive load and not for a resistive load as no free-wheeling path will be required in the later case.

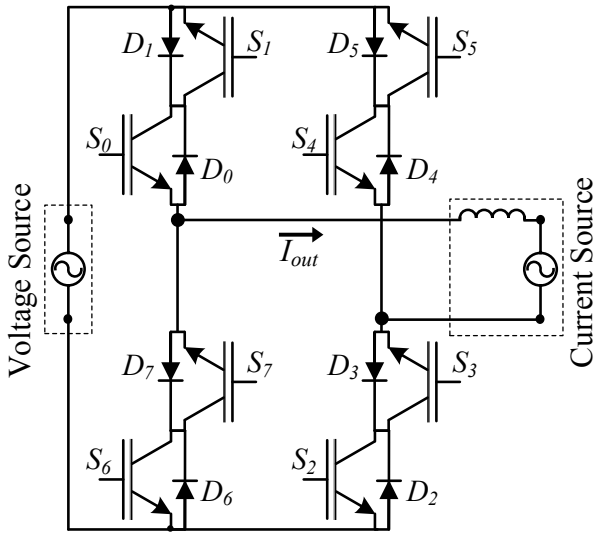


Figure 4.3: 4QSH-bridge with AC current source on output side and AC voltage source on input side

In order to make the simple dead-time commutation method practically viable, the 4QSH-bridge must be equipped with a dissipative clamp circuit to absorb the energy stored in the load inductor at every commutation event. This dumping of load inductor's energy into the clamp circuit at every commutation event will drastically reduce efficiency of the power converter hence making the simple dead-time or single step commutation approach unsuitable for the 4QSH-bridge. Therefore, to achieve safe and reliable commutation of the 4QSH-bridge, a more complicated multi-step approach [88, 91, 92] is required.

4.2 Standard 4-Step Current Commutation Method

To overcome the challenge of commutation in the 4QSH-bridge, a possible solution can be derived from the concept of a multi-stepped approach, for example the 4-step current commutation method [93] which is used in Direct Matrix Converters. As the name suggests, this commutation method takes four steps and the only requirement is information about either the direction of output current [94] or the polarity of input voltage [95].

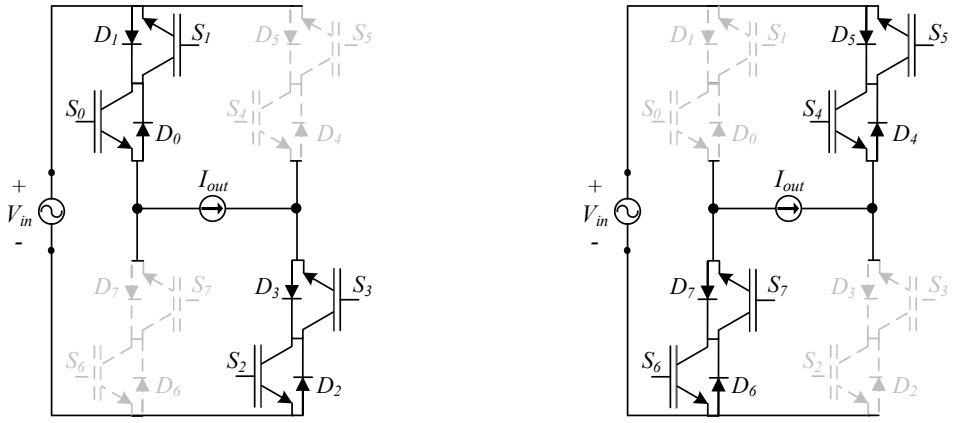
The 4-step current commutation method offers two different solutions:

- The current based 4-step current commutation method
- The voltage based 4-step current commutation method

4.2.1 Current Based 4-step Current Commutation Method

In the current based 4-step current commutation method, information about the direction of the current is required at the initiation of the commutation process with an assumption that the current direction remains same throughout the process [71]. Therefore, the 4-step current commutation method provides a low cost and reliable

solution because current direction information is not required for each of the four steps thus avoiding expensive high-bandwidth sensing. The design and practical implementation of the current detection sensor is presented in detail in Chapter 5. For the derivation of the current based 4-step current commutation method for the 4QSH-bridge [66], consider a case when the required commutation of the 4QSH-bridge shown in Figure 4.3 is from S_0, S_1, S_2, S_3 ON (steady state MS_1) to S_4, S_5, S_6, S_7 ON (steady state MS_2). The definition of the steady states MS_1 and $M2_2$ is same as discussed in Section 3.1 of Chapter 3. For ease of the reader, the steady states are re-shown in Figure 4.4. The current based commutation between these states can be achieved by moving through several commutation states, as shown in Figure 4.5.

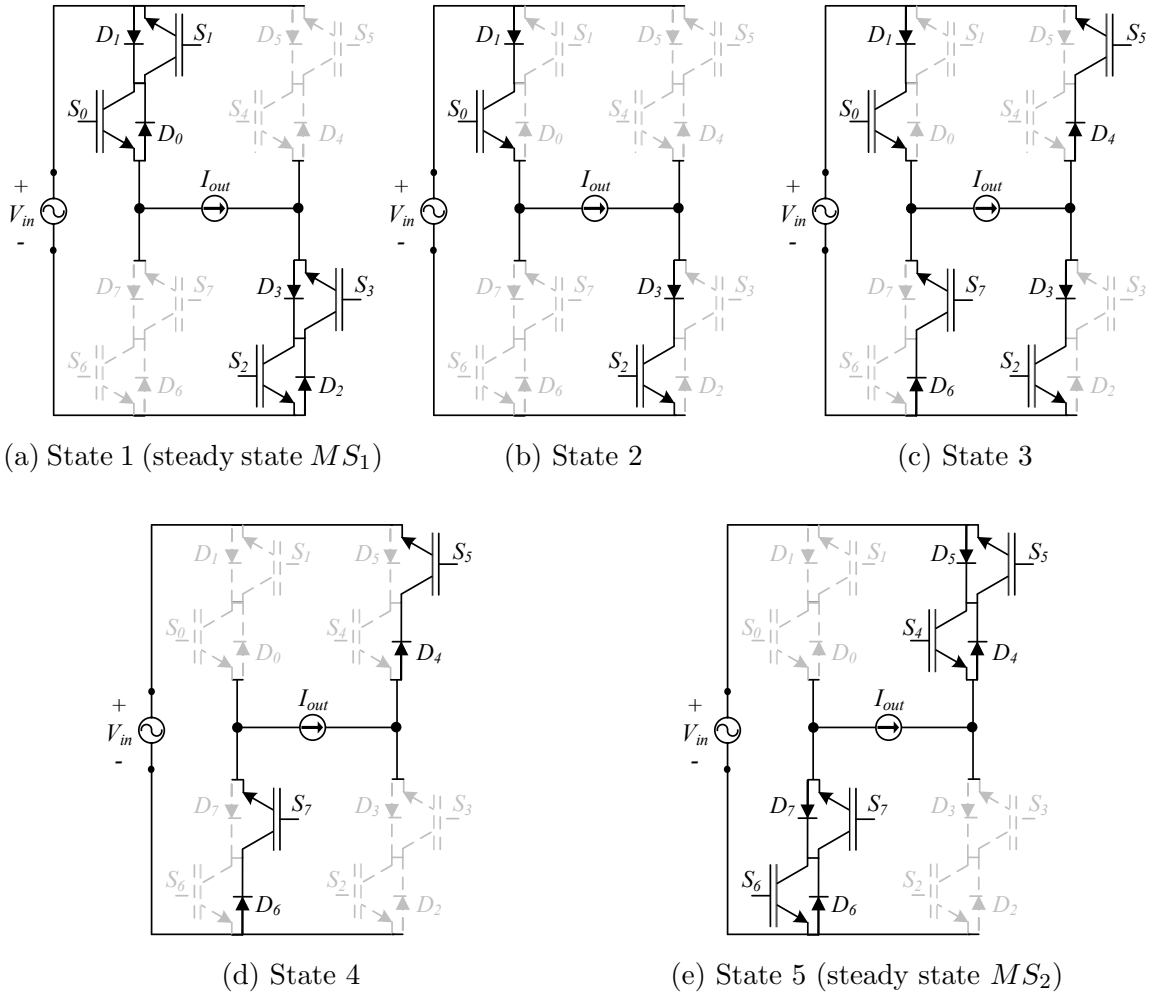


(a) Steady state MS_1 (b) Steady state MS_2

Figure 4.4: Illustration of steady-states MS_1 and MS_2

Note that the assumption that the current source direction does not alter during the process of commutation can be represented by a fixed magnitude DC current source in the direction $I_{out} > 0$, as shown in Figure 4.5. The commutation procedure is:

- **State 1:** The 4QSH-bridge is in the steady state MS_1 with switches S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7 in ON state and the direction of output current is $I_{out} > 0$ as shown in Figure 4.5a.
- **State 2:** With the assumed current direction $I_{out} > 0$, only switches S_0, S_2 are conducting the current I_{out}, therefore the non-conducting switches S_1, S_3 can be turned OFF safely as shown in Figure 4.5b.



(a) State 1 (steady state MS_1) (b) State 2 (c) State 3

(d) State 4 (e) State 5 (steady state MS_2)

Figure 4.5: Steps in the current based 4-step current commutation method for moving from S_0, S_1, S_2, S_3 ON $(MS_1)$to S_4, S_5, S_6, S_7 ON (MS_2) when $I_{out} > 0$

- **State 3:** The switches which can conduct the current in the direction $I_{out} > 0$, S_5, S_7, are turned ON safely without short-circuiting the voltage source as shown in Figure 4.5c.

  Note that the current I_{out} will transfer from S_0, S_2 to S_5, S_7 at this state or next depending on the polarity of the input voltage V_{in}. If $V_{in} < 0$, the current I_{out} will transfer to S_5, S_7 in state 3 however if $V_{in} > 0$, the current I_{out} will transfer in the state 4.

- **State 4:** The switches S_0, S_2 are turned OFF safely, without disrupting the output current I_{out}, as the switches S_5, S_7 are in ON state and can provide the path to the current as shown in Figure 4.5d.

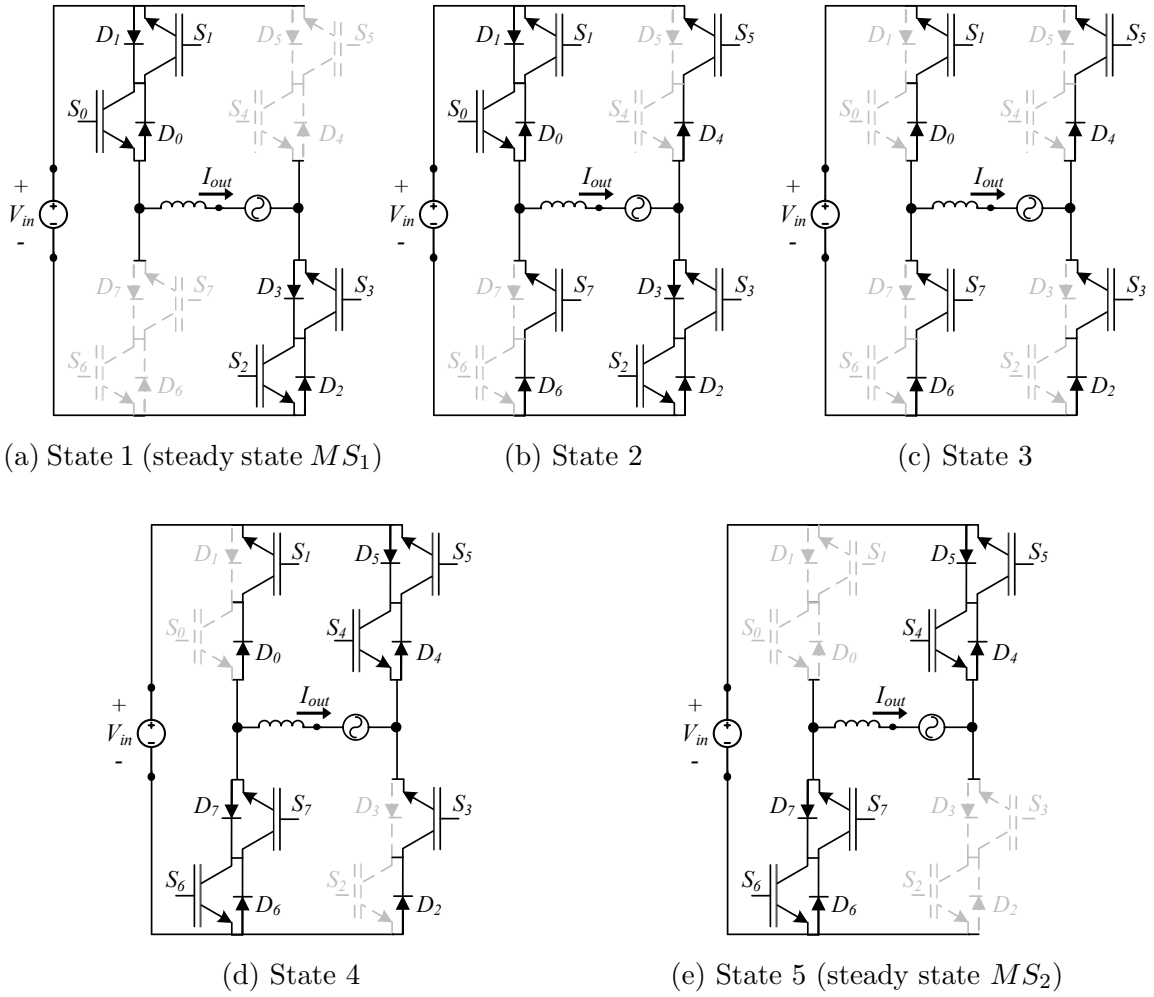
- **State 5:** To be able to reach the steady state MS_2, the 4QSH-bridge must be capable of conducting the output current in the other direction, i.e. $I_{out} < 0$. Hence, the switches S_4, S_6 are finally turned ON, as shown in Figure 4.5e.

4.2.2 Voltage Based 4-step Current Commutation Method

The concept of the voltage based 4-step current commutation method [95] is analogous to the current based current commutation method [94], but it initiates the process based on information about the voltage polarity instead of current direction. No high-bandwidth voltage sensing is required as it is assumed that the voltage polarity remains same throughout the process. For the derivation of the voltage based 4-step current commutation method for a 4QSH-bridge [66], consider the commutation case where the required commutation is from state S_0, S_1, S_2, S_3 ON (MS_1) to state S_4, S_5, S_6, S_7 ON (MS_2). The commutation will be achieved by moving through several commutation states, as shown in Figure 4.6. Note that the same commutation case has been considered to clearly illustrate the difference from the current based current commutation method.

The assumption that the voltage polarity remains same during the process of commutation is represented by a fixed magnitude DC voltage source with the polarity $V_{in} > 0$, as shown in Figure 4.6. The commutation procedure is:

- **State 1:** The 4QSH-bridge is in the steady state MS_1 with switches S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7 in the ON state and the polarity of input voltage is $V_{in} > 0$, as shown in Figure 4.6a.



(a) State 1 (steady state MS_1) (b) State 2 (c) State 3

(d) State 4 (e) State 5 (steady state MS_2)

Figure 4.6: Steps in the voltage based 4-step current commutation method for moving from S_0, S_1, S_2, S_3 ON (MS_1) to S_4, S_5, S_6, S_7 ON (MS_2) when $V_{in} > 0$

- **State 2:** With the assumed polarity of voltage $V_{in} > 0$, switches S_5, S_7 can be turned ON safely without short circuiting the voltage source, as shown in Figure 4.5b.

- **State 3:** Since switches S_5, S_7 are already ON and can provide path for the output current $I_{out} > 0$ the switches S_0, S_2 can be turned OFF safely without open-circuiting the load, as shown in Figure 4.6c.

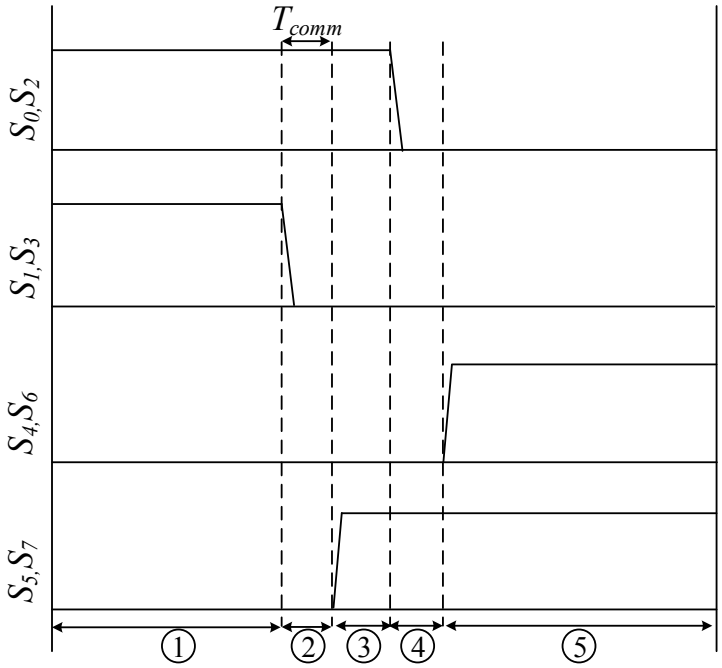
  Note that the current I_{out} will commutate at this state or next. If $I_{out} > 0$, the current I_{out} will transfer from S_0, S_2 to S_5, S_7 in state 3, however if $I_{out} < 0$ the current I_{out} will transfer from S_1, S_3 to S_4, S_6 in the state 4.

- **State 4:** As the polarity of voltage source $V_{in} > 0$ remains same, the switches S_4, S_6 can be turned ON safely as shown in Figure 4.6d.
- **State 5:** Switches S_4, S_6 can conduct the output current $I_{out} < 0$ while the switches S_5, S_7 can conduct the $I_{out} > 0$. So, switches S_1, S_3 are finally turned OFF safely and the 4QSH-bridge reaches steady state MS_2, as shown in Figure 4.6e.

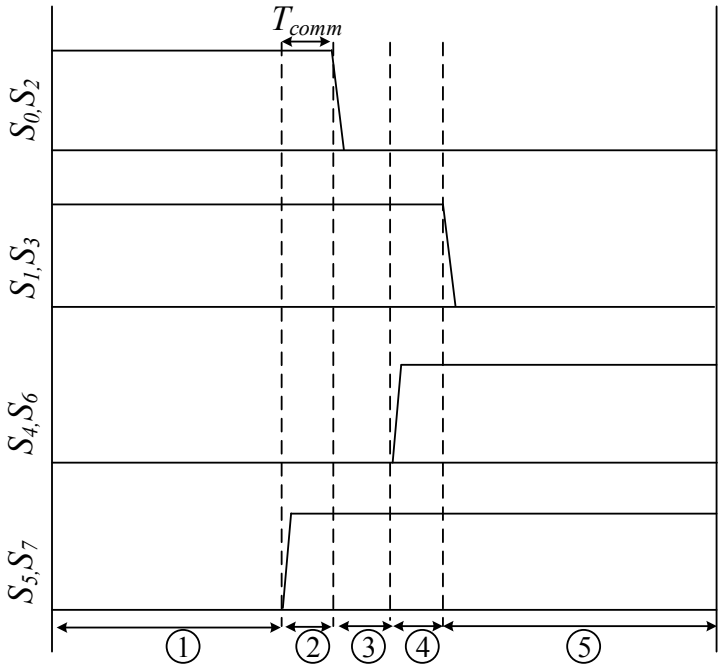
To illustrate the difference between two methods, timing diagrams of both current and voltage based 4-step current commutation methods are presented in Figure 4.7. It is important to mention that any over-lap between the commutation states must be avoided to prevent the shoot-through due to the voltage commutation failure [96]. This can be achieved by introducing a commutation-time T_{comm} between the commutation state changes, as shown in Figure 4.7.

For example, when moving from state 1 to state 2 in current based commutation, shown in Figure 4.7a, the value of T_{comm} should be kept greater than the turn-OFF time of the switches S_1, S_3 i.e. $T_{comm} > T_{OFF}$. Although, the commutation-time between each commutation state can be controlled independently for the ease of practical implementation, the value of T_{comm} is fixed for all the steps [71] based on worst case conditions.

Both of the current commutation methods, current and voltage based, are achieving the same task. The choice to select the current based current commutation method or the voltage based current commutation method can be made by taking into account the application of the 4QSH-bridge. For example in case of the MIMC, the input side bridges have low frequency voltage input and the output side bridges have a low frequency current output. Therefore, for practical design it will be preferable to implement the voltage based current commutation method on the input side bridges whereas the current based current commutation method on the output side bridges because the polarity of the low frequency waveforms at the terminals of the MIMC can be determined more accurately than the MF waveforms at the transformer thus leading to safer current commutation.



(a) Current based 4-step current commutation method when $I_{out} > 0$



(b) Voltage based 4-step current commutation method when $V_{in} > 0$

Figure 4.7: Timing diagrams of current and voltage based 4-step commutation process in 4QSH-bridge for moving from S_0, S_1, S_2, S_3 ON (MS_1) to S_4, S_5, S_6, S_7 ON (MS_2)

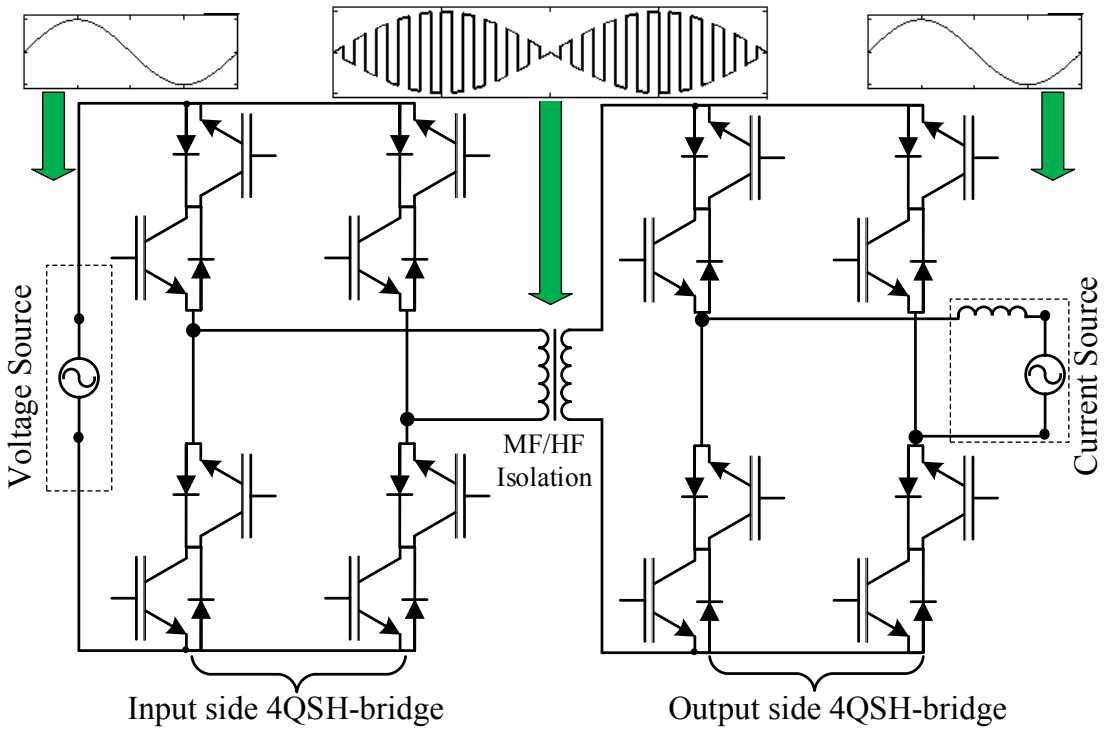


Figure 4.8: A single-cell of the MIMC

However, by using the voltage based 4-step current commutation method on input 4QSH-bridges and current based on output side 4QSH-bridges for the MIMC, each 4QSH-bridge in the MIMC will have an independent commutation, as presented in [66], but the commutation will only be safe if the transformer is ideal with zero leakage inductance. In this case, even a small value of the leakage inductance in the transformer can cause potential damage to the semiconductor devices as whenever the output side 4QSH-bridge requires the state change which corresponds to reversal of current through transformer this abrupt change of current will be opposed by the leakage inductance of the transformer. This is essentially equivalent to connecting in series two current sources with current in opposite direction which result in a voltage spike [97] across semiconductor devices during each commutation. The resulting voltage spikes will damage the semiconductor devices leading to the failure of the MIMC. Therefore, the impact of the leakage inductance of transformer on the 4-step current commutation method must be studied in detail as this is the key technological development for the MIMC topology to be considered for practical applications.

4.3 Impact of Transformer's Leakage Inductance on Standard 4-step Current Commutation Method

The current based 4-step current commutation sequence for 4QSH-bridge was proposed in [65, 66], but the impact of transformer leakage inductance on the commutation process was neglected, thus it relies on negligible transformer leakage to successfully complete the commutation. For practical implementation of the standard 4-step commutation method, a snubber or a clamp circuit would be necessary to absorb the energy stored in the transformer's leakage inductance which would otherwise damage the semiconductor devices. To analyse the impact of transformer's leakage inductance on standard 4-step current commutation method, consider a single-cell of the MIMC with a non-ideal transformer as shown in Figure 4.9. Regardless of the direction of power flow in the single-cell of the MIMC, almost all of the current will be passing through the leakage inductance and only a small part will go towards magnetising inductance [53]. Therefore, regarding commutation only the leakage inductance has been considered as shown in Figure 4.9.

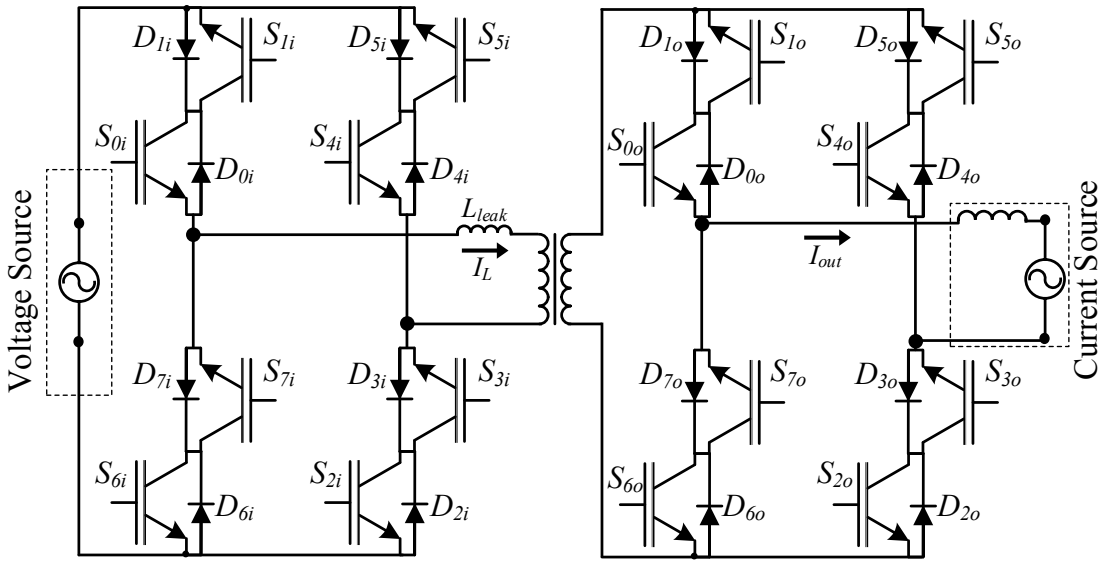


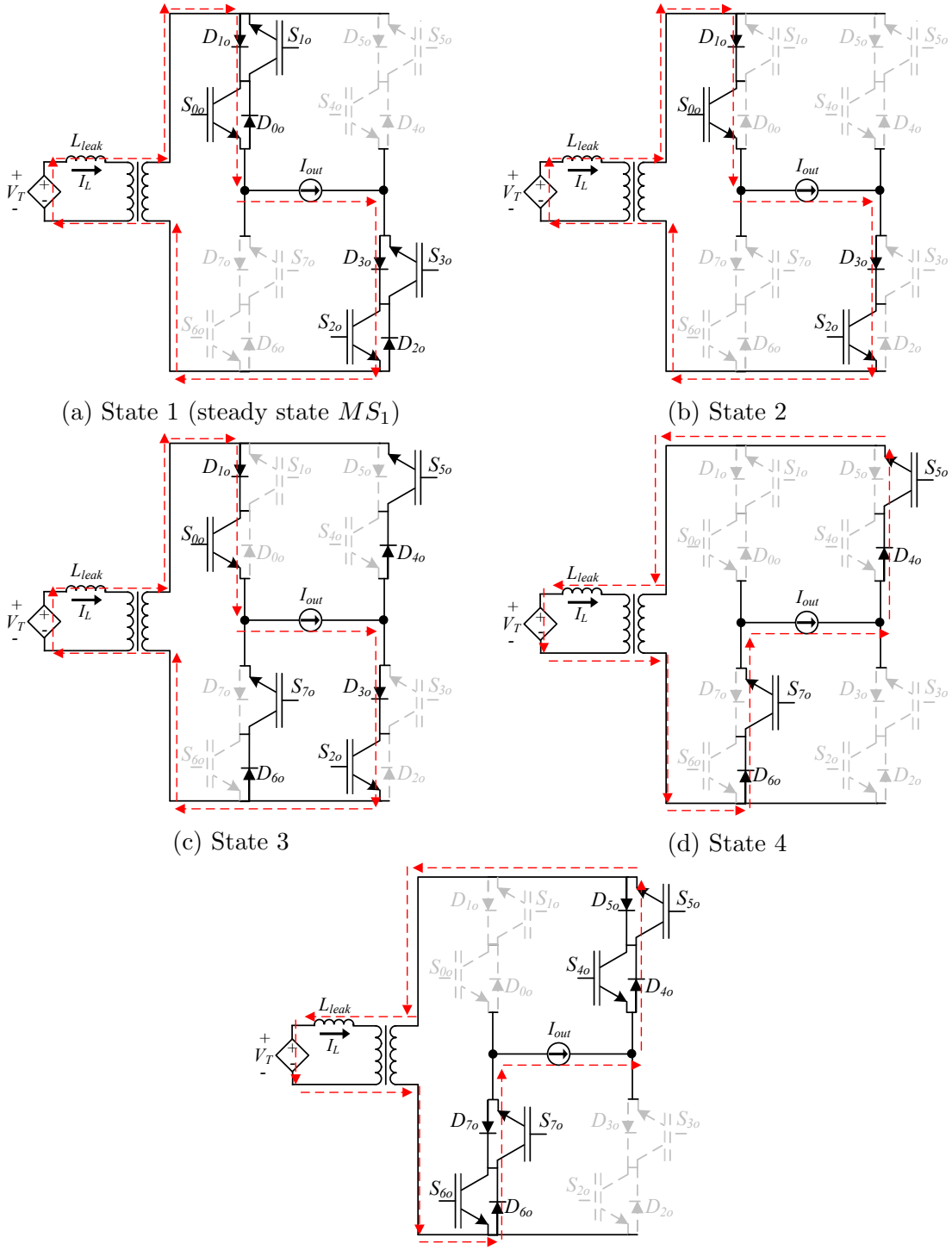
Figure 4.9: A single-cell of the MIMC with a non-ideal transformer

For the ease of understanding the impact of leakage inductance, consider a simple case when only the output side 4QSH-bridge commutates and the input side 4QSH-bridge does not commutate. An example of such a case is the commutation of output side 4QSH-bridge from $S_{0o}, S_{1o}, S_{2o}, S_{3o}$ ON (MS_1) to $S_{4o}, S_{5o}, S_{6o}, S_{7o}$ ON (MS_2) when $I_{out} > 0$. As only the state of the output side 4QSH-bridge changes, the input side 4QSH-bridge can be represented by a constant voltage source during the commutation process, as shown in Figure 4.10. Following the designed current based 4-step commutation approach, the commutation states of the output side 4QSH-bridge are shown in Figure 4.10.

Although the derivation of states 1-5, shown in Figure 4.10, have already been discussed in Section 4.2.1, the effect of a non-negligible leakage inductance can be analysed by considering, states 3 and 4. Note that in state 3 (Figure 4.10c), $I_L = I_{out}$ but when switches S_{0o}, S_{2o} are turned off in state 4 (Figure 4.10d), the current is expected to change path to switches S_{5o} and S_{7o}, thus reversing the direction of the leakage inductance current abruptly from $I_L = I_{out}$ to $I_L = -I_{out}$. The change of current direction will be opposed by the leakage inductance, causing an over-voltage across the semiconductor devices of the output side 4QSH-bridge. If L_{leak} is the transformer's leakage inductance seen from primary side and T_{OFF} is the turn-OFF time of the switches S_{0o} and S_{2o}, then the peak of the voltage spike V_{PK} can be approximated by (4.1), assuming a linear current variation during turn-off of the switches and no clamps circuits:

$$V_{PK} = \frac{2I_{out}L_{leak}}{T_{OFF}} \tag{4.1}$$

For practical implementation of the 4-step current commutation method, all the bridges in the MIMC must be equipped with dissipative clamp circuits to prevent the semiconductor devices from dangerously high over-voltages such that whenever current commutation fails, any voltage spike is clamped to the voltage of the clamp circuit capacitor. Note that the configuration of the clamp circuit is shown in Figure 4.11. The drawback is that the clamp will be triggered every time the modulation requires transitions that reverses the leakage inductance current I_L, thus leading to additional losses.



(a) State 1 (steady state MS_1)

(b) State 2

(c) State 3

(d) State 4

(e) State 5 (steady state MS_2)

Figure 4.10: 4-step current commutation method with non-negligible leakage inductance of transformer for moving from $S_{0o}, S_{1o}, S_{2o}, S_{3o}$ ON (MS_1) to $S_{4o}, S_{5o}, S_{6o}, S_{7o}$ ON (MS_2) when $V_T > 0, I_{out} > 0$

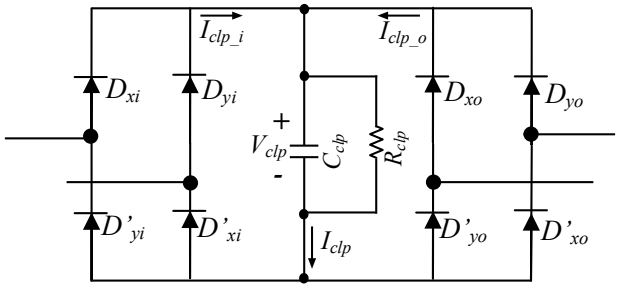
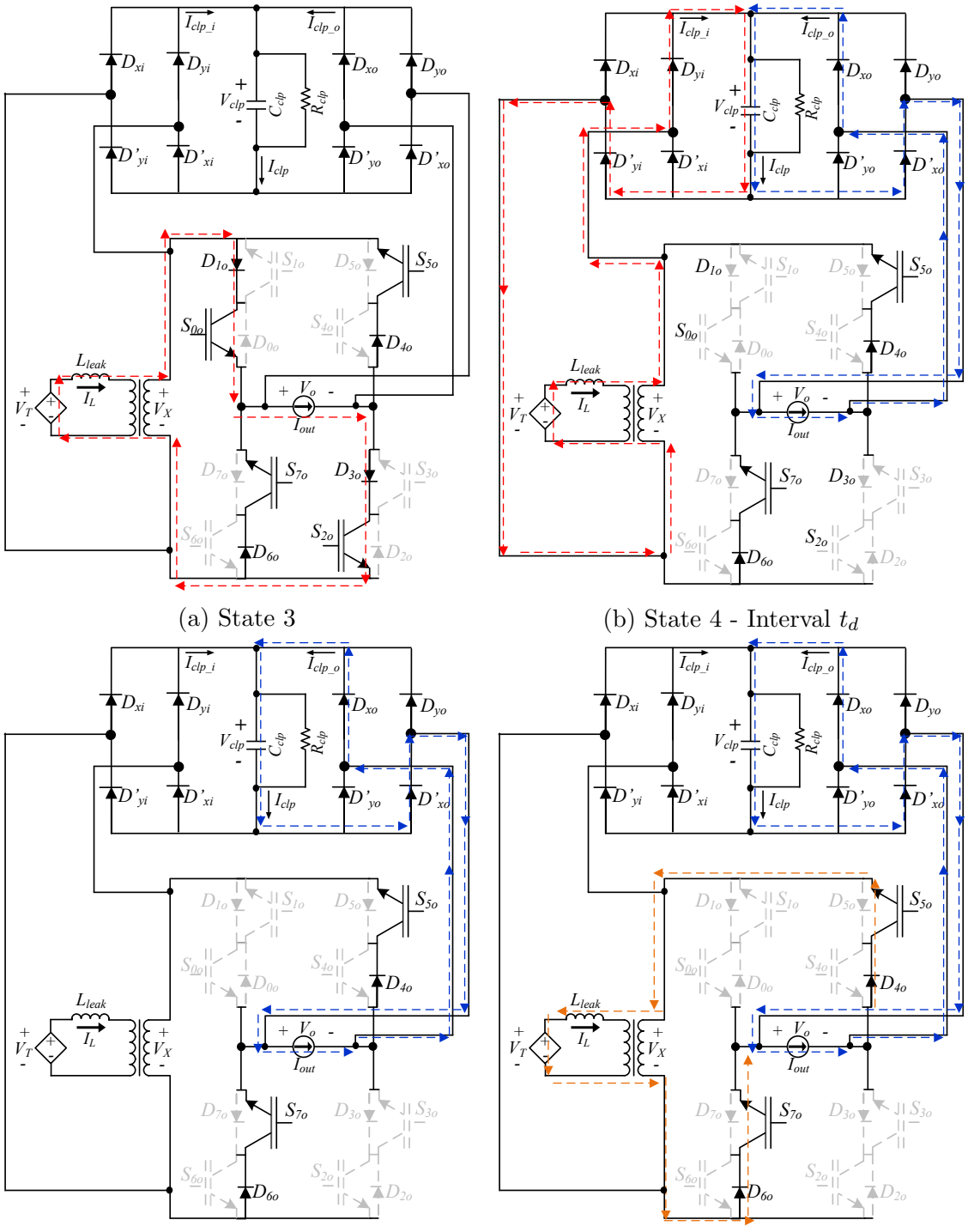


Figure 4.11: Clamp circuit configuration

To highlight the resulting activation of the clamp circuit with a standard 4-step current commutation method, the equivalent circuits, during the transition from state 3 to state 4, are shown in Figure 4.12. Furthermore, a timing diagram has been presented in Figure 4.13 to clearly illustrate the waveforms during the clamp activation. Up till state 3 (Figure 4.12a), the clamp circuit is OFF and no current flows because $I_L = I_{out}$, but in state 4 (Figure 4.12b) the leakage current I_L is taken up the diodes D_{yi} and D'_{yi} making $I_{clp_i} = I_L$ whereas the output current I_{out} is taken up the diodes D_{xo} and D'_{xo} making $I_{clp_o} = I_{out}$. This will cause the voltage V_X to be clamped to V_{clp} and output voltage V_o to be clamped to $-V_{clp}$. The leakage current I_L will start to decrease, in interval t_d, as shown in Figure 4.12b, with a slope of $\frac{V_T - V_{clp}}{L_{leak}}$ until it becomes zero. The leakage inductance is fully discharged in the end of interval t_d (Figure 4.12c). Note that $V_{clp} > V_T$ because the clamp circuit is usually charged to the peak of the input voltage.

Although the leakage current is zero at the end of interval t_d the output current I_{out} is still flowing into the clamp circuit, still maintaining the clamping $V_X = -V_o = V_{clp}$ and charging the leakage inductance L_{leak} until $I_L = -I_{out}$. At this point in time no more current will flow into the clamp circuit at the end of charging interval t_c. The waveforms of I_{clp_i}, I_{clp_o} and the total current of clamp I_{clp} are shown in Figure 4.13. The time-domain equation for the total current flowing into the clamp can be expressed by (4.2).

$$I_{clp}(t) = \frac{-\left(|I_L| + |I_{out}|\right)}{t_d + t_c} t + \left(|I_L| + |I_{out}|\right) \tag{4.2}$$



(a) State 3

(b) State 4 - Interval t_d

(c) State 4 - End of interval t_d

(d) State 4 - Interval t_c

Figure 4.12: Equivalent circuits highlighting the activation of clamp with standard 4-step current based commutation of the output bridge from MS_1 to MS_2 for the case $V_T > 0, I_{out} > 0$

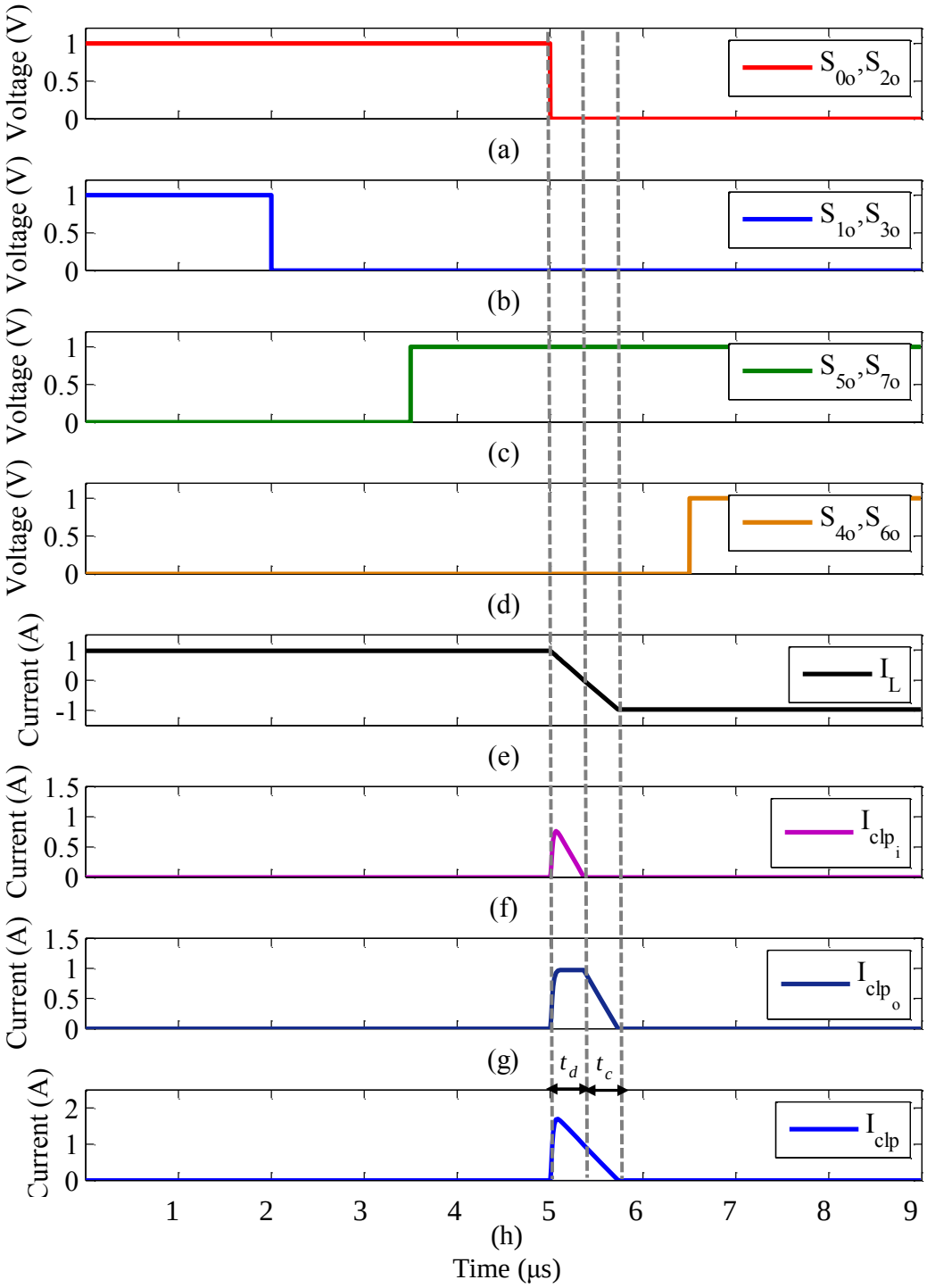


Figure 4.13: Timing diagram showing the activation of clamp circuit when standard 4-step commutation method is used. (a)-(d) switching signals during standard 4-step current commutation of the output side 4QSH-bridge (e) transformer leakage inductance current I_L (f)-(h) currents in the clamp circuit corresponding to Figure 4.12.

The minimisation of the leakage inductance by various methods, such as interleaving the windings [98,99], will attenuate but will not eliminate the problem. In practice it is not always possible to have adequate control over the negligible leakage inductance due to cost, complexity [100] and other system constraints [99]. Therefore a different commutation approach is needed to remove the undesired over-voltages and clamp loss commutation process.

To date, various current commutation methods have been reported in the literature to deal with the leakage inductance energy. For example, employing snubber circuits [101, 102] can help to mitigate the issue but at the cost of additional circuitry and reduced power density.

The snubber capacitors can also be used in parallel to the semiconductor devices [103] but this can lead to turn-ON loss in the devices, as the energy of the capacitor will be dissipated in the semiconductor device and an auxiliary biasing circuit would be required to mitigate the issue. A second approach can be the introduction of a capacitor at the primary side of the transformer, forming a parallel-resonant tank with the magnetisation inductance [5,104]. This approach achieves soft-switching but the leakage energy is dissipated in the transformer winding resistance and tuning of the resonant tank can be challenging. In [58,67] a capacitor in series with the leakage inductance which forms a series-resonant tank is introduced.

A common drawback of all the discussed methods is that they require additional energy storage components or circuits to address the commutation issue. An alternative method to deal with commutation in the presence of leakage inductance could be to drive the commutation using a controllable voltage source. This method does not require additional energy storage components, thus maintaining the power density and avoiding resonance related problems. In this type of method the current is controlled by a controllable voltage source. Therefore it is usually referred to as *source based current commutation method* in [3]. Although the source based current commutation method for a single-phase DC/AC converter [105] achieves complete soft-switching of the AC side 4QSH-bridge, it does not take into account the effect

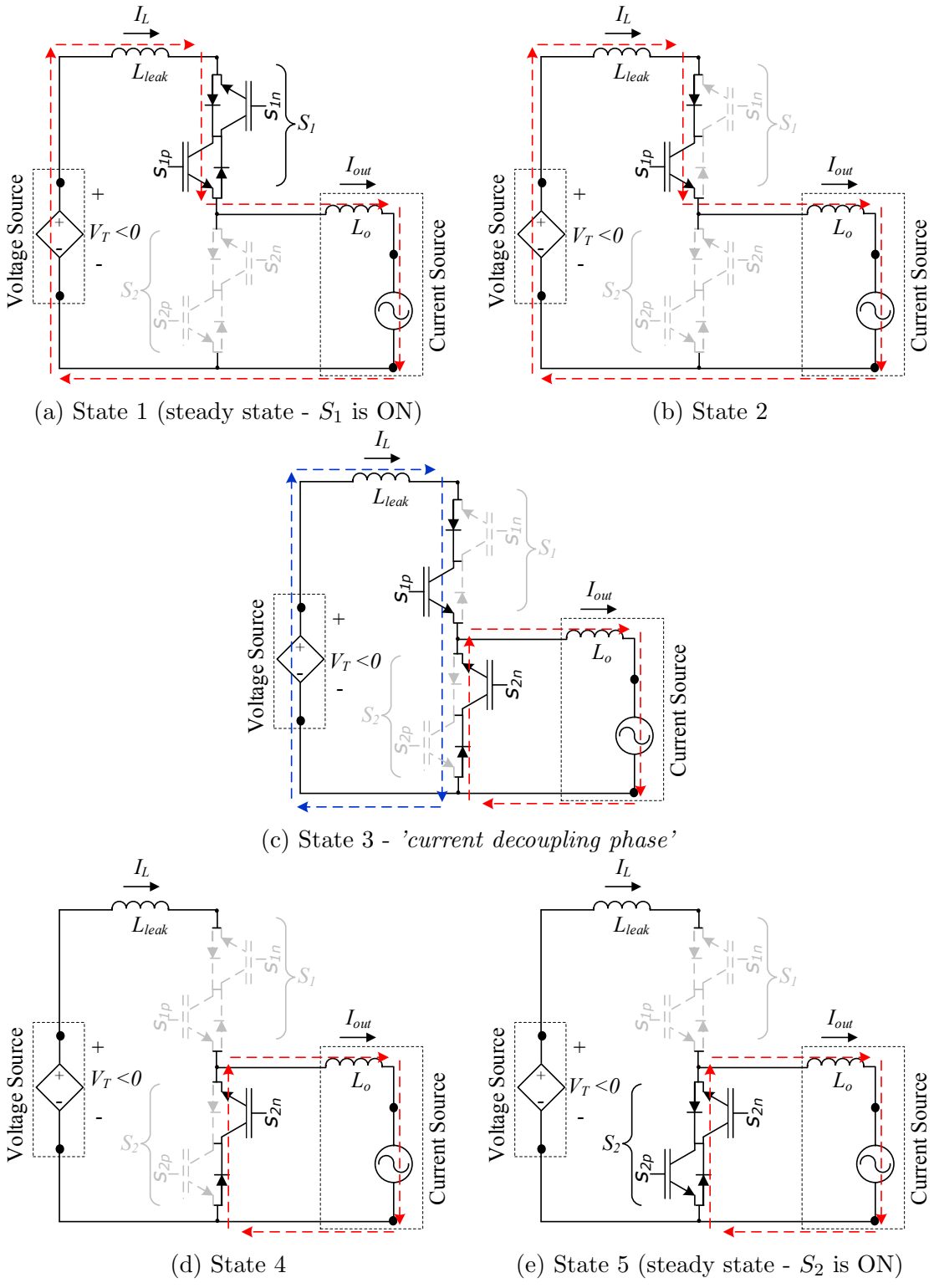
of the leakage inductance. Recently, the importance of the impact of the leakage energy has been highlighted for a MF/HF isolated three phase to three phase direct converter [3]. Note that the proposed solution [3] is only applicable to the specific three-phase to three-phase direct converter and, so far, no research has been done to demonstrate safe-commutation of a single-phase AC/AC converter (single-cell of the MIMC), in presence of leakage inductance. There is a need to clearly address a generalised concept for the source based current commutation method to tackle the leakage inductance energy which can be implemented on all the Matrix-Converter-based topologies of this type.

4.4 A Source Based Leakage Inductance Tolerant Current Commutation Method

The proposed source based leakage tolerant current commutation concept is based on the introduction of an intermediate state, named the *'current decoupling phase'*, during which the leakage inductance current is modified. The leakage inductance current is driven by the input voltage or a modulated version of it to bring its magnitude to the new value required after commutation without requiring snubbers or clamps.

4.4.1 Basic Principle

To illustrate the basic idea, consider the circuit shown in 4.14. It is assumed that the converter has a voltage source at the input and a current source at the output, represented by the filter inductor L_o. The filter inductor is assumed much larger than the leakage inductance, $L_o >> L_{leak}$, so that during commutation the leakage inductance current can be modified while the output current remains nearly constant. In this simple example, the input voltage comes from the previous stage of the converter and is represented by a controllable voltage source V_T.



(a) State 1 (steady state - S_1 is ON)

(b) State 2

(c) State 3 - *'current decoupling phase'*

(d) State 4

(e) State 5 (steady state - S_2 is ON)

Figure 4.14: Illustration of basic principle of the proposed source based leakage tolerant current commutation method

Consider the case where the circuit has to commutate from state 1, as shown in Figure 4.14a, with $S1 = ON$, $S2 = OFF$ to state 5, as shown in Figure 4.14e, with $S1 = OFF$, $S2 = ON$. Also assume that $I_{out} > 0$, $I_L > 0$ and the voltage V_T is reversed i.e. $V_T < 0$ at the instant of commutation.

Under these conditions, the first commutation step is to open the switch that is not carrying current in $S1$ ($S1n$), as shown in Figure 4.14b. Next the switch that can carry I_{out} in $S2$ ($S2n$) is closed. This initiates the most important state of the commutation process which is the *'current decoupling phase'* as shown in Figure 4.14c.

In the *'current decoupling phase'*, the leakage inductance current I_L is decoupled from the output current I_{out} and all of the voltage from the controlled voltage source V_T is imposed across the leakage inductance L_{leak} only as the output current source is short-circuited via $S2n$ which in turn starts to reduce the leakage inductance current I_L from the value $I_L = I_{out}$ to $I_L = 0$ with a rate of discharge $-\frac{V_T}{L_{leak}}$. Once the leakage current I_L is zero, switch $S1n$ can be turned-OFF safely, completing the *'current decoupling phase'* and reaching the state 4, as shown in Figure 4.14d. Now the switch $S2p$ can be turned-ON safely to reach the steady state condition shown in Figure 4.14e. Note that the safe commutation can be achieved by appropriate timing and that no zero-crossing detection of the current is required.

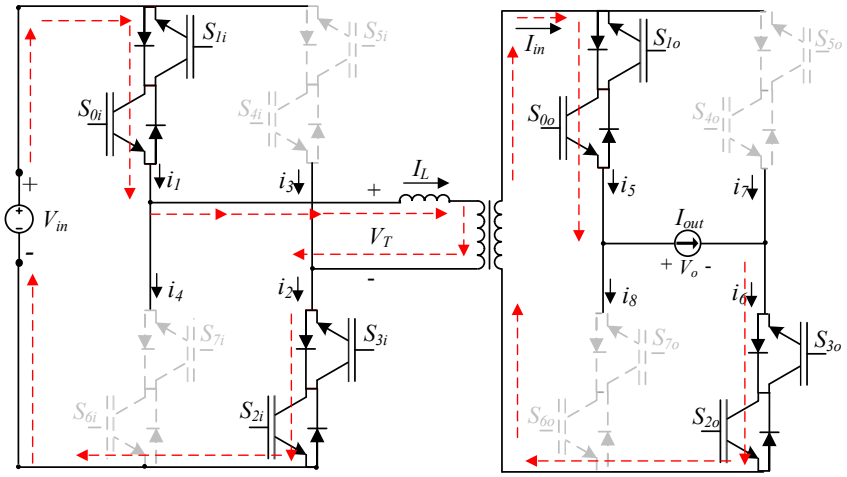
Although in the source based commutation example hence given above, a minimal circuit has been shown to demonstrate the generalised concept but the leakage current reversal $I_L = I_{out}$ to $I_L = -I_{out}$ will be shown in Section 4.4.2 with the full circuit.

It is important to mention that when V_T is an AC voltage source it will not be possible to achieve safe-commutation when voltage is zero as it will require infinite time to discharge the leakage inductance L_{leak}. To cope with this scenario a minimum voltage V_{in}^{MIN} can be set below which the commutation will not be performed.

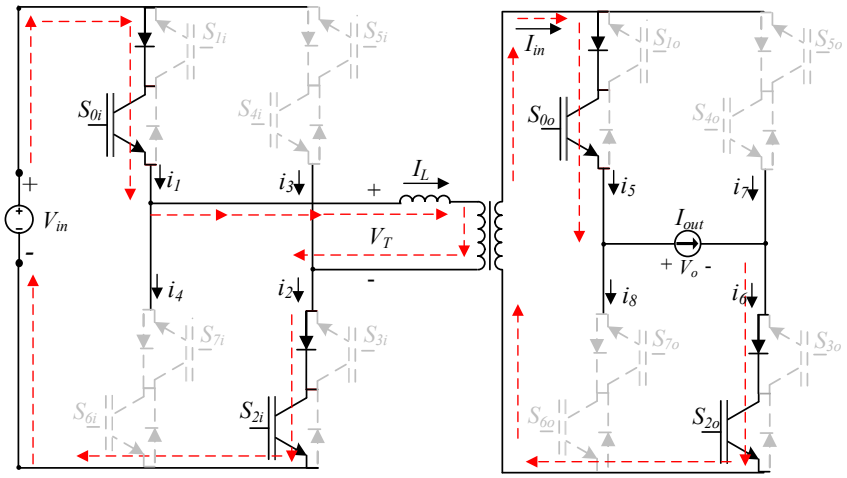
4.4.2 Source Based Leakage Tolerant Current Commutation Method For the MIMC

From the generalised concept of the source based leakage tolerant current commutation method, it can be seen that a voltage source is required to drive the leakage current. This current commutation concept can be applied to the MIMC by shorting the output 4QSH-bridge to decouple the output current from the leakage current and then imposing the voltage using the 4QSH-input bridge. Therefore, both input and output side 4QSH-bridges will take action together to achieve safe current commutation unlike standard 4-step commutation where each bridge commutates independently. This requires the designing of the source based leakage tolerant current commutation method for a single-phase to single-phase AC/AC converter which is the single-cell of the MIMC, as shown in Figure 4.9. Once source based leakage tolerant current commutation method is designed for a single-cell of the MIMC then the same design can be applied to all the cells of the MIMC.

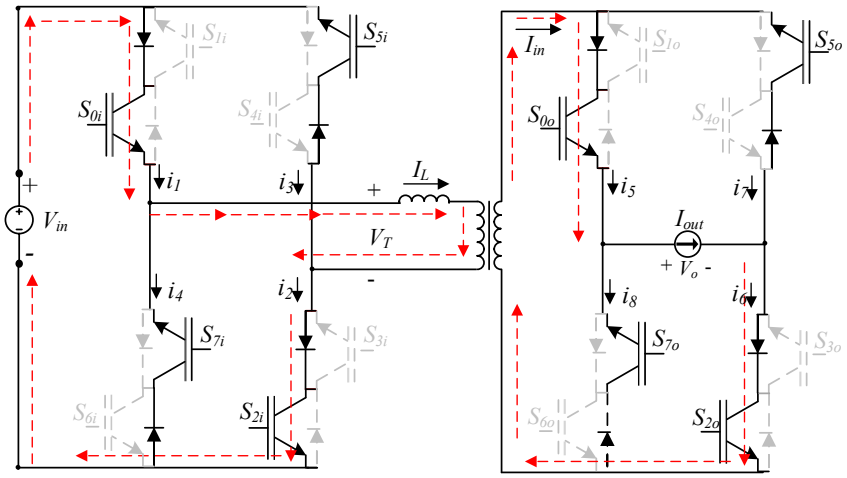
For a single-cell of the MIMC, there can be many possible commutation scenarios depending on the steady state transitions required by the modulation method used and also the direction of the output current and the polarity of the input voltage. First, the concept of the proposed current commutation method can be applied to a single commutation scenario and then all the other commutation cases can be derived following the same approach. The design example, discussed below, shows one of steady-state transitions required by Venturini Modulation for the single-cell to move from steady-state MS_1MS_1 to MS_2MS_2 when the polarity of input voltage V_{in} and the direction of output current I_{out} are both positive, $V_{in} > 0$, $I_{out} > 0$. Note that the polarity of V_{in} and the direction of I_{out} remain effectively constant during the commutation interval as the commutation time is much smaller than their fundamental period. Given that the commutation time is a negligible fraction of the input and output fundamental periods, this is a valid assumption. Therefore, for the design of the current commutation method the voltage and current sources can be represented by fixed polarity or direction DC sources, as shown in Figure 4.15.



(a) State 1 (steady state - MS_1 MS_1)



(b) State 2



(c) State 3

Figure 4.15: States (1-3) of proposed commutation strategy for single-phase AC/AC converter when $V_{in} > 0$, $I_{out} > 0$ and moving from MS_1 MS_1 to MS_2 MS_2

- **State 1:** Initial state: The converter is in steady state with a total of 8 switches, 4 switches of input side 4QSH-bridge $S_{0i}, S_{1i}, S_{2i}, S_{3i}$ and 4 switches of output side 4QSH-bridge $S_{0o}, S_{1o}, S_{2o}, S_{3o}$, in the ON state and the cell is in the steady-state MS_1MS_1, as shown in Figure 4.15a. In this initial state:

$$V_{in} = V_T = V_o \tag{4.3}$$

$$i_1 = i_2 = i_5 = i_6 = I_{out} = I_L \tag{4.4}$$

$$i_3 = i_4 = i_7 = i_8 = 0 \tag{4.5}$$

- **State 2:** With the assumed polarity of the input voltage $V_{in} > 0$ and direction of the output current $I_{out} > 0$, the non-conducting switches of the cell S_{1i}, S_{3i} and S_{1o}, S_{3o} can be turned-OFF. Note that equations (4.3)-(4.5) remain valid.

- **State 3:** Switches S_{5i}, S_{7i} and S_{5o}, S_{7o} can conduct the current in the direction $I_{out} > 0$ and therefore can be turned on safely without short-circuiting the voltage source V_{in}. Equations (4.3)-(4.5) still valid. Note that the current through S_{5i}, S_{7i} and S_{5o}, S_{7o} remains zero because the anti-parallel diodes of S_{4i}, S_{6i} and S_{4o}, S_{6o} are all reverse biased.

- **State 4 - First *'current decoupling phase'*:** Since switches S_{5i}, S_{7i} and S_{5o}, S_{7o} are now already in the ON state and can provide a path for the current $I_{out} > 0$ switches S_{0i}, S_{1i} in the input side 4QSH-bridge can be turned-OFF safely without open-circuiting the output.

  When the input side switches are turned-OFF the leakage inductance current I_L forces the anti-parallel diodes of S_{4i}, S_{6i} and S_{4o}, S_{6o} into conduction. As a result, the output current I_{out} now circulates in $S_{0o}, S_{5o}, S_{2o}, S_{7o}$ and in the anti-parallel diodes of switches $S_{1o}, S_{3o}, S_{4o}, S_{6o}$. This action effectively shorts the secondary winding of the transformer, decoupling the input side 4QSH-bridge from the output side 4QSH-bridge, and in turn decoupling I_{out} from I_L.

At the input side the reversed input voltage appears across the leakage inductance which will start to drive the leakage current I_L towards zero. During this state, equations (4.6)-(4.11) define the circuit behaviour.

$$V_o = 0 \tag{4.6}$$

$$V_T = -V_{in} \tag{4.7}$$

$$i_1 = i_2 = 0 \tag{4.8}$$

$$i_5 = -i_7 = \frac{I_{out}}{2} \tag{4.9}$$

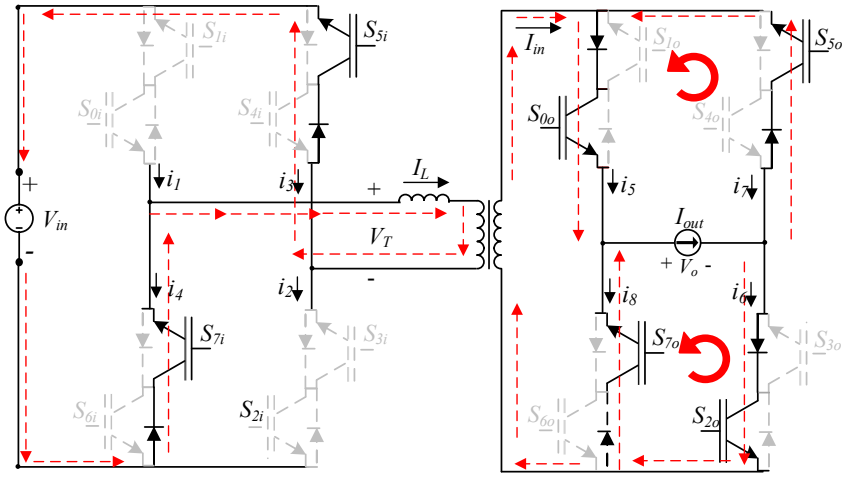
$$i_6 = -i_8 = \frac{I_{out}}{2} \tag{4.10}$$

$$i_L = -i_3 = -i_4 = I_{out} - \frac{V_{in}t}{L_{leak}} \tag{4.11}$$

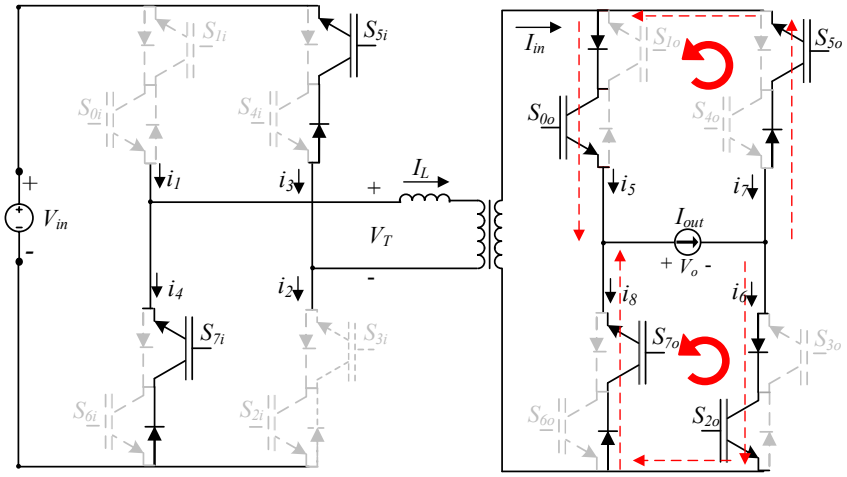
- **State 5 - Second *'current decoupling phase'*:** This state begins when the leakage inductance current I_L that started to decrease in State 4 reaches zero, as given in equation (4.12). Note that the ON/OFF state of the switches is the same as in the previous state, State 4, and no change has been applied. This state could be neglected, but from the perspective of a practical implementation, where the commutation sequence will be timed based on switching times and the worst-case leakage discharge time, the state will be present and has been included here for completeness. Note that this method does not require the detection of the instant when the leakage current I_L reaches zero, $I_L = 0$, thus avoiding the need for sensors.

$$I_L = i_1 = i_2 = -i_3 = -i_4 = 0 \tag{4.12}$$

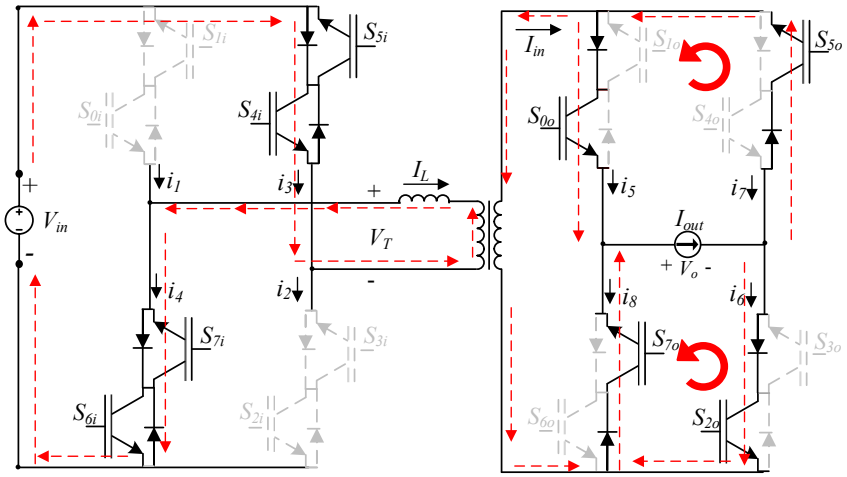
- **State 6 - Third *'current decoupling phase'*:** As the leakage inductance L_{leak} was fully discharged in State 5, the switches S_{4i} and S_{6i} in the input side 4QSH-bridge can now be turned-ON and a negative current through the leakage inductance L_{leak} will start to increase. The output current I_{out} is still circulating in the output side 4QSH-bridge but the leg currents i_5 and i_6 naturally start



(d) State 4



(e) State 5



(f) State 6

Figure 4.15: (Cont.) States (4-6) of proposed commutation strategy for single-phase AC/AC converter when $V_{in} > 0$, $I_{out} > 0$ and moving from MS_1 MS_1 to MS_2 MS_2

to decrease while the currents i_7 and i_8 start to grow, shifting the current from one leg to the other, from i_5, i_6 to i_7, i_8. In this state, equations (4.6)-(4.8) and (4.13)-(4.15) define the currents.

$$i_5 = i_6 = \frac{1}{2}\left(I_{out} - \frac{V_{in}t}{L_{leak}}\right) \tag{4.13}$$

$$i_7 = i_8 = \frac{1}{2}\left(-I_{out} - \frac{V_{in}t}{L_{leak}}\right) \tag{4.14}$$

$$I_L = -i_3 = -i_4 = -\frac{V_{in}t}{L_{leak}} \tag{4.15}$$

- **State 7:** In this state the negative leakage current which started to develop in state 6 reaches the magnitude of I_{out}, $I_L = -I_{out}$, which in turn naturally commutates the output side 4QSH-bridge. The currents i_5, i_6 reach zero whereas the currents i_7, i_8 reach $-I_{out}$ therefore:

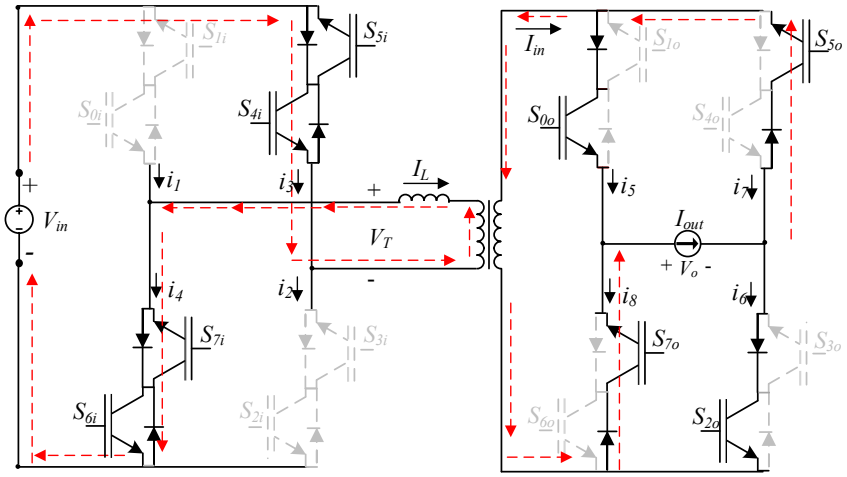
$$V_{in} = -V_T = V_o \tag{4.16}$$

$$i_5 = i_6 = 0 \tag{4.17}$$

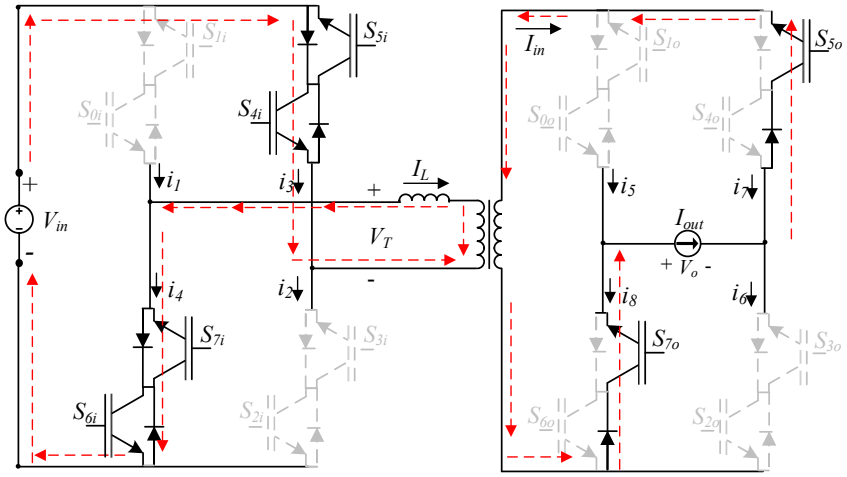
$$-I_L = i_3 = i_4 = -i_7 = -i_8 = I_{out} \tag{4.18}$$

- **State 8:** The current has now naturally commutated from S_{0o}, S_{2o} to S_{5o}, S_{7o} and therefore switches S_{0o}, S_{2o} can be turned-OFF in this state. Note that in this state the current and voltage equations from the previous state are still valid.

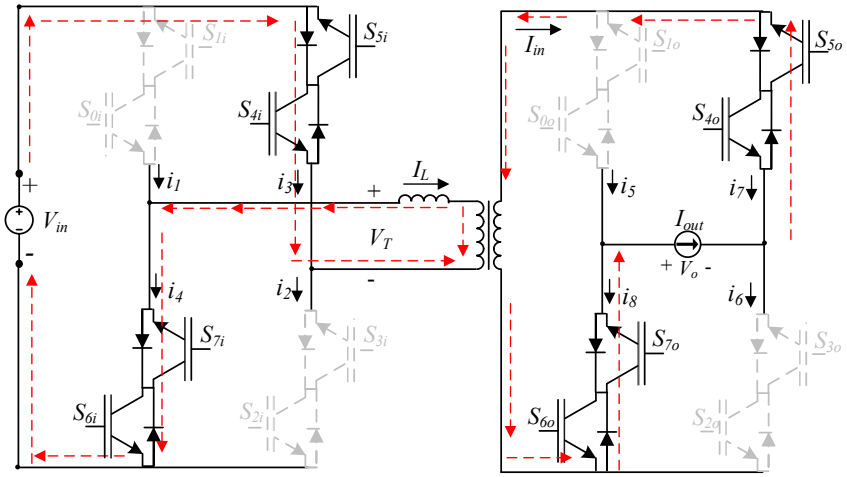
- **State 9:** In order to reach the steady state MS_2MS_2, as shown in Figure 4.15i, the switches S_{4o}, S_{6o} are turned-ON and the converter completes the commutation process. Note that if the turn-ON and turn-OFF times are assumed ideal, the commutation time corresponds to the time required by the leakage inductance L_{leak} to discharge and then recharge, as given by equation (4.19).



(g) State 7



(h) State 8



(i) State 9 (steady state - MS_2 MS_2)

Figure 4.15: (Cont.) States (7-9) of proposed commutation strategy for single-phase AC/AC converter when $V_{in} > 0$, $I_{out} > 0$ and moving from MS_1 MS_1 to MS_2 MS_2

The commutation time is a function of the AC input voltage magnitude that is driving the leakage current I_L. Therefore, for a desired maximum commutation time and load profile, a minimum input voltage exists below which the commutation is not possible. In this condition, the commutation is not immediately performed, resulting in a small zero-crossing output voltage distortion.

$$T_{comm} > 2L_{leak}\left|\frac{I_{out}^{MAX}}{V_{in}^{MIN}}\right| \tag{4.19}$$

In practical applications, the commutation time must be set for the worst-case value based on the possible instantaneous values of input voltage and output current, including the impact of switching times in each of the stages. If this condition is respected, the leakage current reversal occurs without triggering the protection clamps and therefore without generating additional losses.

4.4.3 Theoretical Commutation Waveforms

The theoretical waveforms of both current commutation methods, the source based leakage tolerant current commutation method and the standard 4-step current commutation method have been obtained using a PLECS simulation for the commutation case in Section 4.4.2, from MS_1MS_1 to MS_2MS_2 when $V_{in} > 0$, $I_{out} > 0$, are compared in Figure 4.16. The leakage inductance is assumed to be $L_{leak} = 3.2\mu H$ and the commutation process starts at the instant when $V_{in} = 50V$, $I_{out} = 7A$. To make a fair comparison the same simulation parameters have been used for both of the methods. In the 4-step current commutation method, shown in Figure 4.16a, the output bridge is commutating first and the transition from state 3 to state 4 triggers the protection clamp. As a result, the output voltage V_o stays at minus the clamp voltage until I_L is reversed driven by the voltage $V_T + V_o$, causing power dissipation in the clamp. In the proposed current commutation method, shown in Figure 4.16b, I_L is reversed without triggering the clamp, due to the *'current decoupling phase'* of the proposed current commutation method.

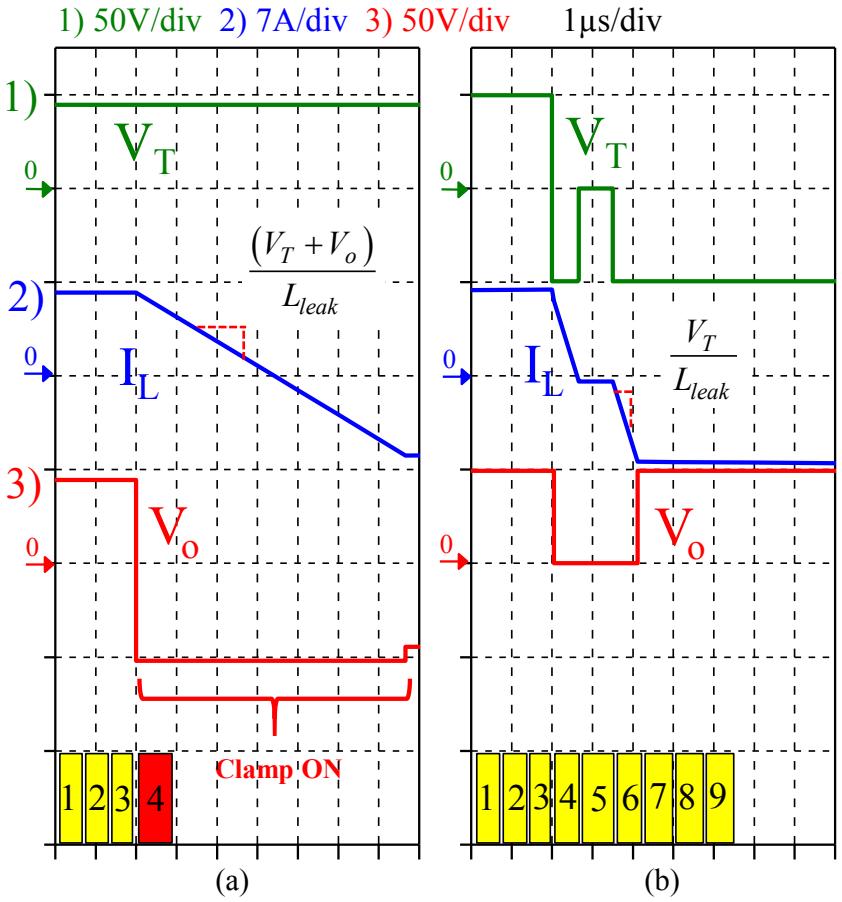


Figure 4.16: Theoretical commutation waveforms for moving from MS_1 MS_1 to MS_2 MS_2 when $V_{in} > 0$, $I_{out} > 0$. (a) With standard 4-step commutation (b) With proposed source based leakage tolerant current commutation method.

Although, the theoretical analysis and the simulation results, presented in Section 4.4.2 and 4.4.3 respectively, suggest that the source based leakage tolerant current commutation method should be applied to the cells of MIMC but an experimental test is necessary to validate the concept and its effectiveness compared to the standard 4-step current commutation method. A detailed experimental validation has been presented in Chapter 5.

4.4.4 Commutation Paths

The current commutation method that has been discussed so far is only for the case where the required change of state is from $MS_1\ MS_1$ to $MS_2\ MS_2$ when $V_{in} > 0$, $I_{out} > 0$. The same strategy can be extended to all the possible changes of the switch states of the converter, by rearranging the sequencing of the commutation procedure similar to commutation paths [106]. The possible modulation or steady states of the single-phase AC/AC converter (single-cell of the MIMC) are shown in Table 4.1.

Table 4.1: Steady states of a single-phase AC/AC converter (single-cell of the MIMC)

Modulation State Code	Transformer Voltage (V_T)	Output Voltage (V_o)
$MS_1\ MS_1$	$= +V_{in}$	$= +V_{in}$
$MS_2\ MS_2$	$= -V_{in}$	$= +V_{in}$
$MS_1\ MS_2$	$= +V_{in}$	$= -V_{in}$
$MS_2\ MS_1$	$= -V_{in}$	$= -V_{in}$
$MS_1\ MS_0$	$= +V_{in}$	$= 0$
$MS_2\ MS_0$	$= -V_{in}$	$= 0$

In order to move between the steady states shown in Table 4.1, the method can be extended. A simplified commutation path diagram is shown in Figure 4.17 in which *'large grey circles'* denote the modulation or steady states, *'small circles'* indicate the temporary commutation states and the arrows represent the commutation paths. The commutation states have been coded with letters where the first letter represents the commutation state (CS) matrix of the input side 4QSH-bridge while the second letter represents that of the output side 4QSH-bridge. Equations (4.20) and (4.21) show the generic commutation matrices for input and output side 4QSH-bridges, respectively.

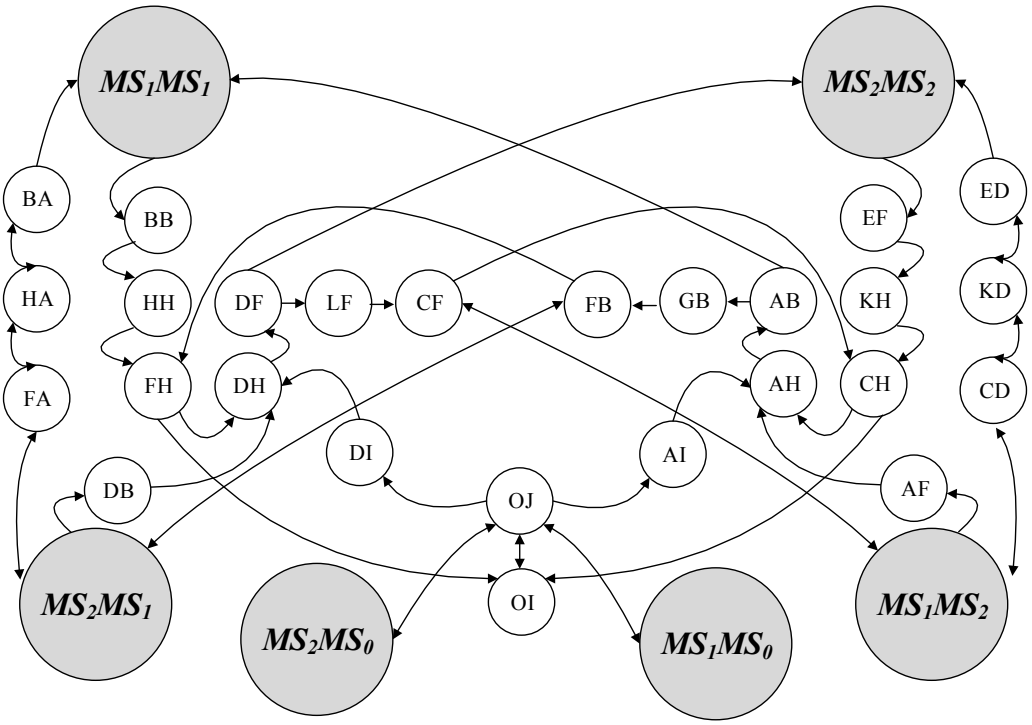
$$CS_i = \begin{bmatrix} S_{0i}S_{1i} & S_{4i}S_{6i} \\ S_{5i}S_{7i} & S_{2i}S_{3i} \end{bmatrix} \tag{4.20}$$

$$CS_o = \begin{bmatrix} S_{0o}S_{1o} & S_{4o}S_{6o} \\ S_{5o}S_{7o} & S_{2o}S_{3o} \end{bmatrix} \tag{4.21}$$

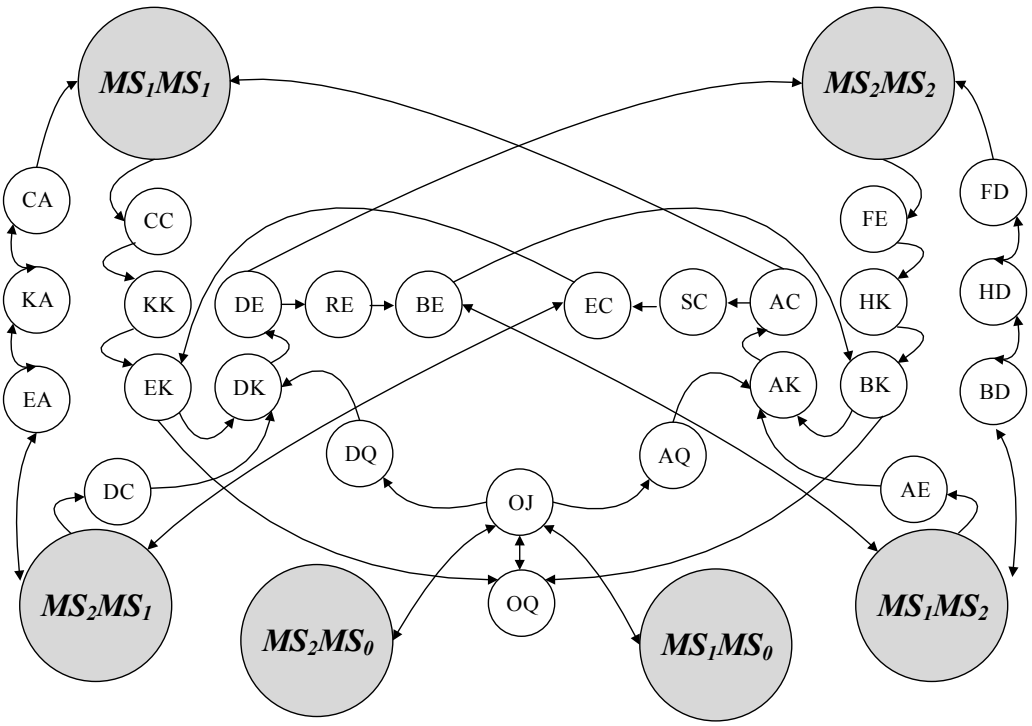
Where the switch numbering 0,..,7 refers to the individual switches in the 4QSH-bridges of cell shown in Figure 4.9. The definition of the CS matrices is given in equation (4.22). Note that in Figure 4.17, the modulation states, in *'large grey circles'*, are represented using form $MS_{Kij}MS_{Koj}$ whereas the commutation states, in *'small circles'*, are represented using form CS_iCS_o.

$$
\begin{aligned}
A &= \begin{bmatrix} 11 & 00 \\ 00 & 11 \end{bmatrix}, B = \begin{bmatrix} 10 & 00 \\ 00 & 10 \end{bmatrix}, C = \begin{bmatrix} 01 & 00 \\ 00 & 01 \end{bmatrix}, D = \begin{bmatrix} 00 & 11 \\ 11 & 00 \end{bmatrix}, \\
E &= \begin{bmatrix} 00 & 10 \\ 10 & 00 \end{bmatrix}, F = \begin{bmatrix} 00 & 01 \\ 01 & 00 \end{bmatrix}, G = \begin{bmatrix} 11 & 01 \\ 01 & 11 \end{bmatrix}, H = \begin{bmatrix} 10 & 01 \\ 01 & 10 \end{bmatrix}, \\
I &= \begin{bmatrix} 00 & 00 \\ 01 & 10 \end{bmatrix}, J = \begin{bmatrix} 00 & 00 \\ 11 & 11 \end{bmatrix}, K = \begin{bmatrix} 01 & 10 \\ 10 & 01 \end{bmatrix}, L = \begin{bmatrix} 01 & 11 \\ 11 & 01 \end{bmatrix}, \\
M &= \begin{bmatrix} 01 & 01 \\ 01 & 01 \end{bmatrix}, N = \begin{bmatrix} 10 & 10 \\ 10 & 10 \end{bmatrix}, O = \begin{bmatrix} 00 & 00 \\ 00 & 00 \end{bmatrix}, Q = \begin{bmatrix} 00 & 00 \\ 10 & 01 \end{bmatrix}, \\
R &= \begin{bmatrix} 10 & 11 \\ 11 & 10 \end{bmatrix}, S = \begin{bmatrix} 11 & 10 \\ 10 & 11 \end{bmatrix}
\end{aligned}
\tag{4.22}
$$

For example, to move from steady state 'MS_1 MS_1' to 'MS_2 MS_1' when $V_{in} > 0$, $I_{out} > 0$, the cell will go through three commutation states 'BA', 'HA' and 'FA' (Figure 4.17a). With a similar approach and using the definitions of the CS matrices shown in (4.22), three additional diagrams can also be derived, corresponding to the commutation paths for ($V_{in} > 0$, $I_{out} < 0$), ($V_{in} < 0$, $I_{out} > 0$) and ($V_{in} < 0$, $I_{out} < 0$) which are shown in Figures 4.17b, 4.17c and 4.17d, respectively. Note that the diagrams shown in Figure 4.17 have been found after arrangement of commutation states to keep the same pattern of paths in all cases of commutation in order to achieve a meaningful representation of commutation paths.

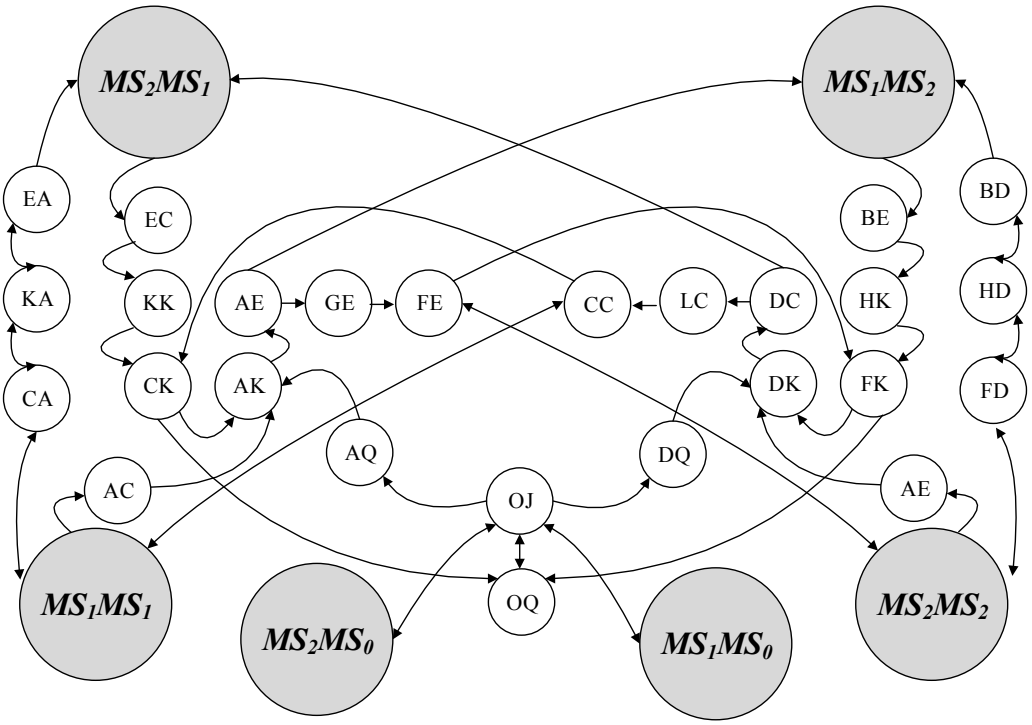


(a) Commutation paths when $V_{in} > 0$, $I_{out} > 0$.

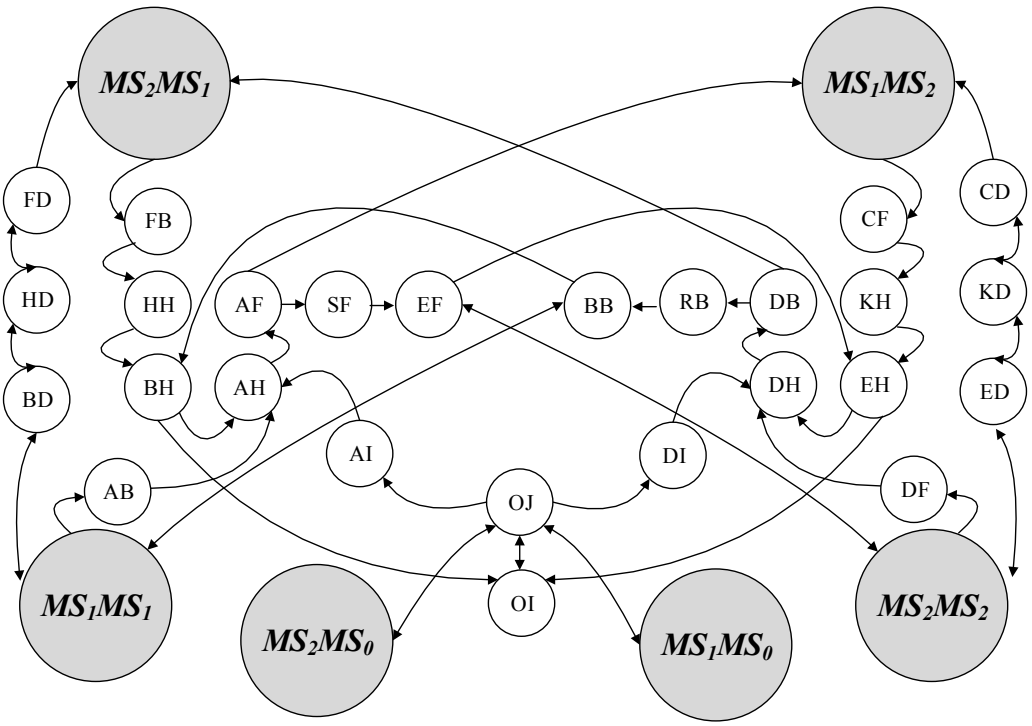


(b) Commutation paths when $V_{in} < 0$, $I_{out} < 0$.

Figure 4.17: Generalised commutation paths for single-phase AC/AC converter (single-cell of the MIMC) to move between the steady states of Table 4.1



(c) Commutation paths when $V_{in} > 0$, $I_{out} < 0$.



(d) Commutation paths when $V_{in} < 0$, $I_{out} > 0$.

Figure 4.17: (Cont.) Generalised commutation paths for single-phase AC/AC converter (single-cell of the MIMC) to move between the steady states of Table 4.1

4.5 Conclusions

The commutation method can be as simple as a *dead-time* between the in-coming and the out-going switches of a 2QSH-bridge which has a current source at AC side and a voltage source at DC side. This is because in 2QSH-bridge, the current source always has a path available through the free-wheeling diodes and there is no possibility of *current commutation failure*. However, in case of 4QSH-bridge there is no free-wheeling paths available to current source and thus a multi-step commutation approach, the 4-step current commutation method is necessary to ensure the availability of a current path. To achieve this, either the direction of the current source or polarity of the voltage source is measured and the switches of 4QSH-bridge are switched ON/OFF in a particular sequence accordingly. When standard 4-step current commutation method is applied to a single cell of the MIMC or a single-phase AC/AC converter then each of the 4QSH-bridge undergoes independent commutation which in the presence of non-negligible leakage inductance of transformer causes over-voltages across the switching devices, thus a dissipative clamp circuit becomes unavoidable.

In order to avoid the commutation related triggering of the clamp circuit, a source based leakage tolerant current commutation method, which does not require additional components, has been proposed for the basic building block of the MIMC, a single-phase AC/AC converter. In this type of commutation the leakage current is decoupled first and then modified by imposing the required polarity of the voltage source using input side 4QSH-bridge.

Chapter 5

Experimental Validation of the Commutation Method

5.1 Experimental Setup

To test the proposed source based leakage tolerant current commutation method a proof of concept prototype single-phase AC/AC converter (a single cell of the MIMC) was built. The experimental architecture is shown in Figure 5.1.

The single-cell can be modulated in various ways [90, 107], but even a simple case of modulation can be considered to validate the proposed current commutation method. A simple case of modulation can be when the input side 4QSH-bridge modulates the low frequency input voltage at 50Hz to a 50% duty cycle MF (10kHz) waveform. This 50% duty cycle waveform at the MF transformer can then be unfolded or demodulated back to a low frequency of 50Hz using the output side 4QSH-bridge. From the modulator's perspective, this requires the single-cell to move between two steady states, MS_1MS_1 and MS_2MS_2, which is the same case as discussed in Section 4.4.2 of Chapter 4. The command which will cause the converter to move between the states, MS_1MS_1 and MS_2MS_2, is generated by a DSP, as shown in Figure 5.1.

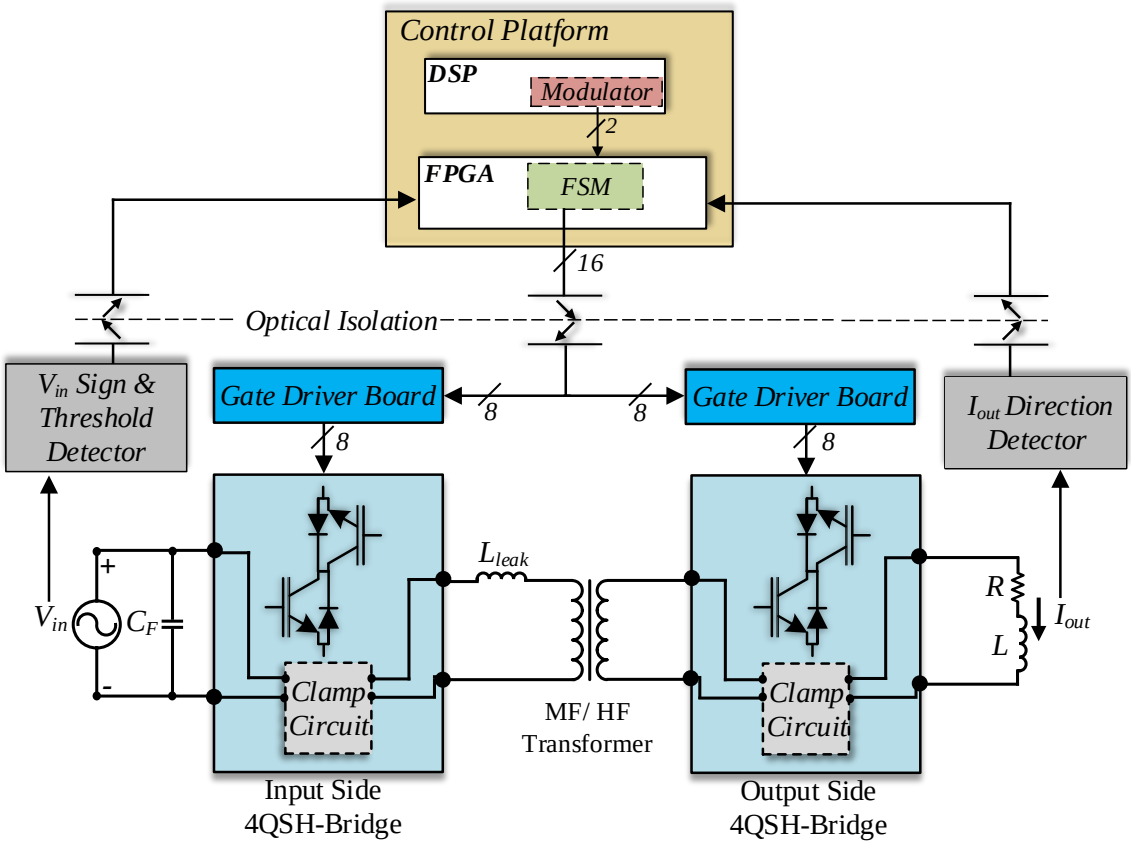


Figure 5.1: Experimental setup diagram for the validation of proposed current commutation method on a single-cell of the MIMC

The DSP will output 00 if the required steady-state is MS_1MS_1 and 11 in case of MS_2MS_2. These modulation signals are then fed to the FPGA where a Finite-State Machine (FSM) [108] performs the current commutation based on the sign of input voltage and the direction of output current and generates 16 independent control signals. Note the current commutation strategy is implemented in the FPGA due to its parallel-processing capability [109,110] which allows the implementation of current commutation steps. Therefore the information of sign and direction of input voltage and output current, respectively, are passed directly to the FSM in the FPGA. The communication between the control platform and the power boards is done optically. The optically-transmitted control signals from FPGA are then applied to the switches on the input and output side 4QSH-bridges by the respective gate driver boards.

To limit the disturbances to the input voltage source, the input side of the 4QSH-bridge is equipped with a filter capacitor. To model the current source/sink a series RL load has been considered on the output side with an assumption that $L >> L_{leak}$. To be able to test the standard 4-step current commutation safely without dissipating the energy of leakage inductance in the switches and to protect the switches against other accidental open-circuit current commutation failures, both bridges of the cell are equipped with dissipative clamp circuits, as shown in Figure 5.1. The configuration of the clamp circuit is shown in Figure 5.2.

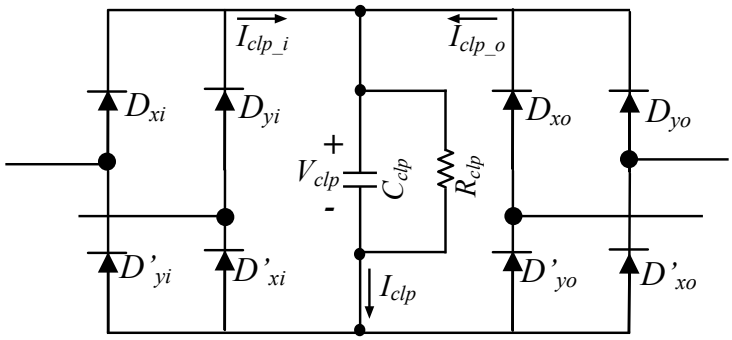


Figure 5.2: Typical rectifier-based-clamp circuit for protection against the current commutation failures

5.1.1 Control Platform

A custom DSP/FPGA based control platform, which is composed of Texas Instrument TMS320C6713DSK (DSP) and Microsemi ProASIC 3 Family-A3P400 (FPGA), has been used to generate 16 independent gate signals which are transmitted to gate board using HFBR-1521Z optical transmitters. The number of optical transmitters on the custom made FPGA board was limited to a maximum of 8. Therefore, an extension board has been used to increase the number of optical outputs to 16. The information of polarity of the input voltage V_{in}, it's threshold V_{in}^{MIN} and I_{out} direction is received at the HFBR-2521Z optical receivers from the sensing board via 3 optical fibre cables. The circuit used for the HFBR-1521Z optical transmitters is shown in Figure 5.8. For details of the circuitry and components used, refer to Appendix A.

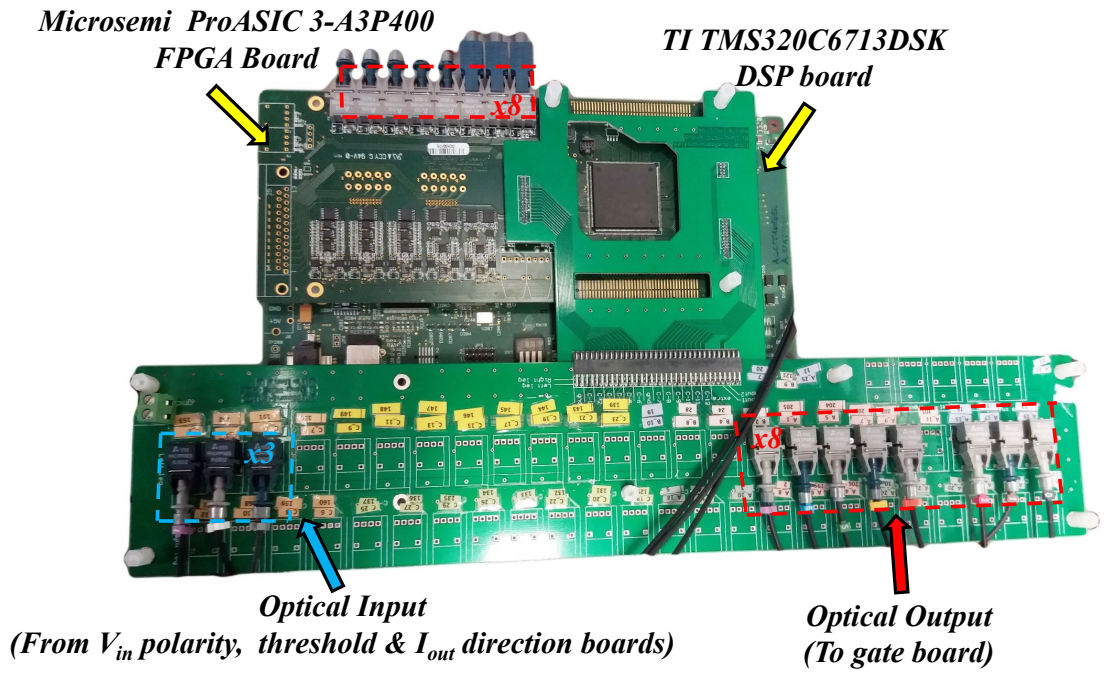


Figure 5.3: Photo of the DSP/FPGA based control platform with 16 optical transmitters and 3 optical receivers

5.1.2 4QSH-bridge and Clamp Circuit

The design of input and output side 4QSH-bridges is identical in terms of PCB layout, except that the input side 4QSH-bridge has a filter capacitor. Each 4QSH-bridge has a individual PCB which has been designed with the aim to develop a flexible and scalable test rig to validate various four-quadrant based topologies. For brevity, only the input side 4QSH-bridge is shown in Figure 5.4, which contains four SEMIKRON SKM150GM12T4G IGBT power modules. Each of the IGBT power modules, shown in Figure 5.5, is a four-quadrant switch formed by a series connection of two IGBTs in a common-emitter configuration.

A parallel connection of two $15\mu F$ snubber film capacitors and four $1\mu F$ ceramic capacitors form the input side AC filter capacitor. The selection and design of the input filter was not optimised for single-phase AC/AC converter, but estimated based on the standard practice used in Direct Matrix Converters because the rig was developed with an aim to test different Matrix Converter based topologies.

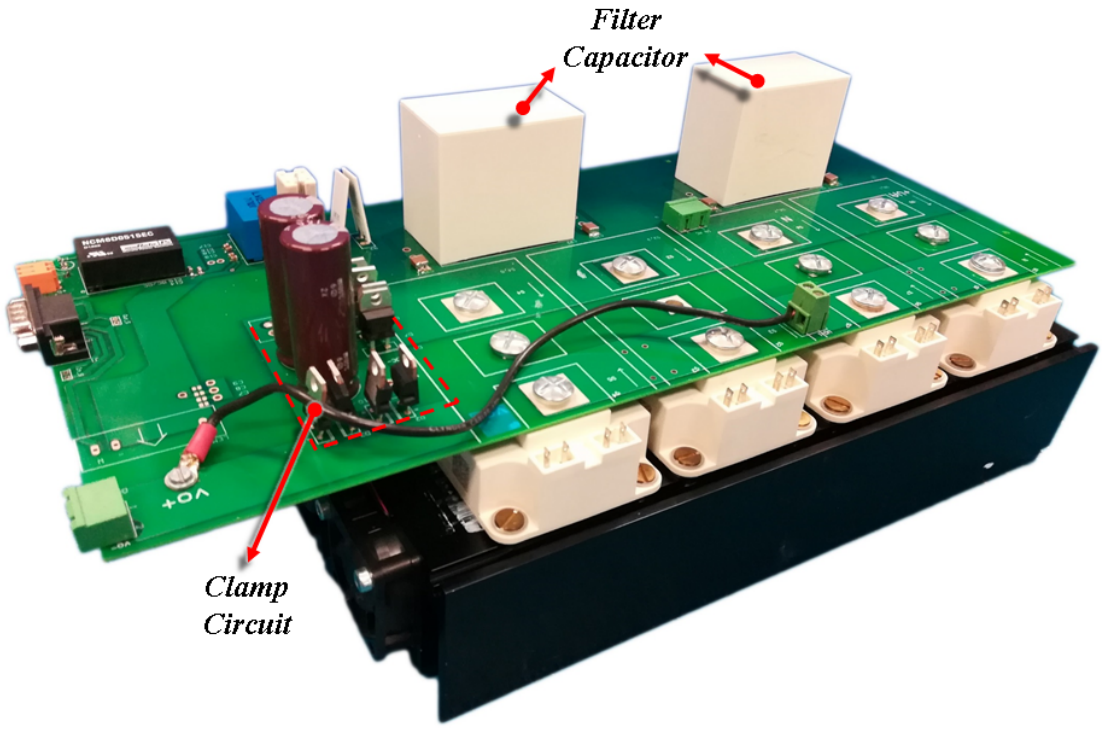


Figure 5.4: Photo of the input side 4QSH-bridge based on SEMIKRON IGBT modules (SKM150GM12T4G)

The on-board clamp circuit, shown in Figure 5.4, is based on ultra fast recovery diode bridges, the configuration is shown in Figure 5.2. The clamp circuit will not be in operation during the normal operation of the converter and clamp voltage V_{clp} will be equal to the peak of the input voltage, but as soon as an open-circuit fault appears, the ultra fast recovery diodes in the clamp circuit will provide path a for the fault current [75] causing the clamp capacitor C_{clp} to charge. The time it will take to charge the clamp capacitor C_{clp} will be defined by the value of the resistor R_{clp} that is connected parallel to it.

The value of the clamp capacitor C_{clp} can be determined by the maximum amount of energy that will flow into during the open-circuit fault without increasing its voltage V_{clp} beyond the rated the voltage of IGBTs. This maximum energy will be the sum of energy stored in the leakage inductance L_{leak} and output filter inductor L. Therefore, value of the clamp capacitor C_{clp} can be calculated by using equation (5.1).



Figure 5.5: Photo of the common-emitter configuration based four-quadrant switch - SEMIKRON SKM150GM12T4G

$$C_{clp} = \frac{(L_{leak} + L)\left|I_{out}^{MAX}\right|^2}{\left(V_{clp}^{MAX}\right)^2 - \left|V_{in}^{MAX}\right|^2} \tag{5.1}$$

Note that in equation (5.1), I_{out}^{MAX} and V_{in}^{MAX} are the peak of values of the output current I_{out} and the input voltage V_{in}, respectively. V_{clp}^{MAX} represents final voltage that will appear at the clamp capacitor after it is fully charged by taking up the energies of L and L_{leak}. V_{igbt}^{MAX} denotes the rated voltage of the IGBT, V_{clp}^{MAX} should be kept below the rated voltage of the IGBT and therefore, must follow the condition $V_{clp}^{MAX} < V_{IGBT}^{MAX}$ to protect the IGBTs from over-voltage.

Although the SEMIKRON SKM150GM12T4G IGBT power modules are rated at 1200V, 150A, the peak power that a 4QSH-bridge can tolerate is limited to 11.2kVA (450V, 25A). This limit was chosen mainly due to cost restrictions and to keep the prototype to a laboratory scale. The current rating was limited to 25A because of the two-layered PCB design and the voltage rating was limited to 450VAC due to the rating of the clamp capacitors employed.
The components used for the PCB of the 4QSH-bridge can be found in the detailed schematic shown in Figure A.2 of Appendix A.

5.1.3 Gate Driver Board

The gate driver board receives the optically transmitted signals from the control platform and converts them to electrical signals which, after signal conditioning, are fed to the gate driver circuitry, as shown in Figure 5.6. The gate driver circuity contains HCPL-315J drivers and current enhancing IXDN-609. Note that IXDN-609 has been added to increase the current source/sink capability of HCPL-315J from +/- 0.5A to +/- 9A. The driver circuitry is fed with isolated supplies which include $+15V_{CC}$ for turn-ON of the IGBT and $-15V_{SS}$ for turn-OFF of the IGBT. A negative voltage of -15V ensures the turn-OFF of IGBT and is considered good practise [111]. This driver circuit design is repeated eight times for driving the eight switches of a 4QSH-bridge and the PCB is shown in Figure 5.7.

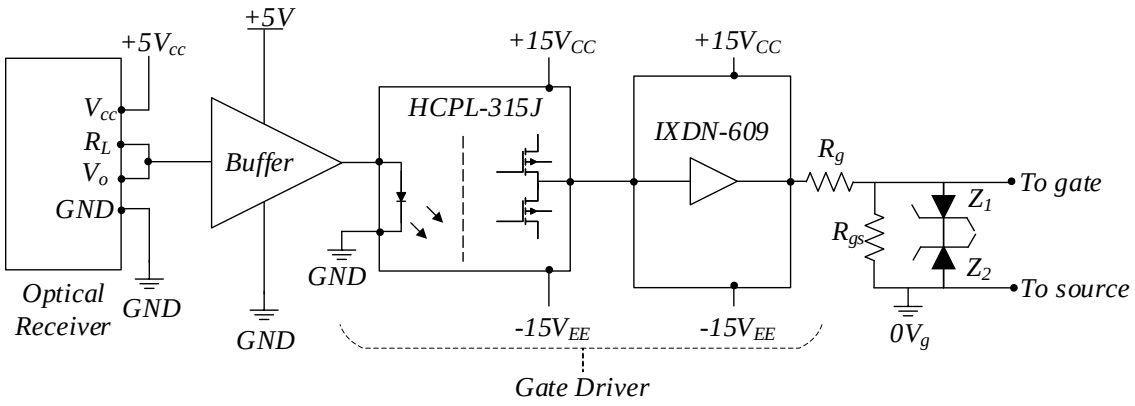


Figure 5.6: Block diagram of the isolated gate driver circuit

For the layout of the gate driver board, the gate to source current path must be minimised and planes should be used instead of tracks. This is done to reduce the stray inductance which will otherwise cause overshoots in the gate-emitter voltage [112]. Although the design of the board, shown in Figure 5.7, has been done following good practise [112, 113] it is impossible to completely eliminate stray inductances. Therefore, to damp any oscillations arising due to stray inductances, a gate resistor R_g is introduced, as shown in Figure 5.6. The zener diodes are added to protect the gate of the IGBT against any unwanted over voltages.

Note that the power supply for the driver circuitry of each 4 quadrant-switch is completely isolated using DC/DC converters. The complete circuit configuration for the driver board can be found in the schematic shown in Figure A.1 of Appendix A.

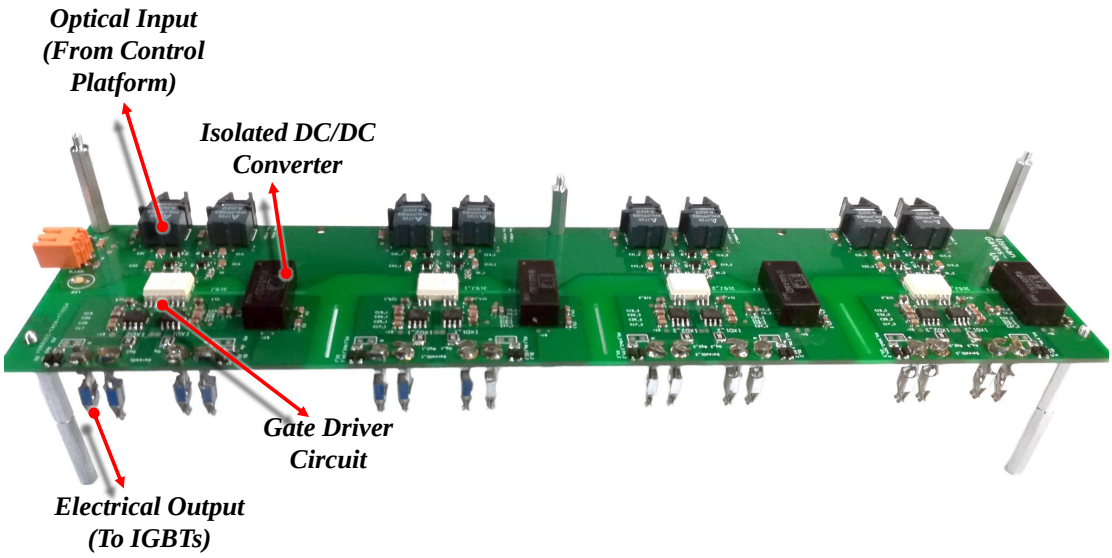


Figure 5.7: Photo of the isolated supply gate driver board

5.1.4 Voltage Polarity and Threshold Detection

The polarity of the input voltage V_{in} is required to initiate the current commutation process and this information is read by the FSM in the FPGA at the start of the current commutation process. It is assumed that the polarity remains the same during the commutation process as the commutation time is very small as compared to the fundamental period of the low-frequency input voltage. Therefore, the polarity must be correctly determined as the whole current commutation process depends on it and a wrong information about polarity will lead to a short circuit of the voltage source causing an over current which can then permanently damage the semiconductor devices. Note that without this assumption, a very high-bandwidth sampling will be required from the control platform which can over burden the FSM in FPGA leading to reduced reliability.

To extract the polarity information, a simple voltage polarity detector circuit is used as shown in Figure 5.8 which uses a single diode to implement a half-wave rectifier. The rectified half wave V_{rec_h} is then then mapped to V'_{rec_h} using a voltage divider such that when $V_{rec_h} = V_{in}^{MAX}$ then $V'_{rec_h} = 5V$. This ensures that the input voltage of the comparator V'_{rec_h} never exceeds its maximum allowed input voltage. It is important to mention that as the mapped range is small, the comparator must offer a low offset voltage and must switch even at minimal voltage differences between its inputs. If this condition is satisfied the comparator will output *high* when $V_{in} > 0$ and *low* in case when $V_{in} < 0$. A small bias is given to the inverting pin using R_{bias} to avoid a zero comparison condition. The output of the comparator is then optically transmitted and is received by the FPGA board where this information will be used to initiate the current commutation process.

Note that the voltage supply V_S of the optical transmitter circuit is provided through a separate isolated DC/DC converter to increase the reliability by keeping the control and power circuitry apart.

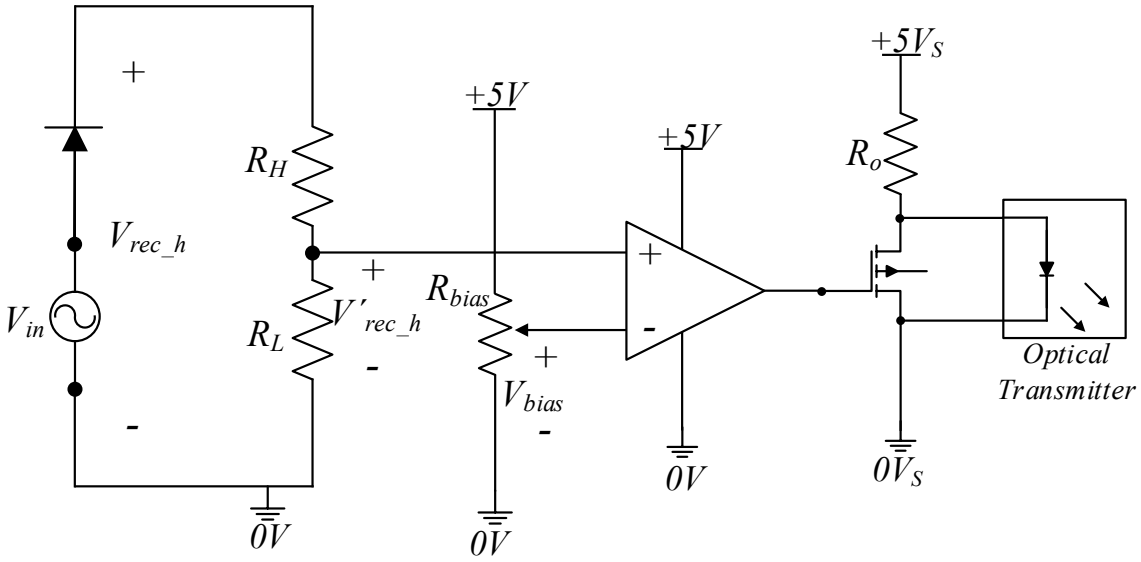


Figure 5.8: Input voltage V_{in} polarity detector circuit

Another circuit, in addition to the voltage polarity detector circuit, is required to determine if the magnitude of the input voltage V_{in} is enough to drive the leakage current. A minimum input voltage magnitude $|V_{in}^{MIN}|$ can be set below which the

current commutation process will not be initiated. The threshold detector circuit is shown in Figure 5.9 where a full wave rectifier is generating voltage V_{rec} which is mapped to V'_{rec}, just as in the polarity detector circuit, and is compared with a threshold voltage V_{th}. Note that V_{th} can be adjusted according to the worse case conditions by varying potentiometer R_{th}. The comparator output, which is *high* for the case when $|V_{in}| > |V_{in}^{MIN}|$, is then optically transmitted to the FPGA. The circuit configuration and the components used in the voltage polarity and threshold detector board can be found in the schematic shown in Figure A.3 of Appendix A.

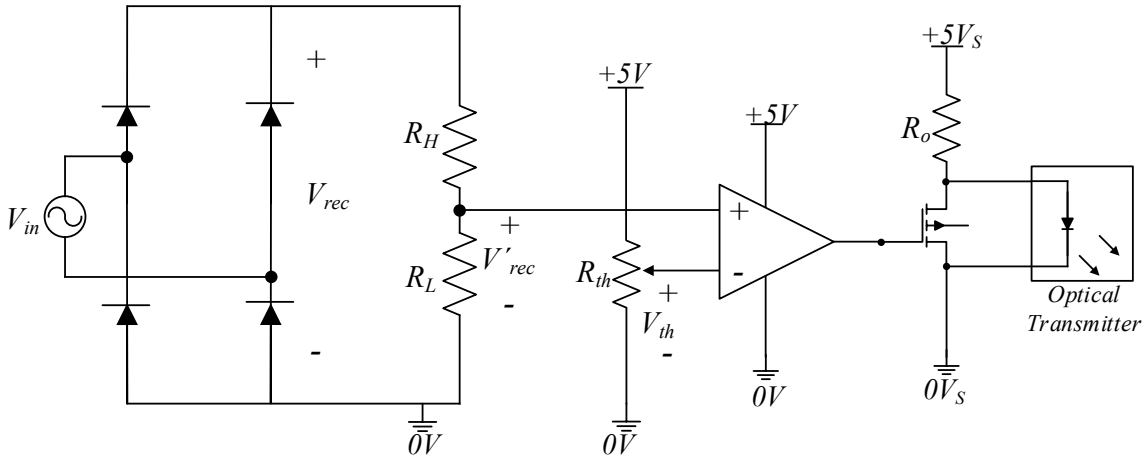


Figure 5.9: Input voltage V_{in} threshold detector circuit

5.1.5 Current Direction Detector Circuit

Two diodes connected in anti-parallel configuration can be used to determine direction of the output current I_{out}. Consider that the output current I_{out} enters into the circuit in the direction as shown in Figure 5.10 then if $I_{out} > 0$ then the forward voltage drop V_F of the conducting diode will cause the comparator to output *high* as $V_{dir} = V_F$. However, in case when $I_{out} < 0$, the comparator will output *low* as $V_{dir} = -V_F$. Finally, the output of the comparator is then fed by the optical transmitter circuit to the FPGA where this information will be used to initiate the current commutation process.

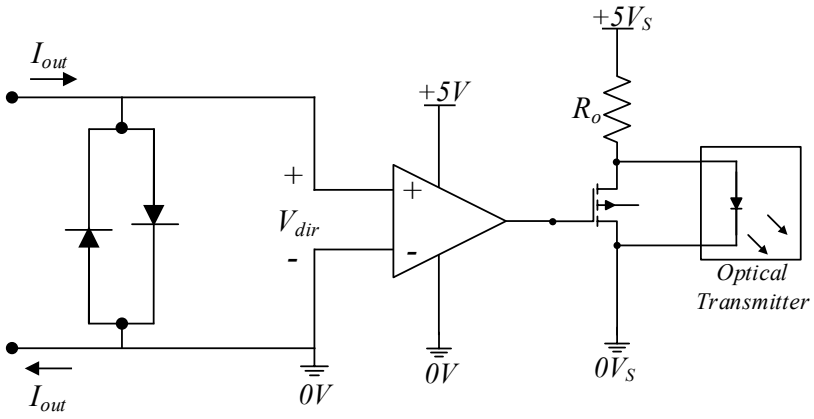


Figure 5.10: Output current I_{out} direction detector circuit

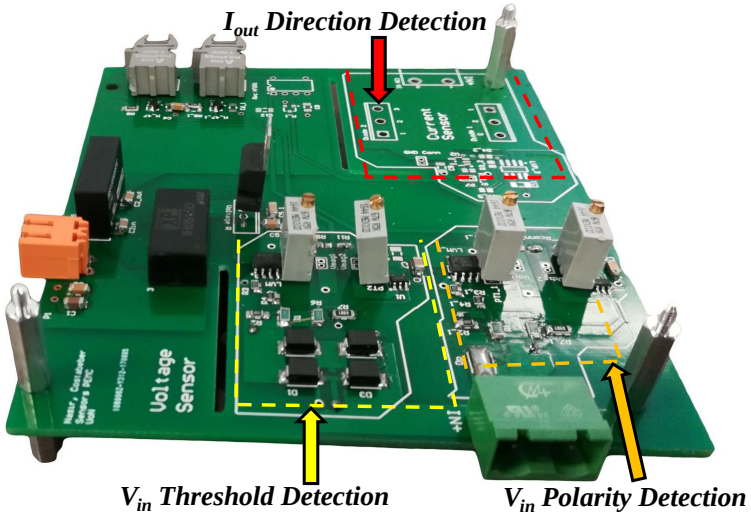


Figure 5.11: Photo of the sensing circuit - V_{in} polarity and threshold detector circuit

Note that, similar to the voltage polarity, the same assumption has been made that the fundamental period of the output current I_{out} is much larger than the commutation time thus requiring the information of the direction of I_{out} at the initiation of the current commutation process.

The layouts of voltage polarity, voltage threshold and current direction detector circuits have been done on the single PCB to reduce manufacturing costs and the electronic components were soldered according the desired sensing circuitry. For example, the PCB board shown in Figure 5.11 was soldered to achieve voltage polarity and threshold detection. The complete circuit and the components used in the current direction board can be found in the schematic shown in Figure A.3 of Appendix A.

5.1.6 The Medium Frequency (MF) Transformer

The conventional approach to the transformer design [114] calculates the required core area by considering that the voltage applied to the transformer is either a sinusoidal waveform (waveform factor $K = 4.44$) or a square waveform (waveform factor $K = 4$) at a single frequency. However, the transformer voltage V_T in a single-cell of the MIMC is actually a product of sinusoidal and square wave and its Fourier spectrum will not have a single component, thus the conventional design approach can not be applied directly. Designing the MF transformer at the switching frequency f_{sw}, by neglecting all the harmonic components, will cause the transformer to saturate. Therefore, the complete Fourier spectrum of the transformer voltage V_T must be analysed and considered for the design of the MF transformer.

To analyse the Fourier spectrum of the transformer voltage V_T, the function of the input side 4QSH-bridge must be studied. As mentioned in Section 5.1, the single-cell moves between steady states MS_1MS_1 and MS_2MS_2 and a 50% duty cycle wave is generated at the transformer. By moving between these steady-states, the input side 4QSH-bridge is actually implementing a periodic square wave function $s(t)$ which is given in (5.2) and shown in Figure 5.12.

$$s(t) = \begin{cases} 1 & for\ nT_s < t < (nT_s\ +\ T_s/2) \\ -1 & for\ (nT_s\ +\ T_s/2) < t < (n+1)\,T_s \end{cases} \qquad n = 0, 1, 2.. \tag{5.2}$$

The periodic square wave function $s(t)$ can be represented by Fourier series as stated in (5.3). Since the function $s(t)$ does not have a DC component and is an *odd* function which follows $s(-t) = -s(t)$ therefore the coefficients a_0 and a_m will be zero and only b_m exists which can be determined by (5.4). Note that b_m is zero for all the even values of m, thus the Fourier series can be simply expressed by (5.5). A generalised expression for the input voltage V_{in} is given in (5.6) where $K = A, B, C$ for a three-phase system.

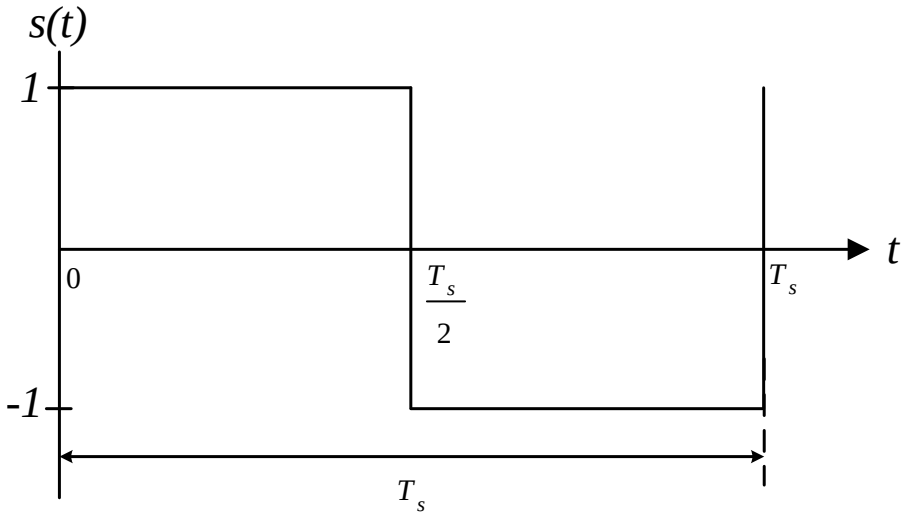


Figure 5.12: Illustration of function $s(t)$ implemented by input side 4QSH-bridge

$$s(t) = a_0 + \sum_{m=1}^{\infty} \left[a_m \cos\left(m\omega_s t\right) + b_m \sin(m\omega_s t)\right] \tag{5.3}$$

$$b_m = \frac{4}{T_s} \int_0^{\frac{T_s}{2}} \sin(m\omega_s t)dt = \frac{2}{m\pi}\left[1^m - (-1)^m\right] \tag{5.4}$$

$$s(t) = \frac{4}{\pi} \sum_{m=1,3,5,..}^{\infty} \left[\frac{1}{m} \sin(m\omega_s t)\right] \tag{5.5}$$

$$V_{in}(t) = V \sin(\omega_i t + \varphi_K) \tag{5.6}$$

The time-domain expression for the transformer voltage V_{TK} can be obtained by the product of the functions (5.2)-(5.6) and has been simplified to equation (5.7). This voltage V_{TK} when appears across the transformer will cause a change in the flux Φ_{TK} which, according to Faraday's Law, as given in (5.8) and re-written in (5.9).

$$\begin{aligned} V_{TK}\left(t\right) &= V_{in}(t)s(t) \\ &= \frac{2V}{\pi} \sum_{m=1,3,5,...}^{\infty} \frac{1}{m}\left[\cos\left(m\omega_s t - \omega_i t - \varphi_K\right) - \cos\left(m\omega_s t + \omega_i t + \varphi_K\right)\right] \end{aligned} \tag{5.7}$$

$$V_{TK} = -N\frac{d\Phi_{TK}}{dt} \tag{5.8}$$

$$\Phi_{TK}(t) = -\frac{1}{N}\int V_{TK}(t)\ dt \tag{5.9}$$

Substituting V_{TK} from equation (5.7) to equation (5.9) will result in:

$$\Phi_{TK}(t) = -\frac{2V}{\pi N}\sum_{m=1,3,5,\ldots}^{\infty}\int \frac{1}{m}\left[\cos\left(m\omega_s t - \omega_i t - \varphi_K\right) - \cos\left(m\omega_s t + \omega_i t + \varphi_K\right)\right] dt \tag{5.10}$$

$$\Phi_{TK}(t) = -\frac{2V}{\pi N}\sum_{m=1,3,5,\ldots}^{\infty}\frac{1}{m}\left[\frac{\sin\left(m\omega_s t - \omega_i t - \varphi_K\right)}{m\omega_s - \omega_i} - \frac{\sin\left(m\omega_s t + \omega_i t + \varphi_K\right)}{m\omega_s + \omega_i}\right] \tag{5.11}$$

Since, $\omega_i T_i = 2\pi$ and $\sin(t + 2\pi) = \sin(t)$ then equation (5.11) can be re-written as;

$$\Phi_{TK}(t) = -\frac{2V}{\pi N}\sum_{m=1,3,5,\ldots}^{\infty}\frac{1}{m}\left[\frac{(m\omega_s + \omega_i)\sin\left(m\omega_s t - \omega_i t - \varphi_K\right)}{m^2{\omega_s}^2 - {\omega_i}^2} - \frac{(m\omega_s - \omega_i)\sin\left(m\omega_s t + \omega_i t + \varphi_K\right)}{m^2{\omega_s}^2 - {\omega_i}^2}\right] \tag{5.12}$$

$$\Phi_{TK}(t) = -\frac{2V}{\pi N}\sum_{m=1,3,5,\ldots}^{\infty}\left[\frac{m\omega_s\left[\sin\left(m\omega_s t - \omega_i t - \varphi_K\right) - \sin\left(m\omega_s t + \omega_i t + \varphi_K\right)\right]}{m^3{\omega_s}^2 - m{\omega_i}^2} + \frac{\omega_i\left[\sin\left(m\omega_s t - \omega_i t - \varphi_K\right) + \sin\left(m\omega_s t + \omega_i t + \varphi_K\right)\right]}{m^3{\omega_s}^2 - m{\omega_i}^2}\right] \tag{5.13}$$

$$\Phi_{TK}(t) = -\frac{4V}{\pi N}\sum_{m=1,3,5,\ldots}^{\infty}\left[-m\omega_s\frac{\cos(m\omega_s t)\sin(\omega_i t + \varphi_K)}{m^3{\omega_s}^2 - m{\omega_i}^2} + \omega_i\frac{\sin(m\omega_s t)\cos(\omega_i t + \varphi_K)}{m^3{\omega_s}^2 - m{\omega_i}^2}\right] \tag{5.14}$$

Note that equation (5.14) is the time-domain expression of the flux $\Phi_{TK}(t)$ but for the design of MF transformer, the expression (5.14) should be solved for the maximum value of flux $|\Phi_{TK}(t)|^{MAX}$ because the MF transformer must be able to accommodate the maximum flux [3] generated by the voltage V_{TK} (5.7).

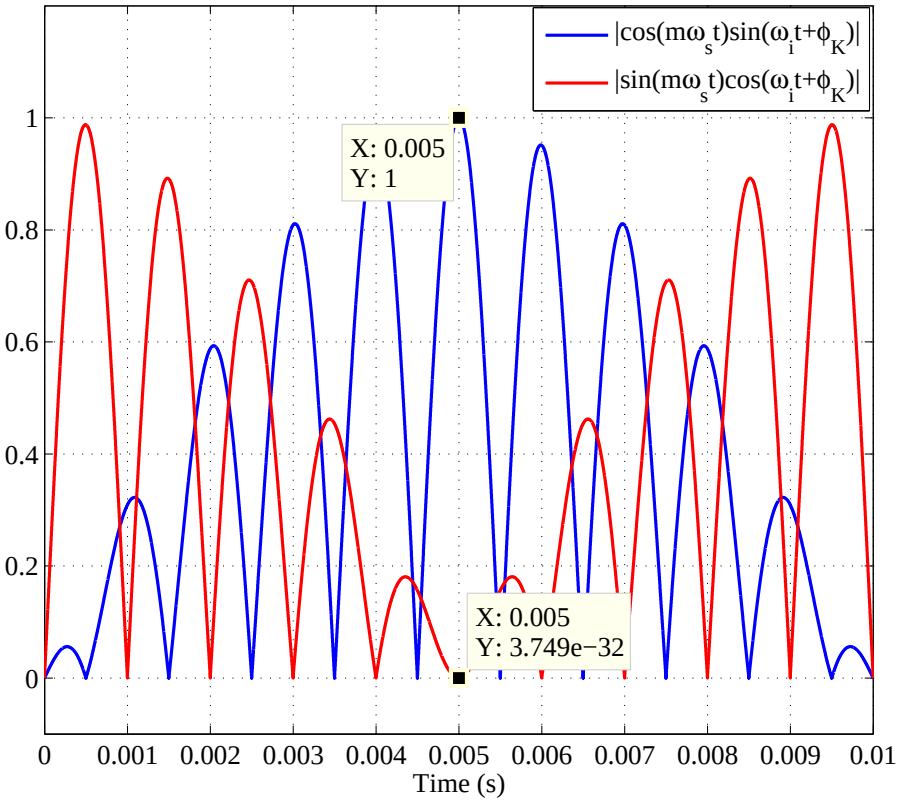


Figure 5.13: Time-domain plot of $|\cos(m\omega_s t)\sin(\omega_i t + \varphi_K)|$ and $|\sin(m\omega_s t)\cos(\omega_i t + \varphi_K)|$ - with $m = 1$, $\varphi_K = 0$, $f_i = 50$Hz, $f_{sw} = 500$Hz- showing when one term is at its peak value of unity, the other term is zero

The two terms in (5.14), $|\cos(m\omega_s t)\sin(\omega_i t + \varphi_K)|$ and $|\sin(m\omega_s t)\cos(\omega_i t + \varphi_K)|$, have the coefficients $m\omega_s$ and ω_i, respectively. The maximum value of either of the mentioned terms can be unity. However, when one term is maximum or unity the other term will be minimum or zero. To clearly show this, the time-domain plot of the two terms for $m = 1$, $\varphi_K = 0$, $f_i = 50$Hz, $f_{sw} = 500$Hz is shown in Figure 5.13. For example, it can seen from Figure 5.13 that at time instant $t = 5ms$, the term $|\cos(m\omega_s t)\sin(\omega_i t + \varphi_K)|^{MAX} = 1$, whereas the other term is zero, $|\sin(m\omega_s t)\cos(\omega_i t + \varphi_K)|^{MIN} = 0$, therefore equation (5.14) can be written as shown in (5.15).

$$|\Phi_{TK}|^{MAX} = \frac{4V}{\pi N} \sum_{m=1,3,5,\ldots}^{\infty} \left[m\omega_s \frac{|\cos(m\omega_s t)\sin(\omega_i t + \varphi_K)|^{MAX} \rightarrow 1}{m^3{\omega_s}^2 - m{\omega_i}^2} + \omega_i \frac{|\sin(m\omega_s t)\cos(\omega_i t + \varphi_K)|^{MIN} \rightarrow 0}{m^3{\omega_s}^2 - m{\omega_i}^2} \right] \tag{5.15}$$

The switching frequency f_{sw} is within a range of 0.5kHz to 20kHz for a typical MF transformer [115]. Therefore, the switching frequency ω_s is much larger than the fundamental frequency ω_s, $\omega_s >> \omega_i$ then the absolute maximum value of the flux $|\Phi_{TK}(t)|^{MAX}$ can then be written as:

$$|\Phi_{TK}|^{MAX} = \frac{4V\omega_s}{\pi N} \sum_{m=1,3,5,\ldots}^{\infty} \frac{1}{m^2{\omega_s}^2 - {\omega_i}^2} \tag{5.16}$$

The minimum core area ${A_c}^{MIN}$ required to accommodate maximum flux $|\Phi_{TK}(t)|^{MAX}$ can be calculated by (5.18) which has been obtained by substitution of $|\Phi_{TK}(t)|^{MAX}$ from equation (5.16) into equation (5.17). The core area A_c of the transformer must be kept above the minimum core area ${A_c}^{MIN}$ to avoid saturation of transformer due to un-expected delays in switching e.g. gate driver delay etc. This must follow the constraint $A_c > {A_c}^{MIN}$. With the parameters reported in 5.1, the minimum core area ${A_c}^{MIN}$ was found to be ${A_c}^{MIN} = 9cm^2$ but a core area of $A_c = 11cm^2$ was selected as it is was the nearest available core size from the manufacturer. A photo of the MF transformer is shown in Figure 5.14.

$${A_c}^{MIN} = \frac{|\Phi_{TK}|^{MAX}}{B^{MAX}} \tag{5.17}$$

$${A_c}^{MIN} = \frac{4V\omega_s}{\pi N B^{MAX}} \sum_{m=0}^{\infty} \frac{1}{(2m+1)^2{\omega_s}^2 - {\omega_i}^2} \qquad \left[m^2\right] \tag{5.18}$$

Table 5.1: Parameters of the MF Transformer

Parameter	Symbol	Value
Core material and shape		2xAMCC125 C-cores Amorphous alloy 2605SA1
Leakage Inductance	L_{leak}	$4\mu H$
Magnetising Inductance	L_m	$2.3mH$
Operating Frequency	f_{sw}	10kHz
Turns Ratio	N_1/N_2	1
Number of Turns	N	16
Current(RMS) at f_{sw}	I_{rms}	20
Voltage(RMS) at f_{sw}	V_{rms}	400
Power Rating	VA	$8kVA$
Core Area	A_c	$11cm^2$

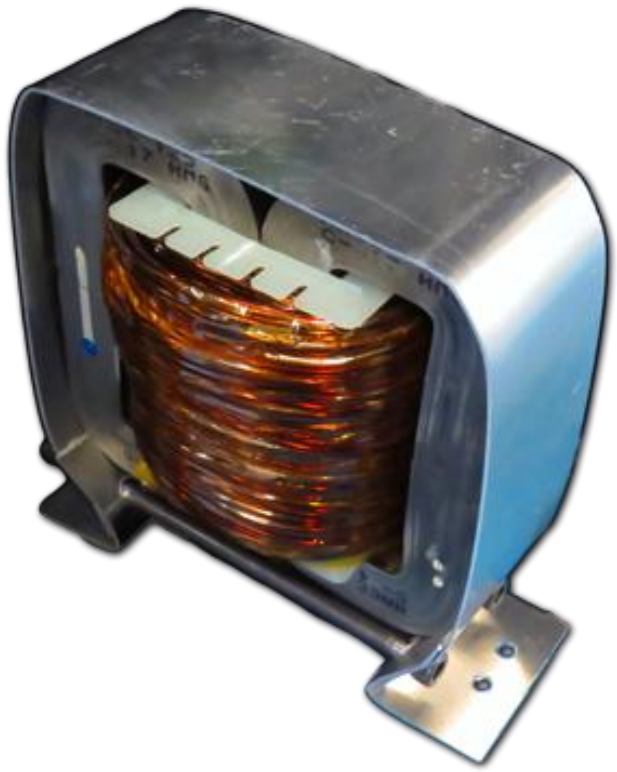


Figure 5.14: Photo of the MF transformer

5.1.7 Experimental Rig and Prototype

A laboratory scale prototype of the MIMC's cell (single-phase to single-phase isolated AC/AC converter) was developed by connecting the individual components described in the previous subsections is shown in Figure 5.1. The experimental rig developed is shown in Figure 5.15 and the parameters are given in Table 5.2.

Note that the components of the experimental rig have not been optimised to show the efficiency of the single-phase isolated AC/AC converter, but to demonstrate the concept of the proposed current commutation method and to compare it with the standard 4-step current commutation method.

Table 5.2: Parameters of the experimental prototype

Parameter	Symbol	Value
Input Voltage Amplitude	V_{in}	100(RMS)
Input Frequency	f_i	50Hz
Output Frequency	f_o	50Hz
Load Resistance	R	7.8Ω
Load Inductance	L	$18mH$
Input Filter Capacitance	C_F	$30\mu F$
Clamp Capacitor	C_{clp}	$300\mu F$
Clamp Resistor	R_{clp}	2.2kΩ

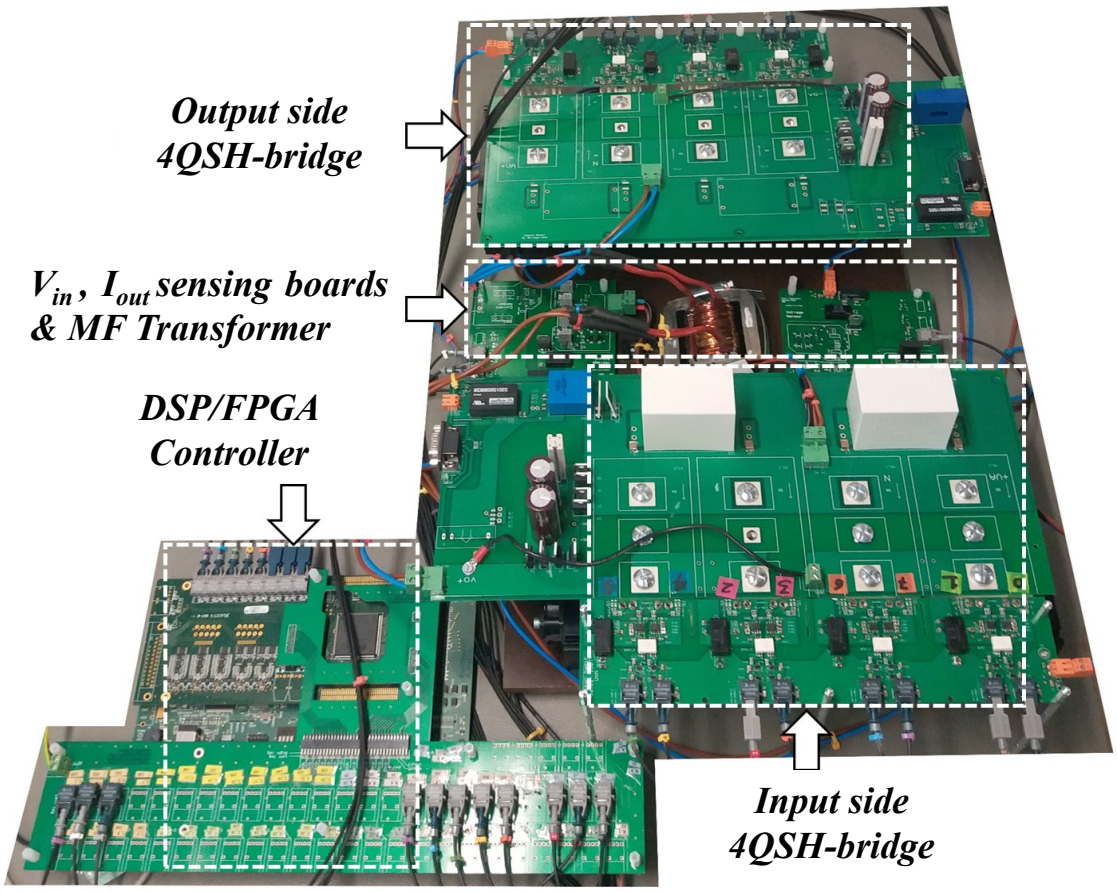


Figure 5.15: Photo of the experimental rig of the MIMC's cell built for the validation of proposed source based leakage tolerant current commutation method

5.2 Experimental Results

To clearly show the points in the converter at which the voltage and current waveforms were measured during the experiment test of the isolated single-phase AC/AC converter for the validation of the current commutation strategy, Figure 5.16 is shown.

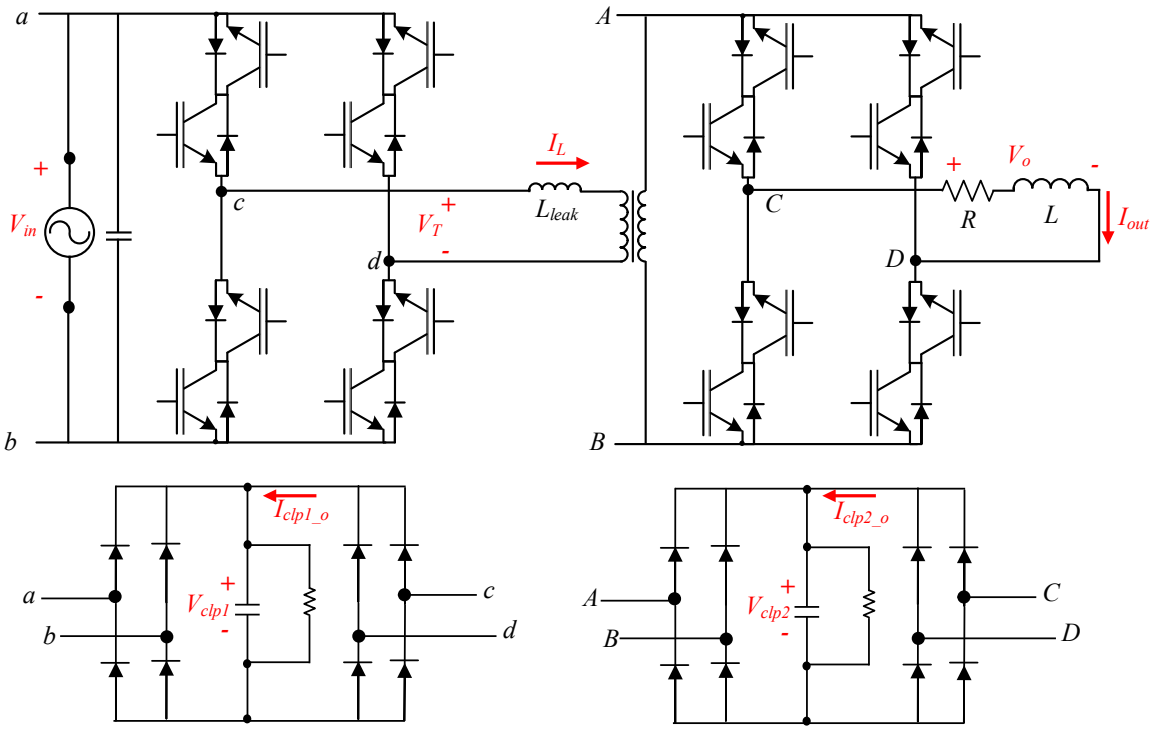


Figure 5.16: The single-phase to single-phase AC/AC converter showing the points at which voltages and currents were measured in the experiment

5.2.1 Standard 4-step Current Commutation Method

The standard 4-step current commutation method was applied to both the input and the output 4QSH-bridges of the MIMC's cell and the waveforms are shown in Figure 5.17-5.20. To keep the consistency between the experimental results and the simulation results given in chapter 4, it was assumed that the output side 4QSH-bridge commutates first from steady-state MS_1 to MS_2 by following the switching sequence of current based current commutation method which is shown in Figure 4.5. The same change of state is then achieved by the input 4QSH-bridge, but following the voltage based current commutation method as shown in Figure 4.6.

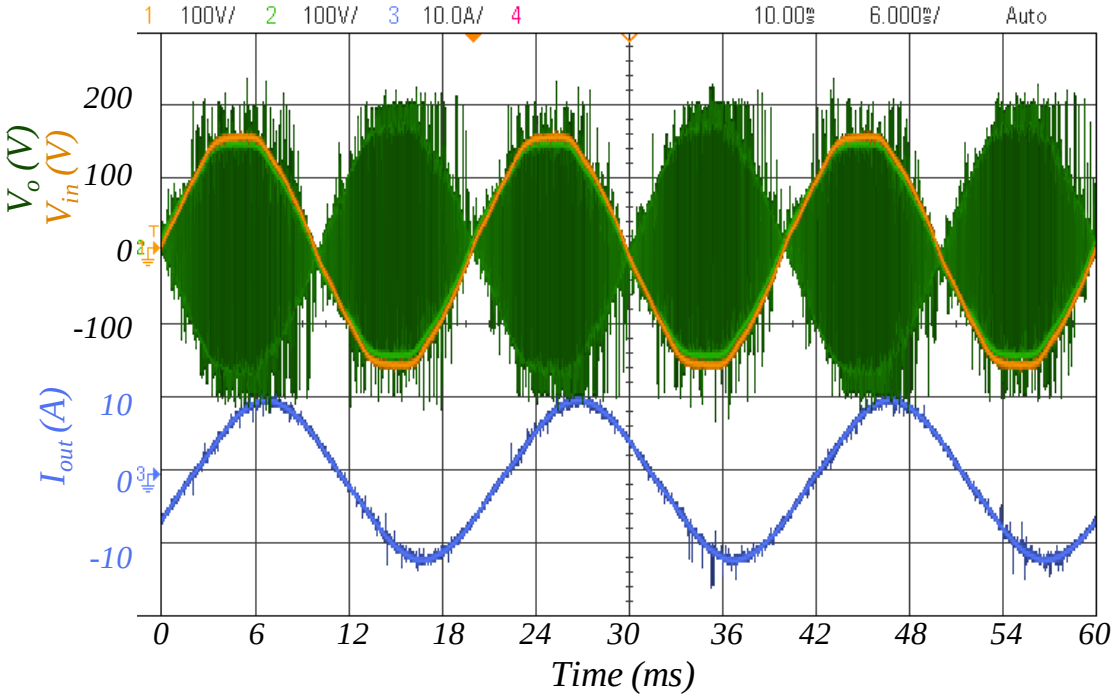


Figure 5.17: Voltages and currents at the terminal of the single-phase isolated AC/AC converter with the standard 4-step current commutation

Figure 5.17 shows the waveforms for the input voltage V_{in}, output voltage V_o and output current I_{out}. It can be seen that the low frequency input voltage V_{in} with fundamental of $50Hz$ is pulse width modulated by the single-phase converter to generate the output voltage V_o whose fundamental frequency is same as that of the input. Since the output voltage is a $10kHz$ pulse width modulated signal, therefore the fundamental period of the V_o is not directly visible. However, the output current I_{out} waveform confirms that the fundamental frequency of V_o is $50Hz$ because the output current is a filtered version of V_o. Another set of results is shown in Figure 5.18 which show waveforms at different points within the converter: transformer voltage V_T (5.7), leakage current I_L and clamp voltages V_{clp1}, V_{clp2}. Note that the clamp voltages V_{clp1}, V_{clp2}, shown in Figure 5.18, were obtained by setting AC coupling on the oscilloscope. This was done to clearly show the change in the clamp voltages V_{clp1}, V_{clp2} during the current commutation process.

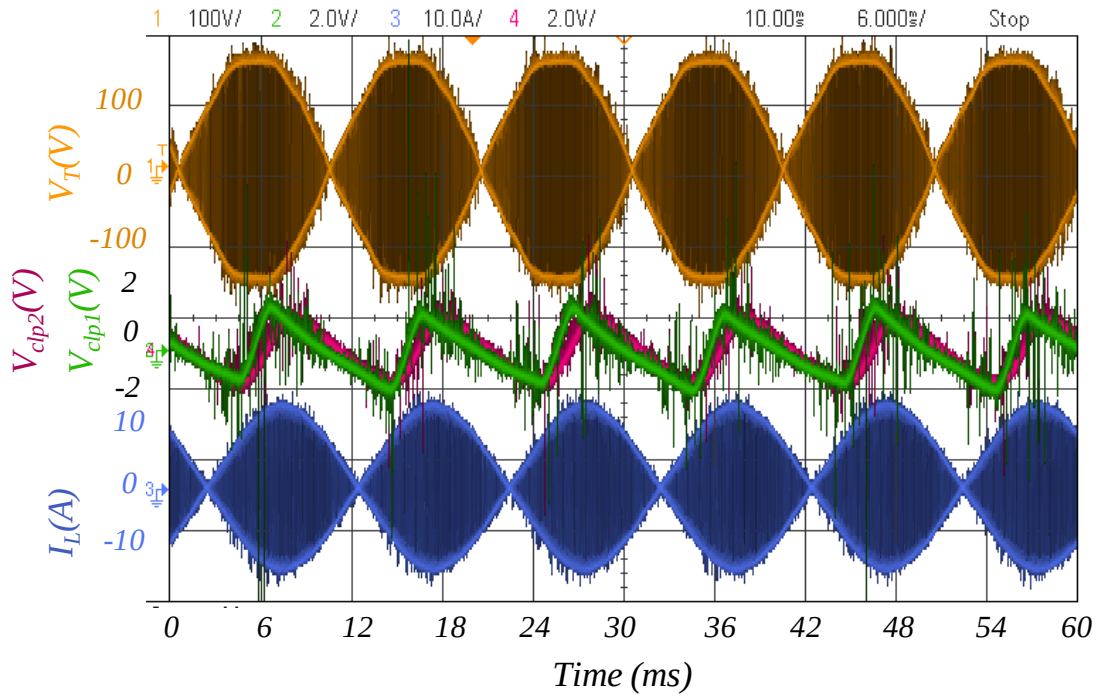


Figure 5.18: Transformer voltage V_T, leakage current I_L and voltages of the clamp circuits (input clamp voltage V_{clp1}, output clamp voltage V_{clp2} - in AC coupling - showing only ripples) with the standard 4-step current commutation

To highlight the problem associated with the standard 4-step current commutation method which is the triggering of the clamp circuit whenever the leakage current I_L reverses, Figure 5.19 is shown.

In Figure 5.19, the waveforms of current flowing into the clamp I_{clp2_o}, transformer voltage V_T and leakage current I_L are shown. It can be seen that at the time instances when the leakage current I_L is reversing, due to the transition from state 3 to state 4 (Figure 4.10), the current flowing into the clamp I_{clp2_o} is non-zero, the output side clamp circuit is being triggered. To clearly show this, a single commutation has been highlighted in Figure 5.19 and a zoomed view of the highlighted region is shown in Figure 5.20.

It can be clearly seen from the single commutation (Figure 5.20), that the clamp current I_{clp2_o} is zero from states 1 to 3, but as soon as the transition to state 4 occurs the over-voltage (4.1) is causing clamp circuit to trigger. The clamp circuit

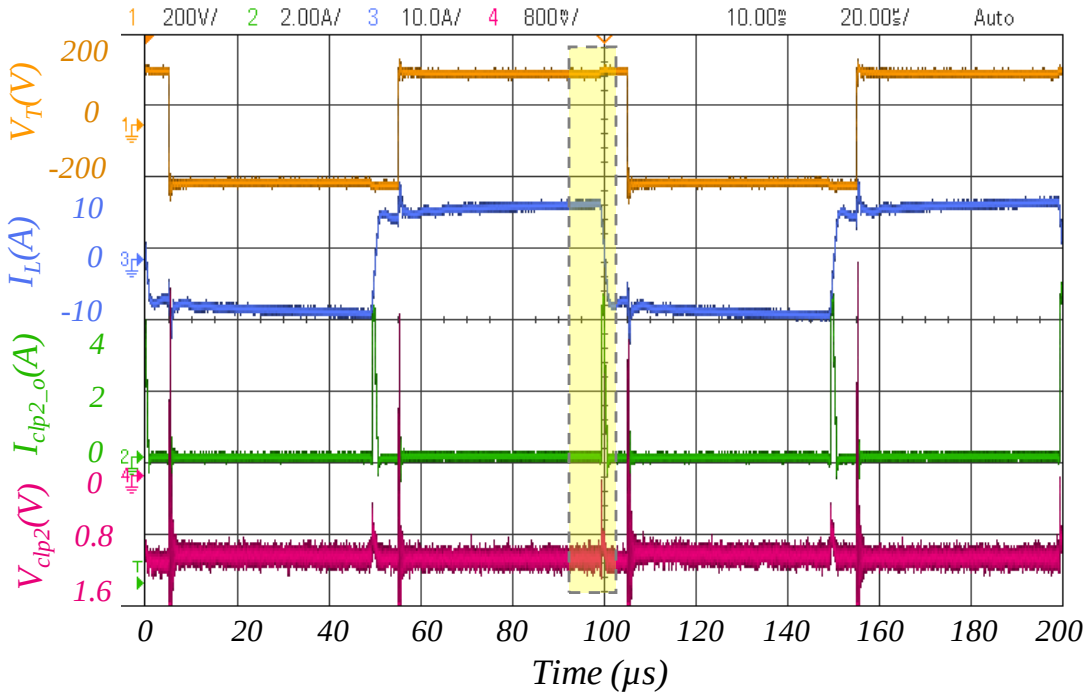


Figure 5.19: Triggering of clamp circuit during the reversal of leakage current I_L happening every commutation in the standard 4-step current commutation method

will quickly take up the output current I_{out} such that $I_{clp2_o} = I_{out}$ at the beginning of interval t_d, which in turn is causing the output voltage to be clamped. The clamp voltage then is driving the leakage current I_L from I_{out} first to zero, at the end of interval t_d, and finally to $-I_{out}$, at the end of interval t_c. Note that the clamp voltage V_{clp2}, shown in Figures 5.19 and 5.20, does not show the DC component in the clamp voltage but only shows the ripples because the channel was set in the AC coupling mode on the oscilloscope.

The experimental waveform of I_{clp2_o} is coherent with that of the simulation results shown in Figure 4.13. The rise in the output side clamp voltage V_{clp2} due to the current flowing into the clamp circuit can be found by using the relationship $V_{clp2_rise}(t) = \frac{1}{C_{clp}} \int_0^{t_d+t_c} I_{clp2}(t)\, dt$ where I_{clp2} is total current flowing into the output side clamp circuit $I_{clp2}(t) = I_{clp2_o}(t) + I_{clp2_i}(t)$.

From the results shown in Figure 5.19 and Figure 5.20, it is confirmed that the clamp circuit is dissipating the energy stored in the leakage inductor L_{leak} in the clamp resistor R_{clp} and hence causing power losses at every commutation at a rate of $2f_{sw}$. The commutation related power losses will get worse with the increase of the switching f_{sw}, but will get even worse when converter is operating at high power because the energy stored in the leakage inductor L_{leak} has a squared relationship with the current $E_{leak} = \frac{1}{2}L_{leak}{I_L}^2$. Therefore, it is not recommended to use standard 4-step current commutation method at high power whenever the transformer has non-zero leakage inductance.

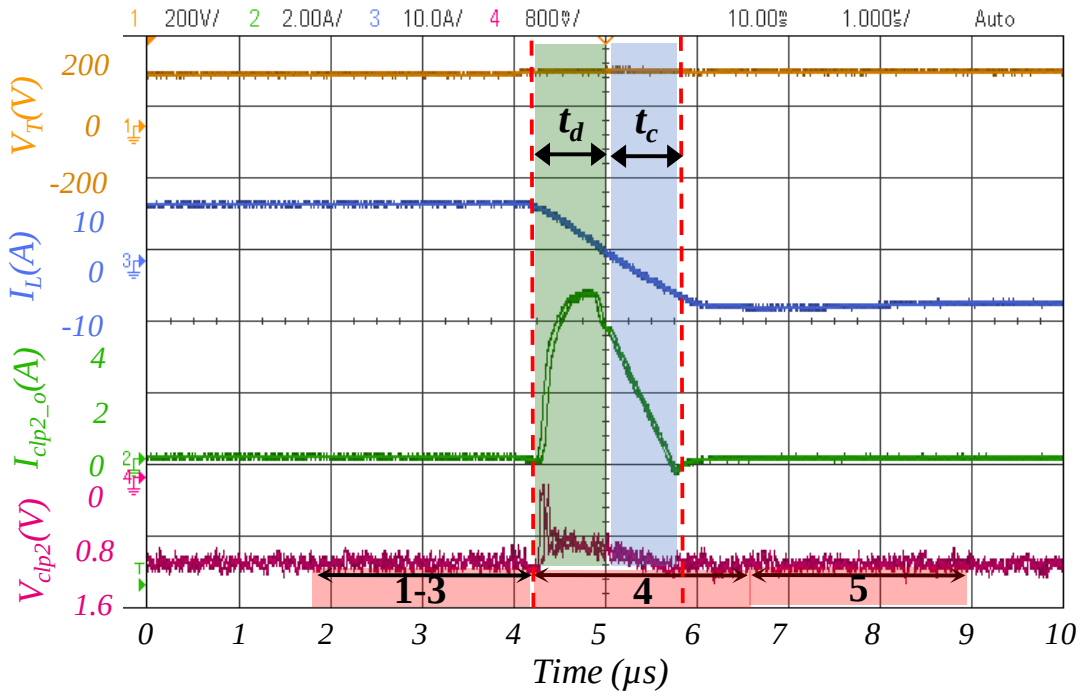


Figure 5.20: Expanded view of the region highlighted in Figure 5.19, showing current through the output clamp circuit during the reversal of leakage current after the transition from state 3 to state 4 in the standard 4-step current commutation - output clamp voltage V_{clp2} in AC coupling

5.2.2 Source Based Leakage Tolerant Current Commutation Method

In order to experimentally validate the source based leakage tolerant current commutation, a FSM has been implemented using VHDL in the FPGA. The FSM has been derived from the generalised commutation paths and is shown in Figure 5.21.

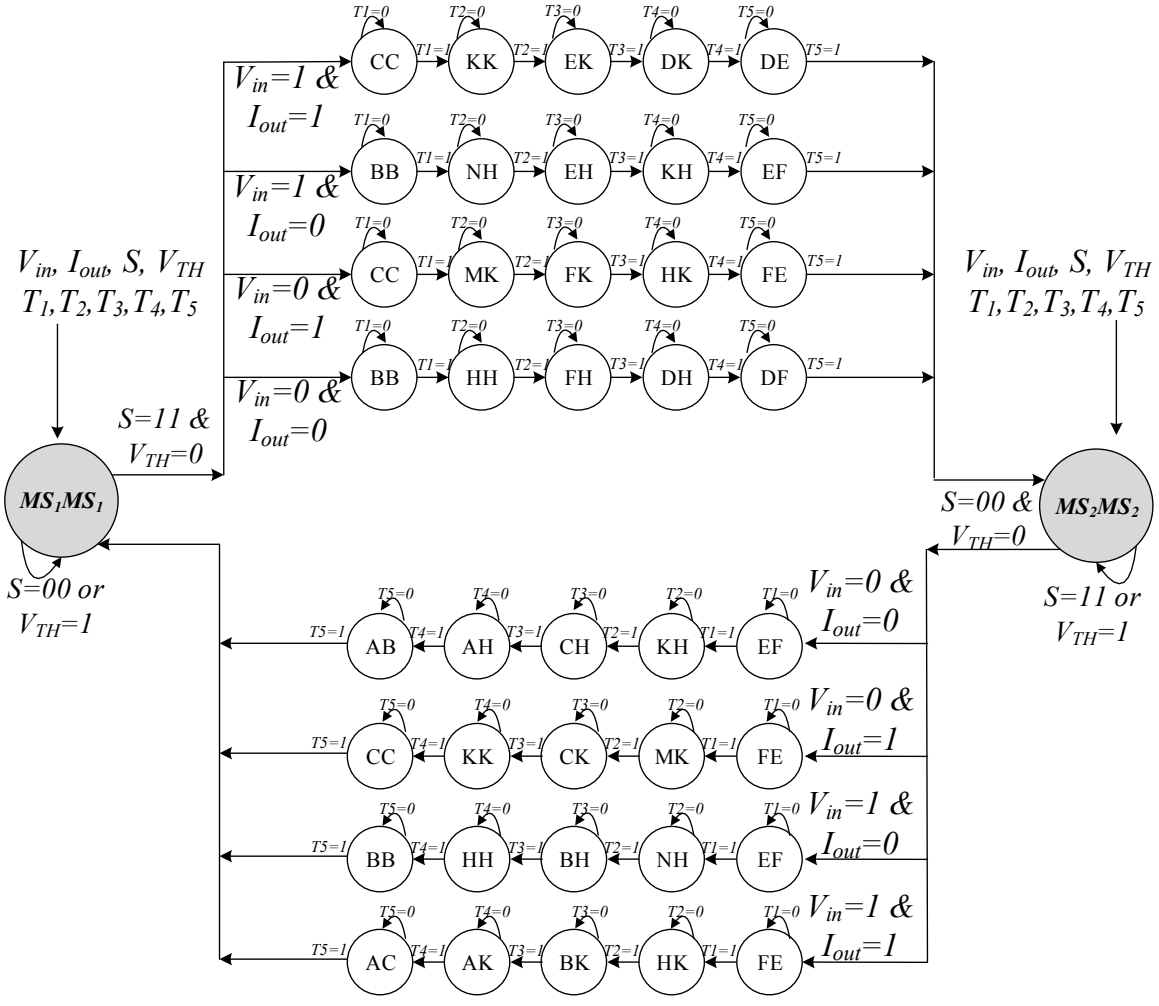


Figure 5.21: Moore type Finite-State Machine (FSM) implemented in FPGA using VHDL to test the proposed source based leakage tolerant current commutation method

To be able to compare the proposed current commutation method with the standard current commutation method, the same test case, which uses the two steady states i.e MS_1MS_1 and MS_2MS_2, has been considered. In order to move back-and-forth between these steady states using the proposed current commutation method, a FSM was developed.

The FSM, shown in Figure 5.21, has a total of nine input variables including V_{in}, I_{out}, S, V_{TH}, T_1, T_2, T_3, T_4 and T_5. Each of the input variables can acquire a Boolean value of either 1 or 0 and has been coded according to the Table 5.3.

Table 5.3: Input variables of FSM

Variable	Symbol	Condition	Coded Boolean Value
Input Voltage	V_{in}	$V_{in} > 0$	$V_{in} = 0$
		$V_{in} < 0$	$V_{in} = 1$
Output Current	I_{out}	$I_{out} > 0$	$I_{out} = 0$
		$I_{out} < 0$	$I_{out} = 1$
State Change	S	$S = MS_1MS_1$	$S = 00$
		$S = MS_2MS_2$	$S = 11$
Input Voltage Threshold	V_{TH}	$V_{TH} > V_{in}^{MIN}$	$V_{TH} = 0$
		$V_{TH} < V_{in}^{MIN}$	$V_{TH} = 1$
Commutation Timer	T_n	$T_n < T_{comm}$	$T_n = 0$
	$n = 1, .., 5$	$T_n = T_{comm}$	$T_n = 1$

The variable S is the state change variable which is responsible for holding the information about the next state. The variable V_{TH} is fed from the voltage threshold detection circuit and it determines if the voltage is above the minimum voltage required to drive the leakage current I_L. The time step between the subsequent commutation states is controlled by the commutation timer T_n $(n = 1, ..., 5)$. For example, assume that the value of state change variable S is 11, $V_{in} = 0$, $V_{TH} = 0$, $I_{out} = 0$ then in order to move to the required steady-state MS_2MS_2, the FSM will choose the commutation state *'BB'* and the timer T_1 will start incrementing until it reaches the defined commutation time T_{comm}. As soon as the timer T_1 reaches T_{comm}, $T_1 = T_{comm}$, the

value of timer T_1 becomes 1 which will cause the FSM to move the the next commutation state *'HH'* and then will move through the subsequent commutation states in a similar manner based on respective timer until it reaches the steady-state MS_2MS_2. Since, the values of timers T_n and all other variables are acquired at the initiation of the commutation process, the transition from one commutation to the next is not dependent on any of the present inputs, therefore the FSM shown in Figure 5.21 is a Moore based state machine [116, 117].

Experimental results obtained by operating single-phase isolated AC/AC converter with the proposed FSM (Figure 5.21) are shown in Figures 5.22-5.25. Figure 5.22 shows the waveforms at the input and output terminals of the converter. Note that the frequency of the waveforms at the input side matches with that at the output side and the converter has sinusoidal waveforms at its input and output terminals. Since the current I_{out} is lagging the voltage, the converter is testing all the commutation paths shown in Figure 5.21 and it can be noted that the behaviour of the output voltage V_o for cases when $V_{in}.I_{out} < 0$ is different than for the cases when $V_{in}.I_{out} > 0$. This is due to those commutation states which cause $V_o = -V_{in}$. For example, if the transition from MS_1MS_1 to MS_2MS_2 is required when $V_{in} > 0$ and $I_{out} < 0$ then the converter will take the commutation path *'CC', 'MK', 'FK', 'HK', 'FE'* in the FSM shown in Figure 5.21. The output voltage is $V_o = -V_{in}$ during the commutation state *'HK'* when the leakage current has fully reversed and the FSM is waiting for next state *'FE'*. This justifies the distortion added in the output voltage V_o during the highlighted regions of Figure 5.22. Nonetheless, it can be seen by comparing Figure 5.22 with Figure 5.17 that the distortion in the output voltage is higher when the standard 4-step current commutation method is used. However, the impact of the distortion associated with the proposed commutation on the output waveform quality of the MIMC is analysed and presented in Section 6.2.1 of Chapter 6.

Figure 5.23 presents the waveforms at different points in the converter including transformer voltage V_T, transformer or leakage current I_L and voltages V_{clp1}, V_{clp2} of the input and output side clamp circuits, respectively.

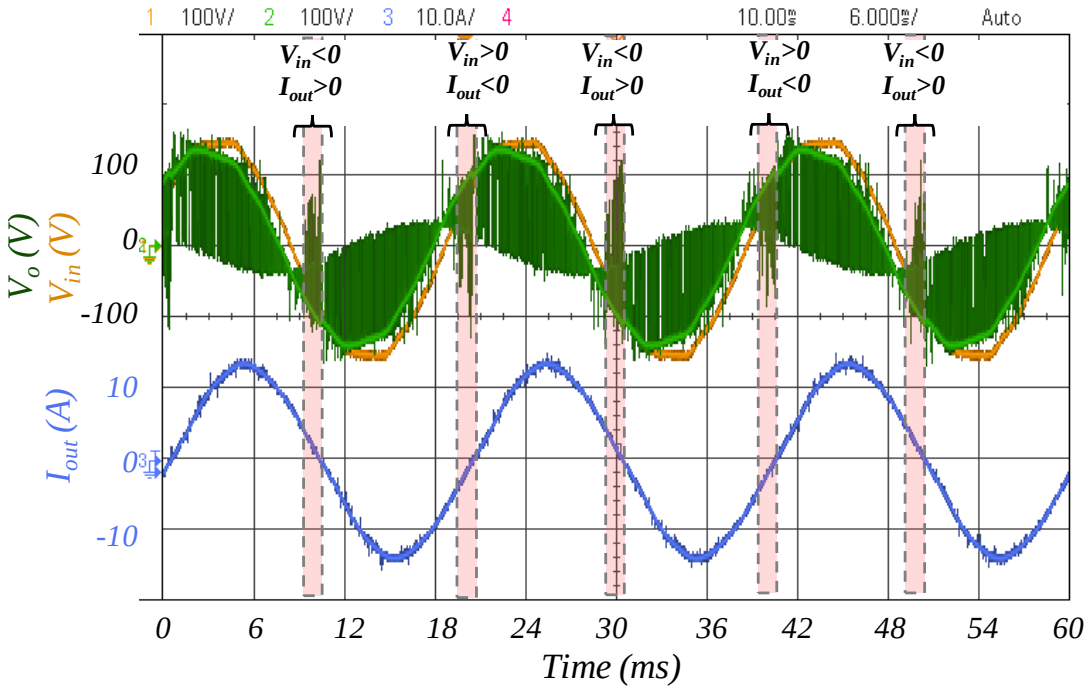


Figure 5.22: Voltages and currents at the terminal of the single-phase isolated AC/AC converter with the proposed current commutation method

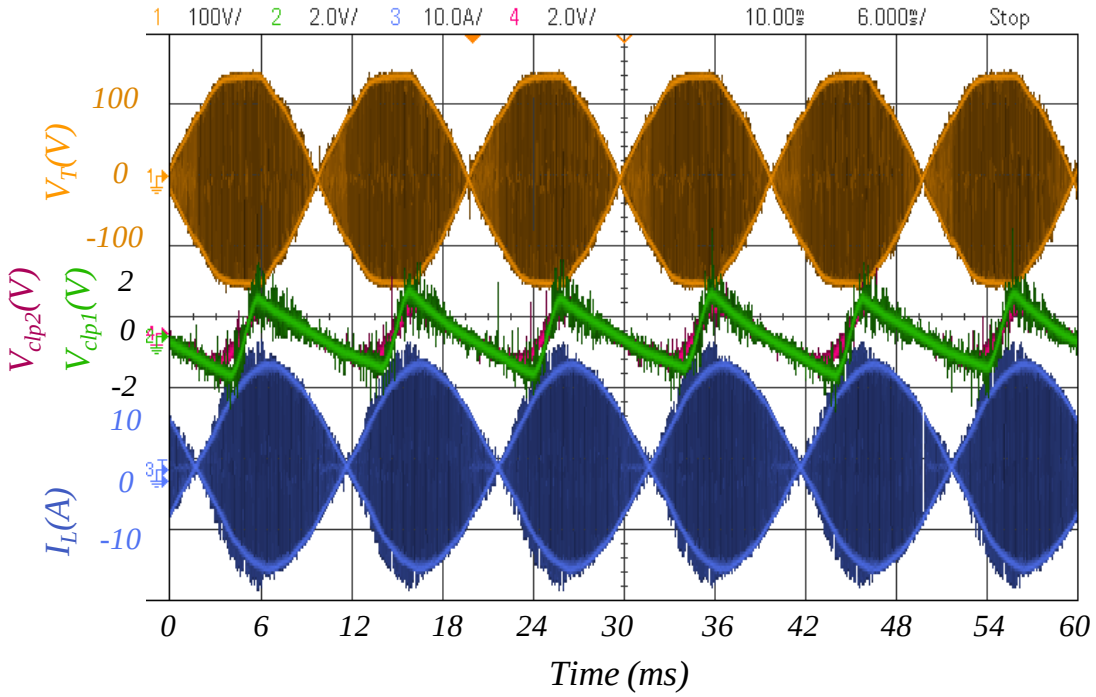


Figure 5.23: Transformer voltage V_T, leakage current I_L and voltages of the clamp circuits (input clamp voltage V_{clp1}, output clamp voltage V_{clp2} -in AC coupling - showing only ripples) with the proposed current commutation method

To show that the leakage current I_L is not disturbed and the clamp circuit is not triggered during commutations, several commutations are shown in Figure 5.24. For the ease of comparison, the time-scale of the results obtained with source based leakage tolerant current commutation method, given in Figure 5.24, has been kept same with that of the standard 4-step current commutation method given in Figure 5.19. When compared to Figure 5.19, it can be noted from Figure 5.24 that the clamp current is not affected during the leakage inductance current reversal.

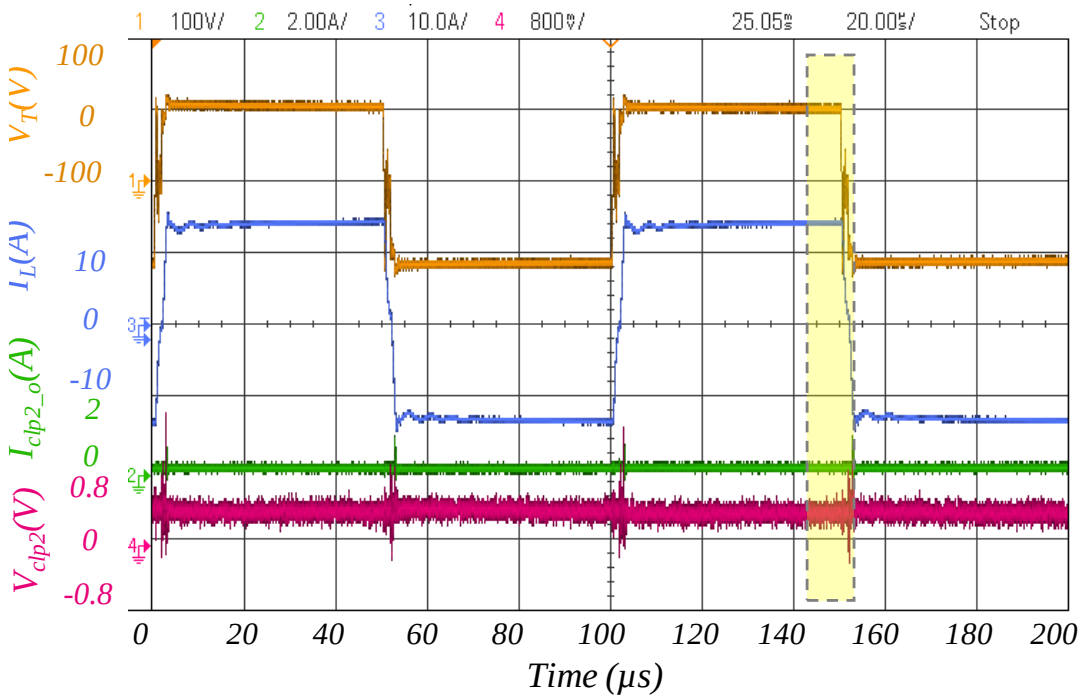


Figure 5.24: Clamp circuit not triggering during the reversal of leakage current I_L with the proposed current commutation method

To highlight that the clamp circuit is not being triggered, a zoomed view of Figure 5.24, focussing on a single commutation event, is shown in Figure 5.25. To keep the experimental results coherent with that of the previous discussion, the single commutation event of Figure 5.25 is for the same case that was discussed in Section 4.4.2 (moving from MS_1MS_1 to MS_2MS_2 when $V_{in} > 0$, $I_{out} > 0$). Furthermore, the state numbers 1 to 9, marked on Figure 5.25, refer to the commutation states illustrated in Figure 4.15. States 4 to 6 are significantly important as the *'current decoupling'* is carried out within these states. It can be seen that the polarity of the transformer

voltage V_T in state 4 is reversed therefore making $V_T = -V_{in}$ and hence equation (4.7) becomes valid. Since, the output bridge is short circuited, this reversed voltage $V_T = -V_{in}$ appears across the leakage inductance and the leakage current I_L starts to decrease in the beginning of state 4 and becomes zero at the end of state 4, following equation (4.12). After the leakage inductance is discharged, $I_L = 0$, the transformer voltage V_T goes to zero and the converter is in state 5. Turn ON of switches $S4i$, $S6i$ initiate the state 6 and the leakage inductor begins to re-energise until the value of leakage current reaches a final value of $I_L = -I_{out}$.

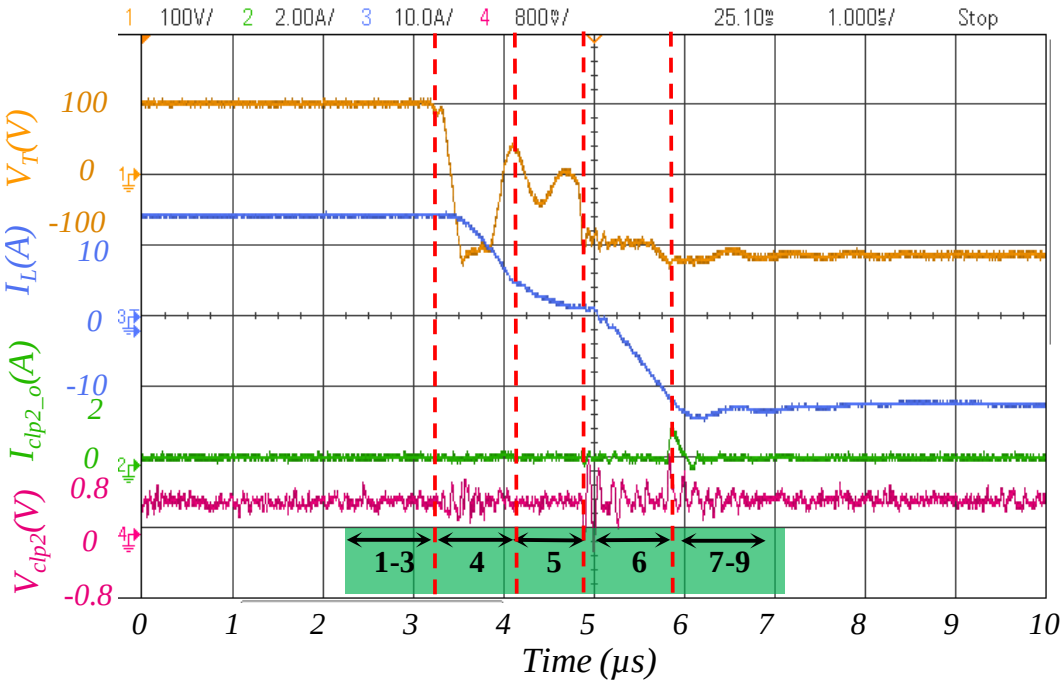
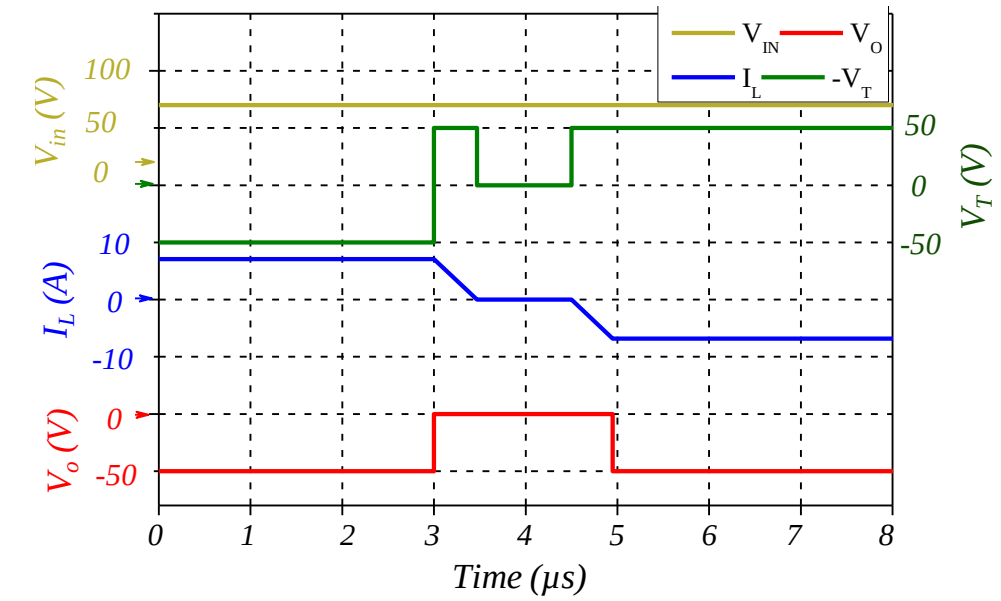
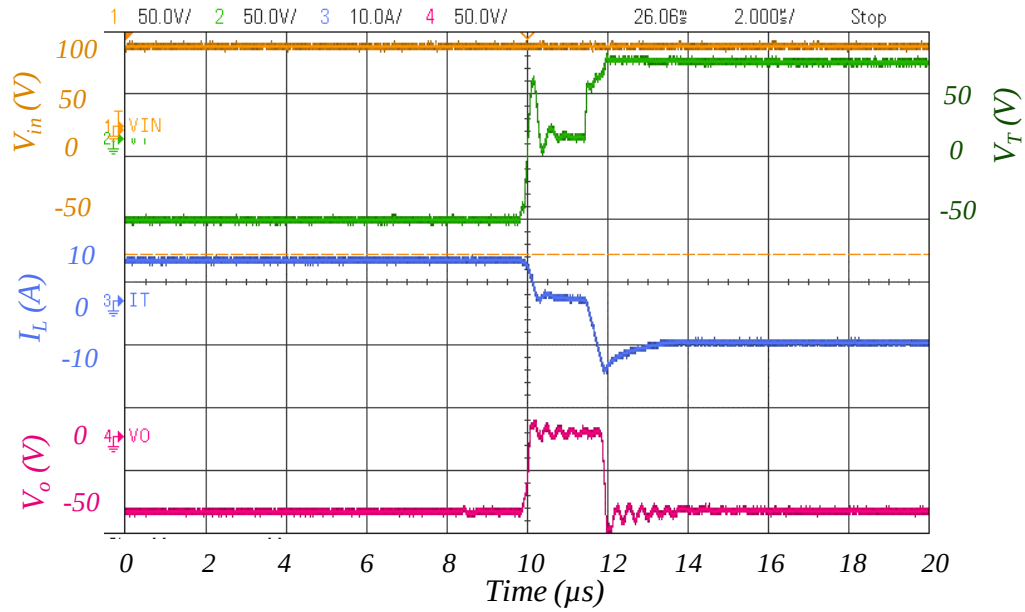


Figure 5.25: Expanded view of the region highlighted in Figure 5.24, showing current through the clamp circuit is zero during the reversal of leakage current with the proposed current commutation method

It can be seen from Figure 5.25 that the value of leakage current at the start of state 4 was $I_L = I_{out}$ whereas the value of leakage current at the end of state 6 is $I_L = -I_{out}$, indicating that the leakage current reversal happening within states 4 to 6 is in accordance with the simulation results shown in Figure 4.16. Moreover, it can seen that during the current reversal process, the clamp circuit current remains zero which indicates that the clamp circuit is not triggered when the proposed source based leakage tolerant current commutation method is used.

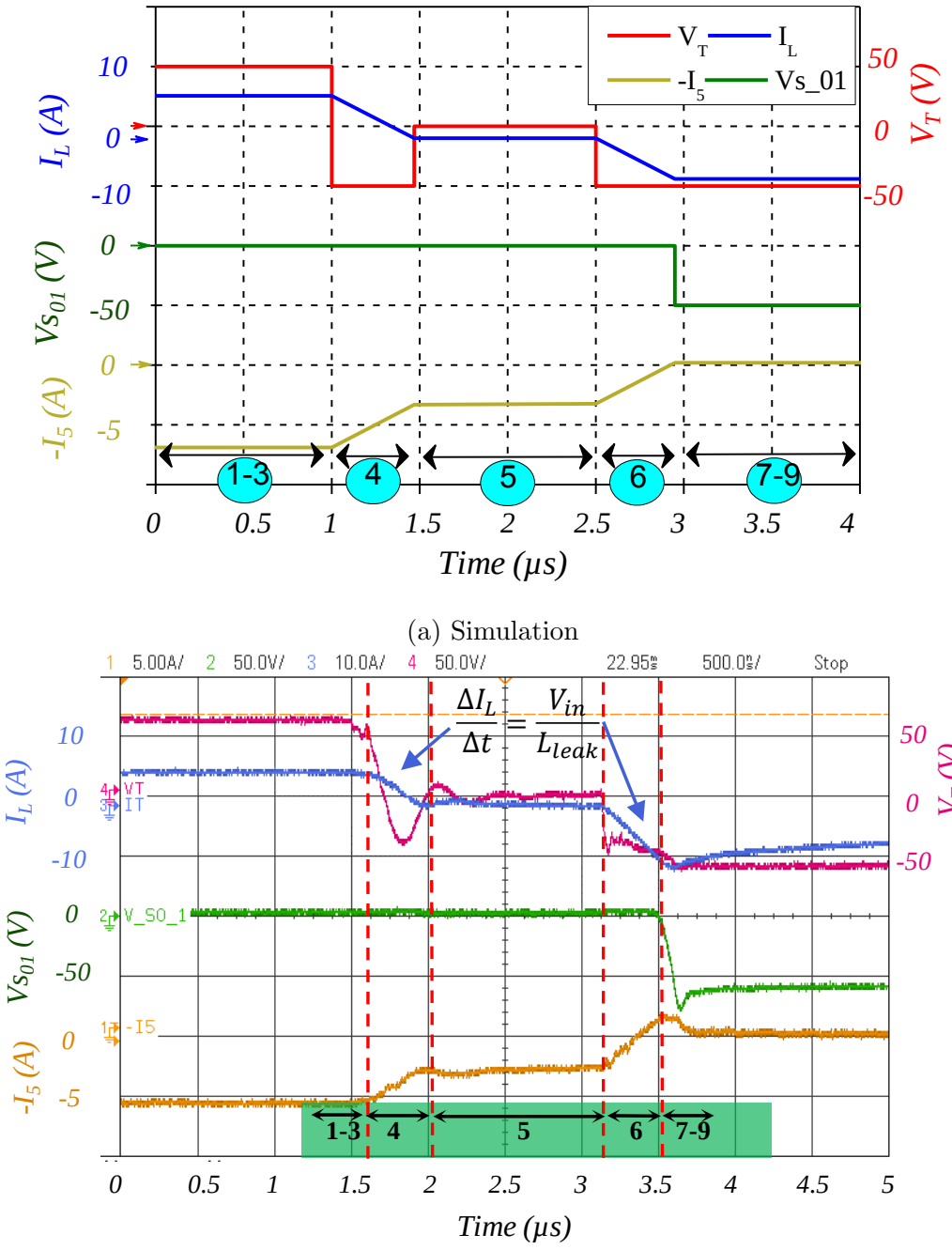


(a) Simulation



(b) Experiment

Figure 5.26: Comparison between simulated and experimented waveforms of input voltage V_{in}, output voltage V_o, transformer voltage V_T and leakage current I_L with the proposed current commutation method for the commutation from MS_1MS_1 to MS_2MS_2 when $V_{in} > 0$, $I_{out} > 0$.



(a) Simulation

(b) Experiment

Figure 5.27: Comparison between simulated and experimented waveforms of voltage across four-quadrant switch $s01$, its current i_5 in relation with the transformer voltage V_T and current I_L during the commutation from MS_1MS_1 to MS_2MS_2 when $V_{in} > 0$, $I_{out} > 0$.

The experimental-comparable simulation results were obtained by using PLECS simulation toolbox and are shown, against experimental waveforms, in Figure 5.26 to Figure 5.27. By comparing simulation waveforms of Figure 5.26a with experimental waveforms of Figure 5.26b, a good match is seen. However, the leakage current I_L in simulation does not have undershoot is because the diode model used in simulation is ideal and thus has no reverse-recovery.

To validate that the current(s) and voltage(s) within the 4QSH-bridge are in agreement with the discussion of Chapter 4, the recorded waveforms of voltage across the switches S_{0o}, S_{1o} in the output bridge and the leg current i_5 are shown in Figure 5.27b. The leg current i_5 equals the output current, $i_5 = I_{out}$, in state 1 to 3 which validate equation (4.4). Note that the slope of the leakage current I_L in state 4 and state 6 depends on the ratio of input voltage V_{in} and leakage inductance L_{leak} and be written as $\frac{V_{in}}{L_{leak}}$. During state 5, the output current is divided in both legs therefore, the leg current i_5 reduces to half of its original value, $i_5 = \frac{I_{out}}{2}$, which makes (4.9) true. Hence, Figure 5.26 and Figure 5.27 validate that the experimental results are in accordance with the discussion of Section 4.4.2 and match with the simulation results.

5.3 Comparison of Losses

For the operating conditions of the experimental setup given in Section 5.1, the losses associated with both the proposed current commutation method and the standard 4-step current commutation method, are compared in this Section.

It has been confirmed from the experimental validation, given in Sections 5.2.1 and 5.2.2, that the clamp circuit is being triggered with the standard 4-step commutation method. Therefore both methods can be compared in terms of clamp related losses. The sequence of switches turning ON/OFF differ in both current commutation methods, hence both methods will offer different switching loss profiles. However, both methods will have similar conduction losses as the commutation time is not a significant part of the switching period. Hence, both of the methods will be compared for

leakage inductance related losses and switching losses.

It is important to note that the experimental rig is a scalable and flexible setup serving as a proof-of-concept demonstrator which is not optimised for efficiency. Hence, the losses shown in this section are not representation of the technology but are a representative comparison between the two current commutation strategies.

5.3.1 Leakage Inductance Related Losses with Standard 4-step Current Commutation Method

In order to model the power flowing into the output clamp circuit when 4-step current commutation is used, the waveform of the total current flowing into the clamp circuit, when transition from state 3 to state 4 occurs (Figure 4.13), can be approximated by the triangular waveform shown in Figure 5.28. As soon as the transition occurs, both the leakage and output current flow into the the clamp causing a total current of $2I_{out}$, $|I_L| + |I_{out}| = 2I_{out}$, which decreases with a slope of $(|V_{in}(t)| - V_{clp2})/L_{leak}$ assuming that the clamp voltage V_{clp2} is constant. The area under the triangle will represent the charge and can be calculated by:

$$Q(t) = \frac{1}{2}\Delta T(2I_{out}(t)) \tag{5.19}$$

$$Q(t) = \frac{2{I_{out}}^2(t)L_{leak}}{V_{clp2} - |V_{in}(t)|} \tag{5.20}$$

$$E(t) = \frac{2{I_{out}}^2(t)L_{leak}V_{clp2}}{V_{clp2} - |V_{in}(t)|} \tag{5.21}$$

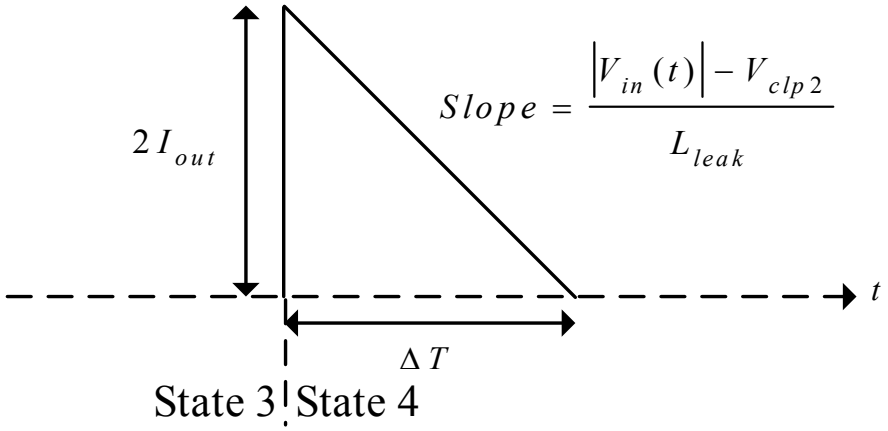


Figure 5.28: Waveform of current flowing into the output clamp circuit due to transition from step 3 to step 4 in standard 4-step current commutation method

The energy per commutation can be obtained by multiplying charge of (5.19) with the clamp voltage V_{clp2}, as given by (5.21). Since there are two commutation events per switching cycle, the average power loss over switching cycle of f_{sw} can simply be found:

$$\bar{P}(t) = \frac{4{I_{out}}^2(t) L_{leak} f_{sw}}{1 - \frac{|V_{in}(t)|}{V_{clp2}}} \tag{5.22}$$

$$\bar{P}(t) = \frac{4\left(I_{out}^{MAX} \sin(\omega_o t - \theta)\right)^2 L_{leak} f_{sw}}{1 - \frac{\left|V_{in}^{MAX} \sin(\omega_o t)\right|}{V_{clp2}}} \tag{5.23}$$

Note that no leakage related power losses are associated with the proposed current commutation.

5.3.2 Switching Losses with Standard 4-Step Current Commutation Method

To analyse the switching losses, refer to the commutation example of Figure 4.5 where commutation of output 4QSH-bridge from steady-state MS_1 to MS_2 is required when $I_{out} > 0$ and $V_{in} > 0$:

- In state 2, the non-conducting switches S_1, S_3 are turned OFF with Zero Current Switching (ZCS).
- In state 3, the switches S_5, S_7 will be turned ON with ZCS.
- In state 4, the switches S_0, S_2 are turned OFF with non-zero current resulting in a hard switching.
- In state 5, the steady-state MS_2 is reached by turning ON the switches S_4, S_6 under Zero Voltage Switching (ZVS).

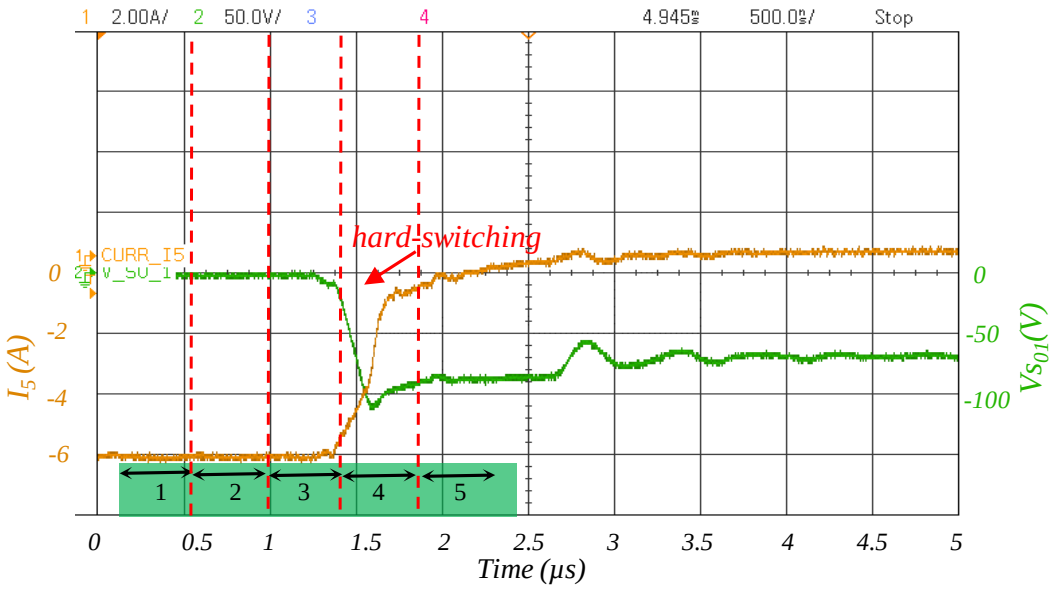


Figure 5.29: Leg current I_5 and voltage vs_{01} across switches S_{0o}, S_{1o} showing the hard turn-OFF of switch S_{0o}

The analysed commutation case discussed above when $I_{out} > 0$ and $V_{in} > 0$ has a total of eight transitions involved in the change of state of a 4QSH-bridge with two of the transitions being hard while the remaining six are soft. This gives a total of sixteen switch transitions, of which four are hard and twelve are soft, for both the input and output 4QSH-bridges. In a similar manner, number of hard and soft switching for all the other cases ($I_{out} > 0$ and $V_{in} < 0$), ($I_{out} < 0$ and $V_{in} < 0$), ($I_{out} < 0$ and $V_{in} > 0$) have been analysed and the information about switch transitions is summarised in Table 5.4. However, for confirmation of hard-switching(s) in the standard 4-step current commutation method, the current I_5 through the switches S_{0o}, S_{1o} and the voltage Vs_{01} across these switches are shown in Figure 5.29 assuming the current commutation method is applied to the output side 4QSH-bridge. It can be noted that the transition from state 3 to state 4 is causing the voltage Vs_{01} to rise from zero while the current I_5 starts to decrease until it reaches zero and this is because the switch S_{0o} is turned OFF in state 4. Since there is an over-lap between the current I_5 and voltage Vs_{01} the turn OFF of the switch S_{0o} is hard. This matches with the above discussion of soft and hard transitions that S_{0o} is turned OFF with non-zero current.

5.3.3 Switching Losses with Proposed Current Commutation Method

The switching losses with the proposed current commutation method can be determined by referring to the commutation states, shown in Figure 4.15, for the case when required steady-state is MS_2MS_2 and $I_{out} > 0$ and $V_{in} > 0$.

- In state 2, the non-conducting switches S_{1i}, S_{3i} and S_{1o}, S_{3o} are turned OFF with Zero Current Switching (ZCS).
- In state 3, the switches S_{5i}, S_{7i} and S_{5o}, S_{7o} will be turned ON with ZCS.
- In state 4, the switches S_{0i}, S_{2i} are turned OFF with non-zero current resulting in hard switching.

- In state 5, no switching action takes place and in terms of ON/OFF state of switches is same as state 4.
- In state 6, switches S_{4i}, S_{6i} are turned ON, to re-energise the leakage inductance L_{leak}, will experience ZCS because the rate of change of current is limited by the leakage inductance L_{leak}.
- In state 7, no switching action takes place and in terms of ON/OFF state of switches is same as state 6.
- In state 8, the switches S_{0o}, S_{2o} are turned OFF with ZCS as they carry no current.
- In state 9, to be able to reach steady-state MS_2MS_2, the switches S_{4o}, S_{6o} are turned ON with ZVS.

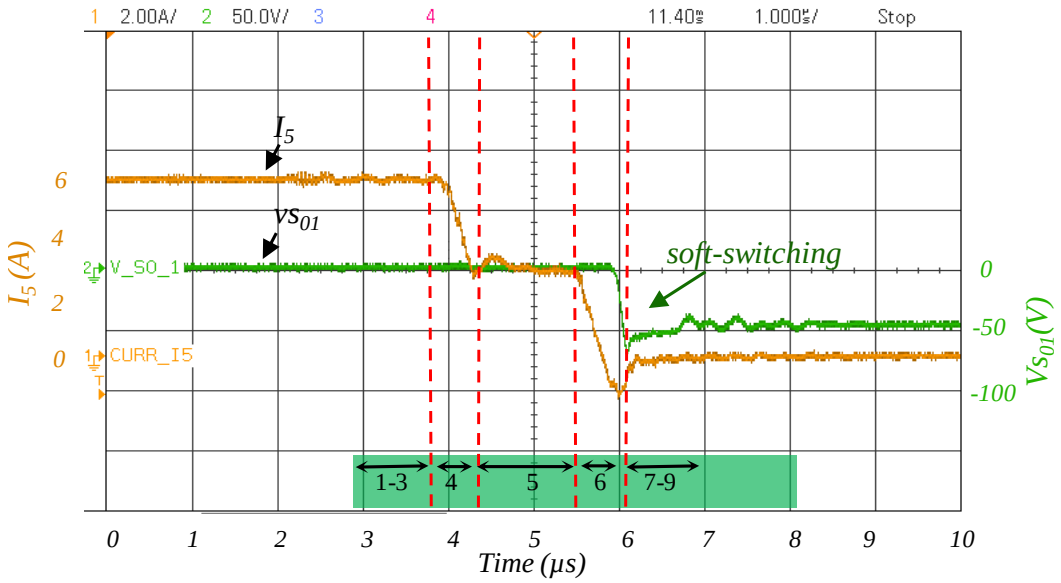


Figure 5.30: Leg current I_5 and voltage vs_{01} across switches S_{0o}, S_{1o} showing the soft turn-OFF (ZCS) of switch S_{0o}

By considering the switch transitions state by state, it can be noted that the there are a total of sixteen switch transitions out of which only two are hard and fourteen are soft. The information of switch transitions for the remaining cases ($I_{out} > 0$ and $V_{in} < 0$), ($I_{out} < 0$ and $V_{in} < 0$), ($I_{out} < 0$ and $V_{in} > 0$) has been found in a

similar manner and is compared with the information of transitions obtained with the standard 4-step current commutation given in Table 5.4.

Waveforms of the voltage across switches S_{0o}, S_{1o} and current I_5 through the switches are shown in Figure 5.30 when source based leakage tolerant current commutation is used. Note that the transition from state 5 to state 6 is causing the current I_5 to decrease until it reaches zero at the end of state 6 but it is important to note that as the voltage vs_{01} starts rising after the current I_5 be has reached zero. There is no over-lap between voltage and current and the turn OFF of the switch S_{0o}, in state 8, is soft which is coherent with the discussion of switch transitions in each state given above.

Table 5.4: Comparison of switch transitions in standard standard 4-step and proposed current commutation methods for all possible scenarios of V_{in} and I_{out} when converter moves between MS_1MS_1 and MS_2MS_2

Current Commutation Method	Input bridge switch transitions	Output bridge switch transitions
Standard 4-step method	Total = 8 Soft = 6, Hard = 2	Total = 8 Soft = 6, Hard = 2
Leakage tolerant method	Total = 8 Soft = 6, Hard = 2	Total = 8 Soft = 8, Hard = 0

It is interesting to note, from Table 5.4, that when proposed current commutation method is used there will be only two hard switchings and the output 4QSH-bridge will be completely soft-switched whereas in case of standard 4-step current commutation method the number of hard switching is double. This indicates that the proposed current commutation method is not only leakage inductance tolerant but also it is offering lower switching and reverse recovery losses because the slope of current is limited by the leakage inductance. In order to validate this claim, thermal model of the SEMIKRON SKM150GM12T4G IGBT power modules power modules was developed in PLECS and the simulation results are shown in Figure 5.31.

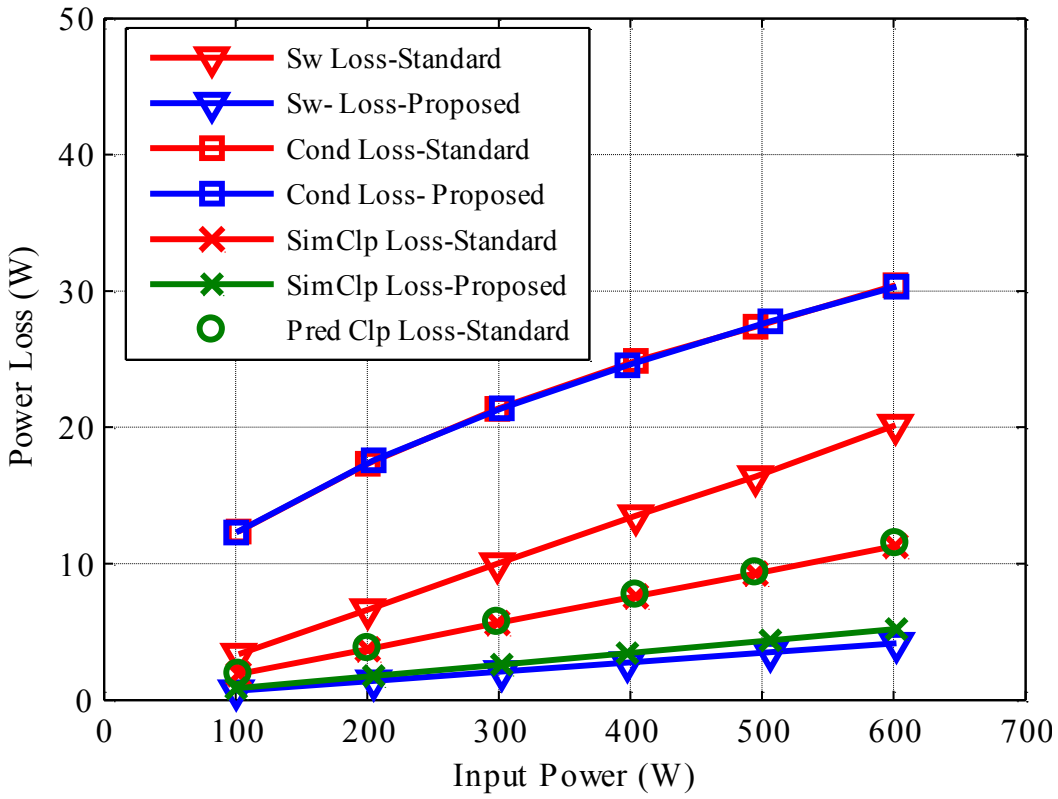


Figure 5.31: Simulated losses with standard and proposed current commutation methods: semiconductor switching loss with standard method (Sw Loss-Standard), semiconductor switching loss with proposed method (Sw Loss-Proposed), semiconductor conduction loss with standard method (Cond Loss-Standard), semiconductor conduction loss with proposed method (Cond Loss-Proposed), clamp circuits loss with standard method (SimClp Loss-Proposed), predicted clamp loss, using (5.23), with standard method (Pred Clp Loss-Standard) and clamp circuits loss with proposed method (SimClp Loss-Proposed)

Note that the results at different power levels are obtained simply by varying the input voltage while keeping the RL load fixed. As expected, both methods are offering similar conduction losses because the commutation takes a very small part of the switching period. The switching losses with the proposed method are reduced to less than the half of that offered by standard method, because not only number of hard switchings are halved, as seen from Table 5.4, but the reverse-recovery losses are also reduced. In addition, the leakage inductance related losses are predicted in Figure 5.31 by averaging equation (5.23) over fundamental period of the input voltage.

Finally, the experimental losses are compared with the simulated losses as shown in Figure 5.32. The simulated losses are total losses obtained by summing up all the losses that are shown in Figure 5.31. Coherency between experimental and simulated loss profiles validate that loss predicted analytically and in simulation, a significant reduction in losses is achievable when the proposed leakage tolerant current commutation method is used instead of the standard current commutation method.

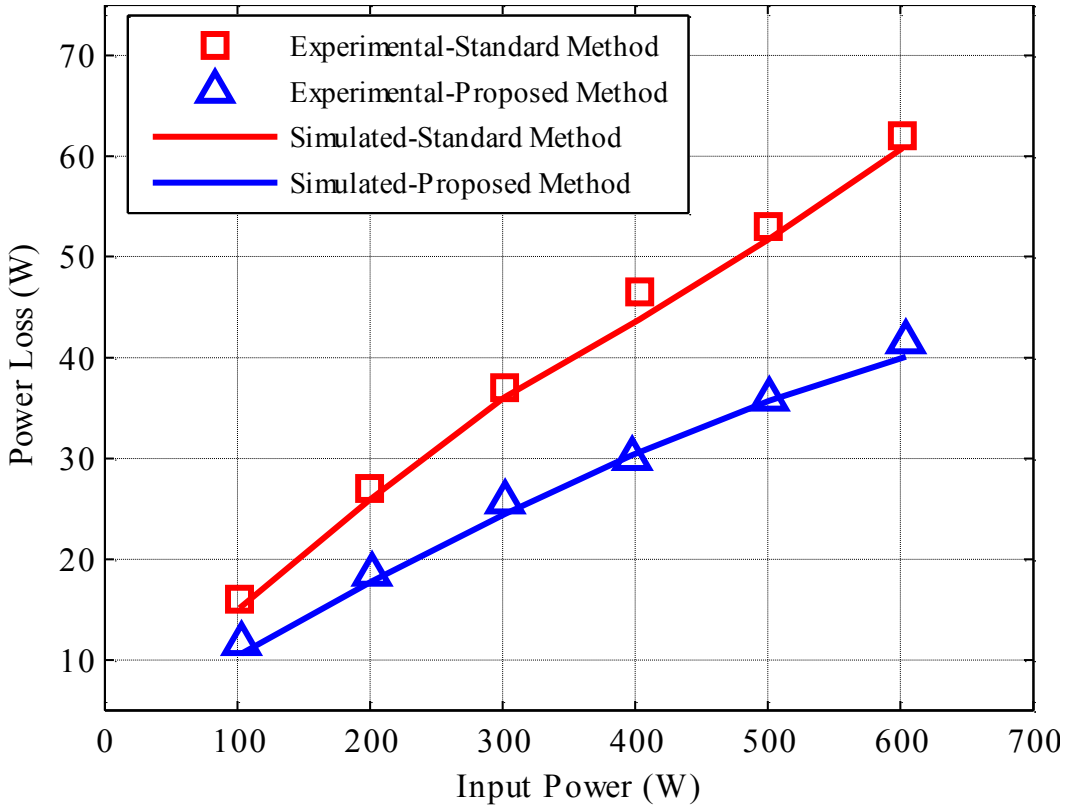


Figure 5.32: Experimental and simulation-predicted losses with standard 4-step current commutation method and proposed current commutation method in a single cell of the MIMC

5.4 Conclusions

To validate the concept of the source based leakage tolerant current commutation method an experimental setup of a single-phase AC/AC converter was developed and tested for a simple modulation case which used two steady states. The transition between the two steady states was done by implementing the standard 4-step current commutation method first, the experimental results validated the triggering of the clamp circuits which lead to additional power losses. The proposed current commutation method was also implemented and the results, when compared with that obtained with the standard 4-step current commutation method, highlight the absence of commutation related triggering of the clamp circuit. Furthermore, the commutation losses in clamp circuit, when the standard current commutation method is used, are confirmed in a comparison of losses. In addition to this, a significant reduction in the switching losses has also been seen when proposed method is employed because the rate of change of current $\frac{dI}{dt}$ through the devices is limited by the leakage inductance, increasing the total number of soft-switchings. Similar to dead-time distortion in a standard two-level inverter, there is a commutation-related distortion associated with the proposed method because the commutation process can never be instantaneous in reality.

Chapter 6

Experimental Validation and Control of Modular Isolated Matrix Converter (MIMC)

6.1 Introduction

Various modulation methods for the Modular Isolated Matrix Converter (MIMC) were presented in Chapter 3 with the assumption that the transitions between the states of the MIMC happen instantaneously. However, this assumption is not valid in reality because a commutation method is essential to achieve a safe transition between the states. For safe transitions between the states, a source based leakage tolerant commutation method was proposed in Chapter 4. The commutation method was experimentally validated on a single-cell of the MIMC for a simple case of modulation in Chapter 5. Chapter 6 validates the operation of the proposed MIMC by modulating the cells according to one of the modulation methods, presented in Chapter 3, and commutating, using the source based leakage tolerant commutation method presented in Chapter 4.

Chapter 6 presents the open-loop operation which experimentally validates the conceptual MIMC. Furthermore, to compensate for the distortion introduced by the commutation strategy and to show that the MIMC can operate in a realistic scenario, a closed-loop system was also presented. However, the optimisation and the performance in terms of the closed-loop control is out of the scope of this work because the key focus is not the control but the practically demonstration of a conceptual MIMC topology.

In Chapter 5 a simple case of modulation which uses two steady-states, MS_1MS_1 and MS_2MS_2, was considered but more steady-states are required to implement the modulation methods presented in Chapter 3.

In the case of the scalar modulation (Venturini Modulation) four steady-states and seven paths are required which are re-shown in Figure 6.1. However, each of the seven paths will contain four sub-paths, for conditions $(V_{Ki} > 0, I_{jo} > 0)$, $(V_{Ki} > 0, I_{jo} < 0)$, $(V_{Ki} < 0, I_{jo} > 0)$, $(V_{Ki} < 0, I_{jo} < 0)$, when the source based leakage tolerant commutation method is used. This will lead to a total of 28 possible commutation paths. Note that these 28 must be implemented in the FPGA using a Finite State Machine (FSM) in order to use the Venturini Modulation method.

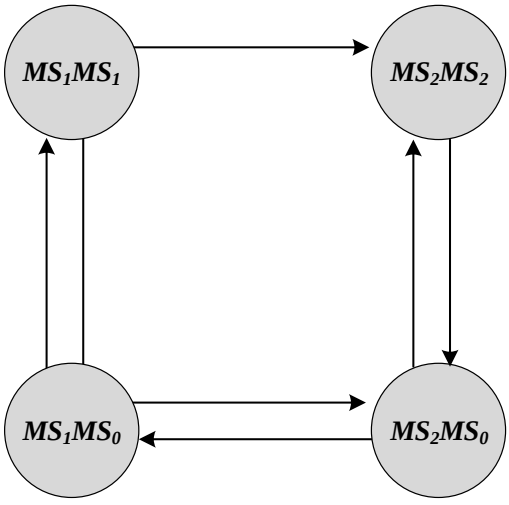


Figure 6.1: State transitions (per-cell) required for the implementation of the Venturini Modulation method

In the case of the SVM method, the number of commutation paths will increase up to 120. In terms of implementation, all 120 commutation paths must be defined in the FSM. Implementation of 120 paths in the FSM will limit the base clock of the FSM to respect the setup and hold times. Therefore, considering ease of implementation as priority, the basic Venturini Modulation method was selected for the validation of operation of the MIMC. Note that the low voltage regulation of the Venturini Modulation method is not an issue in the MIMC because it can be increased by changing the turn-ratio of the MF transformers.

The state-transitions for the Venturini Modulation method, shown in Figure 6.1, can be achieved using the source based leakage tolerant commutation method by implementing the FSM shown in Figure 6.2.

The FSM, shown in Figure 6.2, has a total of nine input variables including V_{Ki}, I_{jo}, S, V_{TH}, T_n with n=1 to 5. Each of the input variables can acquire a Boolean value of either 1 or 0 and has been coded according to Table 6.1.

Table 6.1: Input variables of FSM

Variable	Symbol	Condition	Coded Boolean Value
Input Voltage	V_{Ki}	$V_{Ki} > 0$	$V_{Ki} = 0$
		$V_{Ki} < 0$	$V_{Ki} = 1$
Output Current	I_{jo}	$I_{jo} > 0$	$I_{jo} = 0$
		$I_{jo} < 0$	$I_{jo} = 1$
State Change	S	$S = MS_1MS_1$	$S = 0000$
		$S = MS_2MS_2$	$S = 0100$
		$S = MS_1MS_0$	$S = 0010$
		$S = MS_2MS_0$	$S = 0001$
Input Voltage Threshold	V_{TH}	$V_{TH} > V_{in}^{MIN}$	$V_{TH} = 0$
		$V_{TH} < V_{in}^{MIN}$	$V_{TH} = 1$
Commutation Timer	T_n	$T_n < T_{comm}$	$T_n = 0$
	$n = 1, .., 5$	$T_n = T_{comm}$	$T_n = 1$

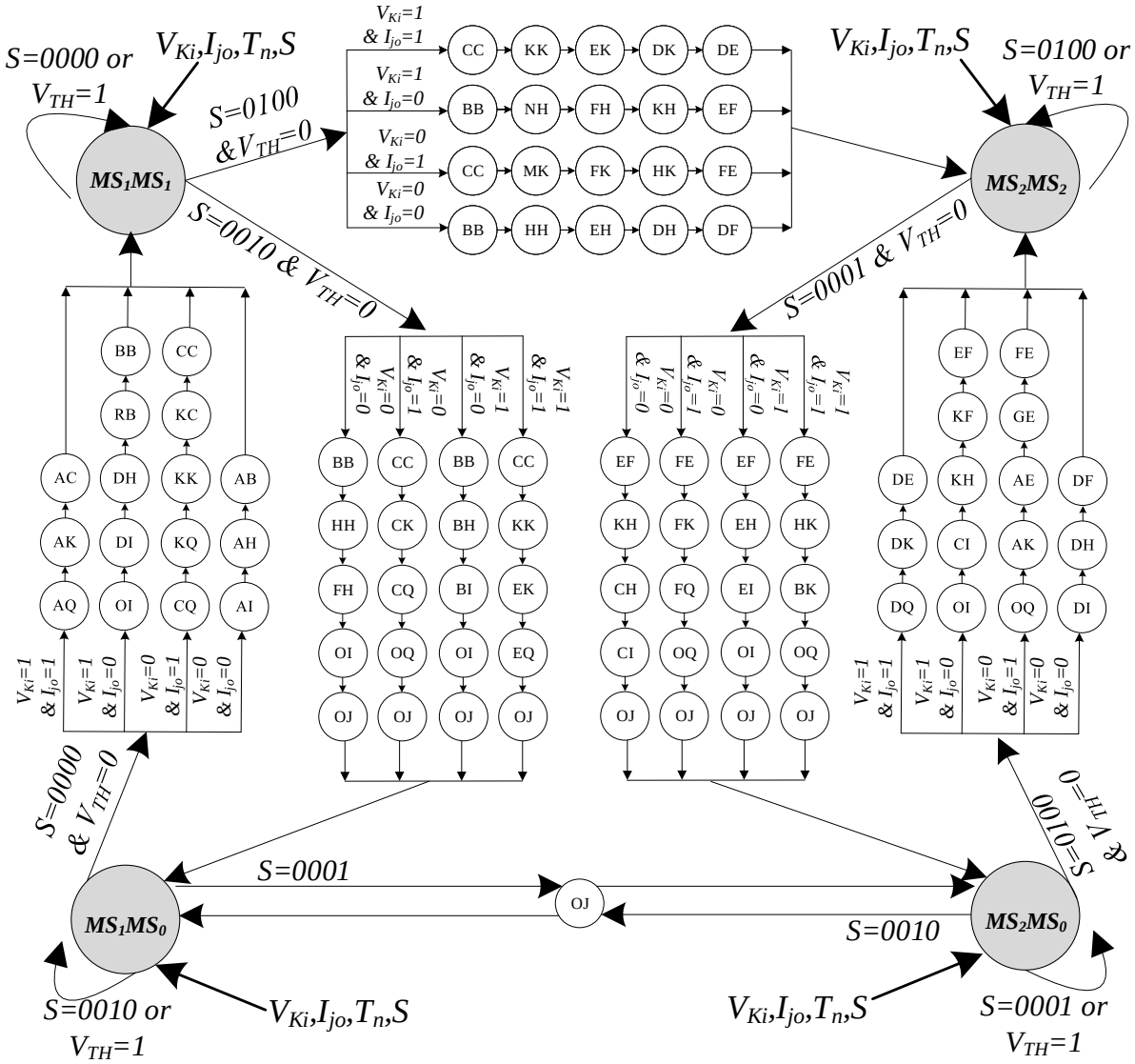


Figure 6.2: Finite State Machine (FSM) for implementing the Venturini Modulation on a cell of the MIMC

In Table 6.1 and Figure 6.2, the variable S is the state change variable which is responsible for holding information about the next state of the cell. Variable V_{TH} determines if the voltage is above the minimum voltage required to drive the leakage current I_L. Just as shown in Figure 5.21, the transition from one commutation state to another is controlled by the commutation timer T_n $(n = 1, ..., 5)$. Due to a large number of commutation states, the commutation timer variable has not been shown in Figure 6.2.

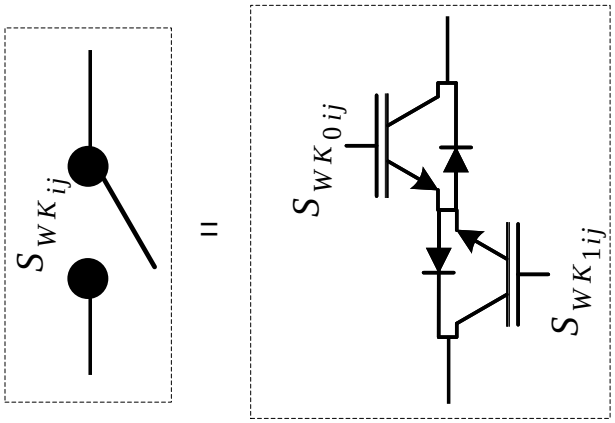


Figure 6.3: Equivalent Common-emitter configuration of a four-quadrant switch

In Figure 6.2, *'large grey circles'* denote the modulation or steady states, *'small circles'* indicate the commutation states and the arrows represent the commutation paths. The commutation states have been coded with letters where the first letter represents the commutation state (CS) matrix of the input side bridge while the second letter represents that of the output side bridge. Equation (6.1) shows the generic CS matrices for input and output side bridges containing a common-emitter configuration switch, shown in Figure 6.3, and the definitions of the CS matrices is given in equation (4.22) of Chapter 4.

$$\begin{aligned} CS_{Kij} &= \begin{bmatrix} S_{WK_{0ij}}S_{WK_{1ij}} & S_{YK_{0ij}}S_{YK_{1ij}} \\ S_{ZK_{0ij}}S_{ZK_{1ij}} & S_{XK_{0ij}}S_{XK_{1ij}} \end{bmatrix} \\ CS_{Koj} &= \begin{bmatrix} S_{WK_{0oj}}S_{WK_{1oj}} & S_{YK_{0oj}}S_{YK_{1oj}} \\ S_{ZK_{0oj}}S_{ZK_{1oj}} & S_{XK_{0oj}}S_{XK_{1oj}} \end{bmatrix} \end{aligned} \tag{6.1}$$

In order to observe the behaviour of the MIMC with the source based leakage tolerant commutation method, the FSM shown in Figure 6.2 was implemented in the simulation and discussed in the next section.

6.2 Open-loop Validation of the MIMC

6.2.1 Simulation Results

This section presents the results from a full three-phase to three-phase open-loop PLECS simulation of the MIMC when operated with the Venturini Modulation and leakage tolerant commutation method. The parameters used in the simulation are shown in Table 6.2.

Table 6.2: PLECS simulation parameters for validation of the MIMC

Parameter	**Symbol**	**Value**
Input Frequency	f_i	50 Hz
Output Frequency	f_o	60 Hz
Input Voltage Amplitude	V_{Ki}	200 V (PEAK)
Load Resistance	R	$10\,\Omega$
Load Inductance	L	10 mH
Switching Frequency	f_{sw}	10 kHz
Voltage Regulation Ratio	q	0.45
Leakage Inductance of Transformer	L_{leak}	$2.5\,\mu$H
Commutation Step	T_{comm}	$1\,\mu$s

The MIMC operates with a fundamental frequency of 50 Hz at the input and 60 Hz at the output. This test case has been selected to show the applicability of the proposed system in applications requiring frequency decoupling e.g. 50 and 60 Hz grids or 50, 25 and 16.7 Hz traction systems [118].

Figure 6.4 shows the three-phase input voltages V_{Ki} and the output currents I_{jo} in the three-phase to three-phase MIMC. By observing the period of the voltages V_{Ki} and currents I_{jo} in Figures 6.4(a) and 6.4(b), respectively, three-phase operation of the MIMC while achieving frequency adaptation can been confirmed. However, it must be seen from Figure 6.4(b) that the output currents I_{jo} are experiencing distortion which is associated with the leakage tolerant commutation scheme. To show the impact of the distortions, switching voltages and currents of a cell are shown in Figure 6.5.

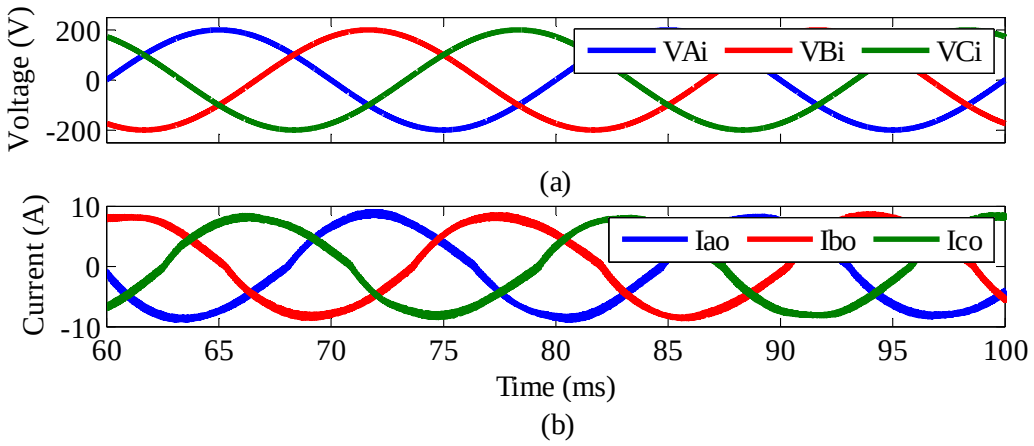


Figure 6.4: Open-loop simulated waveforms at the terminals of the proposed three-phase to three-phase MIMC with Venturini Modulation and leakage tolerant commutation method (a) Three-phase input voltages V_{Ki} (b) Three-phase output currents I_{jo}

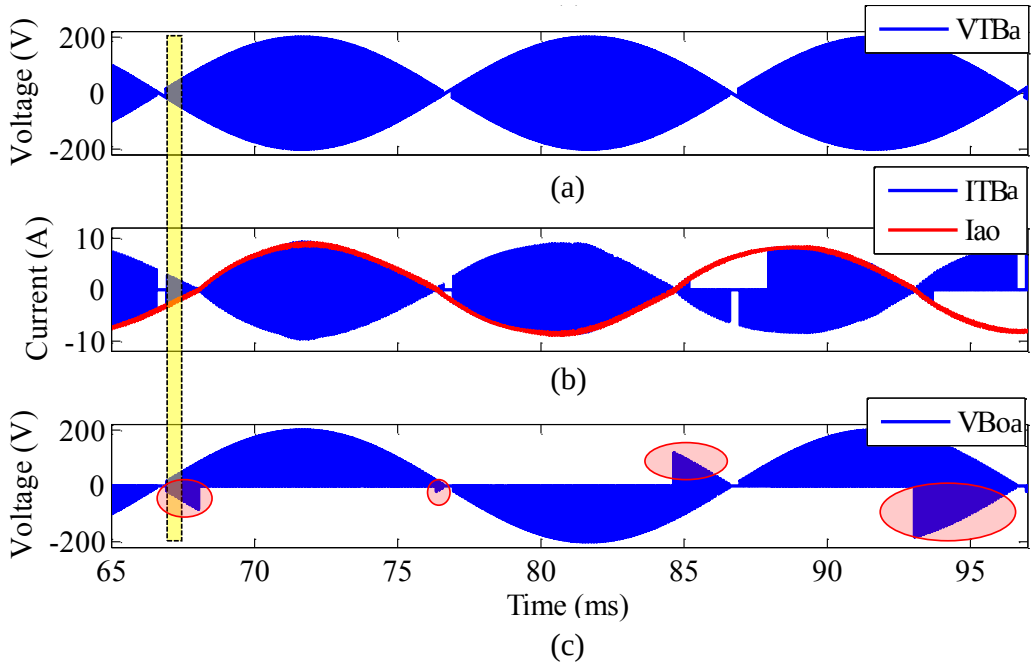


Figure 6.5: Open-loop simulated waveforms in the second cell of Figure 3.3 (a) Transformer voltage V_{TBa} (b) Transformer current I_{TBa} and output current I_{ao} (c) Output voltage V_{Boa}

In Figure 6.5, the red circles indicate the distortion in the cell output voltage V_{Boa} added due to the proposed current commutation method. To clearly show this, a zoomed view of the yellow highlighted region in Figure 6.5 is shown in Figure 6.6. Two state transitions, from MS_1MS_1 to MS_2MS_2 and then from MS_2MS_2 to MS_2MS_0, can be seen in Figure 6.6. Looking at the transition from MS_1MS_1 to MS_2MS_2, it can be seen that the output voltage of cell is being affected during the state transition and therefore, the commutation is non-ideal.

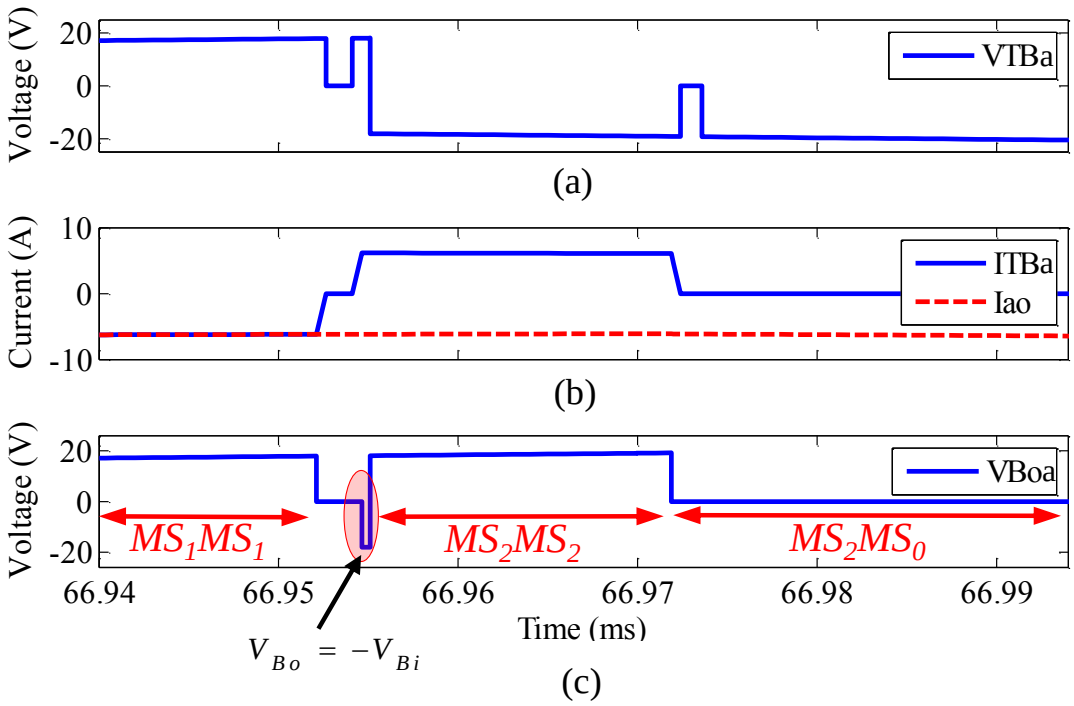


Figure 6.6: Zoomed view of the highlighted region in Figure 6.5, showing non-ideal commutations (f) Transformer voltage V_{TBa} (g) Transformer current I_{TBa} (h) Output voltage V_{Boa}

A comparable ideal case of commutation is shown in Figure 6.7. By comparing the output voltage V_{Boa} during the state transition MS_1MS_1 to MS_2MS_2 in both ideal and non-ideal case, shown in Figure 6.7 and Figure 6.6, respectively it can be seen the cell output voltage V_{Boa} in ideal case remains unaffected. However, this is not true in the non-ideal state transition, shown in Figure 6.6, where the V_{Boa} goes first to zero and then becomes $V_{Boa} = -V_{Bi}$ during the transition from MS_1MS_1 to MS_2MS_2. This is because several commutation states are applied during

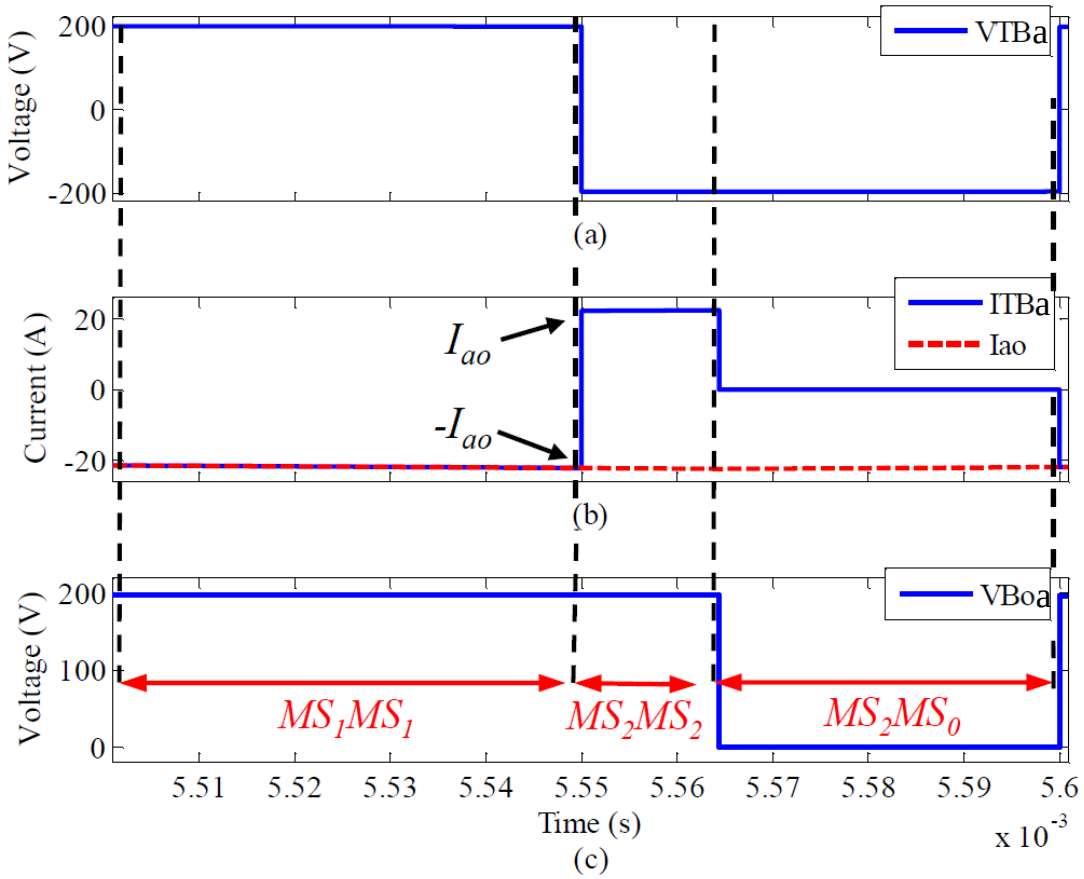


Figure 6.7: Example of an ideal transformer current in a single cell when operated with the 50% Venturini Modulation – zero leakage transformer (a) Transformer voltage V_{TBa} (b) Transformer current I_{TBa} (c) Output voltage V_{Boa}

the commutation process. For example, for this particular case of transition, from MS_1MS_1 to MS_2MS_2 with $V_{Bi} > 0$ and $I_{ao} < 0$, the commutation states applied by the FSM (Figure 6.2) are *'CC', 'MK', 'FK', 'HK', 'FE'*. The output voltage $V_{Boa} = 0$ during transition, from MS_1MS_1 to MS_2MS_2, because of the commutation states *'MK', 'FK'* which short circuit the output bridge and then becomes $V_{Boa} = -V_{Bi}$ when the commutation state is *'HK'* and leakage is charged while the commutation timer is waiting for the next commutation state *'FE'*. This behaviour of the output voltage of cell V_{Boa} to go zero first and then to $-V_{Bi}$, highlighted in red circle in Figure 6.6, is actually a distortion associated with the source based leakage tolerant commutation scheme. Each cell of the MIMC will experience similar distortions in the generic cell output voltage V_{Koa}.

The cell output voltages of top, middle, and bottom cell i.e. V_{Aoa}, V_{Boa}, V_{Coa}, can be seen in Figure 6.8(a)-(c) in which the commutation-associated distortions are highlighted using red circles. The final output voltage V_{ao}, sum of V_{Aoa}, V_{Boa}, V_{Coa}, is shown in Figure 6.8(d).

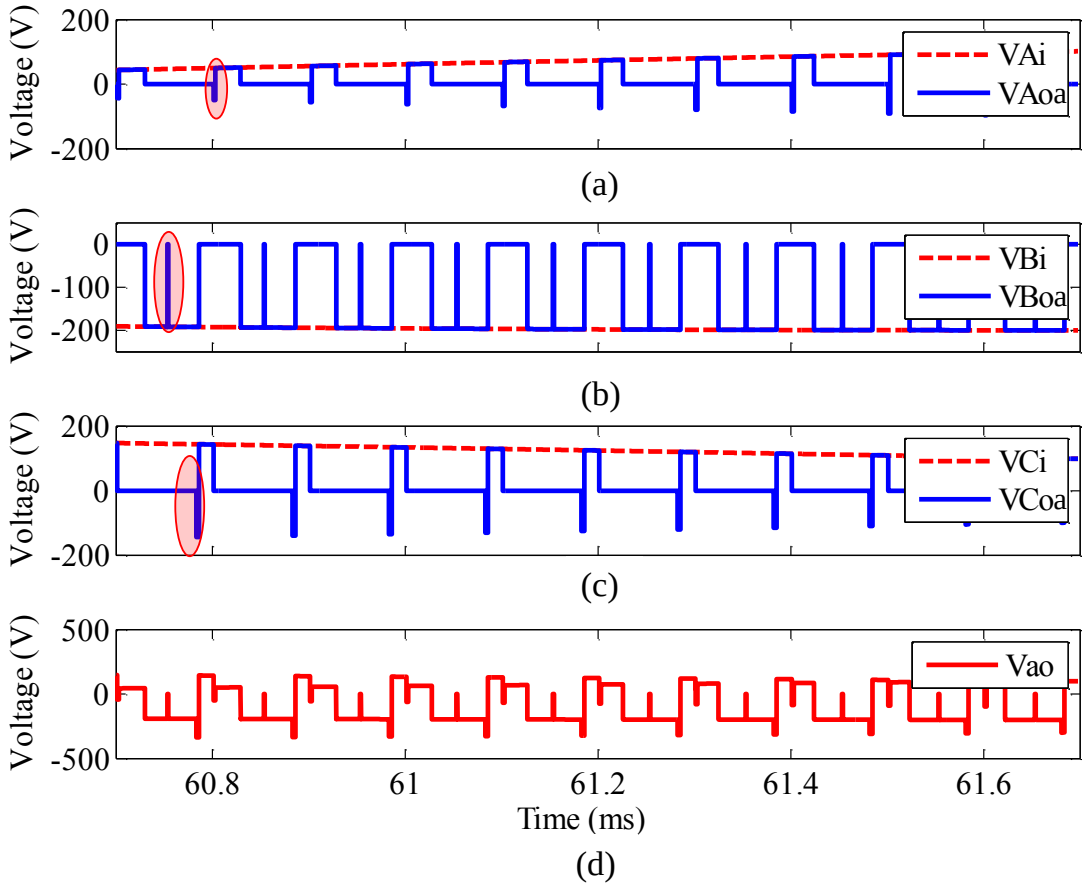


Figure 6.8: Cell output voltages V_{Koa} and final output phase voltage V_{ao} when operated with non-ideal (leakage tolerant) commutation and 50% Venturini Modulation. (a) Output voltage V_{Aoa}. (b) Output voltage V_{Boa}. (c) Output voltage V_{Coa}. (d) Output phase voltage V_{ao}.

It can be seen from Figure 6.8(d) that the open-loop phase output voltage V_{ao} has commutation-related distortions because V_{ao} is the sum of output cell voltages V_{Koa}. This commutation-related distortion at the output of the MIMC must be quantified. In order to quantify the distortion associated with the commutation, the MIMC was operated with the ideal as well as the non-ideal commutation scheme and the THD of the open-loop output current I_{ao} was observed at various switching frequencies

as shown in Figure 6.9. Note that a fixed commutation step T_{comm} was used for simplicity and the open-loop output current I_{ao} is filtered using a 10 mH inductor.

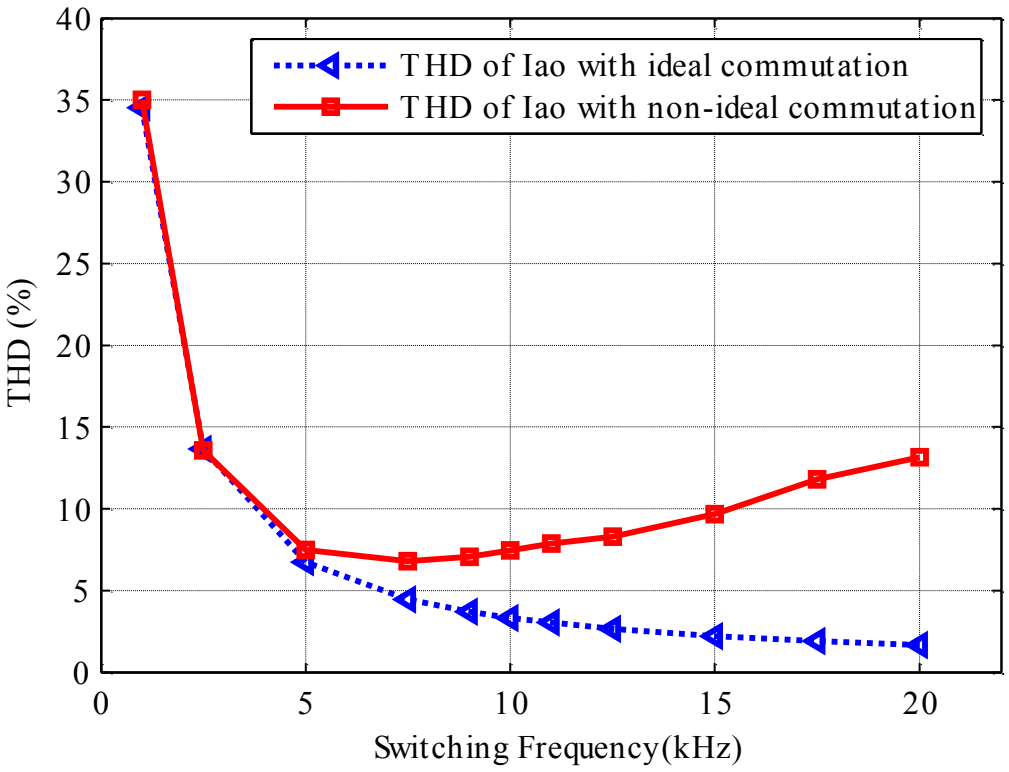


Figure 6.9: Switching frequency vs. Total Harmonic Distortion (THD) with a fixed commutation time T_{comm} and filter inductor L =10 mH in the open-loop MIMC

It can be observed from Figure 6.9 that in the ideal case, the THD of the output current I_{ao} always has an inverse relation with the switching frequency f_{sw} but this is not true for non-ideal case. Up to a switching frequency f_{sw} of 5 kHz, the THD of both cases remains almost same, as the fixed commutation time is negligible compared to the switching period, but with the further increase of switching frequency f_{sw}, the fixed commutation time becomes a significant part of the switching period therefore causing the THD to increase. The observed optimum range of operation for the MIMC is between 5 and 10 kHz. Within the optimum range, a higher switching frequency f_{sw} will be preferred as the size of the magnetic components, which in the case of the MIMC is the MF transformer, will reduce. Therefore, a switching frequency f_{sw} of 10 kHz was selected in simulation and experiment. Note that the THD curve, shown in Figure 6.9, is obtained by keeping a fixed value of leakage inductance.

6.2.2 Experimental Setup and Results

The experimental setup used for validation of the leakage tolerant commutation, shown in Figure 5.15, was a single-cell of the MIMC i.e. single-phase to single-phase AC/AC converter. In order to validate the operation of the MIMC, a minimum three-phase to single-phase version of the MIMC is required as shown in Figure 6.11. Figure 6.11 also shows the points where the waveforms were observed.

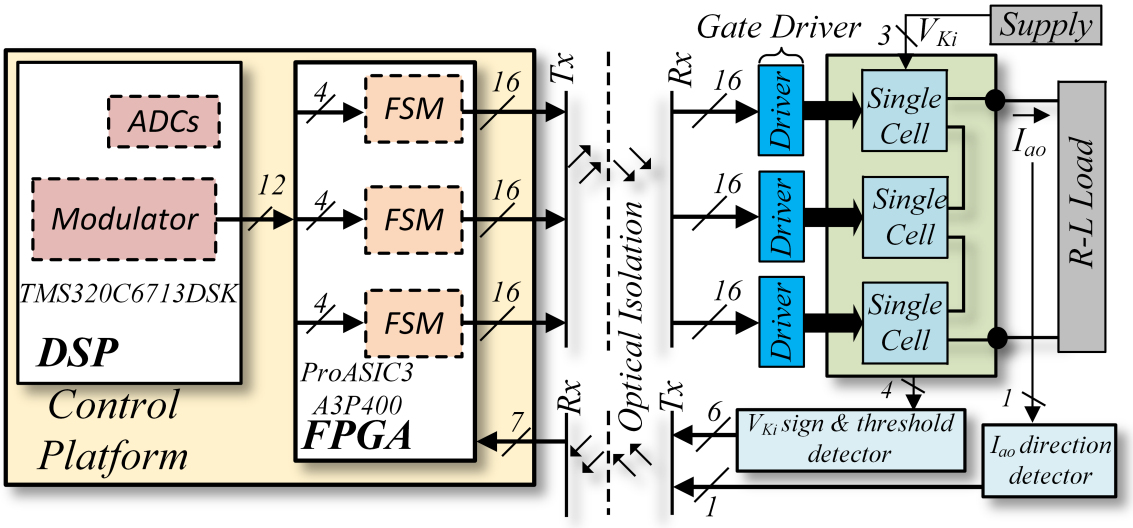


Figure 6.10: Block diagram of the experimental setup for the three-phase to single-phase MIMC topology

The block diagram of the experimental setup for a three-phase to single-phase MIMC topology is shown in Figure 6.10. Since the state change variable S in the FSM, shown in Figure 6.2, is a four-bit variable, four modulation commands per cell and a total of twelve modulation commands for three-cells are generated by the DSP as shown in Figure 6.10. These twelve modulation commands implement the switching functions, given in (3.11)-(3.13), for the 50% Venturini Modulation. The twelve modulation signals are fed to the FPGA where a VHDL based FSM generates sixteen independent gate signals per cell, based on the direction of output current I_{ao} and polarity of input voltages V_{Ki}, to perform the leakage tolerant commutation. A total of 48 independent gate signals for three cells, generated by the FPGA, are then optically transmitted to the gate driver boards of the SEMIKRON SKM150GM12T4G IGBT modules.

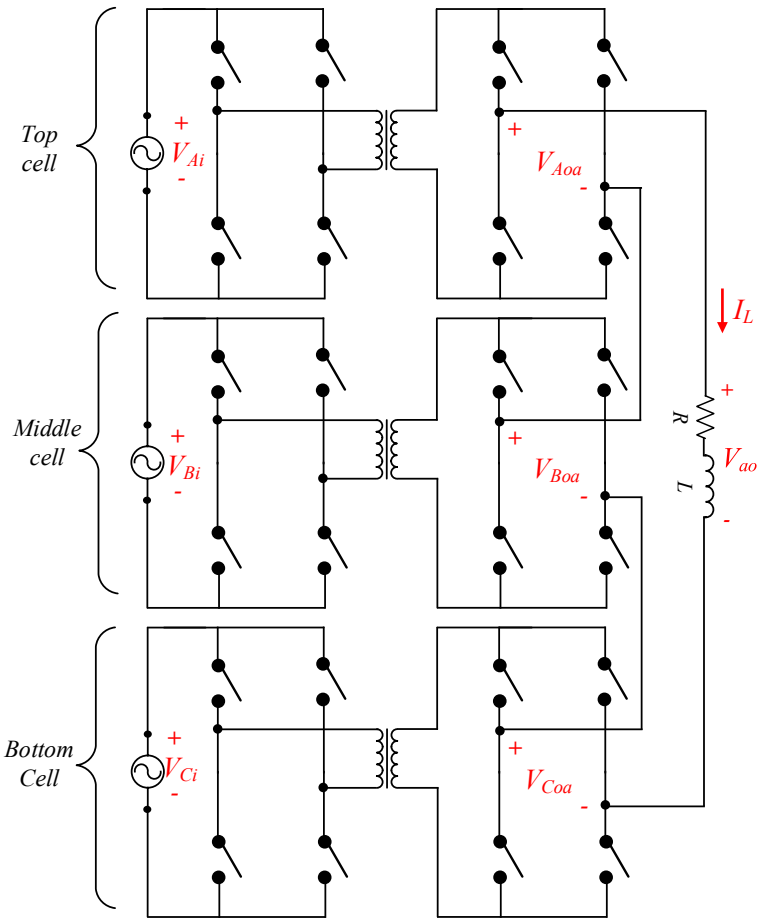


Figure 6.11: Three-phase to single-phase version of the MIMC topology - showing the points where voltages and currents were measured in experiment

The V_{Ki} *sign and threshold detector* block receives four electrical cables as the input voltage V_{Ki} is a three-phase four-wire system. The said block feeds six optical signals to the FPGA, from which three contain the information of sign and the remaining three contain the information of the threshold. The threshold of the input voltages is detected to avoid commutation when the input voltage magnitude is below the set threshold. This can be observed in the simulation result of Figure 6.5(b) where current I_{TB} is zero i.e. no commutation is performed at the instance when the magnitude of voltage V_{TB} is close to zero. The value of threshold can be set by taking into account the peak value of current I_{ao}, leakage inductance L_{leak}, commutation time T_{comm} and using simple formula $V_{TH} = \frac{\Delta I_{ao} L_{leak}}{T_{comm}}$ where $\Delta I_{ao} = 2I_{ao}$ as leakage current changes between I_{ao} and $-I_{ao}$.

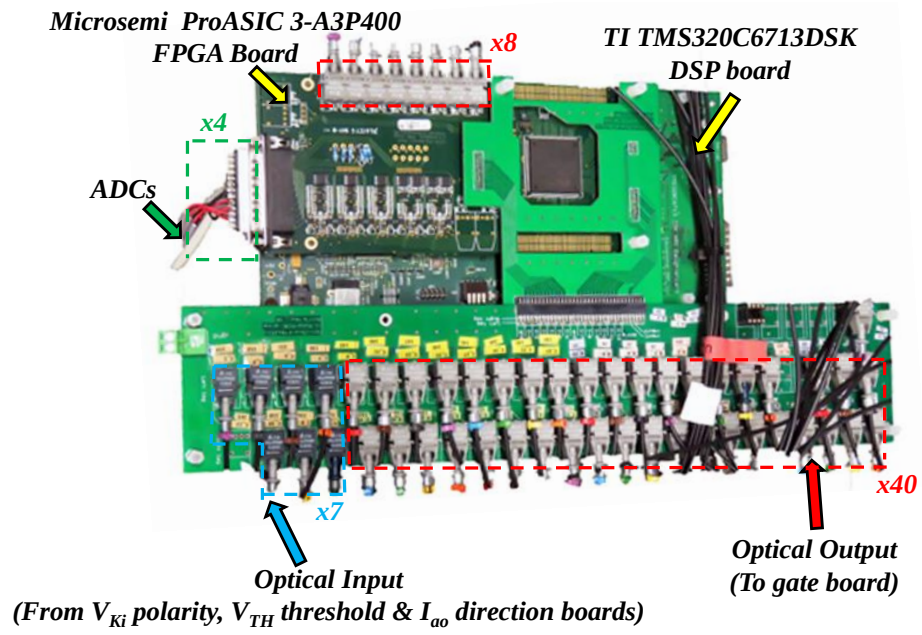


Figure 6.12: Photo of the DSP/FPGA based control platform with 48 optical transmitters and seven optical receivers

The I_{ao} *direction detector* block is connected in series with the output RL load. This block feeds an optical signal to the FPGA. Therefore, the FSM in the FPGA receives a total of seven signals, six from the V_{Ki} *sign and threshold detector* block and one from the I_{ao} *direction detector* block, as shown in Figure 6.10.

To be able to receive seven optical signals and transmit 48 optical signals, the control platform, shown in Figure 5.3 was extended. The extended control platform is shown in Figure 6.12. A total of four ADC channels, three for reading the three-phase voltages V_{Ki} and one for the single-phase output current I_{ao}, are used as shown in Figure 6.12. The instantaneous value of the single-phase output current I_{ao} is required for achieving a closed-loop current control of the MIMC. However, the information about the three-phase input supply V_{Ki} is required for generating modulation duty cycles D_{Kj} (3.5). Although, instantaneous values of the supply voltage V_{Ki} can be fed directly to the duty cycles D_{Kj} modulation of the MIMC but this can cause distortions in the output voltage of the MIMC in the case when the supply voltage is distorted. Therefore, the information, including angle and frequency of the three-phase input supply V_{Ki}, can be extracted using a Phase-Locked Loop (PLL) as shown

in Figure 6.13 [119].

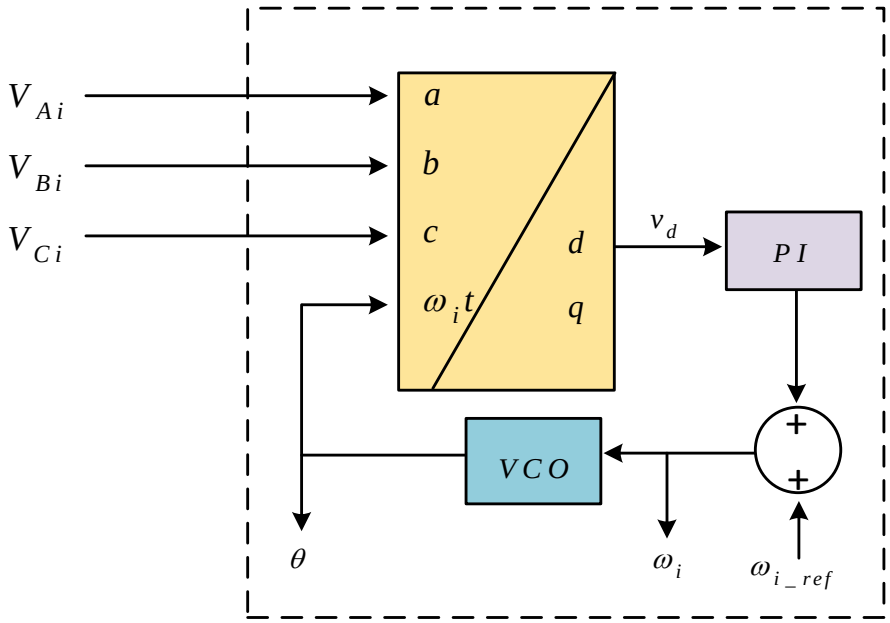
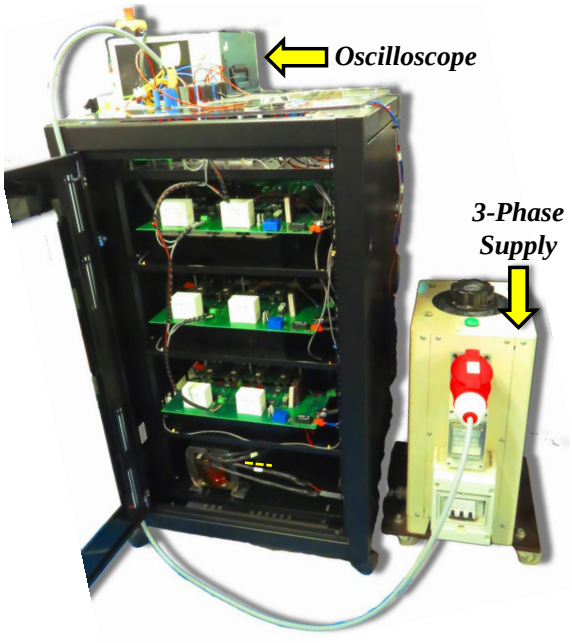


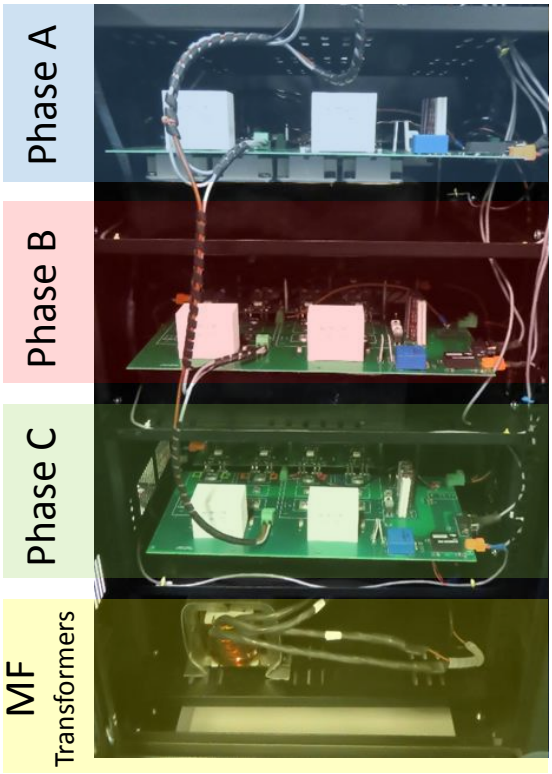
Figure 6.13: Structure of the Phase-Locked Loop (PLL) system

Note that the hardware implementations of the V_{Ki} *sign and threshold detector* and I_{ao} *direction detector* blocks have already been discussed in Chapter 5 under Sections 5.1.4 and 5.1.5, respectively. The PCB for a three-phase input voltage V_{Ki} was built by repeating the PCB shown in Figure 5.11 of Section 5.1.4 and is not re-shown in this section for the sake of conciseness. The design of the MF transformers remains the same as presented in Section 5.1.6 and is repeated to have three MF transformers for three-phase to single-phase MIMC. The experimental rig built is shown in Figure 6.14(a).

The three-phase input V_{Ki} to the experimental rig is supplied using a variac as shown in Figure 6.14(a). The thee cells (for Phase A, B, C) and the MF transformers are stacked horizontally in a server rack as shown in Figure 6.14(b). In order to experimentally validate open-loop operation of the MIMC, the 6kW proof of concept prototype, shown in Figure 6.14, was operated with the parameters given in Table 6.3 and the observed experimental waveforms at the terminals of the MIMC are shown in Figure 6.15.



(a) The experimental setup including three-phase input voltage V_{Ki} variable AC supply and oscillioscope



(b) Front of the rack showing the stacked top (Phase A), middle (Phase B) and bottom (Phase C) cells and MF transformers

Figure 6.14: Photo of the experimental rig for three-phase to single-phase MIMC topology

Table 6.3: Experimental test parameters for validation of the MIMC

Parameter	Symbol	Value
Input Voltage Amplitude	V_{Ki}	120 V (RMS)
Frequency at the input side	f_i	50 Hz
Frequency at the output side	f_o	60 Hz
Switching Frequency	f_{sw}	10 kHz
Load Resistance	R	$1.5\,\Omega$
Load Inductance	L	10 mH
Input Filter Capacitance	C_F	$30\,\mu$F

From Figure 6.15(a), it is important to note that the fundamental component of all the three-phase input voltages V_{Ki} is at 50 Hz whereas that of the filtered output current I_{ao} is at 60 Hz. Current I_{ao} is the average of the pulse-width-modulated output voltage V_{ao}. This confirms that the MIMC is able to achieve input-output frequency decoupling by following equation (3.22) as the components at ω_i and $2\omega_i \pm \omega_o$ are cancelled due to the phase difference of $\frac{2\pi}{3}$, leaving only a single component at ω_o which is 60 Hz in the case shown in Figure 6.15. Note that the experimental setup is only a three-phase to single-phase MIMC hence the input side currents I_{Ki} are not sinusoidal, causing distortions in the input voltages V_{Ki} which will be mitigated in the full three-phase version.

Figure 6.16 shows several cycles of the modulated output voltages of the individual cells V_{Koa} as well as the sum of these voltages which is the output voltage V_{ao}. At any time *'t'* the output voltage V_{ao} is the sum of the cell voltages V_{Koa} and follows $V_{jo} = \sum_{K=A,B,C} V_{Koj} = V_{Aoj} + V_{Boj} + V_{Coj}$.

To clearly show that the he final output voltage V_{ao} is the sum of cell voltages V_{Koa}, a zoomed view of yellow highlighted region of Figure 6.16 is shown in Figure 6.17. Figure 6.17 confirms that the experimental waveforms of V_{Ao}, V_{Bo}, V_{Co} and their sum V_{ao} matches with the simulated waveforms presented in Figure 6.8. Thus, the results shown in Figure 6.15-6.16 have experimentally validated the open-loop operation of the proposed MIMC. A single switching period T_S has been shown in Figure 6.17 to

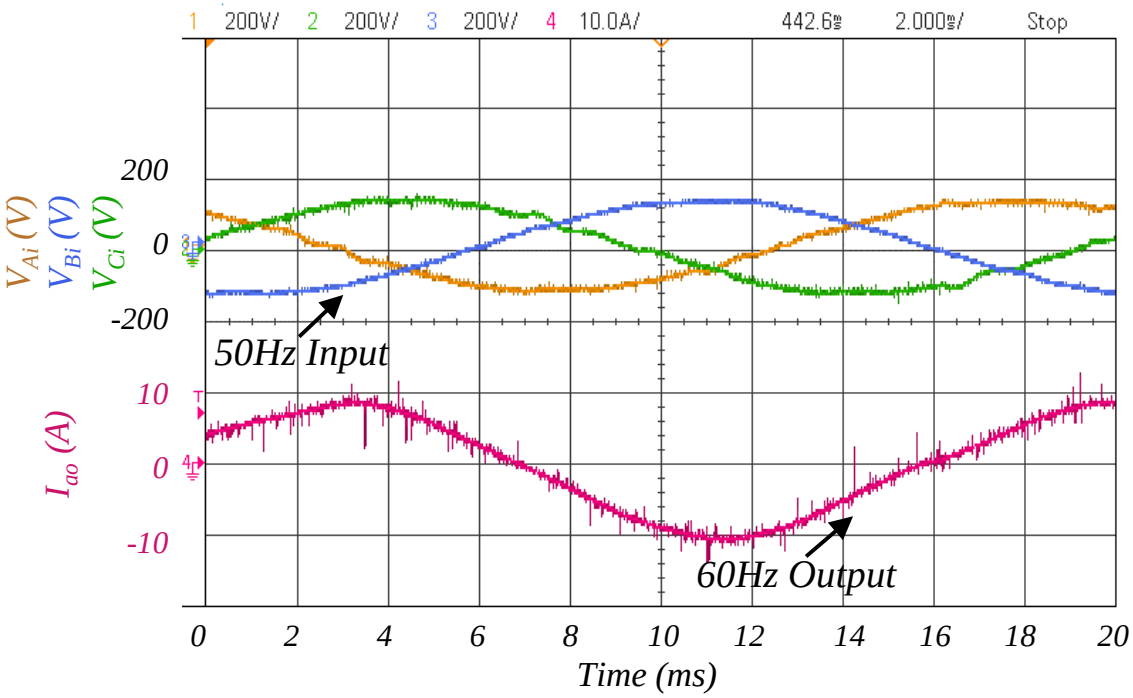


Figure 6.15: Three-phase input voltages V_{Ki} at 50 Hz and single-phase output current I_{ao} at 60 Hz in open-loop three-phase to single-phase MIMC

show that the duty cycles D_{Kj} are arranged in the pattern of D_{Aa}, D_{Ba}, D_{Ca} and are in accordance with the arrangement given in Figure 3.5.

Note that the red regions in the waveforms shown in Figure 6.17 indicate the distortion added in the output voltages of cells V_{Aoa}, V_{Boa}, V_{Coa} due to the commutation. These commutation related distortions in the proposed MIMC topology are analogous to the dead-time distortion in the standard two-level inverters. To compensate for these commutation-related distortions and to enhance the degree of controllability, a current-controller must be added.

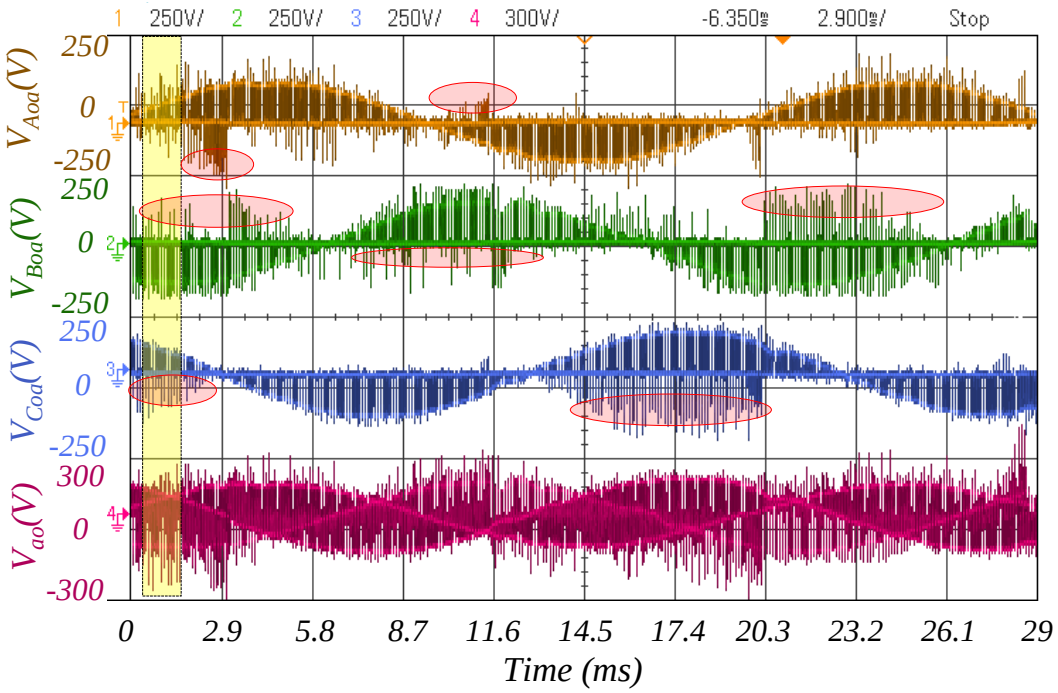


Figure 6.16: Individual cell voltages V_{Koa} and the final output voltage V_{ao} in open-loop three-phase to single-phase MIMC

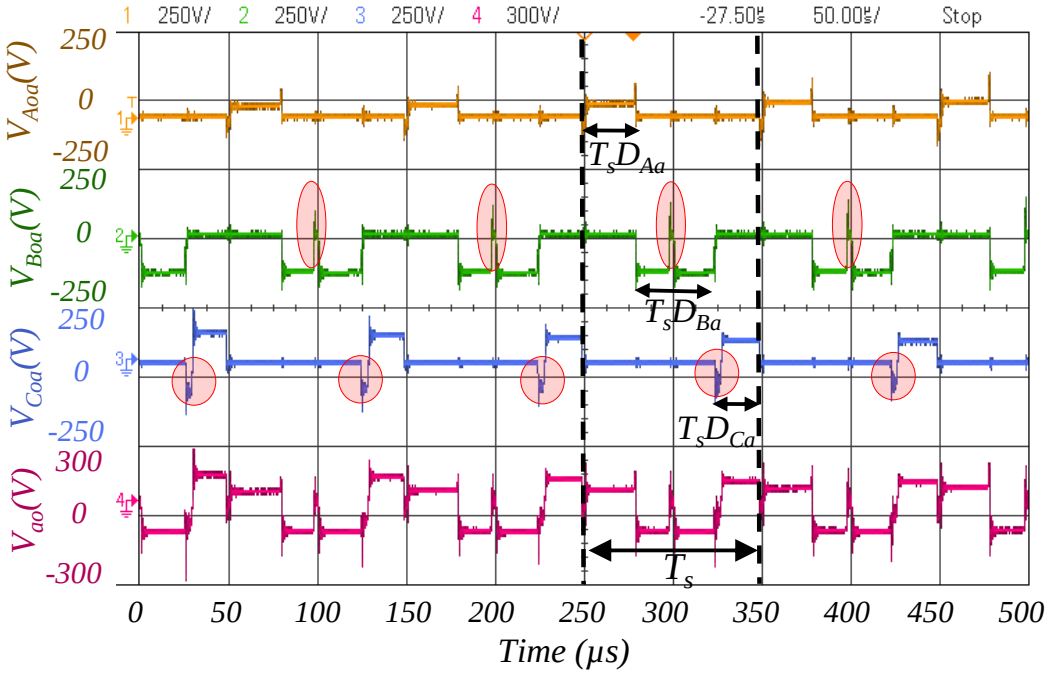


Figure 6.17: Zoomed view of Figure 6.16 showing several switching periods T_S of the individual cell voltages V_{Koa} and the final output voltage V_{ao} in open-loop three-phase to single-phase MIMC

6.3 Closed-loop Control of the MIMC

The choice of the controller can be made by observing the harmonic spectrum [120] of the open-loop output current I_{ao_open}. Figure 6.18 shows the simulated harmonic spectrum of the open-loop output current I_{ao_open}. From Figure 6.18, it can be seen that the leakage tolerant commutation is causing harmonics at the odd multiples of the fundamental, i.e. at 180 Hz, 300 Hz and so on. Therefore, the effect of leakage tolerant commutation is analogous to dead-time in the standard two-level inverter [120, 121]. Moreover, it can also be seen that some low frequency harmonics are also present in the open-loop output current I_{ao_open}. To compensate for the harmonics and to be able to track a sinusoidal current, a Proportional-Resonant (PR) controller was investigated for the MIMC due to its periodic-disturbance rejection capability [122].

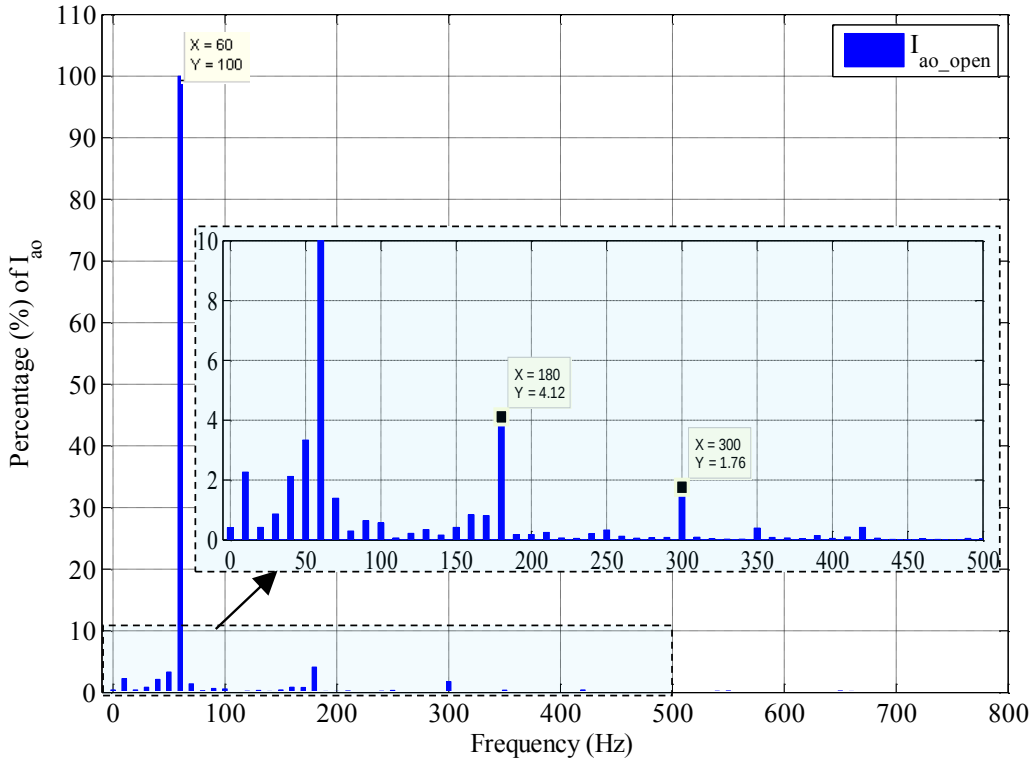


Figure 6.18: Harmonic spectrum of the open loop output current I_{ao_open} in the MIMC (simulation)

6.3.1 Proportional-Resonant (PR) Controller

Although a PR controller offers good harmonic rejection capability [123] this capability can further be enhanced by inserting gains at particular frequencies. This can be achieved by using multi-resonant controllers which are tuned at desired frequencies and are connected in parallel [124]. If third and fifth harmonics, present in the open-loop output current I_{ao_open}, are to be compensated, then the transfer function of a PR controller [122] can be extended to a form given in (6.2) where $K_P = 2L\omega_c$, $K_{R1} = L{\omega_c}^2 + 2R\omega_c$, $K_{R2} = R{\omega_c}^2 - 2L\omega_c{\omega_o}^2$.

$$G_{PR}(s) = K_P + \frac{K_{R2}}{s^2 + (\omega_o)^2} + sK_{R1}\left[\frac{1}{s^2 + (\omega_o)^2} + \frac{1}{s^2 + (3\omega_o)^2} + \frac{1}{s^2 + (5\omega_o)^2}\right] \quad (6.2)$$

The block diagram of the PR based current-controller is shown in Figure 6.19 where V'_{ao} is the required output voltage to track the reference current I_{ao_ref}. The required output voltage V'_{ao} is fed to the MIMC's duty cycle equation given in (3.5). A Bode plot of the loop gain $\frac{G_{PR}(s)}{Ls+R}$ of the multi-resonant current controller is shown in Figure 6.20.

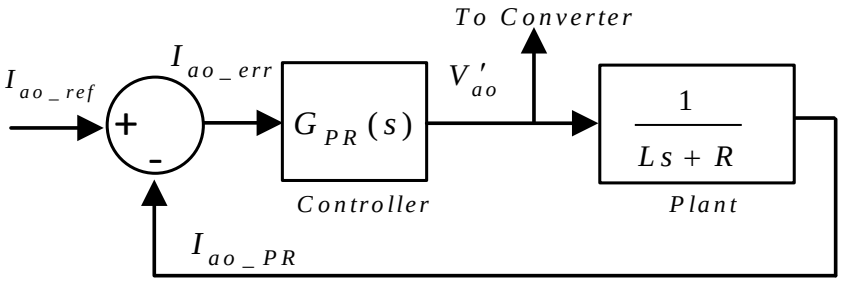


Figure 6.19: Block diagram of PR based current-controller for MIMC

The design of the PR current-controller was first validated using PLECS simulation. Figure 6.21 shows the effect of the designed PR controller on the output current I_{ao} when the PR controller is activated at t=0.3ms. It can be seen from Figure 6.21 that the PR controller is enhancing the current quality. To clearly show the improvement, the harmonic spectrum of the closed-loop current I_{ao_PR} is shown in Figure 6.22.

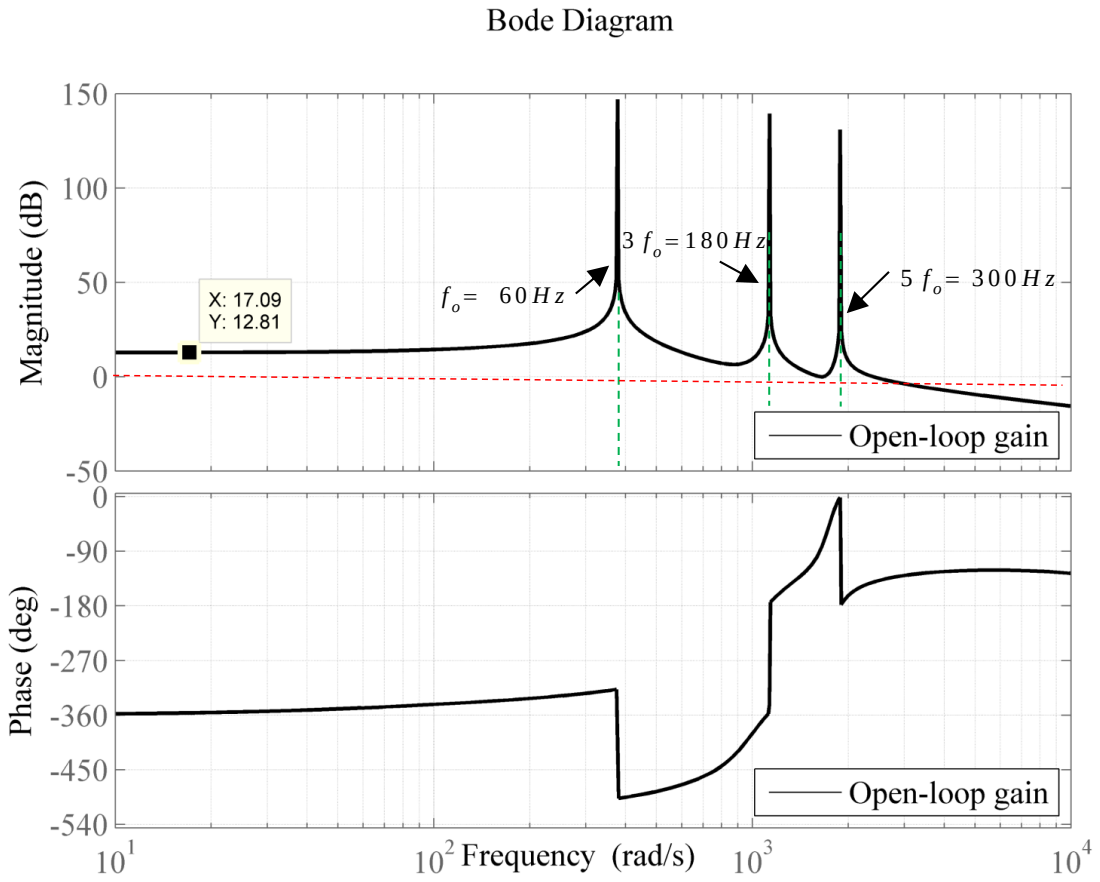


Figure 6.20: Bode diagram of the loop gain $\frac{G_{PR}(s)}{Ls+R}$ in the PR based current-controller with $\omega_c = 250\pi$ and $\omega_o = 120\pi$

It can be seen from the harmonic spectrum, shown in Figure 6.22, that the magnitudes of the third and fifth harmonics have reduced from 4.1% and 1.76%, respectively to 0.03% and 0.02%, respectively when compared with the harmonic spectrum of the open-loop current I_{ao_open} shown in Figure 6.18. In addition to this, it can also be seen that the DC component and other low frequency harmonics are also being partially compensated. This is because the designed PR controller has some gain at DC and low frequency which has been highlighted as a data point in the bode diagram shown in Figure 6.20. Figure 6.22 has confirmed the feasibility of the designed PR controller using simulation.

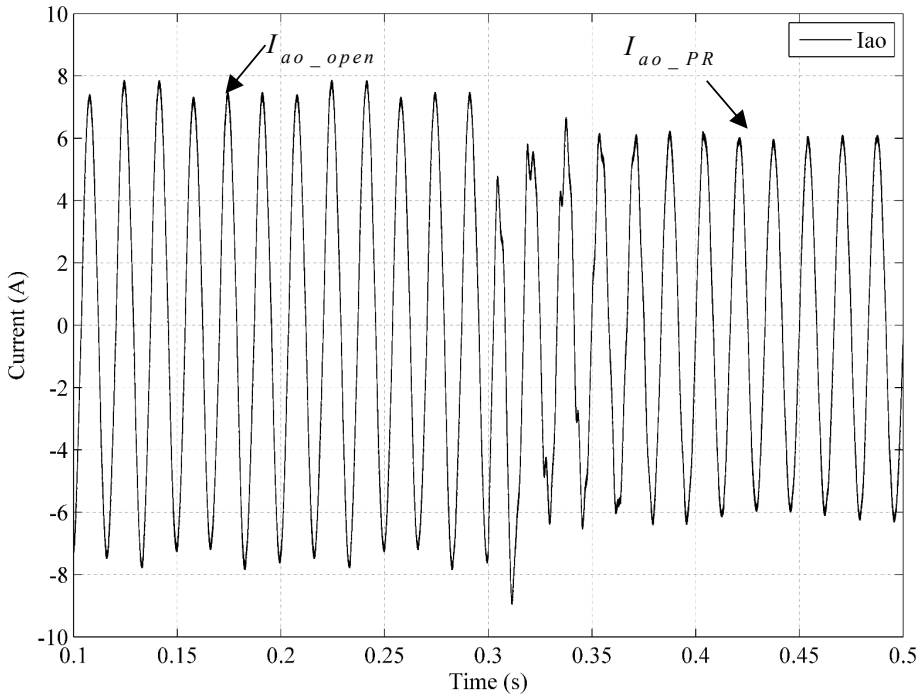


Figure 6.21: The output current I_{ao} in the MIMC when PR controller is activated at t=0.3ms (simulation)

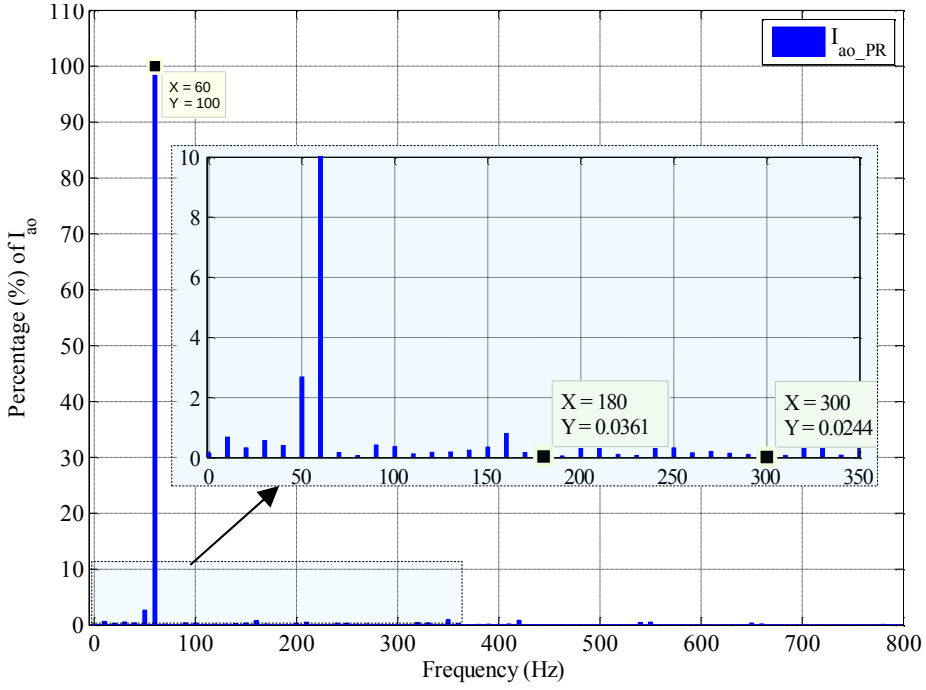


Figure 6.22: Harmonic spectrum of the closed-loop output current I_{ao_PR} in the MIMC (simulation)

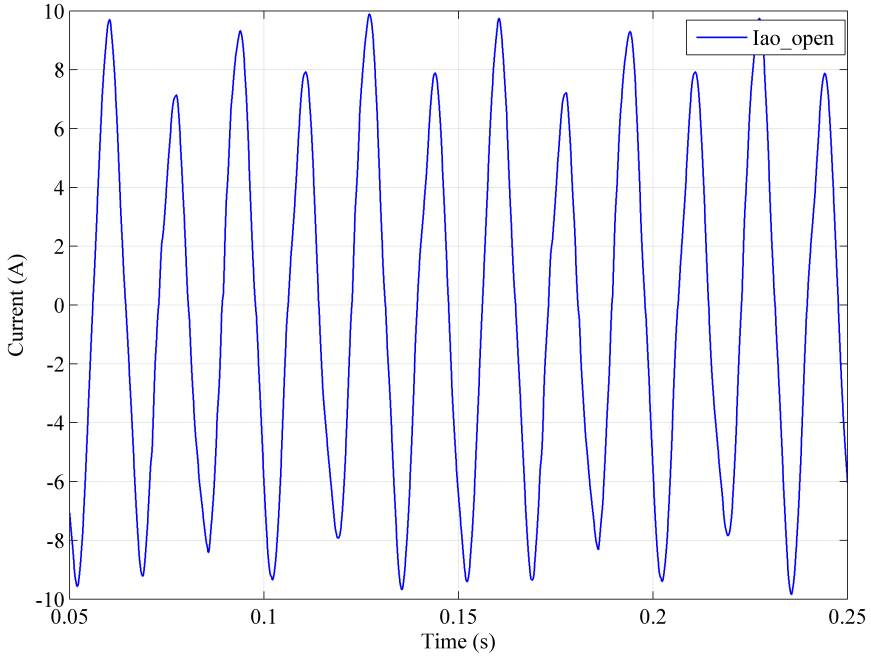


Figure 6.23: The open-loop output current I_{ao_open} in the MIMC (experiment)

To test out the designed PR controller, the s-domain transfer function, given in (6.2), was discretised to a z-domain model using $T_s = 1/f_{sw}$ and Tustin's approximation. The discretised form of the PR controller, given in (6.3), was implemented in the DSP to experimentally validate the designed PR controller for the MIMC.

$$G_{PR}(z) = \frac{0.0842z^7 - 0.404z^6 + 0.696z^5 - 0.351z^4 - 0.413z^3 + 0.684z^2 - 0.367z + 0.071}{z^7 - 6.936z^6 + 20.66z^5 - 34.29z^4 + 34.21z^3 - 20.53z^2 + 6.862z - 0.985} \tag{6.3}$$

The experimental waveforms of the open-loop current I_{ao_open} and closed-loop current I_{ao_PR} are shown in Figure 6.23 and Figure 6.24, respectively. The harmonic spectrums of these are shown in Figure 6.25 and Figure 6.26, respectively. By comparing the harmonic spectrums of the open and closed-loop system, shown in Figures 6.25 and 6.26, it can be seen that the PR controller is compensating for the third and fifth harmonics. Although, the experimental open-loop current I_{ao_open} is experiencing a DC component of 4.22%, the PR controller is partially compensating for it by reducing it to a value of 1.17% as seen in Figure 6.26. A THD of 9.1% in I_{ao_open} rather than a THD of 4.5% in I_{ao_PR} was observed.

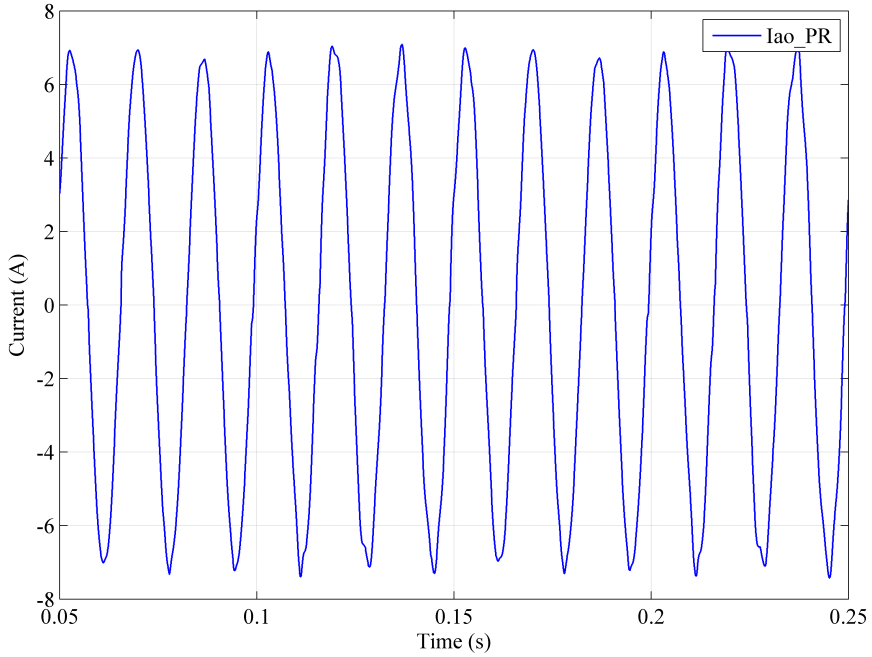


Figure 6.24: The closed-loop output current with PR controller I_{ao_PR} in the MIMC (experiment)

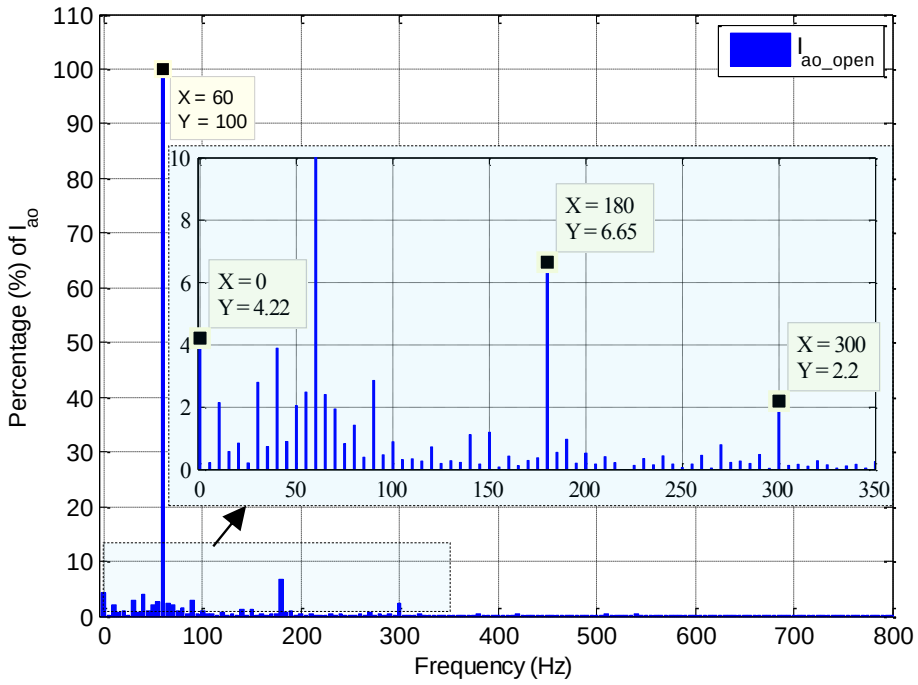


Figure 6.25: Harmonic spectrum of the open-loop output current I_{ao_open} in the MIMC (experiment)

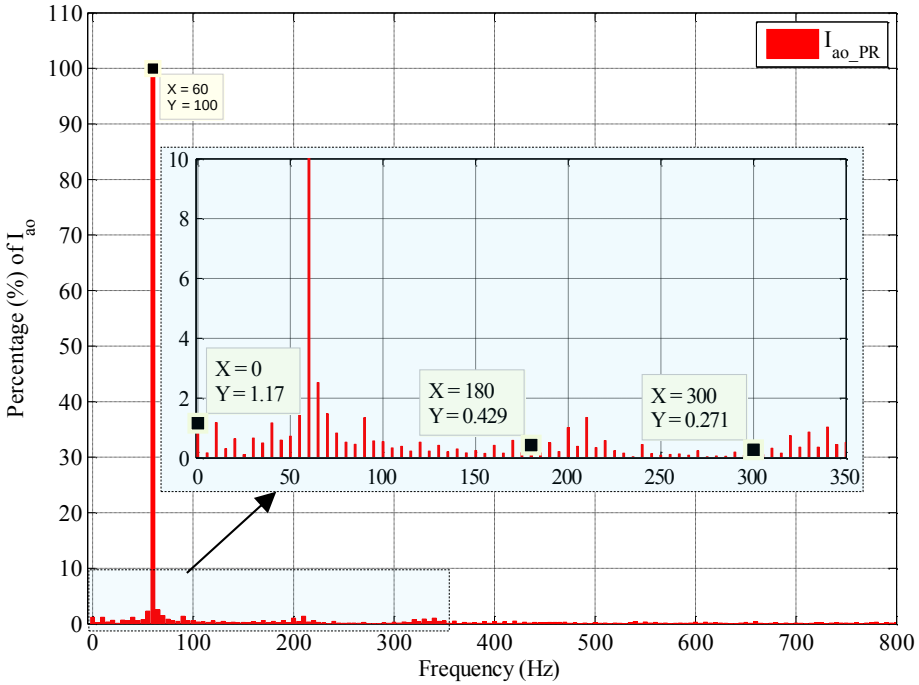
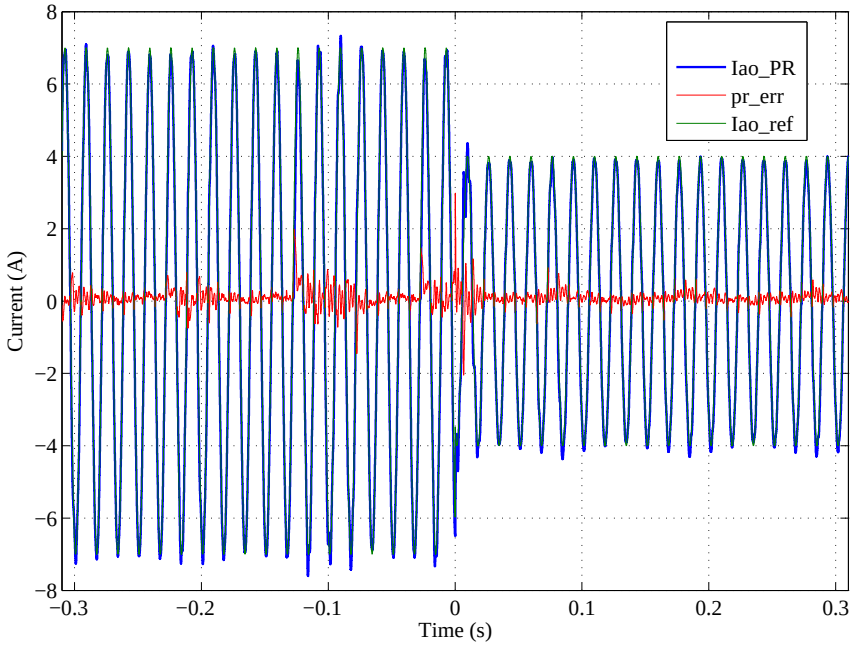


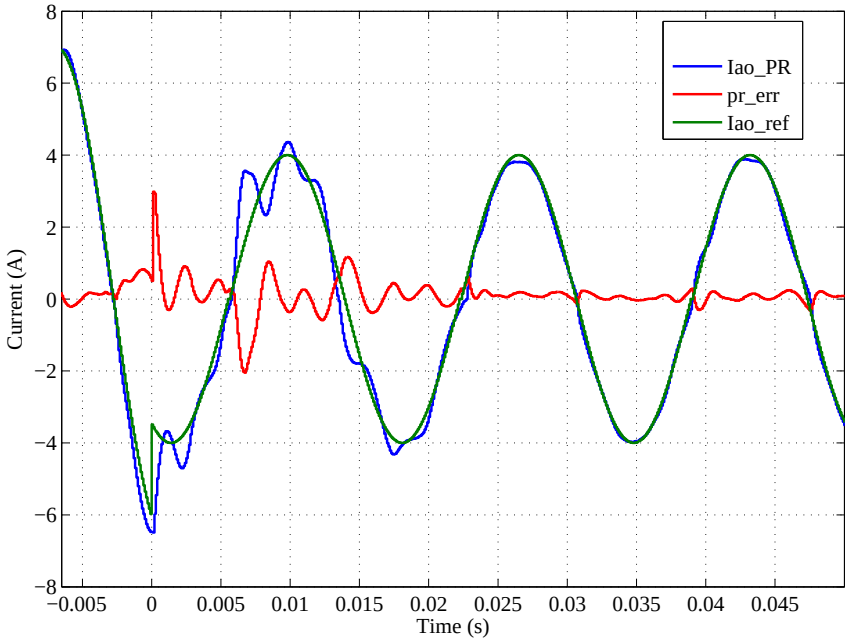
Figure 6.26: Harmonic spectrum of the closed-loop output current I_{ao_PR} in the MIMC (experiment)

Furthermore, the response of the PR based closed-loop system as a result of step change in current reference I_{ao_ref} from 7A to 4A was observed. The experimental waveforms are shown in Figure 6.27(a). It can be seen from Figure 6.27(a) that the system is stable and tracks the reference current I_{ao_ref}. A zoomed view of Figure 6.27(a), shown in Figure 6.27(b), shows experimental transient response.

Figure 6.27(b) has some additional distortions near the zero-crossings of the current which are due to the direction of the current I_{ao_PR} being detected incorrectly when the magnitude is too small, causing selection of the wrong commutation path in the FSM shown in Figure 6.2. This is due to the limitations of the direction detection hardware (shown in Figure 5.10). However, the controller is taking necessary action to compensate these distortions. Note that the experimental results shown in Figure 6.27 validate the application of the PR current-controller to the MIMC. However, a modern control method known as Modulated Model Predictive Control (M2PC) can also be investigated for the MIMC due to its capabilities which include low THD [125, 126] and fast dynamic response.



(a) Step change with PR controller



(b) Transient response with PR controller

Figure 6.27: Experimental waveforms during step response of the closed-loop output current as a result of a PR controller (a) Step change in current reference I_{ao_ref} from 7A to 4A at t=0s (b) Zoomed view of Figure 6.27 showing transient response

6.3.2 Modulated Model Predictive Control (M2PC)

The Model Predictive Control (MPC) utilises the model of the plant to predict the behaviour of its controlled variables. Information of the controlled variables is then fed to the controller in order to obtain optimal actuation, according to a predefined optimization criterion [127].

Traditionally there are two types of MPC which include continuous set MPC and finite set MPC [128]. One of the main drawbacks of these traditional types of MPC is that they lack a modulator causing a larger ripple in the system waveforms, which, in turn, requires variable switching frequency [125]. In order to overcome this limitation, an approach, named Modulated Model Predictive Control (M2PC) which combines the MPC and the modulator to obtain a fixed switching frequency, is recently proposed [125]. M2PC allows the retention of all of the desired characteristics of the traditional MPC but gives an increased performance in terms of power quality [126]. In addition to the fixed switching frequency, the M2PC also allows the use of a limited number of switching states. This can be beneficial for a system with a large number of switching states such as a MIMC because the cost function will otherwise be evaluated for all possible states of the converter which will require high processing power from the DSP [129].

For M2PC based current control of the MIMC, the output current I_{ao} can be discretised using Euler approximation method as shown in (6.4). In equation (6.4, T_S denotes the switching period whereas n represents the number of switching period which can take values $n = 0, 1, 2, ..., \infty$. The output voltage V_{ao} of the MIMC when connected to a RL plant can then be expressed by (6.5) which can then be simplified to a form shown in (6.6).

$$\frac{dI_{ao}(t)}{dt} \approx \frac{I_{ao}(n+1) - I_{ao}(n)}{T_S} \tag{6.4}$$

$$V_{ao} = \frac{I_{ao}(n+1) - I_{ao}(n)}{T_S} L + I_{ao}(n)R \tag{6.5}$$

$$I_{ao}(n+1) = \frac{V_{ao}T_S}{L} + I_{ao}(n)\left[1 - \frac{T_S R}{L}\right] \tag{6.6}$$

Note that in (6.6), $I_{ao}(n+1)$ is the value of the output current I_{ao} in the upcoming switching period and is therefore, the predicted future output current. Considering the Venturini Modulation method there are three cases of the output voltage i.e. $V_{ao} = V_{Ai}$, $V_{ao} = V_{Bi}$ or $V_{ao} = V_{Ci}$ and these three cases will cause three corresponding predicted currents $I_{Aao}(n+1)$, $I_{Bao}(n+1)$ or $I_{Cao}(n+1)$ as shown in (6.7).

$$\begin{aligned} I_{Aao}(n+1) =& \frac{V_{Ai}T_S}{L} + I_{ao}(n)\left[1 - \frac{T_S R}{L}\right] \\ I_{Bao}(n+1) =& \frac{V_{Bi}T_S}{L} + I_{ao}(n)\left[1 - \frac{T_S R}{L}\right] \\ I_{Cao}(n+1) =& \frac{V_{Ci}T_S}{L} + I_{ao}(n)\left[1 - \frac{T_S R}{L}\right] \end{aligned} \tag{6.7}$$

For the current control of the MIMC, the corresponding cost functions g_{Aa}, g_{Ba}, g_{Ca} can be expressed as:

$$\begin{aligned} g_{Aa} =& |I_{ao_ref} - I_{Aao}(n+1)| \\ g_{Ba} =& |I_{ao_ref} - I_{Bao}(n+1)| \\ g_{Ca} =& |I_{ao_ref} - I_{Cao}(n+1)| \end{aligned} \tag{6.8}$$

In equation (6.8), I_{ao_ref} represents the reference output current. The cost functions g_{Aa}, g_{Ba}, g_{Ca} can be translated to the duty cycles D_{Aa}^{lin}, D_{Ba}^{lin}, D_{Ca}^{lin} as shown in (6.9). Note that equation (6.9) is obtained as a result of assuming a linear relation between the duty cycle and the cost function. The constant G in (6.9) is the proportional constant which ensures that the value of the duty cycle does not exceed unity and the corresponding constraint can be represented by (6.10). Solving (6.10) for G results in (6.11) and the duty cycle D_{Aa}^{lin}, D_{Ba}^{lin}, D_{Ca}^{lin} can then be expressed using (6.12).

$$\begin{aligned} D_{Aa}^{lin} &= \frac{G}{g_{Aa}} \\ D_{Ba}^{lin} &= \frac{G}{g_{Ba}} \\ D_{Ca}^{lin} &= \frac{G}{g_{Ca}} \end{aligned} \tag{6.9}$$

$$\frac{G}{g_{Aa}} + \frac{G}{g_{Ba}} + \frac{G}{g_{Ca}} = 1 \tag{6.10}$$

$$G = \frac{g_{Aa}g_{Ba}g_{Ca}}{g_{Ba}g_{Ca} + g_{Aa}g_{Ca} + g_{Aa}g_{Ba}} \tag{6.11}$$

$$\begin{aligned} D_{Aa}^{lin} &= \frac{g_{Ba}g_{Ca}}{g_{Ba}g_{Ca} + g_{Aa}g_{Ca} + g_{Aa}g_{Ba}} \\ D_{Ba}^{lin} &= \frac{g_{Aa}g_{Ca}}{g_{Ba}g_{Ca} + g_{Aa}g_{Ca} + g_{Aa}g_{Ba}} \\ D_{Ca}^{lin} &= \frac{g_{Aa}g_{Ba}}{g_{Ba}g_{Ca} + g_{Aa}g_{Ca} + g_{Aa}g_{Ba}} \end{aligned} \tag{6.12}$$

Note that D_{Aa}^{lin}, D_{Ba}^{lin}, D_{Ca}^{lin} are the optimum duty cycles obtained as a result of a linear approximation however, these optimum duty cycles can also be obtained by a non-linear approach. This can be achieved by substituting V_{ao} from (6.5) to (6.13) which will result in non-linear duty cycles D_{Aa}^{n-lin}, D_{Ba}^{n-lin}, D_{Ca}^{n-lin} given in (6.14).

$$D_{Ka} = \frac{1}{3}\left(1 + \frac{2\ V_{Ki}V_{ao}}{{V_m}^2}\right) \tag{6.13}$$

$$\begin{aligned} D_{Aa}^{n-lin} &= \frac{1}{3}\left(1 + \frac{2V_{Ai}\left[I_{ao}(n+1) - I_{ao}(n)L + I_{ao}(n)RT_S\right]}{T_S{V_m}^2}\right) \\ D_{Ba}^{n-lin} &= \frac{1}{3}\left(1 + \frac{2V_{Bi}\left[I_{ao}(n+1) - I_{ao}(n)L + I_{ao}(n)RT_S\right]}{T_S{V_m}^2}\right) \\ D_{Ca}^{n-lin} &= \frac{1}{3}\left(1 + \frac{2V_{Ci}\left[I_{ao}(n+1) - I_{ao}(n)L + I_{ao}(n)RT_s\right]}{T_S{V_m}^2}\right) \end{aligned} \tag{6.14}$$

In order to validate both the linear and non-linear approaches of the M2PC current control of the MIMC, a PLECS simulation was made. The waveforms of the output currents and corresponding errors with linear and non-linear approaches are shown in Figure 6.28. From Figure 6.28 it can be seen that the non-linear approach is offering better performance in terms of steady-state error magnitude when compared with the linear approach. For a clear comparison of the quality of the output current, a comparative harmonic spectrum of the output current with both approaches is shown in Figure 6.29. The output current with the linear approach $I_{ao_MPC_lin}$ has higher harmonic content than that with the non-linear $I_{ao_MPC_n_lin}$ because of the linear approximation used for the calculation of duty-cycles. Due to this, the non-linear approach was selected for the experiment.

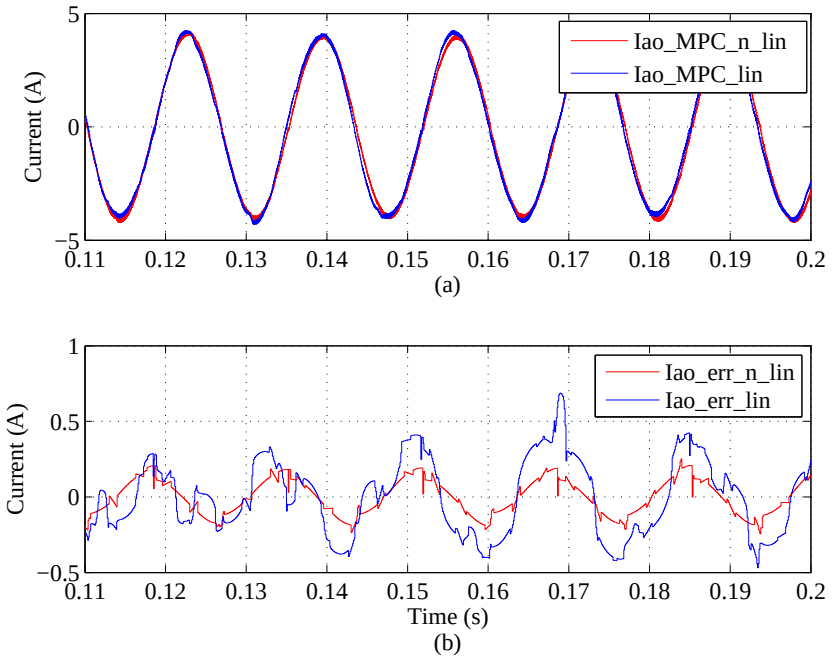


Figure 6.28: M2PC based current controller for the MIMC (simulation) (a) closed-loop output current with linear ($I_{ao_MPC_lin}$) and non-linear ($I_{ao_MPC_n_lin}$) duty-cycles approach (b) Steady-state error - with linear ($I_{ao_err_lin}$) - with non-linear ($I_{ao_err_n_lin}$)

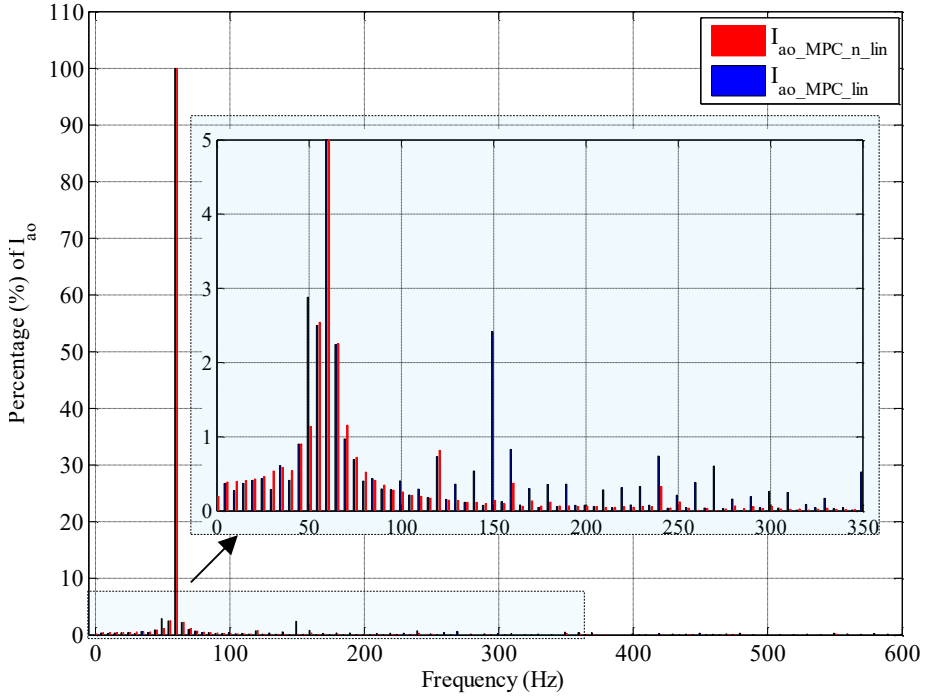


Figure 6.29: Harmonic spectrum of the output current with linear ($I_{ao_MPC_lin}$) and non-linear ($I_{ao_MPC_n_lin}$) duty-cycles approach of M2PC (simulation)

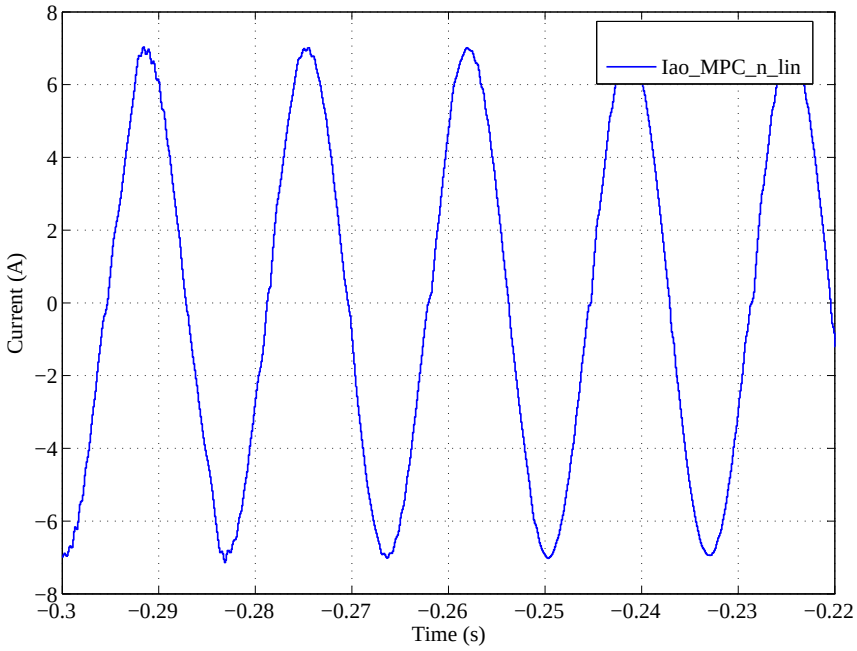


Figure 6.30: The closed-loop output current $I_{ao_MPC_n_lin}$ in the MIMC (experiment)

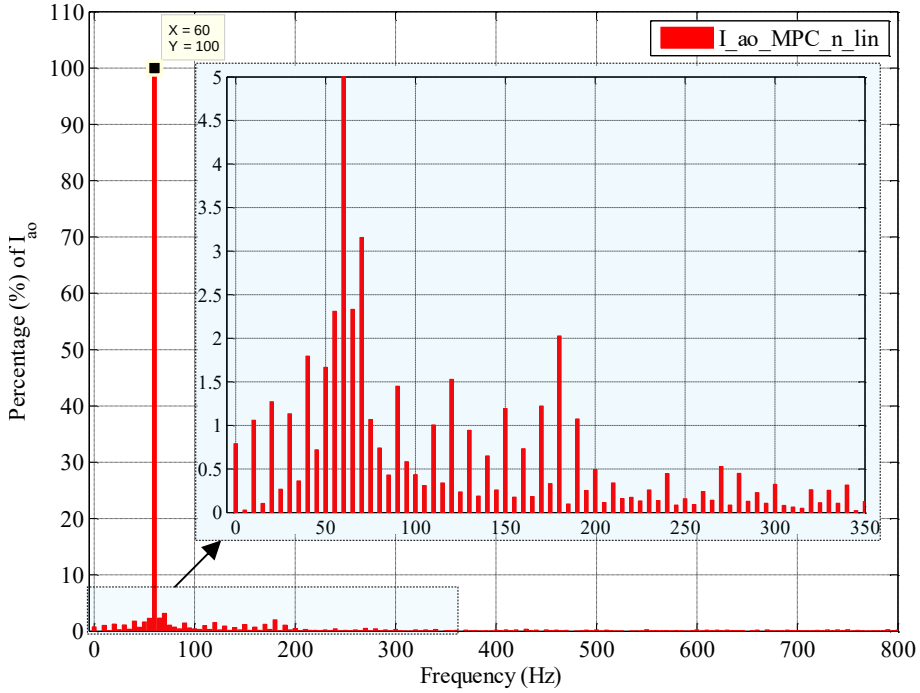
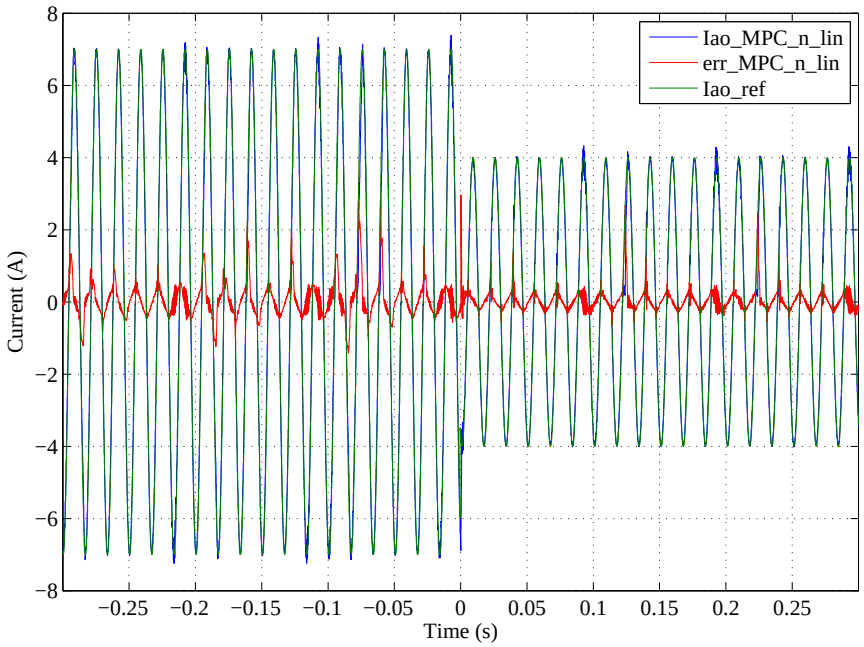


Figure 6.31: Harmonic spectrum of the closed-loop output current $I_{ao_MPC_n_lin}$ in the MIMC (experiment)

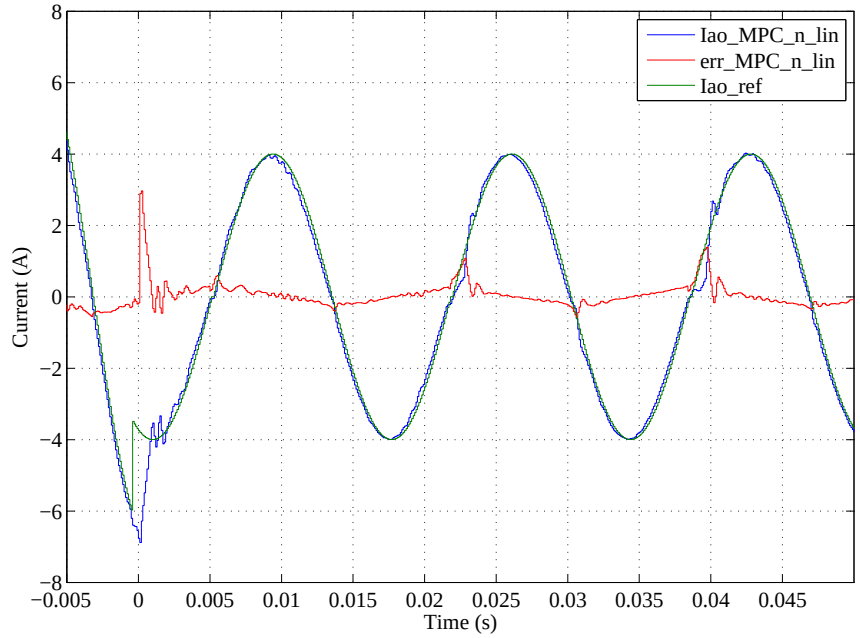
Figure 6.30 shows the experimental waveform of the output current $I_{ao_MPC_n_lin}$ as a result of the current based M2PC on the MIMC. A harmonic spectrum of $I_{ao_MPC_n_lin}$ is shown in Figure 6.31 to clearly show the harmonic content.

The response of the M2PC based closed-loop system as a result of step change in current reference I_{ao_ref} from 7A to 4A was observed. The experimental waveforms are shown in Figure 6.32(a). It can be seen from Figure 6.32(a) that the system is stable and tracks the reference current I_{ao_ref}. A zoomed view of the highlighted region of Figure 6.32(a), shown in Figure 6.32(b), shows the transient response of M2PC based current controller in experiment. It can be seen that when the step change of 3A is applied at t=0s, the M2PC based current controller quickly compensates for the error between the reference current I_{ao_ref} and the output current $I_{ao_MPC_n_lin}$ and this verifies that the M2PC retains the fast dynamic property of a traditional MPC. When compared with the transient response obtained with the PR controller, shown in Figure 6.27(b), it can be seen that the M2PC based controller offers better dynamic performance than the PR based controller.

Furthermore, some additional distortions can be seen in Figure 6.32(b) near the zero crossings of the output current due to the incorrect detection of the direction of the output current when the magnitude is too small. As mentioned earlier, this distortion is due to the limitations of the direction detection hardware (shown in Figure 5.10) but the M2PC based current controller takes necessary action to compensate for these distortions. Note that the experimental results shown in Figure 6.27 validate the application of the M2PC based current-controller to the MIMC.



(a) Step change with M2PC



(b) Transient response with M2PC

Figure 6.32: Experimental waveforms during step response of the closed-loop output current as a result of a non-linear M2PC controller (a) Step change in current reference I_{ao_ref} from 7A to 4A at t=0s (b) Zoomed view of Figure 6.32(a) showing transient response

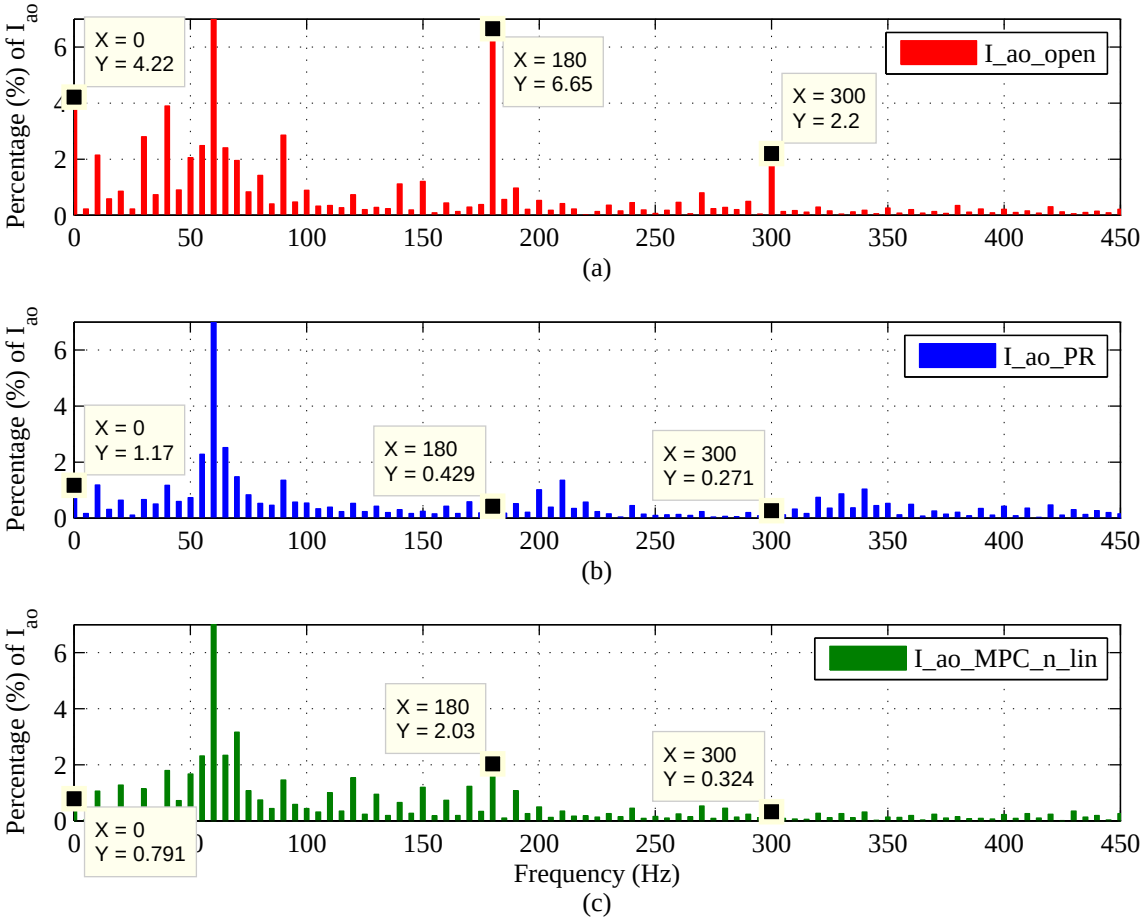


Figure 6.33: Harmonic spectrums of the experimental output current with and without closed-loop systems in the MIMC. (a) open-loop current I_{ao_open} (b) PR based closed-loop current I_{ao_PR} (c) M2PC based closed-loop current $I_{ao_MPC_n_lin}$

To compare the experimental performance of the designed PR and M2PC based controllers for the MIMC in terms of harmonic content, a comparative harmonic spectrum is shown in Figure 6.33. The most dominant harmonic in the open-loop output current I_{ao_open} is the third harmonic (180 Hz) and has a magnitude of 6.65%. When targeted specifically using a PR controller, the magnitude of the third harmonic reduces to 0.429% but in the case of the M2PC this value is 2.03%. Therefore, in selective harmonic elimination, the performance of the PR based controller is better than the M2PC based controller because of the gains at particular frequencies. On the other hand, the M2PC based controller, when compared with the PR based controller, offers good performance in the compensation of the higher order harmonics

which is due to the faster dynamic characteristics of the MPC. The THD observed in the experimental output current with the M2PC based current controller was 3.7% whereas that with the PR based current controller was 4.5%. Therefore, in terms of the THD, the M2PC based current controller has shown better performance than the PR based current controller for the MIMC.

6.4 Conclusions

For the experimental validation of the conceptual MIMC, the Venturini Modulation method was selected for the MIMC due to the lower number of commutation paths. The commutation paths were derived by using the leakage tolerant commutation method and the commutation paths were implemented as a Finite State Machine (FSM) in the FPGA. The control platform and the experimental setup was extended from a single-phase to single-phase AC/AC converter to a three-phase to single-phase version of the MIMC.

The obtained open-loop results validate the feasibility and operation of the MIMC. The open-loop MIMC system is experiencing commutation related distortion which is analogous to the dead-time distortions in the standard two-level inverters. To enhance the degree of controllability of the MIMC and also to show that the commutation related distortion can be compensated for by using basic controller techniques, a PR controller was implemented due to its ability to reject periodic distortion. The harmonics caused by the commutation are odd harmonics and with third and fifth harmonics being dominant, a multi-resonant PR current controller was designed. A 4.6% improvement in the THD of the output current was observed in the experiment with the PR based current controller.

A modern control technique known as Modulated Model Predictive Control (M2PC), which utilises a modulator to generate fixed switching frequency, was also studied for the MIMC. The non-linear type of M2PC based current control, when implemented in the experiment, showed an improvement of 5.7% in THD when compared with the open-loop system. Therefore in terms of compensation of the commutation related distortion, the M2PC has shown better performance than the PR based current controller as the THD observed in the output current with the M2PC was 3.7% which was 0.8% less than that offered by the PR based current controller. This Chapter confirmed the operation and control of the proposed conceptual MIMC.

Chapter 7

An Insight into Reactive Power Capability of the Modular Isolated Matrix Converter (MIMC)

7.1 Introduction

The open and closed-loop operation of the MIMC is confirmed from the experimental results shown in Chapter 6 however, from the application point of view, it is important to highlight what reactive power capability [130, 131] is offered by the MIMC. The MIMC will behave similar to a Direct Matrix Converter in terms of reactive power capability as long as same modulation strategy is employed. Considering that the Venturini modulation was implemented in Chapter 6, this chapter aims to provide a general study showing which factors affect the reactive power in a Venturini modulated MIMC. Note that the study presented in this chapter is an overview which is valid for the Venturini modulated converter only because the reactive power capabilities are mainly dependent on the choice of modulation method [130, 132].

7.2 Reactive Power Capability

The modulation problem which requires generation of output voltage V_{jo} from an input voltage V_{Ki} has two modulation solutions. These modulation solutions were proposed by Venturini [72, 74, 133] and are represented by two modulation matrices and given in (7.5) and (7.6). Note that $X = \omega_o t - \omega_i t$ in (7.5) and $Y = \omega_o t + \omega_i t$ (7.6).

$$[V_{Ki}] = \begin{bmatrix} V_{Ai} \\ V_{Bi} \\ V_{Ci} \end{bmatrix} = V_m \begin{bmatrix} \sin(\omega_i t) \\ \sin\left(\omega_i t - \frac{2\pi}{3}\right) \\ \sin\left(\omega_i t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{7.1}$$

$$[V_{jo}] = \begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} = qV_m \begin{bmatrix} \sin(\omega_o t) \\ \sin\left(\omega_o t - \frac{2\pi}{3}\right) \\ \sin\left(\omega_o t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{7.2}$$

$$[I_{jo}] = \begin{bmatrix} I_{ao} \\ I_{bo} \\ I_{co} \end{bmatrix} = \mathrm{I}_m \begin{bmatrix} \sin(\omega_o t + \phi_o) \\ \sin\left(\omega_o t - \frac{2\pi}{3} + \phi_o\right) \\ \sin\left(\omega_o t + \frac{2\pi}{3} + \phi_o\right) \end{bmatrix} \tag{7.3}$$

$$[I_{Ki}] = \begin{bmatrix} I_{Ai} \\ I_{Bi} \\ I_{Ci} \end{bmatrix} = q\frac{\cos(\phi_o)}{\cos(\phi_i)}\mathrm{I}_m \begin{bmatrix} \sin(\omega_o t + \phi_i) \\ \sin\left(\omega_o t - \frac{2\pi}{3} + \phi_i\right) \\ \sin\left(\omega_o t + \frac{2\pi}{3} + \phi_i\right) \end{bmatrix} \tag{7.4}$$

$$[M_1] = \frac{1}{3}\begin{bmatrix} 1+2q\cos(X) & 1+2q\cos\left(X+\frac{2\pi}{3}\right) & 1+2q\cos\left(X-\frac{2\pi}{3}\right) \\ 1+2q\cos\left(X-\frac{2\pi}{3}\right) & 1+2q\cos(X) & 1+2q\cos\left(X+\frac{2\pi}{3}\right) \\ 1+2q\cos\left(X+\frac{2\pi}{3}\right) & 1+2q\cos\left(X-\frac{2\pi}{3}\right) & 1+2q\cos(X) \end{bmatrix} \tag{7.5}$$

$$[M_2] = \frac{1}{3}\begin{bmatrix} 1-2q\cos(Y) & 1-2q\cos\left(Y-\frac{2\pi}{3}\right) & 1-2q\cos\left(Y+\frac{2\pi}{3}\right) \\ 1-2q\cos\left(Y-\frac{2\pi}{3}\right) & 1-2q\cos\left(Y+\frac{2\pi}{3}\right) & 1-2q\cos(Y) \\ 1-2q\cos\left(Y+\frac{2\pi}{3}\right) & 1-2q\cos(Y) & 1-2q\cos\left(Y+\frac{2\pi}{3}\right) \end{bmatrix} \tag{7.6}$$

The modulation matrix M_1 causes the phase at the input side to be equal to the output side i.e. $\phi_i = \phi_o$ whereas the modulation matrix M_2 reverses the phase at the input side i.e. $\phi_i = -\phi_o$. Therefore, to have a controllable phase at the input

side, the combination of the two matrices can be utilised by defining a relation using constants α_1 and α_2 as below;

$$[M] = \alpha_1 [M_1] + \alpha_2 [M_2] \qquad where \;\; \alpha_1 + \alpha_2 = 1 \tag{7.7}$$

By controlling the values of α_1 and α_2, the reactive power can be controlled. From Figure 7.1 it can be seen that the Venturini based modulated MIMC will deliver maximum reactive power at its input when α_2 is unity whereas the converter will receive maximum reactive power at its input when α_2 is zero. Furthermore, it can also be seen that the MIMC will consume peak reactive power at the input side when the output power factor angle is 90° and $\alpha_2 = 0$ whereas the MIMC will deliver peak reactive power at the input side when the output power factor angle is 90° and $\alpha_2 = 1$.

Also seen from Figure 7.1 is that the MIMC is not able to consume or deliver any reactive power at its input side when the output power factor angle is 0° regardless of the value of α_2.

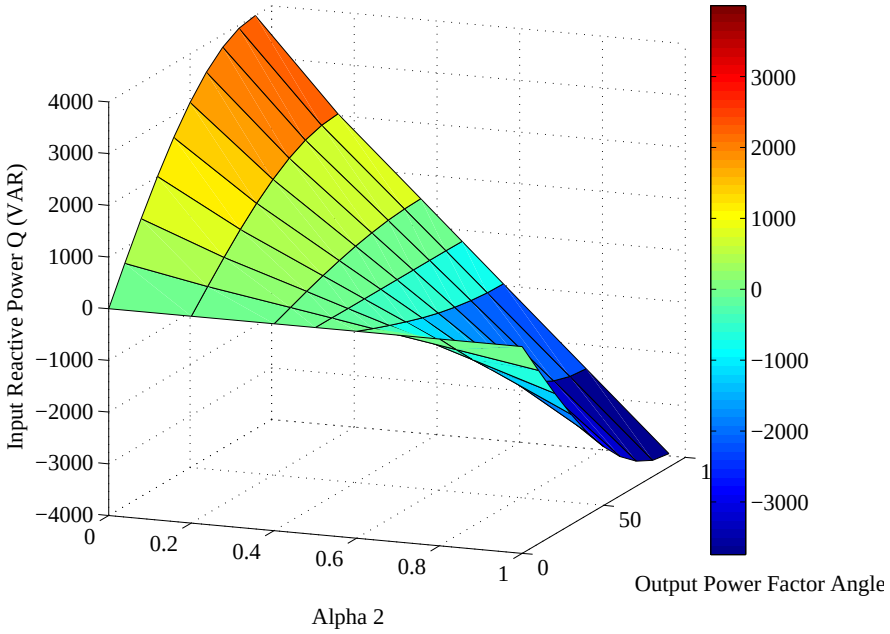


Figure 7.1: Relationship between the input side reactive power, α_2 and output power factor angle ϕ_o in the Venturini based modulated MIMC

In order to study the behaviour of the input reactive power as a result of change in the voltage regulation ratio q, Figure 7.2 is shown. A non-linear relation between the

voltage regulation ratio q and the input side reactive power can be seen in Figure 7.2. This non-linear relation is because the input side current is a square function of the voltage regulation ratio q. The maximum reactive power is consumed at the input side with $\alpha_2 = 0$ when voltage regulation ratio is at maximum i.e. $q = 0.5$. However, the maximum reactive power is delivered by the input side with $\alpha_2 = 1$ and $q = 0.5$ as seen from Figure 7.3.

Figures 7.2 and 7.3 show the relationship between reactive power and the voltage regulation ratio q. To study the relationship between active power and the voltage regulation regulation ratio q, Figure 7.4 is shown. It can be seen from Figure 7.4 that the active power, like the reactive power, has a square function of the voltage regulation ratio q. From Figure 7.2-7.4, it can be summarised that the peak value of the reactive power that the MIMC can deliver ($\alpha_2 = 1$) or consume ($\alpha_2 = 0$) at its input side varies directly with the output power factor angle ϕ_o and voltage transfer ratio q.

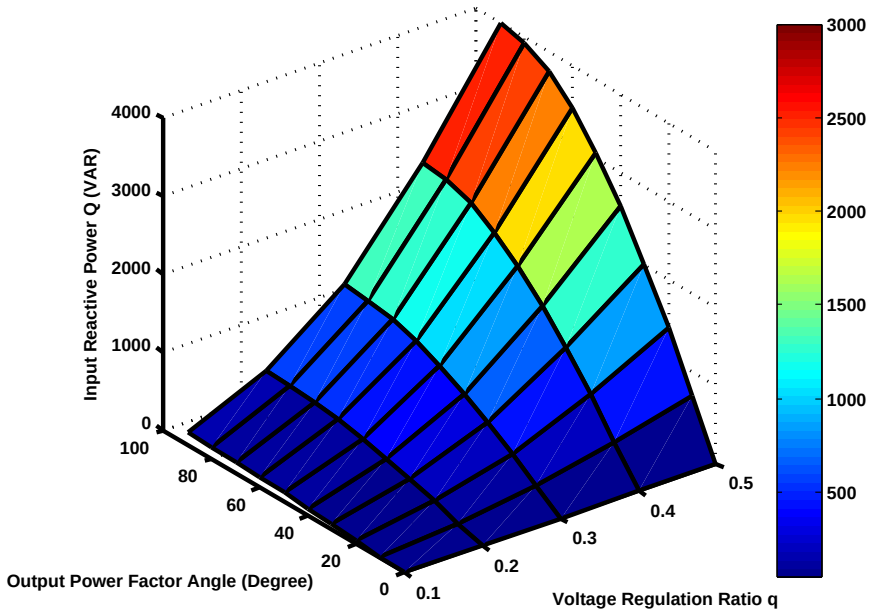


Figure 7.2: Relationship between the input side reactive power, voltage regulation ratio q and output power factor angle ϕ_o with $\alpha_2 = 0$ in the Venturini based modulated MIMC

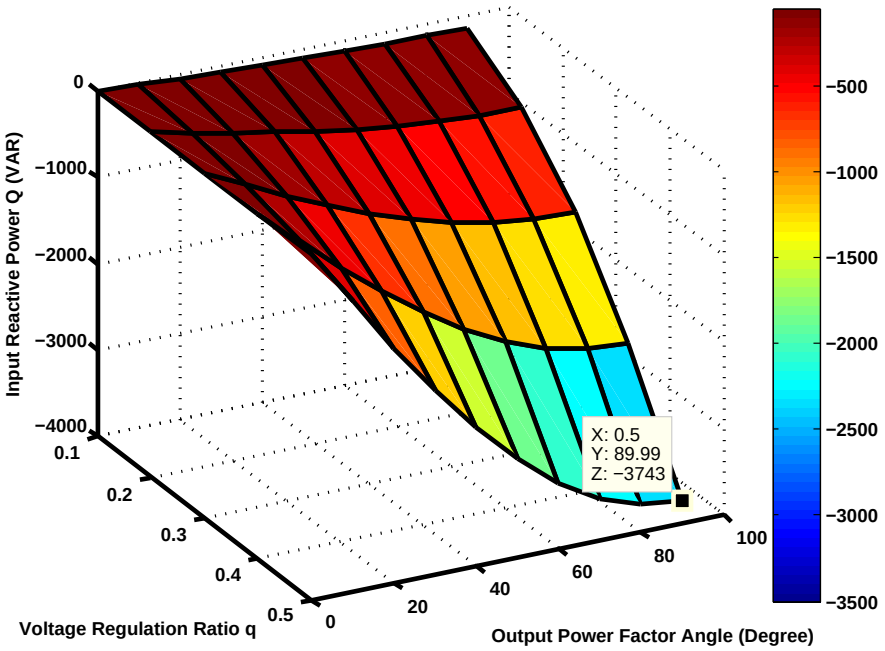


Figure 7.3: Relationship between the input side reactive power, voltage regulation ratio q and output power factor angle ϕ_o with $\alpha_2 = 1$ in the Venturini based modulated MIMC

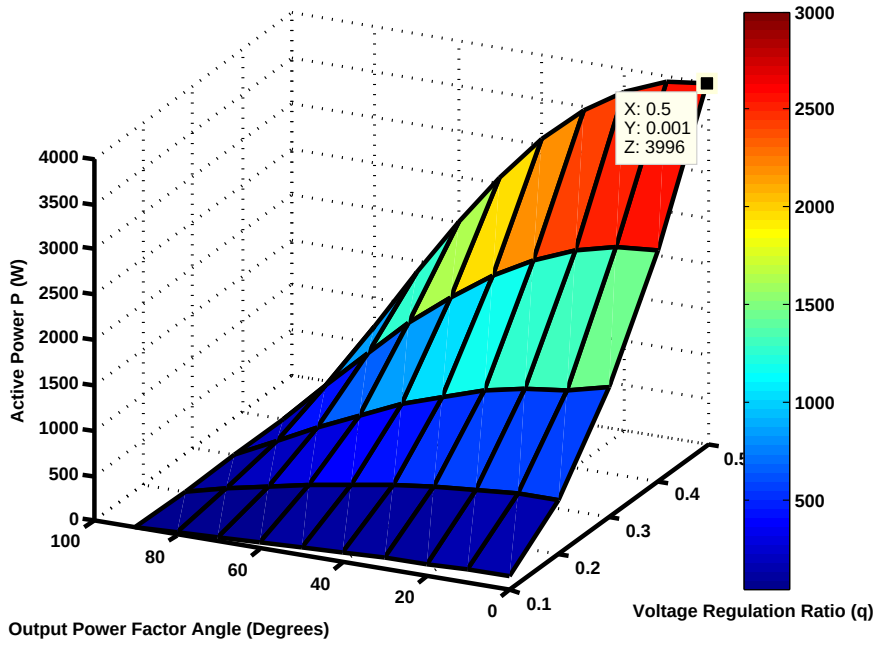


Figure 7.4: Relationship between the active power, voltage regulation ratio q and output power factor angle ϕ_o in the Venturini based modulated MIMC

7.3 Conclusions

This chapter provided a general study highlighting factors which affect the input side reactive power in a Venturini modulated MIMC. The peak value of the reactive power consumed at the input side or delivered from the input side varies directly with the output power factor angle. However, with a given value of output power factor angle, the input side reactive power can be controlled by varying the value of α_2. The input side reactive power also depends on the voltage regulation ratio q and possesses a direct but non-linear relationship with q. By controlling α_2 and q, the MIMC can be seen as a reactive power compensation device.

Chapter 8

Conclusions and Future Work

The single-stage AC/AC SST architecture based converter topologies can offer increased power density in comparison to multi-stage AC/AC SST architectures. This thesis has proposed a single-stage AC/AC SST architecture based three-phase Modular Isolated Matrix Converter (MIMC) topology. The converter topology proposed in this thesis uses the single-phase isolated AC/AC converter as a building block or a cell. The repetition of the cells in the MIMC is based on the concept of the Matrix Converter and allows modularity within a single converter. The proposed Modular Isolated Matrix Converter (MIMC) has an increased number of semiconductor devices, but the modularity within the converter has benefited in terms of ease of hardware implementation and maintenance because all the H-bridges in the MIMC are identical. In addition to this, scalability to higher power level is also possible by stacking of multiple cells as proposed in the future work.

The fundamental concept of the MIMC comes from the Direct Matrix Converter, therefore the assumption that the input side behaves as a voltage source while the output side behaves as a current source remains the same for the MIMC. Therefore, the modulation methods for the Direct Matrix Converter can be applied to the MIMC. However, the application of Direct Matrix Converter modulation methods is challenging due to the presence of MF transformers in the MIMC, unlike a Direct

Matrix Converter and hence require adaptation. This challenge was approached by proposing the switching functions, in Chapter 3, that generate a 50% duty cycle MF waveform at the transformers and meanwhile implementing the Venturini Modulation (VM) method on the MIMC.

The proposed switching functions that implement the VM method were validated using the PLECS simulation toolbox. In the simulation validation, the test case of generating a 60 Hz output from a 50 Hz input was selected to examine the MIMC for input-output frequency decoupling. The harmonic spectrum obtained from the simulation confirmed the input-output frequency decoupling using the proposed VM switching functions. The maximum voltage transfer ratio achieved with the VM method is limited to 0.5. Although, the voltage transfer ratio in the MIMC can be increased by changing the turn ratio of the transformers but the possibilities of increasing the voltage transfer ratio using modulation methods were explored to study the modulation limits of the MIMC. In this regard, a new set of switching functions were proposed in this thesis to increase the voltage transfer ratio of the traditional VM method from 0.5 to unity. This approach exploits the four-quadrant switch based H-bridge and the presence of a balanced input voltage supply to double the voltage transfer ratio. Therefore, the modulation method was named as Double Venturini Modulation method (DVM).

Further improvements in the voltage transfer ratio were made by adopting a third-harmonic injection scheme that increases the voltage transfer ratio to $\sqrt{3}$ by maximum utilisation of the envelope of the three-phase input supply. This modulation method was named as Double Optimum Venturini Modulation (DOVM) method. More modulation possibilities were explored using a vector approach known as Space Vector Modulation (SVM). However, the manual determination of the valid space vectors for the converters with a large number of switches, such as MIMC, can be laborious. Therefore, the possible fixed-direction vectors were computed using a Matlab program. The application times and the switching sequence for the computed vectors were validated using PLECS simulation toolbox.

The current commutation in the MIMC is key challenge specifically in the presence of a practical transformer which has non-negligible leakage inductance due to the lack of freewheeling path in the four-quadrant switches of the MIMC. The application of the standard 4-step current commutation approach in the presence of transformer leakage inductance will cause voltage spikes across the semiconductor devices and therefore threatens the practically feasibility of the MIMC. The safe application of the standard 4-step current commutation is possible only when all the bridges of the MIMC are equipped with dissipative clamp circuits. The impact of the leakage could be minimized with an optimized transformer design, by adding snubbers or overrating the devices, but these options are not convenient in practice.

This thesis presented a new practical leakage tolerant current commutation approach for the single-phase AC/AC converter (single-cell of the MIMC) in Chapter 4. The proposed leakage tolerant current commutation method decouples the leakage inductance current from the output current and then imposes the source voltage to reverse the current through the leakage inductance using the input side bridge. In this way, the energy stored in the leakage inductance is restored, unlike the standard 4-step current commutation approach in which the energy is dissipated in the clamp circuit. The proposed strategy requires an estimation of the leakage inductance and setting of the suitable commutation timing, but does not require additional high bandwidth voltage or current measurements or any auxiliary circuits.

The proposed leakage tolerant current commutation strategy was successfully validated by simulation and experimental results from a single-phase AC/AC converter prototype presented in Chapter 5. Both current commutation strategies were implemented to enable a detailed comparative study. The switching for the commutation paths for both methods were implemented in the FPGA (Field-Programmable Gate Array) using a Finite State Machine (FSM). When compared with the standard method, a reduction in the power losses was seen with the proposed current commutation method due to leakage energy restoration. In terms of the conduction losses, both methods offered similar performance. However, the proposed method offers an exceptional reduction in the switching losses because the rate of change of current $\frac{dI}{dt}$

through the devices is limited by the leakage inductance, increasing the total number of soft-switchings.

For the experimental validation of the conceptual MIMC, the prototype was extended from a single-cell of the MIMC to a 6kW three-phase to single-phase MIMC. The basic VM method was selected for the experimental validation of the MIMC as it offers ease of implementation due to lower number of commutation paths. The commutation paths per cell required for applying the VM method were derived and implemented in the FPGA using FSM. The experimental results validate the feasibility and open-loop operation of the MIMC. However, the open-loop MIMC system is experiencing commutation related distortion which is analogous to the dead-time distortions in the standard two-level inverters. To enhance the degree of controllability of the MIMC and also to show that the commutation related distortion can be compensated for, two control techniques were analysed. First, a Proportional-Resonant (PR) controller was implemented due to its ability to reject periodic distortion. Second, a non-linear type of Modulated Model Predictive Control (M2PC) was also proposed. A comparative analysis of harmonics showed that M2PC based controller is slightly better than PR controller in current quality and possesses excellent dynamic response. The feasibility of the MIMC is confirmed from the open-loop and closed-loop experimental results shown in Chapter 6.

The reactive power compensation capability of the MIMC is similar to the Direct Matrix Converter considering same modulation method is applied to both. In order to give a highlight of reactive power capability of a Venturini modulated MIMC, an overview is presented in Chapter 7. It was observed that the peak value of the reactive power consumed at the input side or delivered from the input side varies directly with the output power factor angle. However, with a given value of output power factor angle, the input side reactive power can be changed from delivered to consumed by changing the value of α_2 from unity to zero. Therefore, the MIMC offers reactive power capability unlike its single-cell i.e. single-phase isolated AC/AC converter.

8.1 Future Work

This thesis presented the first study on the proposed MIMC topology. Therefore, the focus of the study has mainly been limited to the feasibility and validation of the conceptual MIMC topology. Considering this, the experimental prototype was not optimised to show technology and power density but to practically demonstrate the operation including modulation, commutation and control. The author certainly believes that there are areas requiring various improvements. Potential areas of the improvement are discussed as:

- The designed prototype is a three-phase to single-phase version of the MIMC, and therefore the currents at the input side of the MIMC are not completely sinusoidal. By moving to a three-phase to three-phase MIMC system, the input side of the MIMC will draw sinusoidal currents.
- The PCBs of the designed converter can be optimised to show a high power density. Further improvement in the power density of the converter can be made by replacing the IGBTs with wide-band gap devices, for example SiC. This would then lead on to a technology transfer stage to a company who could sell/implement the system.
- The IGBT power modules used in the prototype are rated for power much higher than the other components of the prototype, 150A and 1200V. The converter when tested at low power experiences large forward drops across the devices. Therefore, in order to show excellent efficiency, the power modules must be chosen according to the application. This can also help in implementing a feed-forward compensation for the commutation related distortions.
- After sizing the converter according to a particular application, the next step is to test the converter for the application-specific scenarios including fault conditions, grid unbalance and reactive power compensation.

- To be able to present a comprehensive study, the MIMC can be compared with the other competing isolated AC/AC converter solutions in terms of switching losses, conduction losses, total efficiency, fault-ride-through capability, operation under unbalanced grid and reactive power compensation capability.
- The current direction detector circuit requires improvement in accurately detecting the direction of the current near zero-crossings.

8.1.1 Converter Topology Extension For High Voltage

Due to the modularity in the proposed MIMC topology, the proposed topology can be extended to higher voltage and power levels. This extension can be done by determining N number of cells based on the required voltage level and then inserting a cascade connection of these N cells in the structure of the MIMC to share the input voltage as shown in Figure 8.1.

8.1.2 Converter Topology Extension For High Current

The proposed MIMC topology can also be extended to the desired current level. This extension can be made by determining N number of cells based on the required current level and then inserting a parallel connection of these N cell in the structure of the MIMC to share the input current as shown in Figure 8.2.

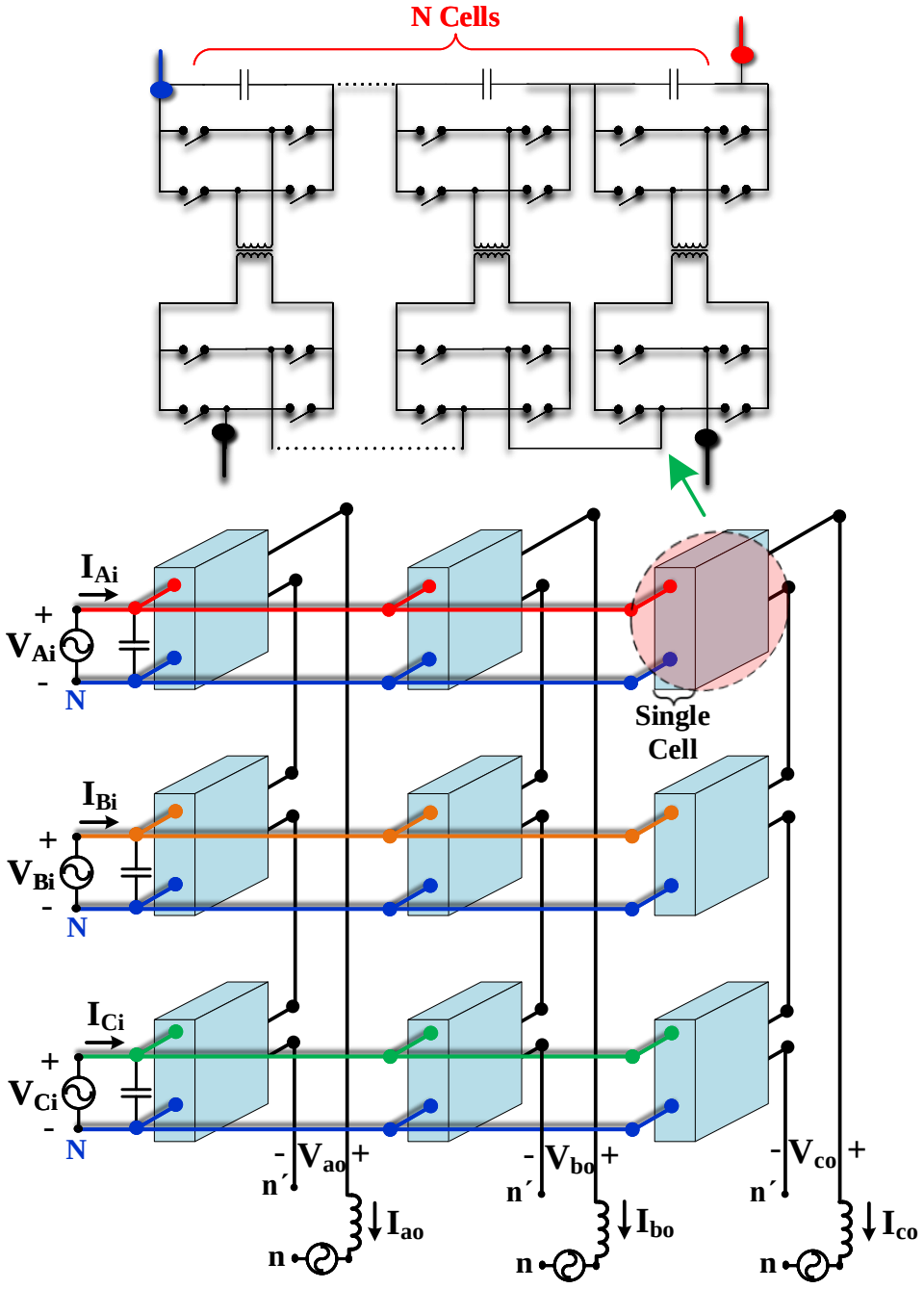


Figure 8.1: Extension of the three-phase Modular Isolated Matrix Converter (MIMC) for high voltage

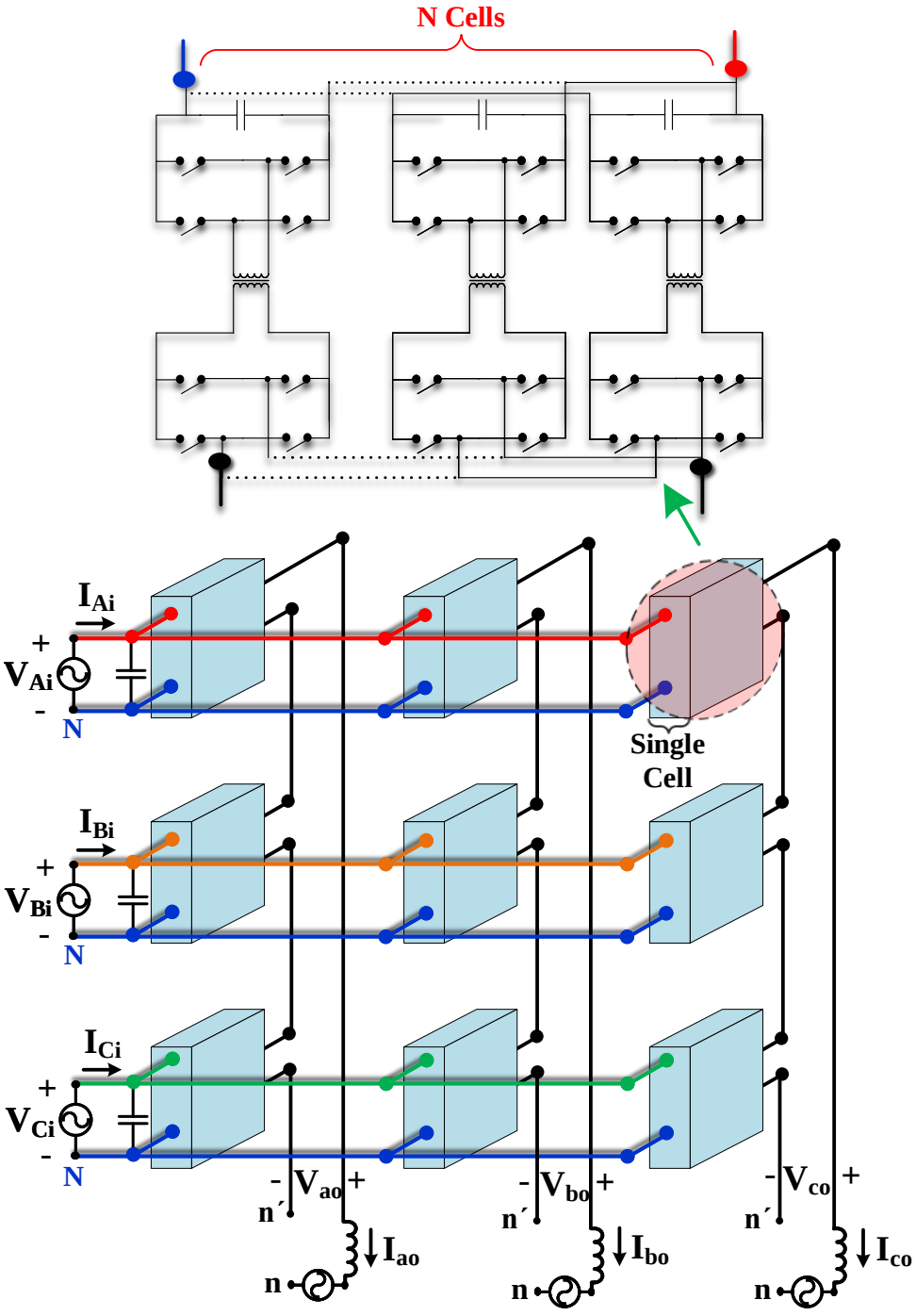


Figure 8.2: Extension of the three-phase Modular Isolated Matrix Converter (MIMC) for high current

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Appendix A

Schematics

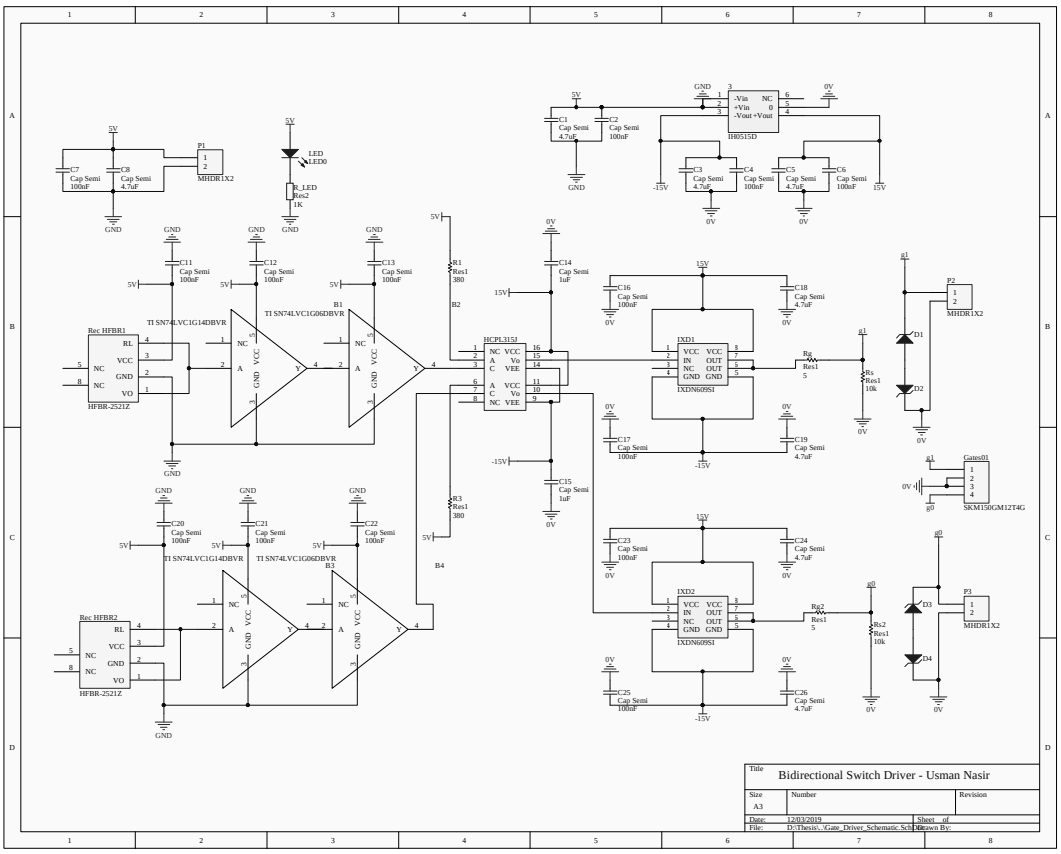


Figure A.1: Schematic of an isolated driver for a 4-quadrant switch

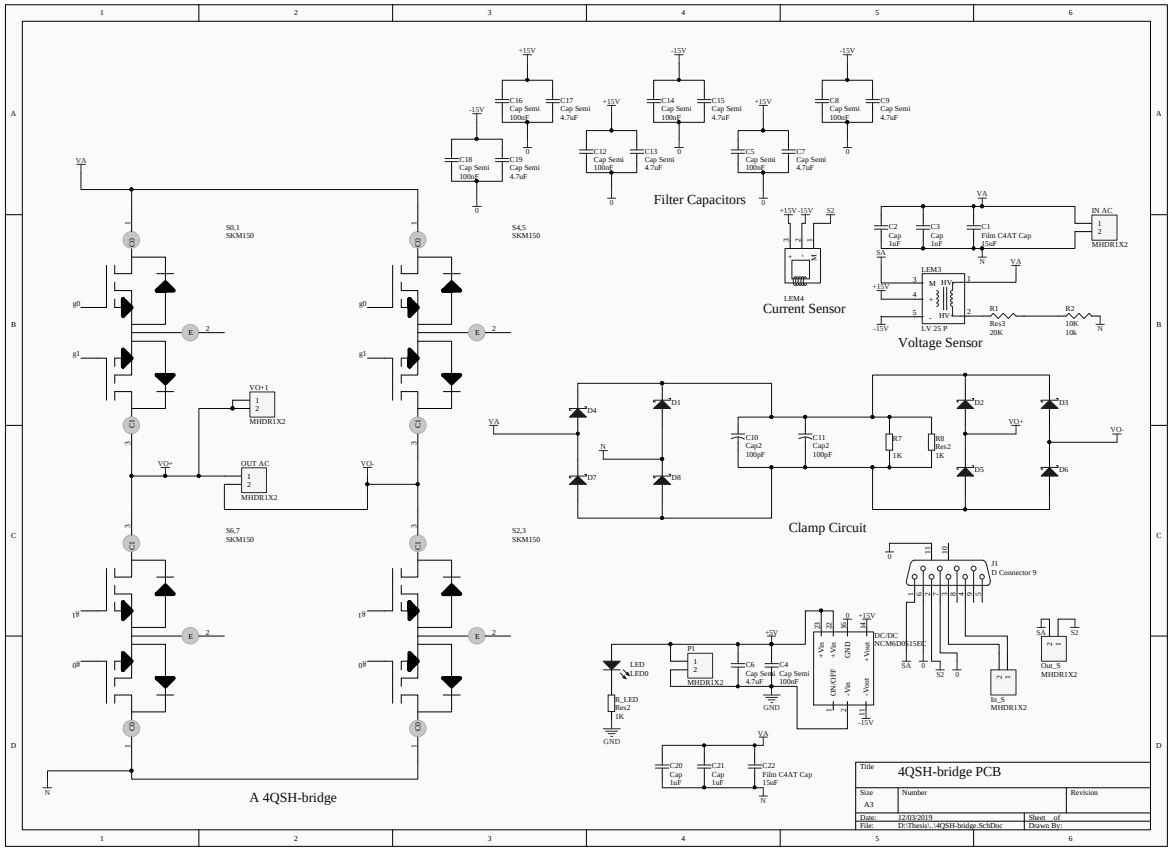


Figure A.2: Schematic of a 4QSH-bridge power board

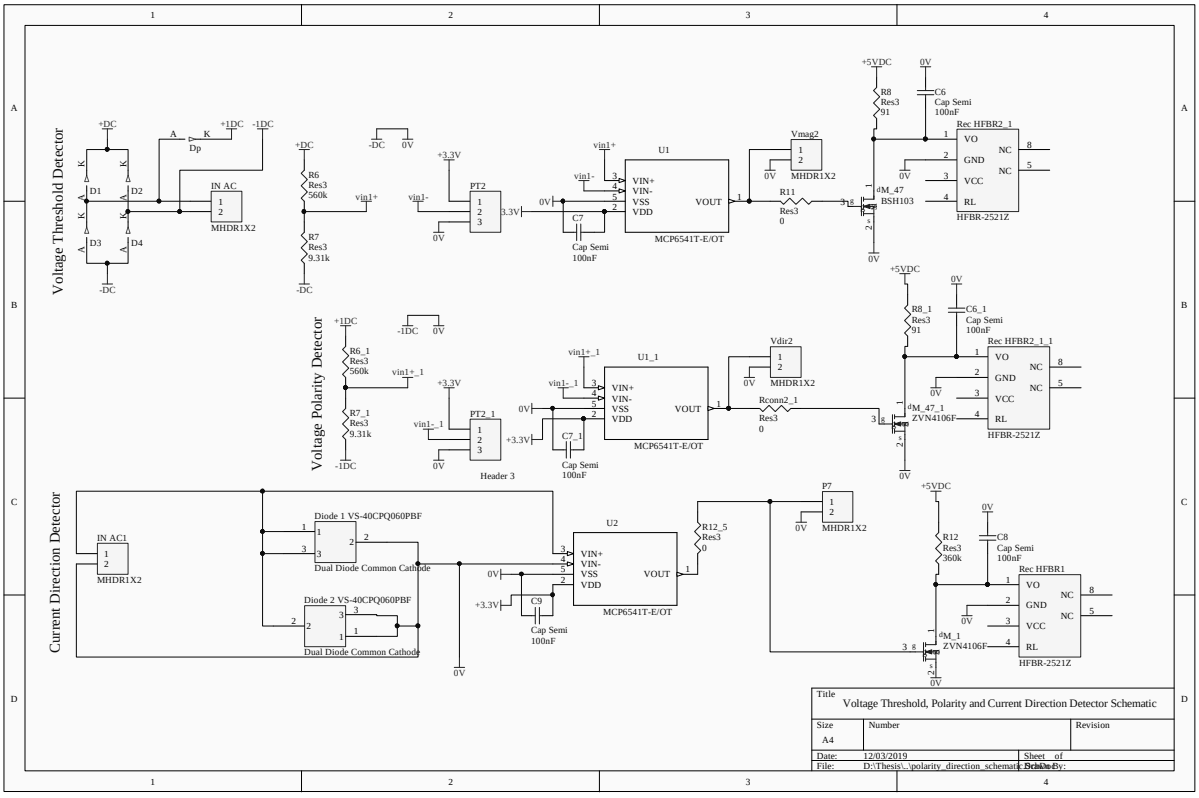


Figure A.3: Schematic of voltage polarity, voltage threshold and current direction detection board

Appendix B

States for Space Vector Modulation(SVM)

State No.	+1	+1C	-1	-1C	+2	+2C	-2	-2C	+3	+3C	-3	-3C	+4	+4C	-4	-4C	+5C	+5C	-5	-5C	+6	+6C	-6	-6C	+7	+7C	-7	-7C	+8	+8C	-8	-8C	+9	+9C	-9	-9C
SWAia	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXAia	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYAia	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZAia	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWAoa	1	0	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0	1
SXAoa	1	0	0	1	1	1	1	1	0	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1
SYAoa	0	1	1	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0
SZAoa	0	1	1	0	1	1	1	1	1	0	0	1	1	0	0	1	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0
SWBia	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXBia	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYBia	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZBia	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWBoa	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
SXBoa	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1
SYBoa	1	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0
SZBoa	1	0	0	1	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1
SWCia	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXCia	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYCia	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZCia	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWCoa	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	1	1	0	0	0	0	1	0	0	0	1	0	0	0	1	1	0
SXCoa	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0
SYCoa	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1
SZCoa	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0	1	0	0	1

Figure B.1: State of the switches in the MIMC corresponding to the active vectors listed in Table 3.2

State No.	+1	+1C	-1	-1C	+2	+2C	-2	-2C	+3	+3C	-3	-3C	+4	+4C	-4	-4C	+5C	+5C	-5	-5C	+6	+6C	-6	-6C	+7	+7C	-7	-7C	+8	+8C	-8	-8C	+9	+9C	-9	-9C
SWAib	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXAib	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYAib	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZAib	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWAob	0	1	1	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	0	0	1
SXAob	0	1	1	0	1	1	1	1	1	0	0	1	1	0	0	1	1	1	1	1	0	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1
SYAob	1	0	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	1	1	0
SZAob	1	0	0	1	1	1	1	1	1	0	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1	1	0	0	1	1	1	1	1	0	1	1	0
SWBib	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXBib	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYBib	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZBib	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWBob	1	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
SXBob	1	0	0	1	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1
SYBob	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0
SZBob	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1
SWCib	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXCib	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYCib	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZCib	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWCob	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	1	0
SXCob	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	0
SYCob	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1
SZCob	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	1

Figure B.1: (Contd.) State of the switches in the MIMC corresponding to the active vectors listed in Table 3.2

State No.	+1	+1C	-1	-1C	+2	+2C	-2	-2C	+3	+3C	-3	-3C	+4	+4C	-4	-4C	+5C	+5C	-5	-5C	+6	+6C	-6	-6C	+7	+7C	-7	-7C	+8	+8C	-8	-8C	+9	+9C	-9	-9C
SWAic	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXAic	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYAic	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZAic	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWAoc	0	1	1	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	1	1	0
SXAoc	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	1	0	0	1	1	1	1	1	0	1	1	0
SYAoc	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	0	0	1
SZAoc	1	0	0	1	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1
SWBic	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXBic	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYBic	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZBic	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWBoc	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0
SXBoc	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1
SYBoc	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
SZBoc	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1
SWCic	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SXCic	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
SYCic	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SZCic	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SWCoc	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1
SXCoc	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	1
SYCoc	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0
SZCoc	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0

Figure B.1: (Contd.) State of the switches in the MIMC corresponding to the active vectors listed in Table 3.2

State No.	Z1	Z1c	Z2	Z2c	Z3	Z3c	Z4	Z4c	Z5	Z5c	Z6	Z6c	State No.	Z1	Z1c	Z2	Z2c	Z3	Z3c	Z4	Z4c	Z5	Z5c	Z6	Z6c	State No.	Z1	Z1c	Z2	Z2c	Z3	Z3c	Z4	Z4c	Z5	Z5c	Z6	Z6c
SWAia	1	0	1	0	1	0	1	0	1	0	1	0	SWAib	1	0	1	0	1	0	1	0	1	0	1	0	SWAic	1	0	1	0	1	0	1	0	1	0	1	0
SXAia	1	0	1	0	1	0	1	0	1	0	1	0	SXAib	1	0	1	0	1	0	1	0	1	0	1	0	SXAic	1	0	1	0	1	0	1	0	1	0	1	0
SYAia	0	1	0	1	0	1	0	1	0	1	0	1	SYAib	0	1	0	1	0	1	0	1	0	1	0	1	SYAic	0	1	0	1	0	1	0	1	0	1	0	1
SZAia	0	1	0	1	0	1	0	1	0	1	0	1	SZAib	0	1	0	1	0	1	0	1	0	1	0	1	SZAic	0	1	0	1	0	1	0	1	0	1	0	1
SWAoa	0	1	1	0	1	0	0	1	0	0	0	0	SWAob	0	1	1	0	1	0	0	1	0	0	0	0	SWAoc	0	1	1	0	1	0	0	1	0	0	0	0
SXAoa	0	1	1	0	1	0	0	1	1	1	1	1	SXAob	0	1	1	0	1	0	0	1	1	1	1	1	SXAoc	0	1	1	0	1	0	0	1	1	1	1	1
SYAoa	1	0	0	1	0	1	1	0	0	0	0	0	SYAob	1	0	0	1	0	1	1	0	0	0	0	0	SYAoc	1	0	0	1	0	1	1	0	0	0	0	0
SZAoa	1	0	0	1	0	1	1	0	1	1	1	1	SZAob	1	0	0	1	0	1	1	0	1	1	1	1	SZAoc	1	0	0	1	0	1	1	0	1	1	1	1
SWBia	1	0	1	0	1	0	1	0	1	0	1	0	SWBib	1	0	1	0	1	0	1	0	1	0	1	0	SWBic	1	0	1	0	1	0	1	0	1	0	1	0
SXBia	1	0	1	0	1	0	1	0	1	0	1	0	SXBib	1	0	1	0	1	0	1	0	1	0	1	0	SXBic	1	0	1	0	1	0	1	0	1	0	1	0
SYBia	0	1	0	1	0	1	0	1	0	1	0	1	SYBib	0	1	0	1	0	1	0	1	0	1	0	1	SYBic	0	1	0	1	0	1	0	1	0	1	0	1
SZBia	0	1	0	1	0	1	0	1	0	1	0	1	SZBib	0	1	0	1	0	1	0	1	0	1	0	1	SZBic	0	1	0	1	0	1	0	1	0	1	0	1
SWBoa	0	0	0	0	0	1	1	0	1	0	0	1	SWBob	0	0	0	0	0	1	1	0	1	0	0	1	SWBoc	0	0	0	0	0	1	1	0	1	0	0	1
SXBoa	1	1	1	1	0	1	1	0	1	0	0	1	SXBob	1	1	1	1	0	1	1	0	1	0	0	1	SXBoc	1	1	1	1	0	1	1	0	1	0	0	1
SYBoa	0	0	0	0	1	0	0	1	0	1	1	0	SYBob	0	0	0	0	1	0	0	1	0	1	1	0	SYBoc	0	0	0	0	1	0	0	1	0	1	1	0
SZBoa	1	1	1	1	1	0	0	1	0	1	1	0	SZBob	1	1	1	1	1	0	0	1	0	1	1	0	SZBoc	1	1	1	1	1	0	0	1	0	1	1	0
SWCia	1	0	1	0	1	0	1	0	1	0	1	0	SWCib	1	0	1	0	1	0	1	0	1	0	1	0	SWCic	1	0	1	0	1	0	1	0	1	0	1	0
SXCia	1	0	1	0	1	0	1	0	1	0	1	0	SXCib	1	0	1	0	1	0	1	0	1	0	1	0	SXCic	1	0	1	0	1	0	1	0	1	0	1	0
SYCia	0	1	0	1	0	1	0	1	0	1	0	1	SYCib	0	1	0	1	0	1	0	1	0	1	0	1	SYCic	0	1	0	1	0	1	0	1	0	1	0	1
SZCia	0	1	0	1	0	1	0	1	0	1	0	1	SZCib	0	1	0	1	0	1	0	1	0	1	0	1	SZCic	0	1	0	1	0	1	0	1	0	1	0	1
SWCoa	1	0	0	1	0	0	0	0	0	1	1	0	SWCob	1	0	0	1	0	0	0	0	0	1	1	0	SWCoc	1	0	0	1	0	0	0	0	0	1	1	0
SXCoa	1	0	0	1	1	1	1	1	0	1	1	0	SXCob	1	0	0	1	1	1	1	1	0	1	1	0	SXCoc	1	0	0	1	1	1	1	1	0	1	1	0
SYCoa	0	1	1	0	0	0	0	0	1	0	0	1	SYCob	0	1	1	0	0	0	0	0	1	0	0	1	SYCoc	0	1	1	0	0	0	0	0	1	0	0	1
SZCoa	0	1	1	0	1	1	1	1	1	0	0	1	SZCob	0	1	1	0	1	1	1	1	1	0	0	1	SZCoc	0	1	1	0	1	1	1	1	1	0	0	1

Figure B.2: State of the switches in the MIMC corresponding to the zero vectors

State Number	Vo_mag	<Vo	Vo_coeff	Ii_coeff	<Ii	Ii_mag	VTK	[Vao, Vbo, Vco]
1	4/3	0	VA - VB	ioa	-30	(4*3^(1/2))/3	Vki	[VA - VB, VB - VA, VB - VA]
10	4/3	0	VA - VB	ioa	-30	(4*3^(1/2))/3	Vki	[VA - VB - VC, VB - VA - VC, VB - VA - VC]
19	4/3	0	VA - VB	ioa	-30	(4*3^(1/2))/3	Vki	[VA - VB + VC, VB - VA + VC, VB - VA + VC]
-1	4/3	180	VA - VB	ioa	150	(4*3^(1/2))/3	Vki	[VB - VA, VA - VB, VA - VB]
-10	4/3	180	VA - VB	ioa	150	(4*3^(1/2))/3	Vki	[VB - VA + VC, VA - VB + VC, VA - VB + VC]
-19	4/3	180	VA - VB	ioa	150	(4*3^(1/2))/3	Vki	[VB - VA - VC, VA - VB - VC, VA - VB - VC]
2	4/3	0	VB - VC	ioa	90	(4*3^(1/2))/3	Vki	[VB - VC, VC - VB, VC - VB]
11	4/3	0	VB - VC	ioa	90	(4*3^(1/2))/3	Vki	[VB - VA - VC, VC - VB - VA, VC - VB - VA]
20	4/3	0	VB - VC	ioa	90	(4*3^(1/2))/3	Vki	[VA + VB - VC, VA - VB + VC, VA - VB + VC]
-2	4/3	180	VB - VC	ioa	-90	(4*3^(1/2))/3	Vki	[VC - VB, VB - VC, VB - VC]
-11	4/3	180	VB - VC	ioa	-90	(4*3^(1/2))/3	Vki	[VA - VB + VC, VA + VB - VC, VA + VB - VC]
-20	4/3	180	VB - VC	ioa	-90	(4*3^(1/2))/3	Vki	[VC - VB - VA, VB - VA - VC, VB - VA - VC]
3	4/3	180	VA - VC	ioa	-150	(4*3^(1/2))/3	Vki	[VC - VA, VA - VC, VA - VC]
12	4/3	180	VA - VC	ioa	-150	(4*3^(1/2))/3	Vki	[VC - VB - VA, VA - VB - VC, VA - VB - VC]
21	4/3	180	VA - VC	ioa	-150	(4*3^(1/2))/3	Vki	[VB - VA + VC, VA + VB - VC, VA + VB - VC]
-3	4/3	0	VA - VC	ioa	30	(4*3^(1/2))/3	Vki	[VA - VC, VC - VA, VC - VA]
-12	4/3	0	VA - VC	ioa	30	(4*3^(1/2))/3	Vki	[VA + VB - VC, VB - VA + VC, VB - VA + VC]
-21	4/3	0	VA - VC	ioa	30	(4*3^(1/2))/3	Vki	[VA - VB - VC, VC - VB - VA, VC - VB - VA]
4	4/3	120	VA - VB	iob	-30	(4*3^(1/2))/3	Vki	[VB - VA, VA - VB, VB - VA]
13	4/3	120	VA - VB	iob	-30	(4*3^(1/2))/3	Vki	[VB - VA + VC, VA - VB + VC, VB - VA + VC]
22	4/3	120	VA - VB	iob	-30	(4*3^(1/2))/3	Vki	[VB - VA - VC, VA - VB - VC, VB - VA - VC]
-4	4/3	-60	VA - VB	iob	150	(4*3^(1/2))/3	Vki	[VA - VB, VB - VA, VA - VB]
-13	4/3	-60	VA - VB	iob	150	(4*3^(1/2))/3	Vki	[VA - VB + VC, VB - VA + VC, VA - VB + VC]
-22	4/3	-60	VA - VB	iob	150	(4*3^(1/2))/3	Vki	[VA - VB - VC, VB - VA - VC, VA - VB - VC]
5	4/3	120	VB - VC	iob	90	(4*3^(1/2))/3	Vki	[VC - VB, VB - VC, VC - VB]
14	4/3	120	VB - VC	iob	90	(4*3^(1/2))/3	Vki	[VA - VB + VC, VA + VB - VC, VA - VB + VC]
23	4/3	120	VB - VC	iob	90	(4*3^(1/2))/3	Vki	[VC - VB - VA, VB - VA - VC, VC - VB - VA]
-5	4/3	-60	VB - VC	iob	-90	(4*3^(1/2))/3	Vki	[VB - VC, VC - VB, VB - VC]
-14	4/3	-60	VB - VC	iob	-90	(4*3^(1/2))/3	Vki	[VB - VA - VC, VC - VB - VA, VB - VA - VC]
-23	4/3	-60	VB - VC	iob	-90	(4*3^(1/2))/3	Vki	[VA + VB - VC, VA - VB + VC, VA + VB - VC]
6	4/3	-60	VA - VC	iob	-150	(4*3^(1/2))/3	Vki	[VA - VC, VC - VA, VA - VC]
15	4/3	-60	VA - VC	iob	-150	(4*3^(1/2))/3	Vki	[VA + VB - VC, VB - VA + VC, VA + VB - VC]
24	4/3	-60	VA - VC	iob	-150	(4*3^(1/2))/3	Vki	[VA - VB - VC, VC - VB - VA, VA - VB - VC]
-6	4/3	120	VA - VC	iob	30	(4*3^(1/2))/3	Vki	[VC - VA, VA - VC, VC - VA]
-15	4/3	120	VA - VC	iob	30	(4*3^(1/2))/3	Vki	[VB - VA + VC, VA + VB - VC, VB - VA + VC]
-24	4/3	120	VA - VC	iob	30	(4*3^(1/2))/3	Vki	[VC - VB - VA, VA - VB - VC, VC - VB - VA]
7	4/3	-120	VA - VB	ioc	-30	(4*3^(1/2))/3	Vki	[VB - VA, VB - VA, VA - VB]
16	4/3	-120	VA - VB	ioc	-30	(4*3^(1/2))/3	Vki	[VB - VA + VC, VB - VA + VC, VA - VB + VC]
25	4/3	-120	VA - VB	ioc	-30	(4*3^(1/2))/3	Vki	[VB - VA - VC, VB - VA - VC, VA - VB - VC]
-7	4/3	60	VA - VB	ioc	150	(4*3^(1/2))/3	Vki	[VA - VB, VA - VB, VB - VA]
-16	4/3	60	VA - VB	ioc	150	(4*3^(1/2))/3	Vki	[VA - VB - VC, VA - VB - VC, VB - VA - VC]
-25	4/3	60	VA - VB	ioc	150	(4*3^(1/2))/3	Vki	[VA - VB + VC, VA - VB + VC, VB - VA + VC]
8	4/3	-120	VB - VC	ioc	90	(4*3^(1/2))/3	Vki	[VC - VB, VC - VB, VB - VC]
17	4/3	-120	VB - VC	ioc	90	(4*3^(1/2))/3	Vki	[VA - VB + VC, VA - VB + VC, VA + VB - VC]
26	4/3	-120	VB - VC	ioc	90	(4*3^(1/2))/3	Vki	[VC - VB - VA, VC - VB - VA, VB - VA - VC]
-8	4/3	60	VB - VC	ioc	-90	(4*3^(1/2))/3	Vki	[VB - VC, VB - VC, VC - VB]
-17	4/3	60	VB - VC	ioc	-90	(4*3^(1/2))/3	Vki	[VB - VA - VC, VB - VA - VC, VC - VB - VA]
-26	4/3	60	VB - VC	ioc	-90	(4*3^(1/2))/3	Vki	[VA + VB - VC, VA + VB - VC, VA - VB + VC]
9	4/3	60	VA - VC	ioc	-150	(4*3^(1/2))/3	Vki	[VA - VC, VA - VC, VC - VA]
18	4/3	60	VA - VC	ioc	-150	(4*3^(1/2))/3	Vki	[VA - VB - VC, VA - VB - VC, VC - VB - VA]
27	4/3	-120	VA - VC	ioc	30	(4*3^(1/2))/3	Vki	[VC - VB - VA, VC - VB - VA, VA - VB - VC]
-9	4/3	-120	VA - VC	ioc	30	(4*3^(1/2))/3	Vki	[VC - VA, VC - VA, VA - VC]
-18	4/3	-120	VA - VC	ioc	30	(4*3^(1/2))/3	Vki	[VB - VA + VC, VB - VA + VC, VA + VB - VC]
-27	4/3	60	VA - VC	ioc	-150	(4*3^(1/2))/3	Vki	[VA + VB - VC, VA + VB - VC, VB - VA + VC]

Figure B.3: Definitions of the 54 voltage and current vectors which generate $V_{TKj} = V_{Ki}$

State Number	Vo_mag	<Vo	Vo_coeff	Ii_coeff	<Ii	Ii_mag	VTK	[Vao, Vbo, Vco]
1C	4/3	0	VA - VB	ioa	-30	(4*3^(1/2))/3	-Vki	[VA - VB, VB - VA, VB - VA]
10C	4/3	0	VA - VB	ioa	-30	(4*3^(1/2))/3	-Vki	[VA - VB - VC, VB - VA - VC, VB - VA - VC]
19C	4/3	0	VA - VB	ioa	-30	(4*3^(1/2))/3	-Vki	[VA - VB + VC, VB - VA + VC, VB - VA + VC]
-1C	4/3	180	VA - VB	ioa	150	(4*3^(1/2))/3	-Vki	[VB - VA, VA - VB, VA - VB]
-10C	4/3	180	VA - VB	ioa	150	(4*3^(1/2))/3	-Vki	[VB - VA + VC, VA - VB + VC, VA - VB + VC]
-19C	4/3	180	VA - VB	ioa	150	(4*3^(1/2))/3	-Vki	[VB - VA - VC, VA - VB - VC, VA - VB - VC]
2C	4/3	0	VB - VC	ioa	90	(4*3^(1/2))/3	-Vki	[VB - VC, VC - VB, VC - VB]
11C	4/3	0	VB - VC	ioa	90	(4*3^(1/2))/3	-Vki	[VB - VA - VC, VC - VB - VA, VC - VB - VA]
20C	4/3	0	VB - VC	ioa	90	(4*3^(1/2))/3	-Vki	[VA + VB - VC, VA - VB + VC, VA - VB + VC]
-2C	4/3	180	VB - VC	ioa	-90	(4*3^(1/2))/3	-Vki	[VC - VB, VB - VC, VB - VC]
-11C	4/3	180	VB - VC	ioa	-90	(4*3^(1/2))/3	-Vki	[VA - VB + VC, VA + VB - VC, VA + VB - VC]
-20C	4/3	180	VB - VC	ioa	-90	(4*3^(1/2))/3	-Vki	[VC - VB - VA, VB - VA - VC, VB - VA - VC]
3C	4/3	180	VA - VC	ioa	-150	(4*3^(1/2))/3	-Vki	[VC - VA, VA - VC, VA - VC]
12C	4/3	180	VA - VC	ioa	-150	(4*3^(1/2))/3	-Vki	[VC - VB - VA, VA - VB - VC, VA - VB - VC]
21C	4/3	180	VA - VC	ioa	-150	(4*3^(1/2))/3	-Vki	[VB - VA + VC, VA + VB - VC, VA + VB - VC]
-3C	4/3	0	VA - VC	ioa	30	(4*3^(1/2))/3	-Vki	[VA - VC, VC - VA, VC - VA]
-12C	4/3	0	VA - VC	ioa	30	(4*3^(1/2))/3	-Vki	[VA + VB - VC, VB - VA + VC, VB - VA + VC]
-21C	4/3	0	VA - VC	ioa	30	(4*3^(1/2))/3	-Vki	[VA - VB - VC, VC - VB - VA, VC - VB - VA]
4C	4/3	120	VA - VB	iob	-30	(4*3^(1/2))/3	-Vki	[VB - VA, VA - VB, VB - VA]
13C	4/3	120	VA - VB	iob	-30	(4*3^(1/2))/3	-Vki	[VB - VA + VC, VA - VB + VC, VB - VA + VC]
22C	4/3	120	VA - VB	iob	-30	(4*3^(1/2))/3	-Vki	[VB - VA - VC, VA - VB - VC, VB - VA - VC]
-4C	4/3	-60	VA - VB	iob	150	(4*3^(1/2))/3	-Vki	[VA - VB, VB - VA, VA - VB]
-13C	4/3	-60	VA - VB	iob	150	(4*3^(1/2))/3	-Vki	[VA - VB + VC, VB - VA + VC, VA - VB + VC]
-22C	4/3	-60	VA - VB	iob	150	(4*3^(1/2))/3	-Vki	[VA - VB - VC, VB - VA - VC, VA - VB - VC]
5C	4/3	120	VB - VC	iob	90	(4*3^(1/2))/3	-Vki	[VC - VB, VB - VC, VC - VB]
14C	4/3	120	VB - VC	iob	90	(4*3^(1/2))/3	-Vki	[VA - VB + VC, VA + VB - VC, VA - VB + VC]
23C	4/3	120	VB - VC	iob	90	(4*3^(1/2))/3	-Vki	[VC - VB - VA, VB - VA - VC, VC - VB - VA]
-5C	4/3	-60	VB - VC	iob	-90	(4*3^(1/2))/3	-Vki	[VB - VC, VC - VB, VB - VC]
-14C	4/3	-60	VB - VC	iob	-90	(4*3^(1/2))/3	-Vki	[VB - VA - VC, VC - VB - VA, VB - VA - VC]
-23C	4/3	-60	VB - VC	iob	-90	(4*3^(1/2))/3	-Vki	[VA + VB - VC, VA - VB + VC, VA + VB - VC]
6C	4/3	-60	VA - VC	iob	-150	(4*3^(1/2))/3	-Vki	[VA - VC, VC - VA, VA - VC]
15C	4/3	-60	VA - VC	iob	-150	(4*3^(1/2))/3	-Vki	[VA + VB - VC, VB - VA + VC, VA + VB - VC]
24C	4/3	-60	VA - VC	iob	-150	(4*3^(1/2))/3	-Vki	[VA - VB - VC, VC - VB - VA, VA - VB - VC]
-6C	4/3	120	VA - VC	iob	30	(4*3^(1/2))/3	-Vki	[VC - VA, VA - VC, VC - VA]
-15C	4/3	120	VA - VC	iob	30	(4*3^(1/2))/3	-Vki	[VB - VA + VC, VA + VB - VC, VB - VA + VC]
-24C	4/3	120	VA - VC	iob	30	(4*3^(1/2))/3	-Vki	[VC - VB - VA, VA - VB - VC, VC - VB - VA]
7C	4/3	-120	VA - VB	ioc	-30	(4*3^(1/2))/3	-Vki	[VB - VA, VB - VA, VA - VB]
16C	4/3	-120	VA - VB	ioc	-30	(4*3^(1/2))/3	-Vki	[VB - VA + VC, VB - VA + VC, VA - VB + VC]
25C	4/3	-120	VA - VB	ioc	-30	(4*3^(1/2))/3	-Vki	[VB - VA - VC, VB - VA - VC, VA - VB - VC]
-7C	4/3	60	VA - VB	ioc	150	(4*3^(1/2))/3	-Vki	[VA - VB, VA - VB, VB - VA]
-16C	4/3	60	VA - VB	ioc	150	(4*3^(1/2))/3	-Vki	[VA - VB - VC, VA - VB - VC, VB - VA - VC]
-25C	4/3	60	VA - VB	ioc	150	(4*3^(1/2))/3	-Vki	[VA - VB + VC, VA - VB + VC, VB - VA + VC]
8C	4/3	-120	VB - VC	ioc	90	(4*3^(1/2))/3	-Vki	[VC - VB, VC - VB, VB - VC]
17C	4/3	-120	VB - VC	ioc	90	(4*3^(1/2))/3	-Vki	[VA - VB + VC, VA - VB + VC, VA + VB - VC]
26C	4/3	-120	VB - VC	ioc	90	(4*3^(1/2))/3	-Vki	[VC - VB - VA, VC - VB - VA, VB - VA - VC]
-8C	4/3	60	VB - VC	ioc	-90	(4*3^(1/2))/3	-Vki	[VB - VC, VB - VC, VC - VB]
-17C	4/3	60	VB - VC	ioc	-90	(4*3^(1/2))/3	-Vki	[VB - VA - VC, VB - VA - VC, VC - VB - VA]
-26C	4/3	60	VB - VC	ioc	-90	(4*3^(1/2))/3	-Vki	[VA + VB - VC, VA + VB - VC, VA - VB + VC]
9C	4/3	60	VA - VC	ioc	-150	(4*3^(1/2))/3	-Vki	[VA - VC, VA - VC, VC - VA]
18C	4/3	60	VA - VC	ioc	-150	(4*3^(1/2))/3	-Vki	[VA - VB - VC, VA - VB - VC, VC - VB - VA]
27C	4/3	-120	VA - VC	ioc	30	(4*3^(1/2))/3	-Vki	[VC - VB - VA, VC - VB - VA, VA - VB - VC]
-9C	4/3	-120	VA - VC	ioc	30	(4*3^(1/2))/3	-Vki	[VC - VA, VC - VA, VA - VC]
-18C	4/3	-120	VA - VC	ioc	30	(4*3^(1/2))/3	-Vki	[VB - VA + VC, VB - VA + VC, VA + VB - VC]
-27C	4/3	60	VA - VC	ioc	-150	(4*3^(1/2))/3	-Vki	[VA + VB - VC, VA + VB - VC, VB - VA + VC]

Figure B.4: Definitions of the 54 complimentary voltage and current vectors which generate $V_{TKj} = -V_{Ki}$