A Novel N-phase Multi-Modular Series HVDC Tap

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Abstract

High-voltage direct-current (HVDC) transmission has higher efficiency and lower expenses for the long-distance bulk-power transmission. A HVDC tap is one type of the multi-terminal HVDC systems which transfers a small amount of power from the HVDC line to the nearby communities with no access to the electricity.

Developed from the 1960s, HVDC taps can be summarised into series taps and parallel taps, between which series taps are considered to be more promising on the use of devices and the cost. The conventional series taps have some evident drawbacks, which a modular multilevel based series tap may overcome. Here a novel n-phase Multi-Modular Series HVDC Tap (MMST) is proposed to realise the utilisation of the modular multilevel structure into the series tap and improve the performance of typical series taps.

In this PhD thesis the theoretical analysis and the parameter design of two-phase and three-phase MMSTs based on the South-West HVDC Link in Sweden have been carried out. The control strategy for the n-phase MMST, including the load current control, the mean capacitor voltage control and the DC link voltage control, has been designed. In order to verify the feasibility of the proposed topology and the validity of the presented control strategy, simulations have been validated using a low power prototype. The simulation and experimental results indicate that the MMST offers better performance when compared to the conventional series taps.

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Glossary of Terms

AAC	Alternate arm converter
AC	Alternating current
CHB	Cascaded H-bridge converter
CSC	Current source converter
DC	Direct current
DSK	Development starter kit
DSP	Digital Signal Processor
FC	Flying capacitor converter
FCC	Force commutated converter
FMA	Fundamental mode approximation
FPGA	Field Programmable Gate Array
GTO	Gate Turn-off Thyristor
HPI	Host Post Interface
HV	High voltage
HVAC	High voltage alternating current
HVDC	High voltage direct current
IGBT	Insulated Gate Bipolar Translator
IGCT	Integrated Gate Commutated Thyristor
LC	Inductor and capacitor
LCC	Line commutated converter
LCR	Inductor, capacitor and resistor
MMC	Modular multilevel converter
MMST	Modular multilevel series tap
MV	Medium voltage
MVAC	Medium voltage alternating current
NLC	Nearest level control
NPC	Neutral-point diode clamped converter
PC	Personal Computer
PI	Proportional Integral
PR	Proportional Resonant

PWM	Pulse Width Modulation
RCD	Resistor, capacitor and diode
RMS	Root Mean Square
SPWM	Sinusoidal Pulse Width Modulation
TF	Transfer function
THD	total Harmonic Distortion
VSC	Voltage source converter
WHO	World Health Organization
ZCS	Zero current switching
ZVS	Zero voltage switching

List of Symbols

x	Instantaneous value of a generic variable
X	RMS value of x
$\widehat{X}$	Peak value of x
$\overline{x}$	Average value of x
A_w	Window winding area
A_c	Cross section area of the magnetic core
A_l	Cross sectional area of the copper coil
A_p	Product of window winding area and the cross section area of magnetic core
C_{Blk}	Blocking capacitor
C_f	Equivalent blocking capacitor
C_{filter}	DC grid filtering capacitor in the experiments
C_{SM}	Capacitor in the sub-module
d	Diameter of a single wire in the branch inductor
e_{off}	Turn-off loss of one IGBT
e_{on}	Turn-on loss of one IGBT
e_{rec}	Reverse recovery loss of one diode
e_{swit}	Switching loss energy of one sub-module
e_{tap-i}	Instantaneous tap energy of phase i
E_{tap}	Total energy change of the MMST
f_f	Operating frequency of the MMST
f_s	Switching frequency of the MMST
$G_{AC}(s)$	Equivalent stationary PR regulator
$G_{DC}(s)$	Conventional integrator
i_0	Sub-module current
i_a, i_b, i_c	AC component of tap currents in the three-phase series tap
i_{AC}	AC loop current
i_{DC1}	Experimental DC current from the DC grid 1
i_{har}	Harmonics in the MMST branch

i_l	Load current
i_m	Current of the middle branch
i_{S1}	Arm current of String 1
i_{S2}	Arm current of String 2
i_{S-circ}	Circulating current
i_{tap}	Tap arm current
I_{DC}	DC line current
$\hat{I}_{SM}$	Maximum current that sub-module can conduct normally
k_{i-y}	Coefficient of integral term in the control of y
k_{p-y}	Coefficient of proportional term in the control of y
k_{r-y}	Coefficient of resonant term in the control of y
L_{arm}	Arm inductor for circulating current balancing
L_b	Inductor on the damping branch
L_{CC}	Chopper inductor in the experiments
L_f	Branch inductor
m_i	Modulation index
n_{Blk}	Number of blocking capacitors
n_{level}	Number of level of the specific waveform
n_{ls}	Number of level-shifted carriers
n_{LA55P}	Turns ratio of LA-55P
n_{LV25P}	Turns ratio of LV-25P
n_{modu}	Number of inserted sub-modules in one arm
n_{ph}	Number of phases
n_{ps}	Number of phase-shifted carriers
$n_{R_{CC}}$	Number of the inserted resistors in the chopper circuit
n_{strand}	Number of strands in the conductor
n_{string}	Number of strings in one arm
n_{SM}	Number of sub-modules in one tap arm
$p_{cond-diode}$	Conduction losses of all the diodes in the MMST
$p_{cond-IGBT}$	Conduction losses of all the IGBTs in the MMST
p_{loss}	Total losses of MMST sub-modules
p_{swit}	Switching loss of one sub-module
p_{tap-i}	Tap power of a single phase
P_{AC}	AC component of the tap power
$P_{cond-tot}$	Total conduction losses of the MMST
P_{cu}	Copper loss of the inductor
P_{DC}	DC component of the tap power
P_{fe}	Core loss of the inductor
P_{fe0}	Core loss per unit volume
P_{loss-L}	Power losses of the inductors in the two-phase MMST
P_{tap}	Total tap power
R_1	External resistor of the transducers
R_{CC}	Chopper resistor in the experiments
R_f	Resistor on the damping branch
R_{filter}	DC grid filtering resistor in the experiments

R_{load}	MMST resistive load in the experiments
R_M	Measuring resistor of the transducers
R_{thC-H}	Thermal resistance of case-to-heat sink
R_{th-HS}	Thermal resistance of heat sink
R_{thJ-C}	Thermal resistance of junction-to-case
T_{air}	Ambient temperature
T_j	Junction temperature of the IGBT
v_a, v_b, v_c	Three-phase output voltage
$v_{AC-avail}$	The voltage available for the tap AC voltage
v_{AC-i}	AC component of the tap voltage
v_{C-mean}	Mean capacitor voltage per arm
v_{Cblock}	Voltage of experimental blocking capacitors
$v_{Chopper}$	Voltage of the chopper circuit
v_{in}	Input voltage
v_{IGBT}	Nominal IGBT operating voltage
v_l	Load voltage
v_{SM}	Voltage of a single sub-module
v_{tap}	Voltage of the series tap on a HVDC line
v_{tap-i}	Tap arm voltage of the MMST
v_{out}	Output voltage
$V_{AC-bound}$	Boundary tap voltage of single and parallel strings
V_{Blk}	Rated voltage of the blocking capacitor
V_C	Voltage of the sub-module capacitor
V_{C-ref}	Reference voltage of mean capacitor voltage control
V_{DC}	DC voltage of a single tap arm
V_{DC-tot}	Total DC voltage of the MMST
V_{GE}	Gate drive voltage of the IGBT
V_{HVDC}	HVDC voltage
V_{ripple}	Voltage ripple on the capacitor in the sub-module
Z_0	Branch impedance
Z_f	Equivalent branch impedance
δ	Skin depth of the conductor
η_{closed}	Efficiency of closed-loop experiments of the two-phase MMST
η_{open}	Efficiency of open-loop experiments of the two-phase MMST
η_{simu}	Efficiency of closed-loop simulation of the two-phase MMST
η_{three}	Loss percentage of sub-module arms in the three-phase MMST
η_{two}	Loss percentage of sub-module arms in the two-phase MMST
θ	Phase shift between tap AC current and voltage
θ_0	Initial phase angle of the load voltage
τ_{PR}	Time constant in the PR control system
ω	Angular speed of the AC voltage
ω_C	Cutoff frequency of the non-ideal PR regulator

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Chapter 1

Introduction

1.1 Motivation

HVDC transmission is known to be more efficient and less expensive than high-voltage alternating-current (HVAC) transmission over distances greater than the break even distance [1]. HVDC is beneficial for optimising the allocation of global energy, saving the energy consumption on the transportation, and reaching renewable energy penetration requirements.

Most of the HVDC systems are point-to-point transmission, for example from a hydropower station in Central Africa to Southern African regions [2]. However, there are still 1.2 billion people that cannot get access to a stable electricity supply [3]. Orthodox methods for the provision of electricity supplies to them, such as a central power station with a transmission and distribution network, may not be the most economical means of providing electricity supplies in developing countries, particularly in rural areas where the demand per customer is only a small fraction of a kilowatt [4]. In such circustmances being able to connect directly to a nearby HVDC transmission network would be desirable and marketable. For this reason a novel HVDC-to-Medium Voltage Alternating Current (MVAC) conversion method is required, this type of connection is referred to here as an *HVDC Tap*. Compared to

the main system the HVDC tap transfers a suitably small power (1%∼10%) to the local customers [5].

The proposed HVDC taps in the literature can be separated into two categories: series and parallel taps [5]. A series tap inserts a direct current (DC) voltage inline with the HVDC transmission line. The interaction with the existing transmission current and this voltage results in power being transferred from the line. A parallel tap utilises the full HVDC voltage such that a relatively small additional current is drawn by the tap. Series taps have a number of advantages considering the efficient utilisation of devices, power losses, cost and volume over parallel taps in the application of HVDC taps [6].

Several series taps have been proposed since the 1960s [7], most of which comprise a first-stage DC/AC converter and a second-stage AC/DC/AC converter with a high-voltage (HV) rated isolation transformer T_1 between the two stages, as shown in Fig 1.1. The first-stage converter is commonly an H-bridge inverter with different implementations ranging from line-commutated semiconductor devices to self-commutated devices. Due to a current sourced characteristic of the first-stage converter, a second-stage converter is normally needed for transferring the current source into an AC voltage source and supply to the remote communities. The previously proposed series taps have the disadvantages of: the need for an HV rated isolation transformer, injection of significant harmonics into the HVDC system, and the voltage sharing problem of the series semiconductor devices as a single switch. In addition, the components used in parallel taps evolute from line-commutated to self-commutated devices, then to sub-modules, but the components in series taps only evolute from line-commutated to self-commutated devices. Therefore, the modular multilevel based series taps, which would be the next generation of the series taps, might be helpful to overcome these problems.

The simplest way of realising the modular multilevel based series tap is to insert a modular multilevel converter (MMC) in series with the HVDC line, but published papers have rarely discussed it before. The series MMC can optimise the harmonics problem and the problem of series devices owing to the features of the modular mul-

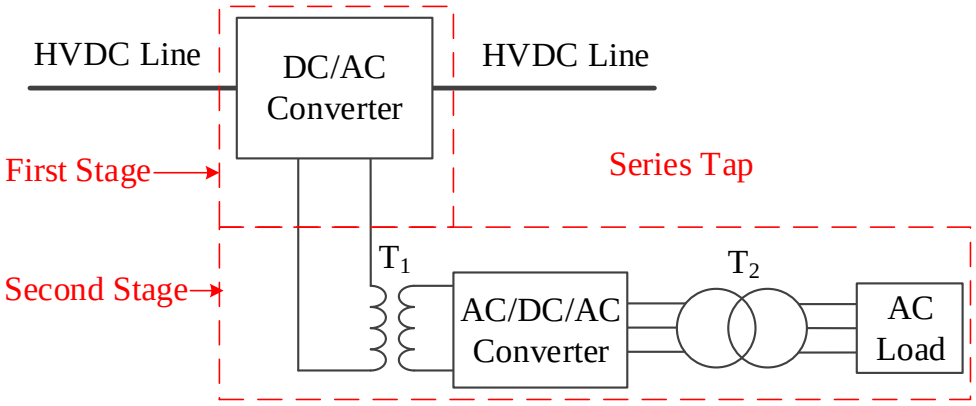


Figure 1.1: Schematic diagram of series taps

tilevel structure itself. Nonetheless the isolation transformer is still necessary, and the modular multilevel structure leads to a higher filtering capability for the second stage (explained in Section 2.2.2), which is even worse than those of typical series taps. **The motivation of the work is therefore to research and develop an innovative modular multilevel based series tap topology which can fully exploit the advantages of the modular multilevel structure and remove the need for the HV rated isolation transformer.**

1.2 Contribution

A novel series HVDC tap, called the n-phase Multi-Modular Series Tap, is proposed. The work that has been undertaken includes the topology innovation and development, control strategy development, detailed theoretical and simulation studies and experimental validation. The contributions of this work are introduced as follows.

1. A novel n-phase MMST with the modular multilevel structure has been proposed. The n-phase MMST can generate any number of phases by the configuration of two types of tap branches. It utilises the modular multilevel structure into the conventional series tap properly, injecting few harmonics into the HVDC network, and removing the need for an HV rated isolation transformer. The detailed operating principle and topology design are introduced

in Chapter 3.

2. Based on the control strategy presented in Chapter 4, a method for eliminating the effects of harmonics from the HVDC grid and MMST on the control system by alternative sampling variables has been proposed and verified in the simulations and experiments. The MMST and power electronics converters in real HVDC systems can generate the harmonics with frequencies close to the resonant frequency of inductor and capacitor (LC) blocking branches, which results in an obvious disturbance in the sampled values, mainly the arm and loop currents. To solve this problem, the load current is sampled per phase and values of arm and loop currents are calculated from load current values and the line current value. This method has no effects on the steady-state operation of the MMST but slows down the transient response speed.

3. The steady-state simulation and the transient- and steady-state experiments verifying the feasibility of the n-phase MMST and the validity of the control strategy have been carried out based on a 6.5kW prototype design. A method for pre-charging the sub-module capacitors has been devised and demonstrated.

1.3 Thesis Structure

Chapter 2 mainly explains the motivation of this work. The development situation of the global energy, HVDC, HVDC taps and multilevel converters in the literature are described. The categories and the development tendencies of HVDC taps are specified. The justification of the research topic based on series taps is given, including the justification for using a modular multilevel structure in the new series tap. Problems that may still exists in the modular multilevel series taps are explained.

Chapter 3 proposes a novel n-phase multi-modular series HVDC tap which has advantages and solves the problems of the modular multilevel series tap discussed in Chapter 2. The operating principle of the n-phase MMST is introduced. The topology design of a two-phase and a three-phase MMST are specified and compared based

on the South West Link Project in Sweden. The methods of selecting the numbers of sub-modules, sub-module capacitor size, LC values in the blocking branch and the analysis of the sub-module power losses based on specific design parameters are introduced.

Chapter 4 presents a control strategy that can allow MMSTs with any phase number to operate in a practical HVDC system. The analyses of the PR current control loop, mean capacitor voltage control loop and the DC link voltage control loop are given. The design of the regulators is also given. The simulation of a two-phase MMST under closed-loop operation has been carried out in PLECS software and the simulation results of the load and arm voltages and currents, and the sub-module capacitor voltages are demonstrated.

Chapter 5 introduces the design of the experimental rig for a two-phase MMST and explains why the experimental results can prove the feasibility of the n-phase MMST and the validity of the control strategy. The detailed design procedure of the rig is given. A solution to the harmonics problem which exists in the experiments and most likely in the real application has been presented.

Chapter 6 shows the experimental and simulation results for the two-phase MMST under open-loop and closed-loop operation. The results prove the validity of a two-phase MMST, which indicates the feasibility of the n-phase MMST and the validity of the control strategy. The start-up method of the rig is also presented.

Chapter 7 concludes the thesis and proposes the potential future work.

Chapter 2

Literature Review

This chapter presents a literature review of HVDC systems, HVDC taps and multilevel converters. The merits and drawbacks of the various technologies used are discussed. The concept of the proposed topology further investigated in this thesis is introduced and how the ideas relate to previous work are explained.

Section 2.1 describes the necessity of HVDC and the development prospect of the HVDC tap. Section 2.2 demonstrates the configuration of HVDC taps and summarises the development tendencies of series taps and parallel taps. Section 2.3 introduces existing multilevel converters and explains the problems of introducing multilevel converters into the series tap.

2.1 HVDC and HVDC Taps

2.1.1 Introduction on HVDC

The severe condition of global energy reflects the significance of the development of renewable energy [3, 8, 9]. Renewable energy, such as solar energy near the equator and wind energy in the Arctic Ocean, is abundant but normally distributed distantly from the electricity consumption area [10, 11]. To supply renewable energy to the

urban customers, optimise the allocation of resources and improve the environment of urban areas, long-distance bulk-power transmission technologies, which are HVDC and HVAC transmission, are necessary.

Compared to HVAC systems, HVDC systems have a number of advantages for bulk power transmission such as [12–14]:

- Lower costs and losses of HVDC transmission systems, as two transmission lines are needed rather than four although the costs and losses of the HVDC terminals are higher than those of HVAC terminals. HVDC systems are more efficient and less expensive than HVAC system over distances greater than the break even distance [1].
- The power factor of AC systems is not unity due to the impedance of the line - especially for long lines unless extra compensation measures are taken.
- The skin effect doesn't exist in DC conductor, so the HVDC transmission has higher efficiency and larger power capacity.
- The frequency and phase problems do not need to be considered in the design and grid-tied connection of the HVDC system. It is technically impossible to connect two AC systems with different frequencies and phases.

In order to optimise the allocation of global energy and cooperate with the development of renewable energy, HVDC technology is demanded. HVDC lines are already constructed or under operation in many places. Many industries including ABB, Siemens, GE and State Grid as well as many universities offer strong acceleration of every aspect of HVDC techniques [15–19]. By 2050 the global grids may be interconnected by HVDC transmission lines [20].

First proposed in 1882 [21], HVDC technology developed following the innovation of the power semiconductor devices. The evolution of the power converters in HVDC systems are from line commutated converter (LCC) [22] to voltage source converters (VSC) [23] then to MMCs [24], with the semiconductor devices developing from line-commutated devices [25] to self-commutated devices [26] then to sub-modules [27],

respectively. The development of HVDC system closely reflects the development of power electronics along with the innovation of semiconductor devices.

2.1.2 HVDC Taps in Multi-terminal HVDC Systems

According to the different applications and locations, HVDC transmission systems have several configurations which include back-to-back converters, monopolar transmissions, bipolar transmissions and multi-terminal systems [13]. Nowadays bipolar transmission is most widely accepted owing to the reduced cost, lower power losses under the same power rating, and fault handling capability with two lines.

Most of the HVDC systems use point-to-point monopolar or bipolar transmission although multi-terminal systems are developing [28]. The configuration of multiple terminal systems can have series, parallel, or hybrid (a mixture of series and parallel) terminals [29]. A five terminal HVDC system was built in Zhoushan in which the five terminals have similar power ratings [30, 31]. However, according to the power demand of each terminal, the power rating of each one is not necessarily the same as the others, i.e. one terminal can transfer a relatively small power compared to the other terminals in the multi-terminal system [5].

Small remote communities benefit from an external electricity connection to ensure their energy demands can be reliably met. In such cases connecting a dedicated transmission line from the existing AC grid may be impractical. Under such circumstances being able to connect directly to a nearby newly constructed bulk-power HVDC transmission line would be desirable [14]. With the development of HVDC technology, a means to connect an HVDC-to-MVAC network would be beneficial and marketable. This type of connection is referred to here as an *HVDC Tap* [32].

The HVDC tap, as one component of the multi-terminal HVDC system, is beneficial to supply energy (including renewable energy) to the remote communities, realising ′Sustainable Energy for All′ as proposed by the United Nations [33]. Belonging to the collection of power converters used in HVDC systems, the development of the HVDC

tap also follows the developing pace of HVDC system technology, as presented below.

2.2 HVDC Taps

The main requirements of an HVDC tap are [6, 34]:

- Suitably small power rating compared with the main HVDC system, typically 1%-10% [5].
- Negligible impact on the reliability of the main HVDC system, i.e. a fault on the HVDC tap should not shut the whole HVDC system down.
- Individual control system for the HVDC tap which doesn't interface with the main HVDC system control.
- Reduced fixed cost and limited volume.

Many different HVDC tap converters, with various ways of connection, power levels and influence on the HVDC systems, have been proposed since the 1960s. The proposed HVDC taps in the literature can be separated into two categories: the parallel tap and the series tap [5]. The schematic diagrams of the parallel tap and series tap are shown in Fig 2.1 [35].

1. Parallel Tap

   The parallel tap is connected in parallel with the HVDC transmission line, as shown in Fig 2.1(a). It operates under the same voltage as the DC line voltage, thus the current rating is only 1%-10% of the DC line current. Considering the installed cost and operating efficiency, parallel taps are more applied where the power ratings are similar with those of the HVDC terminals. Two high-voltage DC circuit breakers are necessary for the protection of the tap when an HVDC fault happens or for the tap insulation if the tap is broken down [32].

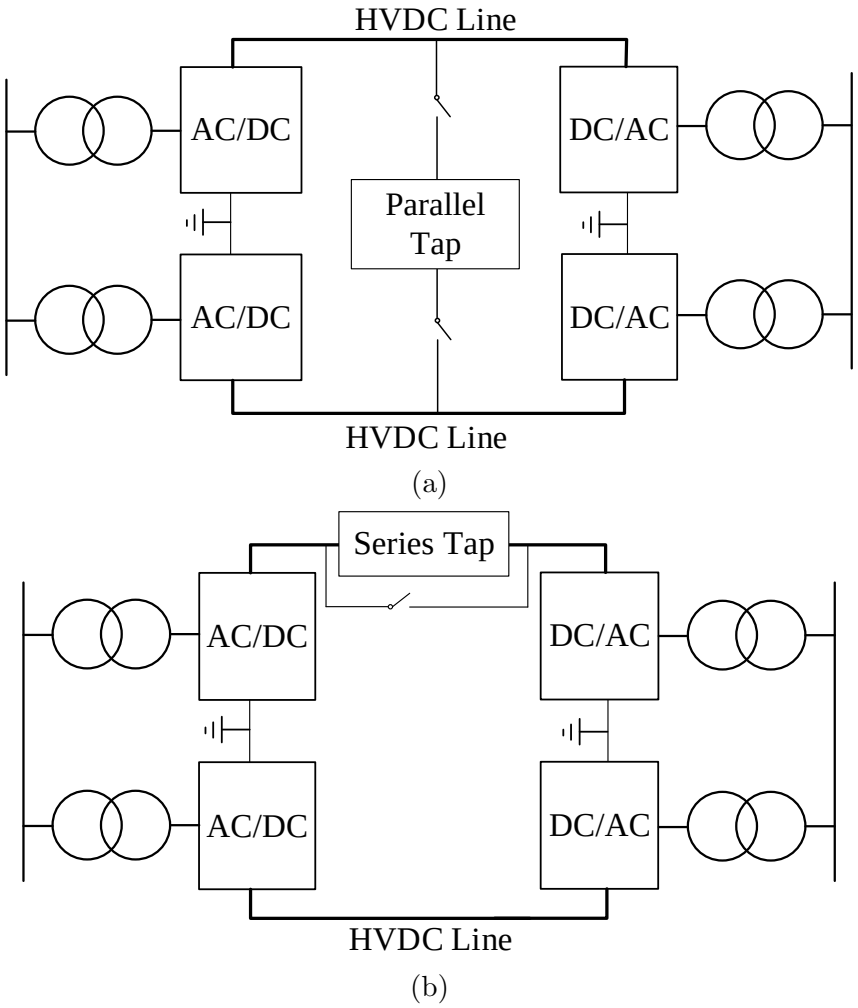


Figure 2.1: Schametic diagrams of the parallel tap and the series tap: (a) Parallel tap, (b) Series tap.

2. Series Tap

   As shown in Fig 2.1(b), the series tap is inserted in series with the HVDC line. As the power rating of the series tap is 1%-10% of the HVDC system and the current rating equals the HVDC line current, it only needs to introduce normally less than 10% of the line voltage. With the series tap, the necessary compensation at the main terminals is minor and the additional regulating range is not high. In the event of a tap fault, a bypass switch can short-circuit the series tap and ensure the normal operation of the HVDC system [36].

2.2.1 Parallel Taps

The parallel tap, as discussed above, has to withstand the full HVDC voltage but only conducts a small fraction of the HVDC current. Two possible categories of parallel taps are shown in Fig 2.2 [37]. A conventional design, shown in Fig 2.2(a), contains a DC/AC converter and a three-phase step-down transformer (or three single-phase transformers depending on the applications). An alternative architecture is shown in Fig 2.2(b), where the DC/DC converter steps down the HVDC voltage and the DC/AC converter can be operated at a medium voltage rating.

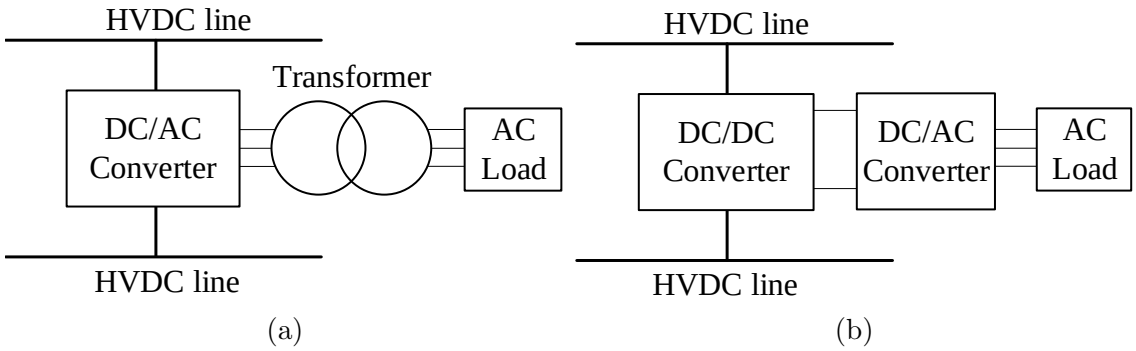


Figure 2.2: Categories of parallel taps: (a) Conventional parallel tap, (b) Alternative parallel tap.

Conventional Parallel Taps

As shown in Fig 2.2(a), the topologies of the DC/AC converters in conventional parallel taps can be similar to those of the terminal converters, such as LCC with thyristors [32] (where AC Load in Fig 2.2(a) should be replaced with an AC network), VSC with IGBTs [38,39] or GTOs [40], or MMC with the sub-module structure [24]. The current rating of the parallel taps is 1%-10% of the HVDC line current, which is beneficial for selecting switches with lower current rating. The cost, however, is still high due to the massive number of series semiconductor devices for sustaining high DC voltage. In addition, the control to ensure the dynamic voltage sharing among the series devices should be carefully designed [41]. Therefore, the recent research on the conventional parallel taps are on series-input parallel-output *multilevel DC/AC*

converters, distributing the HVDC voltage on the converter level rather than the device level.

Compared to the conventional parallel taps, multilevel architectures of parallel taps provide the advantages of avoiding series connection of switches, operating at lower $\mathrm{d}v/\mathrm{d}t$ and reducing the isolation level of the transformers [42]. Several papers have discussed the design of multilevel DC/AC converters, which include multilevel LCC [42], multilevel VSC [43] and series-connected MMC [44, 45]. Fig 2.3 shows the schemetic diagram of the typical multilevel DC/AC converter which is composed of series DC/AC converters and a corresponding transformer with a parallel output to the AC load. The multilevel VSC is demonstrated specifically which contains a VSC and a parallel capacitor in each DC/AC converter [43]. With the voltage balancing of capacitors, each DC/AC converter can be treated as an individual inverter.

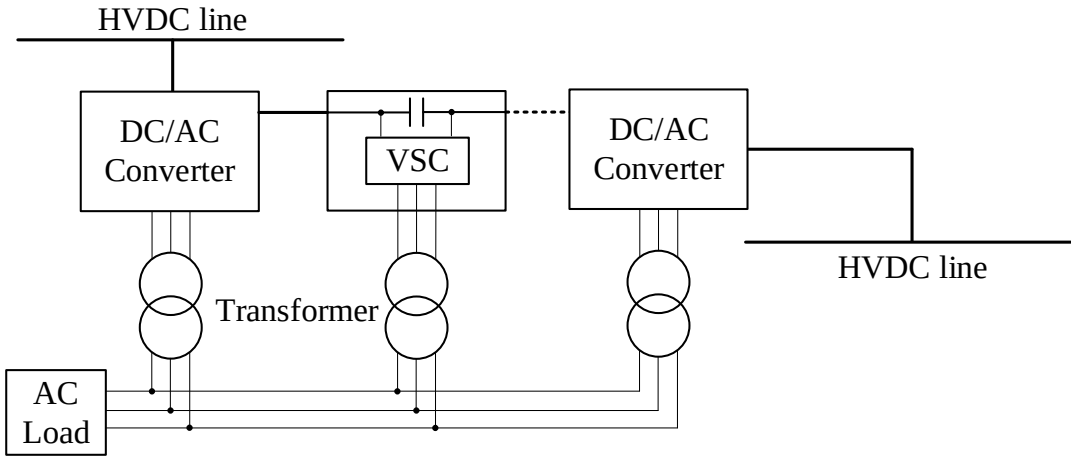


Figure 2.3: Schematic diagram of multilevel DC/AC converters

Alternative Parallel Taps

Rather than stepping down the HVDC voltage using isolation transformers in the traditional design, the DC/DC converter in some alternative topologies of parallel taps (Fig 2.2(b)) functions as the step-down component and the DC/AC converter can operate at a relatively low voltage, avoiding the need for an HV rated transformer although the HV isolation is still needed.

Several bidirectional DC/DC converters, such as thyristor DC transformer [46–48] and front-to-front DC/DC converter based on the MMC [49,50], can be summarised as a *front-to-front DC transformer*. The schematic diagram of the second type is shown in Fig 2.4. The MMC block can also be an alternate arm converter (AAC) which has the DC fault blocking capability [51]. In this topology two MMCs meet each other at the AC sides of an isolation transformer. Due to the multilevel structure of the MMC the fundamental frequency of the AC output can be relatively high, thus potentially reducing the volume of the transformer. From[37, 46–50] it can be concluded that the topology design and the control strategies of alternative parallel taps are complicated, and a large amount of devices are required.

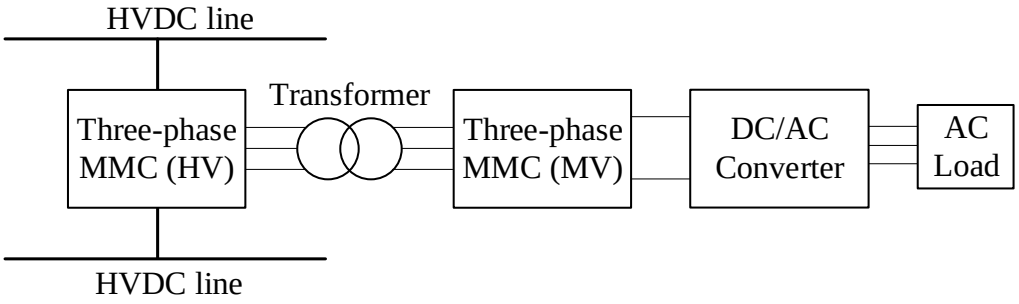


Figure 2.4: Schematic diagram of front-to-front DC transformers

In conclusion, parallel taps upgrade with the development of semiconductor devices. First proposed in 1963 [52], parallel taps with thyristor valves were the only option. After the invention of self-commutated devices, the parallel taps can be VSC based but they still need the series switches to sustain the DC voltage. To distribute the high voltage, taps designed with multilevel converters are proposed.

Parallel taps are quite feasible where the power of the tap is similar (50%) to the HVDC terminal. They are relatively simple to be designed and implemented into the DC grid in that the tap topologies can be obtained from the terminal converters. In addition, the point-to-point HVDC system itself can be treated as a parallel connection of two terminals. However, in applications of tapping 1%∼10% of the line power down to isolated communities, parallel taps have unavoidable drawbacks including [35]:

- Parallel taps operate under the full HVDC voltages and have high voltage step-down ratios. This leads to excessive use of devices, and a relatively low operating current which is challenging for reasonable use of device ratings.
- A tap DC fault may affect the main HVDC system. Two additional high-voltage DC circuit breakers are necessary for isolating the tap.

2.2.2 Series Taps

Due to the full utilisation of the HVDC current, less devices and flexible design, series taps have seen increasing interest since 1965 [7]. Series taps were initially proposed with a thyristor H-bridge due to the absence of self-commutated devices [32]. A force commutated converter (FCC) using a capacitor to force the thyristors to turn off was then proposed [34, 53, 54]. Because the series tap conducts full line current, this topology is a current source converter (CSC). Recently a tap using IGBTs (or GTOs, IGCTs) was proposed in [55]. Another topology, the soft-switching series tap, was discussed in [56–58], realising zero voltage switching (ZVS) when turning off and zero current switching (ZCS) when turning on. In conclusion, series taps normally have two stages: A DC/AC converter and an AC/AC converter, as shown in Fig 2.5 [34]. Here a single-phase topology is selected to show a concept structure of the conventional series tap.

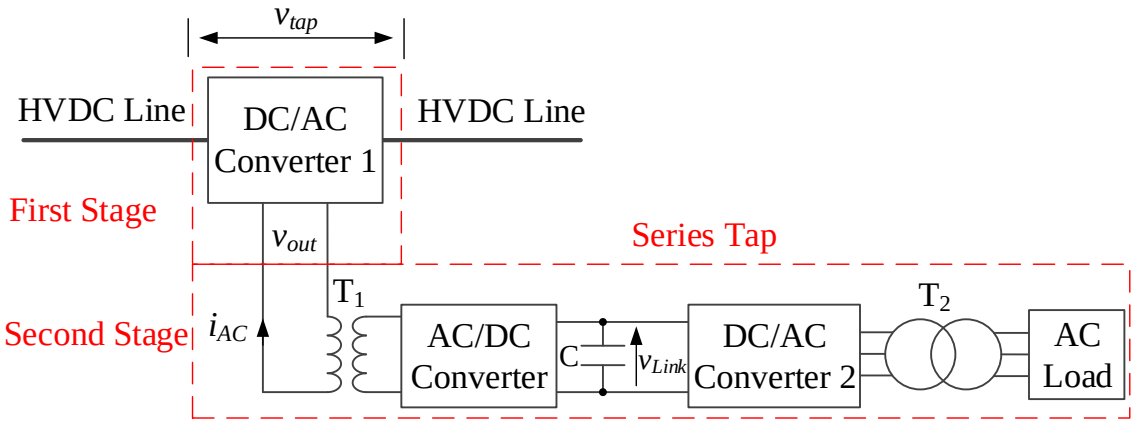


Figure 2.5: Concept structure of the HVDC series tap

The first-stage converter, named the DC/AC converter 1 in Fig 2.5, inverts HVDC to MVAC by various types of inverters shown in Fig 2.6. The second-stage AC/AC converter, consisting of an HV rated isolation transformer T_1, an AC/DC converter, a filtering capcitor C, a second DC/AC converter and a MV rated isolation transformer, transforms the AC output from the first stage to the load. The AC/DC converter in the second stage is often a diode rectifier, but can also be VSC if bidirectional power transmission is required. The second DC/AC converter can be a single-phase or three-phase LCC, VSC or MMC according to the applications and demands. In this work the first-stage converter is mainly focused on.

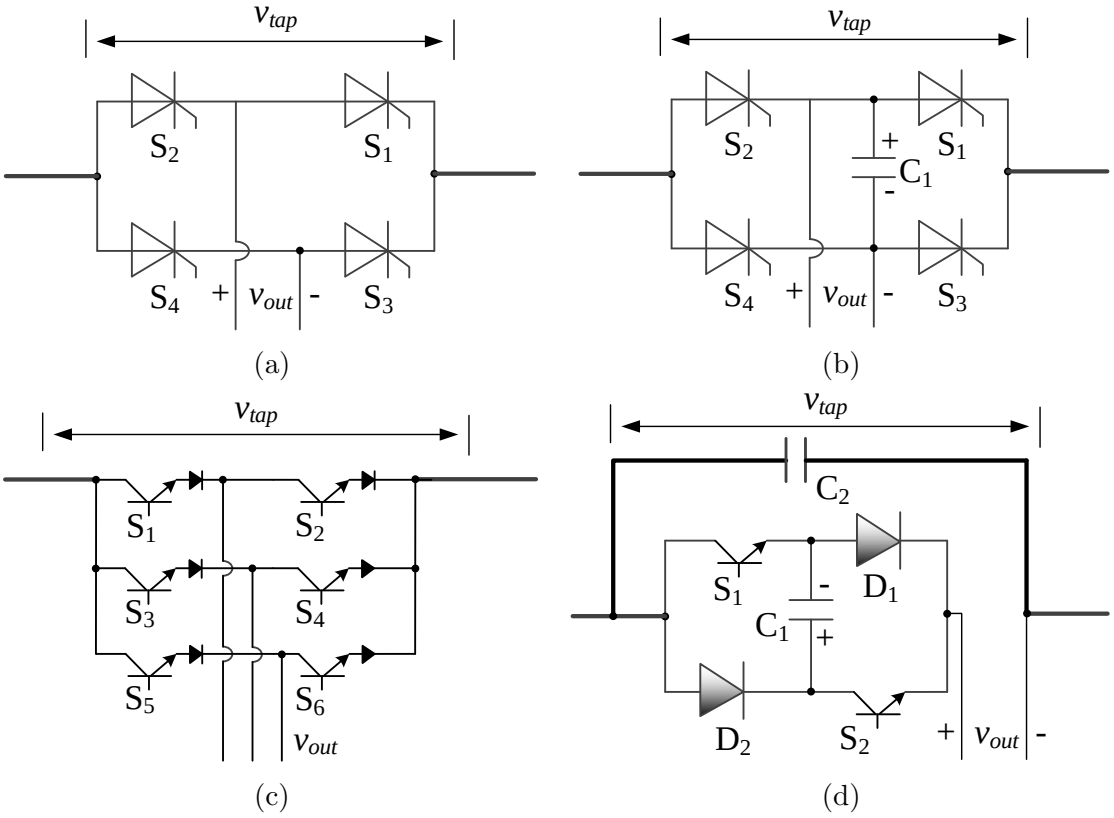


Figure 2.6: First stage of series taps: (a) Typical series tap, (b) FCC series tap, (c) CSC series tap, (d) Soft-switching series tap.

The typical series tap [32], as demonstrated in Fig 2.6(a), is the first proposed series tap due to the technical limitation of self-commutated semiconductor devices. As presented in Fig 2.7(a), when S_2 & S_3 are in the on-state, the DC current flows

through T_1, inducing a positive v_{out}. When S_1 & S_4 are turned on, the positive v_{out} forces S_2 & S_3 to turn off and commutate to S_1 & S_4 and the current direction on the transformer is reverse. Then the DC current can be inverted to AC.

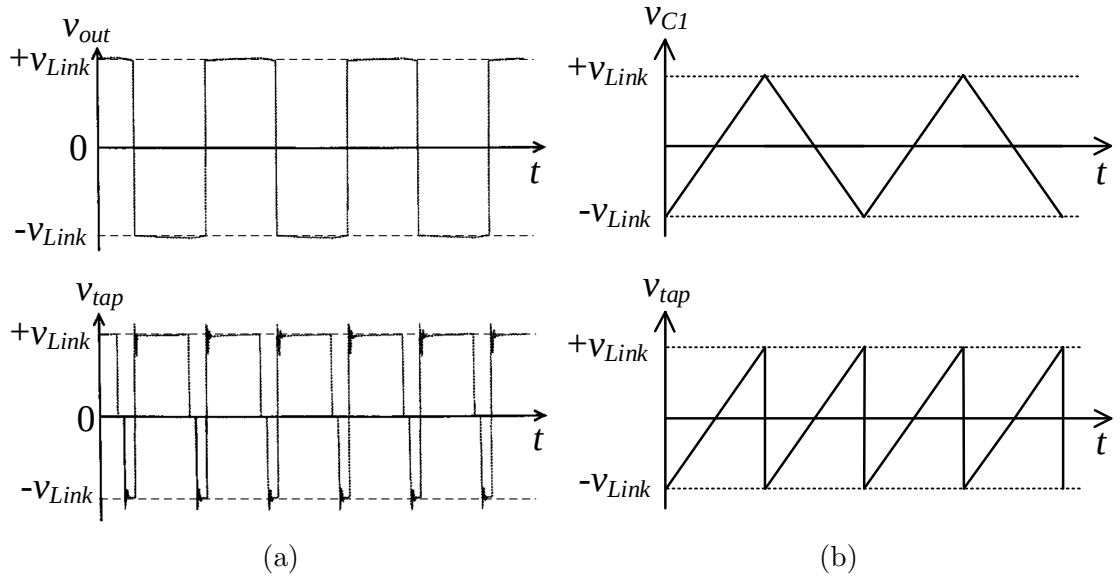


Figure 2.7: Key waveforms of the proposed series taps: (a) Typical series tap, (b) FCC series tap.

The FCC series tap with a resonant capacitor C_1 inserted in the middle of the H-bridge is an updated version of the typical type, as shown in Fig 2.6(b). The operating principle of the FCC series tap is similar to that of the typical one. As illustrated in Fig 2.7(b), when S_2 & S_3 are in the on-state, C_1 is charged to be positive. When S_1 & S_4 are turned on, the voltage on C_1 forces S_2 & S_3 to turn off and commutate to S_1 & S_4 and the current direction on the transformer is reversed [34].

With the appearance of GTOs and IGBTs on the market, series taps designed with these devices were proposed. [55] presents a tap with a three-phase IGBT inverter for off-shore wind energy integration with the HVDC line, as shown in Fig 2.6(c). This approach is similar with typical series taps, but in this case with power reversal. The diode in series to that of the IGBT [59] enables the reverse blocking capability in case of the reverse current flow of the HVDC line. This topology represents the adoption of self-commutated devices in series taps.

Another topology implementing IGBTs or GTOs is shown in Fig 2.6(d). It is called a soft-switching HVDC tap [56–58]. The switching sequence shown in Fig 2.8 are as follows. (1) When S_1 & S_2 are in the on-state, the line current flows through S_1, S_2, D_1 and D_2, bypassing the tap. (2) When S_1 & S_2 are turned off, C_1 is charged, forcing D_1 & D_2 to turn off. Then the line current flows through C_2. In this case S_1 & S_2 are turned off under ZVS conditions. (3) When S_1 & S_2 are turned on, the DC current discharges C_1 first. After the voltage on C_1 decreases to zero, D_1 & D_2 are turned on and the converter turns into the on-state. In this case S_1 & S_2 are turned on under ZCS conditions and the energy stored in C_1 flows back into the system. It can be seen that when the converter bridge is in the on-state the DC current flows through the converter bridge. When the H-bridge is in the off-state the DC current flows through C_2. So the DC current does not interrupt instantaneously with a bypass capacitor C_2.

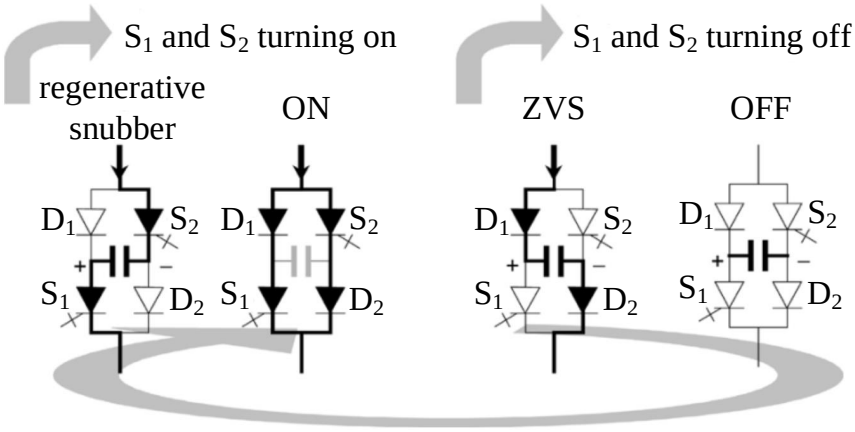


Figure 2.8: Switching sequence of the soft-switching tap

In conclusion, series taps have developed with the pace of the new semiconductor devices, from the original thyristor bridge to IGBT or GTO topologies. Series taps can fully utilise the HVDC line current and the number of semiconductor devices is limited since the tap voltage is only 1%∼10% of the line voltage, i.e. the cost and volume can be reduced when compared with parallel taps. Series taps are mostly current sourced due to the series connection with the HVDC transmission line. However, most of the proposed series taps are two-level which is challenging for

selecting the semiconductor devices or they have to use the series-connected devices as one switch. The HV rated isolation transformer, which is costly, bulky and difficult to design, also cannot be avoided. In addition, series taps inject a large percentage of voltage and current harmonics into the HVDC grid which affects the power quality of the transmission line.

2.2.3 Multilevel Converters in Series Taps

Fig 2.9 shows a brief classification and the development tendency of the proposed HVDC taps. Considering the development tendency of parallel taps, the first generation is the thyristor full-bridge topology which can be picked from LCC terminal technology. The second generation is the IGBT or GTO full-bridge converter (VSC) and the third generation is multilevel converters which can be an MMC or similar topologies. In contrast with parallel taps, series taps have only reached the second generation. Therefore the integration of the multilevel structure into a series tap would be an interesting idea. The multilevel converter generates multilevel AC which reduces the cost and volume of passive components, allow the HVDC current to flow continuously, and inject fewer harmonics into the grid. The literature review of multilevel converters are introduced as follows.

2.3 Multilevel Converters

For high-voltage applications where the converter operating voltage exceeds the voltage rating of single semiconductor device, there are normally two solutions: Series connected devices or the adoption of multilevel converters. The devices in the series connection and with synchronous drive signals can act as one device which has a higher voltage rating. The control strategy of the topology with series semiconductor devices is also simple, however, the equal voltage distribution among them in both transient and steady-state operations is challenging for its application [60]. Multilevel converters can overcome this problem.

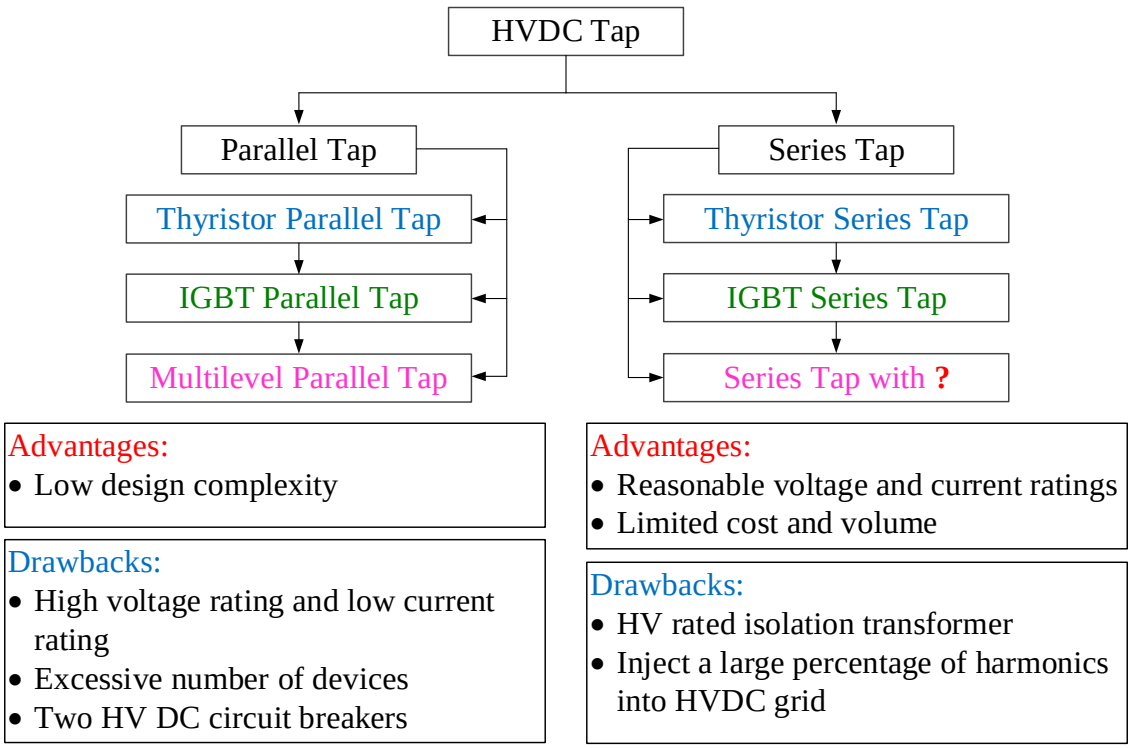


Figure 2.9: Classification of the HVDC tap

2.3.1 Topologies of Multilevel Converters

Recently multilevel converters have raised much attention in the applications at medium and high voltages owing to lower voltage rating of power switches, lower $\mathrm{d}v/\mathrm{d}t$ ratio to generate less harmonics, and no necessity for synchronous drive signals to all the devices. There are typically four types of multilevel converters: the neutral-point diode clamped converter (NPC) [61], flying capacitor (FC) converter [62], cascaded H-bridge (CHB) converter [63] and MMC [24], of which the topologies are shown in Fig 2.10(a), Fig 2.10(b), Fig 2.10(c) and Fig 2.11 respectively.

NPC and FC converters shown in Fig 2.10 can both output three-level AC comprising $+v_{in}/2$, 0 and $-v_{in}/2$, but there is the limitation of complexity and number of components when the level exceeds three [64, 65]. The CHB converter has better expandability when compared with NPC and FC converters under higher level. The CHB converter is composed of a series of H-bridges to synthesize a multilevel volt-

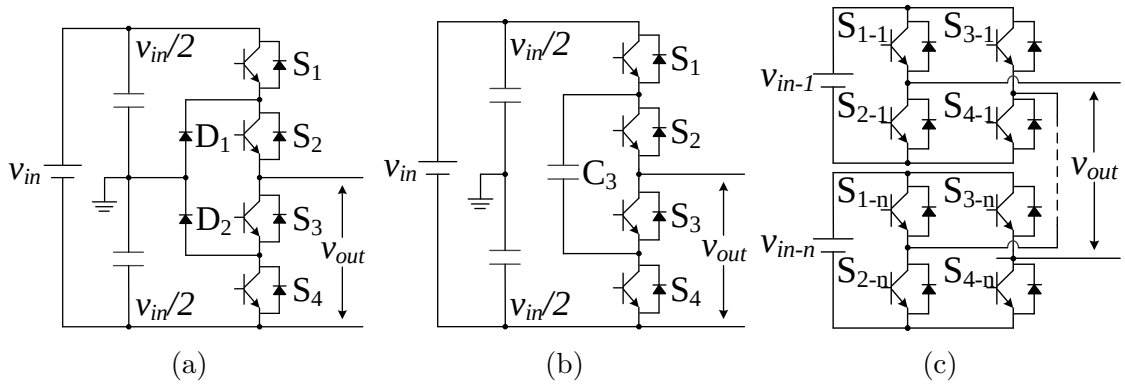


Figure 2.10: Typical multilevel converters: (a) Neutral-point diode clamped converter, (b) Flying capacitor converter, (c) Cascaded H-bridge converter.

age from several independent and isolated DC sources which can be obtained from batteries or solar panels.

MMCs are state-of-the-art multilevel converters for medium and high power applications proposed in recent years. It is normally connected in parallel with the HVDC line as one terminal for DC/AC power transmission. As seen in Fig 2.11, the three-phase MMC comprises two arms per phase leg where each arm consists of n series sub-modules and an arm inductor. Each sub-module leg is controlled to generate the AC phase voltage and the arm inductor suppresses the harmonics in the arm AC currents.

There are several configurations of sub-module circuits including the half-bridge sub-module, the full-bridge sub-module, the clamp-double sub-module and hybrid sub-module circuits [27, 66, 67]. However, the half-bridge sub-module, shown in Fig 2.11(a) is the most widely used owing to less semiconductor devices and lower losses. The full-bridge sub-module, seen in Fig 2.11(b), has more devices which results in a higher loss and cost but has DC short-circuit fault blocking capability [68]. The output voltage v_{SM} of half- and full-bridge sub-modules can be 0V or $+v_C$, where the ability of outputting $-v_C$ for the full-bridge sub-module is abandoned.

The CHB converter and MMC have more advantages in multilevel series taps (high level) due to the reduced number of components and reduced complexity compared

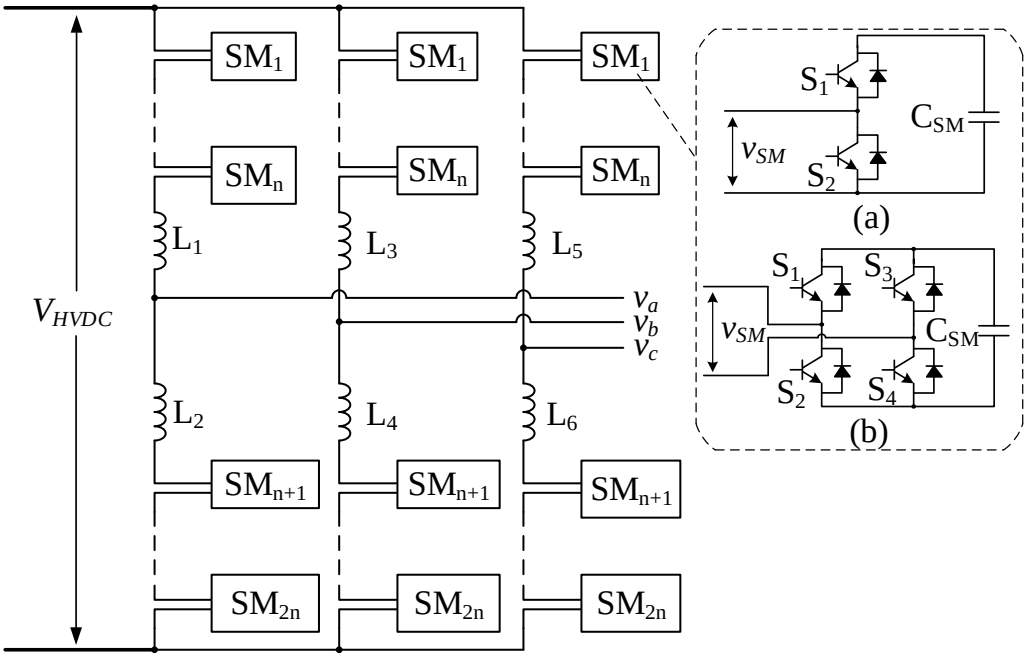


Figure 2.11: Schematic diagram of the MMC with different sub-module topologies: (a) Half-bridge sub-module, (b) Full-bridge sub-module.

with NPC or FC converters. It has good expandability with standardised modules and high voltage capability with the flexible sub-module number. So the CHB converter and MMC are more suitable in multilevel series taps. The main difficulty is to take the power from the tap to the load in a proper way and block HVDC voltage from the transmission line to the load.

The simplest multilevel series tap is created by inserting a single-phase or three-phase MMC into the line in series and then output to the second stage. the possible series MMC is shown in Fig 2.12, which is demonstrated based on Fig 2.5. The series MMC can fully use the line current and inject few harmonics into the line. The sub-module number can also be reduced compared with the MMC parallel tap due to a lower output voltage. The voltage on the two sides of the MMC is only DC because the AC voltages of two arms per leg are cancelled out. However, until now there are no discussions about multilevel series taps in the literature. This is because the high-voltage transformer still exists which offers no advantage over the proposed series taps. In addition, the MMC generates multilevel AC voltages to the second

stage. After the diode rectifier the AC voltages transfer to pulse DC voltage, which results in a larger filter capacitor value compared with the other proposed series taps. **So the research emphasis of the multilevel series tap is to properly utilise the modular multilevel structure into the series tap and remove the need for an HV rated isolation transformer**.

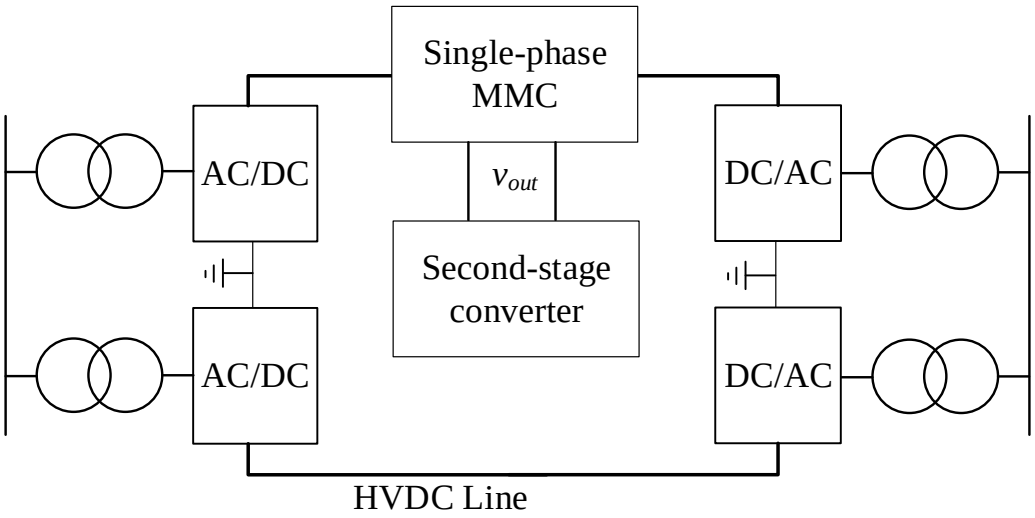


Figure 2.12: Schematic diagram of the possible single-phase series MMC

2.3.2 Technical Requirements of Modular Multilevel Structures

The technical requirements of the modular multilevel structure consist of modulation techniques, sub-module capacitor voltage balancing, the mathematical model, sub-module parameter selection, precharging of sub-module capacitors etc [69]. Here the modulation techniques and capacitor voltage balancing methods are introduced and the other aspects are detailed in later chapters.

Modulation Techniques

Various PWM techniques have been proposed for the modular multilevel structure such as level-shifted PWM [70], phase-shifted PWM [71] and nearest level control

(NLC) modulation [72]. The level-shifted carriers, shown in Fig 2.13(a), are composed of n_{ls} identical triangular carriers per arm, each of which has a specific level matching one sub-module. The phase-shifted carriers, shown in Fig 2.13(b), comprise n_{ps} identical carriers per arm with a phase-shifted angle of $360°/n_{ps}$. Assuming the same number of switching transitions for both the level-shifted and phase-shifted carriers shown in Fig 2.13, the level-shifted PWM produces lower line-to-line voltage total harmonic distortion (THD) [73, 74]. In the modulation of series taps with the modular multilevel structure, the level-shifted PWM technique can be adopted.

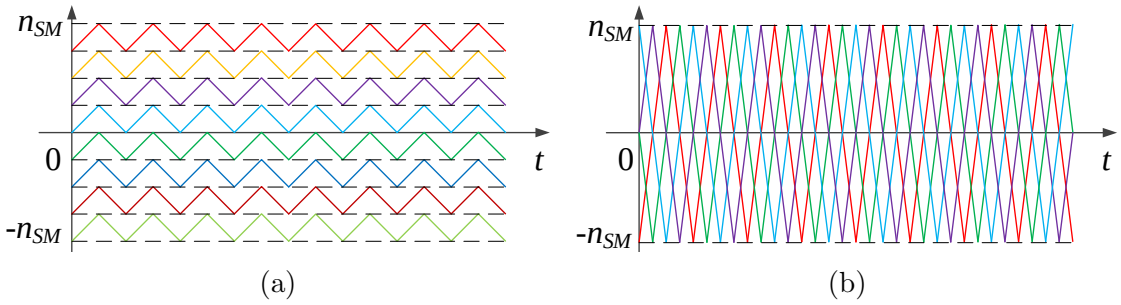


Figure 2.13: Multilevel carriers: (a) Level-shifted carriers, (b) Phase-shifted carriers.

Capacitor Voltage Balancing

Different capacitor voltage balancing methods including capacitor voltage sorting [24], dual sorting [75] and individual controlled balancing [76] methods have been proposed, in which the typical sorting method is most widely accepted. For the sorting method the sub-module capacitor voltages and arm currents are measured. Assuming the number of inserted sub-modules is n_{modu}, when the arm current is positive, n_{modu} sub-modules with the lowest capacitor voltages are inserted and the capacitors of inserted sub-modules are charged, causing a voltage increase. When the arm current is negative, n_{modu} sub-modules with the highest capacitor voltages are inserted and the capacitors of inserted sub-modules are discharged resulting in a decrease of voltages. The algorithm of the sorting method is simple to be realised in the software but it leads to unnecessary switching when the modulation level is unchanged. In the application of multilevel series taps with limited number of sub-modules, the typical sorting method can be implemented.

2.4 Summary

In this chapter the literature review on HVDC, HVDC taps and multilevel converters has been carried out. The idea of implementing the modular multilevel structure into the series tap and the evolutionary process has been discussed.

HVDC has evident advantages for long-distance bulk-power transmission, which is beneficial for optimising the allocation of global energy, developing the renewable energy and protecting the environment. It is also meaningful and marketable for supplying a small amount of power to the communities along the transmission line by HVDC taps where no stable electricity can be accessed and connecting to a dedicated AC network is costly.

HVDC tap topologies can be split into two types: parallel taps and series taps. Parallel taps can be simply designed and realised but operate under high voltage and low current which leads to excessive use of semiconductor devices and high cost. Series taps can fully utilise the HVDC line current and the components are limited which is more suitable for tapping small power from the HVDC line, but the proposed series taps have an HV rated isolation transformer, inject a large percentage of harmonics into the HVDC system and can only generate two-level AC which is challenging for selecting semiconductor devices or results in the usage of series switches. In addition, considering the developing tendency of series taps and parallel taps, the multilevel series tap could be significant for solving these problems.

Inserting an MMC in series with the HVDC line should be the simplest way to realise multilevel series taps which has benefits of injecting few harmonics to the line and avoiding series-connected switches, but the high-voltage transformer still exists and it is even worse for voltage filtering after the rectifier. Therefore the aim of this work is to realise the proper use of the modular multilevel structure into series taps, fully exploiting the merits of modular multilevel structure, and remove the need for HV rated isolation transformer at the same time. A novel modular multilevel series HVDC tap is proposed and analysed in the next chapter.

Chapter 3

N-phase Multi-Modular Series Tap

In this chapter the topology analysis and design of the n-phase MMST are carried out. The parameters and power losses of the two- and three-phase MMSTs are compared. The MMST topology and the operating principle are introduced in Section 3.1. The parameter design of a two-phase MMST is demonstrated in Section 3.2 and Section 3.3. The analysis of a three-phase MMST using a similar procedure to that of the two-phase version is described in Section 3.4. A case study and a comparison of the two- and three-phase MMSTs are discussed in Section 3.5.

3.1 Topology of the N-phase MMST

3.1.1 Introduction

Based on the literature review on HVDC taps in Chapter 2, the modular multilevel based series taps avoid the utilisation of series semiconductor devices and lightly influence the HVDC network compared with conventional series taps. However, if a typical MMC is simply inserted in series to the DC line, an HV rated isolation transformer, possibly air core [58], is still essential and the capacitor filtering after the rectifier is more difficult, as discussed previously in Section 2.3.1. In this work a

novel series HVDC tap, the n-phase multi-modular series tap in Fig 3.1, is proposed which is able to utilise the modular multilevel structure into the series tap properly and overcome the drawbacks of the series MMC in Fig 2.12. This topology can be used in monopole or bipolar HVDC systems which is analysed later in Section 3.1.3. Here the MMST is designed based on a bipolar HVDC system.

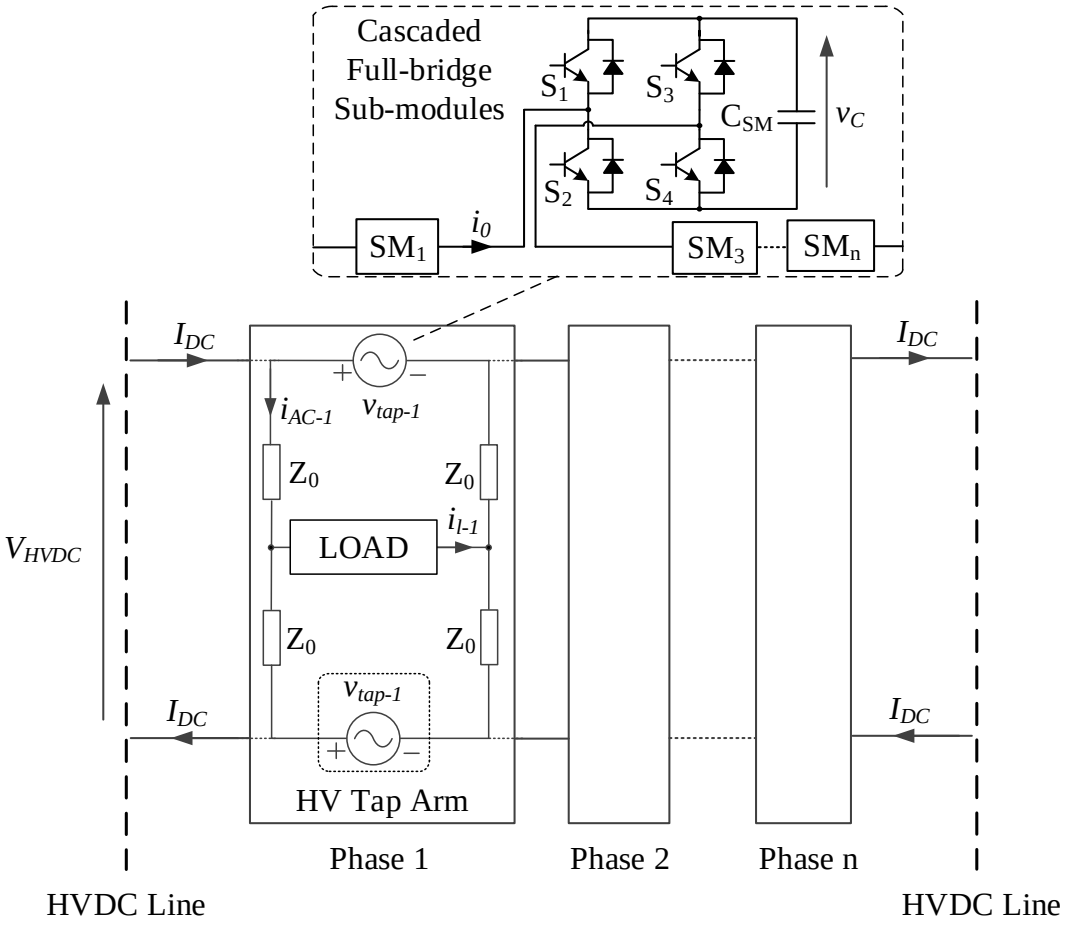


Figure 3.1: Schematic diagram of the n-phase multi-modular series tap

The MMST is a type of bidirectional series HVDC tap that utilises the full-bridge sub-modules typically found in MMCs for HVDC power transmission. It is a polyphase converter which requires a minimum of two phases. Each phase of the tap is constructed from one type of tap branches as shown in Fig 3.2. If the tap is composed of an odd number of phases the Type 1 tap branch is required, if an even number is used the Type 2 tap branch is needed; the reasons for that are discussed later.

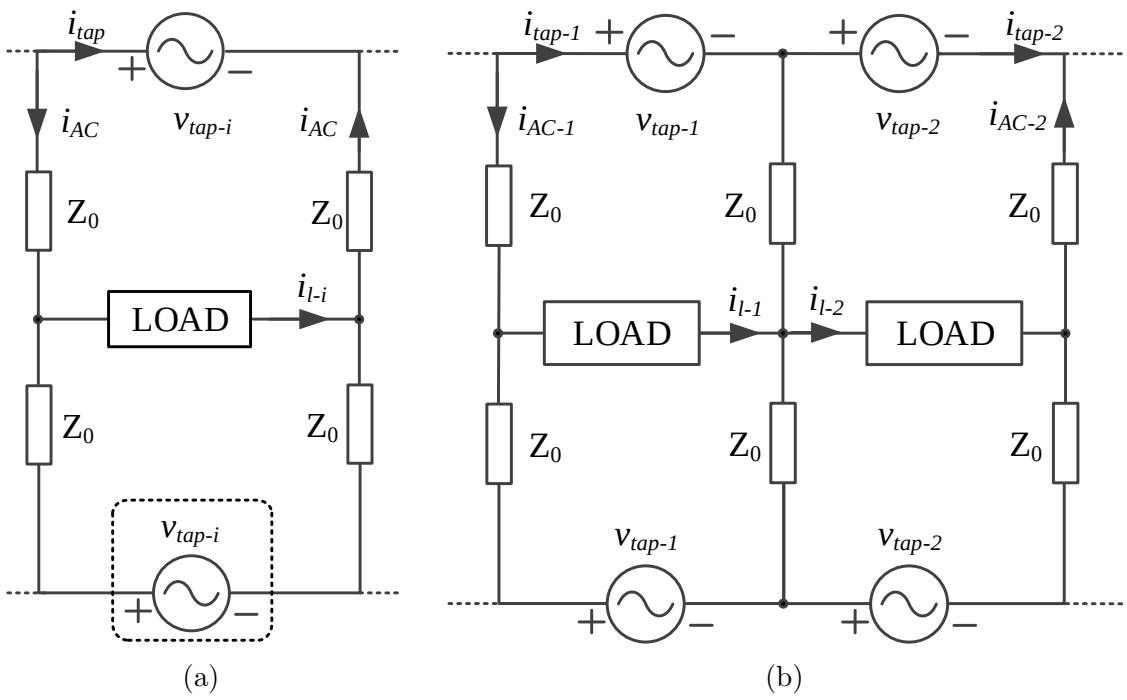


Figure 3.2: Schematic diagram of Type 1 and Type 2 tap branches: (a) Type 1 tap branch, (b) Type 2 tap branch.

In each phase the AC current is actively circulated around the tap and load, and power is exchanged between the HV and MV sides by the insertion of the AC voltage in the tap and load branches. To ensure there is no net energy exchange with the HV tap arms a DC bias voltage is inserted to recharge the tap arms with the DC line current. A branch impedance (including a bocking capacitor and a resonant inductor) is used to block the DC voltage between the HVDC transmission line and the load, while filtering the AC voltage and current at the same time. As will be shown, it is possible to capacitively couple the HV and MV connection removing the need for an HV rated isolation transformer.

The reason for implementing the blocking capacitor is that the capacitor is able to conduct AC current and block the HVDC voltage. If the transformer was connected in parallel with the sub-module string for HV isolation, it would be saturated due to the DC bias voltage on the tap arm. Therefore, the capacitive isolation is a peculiar characteristic of the MMST topology, and the comparison between the capacitor and

the conventional transformer for HV isolation is not necessary in the initial design.

The second-stage converter in the typical series taps (introduced in Section 2.2), which normally contains an isolation transformer and an AC/DC/AC converter, is replaced by the LOAD in Fig 3.1. In the analysis of the MMST topology, the second-stage converter of each phase can be regarded as a voltage source which is synchronous with the load current (explained in Chapter 4), or a resistor (explained in Chapter 5). In practice the second-stage converter of the MMST can be designed in various ways, but the MV rated isolation transformer, a rectifier and a DC link capacitor should be necessary for each phase, which means the phase output of the MMST needs to be transferred to DC first. For instance, a CHB converter can be used to connect to the DC link capacitors, or just series connect the DC link capacitors to obtain a DC bus. In this work the first-stage converter of this series tap, the MMST, is mainly researched.

3.1.2 Operating Principle of the N-phase MMST

It is proposed that the n-phase MMST, shown in Fig 3.1, is operated such that symmetrical sinusoidal voltages with a DC offset are produced at the HV tap arms, as described by (3.1). The use of symmetrical AC voltage components means that the AC voltage sums to zero and is not seen by the HVDC line. The total tap DC voltage seen by the transmission line is given by (3.2) and must be overcome by the difference in converter substation voltages at each end of the line.

$$v_{tap-i} = V_{DC} + \hat{V}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i\right) \qquad i = 1, 2, 3..... \tag{3.1}$$

$$V_{DC-tot} = 2n_{ph}V_{DC} \tag{3.2}$$

where v_{tap} is the tap arm voltage, V_{DC} and V_{AC} are the DC bias voltage and the tap AC voltage of v_{tap} respectively, ω is the angular frequency of V_{AC}, n_{ph} is the phase number of the MMST, and V_{DC-tot} is the total DC bias voltage of the tap. By controlling the AC component of the tap voltage v_{AC}, with respect to an AC

load voltage v_l, the AC current between the tap branches and the load branch can be circulated, such that the tap current is given by (3.3). As can be seen the tap current also includes the DC current that flows in the transmission line. The load current i_l contains upper and lower tap AC currents as in (3.4).

$$i_{tap-i} = I_{DC} + \hat{I}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i + \theta\right) \qquad i = 1, 2, 3..... \tag{3.3}$$

$$i_{l-i} = 2\hat{I}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i + \theta\right) \qquad i = 1, 2, 3..... \tag{3.4}$$

where i_{tap} is the tap arm current, I_{DC} and I_{AC} are the HVDC current and the tap AC current respectively, θ is the phase shift between tap AC current and voltage, and i_l is the load current. I_{AC} is also called as the loop current in the analysis. The instantaneous tap power p_{tap}, given by (3.5), has been derived in Appendix A. In order that there is no net exchange of the bulk stored energy in the tap arm the DC component voltage in (3.1) is selected such that there is zero net power in the HV tap arm, as in (3.6).

$$\begin{aligned} p_{tap-i} \quad &= V_{DC} \cdot I_{DC} + \frac{\hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot cos\theta}{2} \\ &+ V_{DC} \cdot \hat{I}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i + \theta\right) \\ &+ I_{DC} \cdot \hat{V}_{AC-i} \cdot sin(\omega t + \frac{2\pi}{n_{ph}} \cdot i) \\ &- \hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot cos(2\omega t + \frac{4\pi}{n_{ph}} \cdot i + \theta) \quad i = 1, 2, 3..... \end{aligned} \tag{3.5}$$

$$V_{DC} = -\frac{\hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot \cos\theta}{2I_{DC}} \tag{3.6}$$

The total DC power P_{DC} exchanged between the HVDC transmission line and the MMST is therefore given by (3.7). The AC power P_{AC} exchanged between the MMST and the load is given by (3.8).

$$P_{DC} = 2n_{ph}V_{DC}I_{DC} \tag{3.7}$$

$$P_{AC} = n_{ph}\hat{V}_{AC}\hat{I}_{AC}cos\theta \tag{3.8}$$

In operating the MMST the selection of DC voltage and current are respectively fixed by the power demand of the tap and the instantaneous current in the HVDC line. However, if it is assumed that the load of the MMST is perfectly coupled to the AC load by means of an additional second-stage converter, then the AC voltage, current and frequency of the MMST have degrees of freedom and flexibility for the system design.

3.1.3 Topology Analysis of the N-phase MMST

The operating principle of the MMST covers any number of phases. Here with the Type 1 type branch the MMST is able to generate any number of phases. Furthermore, Type 2 tap branch, which a combination of two Type 1 tap branches, is also proposed specifically for the even number of phases. The reason why the Type 2 tap branch is feasible is as follows.

The combination of the middle blocking branch of two Type 1 tap branches lightly influences the operation of the MMST. As the impedance of the middle branch at the fundamental frequency is much lower, the AC currents of one phase will flow through the middle blocking branch rather than flowing into the other phase. In addition, the currents of the middle blocking branch do not need to be sampled and controlled. The main effect is the ratings of the middle blocking branch impedance. In the Type 2 tap branch the AC current of the middle upper blocking branch, which equals to the sum of the currents of upper left and upper right blocking branches, is doubled. Comparing between the MMSTs with one Type 2 tap branch and two Type 1 tap branches, the AC voltage and current ratings of the middle blocking branch impedance in the former MMST are doubled. However the combination of more than two Type 1 tap branches is impossible if the independent sampling and control of each tap arm is required.

The Type 1 and Type 2 tap branches make the MMST design flexible. For instance, for an MMST with the odd number of phases, the n_{ph} Type 1 tap branches or one Type 1 tap branch and $(n_{ph} - 1)/2$ Type 2 tap branches can be selected. For an

even number of phases, the MMST can pick $n_{ph}/2$ Type 2 tap branches or n_{ph} Type 1 tap branches. In the initial analysis the MMST is united to be with Type 1 and Type 2 tap branches for odd and even number of phases, respectively.

Based on the operating principle and the analysis of the two types of tap branches, the MMST has the features including:

- The n-phase MMST can be flexibly adopted in bipolar or monopole HVDC systems. For bipolar systems the tap branches shown in Fig 3.2 can be directly implemented. For monopole systems only the upper halves of the tap branches are required to constitute the MMST.
- It is a polyphase converter which can generate any number of phases greater than one. A single-phase MMST may utilise one Type 1 tap branch and the AC voltages of upper and lower tap arms are cancelled out in the HVDC network illustrated in Fig 2.1(b). However, the single-phase MMST leads to an AC common mode fluctuation on the HVDC network with respect to the ground. In addition, the single-phase MMST cannot be used in monopole HVDC systems.
- The MMST uses the negative output capability of full-bridge sub-modules which is neglected in the typical MMC.
- It injects few harmonics to the HVDC line due to its multilevel structure and the cancellation of AC voltages on a single transmission line.
- The design complexity can be reduced compared to the conventional series taps as the HV rated isolation transformer is replaced by the blocking impedance, and the utilised sub-modules can be found in a typical MMC.

In this work the two-phase and three-phase MMSTs are selected particularly for further analysis and comparison as they contain Type 2 and Type 1 tap branches respectively. The results of the study can be extended to n-phase arrangements.

3.2 Sub-module Analysis of the Two-phase MMST

In this section an analysis is provided in order that the sub-module parameters may be designed. These include the required number of sub-modules, sub-module capacitance and semiconductor losses. The presented analysis is applied to an example two-phase tap as shown in Fig 3.3.

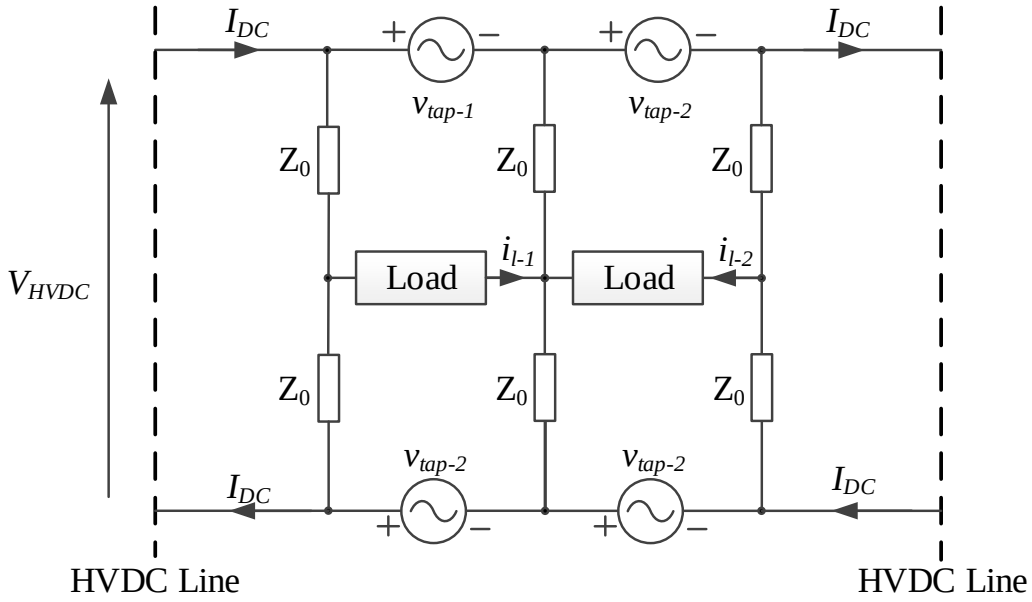


Figure 3.3: Topology of the two-phase MMST

From Fig 3.3 it can be seen that the two-phase MMST has one Type 2 tap branch in Fig 3.2. The two-phase MMST produces the voltage described by (3.9). In the case of a two-phase tap the AC component of each phase is 180° phase shifted such that the AC component sums to zero. As this is a two-phase system, the Type 2 tap branch may be used as there are sufficient degrees of freedom to allow a common impedance branch to be used. It is of particular interest as this should result in less tap branches.

$$\begin{cases} v_{tap-1} = V_{DC} + \hat{V}_{AC} \cdot \sin(\omega t) \\ v_{tap-2} = V_{DC} + \hat{V}_{AC} \cdot \sin(\omega t + \pi) \end{cases} \tag{3.9}$$

The parameters for the MMST analysis and design are provided in Table 3.1. The MMST design is based on the South West Link Project in Sweden with ±300kV and

1kA ratings [77]. The power rating of the MMST is 20MW which is sufficient for supplying more than two thousand households in urban areas [78]. A 10kV sampling voltage of V_{AC-i} is picked for the comparison with the three-phase tap under similar input and output characteristics, the reason for which is explained in Section 3.5.

Table 3.1: Two-phase MMST parameters

Parameter	**Value**
HVDC Voltage (V_{HVDC})	±300kV
HVDC Current (I_{DC})	1kA
Tap Power (P_{tap})	20MW
DC Bias Voltage ($V_{DC-total}$)	20kV
RMS AC voltage in Tap Voltage (V_{AC})	6–25kV (10kV sample)
Maximum Sub-module Current ($\hat{I}_{SM}$)	1500A
Capacitor Voltage of Sub-module (V_C)	2kV
Operating Frequency (f_f)	300–500Hz

Based on the conventional series tap circuit mentioned in Section 2.2, a the second-stage converter is connected on the LOAD of the MMST for supplying a stable AC grid to the remote communities. Therefore, the MMST has a large degree of flexibility on the operating frequency selection. With a higher operating frequency, the inductor value can be reduced due to the resonance with the blocking capacitor. Here the fundamental frequency f_f ranges from 300Hz to 500Hz for a trade-off with the sub-module number and the switching frequency in order that the MMST can generate the high-quality power with a relatively low switching frequency.

3.2.1 Number of Sub-modules

It is anticipated that the MMST would be formed from presently manufactured sub-modules. Thus some operating limits can be applied; firstly it is assumed that the sub-modules will be nominally operated such that the average capacitor voltage is 2kV, it is also assumed that that peak sub-module current is 1.5kA [79].

The DC component of the tap voltage is fixed by the power demand as in (3.7); however there is some degree of freedom with regards to the AC voltage. Here the

choice of the AC voltage and its impact on the sub-module number is considered. It is assumed that if the AC voltage is selected such that the tap current exceeds the rated sub-module current then parallel sub-module strings reducing the semiconductor current or parallel IGBTs distributing the device current may be used.

The utilisation of parallel IGBTs has the problem of asymmetric current sharing. Several current balancing techniques for parallel IGBTs have been presented including de-rating [80], impedance balancing [81] and active gate control [82]. However, parallel IGBTs would lower the system reliability and increase the design complexity, which parallel sub-module strings can overcome. Here in the initial analysis a standardised sub-module found in the typical MMC is assumed to be adopted in the two-phase MMST, and if the tap arm current exceeds the sub-module current rating then the parallel strings are used.

Comparing between parallel sub-module strings and a single sub-module string with parallel IGBTs, the numbers of semiconductor devices are equal under identical voltage and current ratings. Although more sub-module capacitors might be needed in parallel strings, the total equivalent capacitor value is unchanged if the same ripple percentage of the capacitor voltage is required. Therefore the scheme of parallel sub-module strings for arm current sharing is preferred. Here an arm inductor is inserted in series with each sub-module string for current balancing of parallel strings, which is detailed later in Section 4.3.

For a 20MW two-phase MMST the boundary AC voltage between using parallel sub-modules string or not is given by (3.10).

$$V_{AC-bound} = \frac{\frac{P_{tap}}{4}}{\frac{\hat{I}_{SM}-I_{DC}}{\sqrt{2}}} = 14.14 \text{ kV} \tag{3.10}$$

Fig 3.4 shows the variation in the minimum required sub-module number for a two-phase 20MW tap. The red line shows the theoretical minimum number of sub-modules required for a given AC tap voltage. Since there must be an integer number of sub-modules, the blue line shows the practical limit. It can be seen that when the Root-Mean-Square (RMS) AC voltage is lower than the boundary voltage, parallel

sub-module strings are needed, and the number of sub-modules doubles; when RMS AC voltage is higher than this boundary voltage, a single string is sufficient for the tap current. Based on Fig 3.4, the sub-module number at 10kV sampling AC tap voltage is $n_{SM} = 20$.

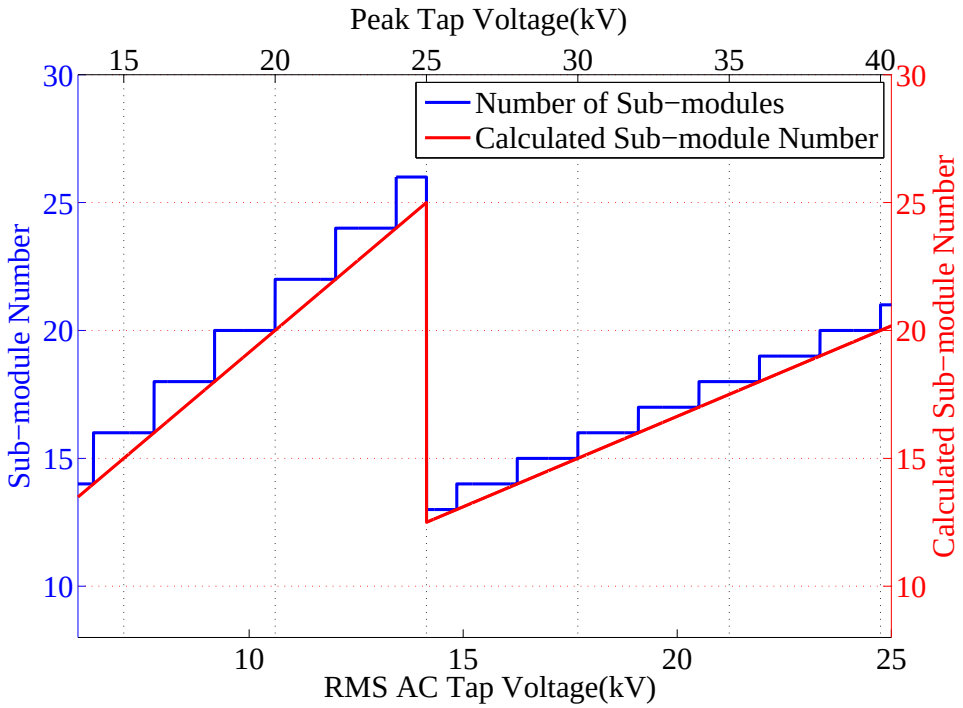


Figure 3.4: Number of sub-modules required per arm for the two-phase MMST

3.2.2 Sub-module Capacitor Size

To ensure there is always sufficient available voltage in the tap arms to produce the target voltage described in (3.1), the sub-module capacitance should be adequately sized such that (3.11) holds true. In this analysis it is assumed that a ±5% ripple in the sub-module capacitor voltage will meet this criteria. The assumptions used in calculating this voltage ripple is that the sub-module energy is always perfectly distributed amongst each sub-module in the tap arm by the rotation operation of

the sub-modules (explained in Section 2.3.1) and that the tap arm can be treated as an ideal voltage source (explained in Chapter 4). As has been shown for the classic MMC, circulating even harmonics arising from the twice fundamental power pulsation causes a deviation from this model; nevertheless valuable insight into capacitor size can still be gained using this approach.

$$\frac{v_{tap}}{n_{SM}} \leq v_C \leq V_{C-max} \tag{3.11}$$

Here v_C is the sub-module capacitor voltage, V_{C-max} is the maximum capacitor voltage that it can sustain, and n_{SM} is the sub-module number per arm. Under these assumptions the energy in the tap arm can be related to the sub-module voltage by (3.12). Assuming a $\pm 5\%$ ripple and making the substitution, the sub-module capacitance can be related to the peak deviation in tap energy using (3.13). Here E_{tap} is the tap arm energy.

$$\begin{cases} E_{tap} = n_{SM} \cdot \frac{1}{2} C_{SM} (V_{C0} - \frac{\Delta V_C}{2})^2 + \Delta E_{tap} = n_{SM} \cdot \frac{1}{2} C_{SM} (V_{C0} + \frac{\Delta V_C}{2})^2 \\ \frac{\Delta V_C}{V_{C0}} = 10\% \end{cases} \tag{3.12}$$

$$C_{SM} = \frac{20 \Delta E_{tap}}{{V_{C0}}^2 \cdot n_{SM}} \tag{3.13}$$

The peak deviation in tap energy can be calculated by integrating (3.5) over a fundamental period (the DC component in (3.5) is 0 with no net energy exchange) to give the steady-state instantaneous tap energy as in (3.14). Here t_0 is the starting time of the integration, and assume a unity power factor of the system with θ=0. At a different operating time, the instantaneous tap energy is changing, but the peak-to-peak energy keeps the same. According to (3.14), the peak energy deviation is a function of the AC voltage and operating frequency. The graph of ΔE_{tap} vs. peak AC current $\hat{I}_{AC}$ and operating frequency f_f under the parameters listed in Table 3.1

(I_{DC}=1kA) is shown in Fig 3.5.

$$\begin{aligned} e_{tap-i} &= \int_{t_0}^{t_0+t} p_{tap-i}(t)dt + \frac{1}{2}n_{SM}C_{SM}{V_{C0}}^2 \\ &= -\frac{1}{\omega}\frac{\frac{P_{tap}}{2n_{ph}}}{I_{DC}}\frac{\frac{P_{tap}}{n_{ph}}}{\hat{V}_{AC-i}}\cos\omega t - \frac{1}{\omega}\cdot I_{DC}\cdot\hat{V}_{AC-i}\cdot cos\omega t \\ &\quad -\frac{1}{2\omega}\frac{P_{tap}}{n_{ph}}sin(2\omega t) + \frac{1}{2}n_{SM}C_{SM}{V_{C0}}^2 \quad i = 1, 2, 3..... \end{aligned} \tag{3.14}$$

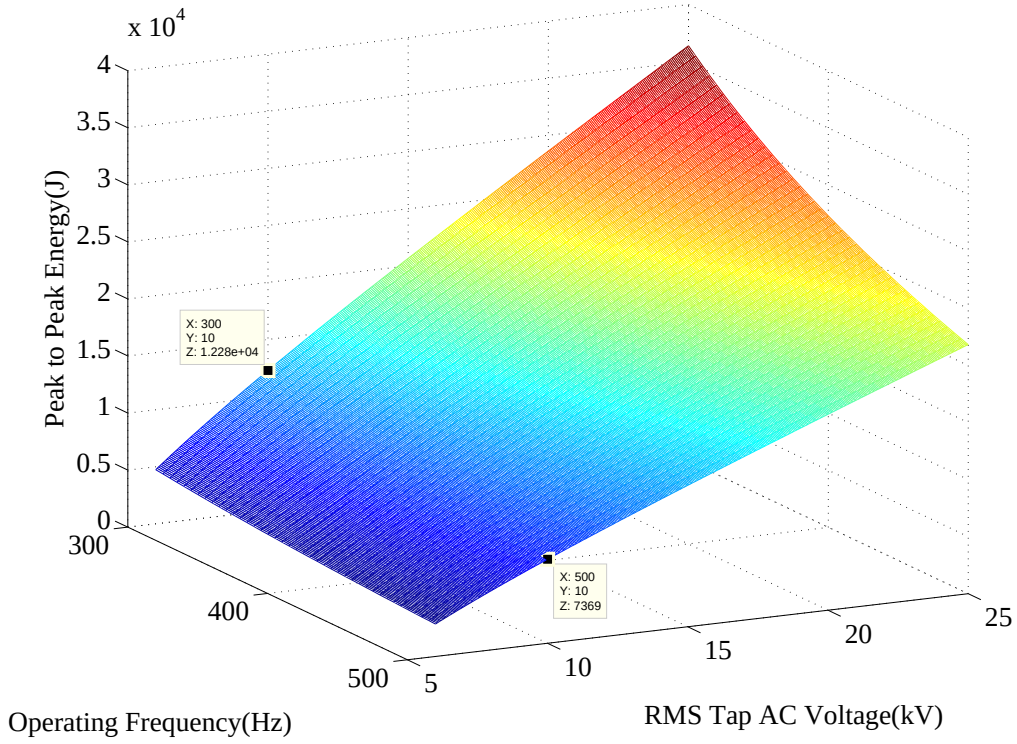


Figure 3.5: Graph of ΔE_{tap} vs. V_{AC} & f_f

By applying the results in Fig 3.5 to (3.13), the required capacitor value can be acquired for a particular set of operating conditions. For a two-phase 20MW tap operating under full DC current and using the sub-module constraints given previously in Table 3.1, the required capacitor value can be plotted as in Fig 3.6. Here the capacitance is plotted against RMS AC voltage V_{AC} and operating frequency

f_f. Sample points are provided on the graph showing a comparison of the required sub-module capacitance at $V_{AC} = 10$kV for the two extremes of operating frequency.

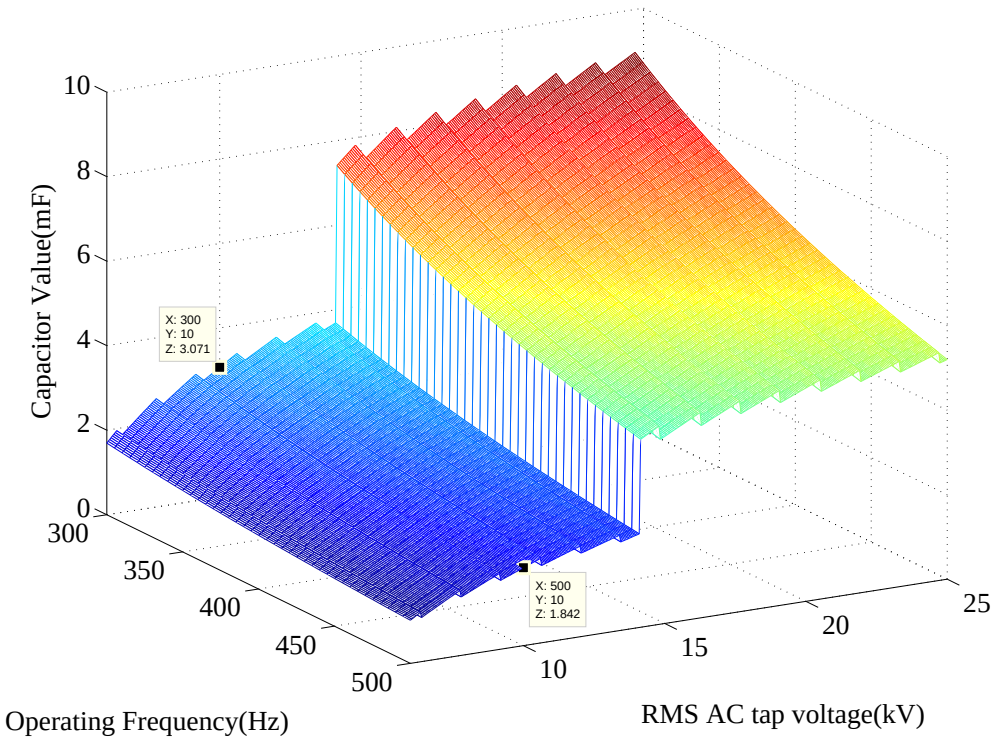


Figure 3.6: Graph of sub-module capacitor value C_{SM} vs. V_{AC} & f_f

In Fig 3.6 the sharp edges in the surface arise from the changes in sub-module number as a function of the operating voltage, previously shown in Fig 3.4. It can be seen that the capacitor values at lower RMS AC voltage (parallel strings) is much lower than those of higher AC voltage (single string), which should be noted that the sub-module number should be taken into account when making this comparison. If only considering the single string rather than parallel strings when $V_{AC} \leq V_{AC-bound}$ despite the limitation of the peak sub-module current, the capacitor value should be doubled and no sharp edges would be seen. Then the required sub-module capacitor value increases with the rise of V_{AC}. Therefore, the equivalent capacitor value of one tap arm C_{arm} considering both the sub-module number and the single capacitor

value, shown in Fig 3.7, is meaningful. C_{arm} also represents the time-average energy storage in the tap arm. The calculation of C_{arm} is based on the condition of the tap operating under full HVDC line current. The relationship of the equivalent capacitor value and the sub-module capacitor value is given in (3.15), where n_{string} is 1 for the single string or 2 for parallel strings.

$$C_{arm} = \frac{n_{string}^2}{n_{SM}} \cdot C_{SM} \tag{3.15}$$

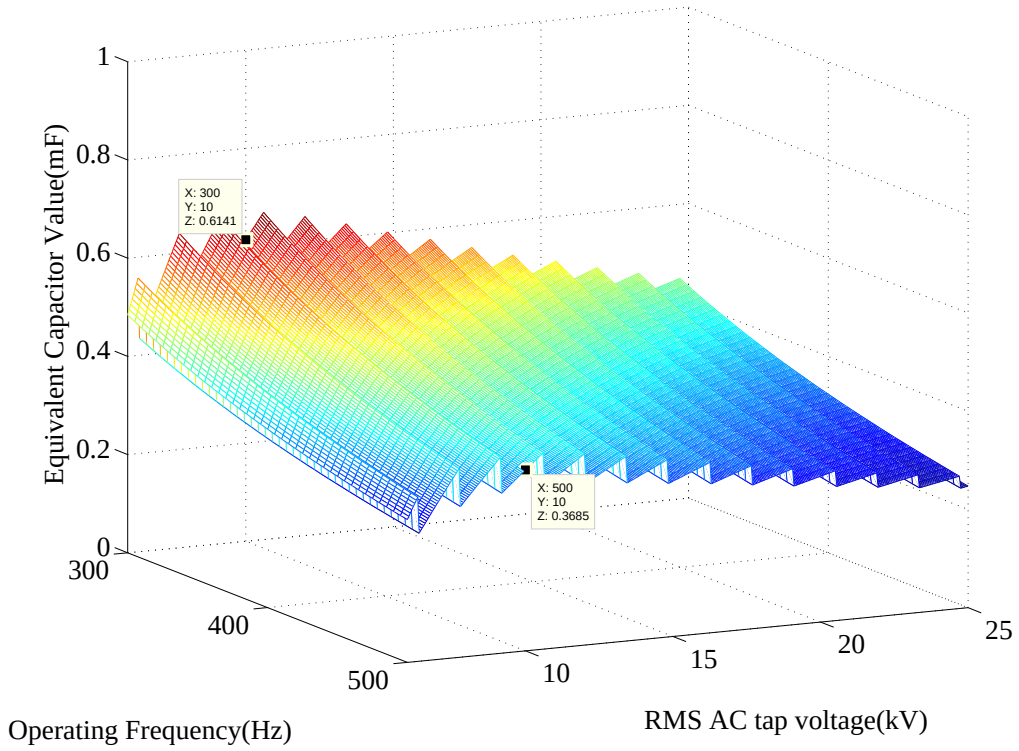


Figure 3.7: Graph of equivalent arm capacitor value C_{arm} vs. V_{AC} & f_f

Comparing with Fig 3.6 and Fig 3.7, the sub-module capacitor values around the sample point $V_{AC} = 10$kV are not the largest, but the values of C_{arm} are larger than the others. This is because when V_{AC} increases, ΔE_{tap} increases but not linearly. In order to sustain the energy variation in one arm and suppress the capacitor voltage ripple, the sub-module capacitor value needs to be higher, and more sub-modules

are needed with the increase of V_{AC} at the same time. This means that both more sub-module capacitors and the larger capacitor values, which make the voltage ripple within ±5%, lead to a higher cost and larger size. This can guide the MMST design to select a suitable V_{AC} which has the largest equivalent capacitor value of one arm with no need of large sub-module capacitors.

3.2.3 Sub-module Loss Analysis

Here the semiconductor losses, including conduction losses and switching losses, are considered. The full-bridge sub-module topology is shown in Fig 3.8. There are four sub-module operating states, listed in Table 3.2, which need to be considered.

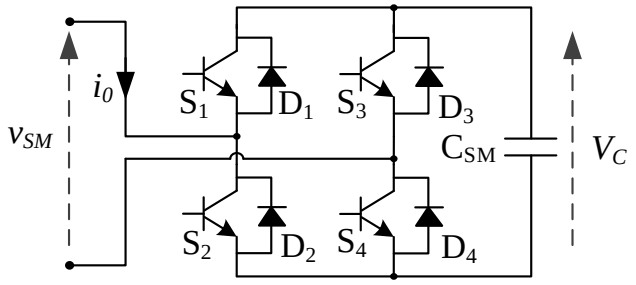


Figure 3.8: Full-bridge sub-module topology

Table 3.2: Full-Bridge sub-module states

Condition	S_1	S_2	S_3	S_4	v_{SM}	Conducting switch	
						$i_0 \geq 0$	$i_0 < 0$
1	1	0	0	1	V_C	2 diodes	2 IGBTs
2	0	1	0	1	0	1 diode, 1 IGBT	1 diode, 1 IGBT
3	1	0	1	0	0	1 diode, 1 IGBT	1 diode, 1 IGBT
4	0	1	1	0	-V_C	2 IGBTs	2 diodes

From this table the number and type of conducting devices can be seen based on the sign of the AC output voltage and current. In the analysis of semiconductor losses the states of the sub-modules are determined from the target waveform in (3.9). In determining the sub-module states the *flat carrier* method [72] illustrated in Fig 3.9

is used to provide an approximation of the switching function. In Fig 3.9 the case for a ten sub-module arrangement is chosen. If the tap voltage v_{tap} is at point A, four sub-modules operate in Condition 1 (output $+V_C$), and the other six operate in Condition 2 or 3 (output zero voltage); at point B, seven sub-modules operate in Condition 4 (output -V_C), and the other three operate in Condition 2 or 3.

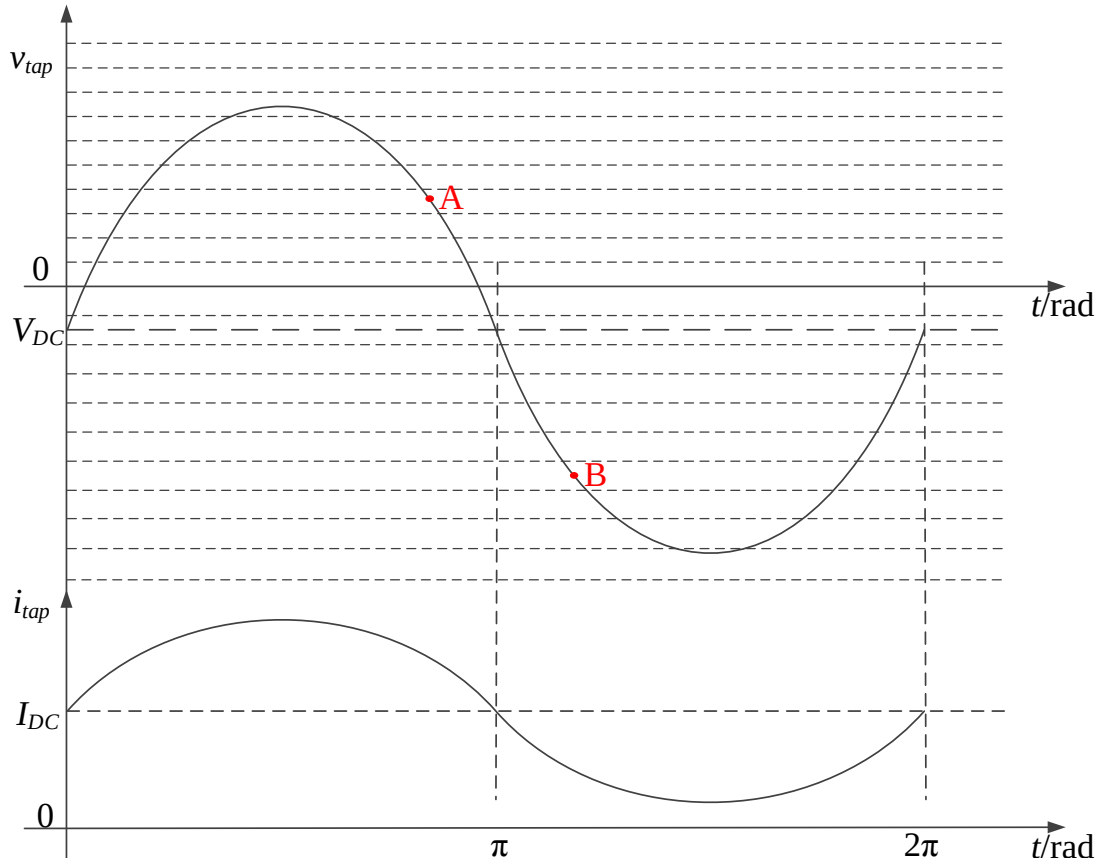


Figure 3.9: The voltage and current of sub-modules

Losses have been calculated based on the MITSUBISHI CM1200HG-66H HVIGBT modules, 3.3kV, 3.6kA [83, 84]. The conduction and switching characteristics of the module are illustrated in Appendix B. The conduction loss of one IGBT, the conduction loss of one diode, the turn-on loss of one IGBT, the turn-off loss of one IGBT and the reverse recovery loss of one diode are represented by $p_{IGBT-one}(i_0)$, $p_{diode-one}(i_0)$, $e_{on}(i_0, v_{IGBT})$, $e_{off}(i_0, v_{IGBT})$ and $e_{rec}(i_0, v_{IGBT})$ respectively.

Conduction Loss Analysis

For the analysis of conduction losses the flat carrier method provides an adequate approximation as only one sub-module can be in the incorrect state at any time. Additionally, referring to Table 3.2 it can be seen that any error in the conduction loss due to the incorrect state of one sub-module will be the difference in the conduction loss for an IGBT as opposed to a diode and will be insignificant.

Equations are now presented to calculate the conduction loss based on the tap arm voltage and current. For the region of the fundamental period T, where n_1 is the number of sub-modules that output V_C when $v_{tap} > 0$ & $i_0 > 0$, or $-V_C$ when $v_{tap} < 0$ & $i_0 < 0$, the conduction losses of diodes are given by (3.16).

$$p_{cond-diode} = \frac{\int \left[n_1 \cdot 2p_{diode-one}\left(|i_0(t)|\right) + (n_{SM} - n_1) \cdot p_{diode-one}\left(|i_0(t)|\right)\right] \cdot \mathrm{d}t}{T} \tag{3.16}$$

The conduction losses of IGBTs are given by (3.17)

$$p_{cond-IGBT} = \frac{\int \left[(n_{SM} - n_1) \cdot p_{IGBT-one}\left(|i_0(t)|\right)\right] \cdot \mathrm{d}t}{T} \tag{3.17}$$

For the region of the fundamental period T, where n_2 is the number of sub-modules that output V_C when $v_{tap} < 0$ & $i_0 > 0$, or $-V_C$ when $v_{tap} > 0$ & $i_0 < 0$, the conduction losses of diodes are given by (3.18).

$$p_{cond-diode} = \frac{\int \left[(n_{SM} - n_2) \cdot p_{diode-one}\left(|i_0(t)|\right)\right] \cdot \mathrm{d}t}{T} \tag{3.18}$$

The conduction losses of IGBTs are given by (3.19)

$$p_{cond-IGBT} = \frac{\int \left[n_2 \cdot 2p_{IGBT-one}\left(|i_0(t)|\right) + (n_{SM} - n_2) \cdot p_{IGBT-one}\left(|i_0(t)|\right)\right] \cdot \mathrm{d}t}{T} \tag{3.19}$$

Switching Loss Analysis

The switching losses of the IGBT module are related to the voltage and current of each switch. Regarding the sub-module capacitor voltage as constant, the voltage on each IGBT is V_C. The current of the IGBT, i_0, is equal to the tap arm current i_{tap}. As illustrated in Appendix B, the switching energies include e_{on}, e_{off} for turn

on and turn off energies of the IGBT and e_{rec} for the reverse recovery energy of the diode. For the different conditions of the tap arm voltage v_{tap}, sub-module current i_0 and the change of modulation level, the composition of switching energies are listed in Table 3.3, where $n_{modu}+1$ represents one level increase of the modulation level and $n_{modu}-1$ indicates one level decrease.

Table 3.3: Conditions of sub-module switching energies

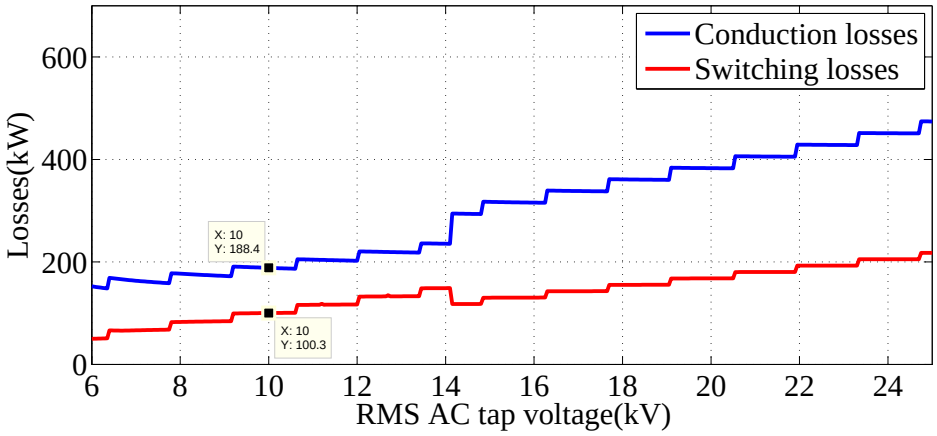
Condition	S_1	S_2	S_3	S_4	Switching energies
$v_{tap}\geq 0, i_0\geq 0, n_{modu}+1$	1	0	$1\rightarrow 0$	$0\rightarrow 1$	$e_{on}+e_{off}$
$v_{tap}\geq 0, i_0< 0, n_{modu}+1$	1	0	$1\rightarrow 0$	$0\rightarrow 1$	$e_{on}+e_{off}+e_{rec}$
$v_{tap}\geq 0, i_0\geq 0, n_{modu}-1$	1	0	$0\rightarrow 1$	$1\rightarrow 0$	$e_{on}+e_{off}+e_{rec}$
$v_{tap}\geq 0, i_0< 0, n_{modu}-1$	1	0	$0\rightarrow 1$	$1\rightarrow 0$	$e_{on}+e_{off}$
$v_{tap}< 0, i_0\geq 0, n_{modu}+1$	$1\rightarrow 0$	$0\rightarrow 1$	1	0	$e_{on}+e_{off}+e_{rec}$
$v_{tap}< 0, i_0< 0, n_{modu}+1$	$1\rightarrow 0$	$0\rightarrow 1$	1	0	$e_{on}+e_{off}$
$v_{tap}< 0, i_0\geq 0, n_{modu}-1$	$1\rightarrow 0$	$0\rightarrow 1$	1	0	$e_{on}+e_{off}$
$v_{tap}< 0, i_0< 0, n_{modu}-1$	$1\rightarrow 0$	$0\rightarrow 1$	1	0	$e_{on}+e_{off}+e_{rec}$

Based on Table 3.3 the switching energies in every step change of the modulation level can be represented by $e_{swit}(v_{tap}, i_0, n_{modu})$. For the region of the fundamental period T, the switching loss of one sub-module is given by (3.20).

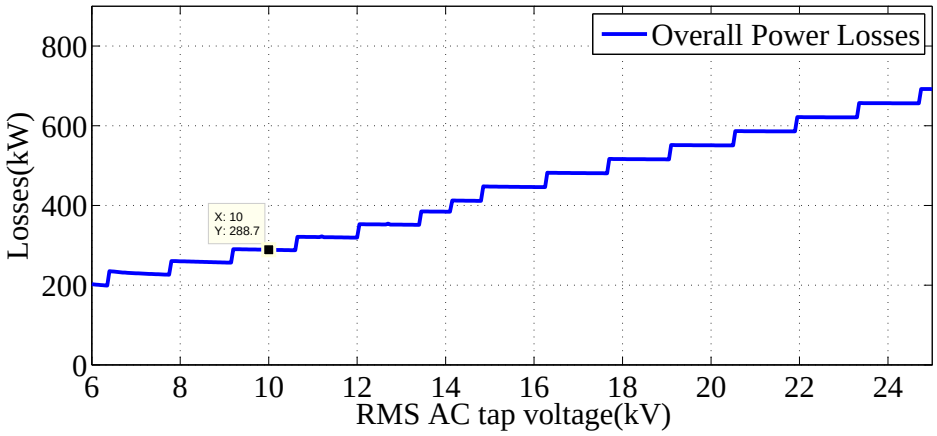
$$p_{swit}=\frac{\sum e_{swit}(v_{tap}, i_0, n_{modu})}{T} \tag{3.20}$$

Using (3.16) to (3.20) and (B.1), a Matlab script has been developed to calculate the power losses. Fig 3.10 shows the plot of conduction, switching and overall losses vs RMS AC voltage for a two-phase 20MW tap operating at the fundamental frequency of 300Hz under the full HVDC line current. Here the losses are not compared under the same amount of semiconductor devices when the tap AC voltage varies. A higher tap AC voltage leads to more sub-modules and higher losses which can be seen from the steps in Fig 3.10(b) since the standardised sub-modules are used.

The flat carrier approximation adopted in the Matlab script for the switching loss calculation means that sub-module switching only happens when the modulation level jumps, i.e. each sub-module turns on and off at most once in half the fundamental period, and no switching action occurs when the modulation wave remains between



(a)



(b)

Figure 3.10: The power losses of the two-phase MMST: (a) Conduction and switching losses vs. V_{AC}, (b) Overall power losses vs. V_{AC}.

two levels (referring to Fig 3.9). With a certain level of the modulation wave n_{level}, the sub-module string switches $(n_{level}-1)$ times in one fundamental period, and the equivalent switching frequency for a single sub-module is always $(n_{level}-1)\cdot f_f$. However, in practice, when a sampled carrier approach is used, the switching frequency f_s will be higher. Therefore, considering the linear relationship of the switching losses and the switching frequency, the switching losses from the Matlab script need to be corrected to a certain switching frequency by a factor $\frac{f_s}{(n_{level}-1)\cdot f_f}$ for more effective analysis and comparison.

The maximum and minimum voltages of the modulation wave of the upper left tap arm in Fig 3.3 are 19.14kV and -9.14kV. With a modulation level of 2kV, the modulated voltage has $n_{level} = (|\frac{19.14}{2}| + |\frac{-9.14}{2}|) = 16$ levels. So the equivalent switching frequency is $(n_{level} - 1) \cdot f_f$=4.5kHz. Set a standard switching frequency which can allow every sub-module turn on and off twice in one fundamental period, then $f_s = 2 \cdot \frac{n_{SM}}{n_{string}} \cdot f_f$=6kHz. The switching losses in the Matlab script is corrected with the factor $\frac{6}{4.5} = 1.33$. The curve of switching losses in Fig 3.10 shows the corrected power losses of the two-phase MMST.

It can be seen that the overall power losses at AC voltages lower than V_{bound} are relatively low where it should be noted that the number of sub-modules are different. At lower tap AC voltages the tap arm current exceeds the maximum current of standardised sub-modules and the parallel strings are used. As the parallel strings share the total tap current the power losses are less. The figure provides a sample point at V_{AC}=10kV. At this point, the value of conduction losses is 188.4kW, the value of switching losses is 100.3kW and the value of overall losses is 288.7kW, which yields a percentage loss of

$$\eta_{two} = \frac{P_{cond-tot} + P_{swit}}{P_{tap}} = 1.44\%$$

The analyses above have shown the required number of sub-modules, sub-module capacitor size and power losses for a two-phase MMST. In this case the power losses and capacitor size can be improved by using parallel strings of sub-modules instead of single strings. The evident disadvantage of parallel strings is the increased number of sub-modules, which results in the additional coupling inductors to ensure that the currents of two sub-module strings remain balanced. Furthermore, the parallel structure leads to a higher cost directly, as well as a larger size of tap converter.

3.3 Connection of HV tap and MV load on the Two-phase MMST

The HV tap arm is connected to the MV load by means of an impedance capable of blocking the high DC voltage potential between the HVDC line and ground instead of an HV rated isolation transformer. It is possible to achieve this using a capacitor, or rather a series string of capacitors to achieve the necessary voltage rating. However, either a large capacitor value is used or the voltage required to circulate the AC current is large. To mitigate this problem, it is proposed here that an inductor can be connected in series with the blocking capacitor, as shown in Fig 3.11. By selecting the parameters such that the inductor and capacitor are resonant near the operating frequency the voltage drop across the blocking branch can be mitigated and only a small capacitance is required. Although the voltage rating is increased, the capacitance with a relatively small value is preferred for reducing the cost and volume.

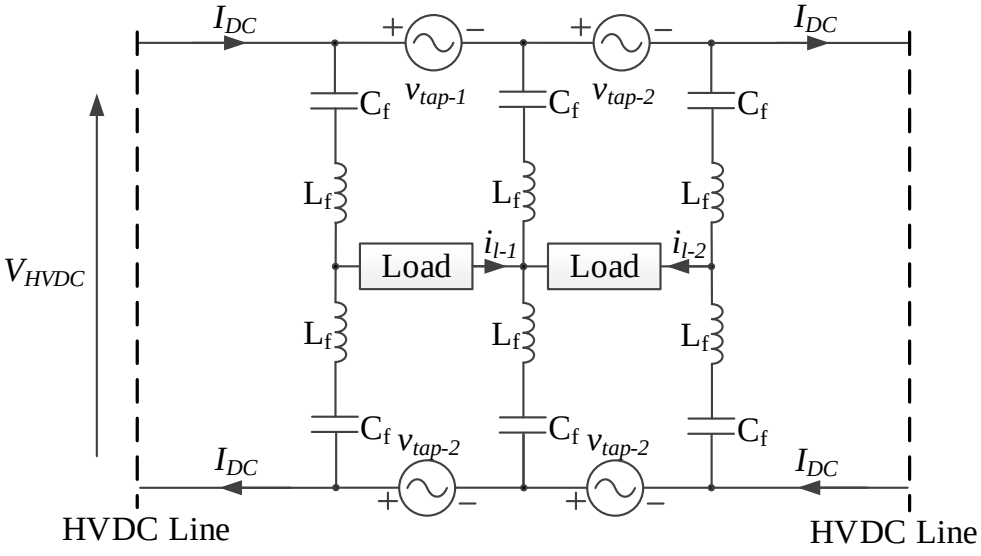


Figure 3.11: Two-phase MMST with LC blocking branches

3.3.1 Design of Blocking Capacitor

To meet the HV requirement of the capacitor blocking branch it is proposed that a series string of capacitors can be used; it is assumed that they would be of similar ratings to those used in standard MMC sub-modules. The number of required series blocking capacitors n_{Blk} is therefore defined by the HVDC line voltage as in (3.21), where V_{Blk} is the average voltage of the blocking capacitor. The equivalent value of the series string of capacitors is therefore given by (3.22).

$$n_{Blk} = \frac{V_{HVDC}}{2V_{Blk}} \tag{3.21}$$

$$C_f = \frac{C_{Blk}}{n_{Blk}} \tag{3.22}$$

With the chosen value of V_{Blk}=2kV the number of series blocking capacitors is n_{Blk}=150. However, it is not enough to just consider the required DC blocking voltage, as the AC current in the blocking capacitor causes a ripple voltage which must be considered. To avoid an excessive AC ripple, a reasonable AC voltage ripple ($\pm$20%) limitation is selected, as in (3.23). Deducing (3.23) gives (3.24).

$$\begin{cases} \frac{\widehat{i}_{AC} \cdot Z_{C_f}}{0.5 V_{HVDC}} \leq 20\% \\ \widehat{i}_{AC} = \sqrt{2} \frac{\frac{P_{tap}}{2n_{ph}}}{V_{AC}} \\ Z_{C_f} = \frac{1}{2\pi f_f \cdot C_f} \end{cases} \tag{3.23}$$

$$C_f \geq \frac{5\sqrt{2} P_{tap}}{2\pi \cdot n_{ph} \cdot V_{HVDC}} \cdot \frac{1}{V_{AC} \cdot f_f} \tag{3.24}$$

Fig 3.12 shows the minimum blocking capacitor values for a two-phase MMST based on (3.24) as the operating frequency and tap AC voltage are changed. It can be concluded that with the increase of V_{AC} & f_f the blocking capacitor can be selected with a lower value. At the sample point of V_{AC}=10kV and f_f=300Hz, a selected branch capacitor value is $C_f = 6.67\mu$F, and the value of single blocking capacitor is $C_{Blk} = 1$mF.

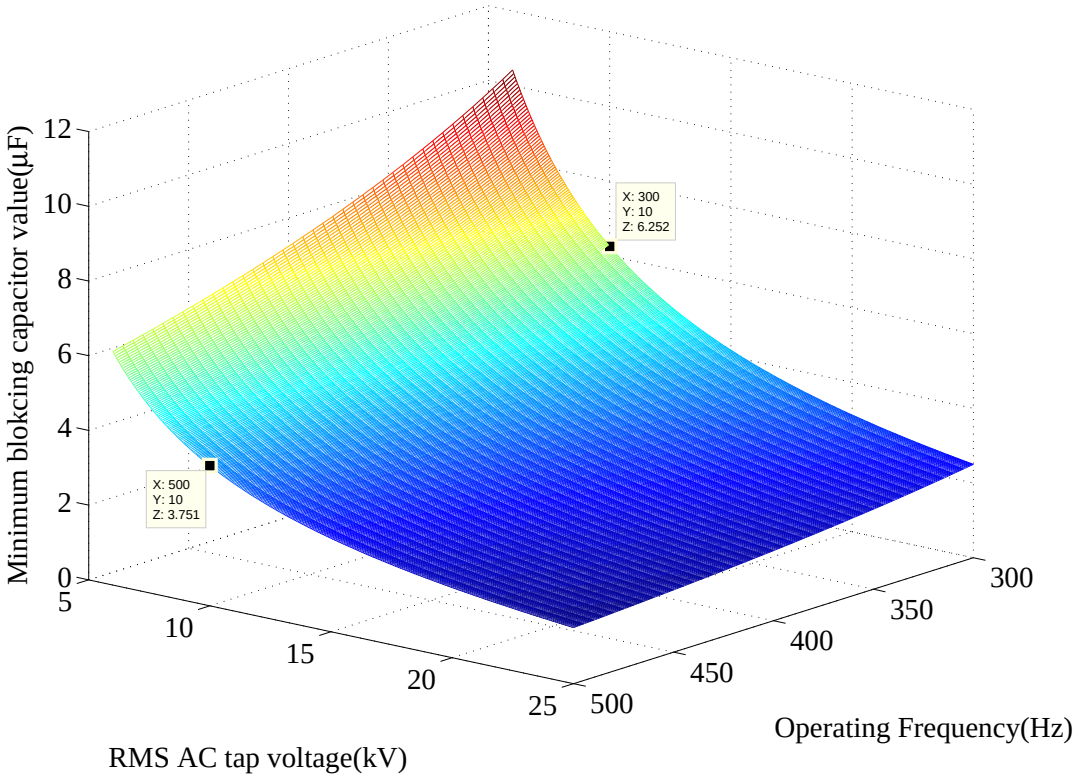


Figure 3.12: Minimum blocking capacitor value vs. V_{AC} & f_f

The AC current in the blocking capacitor causes an increase in peak voltage which must be considered. The peak blocking capacitor voltage is given by (3.25).

$$\begin{aligned}\hat{V}_{Blk} &= V_{Blk_{DC}} + \hat{V}_{Blk_{AC}} \\ &= V_{Blk_{DC}} + \frac{Z_C \cdot \hat{I}_{AC}}{n_{Blk}} \\ &= V_{Blk_{DC}} + \frac{Z_C \cdot \sqrt{2} \cdot \frac{\frac{P_{tap}}{2n_{ph}}}{V_{AC}}}{n_{Blk}} \\ &= \frac{V_{HVDC}}{2n_{Blk}} + \frac{\sqrt{2}P_{tap}}{2n_{ph} \cdot 2\pi C_{Blk} \cdot n_{Blk}} \cdot \frac{1}{f_f \cdot V_{AC}}\end{aligned} \tag{3.25}$$

Then the number of required series blocking capacitors can be rewritten as (3.26).

$$n_{Blk} = \left(\frac{V_{HVDC}}{2} + \frac{\sqrt{2}P_{tap}}{2n_{ph} \cdot V_{AC}} \cdot \frac{1}{2\pi f_f \cdot C_{Blk}}\right) \cdot \frac{1}{\hat{V}_{Blk}} \tag{3.26}$$

Fig 3.13 shows the peak voltage of blocking capacitor as the operating frequency and tap AC voltage are changed, with the chosen value of HVDC voltage as ±300kV and DC blocking voltage as 2kV. At the sample point of V_{AC}=10kV and f_f=300Hz, the peak blocking capacitor voltage is 2.375kV with a 18.8% voltage ripple, which satisfy the ±20% voltage ripple requirement.

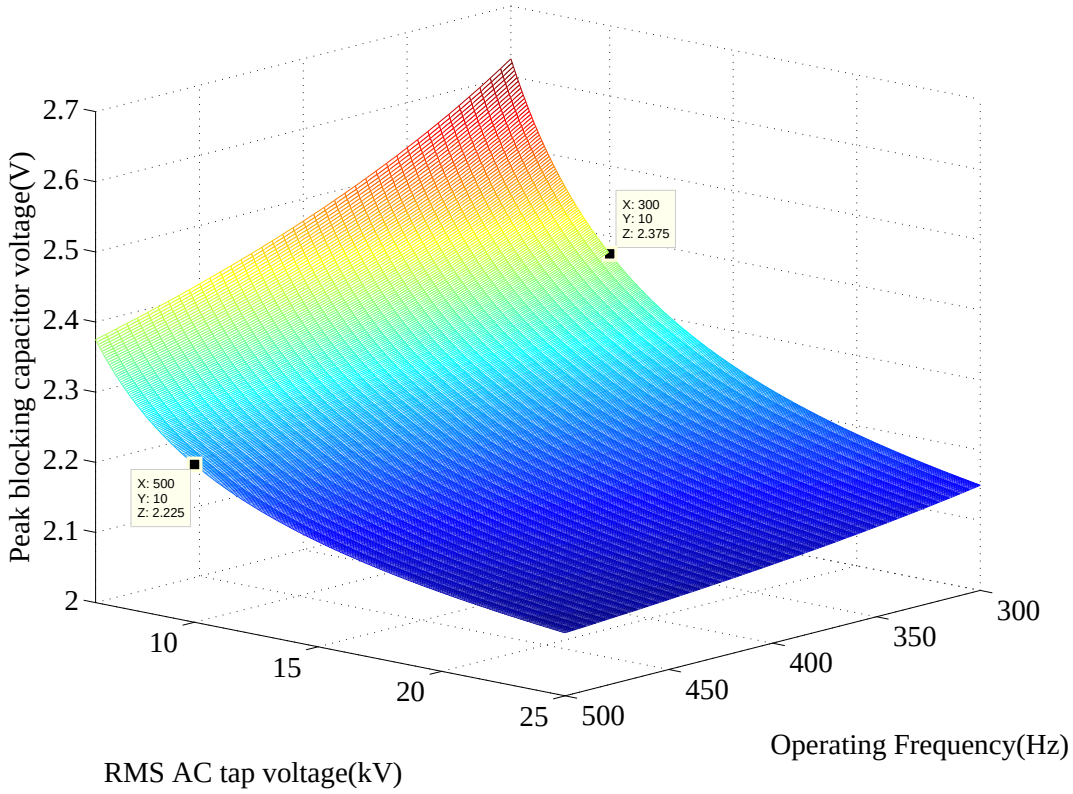


Figure 3.13: Peak blocking capacitor voltage vs. V_{AC} & f_f

3.3.2 Design of Branch Inductor

An inductor is added in series with the blocking capacitor to reduce the net AC voltage drop across the HV to MV coupling impedance by resonating with the capacitor. The following guidelines have been used in designing the branch inductor.

- The maximum voltage drop across the LC branch is required to be 10 % of the AC tap voltage.
- The inductor needs to make the LC branch inductive at the operating frequency for control and filtering of the tap AC current, which means the resonant frequency of the LC needs to be lower than the operating frequency.

Under these assumptions the impedance of the LC blocking branch, Z_f, is given by (3.27). Substituting (3.8) gives (3.28).

$$Z_f \cdot I_{AC} = 0.1 \cdot V_{AC} \tag{3.27}$$

$$Z_f = \frac{0.2{V^2}_{AC} \cdot n_{ph}}{P_{tap}} \tag{3.28}$$

So the inductor L_f is

$$L_f = \frac{1}{(2\pi f_f)^2 \cdot C_f} + \frac{0.1{V^2}_{AC} \cdot n_{ph}}{\pi f_f \cdot P_{tap}} \tag{3.29}$$

Fig 3.14 shows the curves of the inductor value for a two-phase MMST with different branch capacitor valued at the operating frequency of 300Hz and 500Hz.

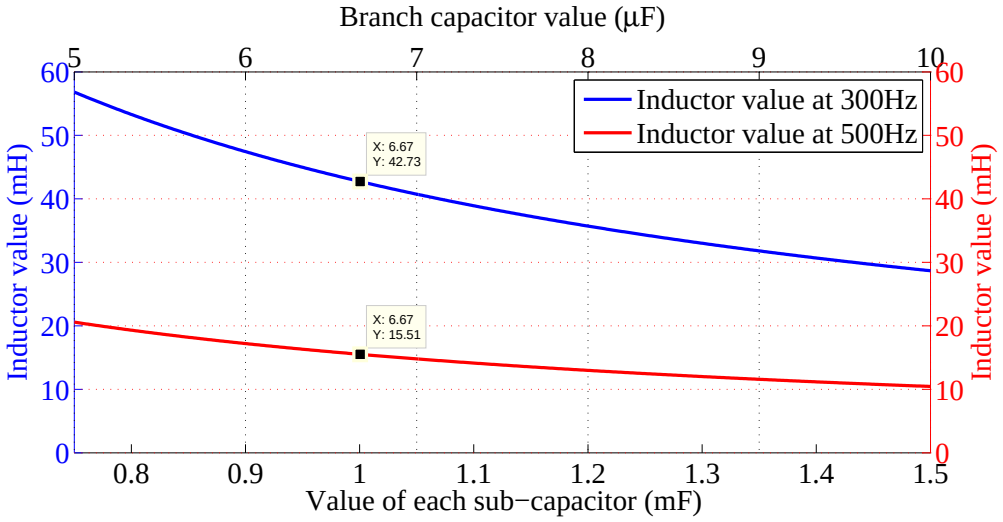


Figure 3.14: Inductor value vs. different capacitor values at 300Hz & 500Hz

The AC current in the conductor will result in the skin effect being observed in the coil. The skin effect is the tendency of an AC current to become distributed within a conductor such that the current density is largest near the surface of the conductor, and decreases with greater depths in the conductor. The electric current flows mainly at the *skin* of the conductor, between the outer surface and a level called the skin depth δ. The skin depth of the conductor is

$$\delta = \sqrt{\frac{\rho}{\pi \mu f_f}} = \frac{6.5}{\sqrt{f_f}} \text{cm} \tag{3.30}$$

where for a copper conductor, the permeability μ is equal to μ_0, and the resistivity ρ is $1.724 \cdot 10^{-6} \Omega \cdot$cm at room temperature. At the operating frequency of $f_f = 300$Hz, the skin depth is $\delta = 3.75$mm. In order to reduce the skin effect, AWG 25 wire (diameter $d = 0.455$mm) is selected. When the diameter of a single wire d is much smaller than the skin depth δ, the proximity effect can be ignored.

The peak current that flows through the coil is

$$\hat{I}_{AC} = \sqrt{2} \cdot \frac{\frac{P_{tap}}{2n_{ph}}}{V_{AC}} \tag{3.31}$$

So the cross sectional area of coil is

$$A_l = \frac{\hat{I}_{AC}}{J} = \frac{\sqrt{2} P_{tap}}{2n_{ph} \cdot V_{AC} \cdot J} = 1.414 \text{cm}^2 \tag{3.32}$$

where J is the maximum current density of the copper coil, which is set to be $J = 5 \text{A} \cdot \text{mm}^{-2}$. Thus the number of strands is

$$n_{strand} = \frac{A_l}{\frac{\pi d^2}{4}} = 228$$

which indicates the branch inductor is designed to be made by 228 AWG25 strands.

In practice the combination of the branch inductor and the blocking capacitor represents a very poorly damped 2$^{\text{nd}}$ order system although the resistance exists in the branch inductor, which is challenging for the control. Therefore an additional damping branch is added. Appendix C gives the method of designing the damping branch.

3.3.3 Size and Loss Analysis of Branch Inductor

For the inductor with the value of 42.7mH and the current of 500A, the volume could be large. The copper losses and core losses of the inductor could also be a significant part of the system loss. Here the size and loss estimation of the branch inductor are carried out. The schematic diagram of the magnetic core is shown in Fig 3.15.

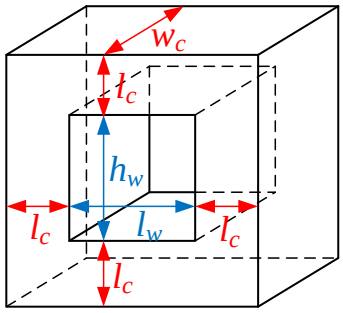


Figure 3.15: Schematic diagram of the magnetic core

The material of the magnetic core is selected to be Si Iron for high maximum flux density. The window utilisation factor k_w is set to be 0.2 considering the isolation of the windings [85]. Then A_p, which is the product of window winding area A_w and the cross sectional area of magnetic core A_c, is calculated as [86]

$$A_p = \frac{L_f \cdot \hat{I}_{AC} \cdot I_{AC-RMS}}{k_w \cdot J_{\max} \cdot B_{\max}} = 1006449\text{cm}^4 \tag{3.33}$$

where B_{max}=1.5T for Si iron core. Setting the number of turns N=100, the window winding area is given by

$$A_w = \frac{N \cdot A_l}{k_w} = 707\text{cm}^2 \tag{3.34}$$

Assuming a square shape of the window winding area, the height and width of the window winding area are $h_w = l_w$ =27cm.

The cross sectional area of the core is given by

$$A_c = \frac{L_f \cdot I_{AC}}{N \cdot B_{max}} = 1423\text{cm}^2 \tag{3.35}$$

Therefore, select l_c=30cm, w_c=50cm. Here $A_p = A_c \cdot A_w = 1093500\text{cm}^4$, which satisfies the requirement of A_p from (3.33). Thus, the branch inductor has the

length of $2l_c + l_w = 87$cm, the width of w_c=50cm and the height of $2l_c + h_w$ =87cm. The volume of the magnetic core is 0.38m^3.

The copper loss of one inductor is calculated as [86]

$$P_{cu} = \rho \frac{N \cdot l_{MLT}}{A_l} I^2{}_{AC-RMS} = 4.88\text{kW} \tag{3.36}$$

where $l_{MLT} = 2l_c + 2w_c$ is the mean length of a turn. The core loss per unit volume is given by [86]

$$P_{fe0} = K_c f^{\alpha} \left(\frac{\Delta B}{2} \right)^{\beta} = 119\text{kW/m}^3 \tag{3.37}$$

where for the Si iron material, K_c=3.388, α=1.7 and β=1.9. δB is the peak -to-peak flux density ripple, which is regarded as $2B_{max}$ in the initial analysis. Then the core loss of one inductor is P_{fe}=35.8kW.

The inductor in the middle blocking branch has the doubled current rating of that of the side branch, so the losses are esimated to be doubled. Therefore, the power losses of the inductors in the two-phase MMST are

$$P_{loss-L} = 8(P_{cu} + P_{fe}) = 325.44\text{kW} \tag{3.38}$$

which yields a inductor loss percentage of

$$\eta_{L-two} = 1.62\%$$

For reducing the inductor losses, the inductor value needs to be reduced by increasing the operating frequency of the MMST or the value of the blocking capacitor.

3.4 Topology Analysis of the Three-phase MMST

3.4.1 Operation Principle of the Three-phase MMST

Here the analysis presented in Section 3.2 and Section 3.3 is repeated for the case of a three-phase MMST. The topology is shown in Fig 3.16, the parameters are provided in Table 3.4. It has three of the Type 1 tap branches in Fig 3.2. The three-phase tap

produces the voltages described by (3.39), in the case of a three-phase tap the AC component of each phase is 120° phase shifted such that the AC component sums to zero.

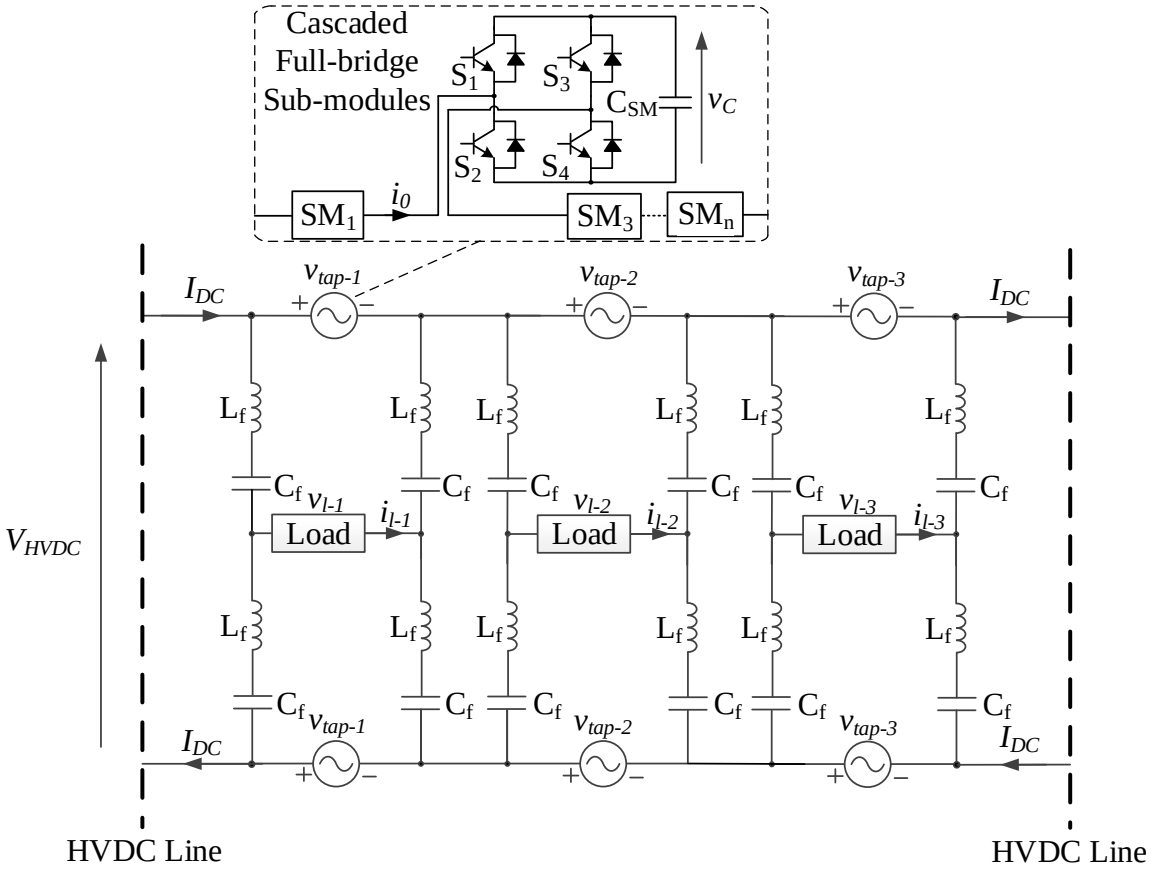


Figure 3.16: Topology of the three-phase MMST

$$\begin{cases} v_{tap-1} = V_{DC} + \hat{V}_{AC} \cdot \sin(\omega t) \\ v_{tap-2} = V_{DC} + \hat{V}_{AC} \cdot \sin\left(\omega t - \frac{2}{3}\pi\right) \\ v_{tap-3} = V_{DC} + \hat{V}_{AC} \cdot \sin\left(\omega t - \frac{4}{3}\pi\right) \end{cases} \tag{3.39}$$

The basic parameters of the three-phase MMST, as listed in Table 3.4, are the same as for the two-phase case except for the DC tap voltage and the RMS AC voltage. The range of RMS AC voltage is 3–20kV. According to (3.6), the DC bias voltage is V_{DC}=-3.3kV.

Table 3.4: Three-phase MMST parameters

Parameter	Value
HVDC Voltage (V_{HVDC})	±300kV
HVDC Current (I_{DC})	1000A
Tap Power (P_{tap})	20MW
DC Bias Voltage ($V_{DC-total}$)	20kV
RMS AC voltage in Tap Voltage (V_{AC})	3–20kV (sample 6.35kV)
Maximum Sub-module Current ($\hat{I}_{SM}$)	1500A
Capacitor Voltage of Sub-module (V_C)	2kV
Operating Frequency (f_f)	300–500Hz

3.4.2 Number of Sub-modules

For the case of a three-phase tap the boundary AC voltage below which parallel strings must be used is given by (3.40). Here it is also assumed that a standardised sub-module found in the typical MMC is utilised in the three-phase MMST, and if the tap arm current exceeds the sub-module current rating then the parallel strings are used.

The minimum number of sub-modules as a function of the AC tap voltage is shown in Fig 3.17. It can be seen that when the RMS AC voltage V_{AC} is lower than the boundary voltage $V_{AC-bound}$, the parallel sub-module strings are needed; when V_{AC} is higher than $V_{AC-bound}$, only one string is required.

$$V_{AC-bound} = \frac{\frac{P_{tap}}{2n_{ph}}}{\frac{\hat{I}_{SM}-I_{DC}}{\sqrt{2}}} = 9.43\text{kV} \tag{3.40}$$

3.4.3 Sub-module Capacitor Size

The analytical method used and assumptions made to calculate the capacitor size are the same as those of the two-phase MMST. The nominal capacitor voltage, V_C, is again chosen to be 2kV and the voltage ripple on the capacitor, V_{ripple}, is set to less than ±5%. The three-phase MMST is operated under the full HVDC

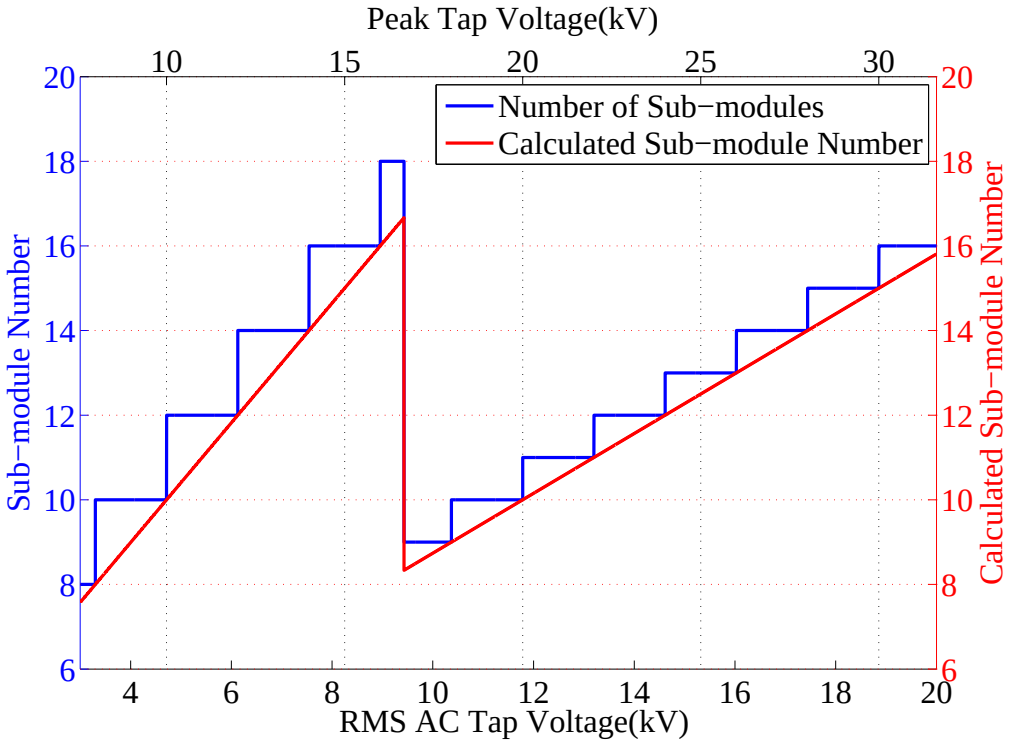


Figure 3.17: Number of sub-modules required per arm for the three-phase MMST

line current. The graph of the capacitor value vs. RMS AC voltage V_{AC} and the operating frequency f_f is shown in Fig 3.18. Sample points are provided for the case of V_{AC} =6.35kV at the operating frequency of 300Hz and 500Hz. The reason why the 6.35kV sample point is selected is introduced later in Section 3.5.

3.4.4 Sub-module Loss Analysis

Power losses have also been calculated for the three-phase MMST using the same modulation and correcting methods presented in Section 3.2. The curves in Fig 3.19 shows the corrected power losses of the three-phase MMST operating at 300Hz fundamental frequency under the full HVDC line current. Here the losses are not compared under the same amount of semiconductor devices when the tap AC voltage varies.

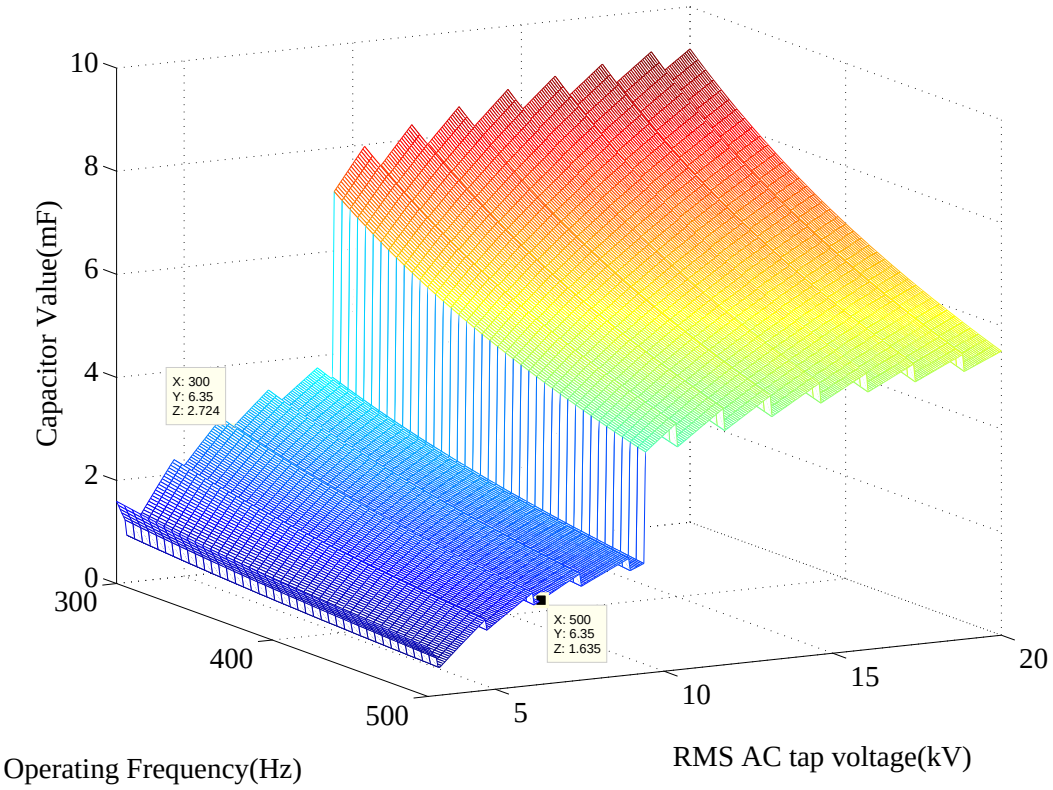
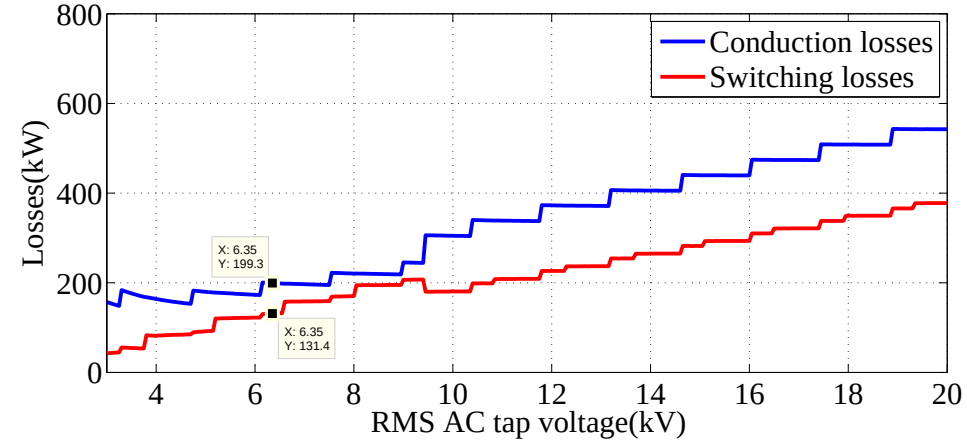


Figure 3.18: Graph of capacitor value vs. V_{AC} & f_f

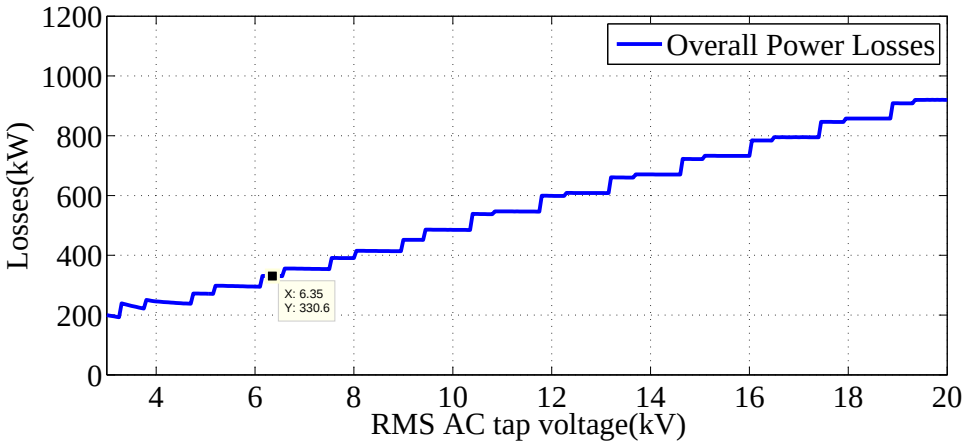
A higher tap AC voltage leads to more sub-modules and higher losses which can be seen from the steps in Fig 3.19(b) since the standardised sub-modules are used.

It can be seen that the overall power losses at AC voltages lower than V_{bound} are relatively low where it should be noted that the number of sub-modules are different. At lower tap AC voltages the tap arm current exceeds the maximum current of standardised sub-modules and the parallel strings are used. As the parallel strings share the total tap current the power losses are less. The figure gives a sample operating point at V_{AC}=6.35kV. At this point, the value of the conduction loss is 199.3kW, the value of the switching loss is 131.4kW and the value of the overall loss is 330.6kW, which yields a percentage loss of

$$\eta_{three} = \frac{P_{cond-tot} + P_{swit}}{P_{tap}} = 1.65\%$$



(a)



(b)

Figure 3.19: Overall power losses: (a) Conduction and switching losses vs. V_{AC}, (b) Overall power losses vs. V_{AC}.

Fig 3.20 shows the overall power losses of the two-phase and the three-phase MMST operating under the full HVDC line current with the same assumption of utilising the standardised sub-module found in the MMC (from Fig 3.10 and Fig 3.19). Comparing the losses of sample operating points, it can be indicated that the two-phase MMST has lower power losses than the three-phase tap under the similar input and output characteristics.

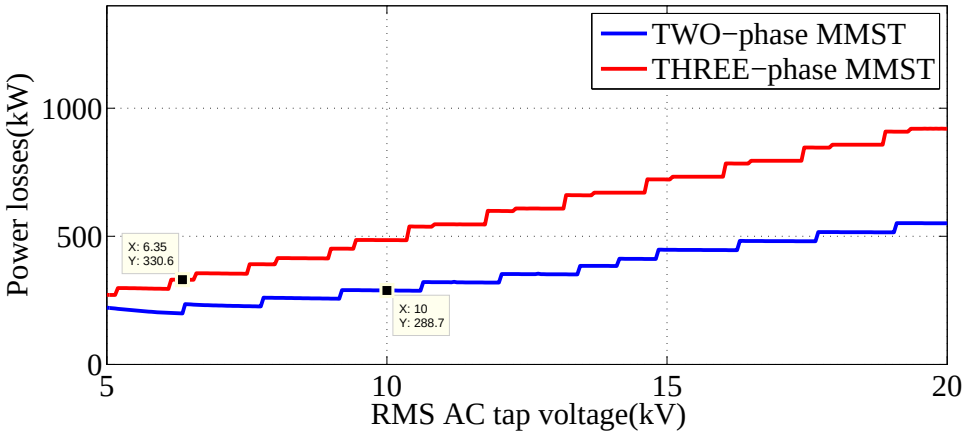


Figure 3.20: Power loss percentage in two-phase and three-phase MMSTs

3.4.5 LC Blocking Branch

Firstly, the blocking capacitor is considered. The DC voltage on the blocking capacitor and the AC current through it in the three-phase MMST are similar to those in the two-phase MMST at the sampling points, so the same blocking capacitor can be applied. The AC loop current is 524A. The voltage ripple on the capacitor is ±19.7% which meets the ±20% requirement. Secondly, the branch inductor can be designed following the procedure for the two-phase case. The AC tap current of the three-phase MMST is higher than that of two-phase, therefore the branch inductor should be designed with more strands.

Following the loss estimation procedure of the inductors in the two-phase MMST, the copper loss of the inductor in the three-phase tap at the operating frequency of 300Hz is P_{cu}=5.12kW, the core loss is P_{fe}=35.8kW. Due to 12 branch inductors used in the three-phase tap, the power losses of the inductors are P_{loss-L}=441.6kW, which yields a percentage of

$$\eta_{L-three} = 2.21\%$$

3.4.6 Three-phase MMST operation during light loading of HVDC Line

For normal operation all series HVDC taps rely on the DC line to conduct current. The case where the DC line is not operating at rated current is refereed to here as light loading. Operation of the MMST under these conditions is considered here.

Due to the voltage and current rating of the sub-module, the tap power is restricted by its maximum tap voltage and sub-module current. Based on the relationship of the variables in the MMST shown in Fig 3.21, the ways of restriction are:

- During light loading, the peak tap AC current limited by the maximum sub-module current can be increased, and the tap AC voltage can be decreased to achieve the same net AC power.
- When the DC current decreases, the DC bias voltage of the MMST needs to increase to keep the same DC power, which decreases the available AC voltage on the tap arm.

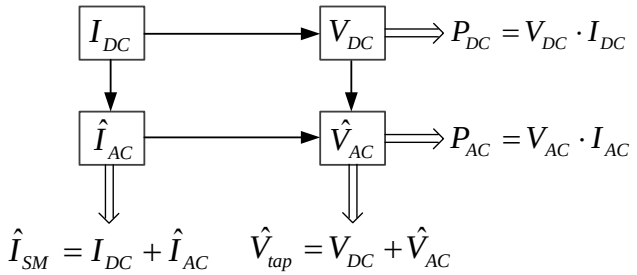


Figure 3.21: Relationship of the MMST variables

On the one hand, the tap power is restricted by the sub-module rated current. During light loading it is proposed that more AC current can be circulated through the sub-module. It is assumed that all the other components are rated for higher current at initial design. At the 10kV, 300Hz sampling point the parallel sub-module strings are required, so the tap AC current is then given by (3.41). The peak tap arm current and the peak tap AC current are shown in Fig 3.22.

$$I_{AC} = \frac{2\hat{I}_{SM} - I_{DC}}{\sqrt{2}} \tag{3.41}$$

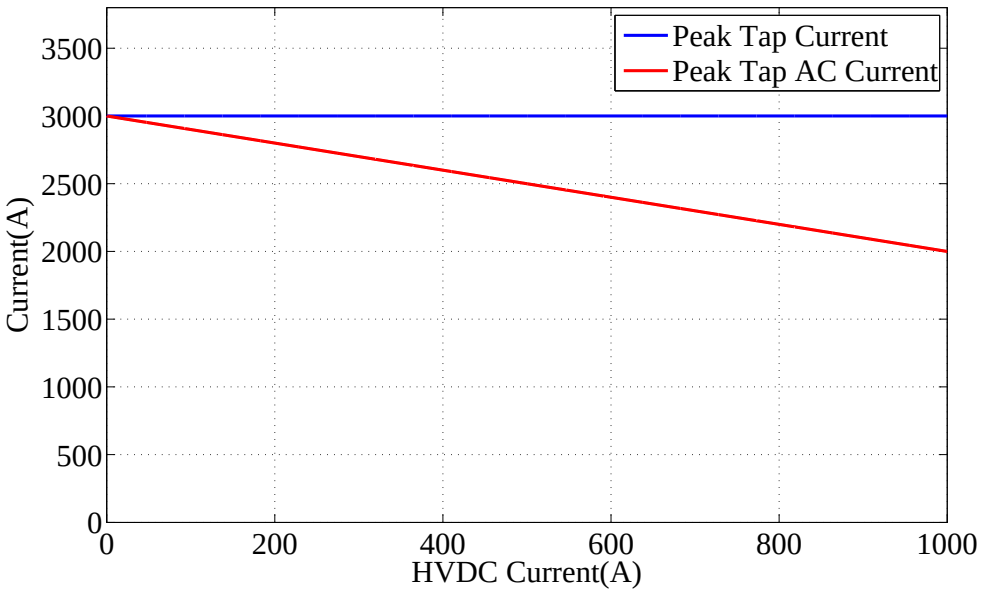


Figure 3.22: Peak arm current and peak tap AC current during light loading

By increasing the tap AC current the tap AC voltage can be reduced to achieve the same net AC power. As consequence of reducing the AC tap voltage there is more available voltage for each tap arm, thus the DC tap voltage may be increased to meet the DC power demand of the tap. Using this approach the peak tap voltage is given by (3.42). However, the peak tap voltage is not able to be higher than the voltage rating of the tap arm $V_{tap-max}$, given by (3.43). Fig 3.23 shows the peak tap voltage requirement during light loading for an example three-phase MMST. The parameters used are listed in Table 3.4 in Section 3.4.

$$\hat{V}_{tap} = V_{DC} + \hat{V}_{AC} = \frac{\frac{p_{tap}}{2n_{ph}}}{I_{DC}} + \sqrt{2}\frac{\frac{p_{tap}}{2n_{ph}}}{\frac{2\hat{I}_{SM}-I_{DC}}{\sqrt{2}}} \tag{3.42}$$

$$\frac{\frac{p_{tap}}{2n_{ph}}}{I_{DC}} + \frac{\frac{p_{tap}}{2n_{ph}}}{\frac{2}{2\hat{I}_{SM}-I_{DC}}} \leq V_{tap-max} \tag{3.43}$$

On the other hand the tap power is limited by the sub-module rated voltage. By decreasing the DC current the DC voltage needs to be increased to maintain the

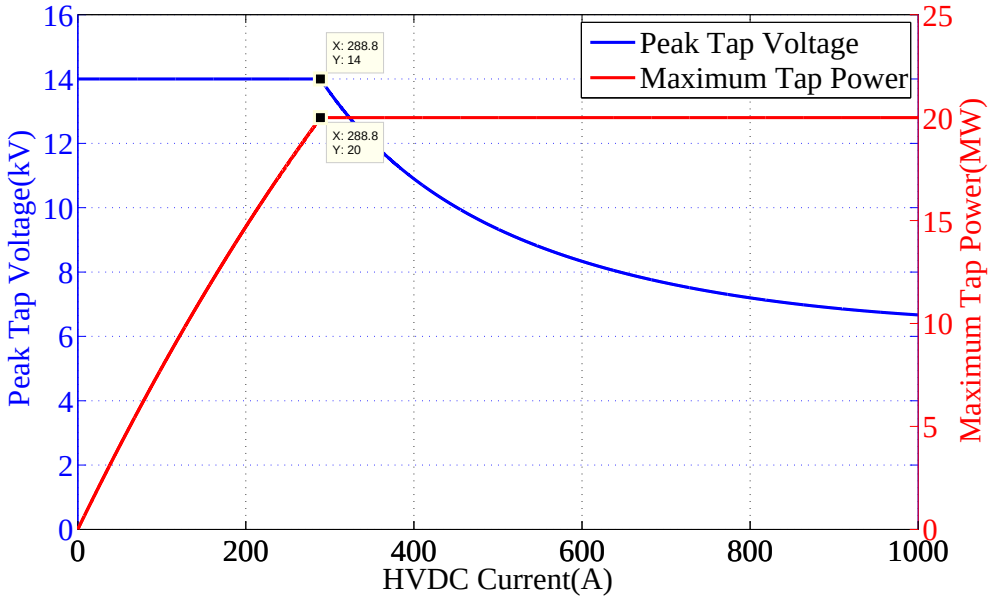


Figure 3.23: Required tap voltage and maximum tap power during light loading

DC power demand of the tap. With the restriction of sub-module rated voltage, the available tap AC voltage is reduced by the increase of DC voltage. The available AC voltage is given by (3.44). However, the AC current can be higher to reach the AC power demand of the tap if the tap current is still lower than the sub-module rated current, which is given by (3.45).

$$v_{AC-avail} = V_{tap-max} - \frac{\frac{p_{tap}}{2n_{ph}}}{I_{DC}} \tag{3.44}$$

$$\hat{I}_{AC} = \sqrt{2} \cdot \frac{\frac{p_{tap}}{2n_{ph}}}{\frac{v_{AC-avail}}{\sqrt{2}}} \leq 2\hat{I}_{SM} - I_{DC} \tag{3.45}$$

Fig 3.24 shows the available tap voltage during light loading. It can be seen from Fig 3.23 and Fig 3.24 that MMST is able to operate at full power without any increase in available voltage even when the DC current is down to 30% of rated current. When DC current is larger than the boundary 288.8A, the tap can operate at the maximum sub-module voltage; when DC current is lower than 288.8A, the tap needs to reduce the operating power in order to meet the requirement of maximum sub-module current. It should be noted however that the DC bias voltage is produced by

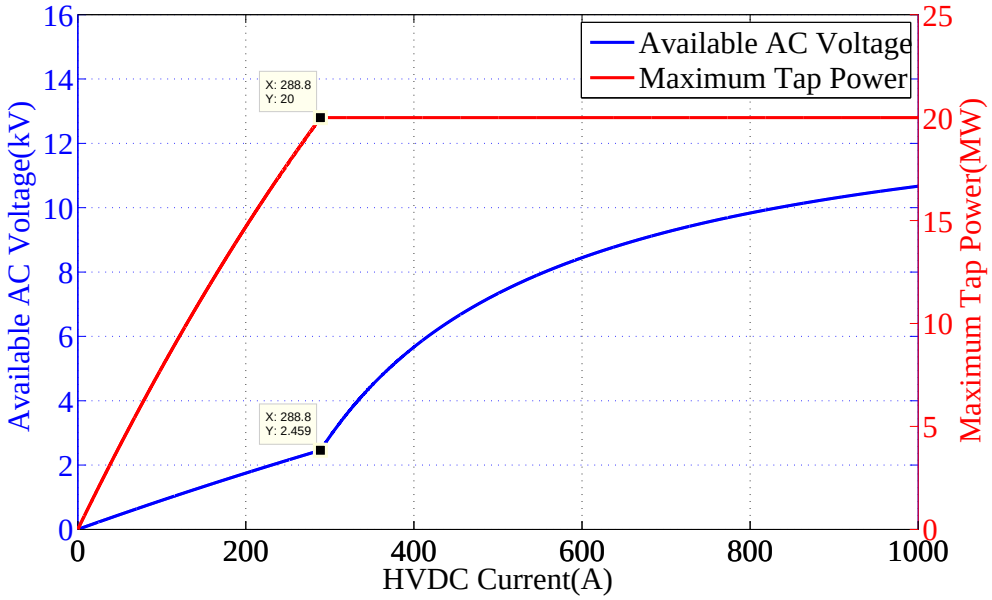


Figure 3.24: Available AC voltage and maximum tap power during light loading

the tap during this type of operation and there should be sufficient available voltage in the HVDC converter station.

3.5 Case Study of Two-phase and Three-phase MMSTs for Sweden South-West HVDC Project

Based on the presented analysis, a case study has been performed based on the South-West Link Project in Sweden presently under construction. The parameters for the case study and two example designs are listed in Table 3.5. 20MW two-phase and three-phase MMSTs are designed based on ±300kV, 1kA South West Link in Sweden. For each type of the MMST two groups of parameters are also calculated with the operating frequencies of 300Hz & 500Hz.

The tap AC voltages of the single phases in two-phase and three-phase MMSTs are selected as 10kV and 6.35kV respectively for more effective comparison under similar input characteristics and output characteristics. The MMST transfers HVDC to

Table 3.5: Case study parameters based on South-West Link

Parameter	**Value**	
	Two-phase	Three-phase
HVDC voltage (V_{HVDC})	±300kV	
HVDC current (I_{DC})	1kA	
Tap Power (P_{tap})	20MW	
Total DC Bias Voltage ($V_{DC-total}$)	20kV	
RMS AC tap voltage (V_{AC})	10kV	6.35kV
RMS load current (I_l)	1kA	1.05kA
Operating Frequency (f_f)	300/500Hz	
Blocking capacitor (C_f)	6.67μF	
Number of blocking capacitors ($n_{Blk-total}$)	900	1800
Branch inductor (L_f)	42.7mH/15.5mH	42.4mH/15.2mH
Number of sub-modules (n_{SM})	80	84
Capacitor value in one SM (C_{SM})	3.07mF/1.84mF	2.73mF/1.64mF
Semiconductor power losses (P_{loss})	288.7kW/355.5kW	330.6kW/418.2kW
Inductor power losses (P_{loss-L})	325.4kW/721.4kW	441.6kW/1.09MW
Power loss percentage of tap power (η)	3.07%/5.38%	3.86%/7.52%

MVAC. The range of middle voltage AC is 1kV–35kV, and 11kV line-to-line voltage is a typical voltage. Therefore, for the three-phase MMST the single-phase load voltage is selected to be $\frac{11}{\sqrt{3}} = 6.35$kV. Under the 20MW load power the single-phase load current is 1.05kA. In order to compare the two-phase and three-phase cases effectively, the input characteristics and output characteristics of them are designed to be nearly identical. So for the two-phase MMST, due to the difference of phase number with the three-phase tap, either the load voltage or the load current can only be selected to be identical with three-phase tap under the same output power. Considering the analysis of the sub-module number and the comparison of the power losses of sub-modules, the single-phase load current of the two-phase MMST is selected to be close to that of the three-phase tap, which is 1kA. Then the single-phase load voltage of the two-phase MMST, which is close to the single-phase tap AC voltage V_{AC} due to the LC resonance near the operating frequency, is calculated as 10kV. Under these two sample points the sub-module number is also similar. In conclusion, these two sample points have the identical input characteristics, close output characteristics and similar sub-module numbers.

From Table 3.5 it can be seen that

- With the increase of the operating frequency, the branch inductor value can be reduced, but the inductor losses and semiconductor losses are increased.
- The power losses of the two-phase MMST are lower than that of the three-phase tap under the parameters listed in the table.
- The parameters of two-phase and three-phase MMSTs are nearly the same, but the two-phase MMST has less LC blocking branches (only 6) than the three-phase MMST (12).

In conclusion, the two-phase MMST has the advantages of lower power losses, less blocking branches and obviously lower cost and volume than the three-phase tap at the conditions given above. The visualized schematics of two-phase and three-phase MMSTs with detailed parameters are shown in Fig 3.25 and Fig 3.26, respectively.

3.6 Summary

In this chapter a novel n-phase multi-modular series HVDC tap utilising the modular multilevel structure has been proposed. The detailed analysis and design of the n-phase MMST have been carried out. Firstly, the operating principle and the advantages of n-phase MMST have been introduced. N-phase can be realised by adopting two types of tap branches according to the application. Secondly, the analysis has shown the required number of sub-modules, sub-module capacitor size and power losses for both two-phase and three-phase MMSTs. The power losses and capacitor size can be optimised by utilising parallel strings, however it leads to the additional components for balancing the string currents. Thirdly, the LC blocking branch couples HV to MV sides removing the need for an HV rated isolation transformer. The resonant branch inductor suppresses the AC voltage on the branch and filters the AC current. The inductor losses are also studied. Finally, a comprehensive comparison between two-phase and three-phase MMSTs has been carried out based

on the case study of Sweden South-West HVDC Project. In conclusion, under the conditions of nearly identical input and output characteristics, the two-phase MMST has the advantages of less blocking branches, lower power losses and lower cost and volume than the three-phase MMST.

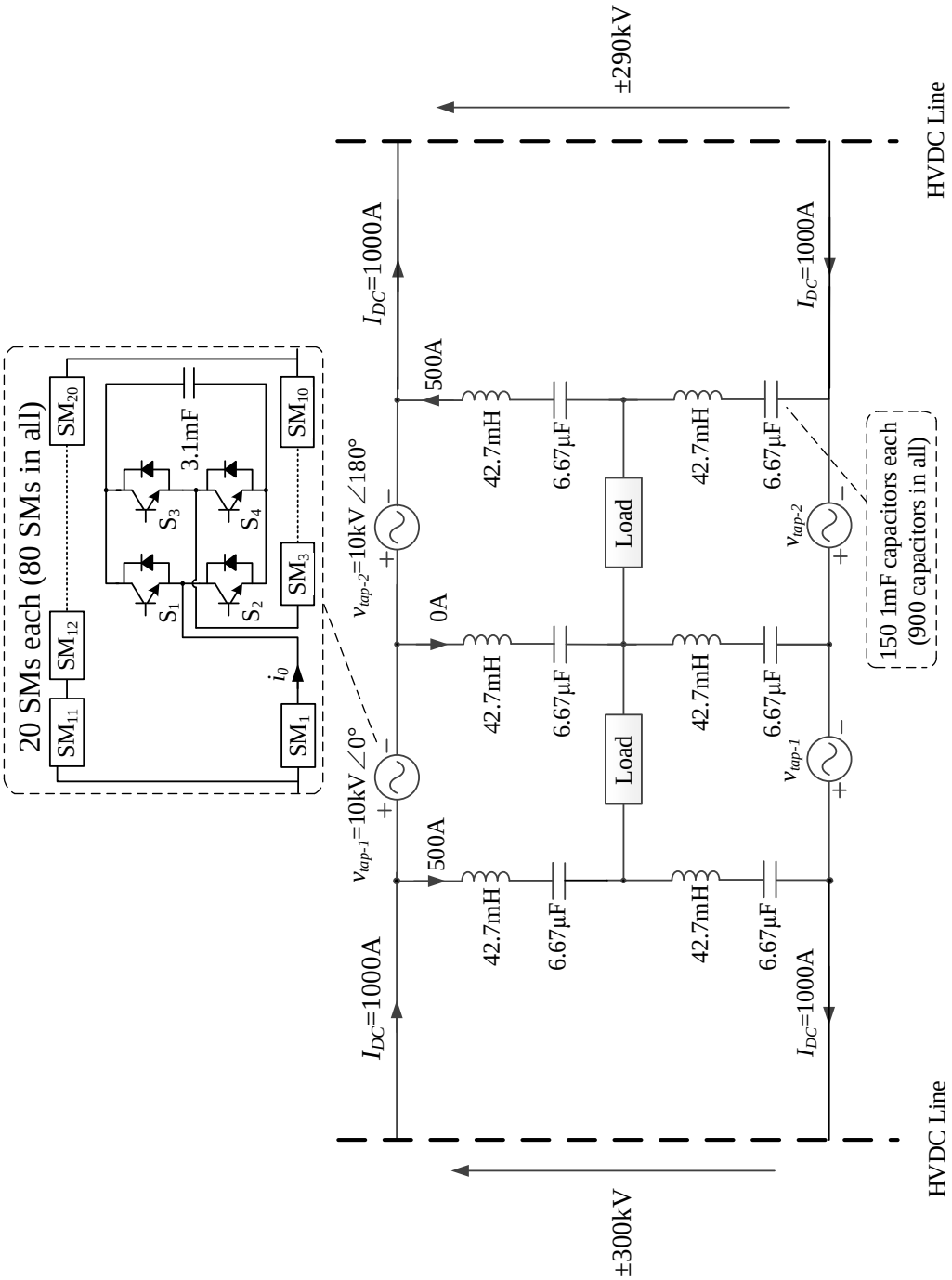


Figure 3.25: Visualized schematic of the two-phase MMST

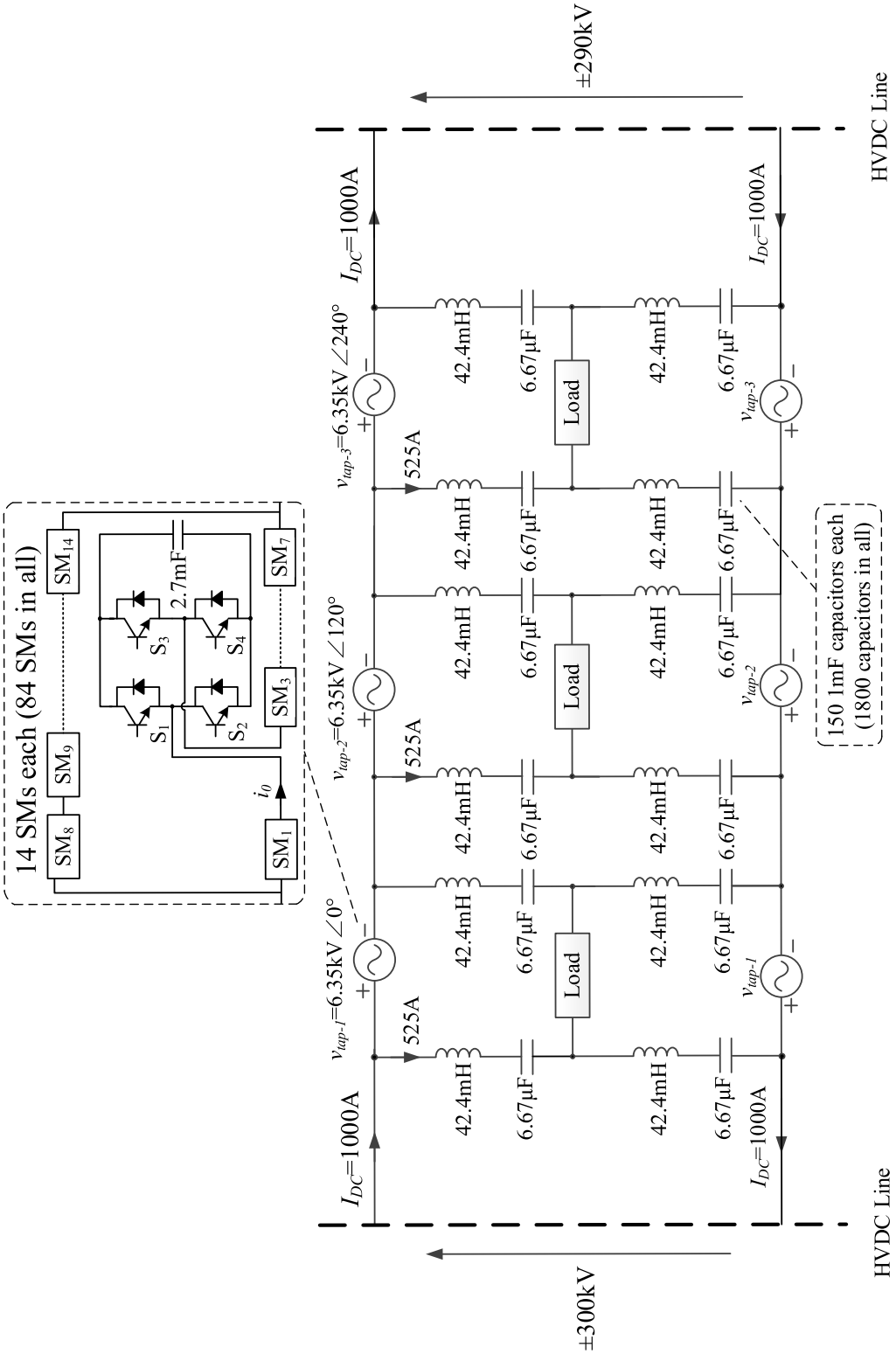


Figure 3.26: Visualized schematic of the three-phase MMST

Chapter 4

Control Strategy of the N-phase MMST

This chapter proposes a control strategy for the two-phase MMST which can be extended into an n-phase topology. This control strategy can also be applied to control any sub-module arm with single or multiple strings. The introduction of the control strategy and the whole control diagram are presented in Section 4.1. The inner current control loop, mean capacitor voltage control loop and outer DC link voltage control loop contained in the presented control strategy are described in Section 4.2, Section 4.3 and Section 4.4, respectively. According to the conclusion of Chapter 3 a two-phase MMST has the advantages of reduced LC branches and power losses when compared to a three-phase MMST, so the simulation of the two-phase MMST has been carried out to validate the control strategy. The simulation results and the loss analysis are presented in Section 4.5.

4.1 Introduction

To realise the MMST operation under the desired conditions, closed loop control of the MMST is implemented. The aims of the MMST control strategy are:

1. To control the AC loop current of each phase.
2. To keep the mean capacitor voltage of the sub-modules across one HV tap arm stable.
3. To keep the second-stage DC link capacitor voltage stable.

For the first aim, the AC loop currents of each phase in the MMST needs to be controlled in order to regulate the energy transmission from the HVDC line to the load. For the polyphase converter a universal control strategy is necessary for any number of phases, for which a single-phase control is required. In addition, in a three-phase MMST it is more suitable to implement the DQ transformation to control the three-phase AC currents, but the mean capacitor voltage control of each tap arm is challenging. Therefore, the loop currents of each phase needs to be regulated individually in the n-phase MMST, and a regulator that can control the single-phase loop current should be selected. For regulating an AC current the proportional-integral (PI) regulator is not the first choice because the bandwidth of PI regulator cannot guarantee high enough gain at the AC frequency, i.e. the tracking error cannot be eliminated. Instead the use of a proportional resonant (PR) regulator [87] is considered for the AC value control.

For the second aim, the sub-module capacitor voltage should be regulated with a limited ripple so that an AC demand can be effectively tracked. With the rotation method based on the sorting method explained in Section 2.3, each capacitor voltage in one tap arm can be balanced, so the second aim can be realised only by controlling the mean capacitor voltage. A PI regulator is adopted for controlling the mean capacitor voltage.

For the third aim, the voltage of the second-stage DC link capacitor needs to be controlled in order that the load voltage of the MMST can be stabilised and the second-stage output voltage can be modulated by the VSC. With this control the load of the MMST can be regarded as a controllable voltage source. Since the second-stage converter and the control design are not included in this work, a proper control loop is presented but not implemented in the control strategy of the MMST.

Each of the tap arms in one phase has an individual control system, controlling the loop current and the mean capacitor voltage of each sub-module string. The schematic diagram of the whole control strategy is shown in Fig 4.1, which the inner loop current control, the mean capacitor voltage control and the outer DC link voltage control are labelled in red, blue and pink, respectively. In Fig 4.1 v_{C-mean} is the mean capacitor voltage of sub-modules in one tap arm.

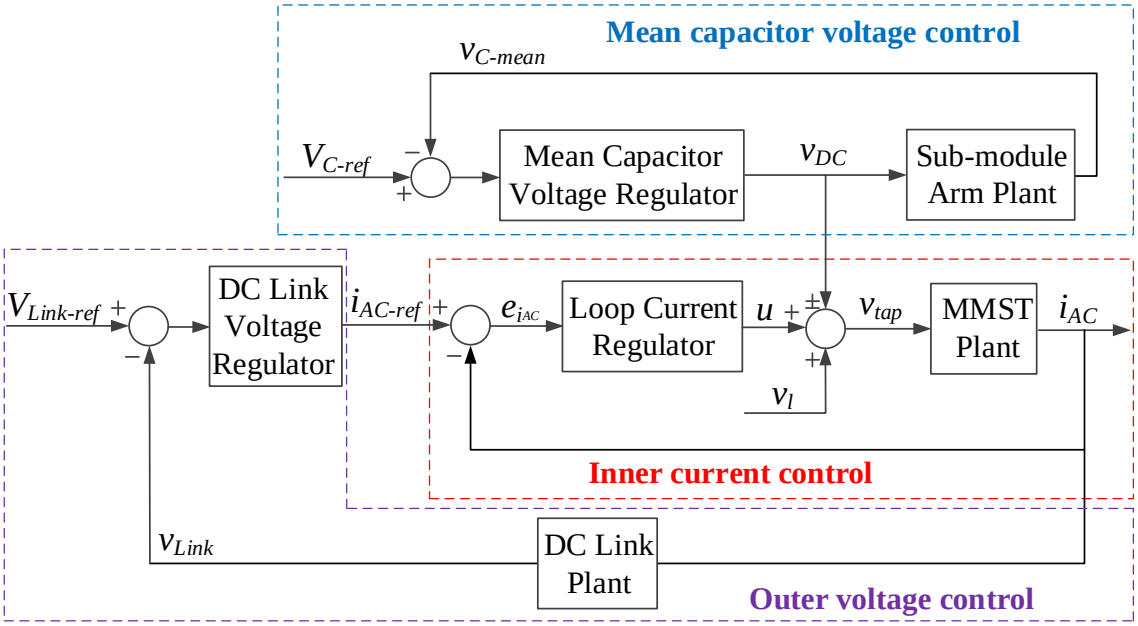


Figure 4.1: Schematic diagram of the control strategy

4.2 Inner Loop Current Control

The diagram of a two-phase MMST is shown in Fig 4.2. Here name the upper and lower tap arms of Phase A, and the upper and lower tap arms of Phase B as ***au***, ***al***, ***bu*** and ***bl***, respectively. The topology of the n-phase MMST is the first stage of the series tap. The load of the MMST is the second-stage converter which typically includes a diode rectifier, a DC link capacitor, and a VSC, as illustrated in Fig 2.5. Therefore, in the analysis the load of the MMST can be regarded as a voltage source. The topology design of the second-stage series tap is not included in this work.

As introduced before, the inner current loop utilises the PR regulator to control the AC loop current. There are several methods of controlling an AC variable including the PR control [87] and the single-phase dq control [88], both of which is able to control the AC loop current. In the initial analysis the PR control is selected to cooperate with the verification of the topology feasibility since the PR control is straight-forward with less mathematical works. The introduction of the PR regulator and the loop design of the inner current control loop are presented as follows.

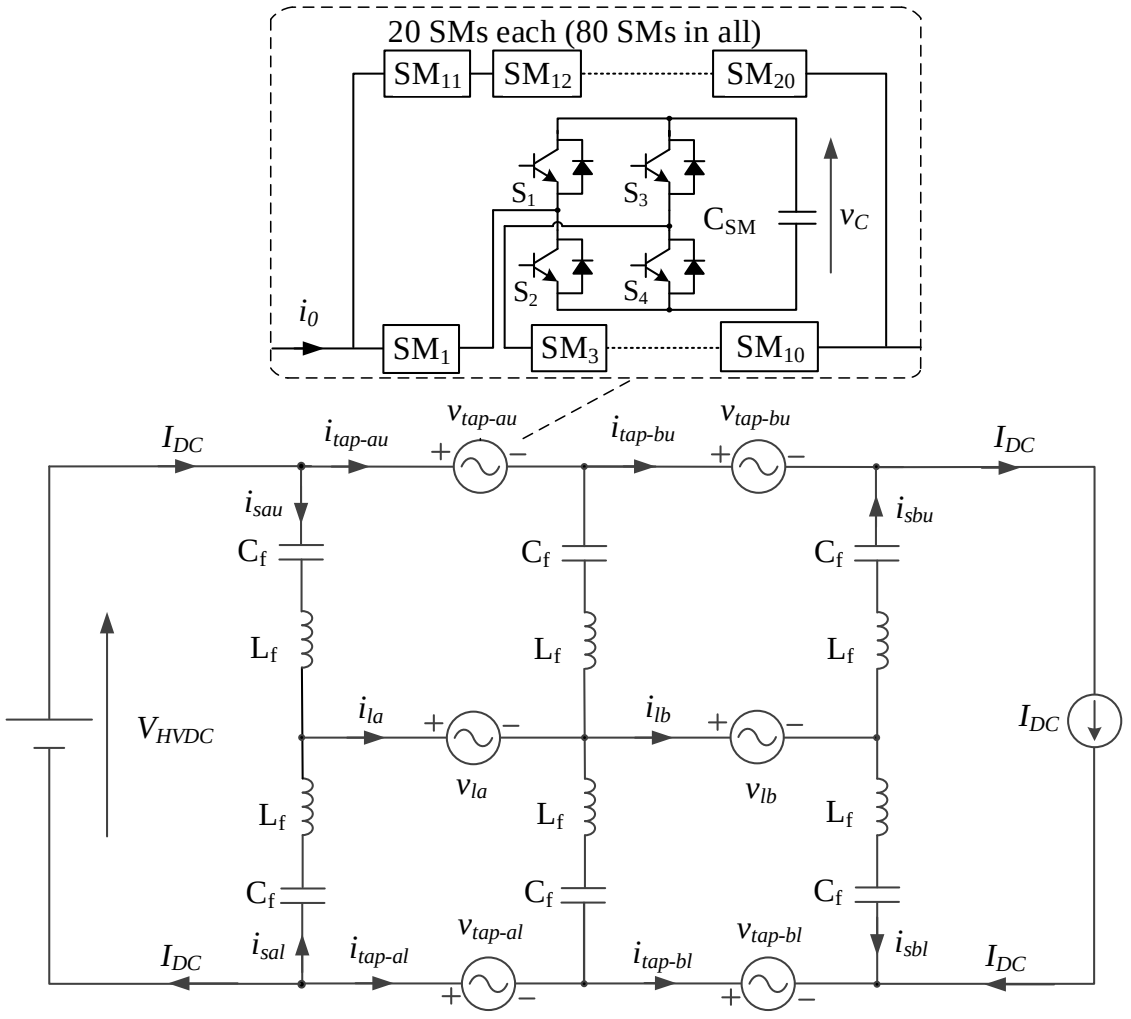


Figure 4.2: Diagram of the two-phase MMST

4.2.1 Introduction of the PR regulator

In the analysis the load is represented by a controllable AC voltage source. As the load is regarded as a voltage source the power transmission from HVDC line to the load is controlled by the AC load current, which is composed of the upper and lower loop currents. For regulating the single-phase AC current the PR regulator is applied for the two-phase MMST.

The PR regulator is widely applied in single-phase AC control systems. It is also utilised for harmonic detection and elimination [87]. The PR regulator is capable of following the AC reference at a certain frequency, eliminating the tracking error and maintaining a good transient response due to the infinite gain at the specific frequency [89].

In this work the major objective for a stationary PR regulator is to achieve zero magnitude and phase errors for the AC loop currents. As illustrated in Appendix D, the PR regulator has an open loop transfer function of [90]

$$G_{PR}(s) = k_p + \frac{2k_r s}{s^2 + {\omega_0}^2} \tag{4.1}$$

$G_{PR}(s)$ gives the ideal PR regulator with an infinite gain at AC frequency ω_0, and no gain and phase shift at other frequencies. Fig 4.3 shows the frequency and phase response of $G_{PR}(s)$ with a set of example parameters.

The ideal integral term provides an infinite gain but a restricted frequency response. However, the LC branch in the n-phase MMST cannot resonate at the exact fundamental frequency due to the inductive impedance design and the errors of capacitor and inductor values. To solve this problem, the non-ideal PR regulator is implemented and gives (4.1) [91].

$$G_{PR}(s) = k_p + \frac{2k_r(\omega_C s + {\omega_C}^2)}{s^2 + 2\omega_C s + ({\omega_C}^2 + {\omega_0}^2)} \approx k_p + \frac{2k_r\omega_C s}{s^2 + 2\omega_C s + {\omega_0}^2} \tag{4.2}$$

where $\omega_C \ll \omega_0$ is the cutoff frequency. The bode diagram of a non-ideal PR regulator is shown in Fig 4.4 with a set of example parameters. It is observed that the gain is finite but still relatively high to keep accurate tracking. In addition, the bandwidth

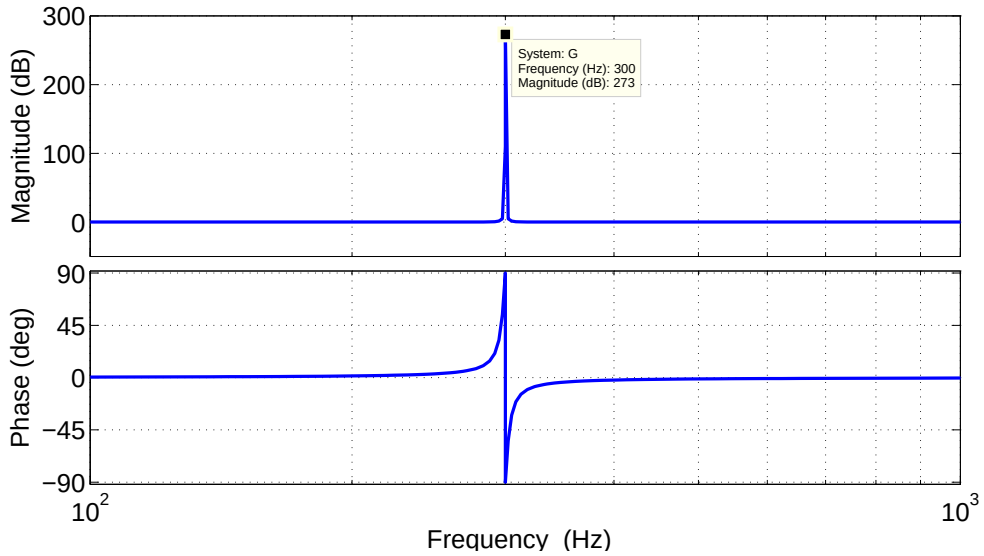


Figure 4.3: Bode diagram of the ideal PR regulator ($k_p = 1, k_r = 20, \omega_0 = 2\pi \cdot 300$rad/s)

can be set using the ω_C value appropriately, which is suitable for the condition of slight frequency variation. In practice, ω_C values of 5-15rad/s have been found to provide a good compromise [92].

In the initial design the ideal PR regulator in (4.1) is applied to control the AC loop current.

4.2.2 Dynamic Model of the Load Current Control

Each phase in the two-phase MMST is longitudinally symmetrical, so the dynamic model can be simplified to a single loop, as shown in Fig 4.5. Here the resistance in the branch inductor and the damping branch is represented by R. The AC current flowing in the middle branch is doubled in that it is equal to the sum of the two symmetric currents of the side branches. Thus the voltage drop on the middle impedance is doubled, which is equivalent as doubled impedance with the same loop current. So the overall impedance is three times the side impedance, given by

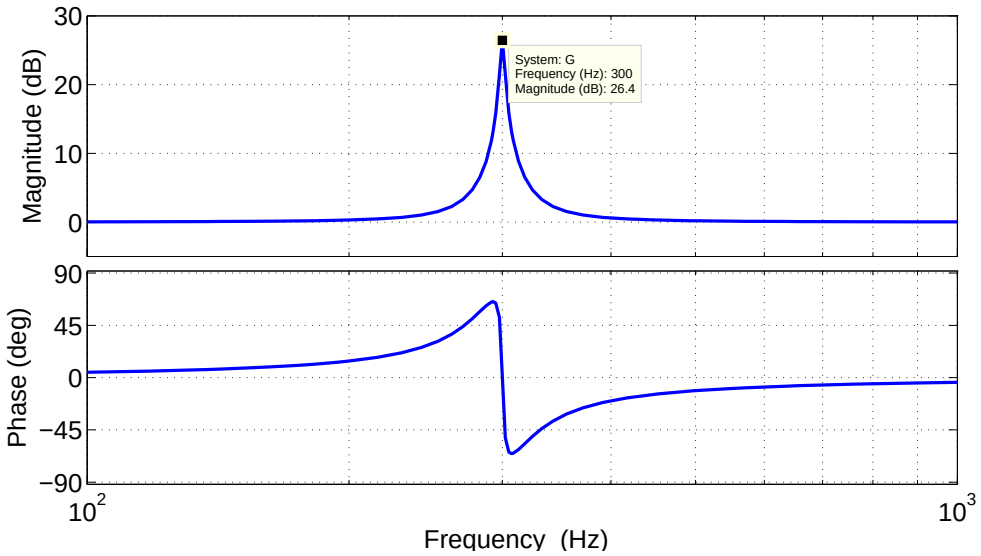


Figure 4.4: Bode diagram of the non-ideal PR regulator ($k_p = 1, k_r = 20, \omega_0 = 2\pi{\cdot}300\text{rad/s}$, $\omega_C = 10\text{rad/s}$)

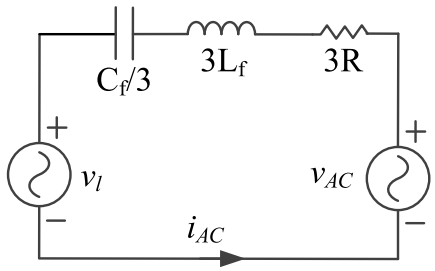


Figure 4.5: Simplified model of the two-phase MMST

$$TF_{equiv}(s) = \frac{1}{3L_f s + 3R + \frac{3}{C_f s}} \tag{4.3}$$

The load voltage can be expressed as [93]:

$$v_l(t) = \hat{V}_l \cos(\omega t + \theta_0) \tag{4.4}$$

where $\hat{V}_l$ is the peak value, ω is the frequency, and θ_0 is the initial phase of load voltage. The dynamic model is given by

$$v_{AC} = 3R \cdot i_{AC} + 3L_f \frac{\mathrm{d}i_{AC}}{\mathrm{d}t} + \int \frac{1}{3C_f} i_{AC} \mathrm{d}t + \hat{V}_l \cos(\omega t + \theta_0) \tag{4.5}$$

which describes a second-order linear system that is excited by a fixed AC output $v_l(t)$. Thus, if v_{AC} is an AC variable with the same frequency ω, i_{AC} is also an AC variable with the same frequency and a certain phase shift.

Based on these equations, the function for the steady-state operating condition is

$$3L_f\frac{\mathrm{d}i_{AC}}{\mathrm{d}t}+\int\frac{1}{3C_f}i_{AC}\mathrm{d}t=-3R\cdot i_{AC}+V_{AC}-V_l \tag{4.6}$$

In (4.6), i_{AC} is the state variable, V_{AC} is the control input, and V_l is the disturbance input. V_{AC} is generated from the sub-modules in the tap arm, which can output from $-n_{SM}{\cdot}V_C$ to $n_{SM}{\cdot}V_C$. Then V_{AC} can be expressed as

$$V_{AC}=n_{SM}{\cdot}V_C{\cdot}m(t) \tag{4.7}$$

where the modulation ratio $m(t)$ is determined by

$$m=\frac{1}{n_{SM}{\cdot}V_C}(u+V_l) \tag{4.8}$$

where u is defined as a new control input, which can be deduced as

$$u=3L_f\frac{\mathrm{d}i_{AC}}{\mathrm{d}t}+\int\frac{1}{3C_f}i_{AC}\mathrm{d}t+3R\cdot i_{AC} \tag{4.9}$$

(4.9) describes a type 0, second-order, linear system. i_{AC} can be controlled by varying u.

4.2.3 Loop Design for the Loop Current Control

According to (4.7) and (4.8) V_{AC} is given by

$$v_{AC}=u+v_l \tag{4.10}$$

which actually expresses the AC component of tap arm voltage V_{tap}. Based on the topology principle described in Section 3.1, a DC bias voltage is required on v_{tap} to inject energy into the tap arms and keep zero net energy exchange in sub-module capacitors, expressed as (3.6). Due to reverse DC current directions in upper and lower arms, the DC bias voltages applied to them are equal but opposite, given by

$$v_{tap}=u+v_l\pm V_{DC} \tag{4.11}$$

The diagram of AC current control loop of a single phase of an MMST is shown in Fig 4.6(a). Fig 4.6(b) shows the simplified current control loop. m_i is the modulation index for one tap arm.

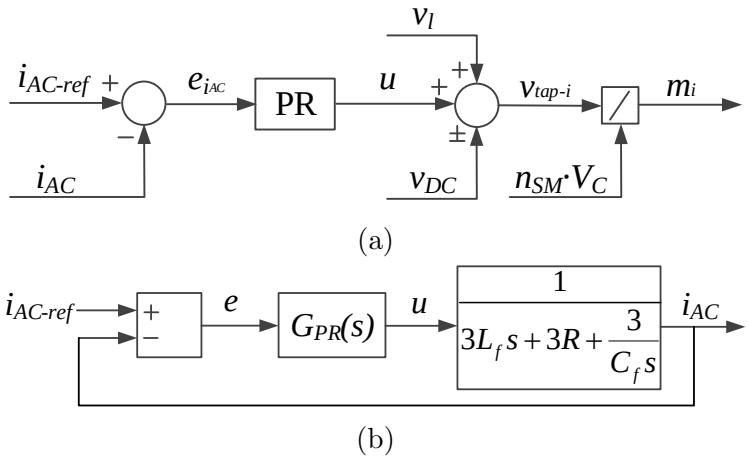


Figure 4.6: Schematic diagram of loop current regulator: (a) Diagram of PR current regulator, (b) Simplified diagram of PR current regulator.

From Fig 4.6(b) and (4.1) the loop gain of current control is given by

$$l(s) = G_{PR}(s) \cdot TF_{equiv}(s) = \frac{s}{s^2 + {\omega_0}^2} \frac{k_{p-I_{AC}} s^2 + 2k_{r-I_{AC}} s + k_{p-I_{AC}} {\omega_0}^2}{3L_f s^2 + 3Rs + \frac{3}{C_f}} \tag{4.12}$$

where $k_{p-I_{AC}}$ and $k_{r-I_{AC}}$ are the proportional and resonant gains of the ideal PR regulator, respectively. It is noted that the loop gain $l(s)$ has four poles and three zeros. Two zeros from PR regulator can be used to cancel two poles from the transfer function, and an AC integrator makes the closed loop transfer function $l(s)/(1+l(s))$ as

$$R(s) = \frac{i_{sa}(s)}{i_{saref}(s)} = \frac{1}{\tau_{PR}\left(s + \frac{\omega^2}{s}\right) + 1} \tag{4.13}$$

if

$$\begin{cases} k_{p-I_{AC}} = \frac{3L_f}{\tau_{PR}} \\ k_{r-I_{AC}} = \frac{1.5\mathrm{R}}{\tau_{PR}} \\ \omega = \frac{1}{\sqrt{L_f \cdot C_f}} \end{cases} \tag{4.14}$$

where τ_{PR} is the time constant of the resultant closed-loop system [93], R is set to be 0.1Ω. τ_{PR} should be small for a fast current-control response, but adequately

large, for example, 10 times the switching frequency of the sub-modules, in order to make the bandwidth of the closed-loop control system $\frac{1}{\tau_{PR}}$ considerably smaller. In this work τ_{PR}=1ms, which gives the parameters of the PR regulator as listed in Table 4.1. In the simulation the parameters of the regulators were minor adjusted.

4.3 Mean Capacitor Voltage Control and the Control Study of Parallel Sub-module Strings

4.3.1 Loop Design of the Mean Capacitor Voltage Control

As for all the converters utilising modular multilevel structures, the energy in the sub-module capacitors has to be maintained throughout the operation. Since the tap arm voltage and current may both have positive and negative polarities in the real application, the charging and discharging time is determined by the real-time power flow direction, calculated from arm voltage multiplied by arm current. Based on the sorting method described in Section 2.3, when the power is injected into the tap arm, the sub-modules with the lowest capacitor voltages are turned on to charge. On the contrary, the sub-modules with the highest capacitor voltages are turned on to discharge [94]. The sub-module switches on or off only when the modulation index changes in order to reduce the switching losses.

The control loop of the mean capacitor voltage is applied as well to cooperate with the sub-module modulation and the capacitor voltage balancing. The dynamic model for a single sub-module capacitor can be given in (4.15). Simplifying ${v_C}^2$ to be $v_C \cdot V_{C0}$ where V_{C0} is the average capacitor voltage, the deduced equation is given in (4.16).

$$n_{SM} \cdot \frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{1}{2}C_{SM} \cdot {v_C}^2\right) = \Delta p_{DC} \tag{4.15}$$

$$\frac{\frac{\mathrm{d}v_C}{\mathrm{d}t}}{\Delta p_{DC}} = \frac{2}{n_{SM}C_{SM}V_{C0}} \tag{4.16}$$

The transfer function of the mean capacitor voltage control loop can be expressed as

$$TF_{V_C} = \frac{v_C}{p_{DC}} = \frac{2}{n_{SM} C_{SM} V_{C0} \cdot s} \tag{4.17}$$

Therefore a proportional regulator $G_{V_C}(s) = k_{p-V_C}$ is utilised to maintain the mean capacitor voltage of one tap arm as constant. The diagram of the mean capacitor voltage control loop of a single tap arm is shown in Fig 4.7(a), where p_{AC} is a feed-forward term, and v_{C-mean} is the mean capacitor voltage of sub-modules in one tap arm. Fig 4.7(b) shows the simplified mean capacitor voltage loop. The energy in each tap arm is maintained by the variation of the DC bias voltage v_{DC}. When the load demands more AC power, the output AC power from the tap arm is increased and the stored energy of the tap arm is decreased, which requires more DC power insertion. Therefore, the DC bias voltage is increased, and vice versa.

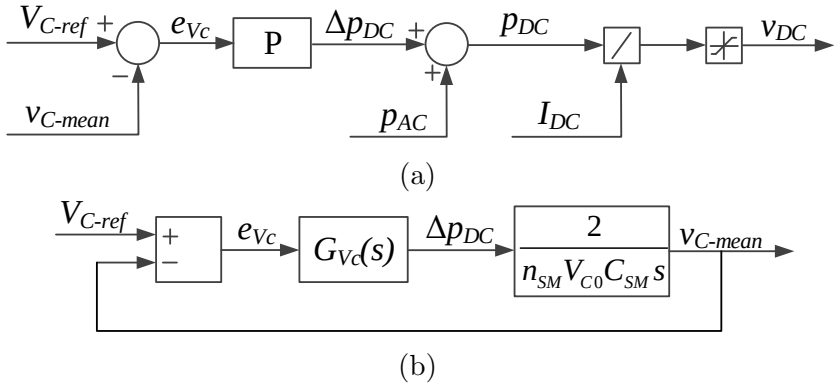


Figure 4.7: Schematic diagram of the mean capacitor voltage control loop: (a) Diagram of the proportional regulator, (b) Simplified diagram of the proportional regulator.

From Fig 4.7(b) the loop gain of the mean capacitor voltage control is expressed as

$$l_{V_C}(s) = \frac{2k_{p-V_C}}{n_{SM} C_{SM} V_{C0} \cdot s} \tag{4.18}$$

Then, the closed-loop transfer function, which is $l_{V_C}(s)/(1 + l_{V_C}(s))$, becomes

$$R_{V_C}(s) = \frac{1}{\tau_{V_C} s + 1} \tag{4.19}$$

if

$$k_{p-V_C} = \frac{n_{SM} C_{SM} V_{C0}}{2\tau_{V_C}} \tag{4.20}$$

where τ_{V_C} is the time constant of the mean capacitor voltage loop [93]. In this work τ_{V_C}=2ms which gives the value of k_{p-V_C} as listed in Table 4.1. In the simulation the parameters of the regulators were minor adjusted.

A proportional regulator is enough for the mean capacitor voltage control in theory. In practice, however, $G_{V_C}(s)$ would need an integral term to avoid error in the steady state capacitor voltage. Therefore, $G_{V_C}(s)$ is given by

$$G_{V_C}(s) = k_{p-V_C} + \frac{k_{i-V_C}}{s} \tag{4.21}$$

4.3.2 Control Study of Parallel Sub-module Strings

With the variation of the output voltage selection of the MMST, a single string or parallel strings of sub-modules may be used for one tap arm to ensure the sub-modules operating within the current rating, as discussed in Section 3.2. For the MMST with the single sub-module string in each tap arm, the inner current regulator, outer DC link voltage regulator and the mean capacitor voltage regulator are sufficient for the basic control. For the MMST with parallel sub-module strings, the same voltage reference can be applied to the modulation of two strings and the capacitor voltages can be averaged together. Here the current reference of each string is half of the loop current reference, the sampled loop current should also be halved. However, the instantaneous voltage on each capacitor of two strings cannot be exactly equal due to the fabrication errors, or the sub-modules are not turned on or off synchronously due to the deadtime. These result in the unbalanced voltages of two strings which may lead to the existence of circulating current i_{S-circ}, as shown in Fig 4.8. In order to solve this problem, an additional arm inductor L_{arm} is inserted in series with each sub-module string to suppress the circulating current. A small arm inductor should be enough since the voltage difference of two strings is not evident, and the time difference of the deadtime is short. i_{S1} and i_{S2} are the arm currents of

String 1 and *String 2*, respectively. m_{S1} and m_{S2} are the modulation index of *String 1* and *String 2*, respectively. The control diagrams for the parallel strings are shown in Fig 4.9, where $v_{C12-mean}$ is the mean capacitor voltage of sub-modules in both the parallel strings of one tap arm.

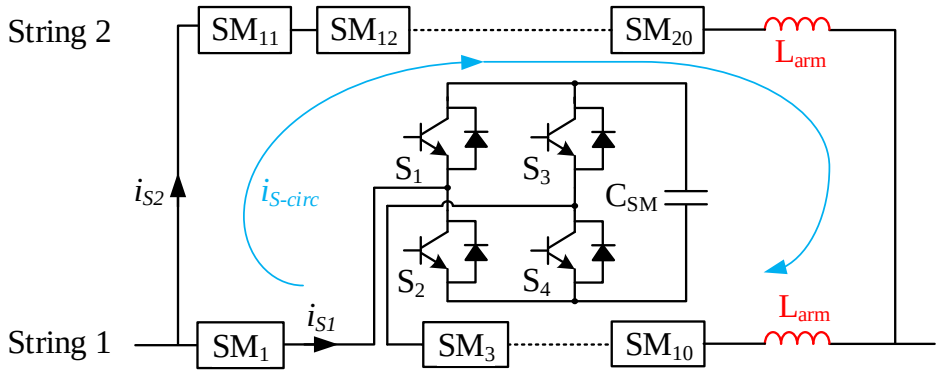


Figure 4.8: Topology of parallel sub-module strings with balancing inductors L_{arm}

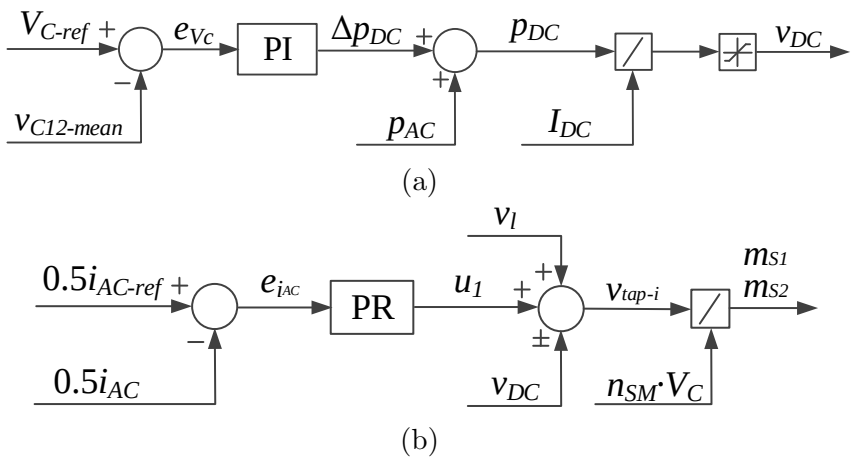


Figure 4.9: Schematic diagram of the control loops of parallel strings: (a) Mean capacitor voltage control, (b) Loop current control.

4.4 Outer DC Link Voltage Control

As a power source, the supplied power from the MMST should vary with the power demand of the load. As shown in Fig 2.5, if the load needs more power, the DC

link capacitor voltage v_{Link} in the second-stage converter of the series tap would decrease, and the MMST should generate more current to recharge the DC link capacitor. Therefore, an outer DC link capacitor voltage loop is used to determine the current reference of the inner current loop, as shown in Fig 4.10.

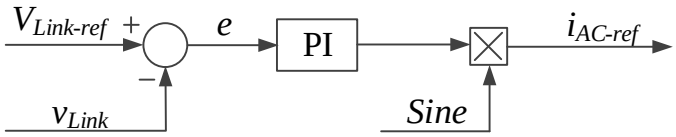


Figure 4.10: Schematic diagram of the load power regulator

Since the research on the second-stage converter of the series tap is not included in this work, the validity of the DC link voltage control loop cannot be verified, and the reference of the inner current loop is set directly according to the designed power and voltage ratings.

4.5 Simulation of a Two-phase MMST

The steady-state simulation of a two-phase MMST with the inner loop current control and the mean capacitor voltage control designed above has been carried out in the PLECS software environment. The diagram of the simulation circuit is shown in Fig 4.2. The parameters in the simulation are listed in Table 4.1. The simulation results including the sub-module losses are presented.

In the simulation the parameters are identical with the designed parameters listed in Table 3.5 in Chapter 3. The HVDC grid is represented by a DC voltage source and a DC current source. As described above the loads are replaced by two 180° phase shifted voltage sources. The modulation technique is based on Sinusoidal Pulse Width Modulation (SPWM) with the level shifted method [95]. The switching frequency is 6kHz which can allow 10 sub-modules to switch twice in one fundamental period. The parameters of the regulators are given as well. The simulation results are shown as follows.

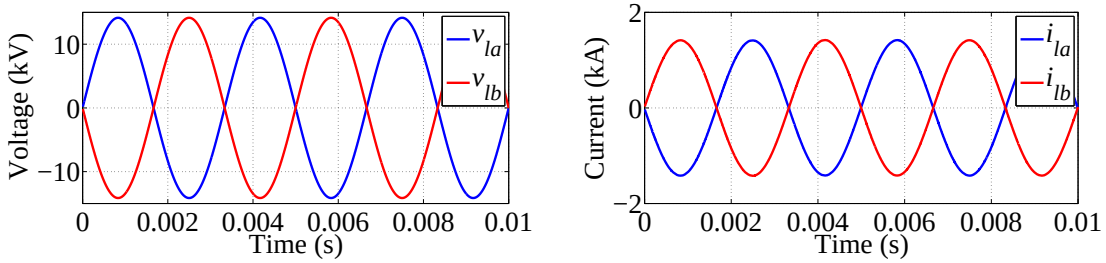
Table 4.1: Parameters of the two-phase MMST in PLECS simulation

Parameter	Value
HVDC Voltage (V_{HVDC})	±300kV
HVDC Current (I_{DC})	1000A
Tap Power (P_{tap})	20MW
Load Voltage (V_l)	10kV
Load Current (I_l)	1000A
Sub-module Capacitor Voltage	2000V
Operating Frequency (f_f)	300Hz
Switching Frequency (f_s)	6kHz
Branch Capacitor (C_f)	6.67μF
Branch Inductor L_f)	42.7mH
Branch Resistor (R_f)	0.1Ω
Arm Inductor (L_{arm})	0.5mH
$k_{p-I_{AC}}$ of current control (PR)	200
$k_{r-I_{AC}}$ of current control (PR)	500
ω of current control (PR)	$2\pi \cdot 300$
ω_c of current control (PR)	10
k_{p-V_C} of capacitor balancing control (PI)	2×10^4
k_{i-V_C} of capacitor balancing control (PI)	2×10^4

4.5.1 Simulation Results

Fig 4.11 shows the waveforms of load voltages and currents of Phase A and Phase B in the two-phase MMST. The load voltages of Phase A and Phase B are sinusoidal with a 180° phase shift generated from two voltage sources, shown in Fig 4.11(a). The RMS values of load voltages are 10kV, the fundamental frequency is 300Hz. The load currents of two phases, shown in Fig 4.11(b), also have a 180° phase shift. The RMS values of load currents are 1kA, and the THD% of each load current is 0.012% due to a large filtering inductor in LC blocking branches. In addition, the load currents flow from the tap arms to the loads, so for each phase the load voltage and current have a 180° phase shift. Fig 4.11 indicates that the inner current loops can operate normally.

Fig 4.12 shows the load powers of Phase A and B, with the reference value varying from 0 to -10MW linearly from 0s to 0.1s. Fig 4.12 indicates that the load power



(a) (b)

Figure 4.11: Waveforms of load voltages and currents of the two-phase MMST: (a) Waveforms of v_{la} & v_{lb}, (b) Waveforms of i_{la} & i_{lb}.

of each phase can reach the -10MW reference value by the current control, and the direction of the power flow is from the HVDC grid to the load. The load power of each phase reaches the reference after 0.8s, which means that the load currents enter into the steady state after 0.8s.

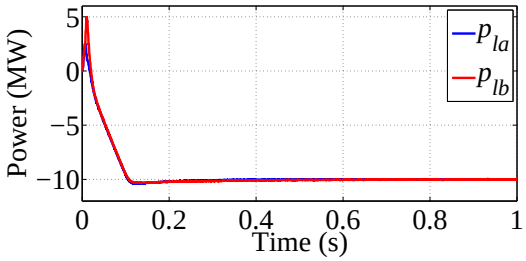
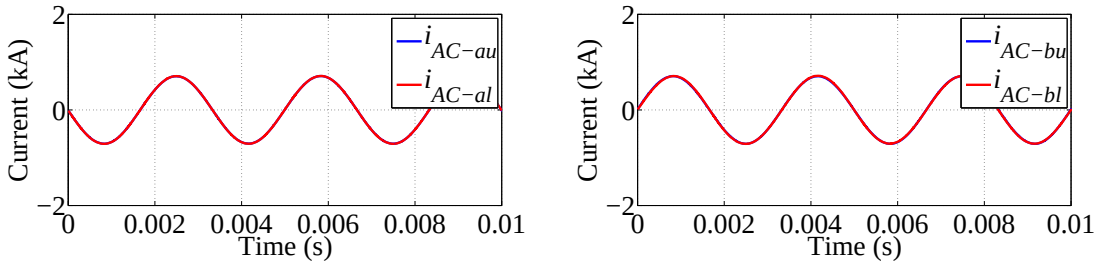


Figure 4.12: Waveforms of load powers of Phase A p_{la} and Phase B p_{lb} in the two-phase MMST

Fig 4.13 shows the waveforms of the loop currents of each phase, the controlled values of inner current loops. It can be seen in Fig 4.13(a) that the amplitude and phase of two loop currents in Phase A i_{AC-au} & i_{AC-al} are nearly identical because the upper and lower tap arms in Phase A generate the same AC currents to the load. This can also be said for the loop currents of Phase B i_{AC-bu} & i_{AC-bl} in Fig 4.13(b). The RMS values of i_{AC-au}, i_{AC-al}, i_{AC-bu} and i_{AC-bl} are 500A, 500.9A, 500A and 501A, respectively. The steady-state error is approximately 0.2%.

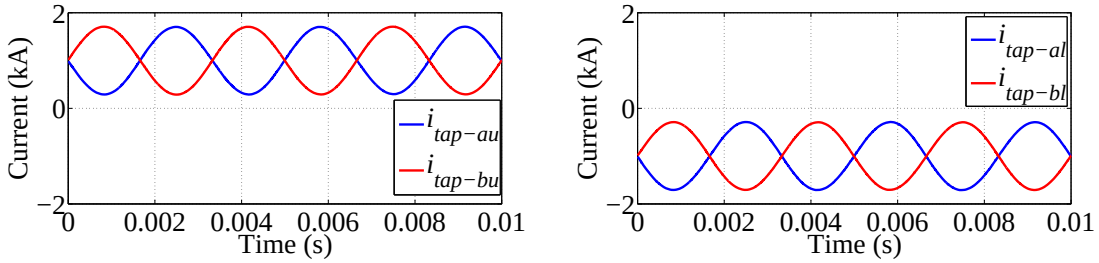
Fig 4.14 shows the waveforms of the currents flowing through the four tap arms. The currents of the two upper tap arms i_{tap-au} & i_{tap-bu}, each of which consists of



(a) (b)

Figure 4.13: Waveforms of loop currents in Phase A and Phase B of the two-phase MMST: (a) Waveforms of i_{AC-au} & i_{AC-al}, (b) Waveforms of i_{AC-bu} & i_{AC-bl}.

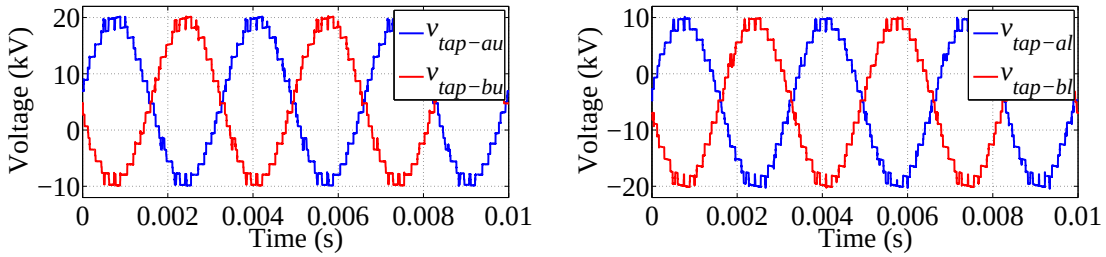
the DC component (HVDC current I_{DC}) and the AC component (loop current i_{AC}), are shown in Fig 4.14(a). The AC components of i_{tap-au} and i_{tap-bu} have a 180° phase shift so there is few AC current flowing into the HVDC line. The currents of two lower tap arms i_{tap-al} & i_{tap-bl}, shown in Fig 4.14(b), also have the DC bias currents but are negative because the HVDC current flows circularly leading to a reverse direction of upper and lower tap arms.



(a) (b)

Figure 4.14: Waveforms of tap arm currents in the two-phase MMST: (a) Waveforms of i_{tap-au} & i_{tap-bu}, (b) Waveforms of i_{tap-al} & i_{tap-bl}.

The waveforms of the tap arm voltages are shown in Fig 4.15. The two upper tap arms v_{tap-au} & v_{tap-bu} have a DC component (DC bias voltage V_{DC}=5kV) and an AC component, as shown in Fig 4.15(a). The AC components of v_{tap-au} & v_{tap-bu} have a 180° phase shift, therefore there are few harmonics from the MMST to the HVDC line. The voltages of the lower tap arms also have the DC bias voltages but are negative due to the reverse direction of the DC current. Whether V_{DC} is positive or not can be determined by (A.3) in Appendix A.

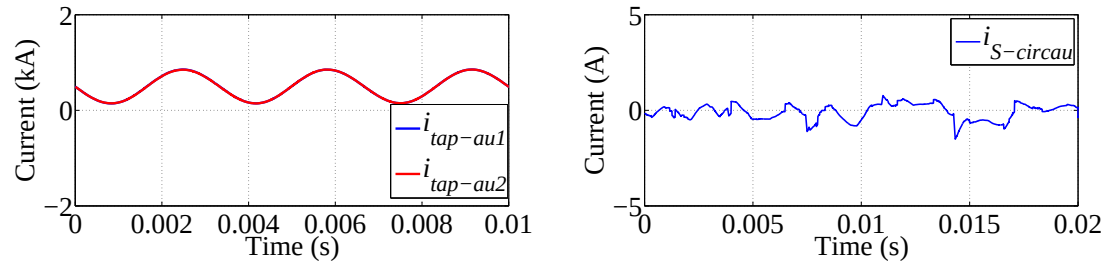


(a) (b)

Figure 4.15: Waveforms of tap arm voltages in the two-phase MMST: (a) Waveforms of v_{tap-au} & v_{tap-bu}, (b) Waveforms of v_{tap-al} & v_{tap-bl}.

Comparing Fig 4.14 and Fig 4.15, it can be found that the arm voltage has an approximately 8° phase lead compared with the arm current in that the LC blocking branch performs inductively at the fundamental frequency.

Fig 4.16 shows the currents of parallel sub-module strings in the upper tap arm of Phase A, $i_{tap-au1}$ & $i_{tap-au2}$, and the circulating current $i_{S-circau}$. It is clear that the currents in the parallel strings can be balanced with the same modulation signal and that the circulating current can be suppressed to be almost zero by the arm inductors.



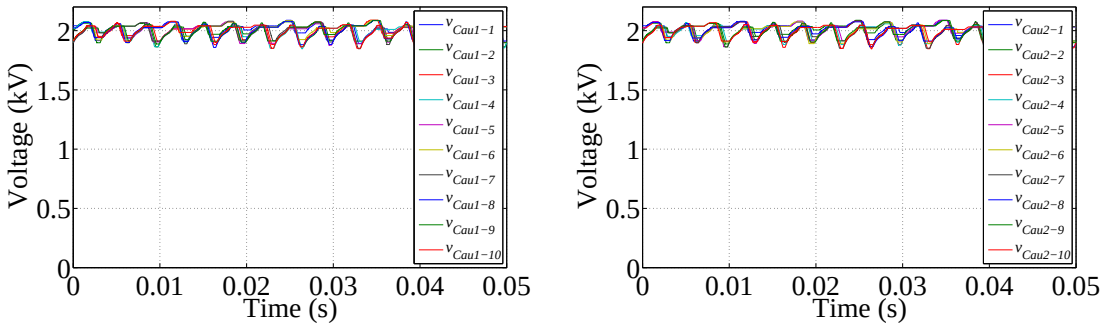
(a) (b)

Figure 4.16: Waveforms of single tap arm currents in the two-phase MMST: (a) Waveforms of $i_{tap-au1}$ & $i_{tap-au2}$, (b) Waveforms of $i_{S-circau}$.

Fig 4.17, Fig 4.18, Fig 4.19 and Fig 4.20 show the capacitor voltages of 10 sub-modules in each of the overall 8 sub-module strings of the two-phase MMST. For instance, in the upper tap arm of Phase A, 10 sub-module capacitor voltages of String 1 in Fig 4.8 are represented by v_{Cau1}, and v_{Cau2} means those of String 2. The

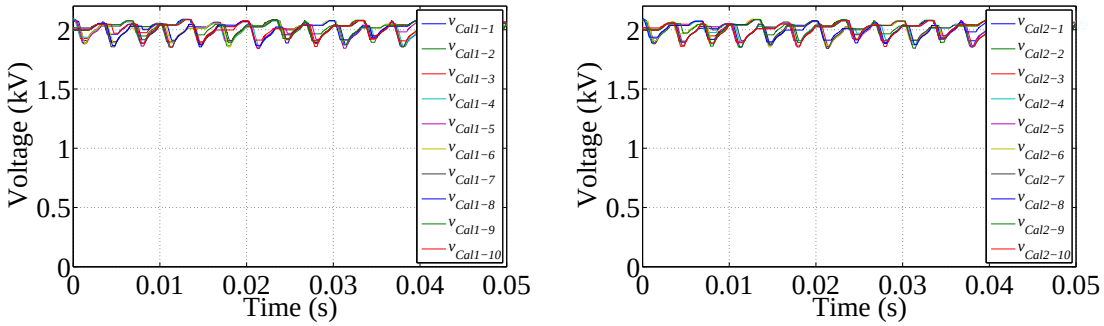
sub-module sorting frequency per arm is equal to the switching frequency.

The switching frequency of every sub-module string is 6kHz, so for each sub-module the switching frequency is 600Hz, which means it can switch on and off twice on average in one fundamental period, i.e. balance on average once in a half period with the balancing method described in Section 4.3. The capacitor voltage ripple is 240V, ±6% of the nominal capacitor voltage, which is slightly more than the designed ±5% voltage ripple. The ripple can be decreased by increasing the switching frequency, but the switching losses will rise.



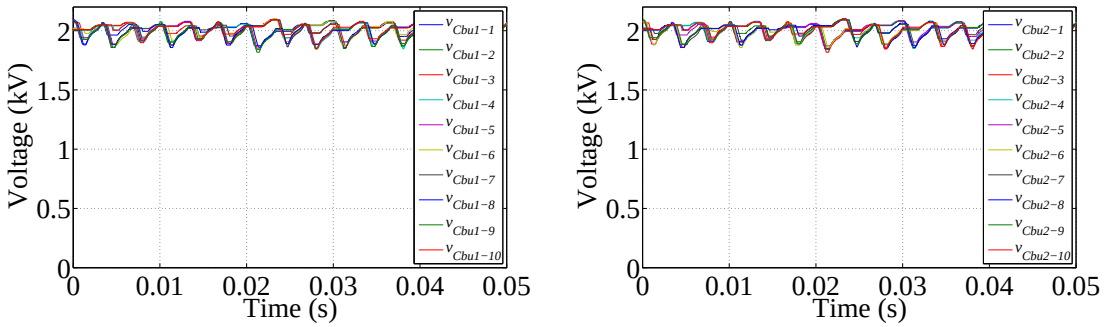
(a) (b)

Figure 4.17: Waveforms of capacitor voltages of the tap arm au: (a) v_{Cau1}, (b) v_{Cau2}.



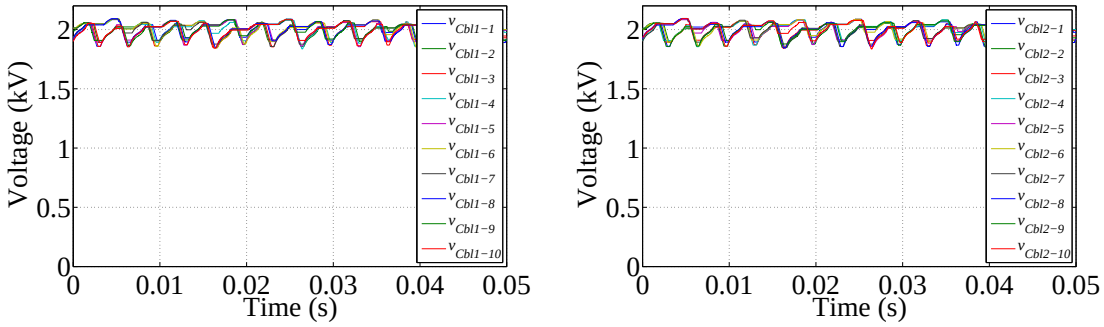
(a) (b)

Figure 4.18: Waveforms of capacitor voltages of the tap arm al: (a) v_{Cal1}, (b) v_{Cal2}.



(a) (b)

Figure 4.19: Waveforms of capacitor voltages of the tap arm bu: (a) v_{Cbu1}, (b) v_{Cbu2}.

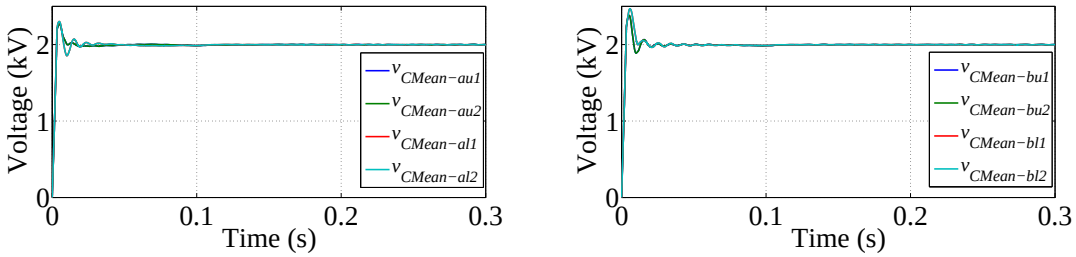


(a) (b)

Figure 4.20: Waveforms of capacitor voltages of the tap arm bl: (a) v_{Cbl1}, (b) v_{Cbl2}.

The mean capacitor voltages of eight sub-module strings are shown in Fig 4.21. It is obvious from the waveforms ranging from Fig 4.17 to Fig 4.21 that the capacitor voltages of each string can be balanced and the mean voltage can be controlled to be 2kV. The mean capacitor voltages enter into steady state after 0.2s, which shows the mean capacitor voltage control is faster than the loop current control.

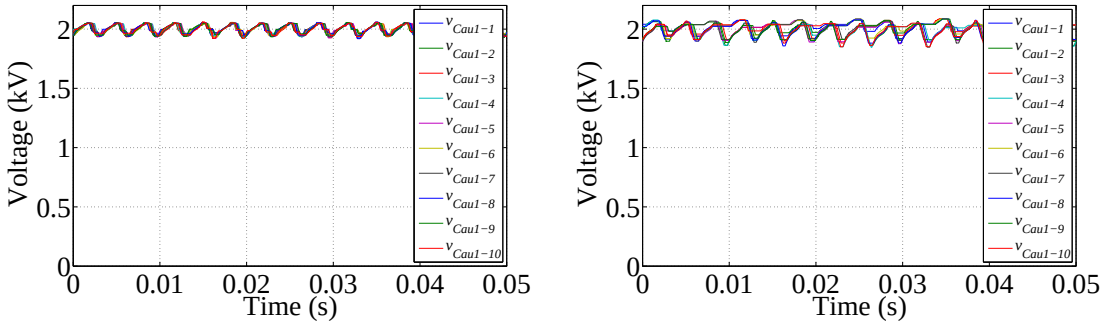
By increasing the switching frequency to 12kHz, the sub-modules are balancing at 12kHz, and the capacitor voltage ripple decreases to 140V, ±3.5% of the nominal capacitor voltage, as shown in Fig 4.22(a). However, the increase of the switching frequency adds little to the performance of the converter since the THD% of the load currents at 6kHz is already low enough (0.012%). Furthermore, the switching losses, which are analysed below, are doubled at 12kHz compared with those at 6kHz. In



(a) (b)

Figure 4.21: Waveforms of mean capacitor voltages of each sub-module string in the two-phase MMST: (a) Waveforms of $v_{Cau1-Mean}$, $v_{Cau2-Mean}$, $v_{Cal1-Mean}$ & $v_{Cal2-Mean}$, (b) Waveforms of $v_{Cbu1-Mean}$, $v_{Cbu2-Mean}$, $v_{Cbl1-Mean}$ & $v_{Cbl2-Mean}$.

conclusion, 6kHz switching frequency is sufficient for the MMST operation.



(a) (b)

Figure 4.22: Waveforms of capacitor voltages of sub-module string au1 under different switching frequencies: (a) Waveforms of v_{Cau1} under 12kHz, (b) Waveforms of v_{Cau1} under 6kHz.

4.5.2 Loss Analysis of the Two-phase MMST

The power loss of the converter is an important design index indicating the efficiency of the system directly. The power losses of the sub-modules in the two-phase MMST have been analysed and simulated in PLECS software. The comparison of conduction losses and switching losses in the simulation with the losses calculated in the Matlab script has also been carried out.

PLECS software allows the designer to input the curves of losses point by point from the datasheet, ensuring the accuracy of the power loss calculation. The curve data of losses, shown in Fig 4.23, is derived from the datasheet of MITSUBISHI CM1200HG-66H HVIGBT modules shown in Fig B.1 by the interpolation method. The temperatures labelled in the figure are the junction temperatures of IGBT modules from the datasheet. These curve data contain the conduction and switching losses for the IGBT and the diode. When the current i_{on} is negative, the diode turns off or conducts, and curves of the reverse recovery losses and conduction losses of the diode with the x-axis of negative current are shown in Fig 4.23(b) and Fig 4.23(c), respectively. The negative diode forward voltage times the negative current turns to the positive power losses.

The results of the conduction losses and switching losses with the variation of switching frequency f_f are listed in Table 4.2. The losses are simulated under the condition of 25°C junction temperature. It can be found that with the increase of the switching frequency, the conduction losses change only slightly, whilst the switching losses rise linearly, as shown in Fig 4.24.

Table 4.2: The power losses of the two-phase MMST

Switching Frequency f_s	Conduction Losses p_{cond}	Switching Losses p_{swit}
6kHz	189.1kW	103.4kW
12kHz	188.5kW	185.8kW
18kHz	188.8kW	312.0kW
24kHz	188.6kW	411.7kW
30kHz	188.9kW	547.6kW

From Table 3.5 the conduction and switching losses at 6kHz switching frequency calculated in the Matlab script is 188.4kW and 100.3kW respectively. Comparing with these results, the conduction and switching losses of two-phase MMST in simulation has 0.4% and 3% differences respectively, which indicates that the results from both Matlab script and the PLECS simulation agree closely.

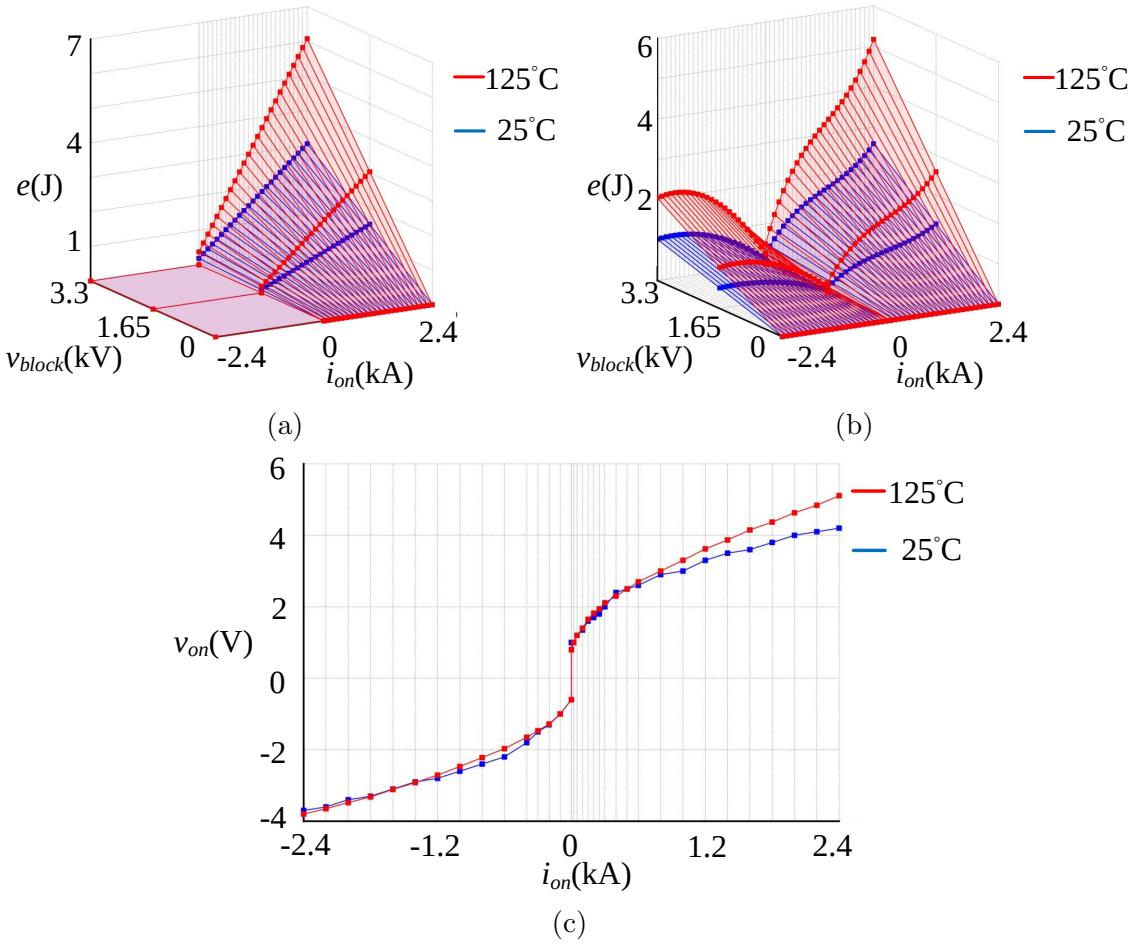


Figure 4.23: Curves of switching losses and conduction losses in the PLECS simulation: (a) Curves of turn-on losses, (b) curves of turn-off losses, (c) Curves of conduction losses.

4.6 Summary

In this chapter the control strategies for the n-phase MMST has been presented. The control loops have been designed and verified based on an example two-phase MMST. The control strategy consists of the inner loop current control, the mean capacitor voltage control and the outer DC link voltage control. In addition, for the topology with the parallel strings in one tap arm, an additional arm inductor is adopted for suppressing the circulating current. The simulation of the two-phase MMST with the loop current control and mean capacitor voltage control has been carried out in

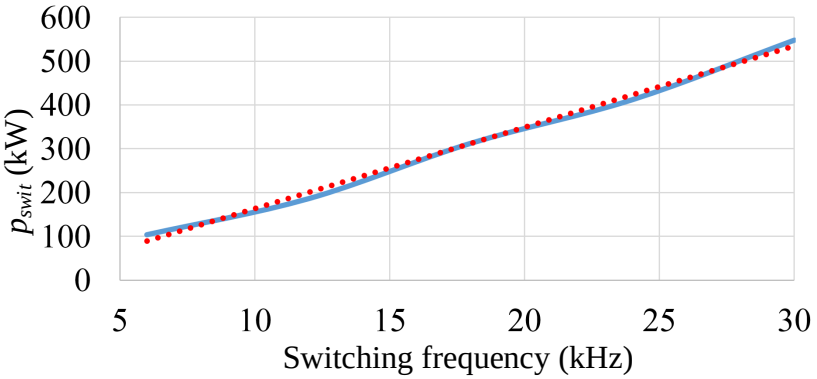


Figure 4.24: Curve of switching losses of the two-phase MMST p_{swit} vs. switching frequency f_s

PLECS Software. The results indicate that the load currents of two phases and the mean capacitor voltage of each sub-module string can be controlled to follow the references, and the MMST can generate 20MW to the load with all the components operating within the ratings. The simulation results proves the feasibility of the topology and the validity of the designed control strategy. The results also show the correspondence of the loss analysis by both Matlab and PLECS.

Chapter 5

Experimental Design of the Two-phase MMST

To verify the feasibility of the two-phase MMST topology and the validity of the designed control strategy in previous chapters, an experimental platform has been built. It comprises a 2kW rated MMST circuit which is tapped in a 7.5kW DC grid emulator, the transducer boards, the control unit and two PCs. The diagram of the experimental circuit is shown in Fig 5.1. The power circuit contains the MMST circuit which operates in the emulated DC grid. It is scaled down from the two-phase MMST design given in the real application as shown in Fig 3.25. The photograph of the whole experimental platform is shown in Fig 5.2.

Fig 5.3 gives the detailed rig photographs of the MMST circuit and the DC grid emulator. The MMST circuit, as shown in Fig 5.3(a), is composed of 16 full-bridge sub-modules, 6 LC blocking branches, and 2 resistive loads to verify the feasibility of the MMST topology. The design procedure is described in Section 5.2. The DC grid emulator, as shown in Fig 5.3(b) and Fig 5.3(c), consists of an AC power source, three isolation transformers and rectifiers, a filtering DC capacitor, and a chopper circuit controlling the DC bus current, which is introduced in Section 5.3. The MMST circuit is tapped in series with the DC grid. The transducer boards and the control

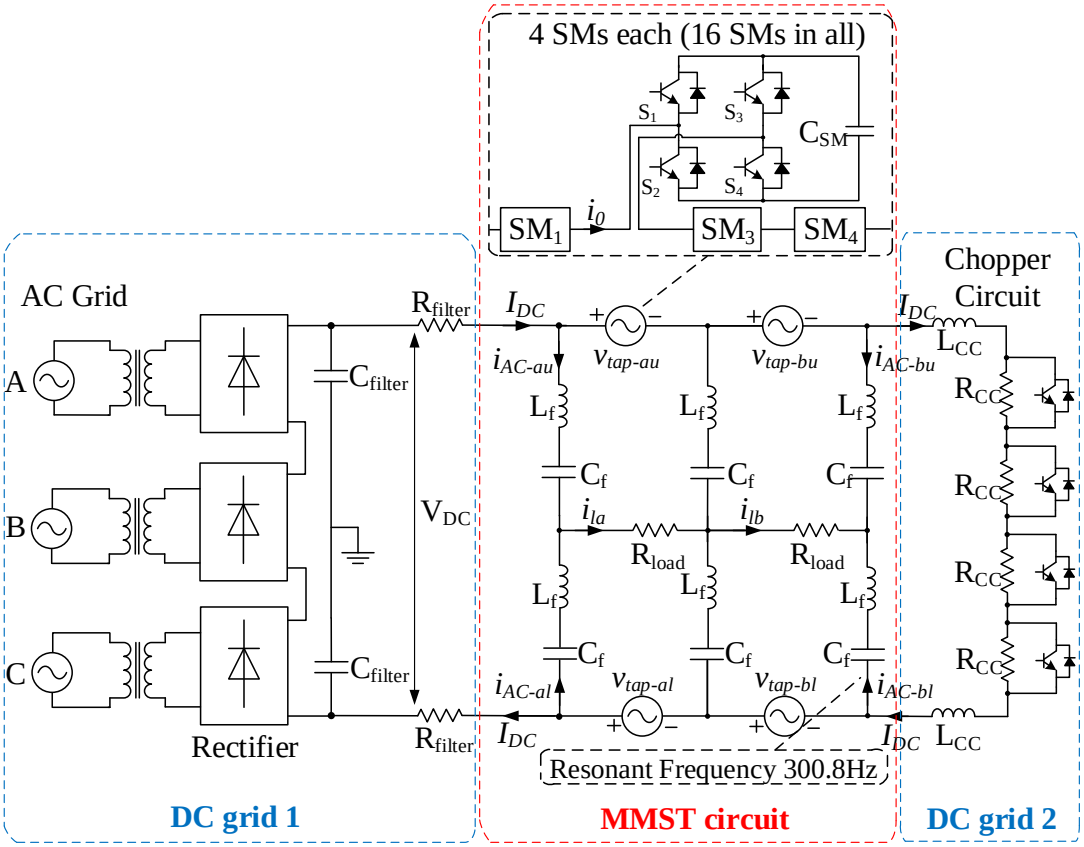


Figure 5.1: The circuit of the experimental platform

unit are described in Appendix E. The transducer boards, presented in Section E.1, sample 18 voltage signals (including 16 sub-module capacitor voltages and 2 DC grid voltages) and 3 current signals (2 load currents and 1 DC grid current) and transmit data to the control unit. The control unit, as described in Section E.2, consists of two DSP boards, 4 FPGA boards and 2 PCs, controlling the MMST circuit and the DC grid emulator individually.

5.1 Basic Parameters in the Experiments

The basic parameters of the experimental platform are listed in Table 5.1. It is a ±325V, 10A DC system with the 2kW rated two-phase MMST circuit tapping inside. The MMST behaves like a sinusoidal current source. The load of the MMST

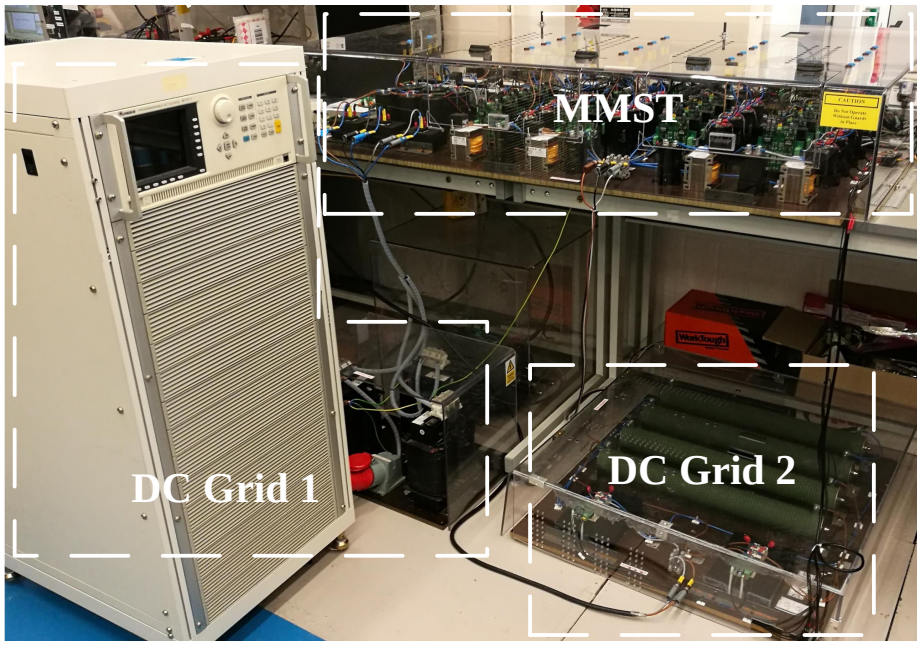


Figure 5.2: The experimental platform of the two-phase MMST

is the second stage of the series tap which is a rectifier load. Using the fundamental mode approximation (FMA) analysis, the MMST load appears as an equivalent resistance [96,97]. So in the experiments the loads of the MMST circuit are replaced by the resistors.

Based on the existing experimental hardware in the PEMC lab, the common number of sub-modules in one arm is four to give a sensible number of the modulation levels to demonstrate multi-level operation and allow simple realisation in the rig. Since each sub-module arm is controlled separately, each arm is operating individually. In addition, assuming all the capacitor voltages are balanced, the inserted sub-module number and the duty cycle are determined by the voltage reference of each arm, which is composed of an AC component and a DC component. Therefore, the AC components of voltage reference for the two arms on one transmission line cannot always counteract exactly, which results in a voltage ripple reflecting to the DC voltage of the chopper circuit, as analysed later in Section 5.4. Thus the lower the sub-module voltage is, the lower the DC voltage ripple is. Considering the sampling precision, the modulation level of the MMST is selected as 60V.

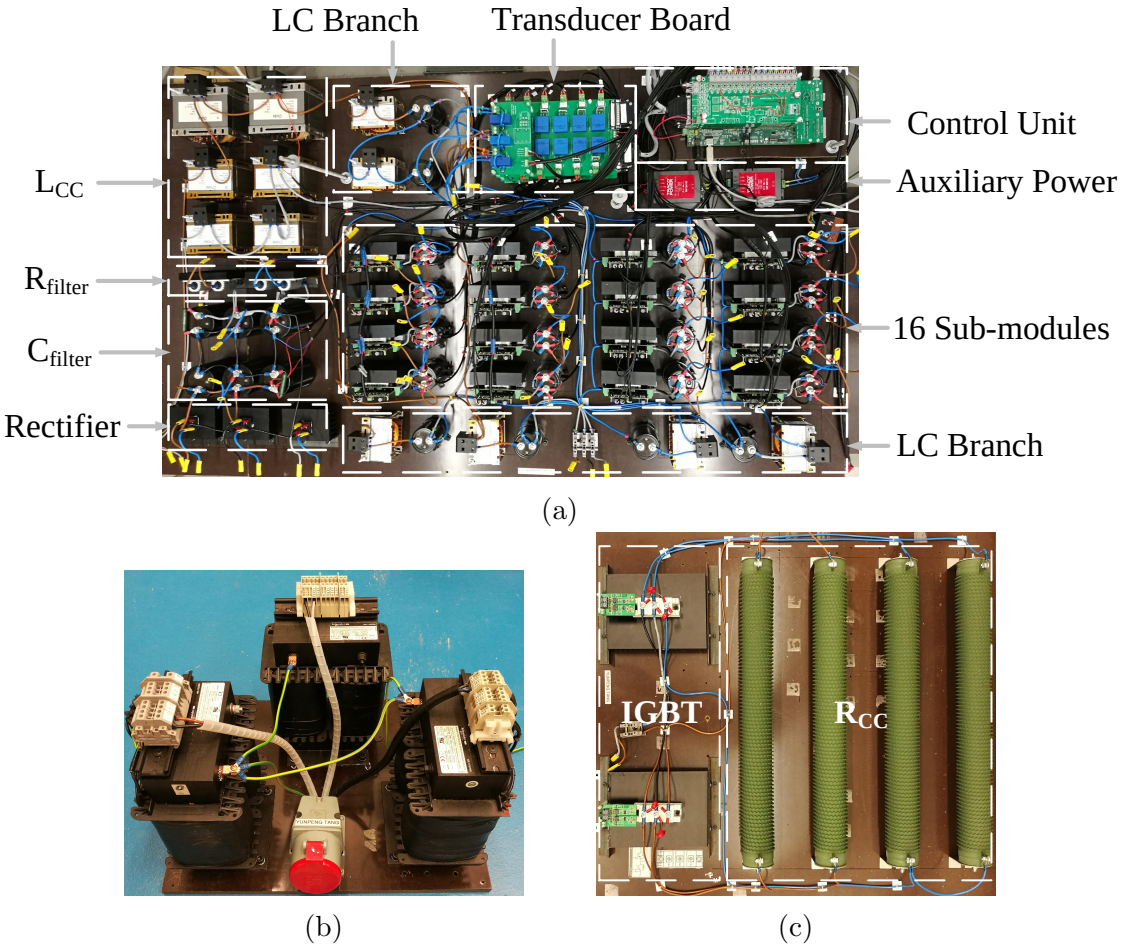


Figure 5.3: The detailed experimental platform. (a) The MMST circuit, (b) The transformer rig, (c) The chopper circuit.

The branch capacitor and inductor of the MMST are selected as 560μF and 0.5mH, respectively. Firstly, for the capacitor voltage rating, the blocking capacitor needs to sustain the 325V DC grid voltage and a relatively small resonant voltage, then the voltage rating of the blocking capacitor is selected as 550V. Secondly, for the values of the branch capacitors and inductors, since the branch impedance is inductive at the fundamental frequency 400Hz for filtering the loop current, a suitable capacitor and inductor value can be obtained based on the resonant frequency and the availability on the market. The resonant frequency of the LC branch is 300Hz. In the rig the AC voltage ripple on the branch capacitor is approximately 7V (2%).

Table 5.1: Parameters of the experiments

Parameter	**Value**
AC grid voltage (v_{ACgrid})	240V (three-phase)
DC Grid Voltage (v_{HVDC})	±325V
DC Current (i_{DC})	10A
System Power (P_{system})	7.5kW
MMST Power	2kW
MMST Arm AC Voltage (v_{AC})	100V
MMST Arm DC Voltage (v_{DC})	50V
MMST Loop Current (i_{AC})	5A
Number of Sub-modules in the MMST (n_{SM})	4 (16 in all)
SM Capacitor in MMST (C_{SM})	1.5mF
MMST Modulation Level (V_C)	60(V)
MMST Operating Frequency	400Hz
Switching Frequency of MMST	12kHz
Load Resistor of MMST (R_{load})	10Ω
MMST Branch Capacitor (C_f)	560μF
MMST Branch Inductor (L_f)	0.5mH
MMST Branch Resistor (R)	0.1Ω
DC Bus Filter Capacitor (C_{filter})	3mF
DC Bus Filter Resistor (R_{filter})	0.24Ω
Switching Frequency of Chopper Circuit (f_{CC})	18kHz
Load Resistor of Chopper Circuit (R_{CC})	22Ω
Inductor of Chopper Circuit (L_{CC})	7.5mH

The switching frequency of the MMST is set to 12kHz. The higher the switching frequency is, the less the observed harmonic distortion will be, and the higher the output power quality is. However, the tested maximum interrupt time running in the DSP is 7.8×10^{-5}s–so the switching period should be longer than one interrupt time. In addition, the switching frequency is selected to be the integral multiple of the fundamental frequency for easier generation of the voltage reference in the DSP code. The final switching frequency is selected to be 12kHz.

5.1.1 Difference of the Parameters between the Experimental and Theoretical Design

The aim of the experiment is to verify the feasibility of the topology design and the control strategy. So the parameters of the two-phase MMST in the experiments, listed in Table 5.1, are scaled down from the parameters designed for real application, listed in Table 3.5, but not with the same ratio due to the requirement of the experimental accuracy.

The comparison of the experimental circuit and the theoretical topology are as follows.

1. The sub-module number in each tap arm of the experimental MMST is 4. In a real application the number would be 20 with two parallel strings. The sub-module number is determined by the maximum voltage on the sub-module arm and the capacitor voltage. Varying these two voltages affects the output power quality of the converter, but lightly influences the fundamental operation. In addition, the parallel sub-module strings in the theoretical design of the MMST act as one tap arm due to the synchronous modulation by the control, as seen in Fig 4.16. Therefore, the tap arm of the experimental MMST which has a single string with four sub-modules is able to represent the tap arm of the MMST topology in the theoretical design.

2. In the experiments the regular sampled PWM method is adopted, while the theoretical simulation uses the naturally sampled PWM method. There are mainly three methods to determine the duty cycle of each switching period, including the naturally sampled PWM, the regular sampled PWM and the direct PWM. In the regular sampled PWM the sampling can be symmetrical or asymmetrical [98]. In the experiments the naturally sampled PWM is difficult to be implemented since the sampling frequency is related to the DSP interrupt frequency which is hard to reach the infinitive naturally sampled frequency. So in the experiments the asymmetrical regular sampled PWM method is applied to keep the modulating accuracy as high as possible.

3. The fundamental frequency in the experiments is 400Hz, while in the theoretical analysis it's 300Hz. Firstly, the variation of the experimental fundamental frequency does not influence the verification of the theoretical design. The frequency range in the theoretical design also includes 400Hz. In addition, as discussed later, the emulated DC grid voltage has a 300Hz ripple, which can result in a 300Hz AC current disturbance on the side blocking branches of the MMST and may affect the control system. Therefore, in the experiments the fundamental frequency is selected differently with 300Hz in order to distinguish the disturbance and analyse its influence to the MMST.

4. The power rating of the experimental MMST is selected as 2kW, 30% of the DC grid power. In a real application the ratio would be 3.3%. The load voltage of the experimental MMST is 100V, 15% of the DC grid voltage. In a real application the ratio would be 1.6%. The sub-module capacitor voltage of the experimental MMST is 60V, 60% of the load voltage. In a real application the ratio would be 20%.

Based on the comparison above, the simulation and experimental results of the experimental two-phase MMST is qualified to justify the feasibility of the n-phase MMST and the validity of the control strategy. The detailed circuit design of the platform is introduced in the following sections.

5.2 Design of the H-bridge Sub-module

The H-bridge sub-module consists of a full-bridge IGBT power module, a gate drive board, an interface board and the heat sink, as shown in Fig 5.4. The IGBT power module is soldered onto the interface board and attached to the heat sink. The design of the sub-module is detailed as follows.

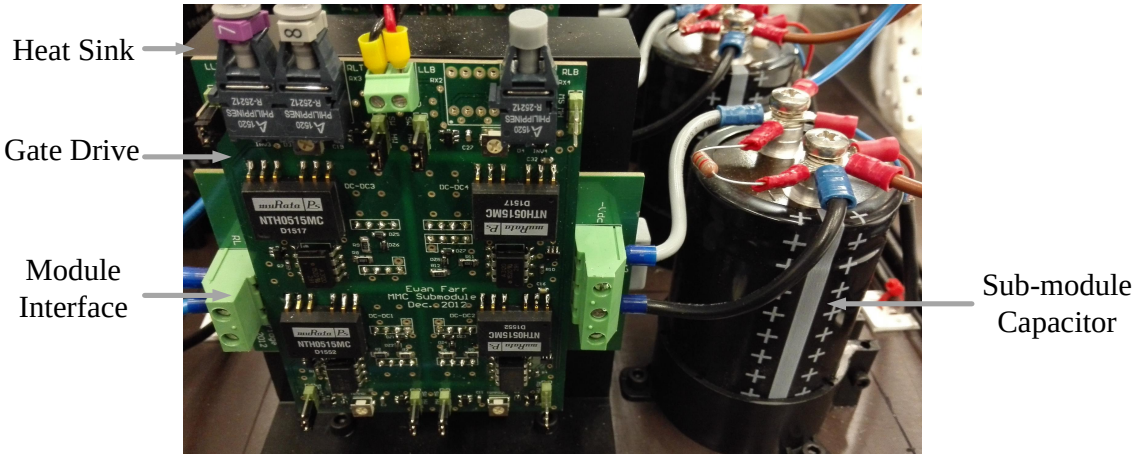


Figure 5.4: The assembled sub-module

5.2.1 IGBT Power Module

In one sub-module there are 4 IGBTs connected in a full-bridge. It is less complex and more cost saving to design the sub-module with one full-bridge IGBT power module rather than two half-bridge modules or four single IGBTs.

From the parameters listed in Table 5.1, the nominal voltage stresses of the IGBTs, which are equal to the sub-module capacitor voltage, are 60V. The peak current flowing through each IGBT is $I_{IGBT-peak} = I_{DC} + \sqrt{2} I_{AC} = 17.1\text{A}$. The current safety margin is set as 2, then the current rating is $I_{IGBT-rated} = 2 \times I_{IGBT-peak} = 34.2\text{A}$.

Thus INFINEON F4-50R06W1E3 IGBT H-bridge Module, 600V 50A, is selected.

5.2.2 IGBT Gate Drive

The IGBT drive signal requires an isolated, ±15V signal with added deadtime, which needs be generated from the gate drive board. The circuit schematic of the IGBT gate drive board is shown in Fig 5.5. The drive signal is received from the optical receiver and then transmitted into the RCD circuit. With the operation of Schmitt trigger, the deadtime of the drive signal can be created by delaying the rising edge of the RCD circuit. Then with the optocoupler and the isolated ±15V power supply,

the drive signal is transferred to an isolated, ±15V signal which is capable of driving the IGBT. The tested output waveforms of one gate drive board are shown in Fig 5.6. The deadtime is approximately 1μs.

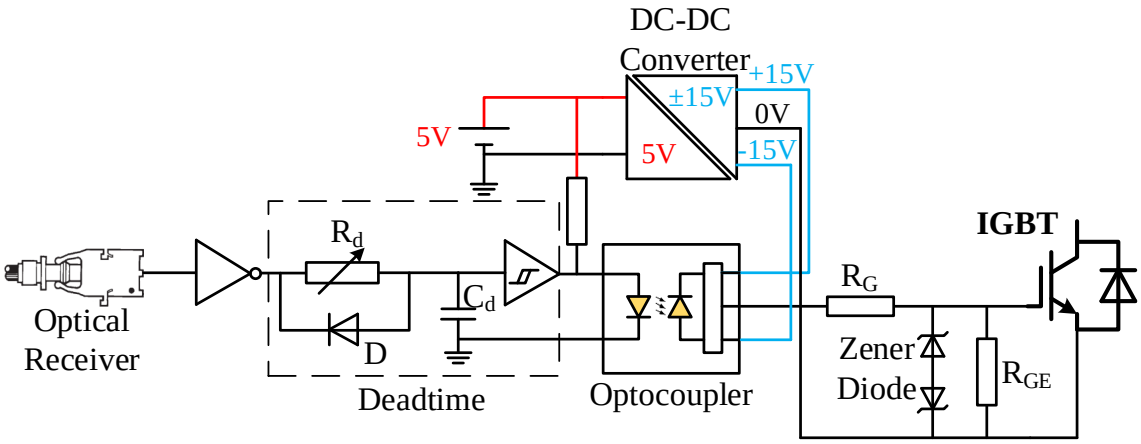
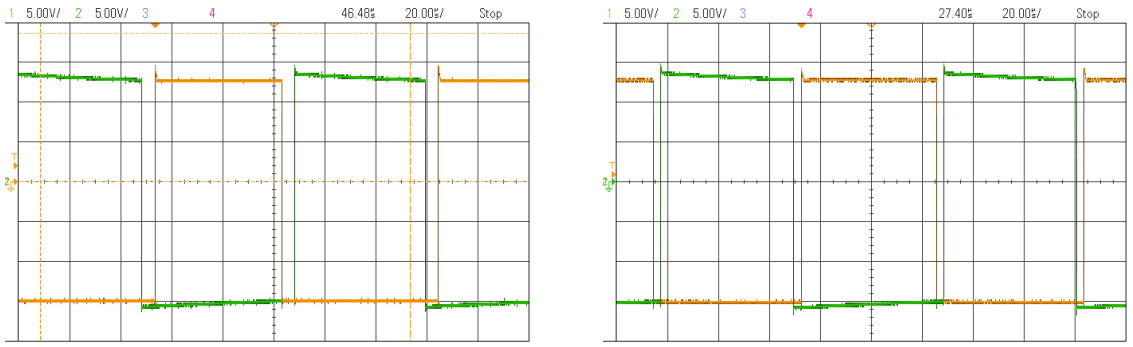


Figure 5.5: Schematic diagram of the gate drive for one IGBT



(a) (b)

Figure 5.6: Tested output waveforms of one gate drive board: (a) Drive signal of S1 and S2, (b) Drive signal of S3 and S4.

5.2.3 IGBT Thermal Design

The heatsink is utilised to keep the IGBT junction temperature in the safe range and protect the IGBTs. To determine the heat-dissipating method and the heatsink parameter, the average power loss of the IGBT power modules is simulated in PLECS software using the same method described in Section 4.5.2. The curves for the

energy losses of the selected F4-50R06W1E3 IGBT module [99] are imported and the simulated average power loss of one IGBT module is $P_{loss-one} = 12\text{W}$. Set a safety margin of 1.2, the power loss is recalculated as $P_{loss-one*} = 14.4\text{W}$.

The thermal resistance of the heat sink can be calculated from the power loss of the IGBT module, the maximum IGBT junction temperature and the thermal resistance of IGBT module. From the datasheet the thermal resistances of the IGBT and diode are listed in Table 5.2 [99]. The average thermal resistance of the IGBT module is

$$R_{th\ J-H} = \frac{0.6 + 0.8}{2} + \frac{0.7 + 0.7}{2} = 1.4°\text{C/W}$$

Table 5.2: Thermal resistances of the IGBT module

Parts	**Junction to case** R_{thJ-C}	**Case to heat sink** R_{thC-H}
IGBT	0.6°C/W	0.7°C/W
Diode	0.8°C/W	0.7°C/W

The maximum junction temperature is $T_j = 80°\text{C}$, the ambient temperature is $T_{air} = 25°\text{C}$. Then the thermal resistance of the heat sink is

$$R_{th\ HS} = \frac{T_j - T_{air}}{P_{loss-one*}} - R_{th\ J-H} = 2.4°\text{C/W}$$

Thus a 1.75°C/W heat sink with air cooling is selected.

5.2.4 Sub-module Capacitor

The sub-module capacitor is utilised to store the energy from the DC grid emulator and output to the AC load. Hence the lower the ripple of the capacitor voltage is, the higher the output AC quality is.

The nominal voltage of the sub-module capacitor is 60V. The voltage ripple is ±5% (Section 3.2). The instantaneous voltage and current of one tap arm are given by

$$v_{tap} = \sqrt{2}V_{AC} \cdot \sin(\omega t) - V_{DC}$$
$$i_{tap} = \sqrt{2}I_{AC} \cdot \sin(\omega t) + I_{DC}$$

The instantaneous energy of one tap arm is $e_{tap} = \int v_{tap} \cdot i_{tap} \mathrm{d}t$. Then the energy change ripple in one period ΔE_{tap} can be obtained. The energy fluctuation reflects to the voltage change on SM capacitors, which is

$$\frac{1}{2} n_{SM} \cdot C_{SM} \cdot [(1-5\%)V_C]^2 + \Delta \mathrm{E_{tap}} = \frac{1}{2} n_{SM} \cdot C_{SM} \cdot [(1+5\%)V_C]^2 \tag{5.1}$$

Then C_{SM} is calculated as 0.85mF. The electrolytic capacitor, 350V 1.5mF, is selected.

5.3 Design of the DC Grid Emulator

To verify the feasibility of the two-phase MMST topology, an emulated DC grid with the constant voltage supply and current flow is necessary for the normal operation of the MMST. The diagram of the DC grid emulator is shown in Fig 5.7.

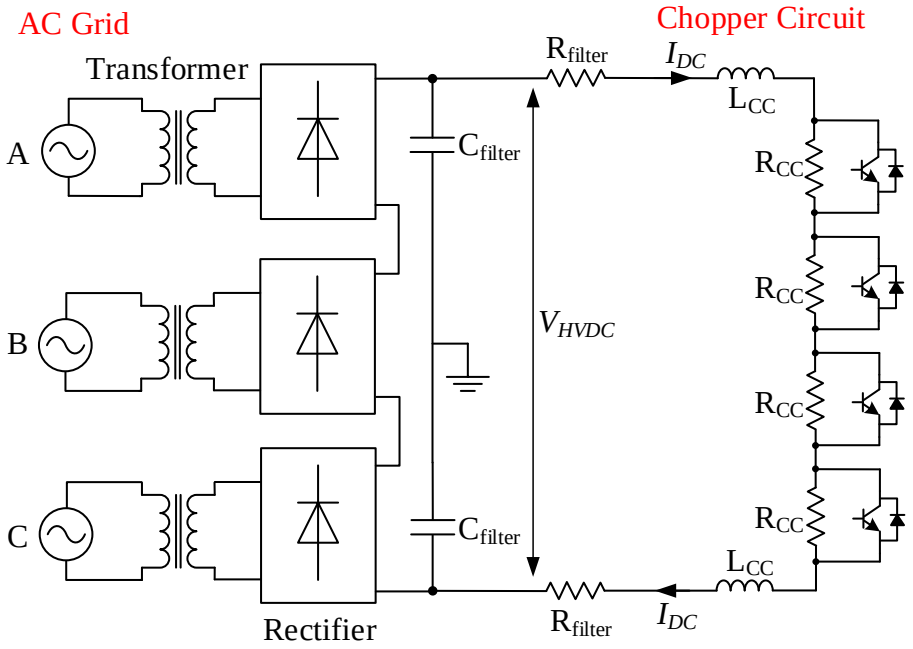


Figure 5.7: Schematic diagram of the DC grid emulator

Since the power of each selected isolation transformer is 2.5kVA, the maximum DC grid power is 7.5kW. The maximum DC bus voltage can be $2\sqrt{2}V_{ACgrid}$=679V as

the grid voltage in the lab is V_{ACgrid}=240V. In the lab experiments it's unrealistic to keep the the MMST power at 1%-10% of the power of the DC grid emulator due to the difficulty of guaranteeing high sampling accuracy, but the ratings of the DC grid emulator are better to be higher in order to make the rig closer to the real system. As a result a higher demand of the DC grid ratings is required. The selected DC grid voltage and power are 650V and 6.5kW, respectively.

In this circuit the power from the AC grid flows through three isolation transformers and is rectified by three rectifiers to create a DC bus. The three-phase 100Hz voltage pulses from the each rectifier are overlaid to a DC voltage with only 6^{th} order harmonic distortion (300Hz) resulting from the series connection of three rectifiers. With the proper design of the filter capacitors the DC bus voltage can be smooth enough for the DC voltage supply. The filter resistors in series with the DC line simulate the cable impedance of the HVDC transmission line and avoid the inrush current during the start-up process of the rig.

The chopper circuit, which is actually a series active load, is applied at the load side of the DC grid to keep the DC current constant. It is composed of 2 inductors, four 22Ω load resistors and four IGBTs. To control the DC grid current, the resistance value of the load connected into the DC grid needs to vary with the DC voltage on the chopper circuit to maintain a certain ratio, i.e. the DC current value. The inductors are adopted to filter the DC current.

The parameter design of the DC grid is described below.

5.3.1 Filter Capacitor on the DC Bus

The filter capacitor is applied to filter the 6^{th} order harmonic from the series rectifiers and maintain the DC bus voltage at a constant. It consists of two capacitors in series for creating a bipolar DC bus.

The maximum operating voltage of the filter capacitor is $V_{HVDC} = 650$V, the voltage ripple on the DC bus is set as ±1%. Based on the principle that the net energy

exchange of the filter capacitor equals to zero in one fundamental period, the energy stored in the capacitor equals to the energy dissipated to the load in one ripple period. Then the equation of filter capacitor calculation is given by

$$\frac{1}{2}C_f \cdot [(1+1\%)V_{HVDC-max}]^2 - \frac{1}{2}C_f \cdot [(1-1\%)V_{HVDC}]^2 = P_{system} \cdot \frac{1}{2 \cdot 300} \quad (5.2)$$

Therefore C_f=1.28mF. The maximum voltage of one capacitor is 325V. Thus 6×500V 1mF electrolytic capacitors are selected. They are configured with three capacitors in parallel and in series with the other three parallel capacitors, so the equivalent capacitor value is 1.5mF.

5.3.2 IGBT Power Module in the Chopper Circuit

One IGBT and one load resistor connected in parallel make up an active load. The resistor is inserted into the DC grid as the load if the IGBT is turned off, otherwise the resistor is short-circuit by the IGBT.

Firstly, in the operating situation that only one load resistor is needed, the parallel IGBT is switching under the 650V DC bus voltage, so the voltage stress of the IGBT is 650V. Secondly, an inrush current may occur during the start-up of the rig due to the chopper circuit inductor, so the current rating is selected to be several times of the 10A steady-state current. The SEMIKRON SKM75GB176D IGBT Module 1.7kV, 80A is selected.

5.3.3 Chopper Circuit Inductor

To improve the quality of the DC grid current, two inductors are connected in series with the load resistors to filter the DC grid current and suppress the current ripple. A rotation method of the load resistors similar with the sorting method of the MMC sub-modules (as explained in Section 2.3) is implemented in order to share the DC grid power and avoid the power dissipation on the certain resistors. With the rotation method, only one resistor is taken in or out in one switching period, which means the

voltage ripple on the inductor is 220V due to 22Ω resistor change and the averaged 10A DC current. Set the DC current ripple as 5% since the lower the DC current ripple is, the closer the DC grid emulator is to the real HVDC system. The DC current ripple is largest when the switching duty cycle is 0.5. Thus the inductor value is given by

$$220 = 2L_{CC}\frac{I_{DC}\cdot 5\%}{0.5\cdot\frac{1}{f_{CC}}} \tag{5.3}$$

Then L_{CC}=6.1mH. Thus the 2.5mH 30A inductor is selected. Three inductors are connected in series to serve as one L_{CC}.

5.4 Analysis and Solution of the Harmonics in the Rig

According to Section 5.1, most of the basic parameters of the experimental MMST have higher ratios than those in the real application, which affects the normal operation and the quality of the output waveforms in the experiments, mainly increasing the harmonics inside the system. For the condition of an MMST operating in a real HVDC transmission line, the cable would have the effects of damping and filtering the harmonics considering it has an LCR model [100]. Therefore, the MMST can be regarded as being connected in the infinite HVDC grid. However, in the experiment the wires are not able to suppress the harmonics in the rig, so the harmonics in the rig need to be focused on.

5.4.1 Harmonics from the MMST to the DC Grid Emulator

Each tap arm is operating individually and the corresponding loop current i_{AC} is modulated and controlled separately. In addition, assuming all the capacitor voltages are balanced, the inserted sub-module number and the duty cycle are determined by the voltage reference of each arm, which is composed of an AC component and a DC component. Therefore, the AC components of modulated tap arm voltages on one

DC line cannot always counteract exactly even in the steady-state operation. As the DC voltage of DC Grid 1 V_{HVDC} is constant, the voltage ripple from four tap arms is reflected to the DC voltage on the chopper circuit, as shown in Fig 5.8. The DC voltage ripple is large enough to disturb the AC currents of the right side branch, which leads to a large current distortion on each loop current, as shown in Fig 5.12.

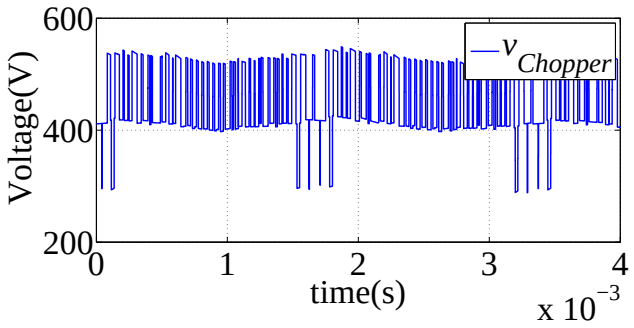


Figure 5.8: Waveform of the DC voltage on the chopper circuit

In the real application, the voltage ripple on the right side of the MMST could be no more than $4V_C$, only 1.3% compared with ±300kV HVDC transmission line, which can be attenuated by the cable impedance. However, in the experimental rig, the ripple can be 240V, 54% compared with 445V average voltage of the chopper circuit. The ripple on the chopper circuit even exceeds the filtering capability of the cable, which is normally 10% of HVDC voltage rating. The large voltage ripple on the chopper circuit affects the AC currents of the right branch too severely to be controlled.

5.4.2 Harmonics from the DC Grid Emulator to the MMST

There are two kinds of harmonics: 300Hz and 800Hz harmonics flowing from the DC Grid 1 to the MMST, as shown in Fig 5.9.

300Hz Harmonic

After rectifying three-phase AC voltage from the rectifiers, the DC voltage on the DC bus has 6^{th} pulses in one fundamental period (50Hz), which the frequency is 300Hz.

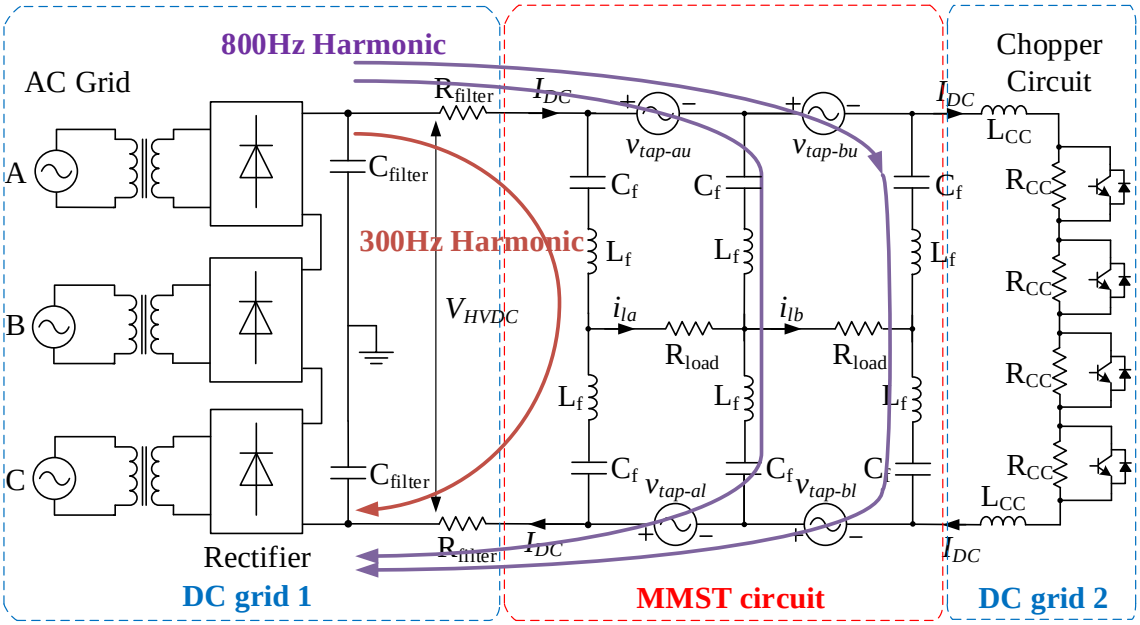


Figure 5.9: Harmonics in the experimental rig

Furthermore, the branch impedance is nearly zero at 300Hz due to the resonance of the branch inductor and capacitor. Therefore, the left branch forms part of the load of the DC bus circuit, of which the impedance is relatively low. Then the 300Hz pulse on the DC bus can generate a 300Hz current on the left side branch. It will influence the loop currents of the left branch which are the controlled values. The reason why the middle and right branches only have a small 300Hz harmonics is that the impedance of these two loops at 300Hz in Fig 5.9 are higher than the left branch loop due to the sub-module capacitance.

800Hz harmonic

Assuming the unity power factor of the MMST system, the voltage and current of the sub-module arm ***au*** are given by (The direction is power outputting direction)

$$\begin{cases} v_{tap-au} = V_{DC} + \hat{V}_{AC} \cdot \sin(\omega t) \\ i_{tap-au} = -I_{DC} + \hat{I}_{AC} \cdot \sin(\omega t) \end{cases} \tag{5.4}$$

Then the instantaneous power of the tap arm ***au*** is given by

$$\begin{aligned} p_{tap-au} &= v_{tap-au} \cdot i_{tap-au} \\ &= -V_{DC} \cdot I_{DC} + \frac{\hat{V}_{AC} \cdot \hat{I}_{AC}}{2} \\ &\quad + \left(V_{DC} \cdot \hat{I}_{AC} - \hat{V}_{AC} \cdot I_{DC}\right) \cdot \sin(\omega t) \\ &\quad - \frac{\hat{V}_{AC} \cdot \hat{I}_{AC}}{2} \cdot \cos(2\omega t) \end{aligned} \tag{5.5}$$

Since there is no net energy exchange in the tap arm ***au*** in one fundamental period, the average DC and AC power is equal, expressed as

$$V_{DC} \cdot I_{DC} = \frac{\hat{V}_{AC} \cdot \hat{I}_{AC}}{2}$$

So the instantaneous power is simplified to be

$$\begin{aligned} p_{tap-au} &= \left(V_{DC} \cdot \hat{I}_{AC} - \hat{V}_{AC} \cdot I_{DC}\right) \cdot \sin(\omega t) \\ &\quad - \frac{\hat{V}_{AC} \cdot \hat{I}_{AC}}{2} \cdot \cos(2\omega t) \end{aligned} \tag{5.6}$$

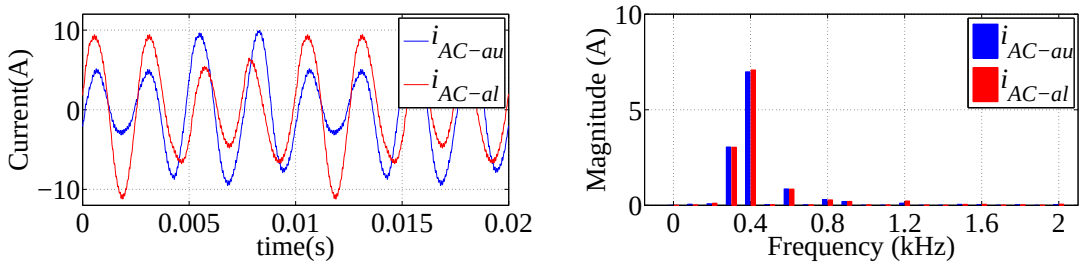
The instantaneous energy stored in the sub-module capacitors is given by

$$\begin{aligned} e_{tap-au} &= \int p_{tap-au} dt + \frac{1}{2} n_{SM} C_{SM} {V^2}_{C-mean} \\ &= \frac{1}{2} n_{SM} C_{SM} {V^2}_{C-mean} \\ &\quad - \frac{V_{DC} \cdot \hat{I}_{AC} - \hat{V}_{AC} \cdot I_{DC}}{\omega} \cdot \cos(\omega t) \\ &\quad + \frac{\hat{V}_{AC} \cdot \hat{I}_{AC}}{2\omega} \cdot \sin(2\omega t) \end{aligned} \tag{5.7}$$

where V_{C-mean} is the averaged capacitor voltage over one fundamental period. The energy stored in sub-module capacitors is related to the capacitor voltage, so according to (5.7), the sub-module capacitor voltage should contain the nominal DC voltage, a 400Hz ripple and a 800Hz ripple. The 800Hz current harmonics on the blocking branches are excited by the 800Hz voltage ripple of the sub-modules [101].

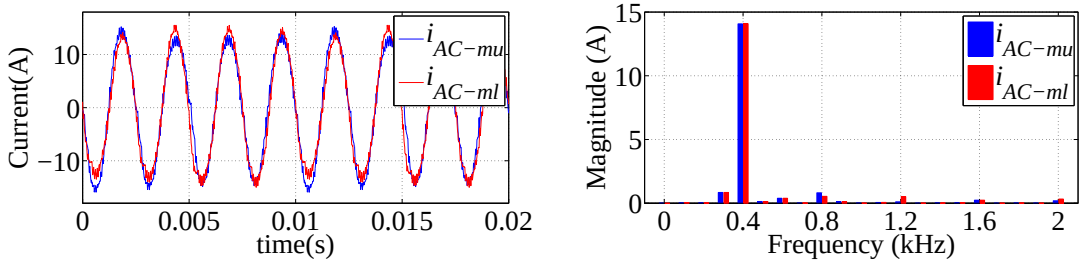
The 300Hz harmonic and 800Hz harmonic can be seen in the waveforms of i_{AC-au} &i_{AC-al} in Fig 5.10, i_{AC-mu} & i_{AC-ml} in Fig 5.11 and i_{AC-bu} & i_{AC-bl} in Fig 5.12.

The 300Hz and 800Hz harmonics in the DC current of DC Grid 1 is the sum of the 300Hz and 800Hz harmonics in three blocking branches, respectively, as shown in Fig 5.13.



(a) (b)

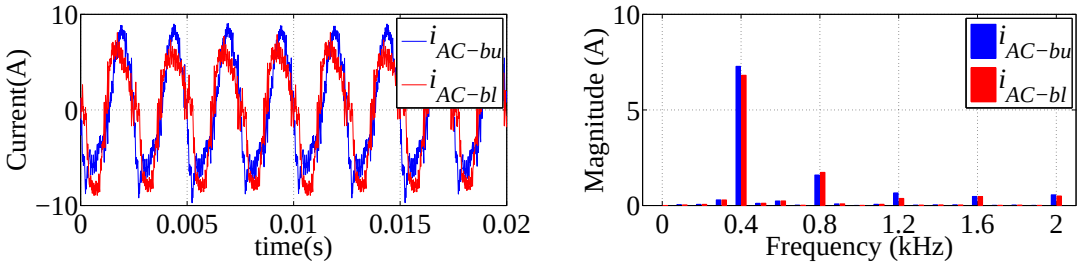
Figure 5.10: Simulation results and the associated spectra of i_{AC-au} & i_{AC-al} (a) Waveforms, (b) The DFT analysis.



(a) (b)

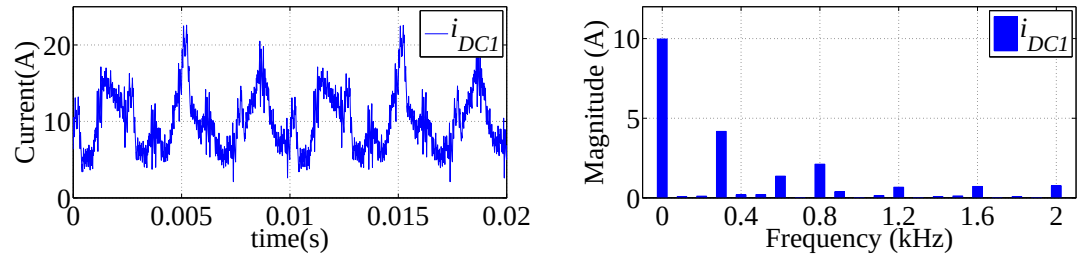
Figure 5.11: Simulation results and the associated spectra of i_{AC-mu} & i_{AC-ml}: (a) Waveforms, (b) The DFT analysis.

While discussing deeper on the real HVDC system, the three-phase LCC is possible to be adopted in the terminals and substations of the HVDC transmission line to sustain the DC voltage. If the MMST is close to the terminals or the substations, there is still the possibility of the existence of harmonics in the branch loops. Therefore a solution of the operation in this case is also proposed and verified in the experiments of the MMST.



(a) (b)

Figure 5.12: Simulation results and the associated spectra of i_{AC-bu} & i_{AC-bl}: (a) Waveforms, (b) The DFT analysis.



(a) (b)

Figure 5.13: Simulation results and the associated spectra of i_{DC1}: (a) The waveform, (b) The DFT analysis.

5.4.3 Solution of the Harmonics

Due to the existence of a DC current disturbance on the right branch generated by the DC voltage ripple on the chopper circuit, as well as the harmonics flowing through the left and right branches from the DC grid, four loop currents have bad qualities to be sampled and controlled. In order to eliminate the effect of the harmonics, the loop currents are calibrated by subtracting the harmonic components. The branch AC currents are recalculated as follows.

Take the calculation of right side branch currents as an example, the current harmonics are expressed as

$$i_{har-b} = \frac{i_{AC-bu} - i_{AC-bl}}{2} \tag{5.8}$$

The calibrated branch AC currents are

$$\begin{cases} i_{AC-bu'} = i_{AC-bu} - i_{har-b} = \frac{i_{AC-bu}+i_{AC-bl}}{2} = \frac{i_{lb}}{2} \\ i_{AC-bl'} = i_{AC-bl} + i_{har-b} = \frac{i_{AC-bu}+i_{AC-bl}}{2} = \frac{i_{lb}}{2} \end{cases} \tag{5.9}$$

Then the branch AC currents can be simplified to be half of the load current. The AC currents of the left side branch can be calibrated in this method as well. Then the sampling of the MMST can also be simplified. Four AC loop currents and four tap arm currents can be recalculated as

$$\begin{cases} i_{AC-au} = i_{AC-al} = \frac{i_{la}}{2} \\ i_{AC-bu} = i_{AC-bl} = \frac{i_{lb}}{2} \\ i_{tap-au} = \frac{i_{la}}{2} + I_{DC} \\ i_{tap-al} = \frac{i_{la}}{2} - I_{DC} \\ i_{tap-bu} = \frac{i_{lb}}{2} + I_{DC} \\ i_{tap-bl} = \frac{i_{lb}}{2} - I_{DC} \end{cases} \tag{5.10}$$

From (5.10), the currents that need to be sampled and controlled can be obtained from i_{la}, i_{lb} and I_{DC}. The control of the load currents doesn't influence the steady-state operation of the MMST. For instance, if the loop currents i_{AC-au} & i_{AC-al} need to be controlled to 5A, the 10A load current i_{la} will return the equivalent values of 5A. In addition, if i_{AC-au} and i_{AC-al} are required to be different values, such as 7A and 3A respectively, the calculation of i_{AC-au} and i_{AC-al} can be adjusted to be $\begin{cases} i_{AC-au} = \frac{7}{10} i_{la} \\ i_{AC-al} = \frac{3}{10} i_{la} \end{cases}$. The main influence of this calibration is on the transient state. For instance, if the loop current i_{AC-au} increases 1A, the feedback from i_{la} is only 0.5A. The control design for the transient state needs to be adjusted.

5.5 Summary

This chapter has considered the overall design of the experimental platform used for verifying the feasibility of the two-phase MMST topology and the validity of the

designed control strategy, including the sub-module design, the emulated DC grid design, the transducer design and the design of other main components. The specifications, procedures and some drawbacks of these design are analysed. Furthermore, the comparison between the experimental design and theoretical design has been considered. In the case of the existence of the 300Hz harmonic from the emulated DC grid and the 800Hz harmonic from the MMST itself in the experimental rig , the solution, which is to sample the load currents instead of the loop currents, are analysed.

The start-up of the platform, the experimental results of MMST circuit, the analysis of the results and the comparison between the experimental and simulation results will be presented in the next chapter.

Chapter 6

Experimental Results of the Two-phase MMST

The experiments for the two-phase MMST have been carried out to verify the feasibility of the n-phase MMST and the validity of the designed control strategy. A 7.5kW experimental rig, consisting of a 7.5kW emulated DC grid and a 2kW two-phase MMST, has been built and introduced in Chapter 5.

In this chapter the start-up, transient-state and the steady-state operation of the experimental rig has been analysed, and a comparison between the experimental results and the corresponding simulation results is demonstrated. The start-up mechanism of the rig, including the anti-windup method and the increasing reference method, is introduced in Section 6.1. The comparison between the experimental results and simulation results of the two-phase MMST under open-loop operation is shown in Section 6.3. The comparison between the experimental and simulation results of the two-phase MMST under closed-loop operation and the transient-state experimental results are given in Section 6.4. The circuit diagram of the experimental platform is shown in Fig 5.1.

6.1 Start-up of the Experimental Rig

Before the experimental rig operates under the full power rating in steady-state conditions, the transient-state case, which is the start-up process, needs to be studied in order to avoid the overshoot and protect the components in the rig. The start-up mechanism of the DC grid and the MMST is explained as follows.

6.1.1 Start-up of the DC Grid Emulator

Based on the design of the chopper circuit in the DC grid emulator described in Section 5.3, assuming the switching frequency of the chopper circuit is infinite, the number of the inserted load resistors $n_{R_{CC}}$ is proportional to the voltage of the chopper circuit $V_{Chopper}$, expressed as

$$n_{R_{CC}} = \frac{V_{Chopper}}{R_{CC} \cdot I_{DC}} \tag{6.1}$$

However, the DC current has the steady-state error when the DC grid is under open-loop operation. Thus, a DC current control loop is integrated into the modulation of the chopper circuit to correct the I_{DC} value in (6.1) and eliminate the steady-state error. The PI regulator of DC current can eliminate the steady-state error, but during start-up the value of the integral term may vary rapidly due to the large transient error of the DC current. Therefore, an anti-windup scheme is applied to prevent integrator wind-up in the PI regulator when it is saturated, as shown in Fig 6.1.

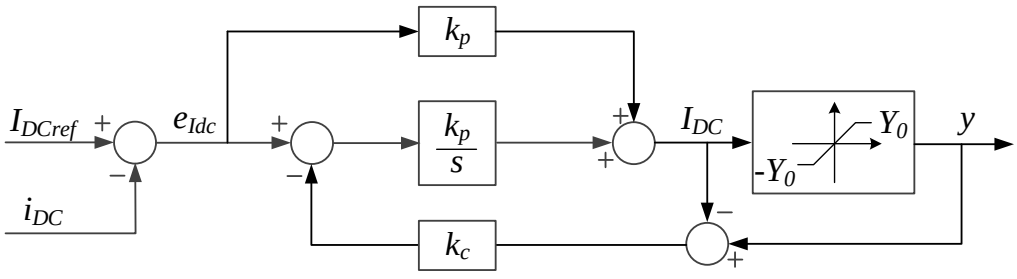


Figure 6.1: Schematic diagram of the PI regulator of the DC current

According to Fig 6.1, a saturation block is added at the output of the PI regulator and the difference between the PI output and the output of the saturation block is fed back into the integral term. The output of the saturation block y is given by (6.2).

$$y = \begin{cases} Y_0 & y_{PI} > Y_0 \\ y_{PI} & -Y_0 \leq y_{PI} \leq Y_0 \\ -Y_0 & y_{PI} < -Y_0 \end{cases} \tag{6.2}$$

When $-Y_0 \leq y_{PI} \leq Y_0$, $y = y_{PI}$ and the PI regulator operates normally. When y exceeds $\pm Y_0$, the difference value of y and $\pm Y_0$ multiplied by the coefficient k_c is fed back to the value of the integral term. With this anti-windup scheme the output from the PI regulator is limited to $\pm Y_0$ and the large overshoot of the DC current during start-up can be prevented.

6.1.2 Start-up of the MMST

It is essential that the sub-module capacitor voltages and branch capacitor voltages of the MMST are charged to a certain value in the start-up process, otherwise there will be a surge current due to the high equivalent capacitance of the sub-module structure [102] and the blocking branches.

There are several pre-charging techniques for the sub-modules on the tap arms. One method is to insert a resistor between the DC grid and the MMST to suppress the inrush current, which is adopted by using R_{filter} in the experiments [103]. Another method is to precharge the sub-module capacitors initially with no output power with the propor control [24]. The sub-module capacitor is able to be precharged only with the control methods [102, 104].

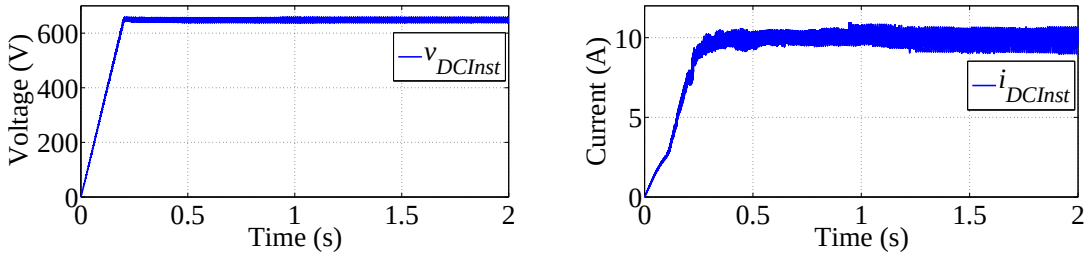
In the experiments a simple and effective precharging method, the increasing reference method, is applied. All the references, including the sub-module capacitor voltage reference, the DC grid current reference and the MMST load current reference, are gradually increased at the same rate and proportion of the DC grid voltage

variation. This means that the rig operates from low ratings to high ratings during the start-up process and the capacitors can be gradually charged from the DC grid energy. The increasing reference method avoids the need for complicated control for capacitor charging, removes the step change in the transient state which may lead to the inrush current, and improves the system reliability.

6.1.3 Simulation Results of the Start-up of the Experimental Rig

The simulation of the start-up of the experimental rig with the anti-windup method of the DC grid emulator and the increasing reference method of the MMST has been carried out. The simulation results are shown below.

Fig 6.2 shows the waveforms of the DC voltage v_{DC} and current i_{DC} of the DC grid emulator. The instantaneous DC voltage, shown in Fig 6.2(a), increases from 0V to 650V within 0.2s linearly, and all the references follow the variation of the DC voltage, i.e. change from 0 to the steady-state values within 0.2s linearly. Fig 6.2(b) indicates that the instantaneous current of the DC grid, of which the reference varies from 0A to 10A within 0.2s linearly, can be controlled to 10A and has no inrush current with the PI regulator and the anti-windup method.

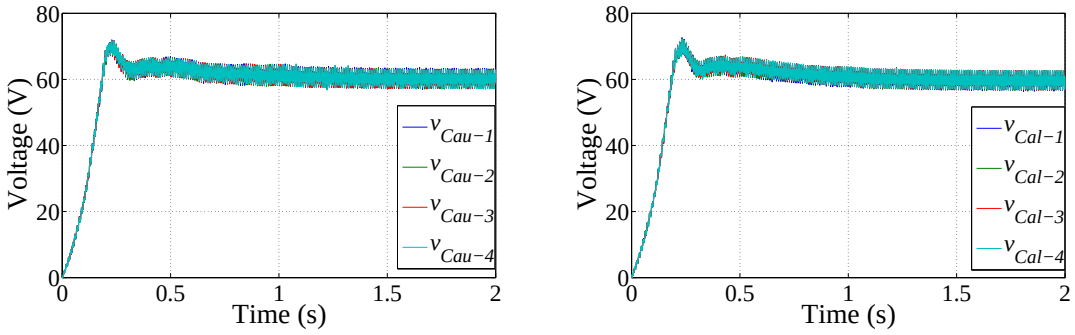


(a) (b)

Figure 6.2: Waveforms of start-up process of the DC grid emulator: (a) Waveform of v_{DC}, (b) Waveform of i_{DC}.

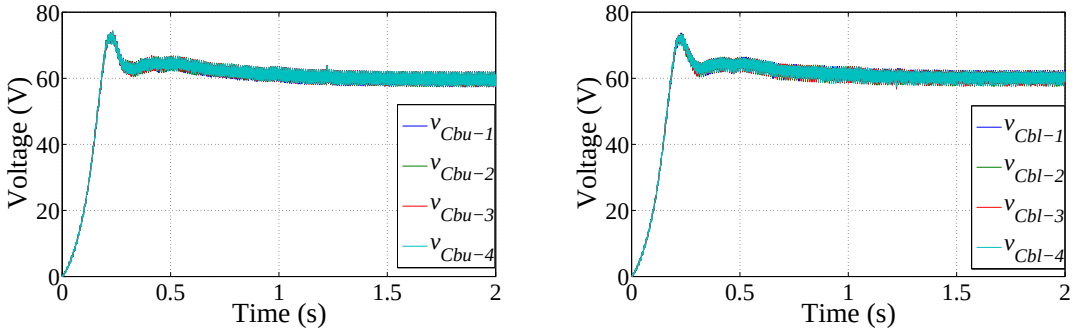
Fig 6.3 and Fig 6.4 demonstrates the sub-module capacitor voltages of four tap arms in the transient state. The voltage reference increases from 0V to 60V within 0.2s

linearly. With the mean capacitor voltage control loop implemented, the capacitor voltages of the tap arm ***au*** v_{Cau} in Fig 6.3(a), arm ***al*** v_{Cal} in Fig 6.3(b), arm ***bu*** v_{Cbu} in Fig 6.4(a) and arm ***bl*** v_{Cbl} in Fig 6.4(b) increase gradually and a maximum 12V overshoot (20%) is observed on each capacitor voltage even when the DC grid voltage rises sharply.



(a) (b)

Figure 6.3: Waveforms of sub-module capacitor voltages in Phase A of the MMST during the start-up process: (a) Waveform of v_{Cau}, (b) Waveform of v_{Cal}.



(a) (b)

Figure 6.4: Waveforms of sub-module capacitor voltages in Phase B of the MMST during the start-up process: (a) Waveform of v_{Cbu}, (b) Waveform of v_{Cbl}.

The voltages of branch capacitors in the 6 LC blocking branches are shown in Fig 6.5. The upper and lower blocking capacitors in the left branches, named as $v_{Cblock-au}$ and $v_{Cblock-al}$ respectively, have the average voltages of $\frac{V_{HVDC}}{2} = 325$V. The upper and lower blocking capacitors in the middle branches, named as $v_{Cblock-mu}$ and $v_{Cblock-ml}$

respectively, have the average voltages of $\frac{V_{HVDC}-2V_{DC}}{2} = 275$V. The upper and lower blocking capacitors in the right branches, named as $v_{Cblock-bu}$ and $v_{Cblock-bl}$ respectively, have the average voltages of $\frac{V_{HVDC}-4V_{DC}}{2} = 225$V. The waveforms of top, middle and bottom curves are $v_{Cblock-au}$ & $v_{Cblock-al}$, $v_{Cblock-mu}$ & $v_{Cblock-ml}$ and $v_{Cblock-bu}$ & $v_{Cblock-bl}$, respectively. The AC voltages of the capacitors on the middle branch are twice that of the left and right branches as the AC currents are doubled. From Fig 6.5 it is clear that the branch capacitors are charged gradually with the increase of the DC grid voltage, and the overshoot of the capacitor voltages are too small to influence the normal operation of the MMST.

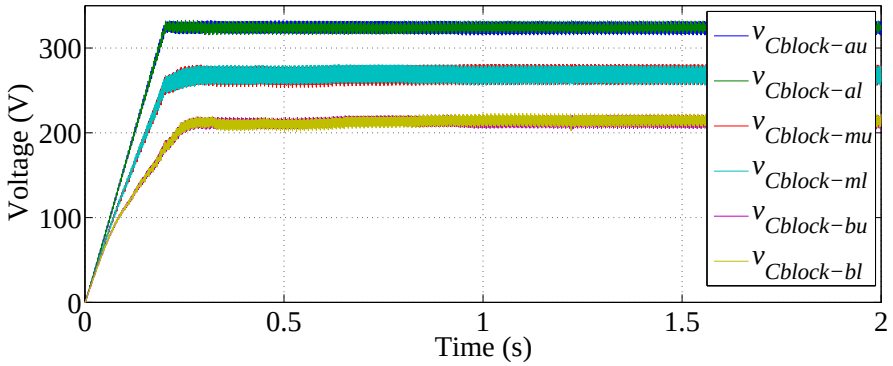


Figure 6.5: Waveforms of the capacitor voltages of blocking branches of the MMST during the start-up process (Top curves: $v_{Cblock-au}$ & $v_{Cblock-al}$; middle curves: $v_{Cblock-mu}$ & $v_{Cblock-ml}$; bottom curves: $v_{Cblock-bu}$ & $v_{Cblock-bl}$).

In conclusion, the start-up of the rig, with the implementation of anti-windup method of the DC grid emulator and the increasing reference method of the MMST, can charge the capacitors in the MMST with relatively low overshoot voltages, avoid the inrush DC grid current and ensure the normal operation of the rig during the transient state. The experimental rig can enter into steady-state operation after 1.5s. The results of the DC grid emulator and the two-phase MMST in the steady-state operation are shown as follows.

6.2 Experimental Results of the DC Grid Emulator and the Comparison with Simulation Results

The emulated DC grid is to provide an operating situation to the MMST in the lab experiments. The steady-state operation of the DC grid with the anti-windup method has been described in Section 6.1. The experimental and simulation results of the DC grid in the steady-state operation, with the MMST operating in the closed-loop condition at the same time, are shown in Fig 6.6 and Fig 6.7.

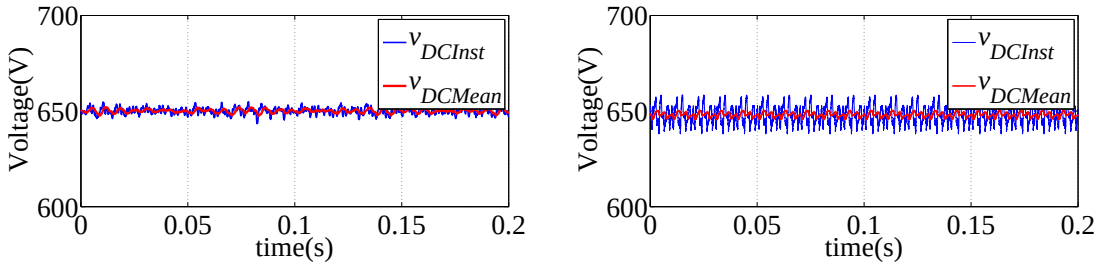


Figure 6.6: **Closed-loop experimental and simulation results** of the emulated DC grid voltage v_{HVDC}: (a) Experimental results of v_{HVDC}, (b) Simulation results of v_{HVDC}.

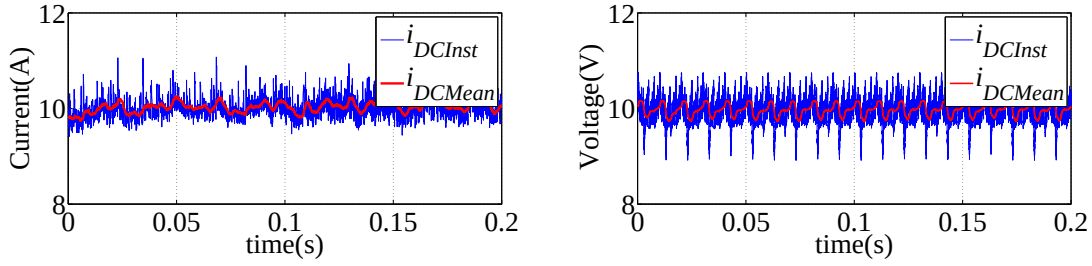


Figure 6.7: **Closed-loop experimental and simulation results** of the emulated DC grid current i_{DC}: (a) Experimental results of i_{DC}, (b) Simulation results of i_{DC}.

It can be seen from Fig 6.6 that the DC voltage reaches the required value of 650V both in the experiments and the simulation. From Fig 6.7 it's clear that the DC

current is controlled to 10A by the PI regulator introduced in Fig 6.1. In addition, the ripple on the DC voltage and current in the experiments are less than those in the simulation due to the damping and the equivalent resistance in the experimental rig.

The experiments for verifying the dynamic response of DC current control are also carried out. The experimental results with the DC current reference changing from 8A to 10A at 0.2s are shown in Fig 6.8. The DC grid enters into the steady state within 0.3s.

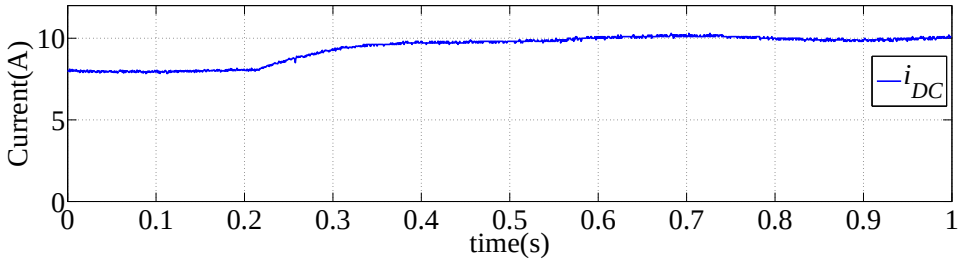


Figure 6.8: Waveforms of the DC current

6.3 Experimental Results of the Two-phase MMST under Open-loop Operation and the Comparison with Simulation Results

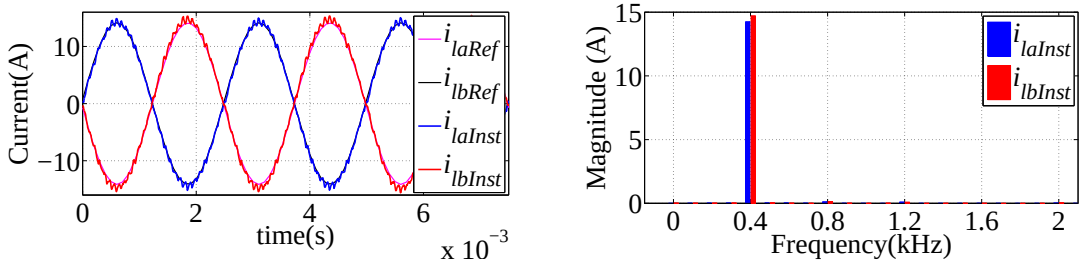
To verify the feasibility of the n-phase MMST, the experiments of the two-phase MMST with the parameters listed in Table 5.1 under open-loop operation have been carried out, and the comparison with the simulation results has been analysed as follows.

6.3.1 Open-loop Results of the Load Currents

The experimental and simulation results of the load currents i_{la} & i_{lb} under open-loop operation, and the corresponding DFT analyses, are shown in Fig 6.9 and Fig 6.10, respectively.

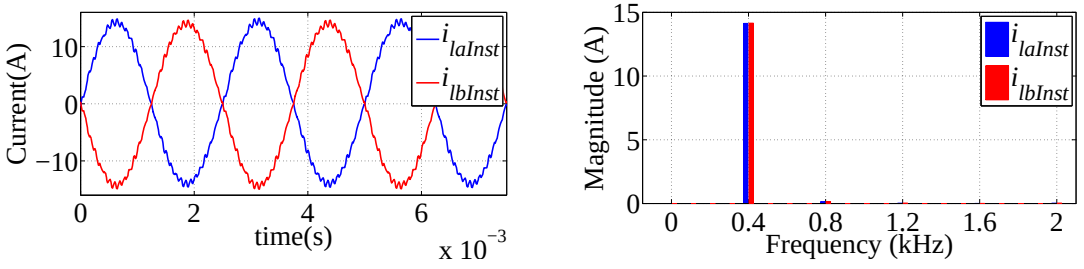
It can be found from Fig 6.9 and Fig 6.10 that

- The frequencies of the load currents are 400Hz and the phase difference of i_{la} & i_{lb} is 180°.
- The load currents almost follow the references but a tracking error exists due to the open-loop operation. The DFT analyses of the load currents show that the RMS values of i_{la} & i_{lb} are 10.04A and 10.36A because higher voltages of the sub-module capacitors lead to higher load voltages although the MMST input power in partly consumed by the losses in the rig. As the loads are resistors the load voltages are not sampled.
- The total harmonic distortion (THD) of i_{la} & i_{lb} are both 3.3%, which indicates a good output power quality of the modular multilevel structure.
- The simulation results in Fig 6.10 are quite similar with the experimental results, which proves the validity of both of them.



(a) (b)

Figure 6.9: **Open-loop experimental results** and the associated spectra of the load currents i_{la} & i_{lb}: (a) Waveforms, (b) The DFT analysis.

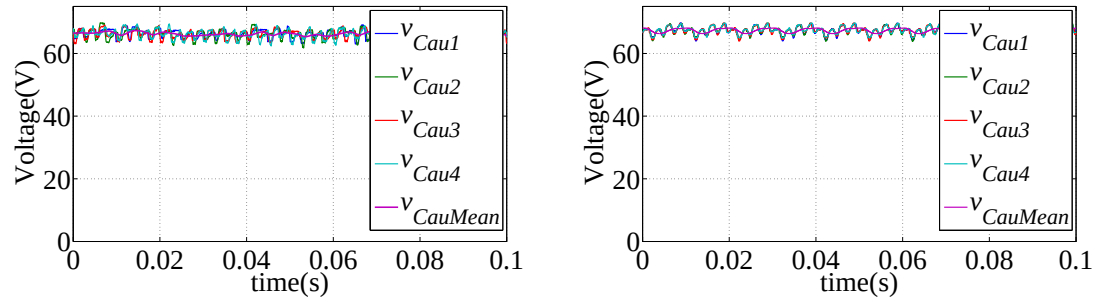


(a) (b)

Figure 6.10: **Open-loop simulation results** and the associated spectra of the load currents i_{la} & i_{lb}: (a) Waveforms, (b) The DFT analysis.

6.3.2 Open-loop Results of the Sub-module Capacitor Voltages

The experimental and simulation results of capacitor voltages and the mean voltages of the tap arms ***au***, ***al***, ***bu*** and ***bl*** in the open-loop situation are shown in Fig 6.11, Fig 6.12, Fig 6.13 and Fig 6.14, respectively.

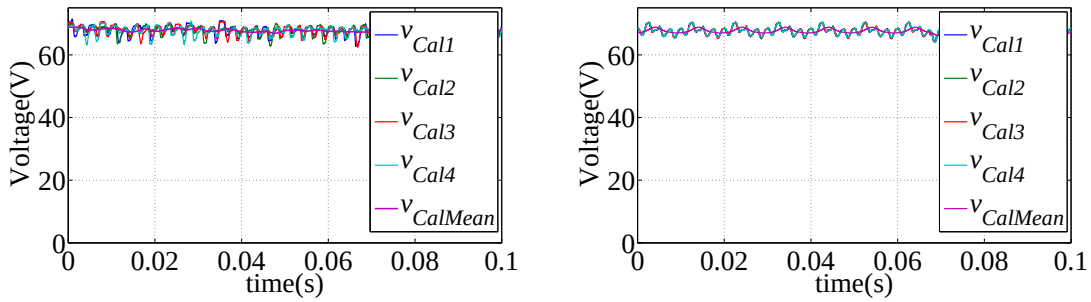


(a) (b)

Figure 6.11: **Open-loop experimental and simulation results** of capacitor voltages v_{Cau} of the tap arm ***au***: (a) Experimental results, (b) Simulation results.

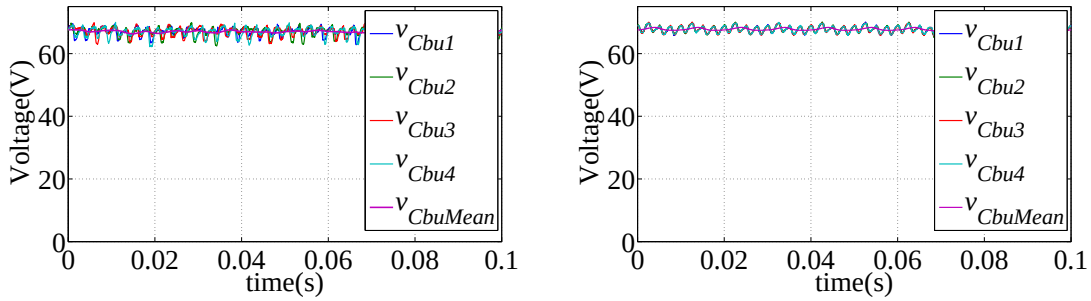
From Fig 6.11 to Fig 6.14 it can be seen that

- The capacitor voltages of each arm can be naturally balanced only with the rotation method described in Section 4.3 and no specific control loops are required for balancing. The mean capacitor voltages of the tap arms ***au***, ***al***, ***bu*** and ***bl*** are 67.4V, 68.0V, 67.3V and 67.9V respectively. It is clear that there



(a) (b)

Figure 6.12: **Open-loop experimental and simulation results** of capacitor voltages v_{Cal} of the tap arm ***al***: (a) Experimental results, (b) Simulation results.

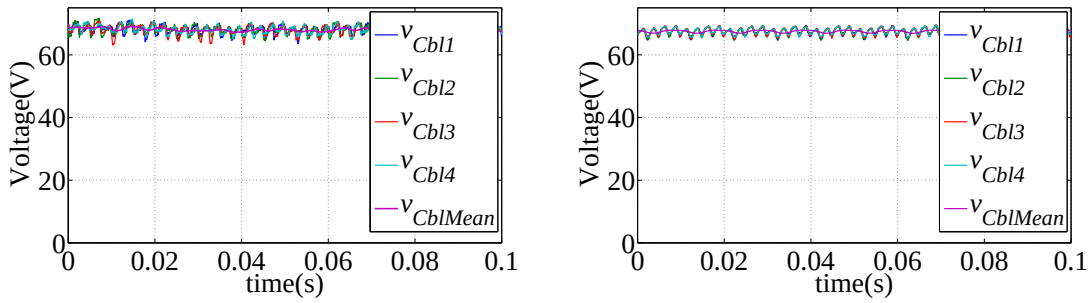


(a) (b)

Figure 6.13: **Open-loop experimental and simulation results** of capacitor voltages v_{Cbu} of the tap arm ***bu***: (a) Experimental results, (b) Simulation results.

are errors when compared with the reference value of 60V. The mean voltages of four tap arms in the simulation are close to those in the experiments.

- The 400Hz ripple on the capacitor voltages results from the fundamental AC current which charges and discharges the capacitors. The average voltage ripple of all the capacitors is 8V, ±6% of the mean capacitor voltage, which is similar to the 6V ripple (±4.5%) found in the simulation. The ripple in the experiments and the simulation is larger than the ±5% ripple in theory in that the switching frequency of the MMST is not high enough to guarantee a high balancing speed when the modulation wave is near the peak values.



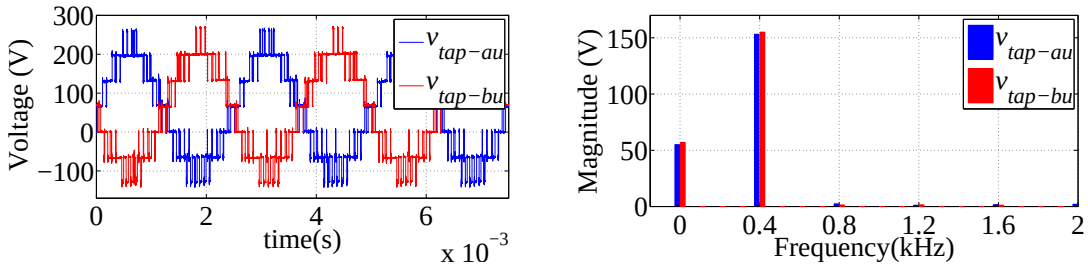
(a) (b)

Figure 6.14: **Open-loop experimental and simulation results** of capacitor voltages v_{Cbl} of the tap arm ***bl***: (a) Experimental results, (b) Simulation results.

6.3.3 Open-loop Results of the Tap Arm Voltages and Currents

Open-loop Results of Upper Tap Arm Voltages

The experimental and simulation results of the voltages v_{tap-au} & v_{tap-bu} of tap arms ***au*** and ***bu*** under open-loop operation are shown in Fig 6.15 and Fig 6.16 respectively.

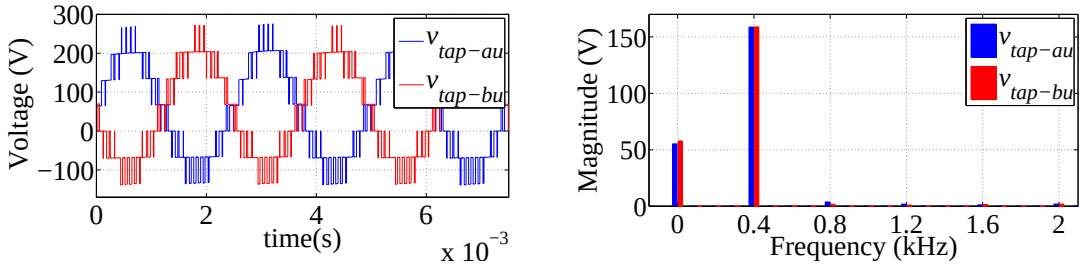


(a) (b)

Figure 6.15: **Open-loop experimental results** and the associated spectra of the voltages v_{tap-au} & v_{tap-bu} of tap arms ***au*** and ***bu***: (a) Waveforms, (b) The DFT analysis.

From Fig 6.15 and Fig 6.16 it can be found that

- The tap arm voltages v_{tap-au} & v_{tap-bu} consist of DC components and AC components. The DC bias voltages of v_{tap-au} & v_{tap-bu} are 54.9V and 56.9V



(a) (b)

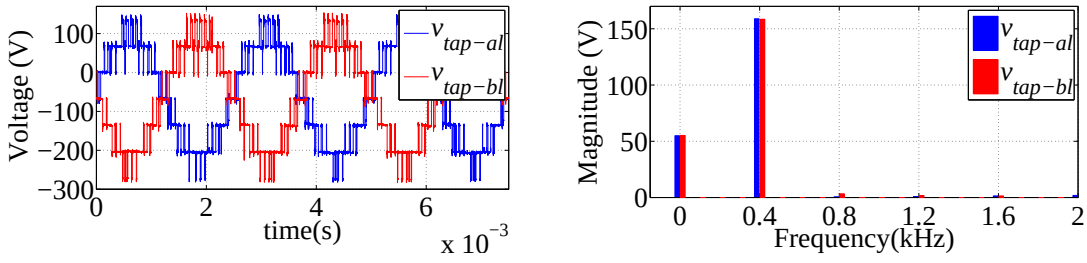
Figure 6.16: **Open-loop simulation results** and the associated spectra of the voltages v_{tap-au} & v_{tap-bu} of tap arms ***au*** and ***bu***: (a) Waveforms, (b) The DFT analysis.

respectively, which are higher than the reference value of 50V. The RMS AC voltages of v_{tap-au} & v_{tap-bu} are 108.3V and 109.6V respectively, which are higher than the reference value of 100V. This is because the capacitor voltages are higher than the reference value under open-loop operation.

- The tap voltage waveforms from the experiments have several spikes in one fundamental period, which may occur only at the start of the switching period. This is because, for instance, the number of the inserted sub-modules is unchanged at 3, then there may be no sub-module switching on or off, or may be one sub-module switching on and one sub-module switching off based on the rotation method. Therefore in the second circumstance the sub-module number drops to 2 and jumps back to 3 very shortly because of the dead time of the IGBTs. The dead time for the rig is 1μs, so the one sub-module is switched off at 1μs before the start of the switching period and the other one is switched on at 1μs after. Therefore the spike is approximately 2μs. In the simulation the spike won't appear due to the zero dead time required for ideal switches.

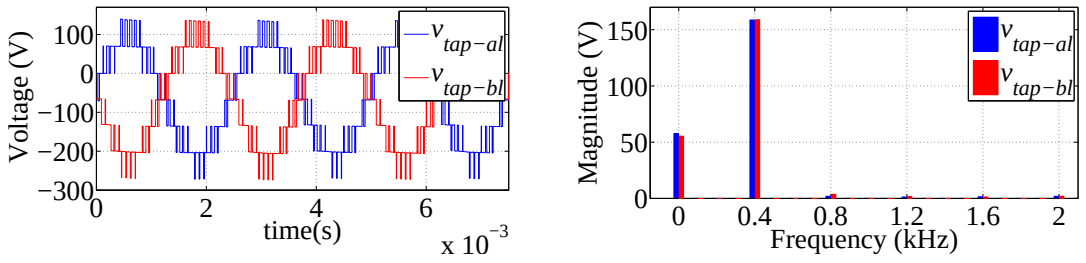
Open-loop Results of Lower Tap Arm Voltages

The experimental and simulation results of the voltages v_{tap-al} & v_{tap-bl} of the tap arms ***al*** and ***bl*** under open-loop operation are shown in Fig 6.17 and Fig 6.18 respectively.



(a) (b)

Figure 6.17: **Open-loop experimental results** and the associated spectra of the voltages v_{tap-al} & v_{tap-bl} of tap arms ***al*** and ***bl***: (a) Waveforms, (b) The DFT analysis.



(a) (b)

Figure 6.18: **Open-loop simulation results** and the associated spectra of the voltages v_{tap-al} & v_{tap-bl} of tap arms ***al*** and ***bl***: (a) Waveforms, (b) The DFT analysis.

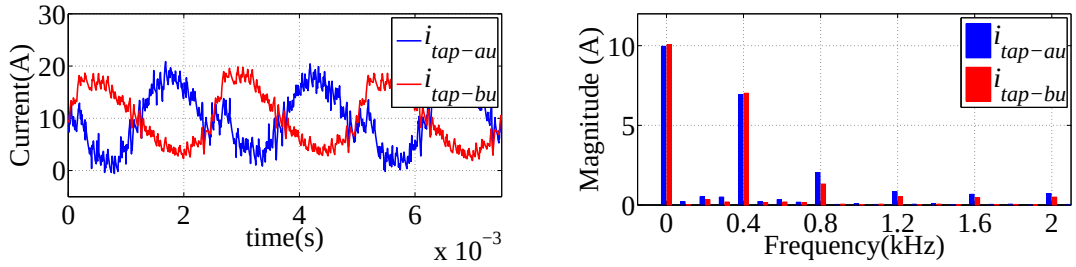
From Fig 6.17 and Fig 6.18 it can be seen that the tap arm voltages v_{tap-al} & v_{tap-bl} also consist of the DC components and AC components. The DC bias voltages of v_{tap-al} & v_{tap-bl} are 55.0V and 55.2V respectively. The RMS AC voltages of v_{tap-au} & v_{tap-bu} are 112.4V and 112.0V respectively. The AC and DC components of v_{tap-al} & v_{tap-bl} are higher than the reference values since the sub-module capacitor voltages are higher than the reference value. The simulation results in Fig 6.16 and Fig 6.18 are very similar to the experimental results shown in Fig 6.15 and Fig 6.17, which indicates that the simulation results are correct and the experimental rig is operating normally.

Open-loop Results of Upper Tap Arm Currents

The experimental and simulation results of the currents i_{tap-au} & i_{tap-bu} of tap arms

au and ***bu*** under open-loop operation are shown in Fig 6.19 and Fig 6.20 respectively.

It can be concluded from Fig 6.19 and Fig 6.20 that the tap arm currents i_{tap-au} & i_{tap-bu} both consist of the DC components and the AC components. The DC components are the 10A DC grid current. The AC components include the fundamental loop currents (which have a 180° phase shift with each other and the RMS values are approximately 5A) and the 800Hz harmonics. Based on the harmonic analysis of the experimental rig in Section 5.4, there are nearly no 300Hz harmonics in i_{tap-au} & i_{tap-bu}, and the 800Hz harmonics can be observed. In addition, comparing Fig 6.19 and Fig 6.20, the waveforms and the component magnitudes of i_{tap-au} & i_{tap-bu} in the experiments and the simulation are very close, proving that both of the results are correct. The waveforms for i_{tap-al} & i_{tap-bl} of the tap arms ***al*** and ***bl*** are not given but show similar results.

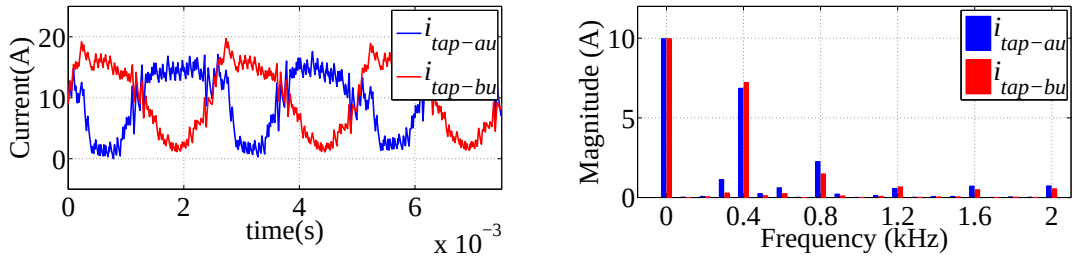


(a) (b)

Figure 6.19: **Open-loop experimental results** and the associated spectra of the currents i_{tap-au} & i_{tap-bu} of tap arms ***au*** and ***bu***: (a) Waveforms, (b) The DFT analysis.

6.4 Experimental Results of the Two-phase MMST under Closed-loop Operation and the Comparison with Simulation Results

To verify the validity of the control strategy of the n-phase MMST introduced in Chapter 4, the experiments of the two-phase MMST under closed-loop operation



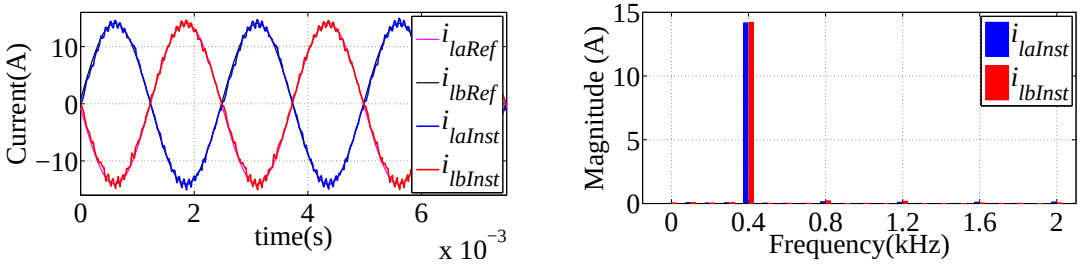
(a) (b)

Figure 6.20: **Open-loop simulation results** and the associated spectra of the currents i_{tap-au} & i_{tap-bu} of tap arms ***au*** and ***bu***: (a) Waveforms, (b) The DFT analysis.

with the modified sampling method from Section 5.4 have been carried out. And the comparison with the simulation results has been analysed.

6.4.1 Closed-loop Results of the Load Currents

The experimental and simulation results of the load currents i_{la} & i_{lb} under closed-loop operation are shown in Fig 6.21 and Fig 6.22 respectively.

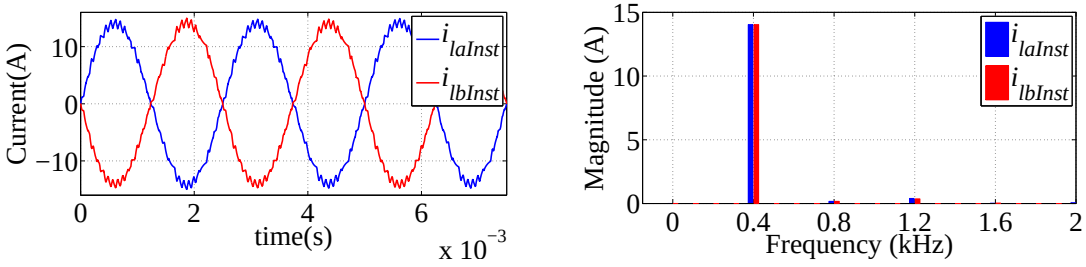


(a) (b)

Figure 6.21: **Closed-loop experimental results** and the associated spectra of the load currents i_{la} & i_{lb}: (a) Waveforms, (b) The DFT analysis.

It can be found from Fig 6.21 and Fig 6.22 that

- Comparing between Fig 6.9 and Fig 6.21, the instantaneous load currents i_{laInst} & i_{lbInst} of the MMST follow the references i_{laRef} & i_{lbRef} perfectly under closed-loop operation and that the steady-state errors are eliminated.



(a) (b)

Figure 6.22: **Closed-loop simulation results** and the associated spectra of the load currents i_{la} & i_{lb}: (a) Waveforms, (b) The DFT analysis.

- The frequencies of the load currents are 400Hz and the phase difference between i_{la} & i_{lb} is 180°.
- From the DFT analyses of the load currents in Fig 6.21(b), the RMS values of i_{la} & i_{lb} are both 10A. The THD of i_{la} & i_{lb} are 3.7% and 4.0% respectively, lower than the open-loop output quality due to lower magnitudes of the fundamental waves.
- The load current waveforms and the DFT results indicate that the inner current control loops are operating correctly.
- The experimental results in Fig 6.21 and the simulation results in Fig 6.22 are nearly identical, which proves the validity of these results.

The experiments for verifying the dynamic response of the loop current control are also carried out. In the experiments the time constant of the PR regulator τ_{PR} is set to be 5ms which gives the coefficients of the PR regulator as $k_{p-I_{ac}}$=0.3 and $k_{r-I_{ac}}$=30 based on the analysis in Section 4.2 and the experimental parameters listed in Table 5.1.

Fig 6.23 shows the waveforms of the load currents with the current reference varying from 4A to 5A at 0.04s. The settling time of the transient response for the second-order system is approximately 43ms with a 2% criterion. Therefore the time constant of the inner current control loop from the experimental results is $\tau_{PR} = \frac{47}{4}$=10.8ms, which is twice of the designed τ_{PR}. The time constant in the experiments is accept-

able due to a possible higher branch resistance in the rig.

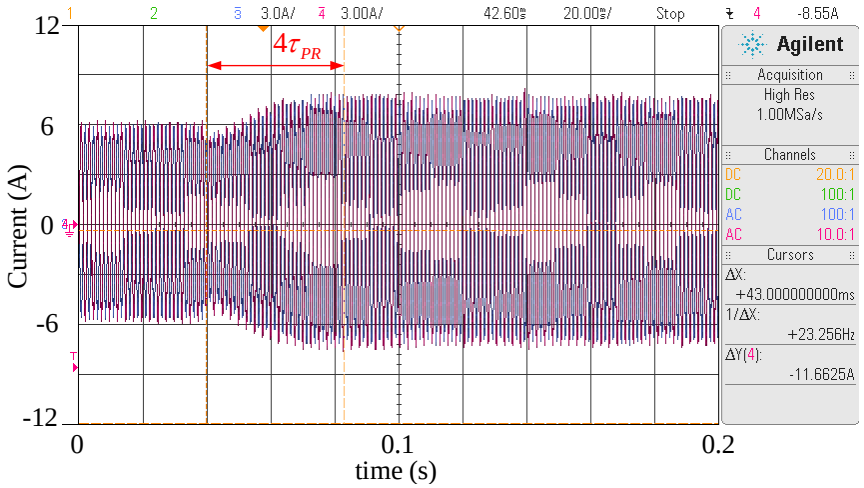
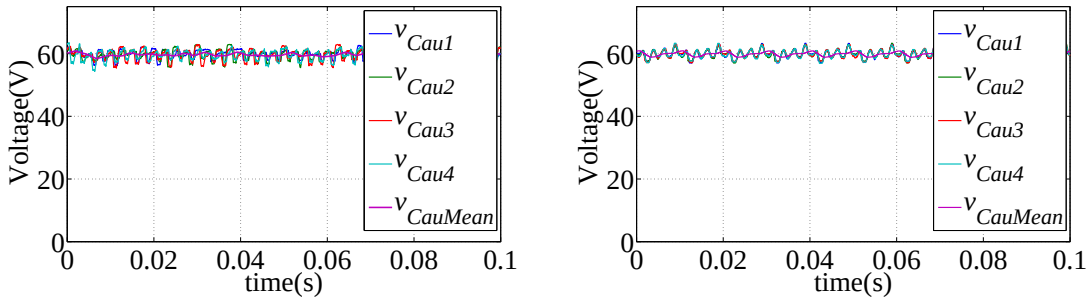


Figure 6.23: Waveforms of the load currents in the transient state

6.4.2 Closed-loop Results of the Sub-module Capacitor Voltages

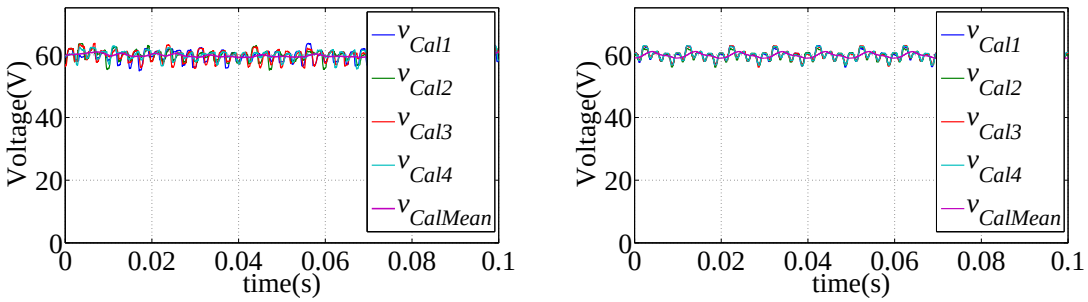
The experimental and simulation results of the capacitor voltages and mean voltages of the tap arms ***au***, ***al***, ***bu*** and ***bl*** under closed-loop operation are shown in Fig 6.24, Fig 6.25, Fig 6.26 and Fig 6.27, respectively.



(a) (b)

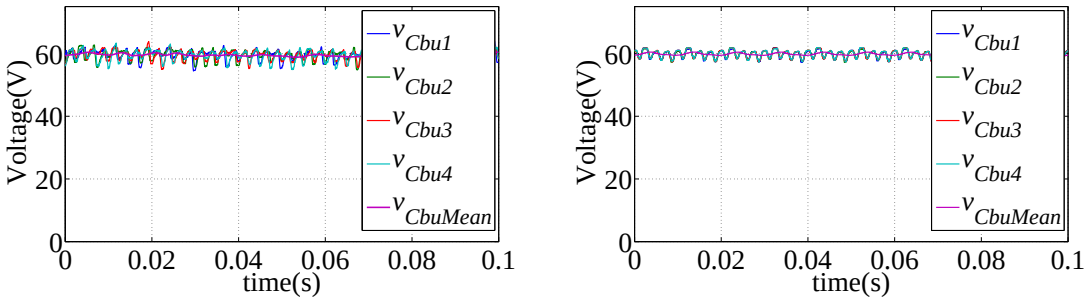
Figure 6.24: **Closed-loop experimental and simulation results** of capacitor voltages v_{Cau} of the tap arm ***au***: (a) Experimental results, (b) Simulation results.

From Fig 6.24–Fig 6.27 it can be seen that



(a) (b)

Figure 6.25: **Closed-loop experimental and simulation results** of capacitor voltages v_{Cal} of the tap arm ***al***: (a) Experimental results, (b) Simulation results.



(a) (b)

Figure 6.26: **Closed-loop experimental and simulation results** of capacitor voltages v_{Cbu} of the tap arm ***bu***: (a) Experimental results, (b) Simulation results.

- The capacitor voltages of each tap arm can be balanced with the rotation method. The mean capacitor voltage of each tap arm can be controlled to the reference value of 60V.
- The average voltage ripple on each capacitor in the experiments is 7V, 11% of the mean capacitor voltage, which is close to that observed under open-loop operation. The percentage is larger than the designed ±5% ripple, the reason of which is the same as that under open-loop operation.

The dynamic experiments of the mean capacitor voltage loop are also carried out. The time constant of the PI regulator τ_{V_C} is set to be 10ms which means the mean capacitor voltage loop responses slower than the current loop. Then the parameters

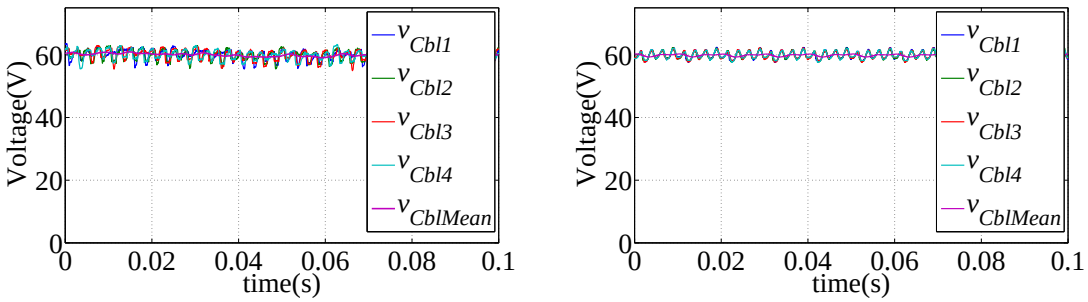


Figure 6.27: **Closed-loop experimental and simulation results** of capacitor voltages v_{Cbl} of the tap arm ***bl***: (a) Experimental results, (b) Simulation results.

of the PI regulator is k_{p-V_C}=18 and k_{i-V_C}=20 based on the analysis in Section 4.3 and the experimental parameters listed in Table 5.1.

Fig 6.28 shows the waveforms of the capacitor voltages with the voltage reference varying from 60V to 70V at 0.05s. The response of the mean capacitor voltage control loop (first-order system) takes approximately 52ms to reach the 98% of the reference value. This indicates that the the time constant of the mean capacitor voltage regulator is $\tau_{V_C} = \frac{52}{4}$=13ms, which is close to the designed time constant.

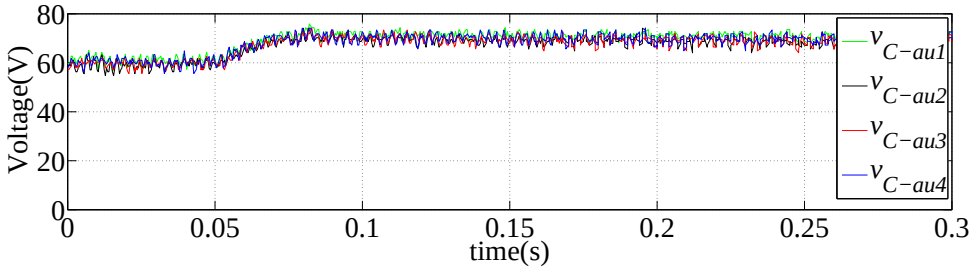
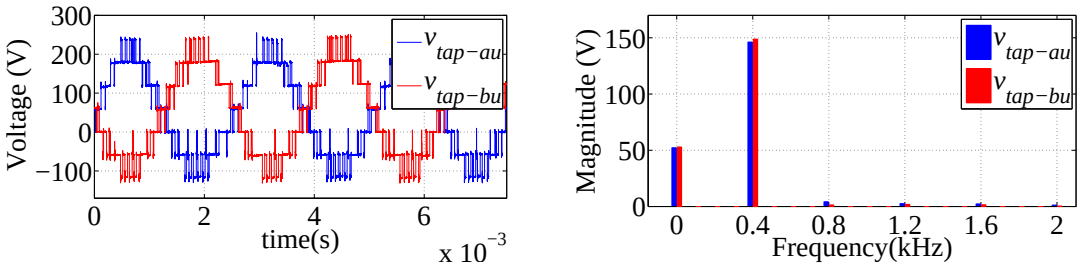


Figure 6.28: Waveforms of the sub-module capacitor voltages

6.4.3 Closed-loop Results of the Tap Arm Voltages and Currents

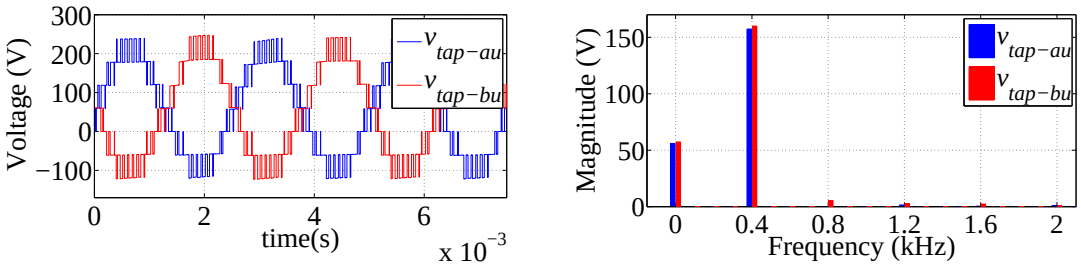
Closed-loop Results of Upper Tap Arm Voltages

The experimental and simulation results of the voltages v_{tap-au} & v_{tap-bu} of the tap arms ***au*** and ***bu*** under closed-loop operation are shown in Fig 6.29 and Fig 6.30 respectively.



(a) (b)

Figure 6.29: **Closed-loop experimental results** and the associated spectra of the voltages v_{tap-au} & v_{tap-bu} of tap arms ***au*** and ***bu***: (a) Waveforms, (b) The DFT analysis.



(a) (b)

Figure 6.30: **Closed-loop simulation results** and the associated spectra of the voltages v_{tap-au} & v_{tap-bu} of tap arms ***au*** and ***bu***: (a) Waveforms, (b) The DFT analysis.

From Fig 6.29 and Fig 6.30 it can be found that

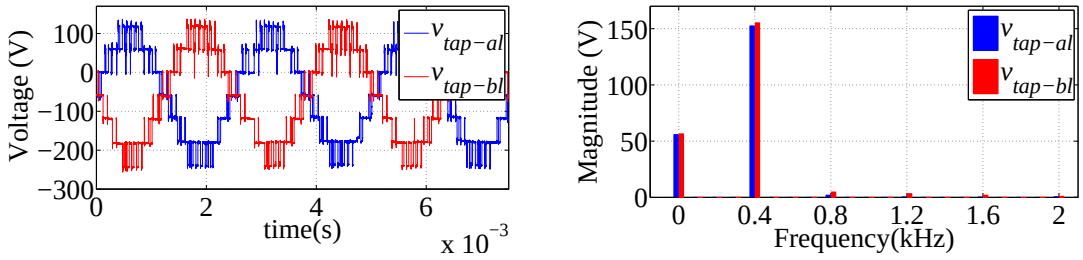
- The tap arm voltages v_{tap-au} & v_{tap-bu} consist of the DC components and AC components. The DC bias voltages of v_{tap-au} & v_{tap-bu} are 54.1V and 55.9V

respectively, which are higher than the reference value of 50V. The RMS AC voltages of v_{tap-au} & v_{tap-bu} are 103.4V and 105.2V respectively, which are higher than the reference value of 100V. The errors between the measured values and the reference values occur because the DC power inserted into each tap arm is equal to the load power plus the power losses of sub-modules and the LC branches, and the AC load power is controlled to be the reference value by the inner current loops. The power losses lead to a higher DC input power of the tap arm, which results in higher DC and AC tap voltages. The errors between the voltage components of two tap arms come from the uncontrolled power balance of the two arms.

- The tap voltage waveforms from the experiments have several spikes in one fundamental period, which, as analysed in Section 6.3, results from the rotation method and the dead time.

Closed-loop Results of Lower Tap Arm Voltages

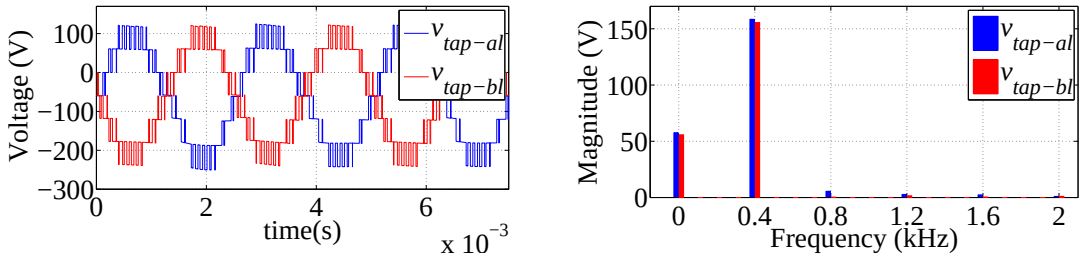
The experimental and simulation results of the voltages v_{tap-al} & v_{tap-bl} of the tap arms ***al*** and ***bl*** under closed-loop operation are shown in Fig 6.31 and Fig 6.32 respectively.



(a) (b)

Figure 6.31: **Closed-loop experimental results** and the associated spectra of the voltages v_{tap-al} & v_{tap-bl} of tap arms ***al*** and ***bl***: (a) Waveforms, (b) The DFT analysis.

From Fig 6.31 and Fig 6.32 it can be seen that the DC bias voltages of v_{tap-al} & v_{tap-bl} are 55.8V and 56.5V respectively. The RMS AC voltages of v_{tap-au} & v_{tap-bu} are 107.8V and 109.8V respectively. The simulation results in Fig 6.30 and Fig 6.32



(a) (b)

Figure 6.32: **Closed-loop simulation results** and the associated spectra of the voltages v_{tap-al} & v_{tap-bl} of tap arms ***al*** and ***bl***: (a) Waveforms, (b) The DFT analysis.

are nearly identical with the experimental results in Fig 6.29 and Fig 6.31, which indicates that the simulation results are correct and the experimental rig operates as expected.

Based on the data in Fig 6.29 and Fig 6.31, the efficiency of the two-phase MMST under closed-loop operation of the experiments can be estimated as

$$\eta_{closed} = \frac{(I_{la}^2 + I_{lb}^2) \cdot R_l}{I_{DC} \cdot (V_{DC-au} + V_{DC-al} + V_{DC-bu} + V_{DC-bl})} = 90\%$$

The efficiency can be improved by decreasing the switching frequency but the output characteristics would be worse. In the simulation of the two-phase MMST, the power loss of one IGBT module is $P_{loss-one}$=12W, as mentioned in Section 5.2. If only counting the power losses of the IGBTs and ignoring the resistive losses in the rig, the efficiency can be estimated to be

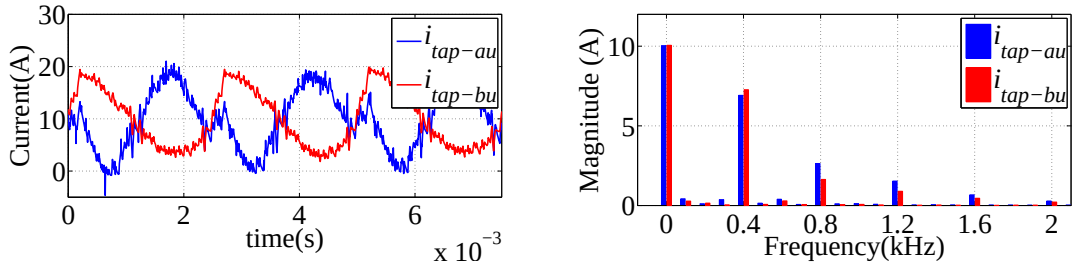
$$\eta_{simu} = \frac{P_l}{P_l + 2n_{ph} \cdot n_{SM} \cdot P_{loss-one}} = 91.3\%$$

which is close to the estimated efficiency in the experiments.

Closed-loop Results of Upper Tap Arm Currents

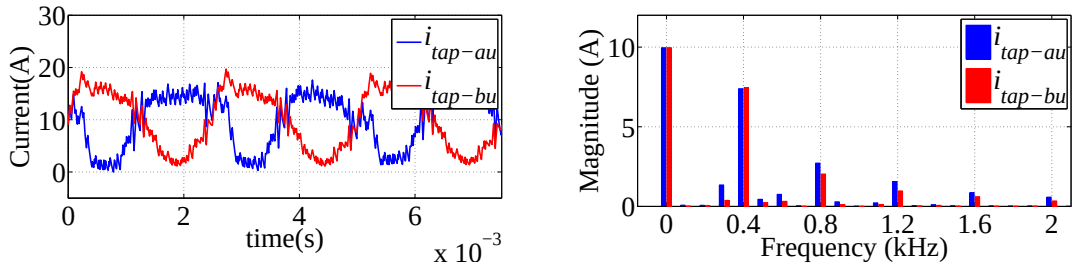
The experimental and simulation results of the currents i_{tap-au} & i_{tap-bu} of tap arms ***au*** and ***bu*** under closed-loop operation are shown in Fig 6.33 and Fig 6.34 respectively.

From Fig 6.33 and Fig 6.34 it can be concluded that



(a) (b)

Figure 6.33: **Closed-loop experimental results** and the associated spectra of the currents i_{tap-au} & i_{tap-bu} of tap arms ***au*** and ***bu***: (a) Waveforms, (b) The DFT analysis.



(a) (b)

Figure 6.34: **Closed-loop simulation results** and the associated spectra of the currents i_{tap-au} & i_{tap-bu} of tap arms ***au*** and ***bu***: (a) Waveforms, (b) The DFT analysis.

- Both of the tap arm currents i_{tap-au} & i_{tap-bu} consist of the DC components and AC components. The DC components are the 10A DC grid current. The AC components here include fundamental loop currents, 800Hz harmonics and other higher order harmonics.
- Comparing Fig 6.33 and Fig 6.34, the waveforms of i_{tap-au} & i_{tap-bu} in the experiments and the simulation looks different but the difference in magnitudes for the components from the DFT analysis are almost identical.

6.5 Summary

In this chapter the start-up, transient-state and the steady-state operation of the experimental rig have been analysed and the experimental and simulation results have been presented. Firstly, during the start-up the anti-windup method of the DC grid emulator and the increasing reference method of the two-phase MMST have been implemented and the overshoot of the DC current and the capacitor voltages are relatively small. Secondly, in the steady state the experimental results of the DC grid emulator and the MMST under open-loop and closed-loop operation have been shown, and the comparison with the simulation results have been provided. The results show that the experimental MMST operates well, and that the controlled values follow the given references. Thirdly, in the transient state the dynamic response of the control loops can match the theoretical design. According to the results and the comparison, the feasibility of the experimental two-phase MMST has been verified both by the simulation and the experiments, and the validity of the control strategies has been proved by the comparison between the transient experimental results. In conclusion, with the simulation and experimental results of the two-phase MMST, the feasibility of the n-phase MMST and the validity of the control strategies have been verified.

Chapter 7

Conclusion

7.1 Conclusion

The thesis proposes a novel n-phase multi-modular series HVDC tap and a corresponding control strategy. The theoretical analysis, simulation and experimental verification of the n-phase MMST has been provided.

HVDC transmission has advantages for long-distance bulk-power transmission, which is beneficial to optimise the allocation of natural resources and decrease the consumption of the energy transportation. Connecting the small remote communities to the HVDC transmission line using an HVDC tap would be beneficial.

Until now various HVDC taps have been proposed, among which the series taps are advantageous in the application of acquiring small amount of power. Considering the development tendencies of power electronics converters in parallel taps, the 3rd generation of series taps with a modular multilevel structure, such as a series MMC, could solve the problems of large harmonics injection into the HVDC network and difficult synchronous operation of series semiconductor devices in conventional series taps. However, the HV rated transformer is still necessary for isolation. An n-phase MMST is proposed to remove the need for the transformer and fully utilise the capability of full-bridge sub-module arms.

As described in Chapter 3, the n-phase MMST topology replaces the high-voltage isolation transformer with LC blocking branches, reducing the design difficulty of the high-voltage decoupling components in conventional series taps. Furthermore, it utilises the AC output capability of full-bridge sub-modules to generate the AC voltage to the load. With the DC bias voltage added on the arm voltage, the injected DC power is equal to the outflowing AC power and the net energy exchange is zero. The topology can be designed mainly by the power, voltage and current ratings, the number of phases and the current-carrying capability of the sub-modules. A 20MW, 10kV two-phase MMST operating at 300Hz basically needs 80 sub-modules with a 2kV, 3.07mF capacitor inside each one, 6 42.7mH branch inductors and 900 2kV, 1mF blocking capacitors. The semiconductor power loss of this MMST is 288.7kW under 6kHz switching frequency. The inductor power losses of the two-phase MMST is 325.4kW under 300Hz operating frequency. The power losses of the semiconductor devices and the inductors yields a percentage of 3.07% comparing to the power rating of the two-phase MMST.

The control strategy of an n-phase MMST has been proposed and verified in a PLECS simulation. As introduced in Chapter 4, with the inner loop current control, mean capacitor voltage control and outer DC link voltage control, the two-phase MMST can operate effectively in the idealised HVDC system. The controlled values follow the references and the steady-state errors can be eliminated.

The topology and control design for the MMST with the ideal AC loads in the ideal HVDC system have been analysed. Nonetheless in the real application the harmonics at the frequencies similar with the MMST's fundamental frequency would possibly appear, overlaying on the sampled controlled values and then disturbing the control loops. However, the harmonics lightly influences the output power quality and the could probably be filtered by the cable. In addition, in MMC the sub-module arm currents are mainly sampled for the 2^{nd} harmonic suppression. Therefore, mainly focusing on the output characteristics of the MMST and ignoring the influence of harmonics, a new sampling variable avoiding the harmonic disturbance in the control loops is proposed. The load currents and the DC line current are sampled and the

arm and loop currents are calculated from these values. These new sampling variables have no difference with the typical sampling variables in the steady-state operation.

The experiments for further proving the feasibility of the n-phase MMST and validity of the proposed control strategy have been carried out. The experimental rig of the two-phase MMST with the scaled-down parameters has been built in the lab. The detailed design procedure for the rig has been given. The experiments of the two-phase MMST under open- and closed-loop operation have been carried out. The experimental results and the simulation results with the same circuit and parameters have been compared. In the closed-loop experiments the load current per phase can follow the reference at 10A, the mean capacitor voltage of each tap arm can follow the reference at 60V and the capacitor voltages can be balanced. The simulation results closely match with the experimental results, verifying the correctness of both results.

In conclusion, an n-phase MMST which realises the utilisation of the modular multilevel structure in the series tap, removes the need for an HV rated isolation transformer, injects few harmonics into the HVDC network and avoids the adoption of series-connected semiconductor devices is proposed. The corresponding control strategy is introduced. The feasibility of an n-phase MMST and the applicability of the presented control strategy for an n-phase MMST are verified through simulation studies and experiments.

7.2 Future Works

In the future the research of the n-phase MMST can focus on the following points.

1. Optimise the topology design of the n-phase MMST. For instance, the inductors in the blocking branches may be moved to the load branch in each phase, in series with the load. Then the branch inductors can be removed and the value of the load branch inductor may be identical with the original branch inductor, reducing the inductor number from 4 to 1. The feasibility of the new topology

needs to be verified. Also there are various other topologies of the MMST that can be researched and proposed.

2. Carry out the dq current control loop and the corresponding control loops specifically for the three-phase MMST. The three-phase systems are most widely accepted in the power networks, which may lead to an extensive application of the three-phase MMST. Therefore an optimised control strategy simplifying 6 individual loops for 6 tap arms to 2 control loops for upper three arms and lower three arms could be beneficial.

3. Combine the MMSTs with the odd and even number of phases based on the new sampling variables. The main reason for separating the MMST topology by the odd and even number of phases is the difficulty to acquire the currents of each loop individually from the combined branch. But the loop currents are not necessary if adopting the new sampling variables. Therefore combining the MMST topologies of odd and even numbers of phases are feasible. The potential for this combination needs to be verified.

4. Solve the harmonic problems in the MMST. The fundamental harmonic in each branch of the two-phase MMST can be obtained from the upper and lower loop currents of each phase. The algorithm of suppressing the harmonics may be developed and the comparison between the control effects of this method and the new sampling variables can be achieved.

5. Develop the second-stage circuit for the n-phase MMST. For example, the concept of using a CHB converter in the DC/AC part of the second stage may present many advantages.

6. Compare the modular multilevel based parallel tap and the MMST with the investment and losses.

Appendix A

Net Energy Analysis of N-phase Series Tap

Technically the sub-modules in n-phase series tap cannot store or release energy continuously in order to keep the capacitor voltage constant. The net energy exchange of sub-modules is the integral of power in one period. And the power equals to the product of the voltage and current of the sub-modules, which is given in (3.1) and (3.3). The detailed derivation is given by

$$\begin{aligned} p_{tap-i} &= v_{tap-i} \cdot i_{tap-i} \\ &= \left(V_{DC} + \hat{V}_{AC-i} \cdot sin(\omega t + \frac{2\pi}{n_{ph}} \cdot i)\right) \cdot \left(I_{DC} + \hat{I}_{AC-i} \cdot sin(\omega t + \frac{2\pi}{n_{ph}} \cdot i + \theta)\right) \\ &= V_{DC} \cdot I_{DC} + \frac{\hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot cos\theta}{2} \\ &\quad + V_{DC} \cdot \hat{I}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i + \theta\right) \\ &\quad + I_{DC} \cdot \hat{V}_{AC-i} \cdot sin(\omega t + \frac{2\pi}{n_{ph}} \cdot i) \\ &\quad - \hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot cos(2\omega t + \frac{4\pi}{n_{ph}} \cdot i + \theta) \end{aligned} \tag{A.1}$$

where n_{ph} is thedesired number of phases in the tap, i is the specific phase number, θ is the phase difference of source voltage and current. i_{tap-i} is the tap AC current

of phase i, I_{DC} is the DC current of HVDC line, v_{tap-i} is tap AC voltage, and V_{DC} is the DC bias voltage that the sub-modules should generate.

If energy change $e_{tap-i} = \int p_{tap-i} dt$ in one fundamental period is zero, the DC component of p_{tap-i} needs to be 0. So

$$V_{DC} = -\frac{\hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot cos\theta}{2I_{DC}} \tag{A.2}$$

If the tap is operating at unity power factor, $\theta = 0$, then

$$V_{DC} = -\frac{\hat{V}_{AC-i} \cdot \hat{I}_{AC-i}}{2I_{DC}} \tag{A.3}$$

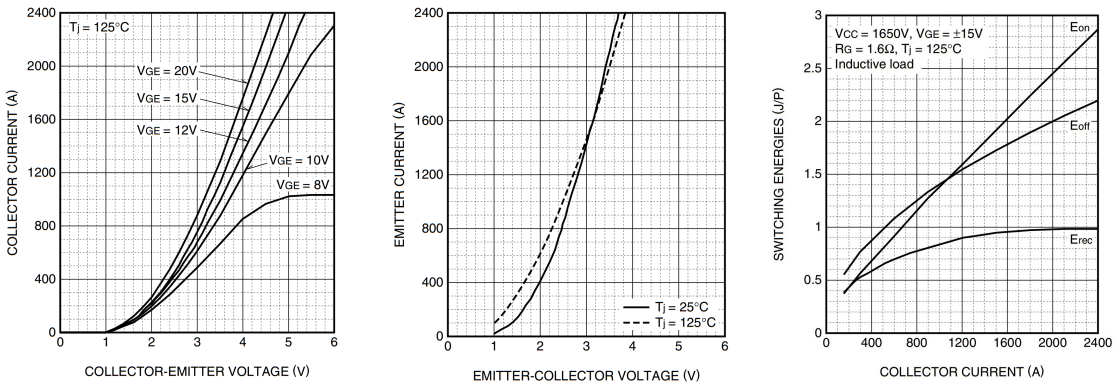
Based on (A.3), the DC bias voltage can be calculated and put into control system.

Appendix B

Characteristics of the IGBT Module Used in the Theoretical Analysis

Figure B.1 shows the conduction and switching characteristics of the MITSUBISHI CM1200HG-66H HVIGBT module [105]. Values of IGBTs′ voltage drop values are based on the $V_{GE} = 15V$, $T_j = 25°C$ curve, and the diodes′ values are based on the $T_j = 25°C$ curve.

The conduction loss of one IGBT $p_{IGBT-one}$ from Figure B.1(a), The conduction loss of one diode $p_{diode-one}$ from Figure B.1(b) and the switching loss energy e_{on}, e_{off} and e_{rec} from Figure B.1(c) are the curves in the figure which need to transfer to the formulas utilising the curve fitting method. The results of the curve fitting are given



(a) (b) (c)

Figure B.1: IGBT & Diode Characteristics from the Datasheet: (a) IGBT output characteristics, (b) Diode forward characteristics, (c) Switching energy characteristics.

in (B.1).

$$\begin{cases} p_{IGBT-one}(i_0) = |i_0| \cdot (0.0003759\,|i_0| + 0.06981\sqrt{|i_0|} + 0.744) \\ p_{diode-one}(i_0) = |i_0| \cdot (0.0002018\,|i_0| + 0.06075\sqrt{|i_0|} + 0.3572) \\ e_{on}(i_0, v_{IGBT}) = (1.1875\,|i_0| + 0.1875) \cdot \frac{v_{IGBT}}{1650} \\ e_{off}(i_0, v_{IGBT}) = \left(0.2505|i_0|^3 - |i_0|^2 + 1.93\,|i_0| + 0.2505\right) \cdot \frac{v_{IGBT}}{1650} \\ e_{rec}(i_0, v_{IGBT}) = \left(-0.2263|i_0|^2 + 0.9129\,|i_0| + 0.1337\right) \cdot \frac{v_{IGBT}}{1650} \end{cases} \tag{B.1}$$

Appendix C

The Damping in LC Blocking Branch

C.1 Theoretical Analysis of LR Damping Branch

The design of the LC blocking branch requires to be adequately damped, preventing transients and disturbances in the sub-module strings, attaining the desired attenuation as well. [85] Figure C.1 shows three commonly used damping methods, including LR parallel damping (Figure C.1(a)), CR parallel damping (Figure C.1(b)) and LR series damping (Figure C.1(c)). The LC parallel damping is put into detailed analysis.

In this circuit, the transfer function between the load voltage V_l and the tap arm voltage V_{tap} is difficult to figure out, so the analysis is mainly focused on the impedance of the LC branch with damping. The impedance in frequency-domain is given by

$$\begin{aligned} Z_0 &= \frac{1}{j\omega C_f} + j\omega L_f || (j\omega L_b + R_f) \\ &= \frac{{L_f}^2 \cdot R_f \cdot \omega^2}{{R_f}^2 + (L_f + L_b)^2 \cdot \omega^2} \\ &\quad + j(-\frac{1}{\omega C_f} + \frac{L_f \cdot {R_f}^2 \cdot \omega + {L_f}^2 \cdot L_b \cdot \omega^3 + L_f \cdot {L_b}^2 \cdot \omega^3}{{R_f}^2 + (L_f + L_b)^2 \cdot \omega^2}) \end{aligned} \tag{C.1}$$

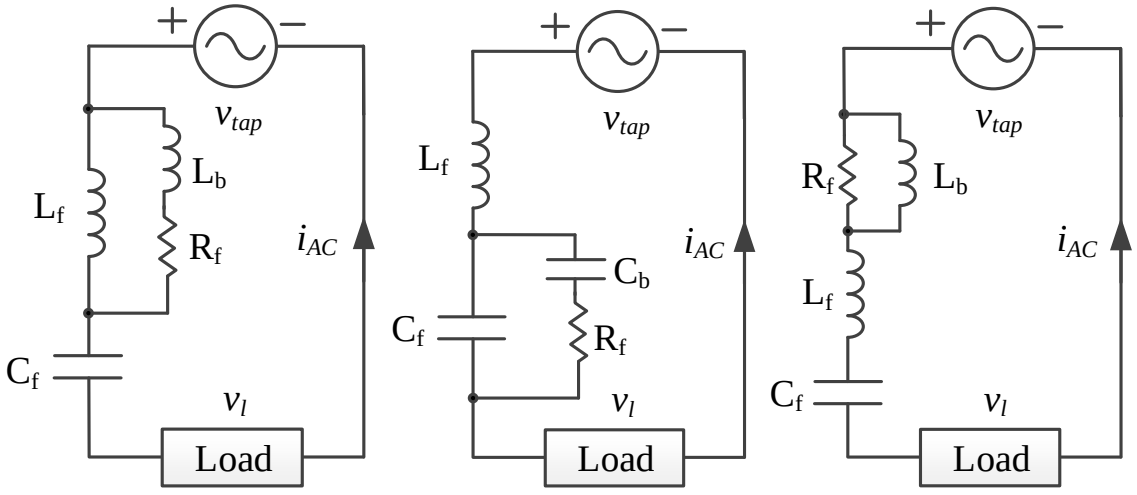


Figure C.1: Three approachs for damping the LC filter: (a) LR parallel damping, (b) CR parallel damping, (c) LR series damping.

For the convenience of the analysis, assume

$$\begin{cases} Re\left(Z_0\right) = \frac{{L_f}^2 \cdot R_f \cdot \omega^2}{{R_f}^2 + (L_f + L_b)^2 \cdot \omega^2} = R_{equiv} \\ Im\left(Z_0\right) = {Z'}_{L_{equiv}} \\ Z_{L_{equiv}} = {Z'}_{L_{equiv}} + \frac{1}{\omega C_f} \\ Z_{L_f} = \omega L_f \\ Z_{L_b} = \omega L_b \end{cases} \tag{C.2}$$

So

$$\begin{cases} R_{equiv} = \frac{{Z_{L_f}}^2 \cdot R_f}{{R_f}^2 + (Z_{L_f} + Z_{L_b})^2} \\ Z_{L_{equiv}} = \frac{Z_{L_f} \cdot {R_f}^2 + {Z_{L_f}}^2 \cdot Z_{L_b} + Z_{L_f} \cdot {Z_{L_b}}^2}{{R_f}^2 + \left(Z_{L_f} + Z_{L_b}\right)^2} \end{cases} \tag{C.3}$$

After simplification

$$\begin{cases} \left(R_f - \frac{{Z_{L_f}}^2}{2R_{equiv}}\right)^2 + \left(Z_{L_b} + Z_{L_f}\right)^2 = \left(\frac{{Z_{L_f}}^2}{2R_{equiv}}\right)^2 \\ {R_f}^2 + \left(Z_{L_b} - \frac{Z_{L_f} \cdot \left(2Z_{L_{equiv}} - Z_{L_f}\right)}{2\left(Z_{L_f} - Z_{L_{equiv}}\right)}\right)^2 = \left(\frac{Z_{L_f} \cdot \left(2Z_{L_{equiv}} - Z_{L_f}\right)}{2\left(Z_{L_f} - Z_{L_{equiv}}\right)}\right)^2 + \frac{Z_{L_{equiv}} \cdot {Z_{L_f}}^2}{Z_{L_f} - Z_{L_{equiv}}} = \frac{{Z_{L_f}}^4}{4\left(Z_{L_f} - Z_{L_{equiv}}\right)^2} \end{cases} \tag{C.4}$$

The reason of simplifying to (C.4) is that the relationship among R_f, Z_{L_b} and R_{equiv}, $Z_{L_{equiv}}$ needs to be found, and the solutions of the equation, which are R_f and Z_{L_b},

need to be obtained. If R_f and Z_{L_b} are treated as unknown quantities, Z_{L_f}, R_{equiv}, Z_{equiv} are treated as known quantities, these equations can be drawn to two circles in one coordinate system, in which x-axis is R_f and y-axis is Z_{L_b}. So the coordinates of their intersections are the solutions of (C.4). This method can give some guidance of the relationship among all the components in the LC damping branch, as well as some significance of R_f and Z_{L_b} value selection. Figure C.2 shows the graph of R_f and Z_{L_b} equations.

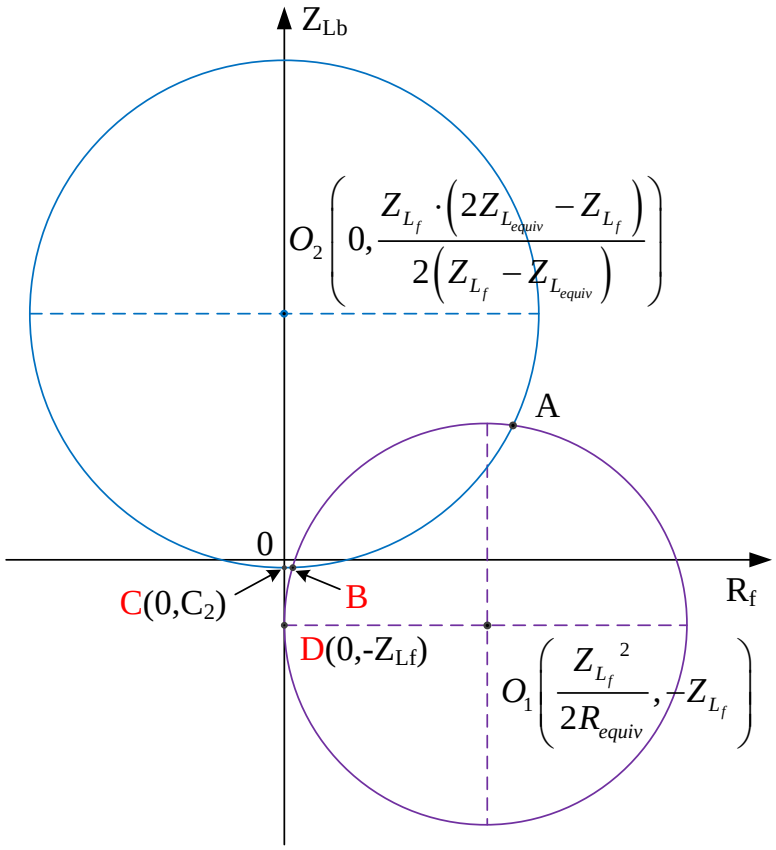


Figure C.2: Graph of R_f and Z_{L_b}

In Figure C.2, point C is the intersection of O_2 circle and y-axis. The position of C

needs to be figured out first.

$$\begin{cases} CO_2 = \frac{{Z_{L_f}}^2}{2\left(Z_{L_f} - Z_{L_{equiv}}\right)} \\ OO_2 = \left(\frac{Z_{L_f} \cdot \left(2Z_{L_{equiv}} - Z_{L_f}\right)}{2\left(Z_{L_f} - Z_{L_{equiv}}\right)}\right) \\ DO_2 = \left(\frac{Z_{L_f} \cdot \left(2Z_{L_{equiv}} - Z_{L_f}\right)}{2\left(Z_{L_f} - Z_{L_{equiv}}\right)}\right) + Z_{L_f} = \frac{{Z_{L_f}}^2}{2\left(Z_{L_f} - Z_{L_{equiv}}\right)} \end{cases} \tag{C.5}$$

So $\begin{cases} CO_2 = DO_2 \\ CO_2 > OO_2 \end{cases}$. B, C and D are the same points. One of the intersections of two circles is $B(0, -Z_{L_f})$. The modified graph is shown in Figure C.3.

There are two intersections of two circles, A and B. It is obvious that the coordinate of intersection B cannot be used as the values of R_f and Z_{L_b}. So point A is the only one that is useful for R_f & L_b value selection. Generally there are some guidance for value selection of R_f and Z_{L_b}:

- Given the cost and power, the value of Z_{L_b} is better to be lower than Z_{L_f}, but above zero.
- R_{equiv} is better to be low, in order to reduce the power loss of the LC branch.

It can be seen that the abscissa of O_1 is increasing when R_{equiv} reduces. But when R_{equv} reduces, the ordinate of point A is increasing. Then if Z_{L_b} is kept to be low, a bigger circle O_2' is needed to decrease the ordinate of point A, which means a larger radius of circle O_2 is needed. Because point B has been set, the ordinate of O_2, $\frac{Z_{L_f} \cdot \left(2Z_{Lequvi} - Z_{L_f}\right)}{2\left(Z_{L_f} - Z_{L_{equiv}}\right)}$ needs to be higher in order to increase the radius of circle O_2.
Since the operating frequency is higher than the LC resonant frequency, Z_{L_f} is larger than $\frac{1}{\omega C_f}$ at the operating frequency. Therefore, there is a difference between Z_{L_f} and $\frac{1}{\omega C_f}$. And if $Z_{L_{equiv}}$ is larger than Z_{L_f}, the ordinate of O_2 is minus and point A is in fourth quadrant. The ordinate of point A is minus, which is not a suitable value for Z_{L_b}. So

$$\begin{cases} \frac{1}{\omega C_f} @ f_f < Z_{L_{equiv}} < Z_{L_f} @ f_f \\ 0 < {Z'}_{L_{equiv}} < \left(Z_{L_f} - \frac{1}{\omega C_f}\right) @ f_f \end{cases} \tag{C.6}$$

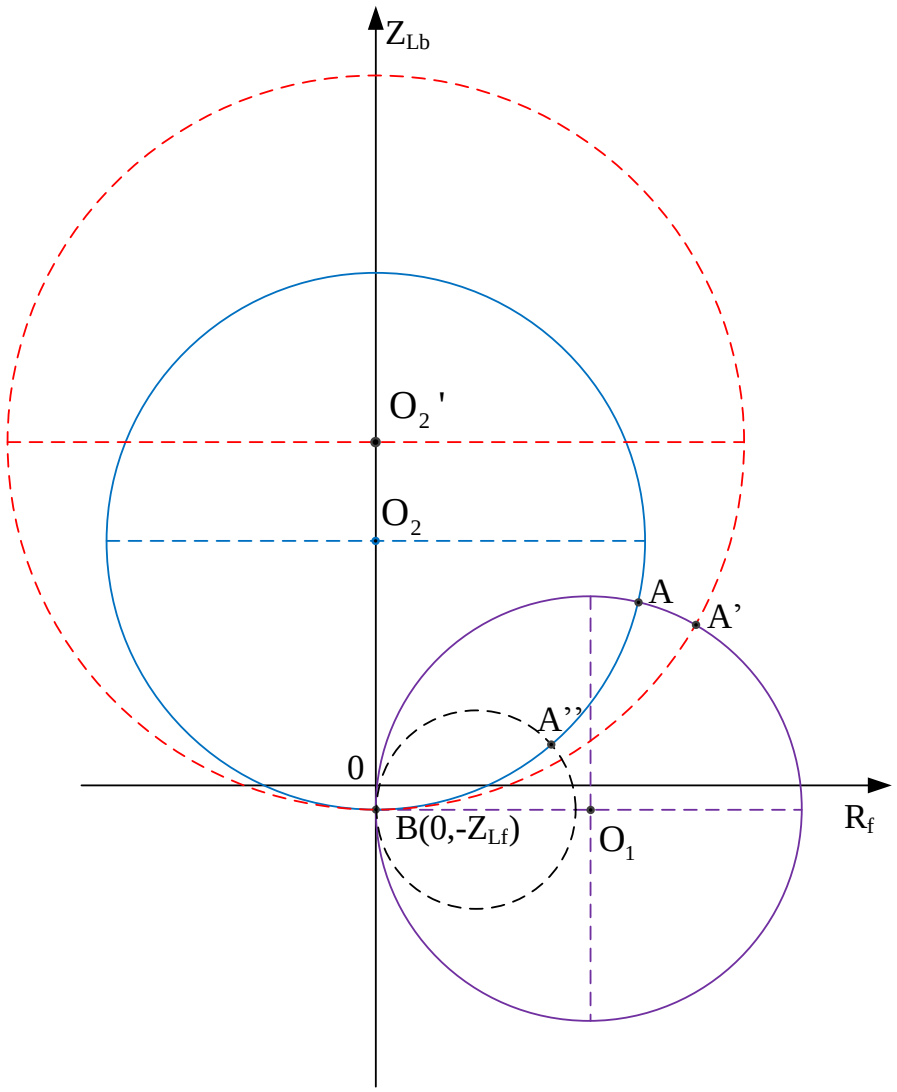


Figure C.3: Modified graph of R_f and Z_{L_b}

If $\frac{Z_{L_f}\cdot\left(2Z_{L_{equiv}}-Z_{L_f}\right)}{2\left(Z_{L_f}-Z_{L_{equiv}}\right)}$ needs to be high, $Z_{L_{equiv}}$can be selected to be near Z_{L_f}, but lower than Z_{L_f}. After some geometrical analysis of (C.4), some guidance can be concluded if seen conversely:

- In a reasonable range, no matter what L_b & R_f values are, the equivalent impedance of the LC branch with damping ($Z'_{L_{equiv}}$) won't be larger than the impedance of LC branch without damping($\left(Z_{L_f}-\frac{1}{\omega C_f}\right)$ @f_f).
- In order to reduce the equivalent resistance of the LC branch with damping

(to reduce the power loss on the equivalent resistance), the reactance of R_f should be much larger than that of L_b. The value of R_f can be determined by the maximum power losses of the MMST.

- The equivalent resistance of the LC branch with damping (R_{equiv}) is mainly influenced by R_f. The larger the R_f value is, the smaller the R_{equiv} value is.
- The equivalent inductance of the LC branch with damping is determined by R_f & L_b. The reactance of R_f is relatively large compared with Z_{L_b}. So once R_f is set, the value of L_b is not the vital one to influence the impedance characteristics.

C.2 Example of LR Damping Design for South West Link

Based on the analysis above, the selection of R_f & L_b values can follow the steps of:

1. R_{equiv} can be determined by the desired maximum power losses.
2. A recommended value of R_f can be obtained by the method above.
3. A reasonable L_b can be given based on the feasibility in a real application.
4. The equivalent impedance of the LC branch with damping can be obtained.

The specific procedure of the LR damping design for a two-phase MMST in South West Link is as follows.

The power losses on the LC blocking branches: <1% of the tap power

$$I_{AC} = \frac{\frac{P_{tap}}{2n_{ph}}}{V_{tap}} = 500\text{A}$$

There are 6 LC branches in the two-phase MMST with the double AC current flowing through the middle branch. Thus the power losses on the middle branch is doubled.

$$\therefore R_{equiv} = \frac{1\% \cdot P_{tap}}{(4 + 2{\times}2) \cdot {I_{AC}}^2} = 0.1\Omega$$

So R_f is set to be **64.8k**Ω, L_b is set to be **0.5mH**. Then

$$R_{L_{equv}} = 0.1004\Omega$$

$$Z'_{L_{equiv}} = 1.4076$$

$$Z_0 = R_{equiv} + sL_{equiv} = 0.1004 + s1.1076$$

The LC branch with damping can be seen as a **0.1004**Ω **resistor and a 0.59mH inductor** in series. The maximum voltage drop on LC branch:

$$\hat{V}_{LC} = |Z_0| \cdot \hat{I}_{AC} = 786\text{V}$$

$$V_{LC}\% = \frac{\hat{V}_{LC}}{\hat{V}_S} = \frac{786}{14.14 \times 10^3} = 5.6\%$$

The parameters are:

$$C_f = 6.67\mu\text{F}$$
$$L_f = 42.7\text{mH}$$
$$R_f = 64.8\text{k}\Omega$$
$$L_b = 0.5\text{mH}$$

C.3 Comparison between LC Branch without and with Damping

Figure C.4 and Figure C.5 shows the bode diagrams of the impedance of the LC branches without and with damping, respectively. It can be seen that the impedance characteristics of the LC branch improves evidently after adding the LR damping branch. The LC branch has reasonable impedance at the operating frequency, which is useful for the loop current control; and relatively high impedance at higher frequencies, which can filter the high frequency harmonics.

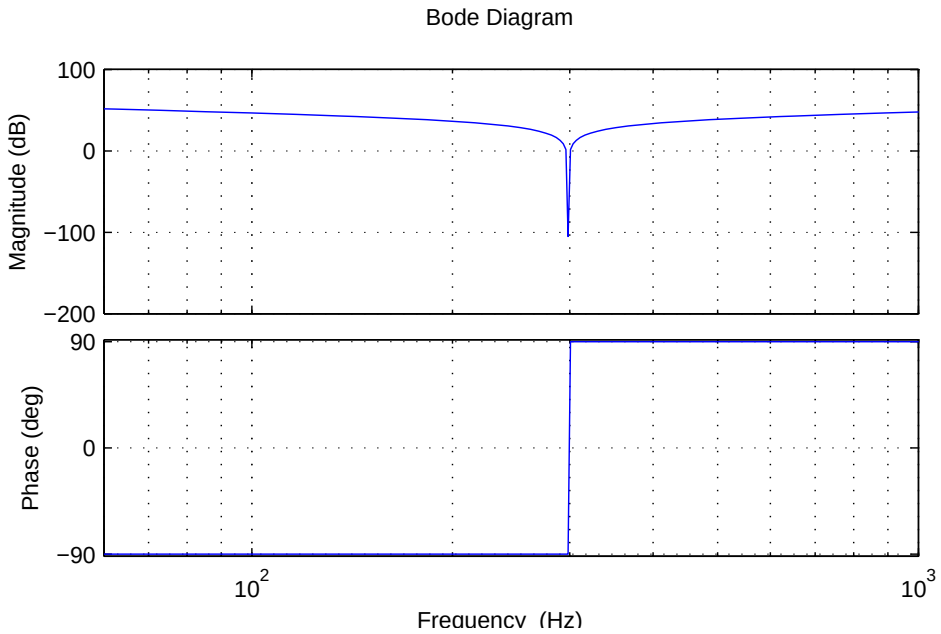


Figure C.4: Bode diagram of the LC branch without damping

C.4 Design Procedure of LC Branch with LR Damping

1. Determine the number of the blocking capacitors according to the HVDC line voltage and the nominal voltage of each capacitor.
2. Determine the inductor value of the LC branch according to the required equivalent impedance at operating frequency and ideal voltage drop on the LC branch.
3. Determine the damping resistor value based on the required maximum power losses on the LC branches.
4. Select a reasonable damping inductor value and calculate the damping resistor value.

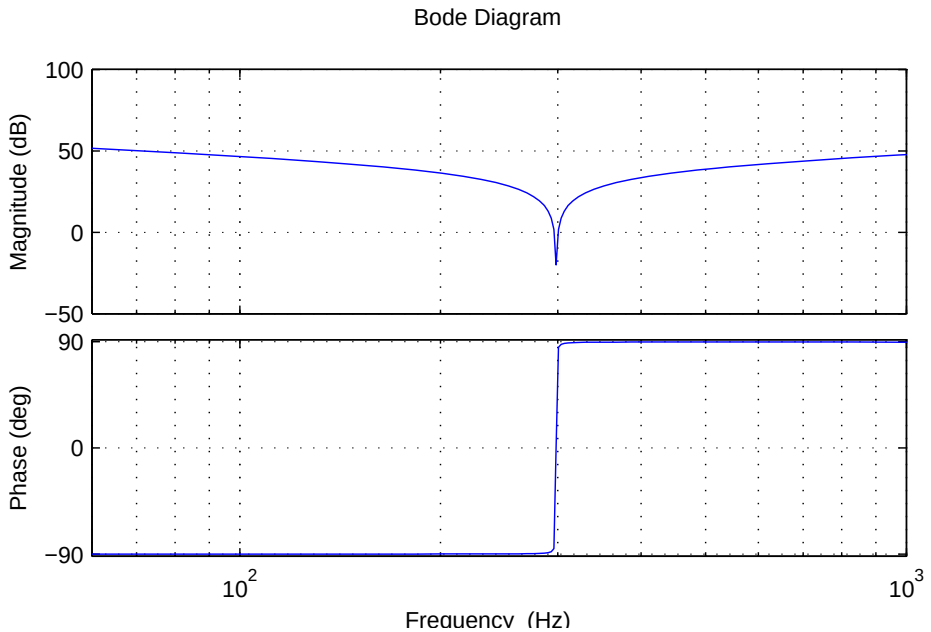


Figure C.5: Bode diagram of the LC branch with RL parallel damping

Appendix D

The Derivation of Equivalent Stationary Controller for PR Regulator

In a single-phase system, the synchronous dq transformation cannot be adopted directly. To date, one of the closest equivalent method is to multiply the reference signal $e(t)$, in turn, by sine and cosine functions, which are synchronised with the reference signal, as shown in Fig D.1 [89]. This achieves the same effect of transforming the component at the chosen frequency to DC, leaving all other components as AC quantities.

For example, take a reference signal at the fundamental frequency, as expressed in (D.1) [92]

$$e(t) = E_0 \cos(\omega t + \theta_0) \tag{D.1}$$

where ω and θ_0 are the fundamental angular frequency and phase shift, respectively. Multiplying this by $\cos(\omega_0 t)$ and $\sin(\omega_0 t)$ gives (D.2) and (D.3), respectively.

$$e_C(t) = \frac{E_0}{2}[\cos(\theta_0) + \cos(2\omega t + \theta_0)] \tag{D.2}$$

$$e_S(t) = \frac{E_0}{2}[\sin(-\theta_0) + \sin(2\omega_0 t + \theta_0)] \tag{D.3}$$

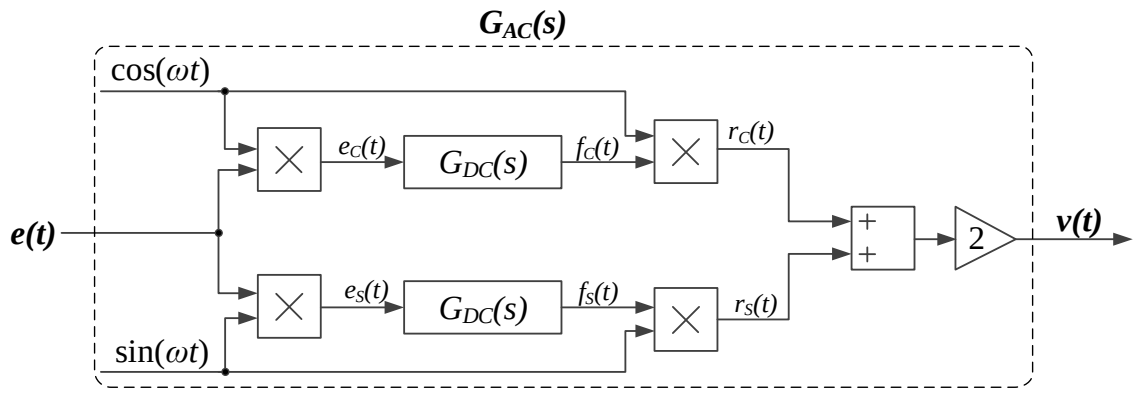


Figure D.1: Single-phase equivalent diagram of the stationary PR regulator and the synchronous PI regulator

It can be seen that the reference signal now appears as DC quantities $\frac{E_0}{2}\cos(\theta_0)$ and $\frac{E_0}{2}\sin(-\theta_0)$, with the values of amplitude and phase shift. But the complication with this equivalent single-phase transformation is that it contributes the harmonic terms at higher frequency terms like $\cos(2\omega t + \theta_0)$ and $\sin(2\omega_0 t + \theta_0)$.

This is different with three-phase synchronous dq transformation, where an undistorted input at a certain frequency contributes only towards the DC term. The main restriction of most stationary frame linear regulators is that they are not able to eliminate steady-state error. The three-phase synchronous dq regulator can solve this problem by eliminating the steady-state error of DC terms in synchronous frame and transferring them back to AC quantities in the stationary frame. For this kind of conventional linear regulators, the integral term gives infinite gain at DC terms and therefore achieves zero steady-state error. The proportional term is mainly responsible for the transient response speed, so it is independent with the frequency variation and whether it is implemented into or out of the frequency transformation is of no consequence. Therefore the proportional and integral term can be analysed separately. The integral term in low-pass filter $G_{DC}(s)$ forces the errors of DC amplitude $\frac{E_0}{2}$ in $e_C(t)$ and $e_S(t)$ to zero, because of its infinite gain. Then it is more like a frequency oscillator [106].

The single-phase synchronous frame controller of Fig D.1 can be given in the time-

domain by

$$\begin{aligned} v(t) &= \{[e(t)\cdot\cos(\omega t)] * g_{DC}(t)\}\cdot\cos(\omega t) \\ &\quad + \{[e(t)\cdot\sin(\omega t)] * g_{DC}(t)\}\cdot\sin(\omega t) \end{aligned} \tag{D.4}$$

where $*$ signifies a convolution product. Based on Fig D.1, the primary aim is to get the transfer function of $G_{AC}(s)$ without the transformation process for stationary to synchronous frame. So in Laplace domain the system is given by

$$V(s) = G_{AC}(s)\cdot E(s) \tag{D.5}$$

To simplify the mathematical derivation, two functions, $f_C(t)$ and $f_S(t)$, are defined as

$$\begin{cases} f_C(t) = [e(t)\cdot\cos(\omega t)] * g_{DC}(t) \\ f_S(t) = [e(t)\cdot\sin(\omega t)] * g_{DC}(t) \end{cases} \tag{D.6}$$

Transform to Laplace domain

$$\begin{aligned} F_C(s) &= l[e(t)\cdot\cos(\omega t)]\cdot G_{DC}(s) \\ &= \frac{1}{2}G_{DC}(s)\cdot[E(s+j\omega)+E(s-j\omega)] \end{aligned} \tag{D.7}$$

$$\begin{aligned} F_S(s) &= l[e(t)\cdot\sin(\omega t)]\cdot G_{DC}(s) \\ &= \frac{1}{2}G_{DC}(s)\cdot[E(s+j\omega)-E(s-j\omega)] \end{aligned} \tag{D.8}$$

Then transform $r_C(t)$ and $r_S(t)$ into Laplace transform

$$\begin{aligned} R_C(s) &= l[f_C(t)\cdot\cos(\omega t)] \\ &= \frac{1}{2}[F_C(s+j\omega)+F_C(s-j\omega)] \\ &= \frac{1}{4}G_{DC}(s+j\omega)\cdot[E(s+2j\omega)+E(s)] \\ &\quad + \frac{1}{4}G_{DC}(s-j\omega)\cdot[E(s)+E(s-2j\omega)] \end{aligned} \tag{D.9}$$

$$\begin{aligned} R_S(s) &= l[f_S(t)\cdot\sin(\omega t)] \\ &= \frac{1}{2}[F_S(s+j\omega)-F_S(s-j\omega)] \\ &= \frac{1}{4}\{-G_{DC}(s+j\omega)\cdot[E(s+2j\omega)-E(s)]\} \\ &\quad + \frac{1}{4}\{G_{DC}(s-j\omega)\cdot[E(s)-E(s-2j\omega)]\} \end{aligned} \tag{D.10}$$

Thus the output signal in Laplace domain is given by

$$\begin{aligned} V(s) &= 2\left[R_C(s) + R_S(s)\right] \\ &= \left[G_{DC}(s+j\omega) + G_{DC}(s-j\omega)\right] \cdot E(s) \end{aligned} \tag{D.11}$$

Hence

$$G_{AC}(s) = \frac{\mathrm{V(s)}}{E(s)} = G_{DC}(s+j\omega) + G_{DC}(s-j\omega) \tag{D.12}$$

(D.12) shows the frequency response of AC controller $G_{AC}(s)$ for any given DC controller $G_{DC}(s)$. This analysis also illustrates that the equivalent diagram can cancel the double-frequency components generated in the first-stage frequency oscillator.

Considering a conventional integrator $G_{DC}(s) = k_p + \frac{k_i}{s}$, the equivalent AC regulator would have an open loop transfer function of

$$G_{AC}(s) = k_p + \frac{2k_r s}{s^2 + \omega^2} \tag{D.13}$$

The ideal integral term provides infinite gain but a restricted frequency response. However in the real application the may have a small frequency difference due to the errors of the components. To solve this problem, the non-ideal integrator $G_{DC}(s) = k_p + \frac{k_r \cdot \omega_C}{s+\omega_C}$ ($\omega_C \ll \omega_0$ is the cutoff frequency) is implemented and gives (D.14) [91].

$$G_{AC}(s) = k_p + \frac{2k_r(\omega_C s + {\omega_C}^2)}{s^2 + 2\omega_C s + ({\omega_C}^2 + \omega^2)} \approx k_p + \frac{2k_r\omega_C s}{s^2 + 2\omega_C s + \omega^2} \tag{D.14}$$

The bandwidth of the non-ideal PR regulator can be set with ω_C value appropriately, which is suitable for the condition of slight frequency variation. In practice, ω_C values of 5-15rad/s have been found to provide a good compromise [92].

It is noted that there is another AC regulator presented in[107] that gives

$$G_{AC}(s) = k_p + \frac{2k_r\omega}{s^2 + \omega^2} \tag{D.15}$$

This regulator can also give infinite gain at the frequency ω_0 and hence achieves zero steady-state error. But the absence of a zero at $s = 0$ results in a slower transient performance [89], and a 180° phase shift of this AC regulator leads to a poorer phase margin [90].

Appendix E

Transducer boards and the Control Unit in the Experiments

The transducer boards and the control unit used in the experimental rig are introduced here. The design procedure and the parameter selection are presented.

E.1 Transducer Boards

The transducer boards are utilised for sampling the instantaneous values of the variables in the experimental platform and transmitting them to the control unit. LV 25-P and LA 55-P are used for voltage and current measurements, respectively, as shown in Fig E.1. In total there are 18 voltage signals including 16 sub-module capacitor voltages and 2 DC grid voltages, and 3 current signals including the DC grid current and 2 load currents of the MMST.

E.1.1 Current Transducer

The current transducer is used to sense the DC grid current and 2 load currents of the MMST. The reason why the load currents i_l are sampled and controlled rather

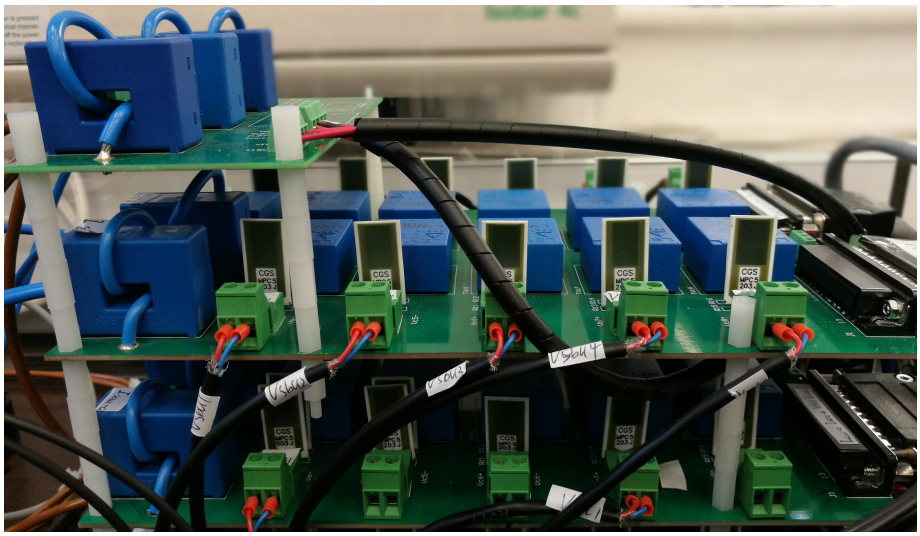


Figure E.1: The transducer boards

than the upper and lower loop currents i_{AC} is discussed in Section 5.4. A closed-loop Hall Effect current transducer, LA 55-P, is selected due to its excellent accuracy, good linearity and high bandwidth [108]. The inner circuit of the LA 55-P current transducer is shown in Fig E.2. The conversion ratio inside LA 55P n_{LA55P} is 1:1000, then the measuring resistance R_M and the number of turns on the transducer need to be calculated.

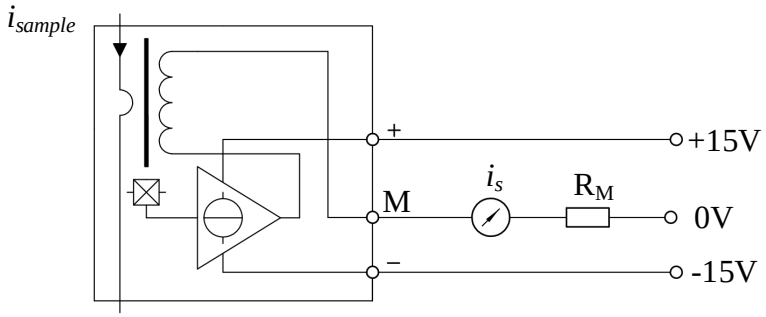


Figure E.2: The inner circuit of LA 55-P current transducer

The maximum current that needs to be measured is the load current with the peak value of 14.1A. Taking the load current i_l as an example, the current measuring range is 28.3A with a double current safety margin. Therefore, in order to make almost full use of the current measuring range of LA 55P, which is ±70A, 2 turns of

primary wiring are needed.

The secondary measuring resistance is to transfer the output current signal from the current transducer to the voltage signal that the FPGA board A2Ds can sample. The voltage sampling range of the FPGA is ±5V. Then the measuring resistance R_M is calculated as

$$2I_{l-peak} \cdot 2 \cdot n_{LA55P} \cdot R_M \leq 5V \tag{E.1}$$

Then $R_M \leq 88.4\Omega$. So the 75Ω measuring resistance is selected. The transducer design for DC grid current is similar with the design for load currents.

E.1.2 Voltage Transducer

The voltage transducers sample 16 sub-module capacitor voltages and 2 voltages at the two sides of the MMST on the DC grid. The Hall Effect voltage transducer LV 25-P is selected. Its inner circuit is shown in Fig E.3. The measured voltage signal is converted to a current signal by an external resistor R_1, and the measuring resistance R_M is also added to convert the output current signal to the voltage signal at the FPGA board. The conversion ratio n_{LV25P} is 2500:1000. R_1 and R_M are calculated as follows.

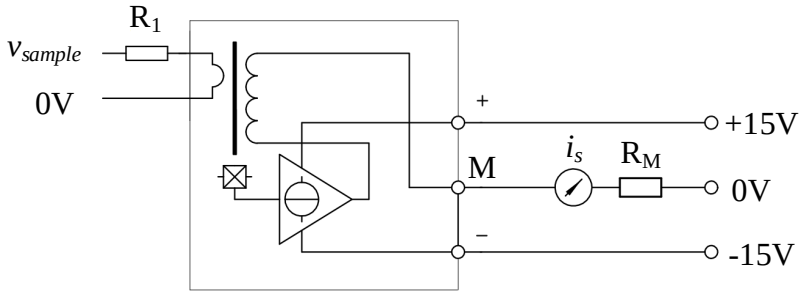


Figure E.3: The inner circuit of LV 25-P voltage transducer

Take the sampling of the sub-module capacitor voltage for example, the nominal voltage of V_C is 60V. With a double voltage safety margin the voltage sampling range is 120V. R_1 acts as a current limiting resistor which prevents the primary

current exceeding ±14mA [109]. Thus the minimum value of R_1 is $\frac{120}{0.014} = 8.5k\Omega$. A 10kΩ MPC series resistor which has a wide operating temperature range is selected.

Using the same calculation method for the measuring resistance R_M on the current transducer circuit, the range of R_M in the voltage transducer circuit can be expressed as

$$\frac{2V_C}{R_1} \cdot n_{LV25P} \cdot R_M \leq 5V \tag{E.2}$$

Then $R_M \leq 167\Omega$. In this work a 137Ω measuring resistor is selected. The transducer design for DC grid voltages is similar to the design for the sub-module capacitor voltages, and is not shown here.

E.2 Control Unit

The control unit consists of 2 TI C6713 development starter kit (DSK) boards, 4 FPGA boards (designed by the PEMC Group, UoN), 2 host post interface daughtercards (HPI) and 2PCs to command the normal operation of the MMST circuit and the DC grid emulator separately. The reason of using two DSPs is that due to the different interrupt time of the two systems, two control algorithms need to be executed within the interrupt time. In order to ensure that both can be executed in a single sampling period, they are run on different DSKs. In conclusion, the DC grid emulator occupies 1 DSK for code executing, 1 FPGA for sampling and PWM generation, and 1 PC for user interaction; the MMST employs 1 DSK, 3 FPGAs and the other PC. The photograph of the assembled MMST control unit is shown in Fig E.4.

The DSP on the DSK is a TMS320C6713 with 225MHz clock rates. This DSP can execute up to 1350 million instructions per second and is suitable for complex algorithms. The DSK is also the interface of the FPGAs and the HPI.

The FPGA board was originally developed by the PEMC Group in the University of Nottingham, and it has been proved a very flexible and versatile board in many other applications [110]. The FPGA chip is a ProASIC3 device with up to one

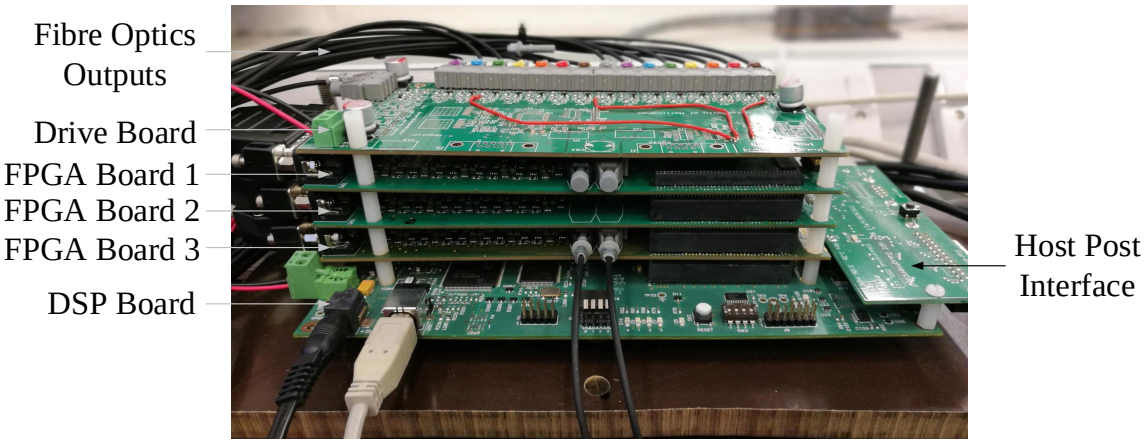


Figure E.4: The control unit of the experimental MMST

million system gates. In addition, this board contains 10 conditioning circuits and A2D converters for signal sampling, 10 hardware protection circuits for over-current and over-voltage protection, 10 optical transmitters for the PWM signal output, and some connectors and buffers for the communication with the DSK or some other devices.

The HPI daughtercard can facilitate a bidirectional data transfer between the host PC and the DSP without interrupting the central processor operation. In addition, this daughtercard provides an alternative way to download the code to the DSP [111].

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