Design and Implementation of a Three-phase Dual Active Bridge DC-DC Converter for MVDC Applications

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Abstract

Due to continuous improvements in power electronics technologies, such as semiconductor devices, passive components, control schemes, and their application at megawatt levels, MVDC grids have emerged as an alternative distribution infrastructure. Furthermore, MVDC technology is starting to be considered as a new power system for enabling the electrification of transportation – automotive, railway, aircraft, and ship – as well as for supplying increased power in urban distribution networks.

High-power DC-DC conversion is one of the primary technologies needed for interconnecting MVDC grids operating at different voltage levels. The three-phase dual active bridge DC-DC (3DAB) converter is recommended for the high-power DC-DC conversion system owing to its high efficiency and bidirectional capability. In the AC link, a galvanically isolated transformer operated in the medium frequency range enables the stepping up or down of the secondary bridge voltage.

This thesis investigates the design considerations of a bidirectional and isolated 3DAB converter with a medium voltage side (ranging up to 40 kV DC), a low voltage side (1.1 kV and 5.2 kV DC), and a rated power of 4 MW. This thesis shows that the above design considerations should be taken into account for passive devices. First, the use of a snubber capacitor in medium voltage and medium frequency operating condition is proposed. Secondly, this thesis presents a step-by-step design and optimisation for medium frequency transformer. The work starts with an overview of the operation of the 3DAB converter topology, followed by a systematic investigation of the design considerations for the given 3DAB converter.

The influence of a snubber circuit on the turn-off current levels and zero-voltage switching (ZVS) operating range is investigated. In DAB converters, hard switching happens for a turn-off. The ZVS snubber capacitor can limit the dv/dt during turn-off, corresponding to hard switching. Therefore, the overlapping area of the voltage and current can be reduced. To obtain the ZVC limits, a DC conversion ratio between the primary bridge and secondary bridge must be carefully set. In a practical system, the

phase-shift angle required to operate the converter can be distorted by dead time. Therefore, the phase-shift angle must be compensated in order to maintain the desired output voltage and power. The ZVS range as snubber capacitance influence with dead time compensation is investigated in this thesis. The compensated phase-shift angle corresponding to the dead time is validated from an experimental validation.

One key component within this 3DAB converter is the medium frequency (≤1 kHz) transformer that provides the galvanic isolation for the step up/down of the different voltage levels. A novel magnetic design optimisation of the three-phase medium frequency transformer for maximising its efficiency when excited by a non-sinusoidal waveform is proposed. Each step in the design is carefully discussed alongside the design requirements, such as identification of optimum geometry parameters, flux density limits, leakage inductance, isolation, and thermal requirements of the transformer. Special attention is paid to the new design optimisation method using low free parameters which is combined with a two-dimensional (2D) finite element analysis (FEA) to set large-scale transformer geometric parameters optimally. The geometric programme can eliminate time-consuming calculations associated with iterative optimisation procedures owing to the use of five degrees of freedom. The optimally computed geometry parameters using a computer-aided looping algorithm are verified using 2D FEA. The FEA design optimisation seeks all important design constraints of the transformer, both internal and external, including winding voltage and current, core material magnetic saturation, temperature rise, and winding and core losses. The proposed design programme is applied to a core-type transformer analysing the outcome of the optimisation process. It also includes a laboratory design of the transformer rated at 10 kW, 1 kHz of fundamental frequency, and turn ratio of 0.5.

Simulation results from two 4-MW demonstrators and experimental results from a 10-kW scale prototype are presented to validate the design methods introduced and examine the efficiency improvements achievable for the given 3DAB converter topology

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Abbreviations list

V_{an}	Phase voltage on primary winding	[V]
V_{rn}	Phase voltage on secondary winding	[V]
φ	Phase shift angle	[rad]
f_{sw}	Switching frequency	[Hz]
ω_{sw}	Switching frequency	[rad/s]
L_{σ}	Leakage inductance	[μH]
d	DC conversion ratio of 3DAB converter	
P_o	Average output power	[W]
V_{pri}	Peak amplitude of DC input voltage	[V]
V_{sec}	Peak amplitude of DC output voltage	[V]
n	Turns ratio of transformer	
i_{a}	Phase current on primary winding	[A]
i_{r}	Phase current on secondary winding	[A]
$I_{\text{OFF_max_p}}$	Maximum turn-off current of primary bridge	[A]
$I_{\text{OFF_max_s}}$	Maximum turn-off current of secondary bridge	[A]
$\omega_{r_p,s}$	Resonant frequency	[Hz]
$Z_{r_p,s}$	Resonant impedance	[Ω]
$t_{\text{off}\|\text{min}}$	Minimum turn-off commutation time	[s]
$C_{sn_p,s}$	Snubber capacitors	[F]

$t_{\text{off_p}}$	Turn-off time of primary bridge	[s]
$t_{\text{off_s}}$	Turn-off time of secondary bridge	[s]
S_T	Apparent power of transformer	[VA]
$\widehat{B}_m$	Maximum flux density	[T]
$N1$	The number of turns on primary winding	
$N2$	The number of turns on secondary winding	
J_p	Current density for primary winding	[A/m^2]
J_s	Current density for secondary winding	[A/m^2]
a	Width of core sectional area	[mm]
d	Length of core sectional area	[mm]
η_e	Estimated efficiency	[%]
$\eta_{\max}$	Maximum efficiency	[%]
A_c	Core sectional area	[mm^2]
k_f	Waveform coefficient	
A_{cu}	Conductor area	[mm^2]
d_{cu}	Conductor diameter	[mm]
A_{cu_p}	Primary conductor cross section area	[mm^2]
A_{cu_s}	Secondary conductor cross section area	[mm^2]
A_{w_p}	Primary conductor area	[mm^2]
A_{w_s}	Secondary conductor area	[mm^2]
A_{w_cu}	Total conductor area	[mm^2]
A_a	Window area for three-phase transformer	[mm^2]
k_u	Window utilisation factor	
w	Width of window area	[mm]
h	Height of window area	[mm]
δ	Skin depth	
ρ	Resistivity of copper conductor	[Ωm]

μ_r	Relative magnetic permeability of the conductor	[H/mm]
μ_0	The permeability of free space	[H/mm]
μ	Permeability of copper	[H/mm]
vol_{core}	Volume of core	[m^3]
W_{tr}	Width of transformer	[mm]
H_{tr}	Height of transformer	[mm]
D_{tr}	Depth of transformer	[mm]
d_{ins_core}	Isolation distance between core and primary conductor	[mm]
d_{ins_ps}	Insulation thickness between the conductors	[mm]
d_{ins_p}	Isolation distance for primary side turns	[mm]
d_{ins_s}	Isolation distance for secondary side turns	[mm]
k_s	Safe factor	
E_{s_ins}	Dielectric strength of the isolation material	[kV/mm]
k_c	The calculated window utilisation factor	
w_{cu_tot}	Total width of conductor area	[mm^2]
w_{cu_p}	Width of primary conductor area	[mm]
w_{cu_s}	Width of secondary conductor area	[mm]
h_{cu_p}	Height of primary conductor area	[mm]
h_{cu_s}	Height of secondary conductor area	[mm]
MLT_p	Mean length of turns of primary winding	[mm]
MLT_s	Mean length of turns of secondary winding	[mm]
P_{cu_tot}	Total copper losses	[W]
P_{cu_p}	Primary side copper losses	[W]
P_{cu_s}	Secondary side copper losses	[W]
P_{s0}	Specific core loss	[W/kg]

P_s	Core loss	[W]
ρ_s	Mass density of core material	[kg/m^3]
MMF_{core}	Magnetomotive forces for core	
MMF_{yoke}	Magnetomotive forces for yoke	
I_{m_peak}	Peak value of magnetising current	[A]
I_{m_rms}	RMS value of magnetising current	[A]
P_{con_igct}	Instantaneous conduction loss for IGCT	[W]
P_{con_d}	Instantaneous conduction loss for diode	[W]
$P_{avg_con_igct}$	Average conduction loss for IGCT	[W]
$P_{avg_con_d}$	Average conduction loss for diode	[W]
P_{sw_off}	Turn-off switching loss	[W]
P_{sw_on}	Turn-on switching loss	[W]
E_{OFI}	Turn-off switching loss	[J]
E_{ON}	Turn-off switching loss	[J]
v_T	On-state voltage of IGCT	[V]
v_F	On-state voltage of diode	[V]
v_{T0}	Threshold voltage of IGCT	[V]
v_{D0}	Threshold voltage of diode	[V]
r_T	Slope resistance	[mΩ]
V_{CE}	Operating voltage of semiconductor	[V]
V_{CC}	Maximum voltage defined from the energy loss curve	[V]
$t_{d(off)}$	Turn-off delay time	[ns]
t_f	Fall time	[ns]
$t_{d(on)}$	Turn-on delay time	[ns]
t_r	Rise time	[ns]
T_s	Heat sink temperature	[ºC]
T_c	Case temperature	[ºC]
T_j	Junction temperature	[ºC]

$R_{th(j-c)}$	Junction – case thermal resistance	[K/W]
$R_{th(c-s)}$	Case-heat sink thermal resistance	[K/W]
$R_{th(s-a)}$	Heat sink – ambient thermal resistance	[K/W]

Chapter 1

Introduction

1.1 Background to research project

In the last decade, research in the area of electric power systems has been driven by a number of global trends, such as fast-growing renewable energy industries and reduction strategies for carbon emission.

Power electronics conversion equipment plays a key role in providing technical solutions for many challenges associated with the improvement in efficiency and reliability of renewable energy sources, electrification of transport, and urban networks in modern electricity grids, especially with respect to the increasing penetration of renewable power generation and need for ensuring system reliability, security, and stability.

Today, at the medium voltage level, direct current (DC)-based electric power transmission and distribution applications are increasingly discussed as an alternative system to alternating current (AC) transmission networks. Moreover, DC-based distribution networks could help increase the power supply capacity in highly populated urban or industrial areas. Considering a future distribution network consisting of medium-voltage direct current (MVDC) technology, the MVDC grid

becomes a feasible support structure for greater penetration of dc end-use applications and for renewable energy integration. In distribution networks up to 66 kV, MVDC has more advantages in contrast to the conventional AC distribution structures. Within MVDC installations at a voltage level up to 40 kV (DC), compared to the 66-kV (AC) conventional ac network, the required components can be reduced. By using high-power DC-DC converters, a bulky conversional 50/60 Hz transformer can be replaced by medium-frequency transformers operating in the kilo-hertz range so that a considerable reduction in transformer weight/size can be achieved.

Regarding the current study and development activities in MVDC grids, the multi-megawatt scale isolated DC-DC converters are likely to interconnect the MVDC grids of different voltage levels. A number of potential structures for high-power DC-DC converters are surveyed in Section 2.3. They can be divided into the categories ‘galvanically isolated’ and ‘non-isolated’. The key research question concerning the design of high-power DC-DC converters is how existing advanced power electronics and transformer technology can be used to realise high-power conversion systems. Considering the multi-megawatt scale transformer, medium-frequency (typically in the range of 1 kHz to 10 kHz) operation significantly reduces the volume and weight of the converters.

In recent years, magnetic component technology has received considerable attention in power electronics converters owing to its ability to design small and efficient magnetic components for achieving high power density. In the present work, the focus is extended to the optimum design of a high-power and medium-frequency transformer for a three-phase dual active bridge DC-DC (3DAB) converter topology operating on soft-switching conditions. The specifications of the bidirectional 3DAB converter proposed in this work have been investigated using a target multi-megawatt design example. The design specifications are set as follows: The 3DAB converter comprises a low voltage (LV) port with the DC terminal voltage (1 kV ≤ $V_{in} \leq$ 5.5 kV; nominal voltage V_{in} = 1.1 kV or 5.2 kV) and a medium voltage (MV) port with the DC nominal terminal voltage V_{out} = 40 kV. A nominal output power P_{out} of 4 MW is required within the specified voltage ranges. An important design parameter to be defined in this work is the switching frequency, f_{sw}. Considering the higher switching frequency, the volumes of the transformers and capacitors decrease

with increasing switching frequency. Therefore, the power density of a converter can be increased by increasing the $f_{sw.}$ However, the conduction and core losses in the transformer increase owing to high frequency skin and proximity effects and the switching losses on the power semiconductors increase unless soft switching approaches are considered. Since the size reduction of the transformer in a high power DC-DC converter is limited by the level of DC-link voltage and switching losses and other mechanical considerations, the operating frequency in the AC link may be constrained to ≤ 1 kHz [135]. The switching frequency f_{sw} = 1 kHz was selected as the design parameter for the targeted power transfer owing to the expected low impact of skin and proximity effects on the conduction losses of the magnetic component and low impact of switching losses on the switching devices.

A design method that supports the selected converter topology and ensures it is optimised with respect to high conversion efficiency is proposed. The proposed design method considers passive components such as medium-frequency transformer and snubber capacitors. The study is focused on the design of the isolation transformer and medium voltage power electronics circuits with improved power density. Additionally, the design of the snubber capacitor ensures that the turn-off commutations in the 3DAB converter are minimised and extends the converter's ZVS range. Snubber capacitors are optimised in order to extend the ZVS operation within the specified voltage ranges. Further aims regarding the design of the 3DAB converter are as follows:

- Low converter volume with respect to high power density
- Transformer efficiency ≥90% with maximum efficiency of 97% at the nominal operating cases (V_{in} = 1.1 kV and 5.2 kV, V_{out} = 40 kV) within reasonable transferred power ranges ($0 \leq P_{out} \leq 4$ MW).
- Total converter efficiency ≥90% with maximum efficiency of 95% at nominal operating cases (V_{in} = 1.1 kV and 5.2 kV, V_{out} = 40 kV), within reasonable transferred power ranges ($0 \leq P_{out} \leq 4$ MW).

1.2 Objectives and contributions of the work

1.2.1 Objectives

This thesis addresses the design considerations for passive components of the 3DAB converter.

In phase-shift modulation, the dead time impact becomes significant on the current waveforms at hard-switching operation or when the current crosses zero during the dead time. Also, with the increase in the dead time, the performance of any control scheme will deteriorate. Furthermore, the calculated ideal phase-shift angle can be distorted by the dead time. Therefore, the phase-shift angle must be compensated in order to maintain the desired output voltage and power. A theoretical calculation of the dc conversion ratio as the influence of snubber capacitance with the compensated phase-shift angle corresponding to the dead time is introduced to investigate the ZVS areas with dead time effects.

The objective of transformer design optimisation is to seek a constrained minimum solution for low transformer manufacturing cost by optimally designing the transformer geometry parameters. Traditionally, transformer designers have had to rely on their experience to solve design problems. In early research, the designers attempted to reduce their judgement in favour of mathematical relationships [157]. However, the main problem is that of time consumption in transformer design. To address the problem, designers attempted to use computer-aided design techniques in order to reduce the time taken for mathematical operations in design procedures [158]-[159]. Only mathematical models are included in the computer programme to compile a flowchart of the transformer design procedure. However, it is not enough to find a solution that satisfies all the constraints of physical, electrical, and thermal data.

In this work, a new design optimisation method, using low free parameters (only five parameters: the number of turns on primary winding, current densities for primary and secondary windings, window area ratio, and core sectional area ratio), is introduced to set the transformer geometry optimally. In the proposed design, analytical formulations are computed using a computer-aided looping algorithm in an attempt to eliminate time-consuming calculations associated with reiterative

optimisation procedures. Especially for cores with non-liner materials, how to accurately and efficiently analysis the electrical parameters (currents and voltages on the both windings) is a challenging problem. The proposed design optimisation method is combined with a 2D finite element analysis (FEA). The FEA method enables simulation of all important design constraints of a transformer, both internal and external, including winding voltages and currents, core material magnetic saturation, temperature rise, and winding and core losses.

A detailed design procedure of medium-frequency three-phase transformer for a 3DAB converter is proposed for reducing the volume and weight of the converters and increasing the total efficiency for medium voltage and megawatt-rated systems. An optimisation procedure combined with FEA magnetic and power electronics circuit simulation is proposed and validated to determine the appropriate values for geometry parameters of the three-phase transformer and leakage inductance of the 3DAB converter.

Another objective of the research work is to select a converter topology that is able to fulfil the requirement specified in section 1.1. Furthermore, this work is aimed at making more information available on the operation of the selected converter topology and identifying appropriate design methodologies that would enable the converter to meet the target of the required high power DC-DC converter for MVDC applications within reasonable, medium operating voltage ranges and power ratings.

1.2.2 Contributions of this work

In this regards, the new contributions of this work can be summarized as follows:

- A compensated phase-shift modulation scheme corresponding to the dead time for 3DAB converter
- A transformer geometry design method, which uses low free parameters to eliminate time-consuming calculations associated with optimisation method of the given 3DAB converter

- An optimisation prodedure, which is combined with a 2D FEA and power electronics circuit simulation, to determine the appropriate values for three-phase MF transformer and leakage inductance of the 3DAB converter

Five scientific papers have been published during the course of this work:

- Y. S. Lee, G. Vakil, Alan. J. Watson, and Patrick W. Wheeler, "An Analytical Modeling and Estimating Losses of Power Semiconductors in a Three-Phase Dual Active Bridge Converter for MVDC Grids"*, IEEE Power and Energy Conference at Illinois (PECI 2017),* Illinois, 2017
- Y. S. Lee, G. Vakil, R. Feldman, Alan. J. Watson, and Patrick W. Wheeler, "A High-Power Dc-DC Converter based Dual Active Bridge for MVDC Grids on Offshore Wind Farms", *EPE2016-ECCE Europe, 18th European Conference on Power Electronics and Applications,* Karlsruhe, 2016.
- Y. S. Lee, G. Vakil, R. Feldman, A. Goodman, and P. Wheeler, "Design Optimisation of a High-Power Transformer for Three-Phase Dual Active Bridge DC-DC Converter for MVDC Grids", *Power Electronics, Machines and Drives (PEMD 2016), 8th IET International Conference on*, Glasgow, 2016.
- Y. S. Lee, G. Vakil, Alan. J. Watson, and P. Wheeler, "Design Considerations for A High-power Dual Active Bridge DC-DC Converter with Galvanically Isolated Transformer", *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.
- Y. S. Lee, G. Vakil, Alan. J. Watson, and P. Wheeler, "Geometry Optimisation and Characterization of Three-phase Medium Frequency Transformer for 10kVA Isolated DC-DC Converter", *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.

1.3 Chapter overview

Chapter 2 gives an overview on the potential MVDC applications of high-power DC-DC converters. The main units involved in MVDC distribution networks are

discussed and the benefits derived from the isolated high-power DC-DC converter technologies used for MVDC distribution networks are presented. Based on the findings of Chapter 2, the 3DAB converter topology is considered most promising for achieving the key performance requirements of the MVDC system.

In **Chapter 3**, the operating principle of the 3DAB converter is explained on the basis of symmetric operation conditions. This includes the steady-state converter model that facilitates basic analytical studies and allows for a simplified loss calculation for the converter. Moreover, an RMS current model of the 3DAB converter, based on piecewise modelling, is presented in order to calculate the losses in the most relevant components, i.e. high-power semiconductor switches and diodes (conduction and switching losses). In this chapter, the focus is extended to 3DAB converter topologies that operate on the ZVS scheme; these are validated using a simulation model based on a 40 kV(DC)/4 MW 3DAB converter. The design of snubber capacitor ensures that the turn-off commutations in the 3DAB converter are minimised and the converter's ZVS range is extended.

A systematic approach to the use of the snubber capacitor in medium-voltage/ medium-frequency operating conditions for the given converter is outlined. This work includes their influence on turn-off current levels, power characteristics, and ZVS operating range. An optimisation strategy for the standard control angle, based on the resonant snubber capacitor, which enables the extension of the converter's ZVS soft switching boundaries, is also analysed. In this chapter, a detailed lossless snubber circuit model for the 3DAB converter is developed, which includes the influence of the snubber capacitor on power transfer, turn-off commutations, and ZVS range of the 3DAB converter

Chapter 4 considers the high-power, medium-frequency transformer for application in the studied 3DAB converter. This includes a detailed geometry model of the three-phase transformer needed to parameterise the model and to develop the efficiency for the optimised transformer. This geometry model is used to calculate the copper and core losses. In the following step, a medium-frequency transformer design and optimisation is developed based on an assembled 10 kW/1000 Hz experimental transformer featuring a copper wire winding assembly. An experimental characterisation of a silicon steel laminated 1000 Hz transformer is

carried out under non-sinusoidal excitation. Using the excitation waveforms, the specific losses for the transformer used in the constructed converter are determined.

Chapter 5 presents the small-scale experimental prototype and the components used for the construction of the laboratory converter. Details of the gate drive circuit, passive components, and heat sink design are outlined. The structure of the digital control platform including the DSP, FPGA card, data acquisition card, and the fibre optic interface card are described. The implementation of the phase-shift modulation algorithm in the digital control platform is discussed.

In **Chapter 6**, the experimental results obtained from the prototype converter described in the previous chapter are presented. The obtained results are compared with simulation results from a simulation model using the PLECS simulation package. The developed prototype is used to validate the power losses of the proposed 3DAB design method, which includes the conduction and copper losses, switching losses, and transformer core losses.

Chapter 7 concludes the research outcomes of this work and summarises the potential for future work with the DC-DC converter concept.

Chapter 2

Medium voltage direct current Applications

In recent years, based on the development of HVDC technologies [1-12], medium voltage direct-current (MVDC) systems are starting to be considered as a new power distribution architecture for enabling the electrification of transportation systems such as automotive, railway, aircraft, and ships, as well as providing increased power quality in the urban distribution networks and micro-grids [13-42]. MVDC technology can enable the installation of large renewable resources such as wind and solar generation. MVDC grid collection configurations for large scale solar parks are proposed and analysed in [15]. In the proposed dc configurations, analytical loss models for various electrical components are developed. The study of [24] introduces a possible future MVDC distribution gird in urban areas with wind and solar parks to connect the distributed generation to the dc-power supply of future dc households.

The design and performance of high power electronics converters for large wind farms connected to MVDC grids [16] and [27]. Meanwhile, some protection and circuit breaker topologies have been reviewed for the dc fault protection in MVDC grids, as in [32] and [40]. In addition, MVDC systems can be used for distribution networks and renewable resources, corresponding to AC network voltages (11kV,

33kV or 66kV) without affecting short circuit levels. Due to continuous improvements in power electronics technologies such as semiconductor devices, passive components, control schemes, and application circuits at megawatt levels, MVDC grids have emerged as an alternative distribution infrastructure. In the renewable energy systems, MVDC can be employed as a robust flexible DC collection scheme for the interconnection of wind and solar generators [38] and [55].

Recently, MVDC distribution networks have been attracting global attention, particularly in Europe and China. For example the Wenchang MVDC platform project which was developed and provided by RXPE has been operating successfully [19]. In this project, two 4MVA converters with nominal voltages of 10.5kV AC and 15kV DC have been installed for the rectifier substation as shown in Fig 2.1.

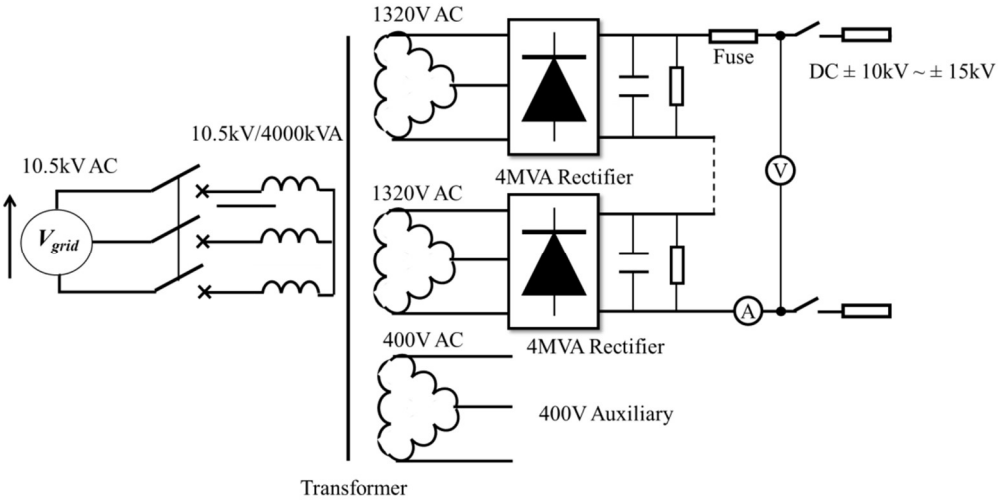


Figure 2. 1 An 8MVA /±15kV MVDC Rectifier Substation [19]

2.1 Advantages of MVDC Technology

DC systems have advantages over AC systems in long distance power utility networks (for example between the UK and mainland Europe [43-45]). References [1-4] present many of the advantages of DC grids such as low power losses and small size cable when carrying large amounts of power over long distances. In a DC system the cable capacitance is charged only when the cable is first energised or if the voltage level changes, this compares to AC systems where the cable capacitance

can generate a considerable amount of reactive power. Therefore DC systems are not affected by cable charging currents and no reactive power flows.

MVDC systems are becoming more and more feasible for applications in the distribution infrastructure within urban areas like industrial areas and also in small towns or cities [24]. Additionally, MVDC systems provide benefits for interconnections of large and small scale wind or solar farms as well as other forms of bulk and distributed power supply applications. Considering a future distribution network consisting of MVDC technology, the MVDC grid becomes feasible support for greater penetrations of DC end-use applications and for renewable energy integration [21]. In the distribution networks up to 66kV, MVDC has more advantages in contrast with that of the conventional AC distribution structures. Furthermore, increasing the medium voltage level of the MVDC distributions results in lower conducting currents, hence demand of higher conducting material and conduction losses can be avoided [34]. Thereby, overall efficiency is expected to increase due to minimized conducting materials. Overall, MVDC systems make better enhancement of existing interconnecting AC infrastructure and also provides enabled development of additional HVDC transmission systems. The advantages of MVDC technology are:

- Straightforward interconnection and improved efficiency for renewable energy integration
- Increased penetrations of DC loads and resources in urban areas
- Enhanced integration of the electrification of transportation systems such as railway, electric vehicle (EV)s
- Lower conduction losses in power delivery lines
- Increased efficiency in power delivery, generation, and applications

2.2 MVDC distribution networks

MVDC distribution networks can lead to more efficient systems capable of supplying higher levels of power into DC urban areas. This implementation of the MVDC concept in distribution networks also allows more penetration of large-scale power electronic interfaced renewable energy systems such as wind farms, solar

farms and energy storage systems. Only active power has to be fed in the DC networks, therefore the power transfer capacity and quality can be enhanced since there is no reactive current as in an AC system.

A typical layout of a MVDC is shown in Fig. 2.2. The layout integrates various renewable energy resources, including solar and wind farms, energy storage, railway substations, EV charging stations and other applications for MVDC interconnection. In addition, the MVDC distribution provides an additional interconnection between the existing HVAC grids and energy sources. The conversion blocks in this layout represent high-power converter topologies for interfacing the MVDC bus with associated power sources and loads. In general, the energy resources operate with an internal LVDC link which is interconnected with the AC grid. A high-power DC-DC converter converts the LVDC into various MVDC levels.

High-power DC-DC converters are the key component for the interconnection of different DC networks operating at different voltage levels. For example, boost converters serve to step-up the low DC voltage level or the MVDC levels are stepped down using buck converters. Furthermore, bidirectional power transfer controllability of the converter ensures high flexibility in the multi-terminal DC network.

In the following sections the detailed models that could be used for the MVDC distribution networks in urban areas are introduced, and high-power DC-DC converter topologies are compared.

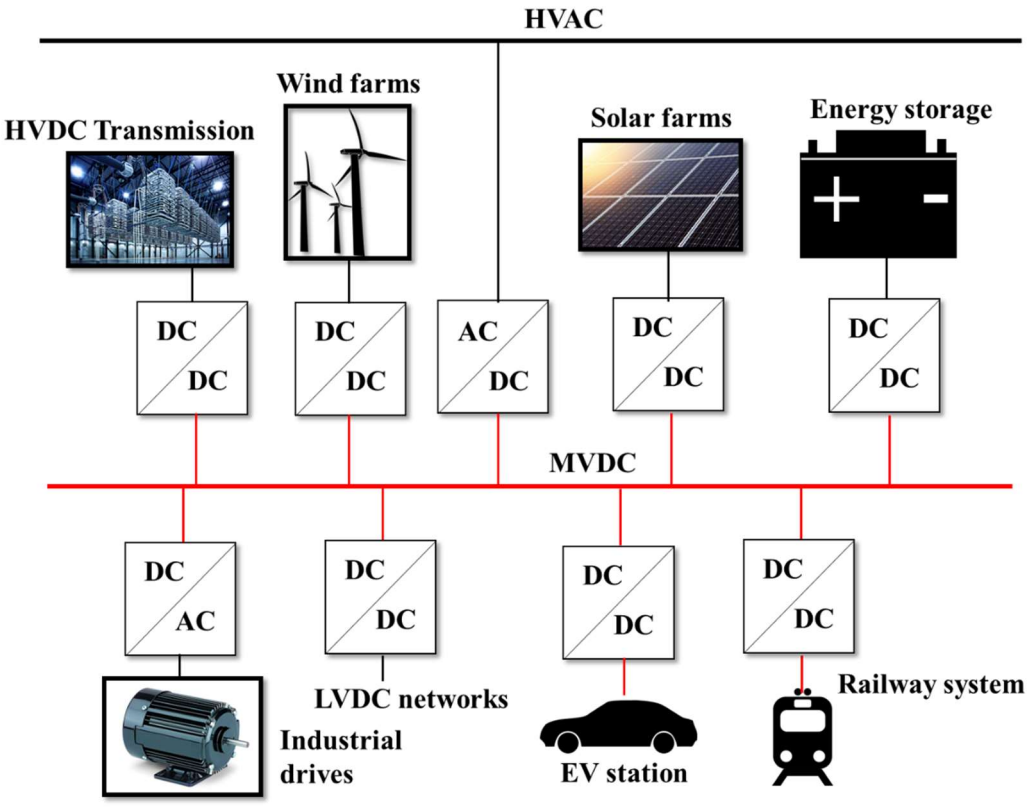


Figure 2. 2 A possible MVDC grid infrastructure in urban areas

2.2.1 DC collector grid for large wind farms

MVDC grids are particularly attractive for offshore applications such as offshore wind and ocean energy, supplying offshore oil and gas platforms, and supplying power to islands. For example, large offshore wind farms for DC grid connection have been evaluated in [2, 4]. By using centralised power conversion, the DC transmission converters control wind turbine speed. New strategies to use and control voltage source converter based multi-terminal DC transmission systems for connecting large offshore wind farms have been proposed in [8-10]. Recently 3–8MW large wind turbines have been developed, and these will be used for offshore farms [120]. Table 2.1 shows the specifications of several high-power generators for use in wind turbines, both in service and in development. Most of these generators are 690V AC rated because these three-phase generators are typically star connected and have 400V windings. Currently, 400VAC is the standard three-phase power supplies in Europe. Thus, square root of three times 400V equals 690V. However

these carry high-line currents of approximately 3.35kA for 4MW distribution networks, leading to high costs and high conduction losses in the power cables. An alternative solution is to use an MV generator. This technology has now been developed by two companies, ABB [46] and GE [47] (3.3kV AC rated).

Table 2. 1 High Power generators for wind turbine

Manufacturer	Model	Type	Rated power	Voutput
Gamesa [121]	G128-4.5MW	PMSG	4.5MW	690V AC
Gamesa [121]	G128-5.0MW	PMSG	5.0MW	690V AC
GE [47]		PMG	4.0MW	690 ~ 3.3kV AC
SIEMENS [122]	SWT-4.0-120	asynchronous	4.0MW	690V AC
SIEMENS [122]	SWT-8.0-154	PMG	8MW	690V AC
ABB [46]		asynchronous	up to 5MW	690 ~ 3.3kV AC
ABB [46]		PMG	up to 7MW	690 ~ 3.3kV AC
GOLDWIND [123]	GW 100/2500	PMSG	2.5MW	690V AC
Doosan [124]	WinDS3000	PMSG	3.0MW	690V AC

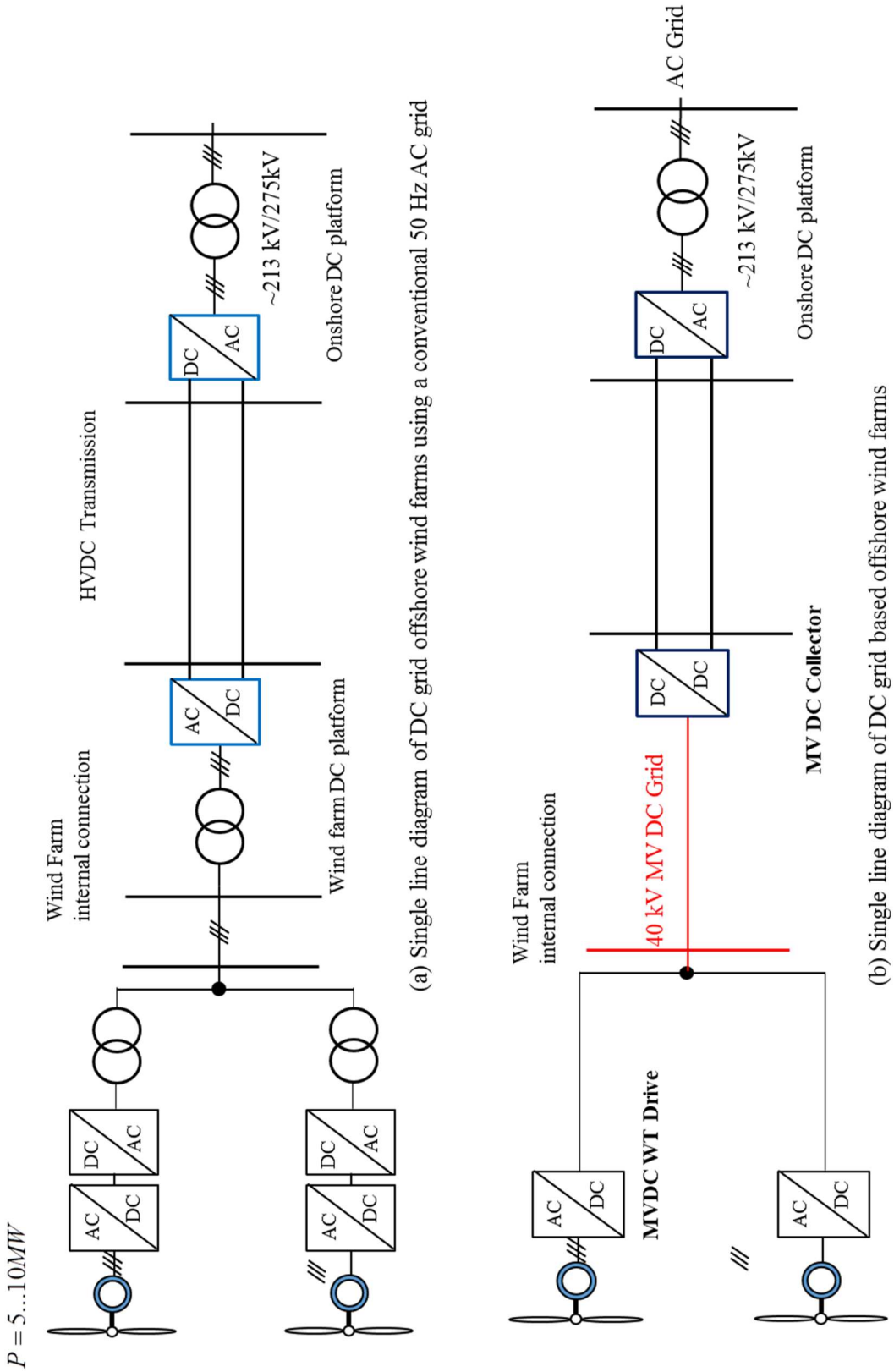


Figure 2. 3 Single line diagram of DC grid offshore wind farms

Fig. 2.3 shows offshore wind energy conversion systems for long-distance HVDC transmission. In offshore wind farms using a conventional 50Hz AC grid, the wind generator is connected to a back-to-back voltage source converter (VSC). Fig. 2.4 shows a PMSG system with back-to-back VSC [48-50].

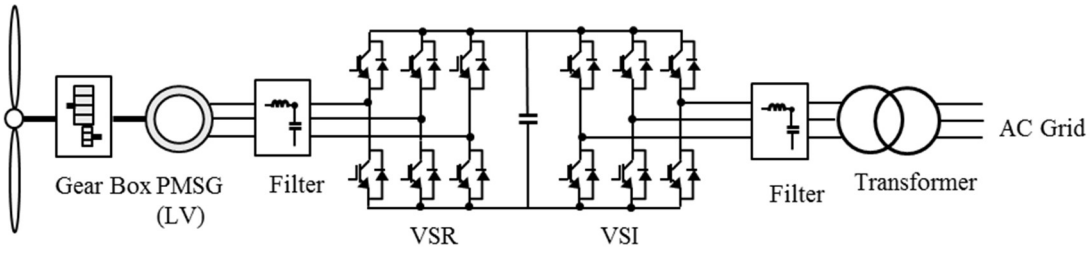


Figure 2. 4 Configuration of PMSG with back-to-back VSC.

The voltage source rectifier (VSR) is controlled using a PI controller such that the *d*-axis current is held to zero, to obtain maximum electrical torque with minimum current. A maximum power point tracking (MPPT) technique is used to determine the optimum rotor speed for each wind speed in order to obtain maximum rotor power. In contrast, the voltage source inverter (VSI) controls the line current. The DC-link voltage can also be controlled using a PI controller, via the VSI. The output voltage of the back-to-back VSC is transferred over a short distance through the transformer. The output power of several turbines can be collected and transferred to an offshore wind farm DC platform. A high power AC-DC converter with a bulky 50Hz step-up transformer is often used as a point of common coupling to step up the voltage from the distribution to the transmission level. Finally, the power is fed into the grid through the onshore converter.

Fig. 2.3(b) shows a proposed 40kV MVDC grid-based offshore wind farm [80]. In this configuration a MVDC wind turbine converts the output terminal voltage of the wind turbines to the MVDC collection voltage of up to 40kVDC, as shown in Fig. 2.5. Then a DC/DC converter boosts the MVDC voltage to the voltage required by the HVDC transmission line.

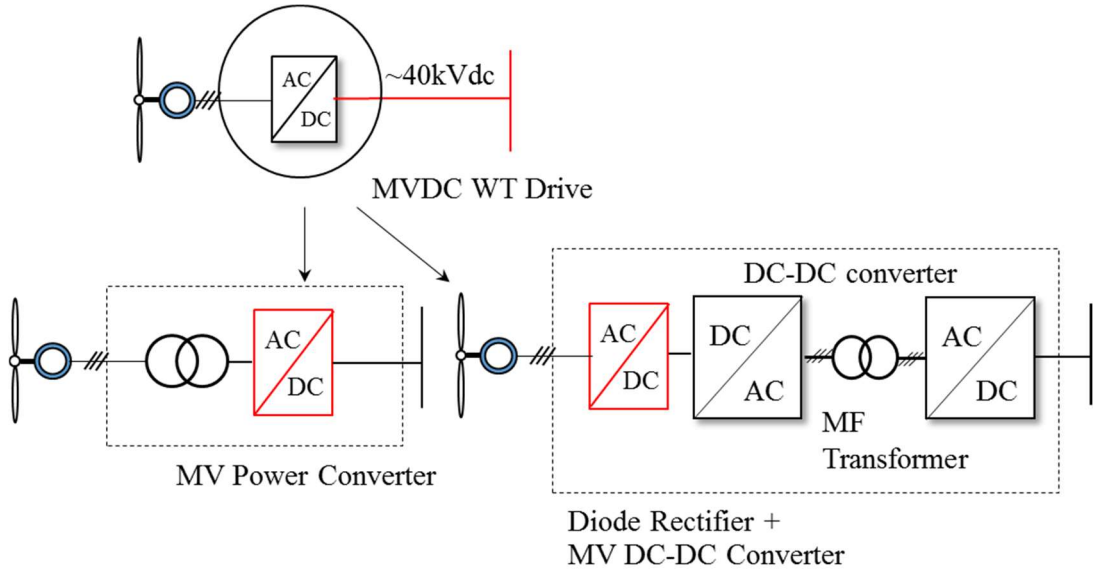


Figure 2. 5 MVDC wind turbine drive for MVDC girds

A circuit comprising of a rectifier and dual active bridge (DAB) DC-DC converter has been considered for the wind turbine drive since it can handle higher levels of power and provide galvanic isolation [27]. The use of this conversion system can replace the large, bulky conventional 50Hz transformers, thereby reducing the size of the system as well as increasing the efficiency. In addition, the DC grid can provide economic benefits using multi-terminal DC (MTDC) grids which utilise an offshore DC network [30]. A DC-DC converter gives good control over the DC network and simplifies the operation of multiple converters on the same DC grid.

In a conventional AC grid the internal connection network is based on low frequency transformer technology. This solution gives the system controlled voltage and a near constant frequency. However, the power converters are not usually optimised for the utilisation of the flexible AC grid. Therefore, additional line filters are required in order to synchronise the conversion unit to sinusoidal AC voltage, and these filters also lead to extra losses and investment costs. Secondly, as a rule, the conventional 50Hz AC grid involves an extremely large components, for example, transformers. A heavy and bulky transformer obviously becomes an important consideration for investment costs in offshore wind farms. In contrast to this, the transformer in the DC offshore wind farm system is replaced with a DC-DC converter with a higher operating frequency of over 5kHz, and low-cost conversion

units. Compared with the AC system, a power conversion efficiency saving of 5% can be achieved [16] leading to significant overall cost reductions.

2.2.2 DC collector grid for large solar farms

Large solar farms use a large-scale photovoltaic (PV) system which has been developed for the supply of renewable power to the electricity grid at a scale of at least one megawatt. Today, the largest solar park has a capacity of 850 megawatt-peak (MWp) in China [51]. In typical solar farms, centralised inverters with a relatively high capacity, in the order of 250kW or above, convert the PV array's DC output to LVAC, with voltages up to 600VAC.

The utility grid connection is a three-phase system with bulky step-up transformers with typical operating frequency of 50–60Hz. Recently, possible DC grid connection frameworks for large-scale solar farms have been investigated [15,52-54]. The primary features of the DC connection scheme are its reliability, fault protection, locality and capacity of connections to the MVDC distribution networks [15, 24]. The DC collector bus bar also needs to be connected to an existing utility grid within a few kilometres of the solar farm. In the following sections two configurations of the conventional AC and DC collector grids are described.

- **Conventional AC configuration**

The most common configuration of the electrical system for large solar farms for AC grid connection is shown in Fig. 2.6. This system consists of many PV subsystems, which comprise a multitude of PV modules for delivering DC power into centralised PV inverters. Centrally installed PV inverters are implemented to convert DC power generated from the PV strings into AC power and to feed this power into the AC grid.

To maximise the conversion efficiency, these inverters also perform maximum power point tracking (MPPT) to keep each PV string close to its peak power point [125]. To enable greater power delivery, several inverters can be connected in parallel [126]. A three-winding design of the transformer enables the connection of

two inverters with galvanic isolation. Moreover, the three-winding transformer is the optimal link between centralised inverters and the medium voltage alternating-current (MVAC) collector grid and gives considerably reduced fault current levels [127]. The total power generated by the centralised inverters is collected at the MVAC bus bar. Finally, the total power may be fed to the MVAC distribution networks or stepped up to HVAC level using an MV/HV high power transformer for transmission over long distances.

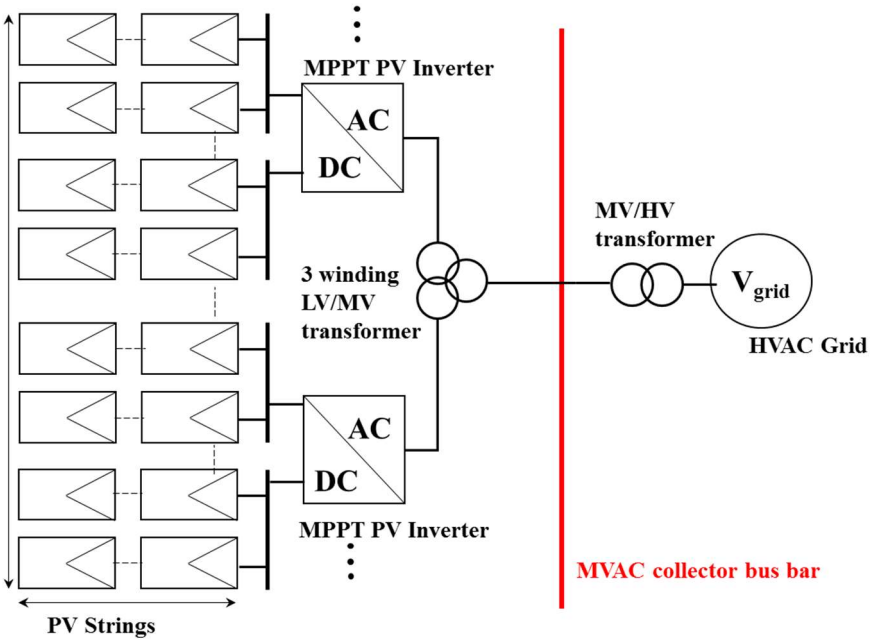


Figure 2. 6 Conventional AC configuration

- Possible DC configuration

A possible DC electrical system configuration is shown in Fig. 2.7. The installation of a high-power DC-DC converter with an input voltage of up to 1500V enables significant system cost reductions for large solar farms due to fewer string junction boxes and less wiring [15]. MPPT algorithm is performed within the PV subsystems by the DC-DC converter, which operates to boost the DC voltage level [55, 56]. The output power from these converters is collected using an MVDC bus bar and fed to the MVDC distribution grids. Alternatively, the collected power may be inverted to the MVAC system using a single large-scale centralised inverter [57].

Eventually, the voltage level can be stepped up using an MV/HV transformer to allow coupling to the HVAC transmission line. In the DC configuration, resistive losses are the only loss phenomenon in the DC cables. In contrast, dielectric losses corresponding to charging capacitance and sheath losses add to the resistive losses in the AC configuration.

Reference [15] presents a comparison of the losses in these two system configurations. According to this work, the DC configuration (which achieves an efficiency of 97.9%) performs better than the AC configuration (with a 96.3% efficiency).

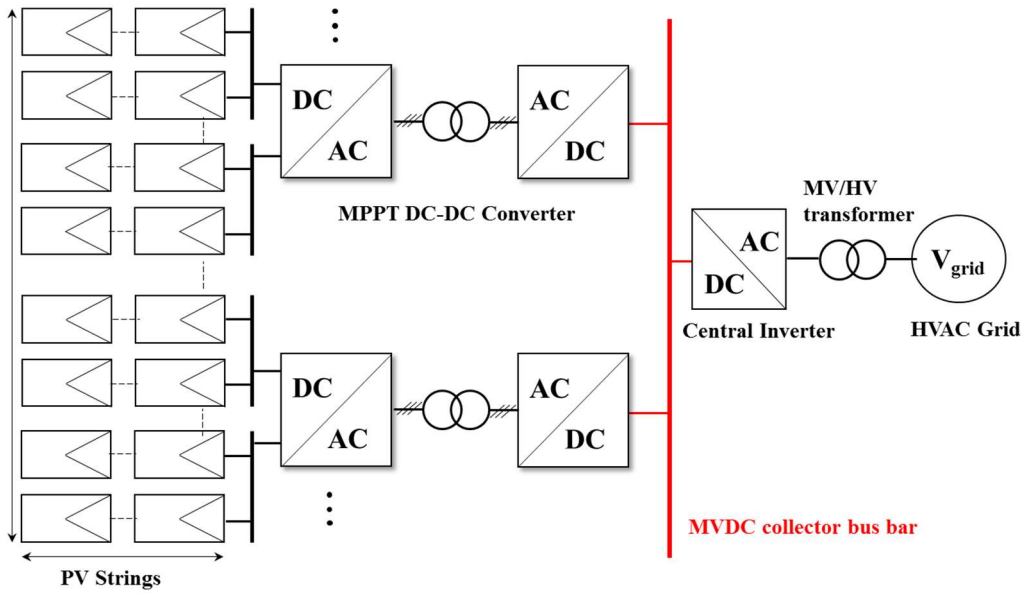


Figure 2. 7 Possible DC configuration

2.3 MVDC urban electrified public transport

The MVDC electrical system is an attractive solution for electrified public transport [24,25,28,29,58]. For example, with an MVDC supply, railway substation systems for trams and metros can be operated with lower peak power demands, more efficiently and with higher reliability [25]. In addition, the installation of MVDC infrastructure can be optimally utilised within a fast EV charging station for cars [29,59,60]. The fast charging station has typically several level 3 fast charging units

(50-70kW) that can be supplied by the MVDC system. The fast charging unit can fully charge a vehicle within 20 to 50 minutes [29].

2.3.1 Railway substation

Conventional railway systems are normally connected to MVAC grids via substations which rectify the AC voltage level into a DC voltage that feeds the catenary line [128]. The DC voltage supplied to the catenary at a relatively high voltage of up to 3000 V, with a ±20% tolerance. A drawback of MVAC-based systems is problematic harmonics generated by the diode rectifier. In contrast, a power converter only generates distortion at the switching frequency harmonics in the MVDC grid.

Recently several megawatt, three-phase, dual active bridge (3DAB) DC-DC converters [75, 78, 80] have become attractive topologies for MVDC-supplied railway substations, an example is shown in Fig.2.8. The 3DAB DC-DC converter provides galvanic isolation from the MVDC line to the LVDC line. The galvanic transformer enables the use of soft switching control, which can dramatically reduce the switching losses in the semiconductor devices. Moreover, this 3DAB converter-based railway substation enables bi-directional power flow. Hence, the transferred power can be fed back into the MVDC distribution network. The recuperated power can then be used to serve other loads such as an EV charging station or variable frequency drive. The recuperated electric energy also can be stored in energy storage systems and resupplied when there is insufficient demand in the grid [60].

In the MVAC grid, the installation of more reactive power compensation and bulky filters is needed to integrate the renewable energy sources and energy storage systems into the supply for a railway system. Conversely, no reactive power is needed in the MVDC grid. Thus, the replacement of a rectifier substation by a 3DAB converter-based substation can increase the total system efficiency.

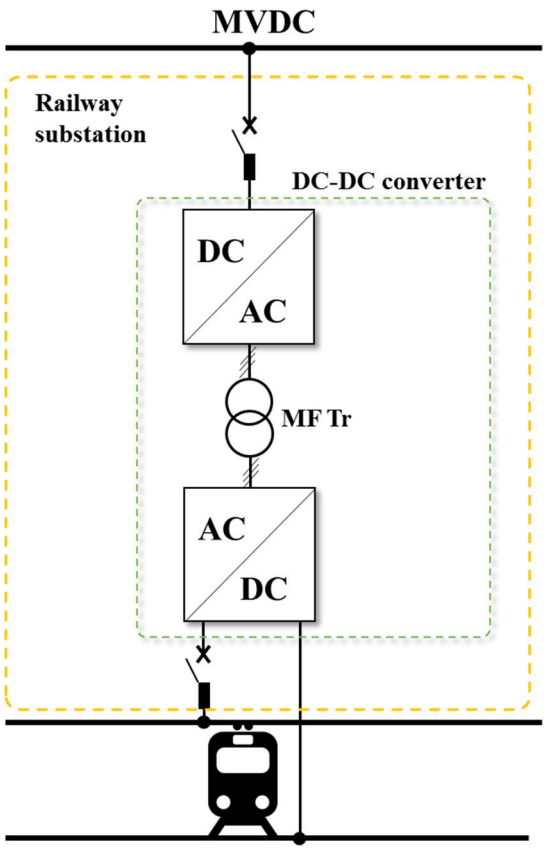


Figure 2. 8 An urban railway substation using a MVDC distribution network

2.3.2 EV charging station

In recent years, numerous studies have attempted to design EV technologies for mobility applications based on their promise of zero emissions [61]. However, EVs are yet widely implemented for commercial use due to the lack of public charging infrastructure. Most EVs can be plugged in on private property for overnight charging, but the number of charging points are limited at highway service areas or university campus sites. In MVDC grids, public charging stations are likely to be extended to urban areas. The MVDC can also offer the possibility of DC fast charging in less than an hour [60]. The concept of a MVDC grid-supplied EV charging station is shown in Fig. 2.9. This system consists of one high-power 3DAB converter and individual off-board battery chargers to provide a regulated DC-DC conversion [60 ,61, 66].

An off-board charger for an EV typically operates with a DC voltage of up to 1000V. This type of charger needs to handle power levels of up to 100kW [29]. Using a bidirectional dc-dc converter, chargers can enable the isolation of circuits from the supply grid and support the injection of battery energy back to the grid [61]. The 3DAB converter is suited to the operation of a DC fast charging station and can increase the charging capabilities of EV chargers. Therefore a multi-megawatt 3DAB converter station could handle of a large number of EVs at the same time, as shown in Figure 2.9.

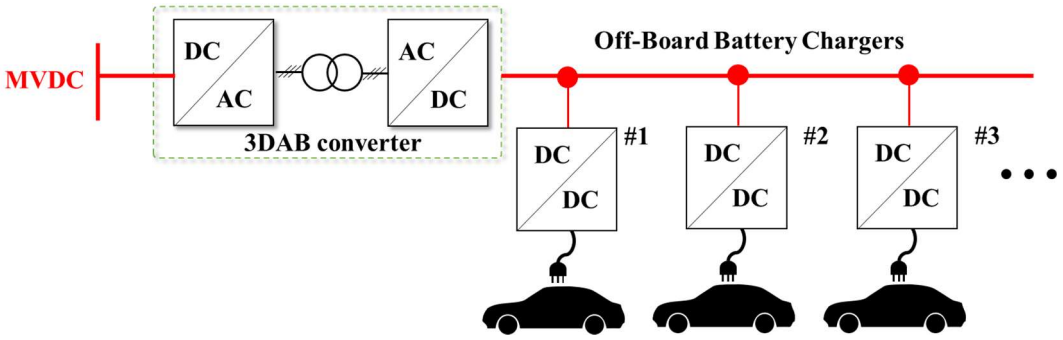


Figure 2. 9 Possible EV charging station

2.4 High power DC-DC converter topologies

High-power DC-DC converters are one of the primary technologies needed for interconnections with MVDC grids. High-power DC-DC converters must provide galvanic isolation between the MVDC line to the LVDC line for safety reasons, breaking ground loops of the two electric circuits by preventing a zero-sequence current circulating between the two circuits. Using a galvanic transformer linked by magnetic flux, the voltage difference can safely be specified in kilovolts without the risk of breakdown. Galvanic isolation is also required to enable the series or parallel connection of several converter modules in modular power converter arrangements. Many DC-DC converter topologies have previously been presented in various fields such as the automotive industry [62,66], urban railway substations [25,28,68], renewable energy sources [38,56], and DC grid collectors [22,31,38,54]. These

power converter topologies can be divided into the categories of 'isolated' and 'non-isolated'. Some of the suitable converter topologies are given in Table 2.2.

Table 2. 2 Candidates for High-Power DC-DC Conversion Applications

Converter topology	Characteristics	Example
Series Resonant converter	Galvanic isolation, unidirectional power flow	[67]
Single-Active Bridge	Galvanic isolation, unidirectional power flow	[68]
Modular Multilevel DC converter	Non-isolation	[69]
Single-Phase Dual-Active Bridge (1DAB)	Galvanic isolation, bidirectional power flow, alternative modulation schemes are required	[64]
Three-Phase Dual-Active Bridge (3DAB)	Reduced current ripple, Higher transformer utilization	[70]

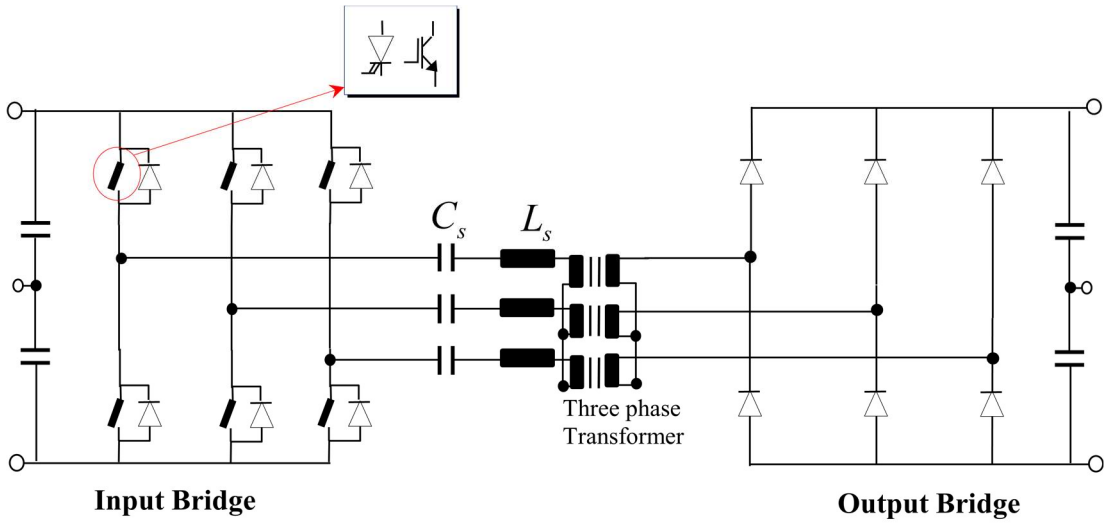


Figure 2. 10 Basic schematic of three-phase series resonant converter

A multi-megawatt three-phase series resonant converter was introduced in [67]. Fig. 2.10 is the diagram of a three-phase series resonant DC-DC converter with unidirectional power flow capability that can be used in high-power applications. The converter consists of an active bridge at the input, a medium-frequency

transformer, and a passive diode rectifier at the output. Resonant capacitors are connected in series to the ac-linked lines. Owing to its location in the AC-link current path, a sizeable ripple current would be expected in the resonant capacitor. Also, the resonant capacitor carries the full load current. Despite the unidirectional power flow due to the diode bridge at the output, the converter offers high efficiency and low cost for higher power levels. In comparison to a single-phase series resonant converter as show in Fig. 2.11, the three-phase converter has lower ripple current in the DC-link capacitors and also the core size of the transformer can be reduced if it is implemented as a three-phase unit.

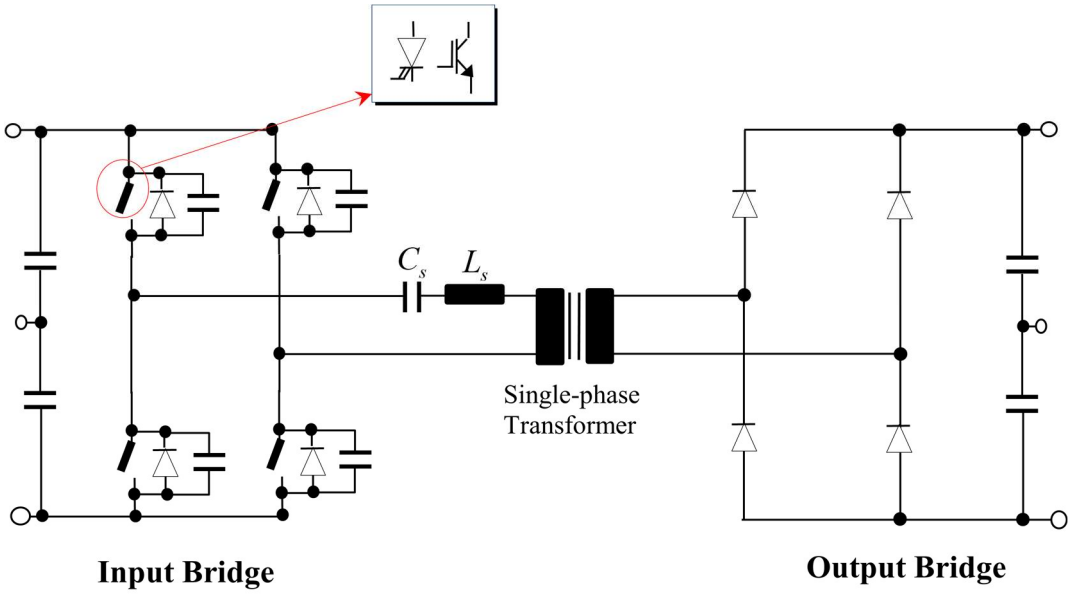


Figure 2. 11 Basic schematic of single-active bridge converter

Similarly, a single-active bridge converter [68] as shown in Fig. 2.11 employs an active bridge at the primary side and a passive bridge at the secondary side with a magnetically isolated component. Soft-switching is achieved with snubber capacitors and switching losses are kept low with the soft-switching for a wide load and voltage range. However, the single-active bridge is limited to only the unidirectional power flow.

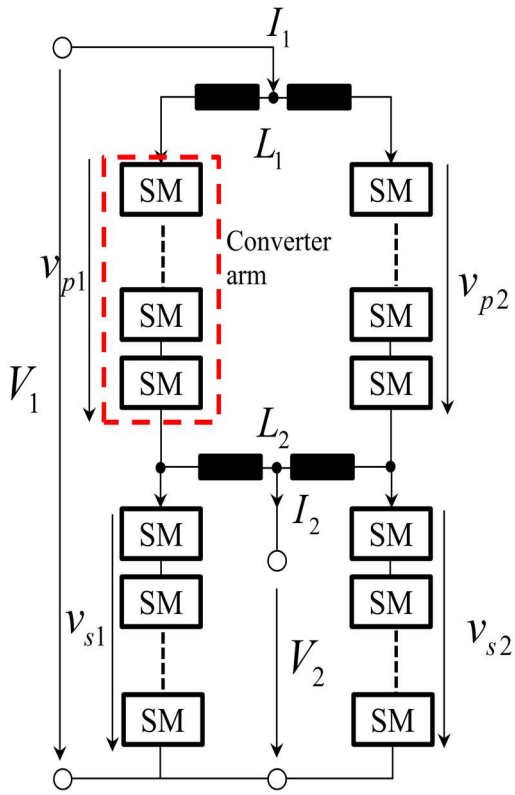


Figure 2. 12 Schematic of a modular multilevel topology

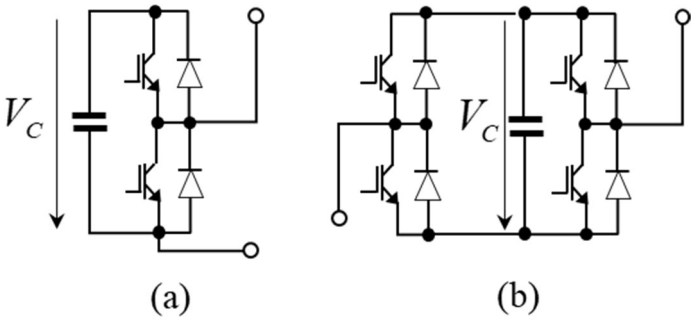


Figure 2. 13 Schematic of sub-modules (SM): (a) unipolar SM and (b) bipolar SM

A non-isolated modular multilevel (MMC) topology for DC-DC converter was introduced in [69]. Fig. 2.12 shows the push-pull MMC dc-dc converter presented in [69]. Each phase arm contains several submodules connected in series. The submodules consist of an active half bridge or full bridge and a capacitor bank as shown in Fig. 2.13. The main advantage of the modular multilevel topology is that the converter can continue operation even when a submodule has failed. Furthermore,

the operating voltage levels can easily be adjusted by changing the number of submodules. However, the drawback of the topology is that the required capacitance of the submodules is inversely proportional to the operating frequency of the converter [69]. Additionally, transformer-less operation may lead to poor utilisation at the high-voltage level and low efficiency with circulating reactive power in the AC link. In [69], on comparison of the push-pull MMC and 3DAB converter, it was found that the amount of required filtering at the ac port is similar to that in an equivalent multi-modular 3DAB converter. Thereby, this topology may not be feasible in medium- and high-voltage applications.

Recently, single-phase dual active bridge (1DAB) converters [64] have been suggested for automotive or aerospace applications. Fig. 2.14 shows the schematic of a 1DAB converter with bidirectional power flow capability.

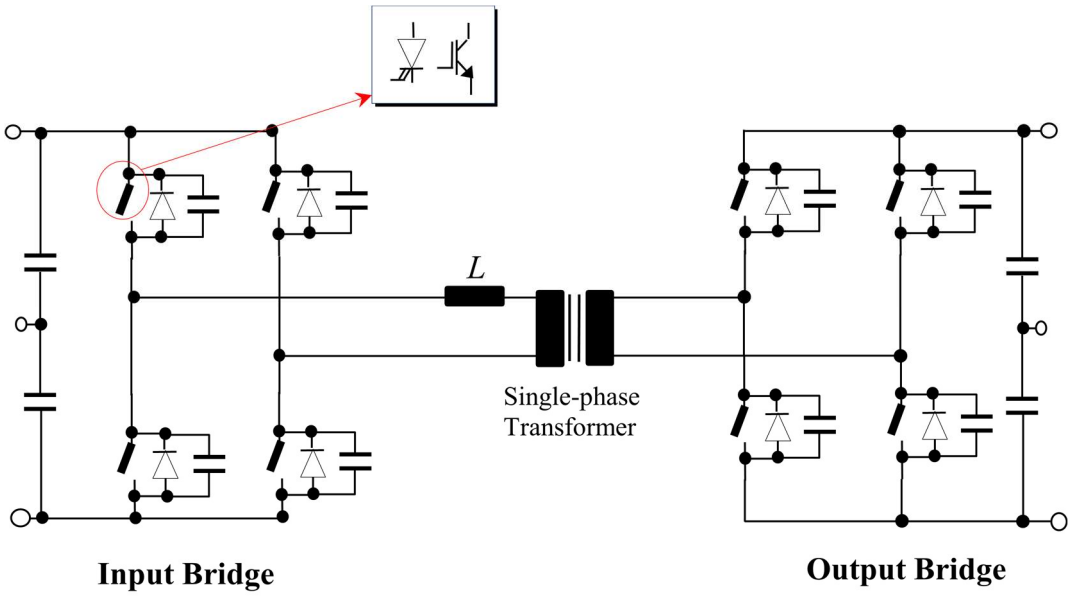


Figure 2. 14 Basic schematic of single-phase dual active bridge converter

The 1DAB topology offers a wide operating range with a low voltage and high current output. With different modulation schemes [129], zero-voltage switching (ZVS) can be improved for a wide operating range and the converter efficiency can be increased. However, the high output currents lead to a high output filter volume. This substantially limits the applicability for higher power applications.

The drawback can be reduced by the extension to a three-phase dual active bridge (3DAB) topology. In [129], a detailed comparison of both topologies is presented with respect to performance and volume. The required output filter size of the 3DAB is significantly lower compared to the 1DAB's single-phase layout. Compared to 1DAB, good overall performance is achieved with the 3DAB converter: low total apparent VA rating of the transformer, low power electronic switch VA ratings, and a low passive energy storage capability due to considerably smaller RMS currents. However, the major drawback of the 3DAB converter is that asymmetric leakage inductance of the three-phase transformer leads to unbalanced phase currents [111]. Consequently, it leads to more current ripple in the DC-link capacitors. Furthermore, the 3DAB converter has significantly lower efficiencies at low load operating points than the 1DAB converter.

Recently, the DAB DC-DC converter with modular multilevel converter (MMC) structure was proposed [160-167]. This topology is best suited for high-power handing and high-voltage DC transformers for the HVDC network with DC operating voltage of up to 800 kV (pole-to-pole). Fig. 2.15 shows a 3DAB converter configuration that employs MMC (3DAB-MMC) with a medium-frequency transformer in the AC link.

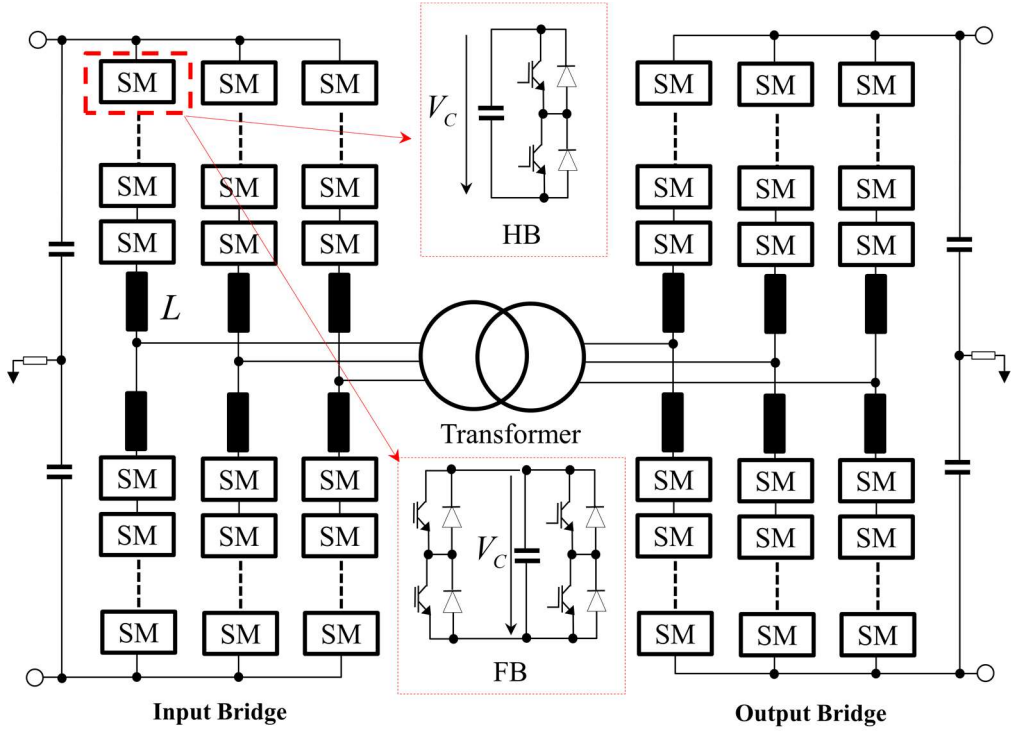


Figure 2. 15 3DAB converter based on MMC structure (3DAB-MMC)

Basic operation principle of the 3DAB-MMC can be explained using a sub-module in each bridge. Each phase-leg of the bridge comprises upper and low arms, each consisting of N (the number of cells) half-bridge or full-bridge cells, as shown in Fig. 2.15. Using full multilevel modulation with sinusoidal voltage, the AC link of the 3DAB-MMC can be operated similar to that used in the ac terminal of the HVDC link. Each arm supports the DC-link voltage (V_{dc}), so the voltage across each cell capacitor (V_c) must be maintained around $V_c = V_{dc}/N$. Also, the full modulation index range can be made available for voltage control in the AC link of the 3DAB-MMC during DC faults. The main advantage of the MMC operation is that of the low switching losses and voltage stresses (dv/dt) on the transformer of the 3DAB-MMC compared with its two-level 3DAB converter. However, the topology does not fully utilise the active powers associated with specific low-order harmonic voltages and currents [167]. Therefore, the 3DAB-MMC is expected to have lower power density than the 3DAB converter. Additionally, full utilisation of soft switching operation as in the DAB configuration is not expected. Only some devices will turn on and off at the ZCS condition. Also, the 3DAB-MMC utilises many switching devices for both low- and medium-voltage side converters.

Similar to the 3DAB converter, the use of a medium-frequency transformer of the 3DAB-MMC is not only beneficial for reduction of the transformer size in the AC link but also leads to overall reduction in the size of MMC cell capacitances and arm reactors. Although the use of medium frequency in the AC link may lead to a compact design of passive components, the 3DAB-MMC operation with low modulation index during a dc fault will increase the loading stress on the cell capacitors. Therefore, cell capacitance must be oversized to limit cell capacitor voltage ripple and avoid defecting switching devices from increased voltage stress.

It is necessary to use an interfacing transformer for galvanic isolation in high power DC-DC converter topologies scalable to high-voltage [136]. In this manner, circulating reactive power in the AC link is minimised when the primary and secondary bridge DC-link voltages are significantly different. However, without a transformer, a DC-DC converter with different primary and secondary side DC voltages may suffer from relatively high losses due to excessive circulating reactive power.

Given the focus of this study on transformer design for MVDC (≤40 kV) and a multi-megawatt (4 MW) system, a 3DAB converter is selected as the study model although 3DAB-MMC is well suited for DC-DC converters for HVDC networks (≤800 kV). This is because better utilisation of the magnetic material of the transformer and switching devices can be realised for the low-voltage side converter (≤5.2 kV). However, the proposed design optimising methodology can be utilised in dc-dc converters based on MMC structure in further work.

2.5 Summary

This chapter presented an overview of possible future medium-voltage DC-based power distribution applications. Interesting fields of application include medium-voltage DC-based power transmission grids and distribution networks, offering potential advantages for urban power networks associated with various renewable energy generation systems and loads.

One particularly promising application of a multi-megawatt scale DC-DC conversion system is the efficient electrification of large-scale renewable energy sources for medium-voltage DC collector access points. With respect to the DC-DC converters, all surveyed DC-DC converter platforms require multi-megawatt and tens to hundreds of kilovolt ratings. Furthermore, successful converter developments will need to be galvanically isolated from the medium-voltage point to the low-voltage point for safety reasons.

To meet the requirements of multi-megawatt and tens of kilovolt applications, a three-phase dual active bridge DC-DC (3DAB) converter has been introduced as the most promising topology for high achievable conversion efficiency.

Chapter 3

Three-phase dual active bridge DC-DC (3DAB) Converter

3.1 Introduction

A 3DAB converter, suitable for high-power applications, was studied in [70] and the results of the simulation and experimental work using the converter are presented in [71]. The proposed 3DAB converters operate in the symmetric six-step switching mode with a 50% duty cycle for each of the phase legs. The three-phase legs operate with a 120° phase-shift from each other at the switching frequency. The 3DAB converter is also suitable for bi-directional power flow and buck-and-boost converter applications in which the transformer has a different turns ratio. A current-fed topology for the 3DAB converter has been proposed in [73] to improve the efficiency of a wide operating range. However, the drawback of the topology is that a large DC inductor is required to lower the primary side current ripple compared to the voltage-fed topology.

The proposed new combined modulation of the 3DAB with triangular and trapezoidal control can be optimised to overcome the poor performance at low load conditions.

Recently, design considerations for multi-megawatt scale converters have been studied [75-80]. In [78], a 2.2-MVA prototype was introduced. Dynamic control strategies for the 3DAB have recently been introduced [81-83]. One of key components of the 3DAB converter is a high-power galvanic transformer that enables isolation from the MV line for safety reasons and also allows for soft-switching control, which can dramatically reduce the switching losses. [114] presents a detailed design optimisation of a three-phase transformer for a 4-MW large-scale step-up 3DAB converter. In order to validate the core losses under non-sinusoidal excitation, the improved generalised Steinmetz equation (iGSE) [130] is used.

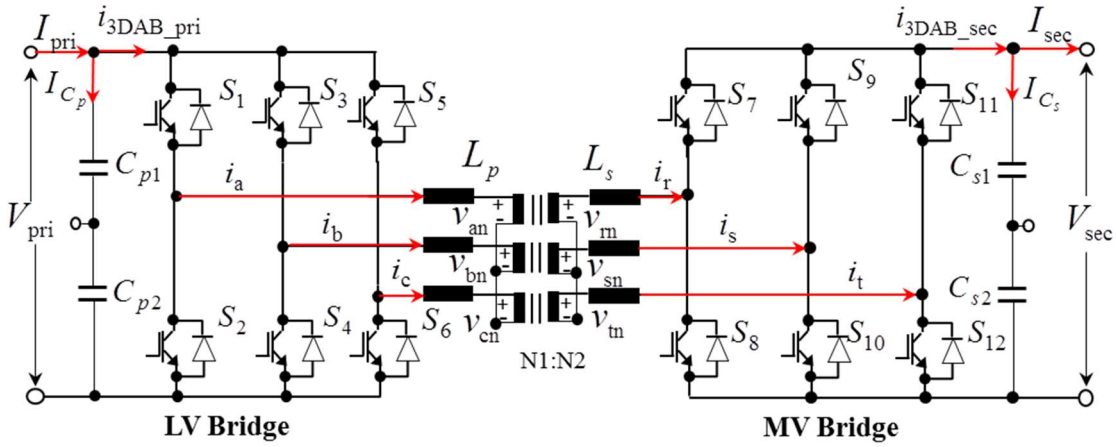


Figure 3. 1 A 3DAB converter topology

The topology of the 3DAB converter is shown in Fig. 3.1. The 3DAB converter has the advantages of higher power capability and smaller passive filters than the single-phase dual-active bridge (1DAB) type [62-66]. The 3DAB converter has two active voltage-sourced bridges that are magnetically connected using a medium-frequency (MF) transformer. The 3DAB converter uses three half bridges on the LV side and another three half bridges on the MV side. The primary side bridge converts the DC input voltage into a medium-frequency AC voltage that is applied to the MF

transformer; the voltages at the secondary terminals of the transformer are then rectified by the secondary side bridge.

The 3DAB converter is operated with a symmetric phase-shift (SPS) modulation scheme with a duty cycle of D = 50%. Detailed discussions on the modulation and the converter layout criteria for a focus on high-power applications are outlined in [1-3]. In [72], a novel asymmetrical duty cycle method has been introduced. The 3DAB converter can also be operated using ZVS soft switching with a wide range of operations while the switches are turned on with zero voltage across them. Various modulation schemes have been proposed and compared in [74, 137-144] to improve the efficiency at partial load conditions of the 3DAB converter. Accordingly, two current shapes, the triangular current mode (TRI-CM) and trapezoidal current mode (TRAP-CM) are feasible [139, 140, 141-144]. Both modulation methods are considered efficient for ZCS achievement without circulating currents. Also, a considerable advantage is that the description for the TRI-CM and TRAP-CM can be expressed with simple equations, which make them easy to implement in a control scheme. For the 3DAB converter, characteristic operational areas of SPS and TRI/TRAP-CM are shown in Fig. 3.2. It can be seen that the boundaries for TRI/TRAP-CM operation are below the boundary for hard-switching areas of the SPS modulation. Therefore, a strategy for the TRI/TRAP-CM operation is to compensate for hard-switching operation areas of the SPS modulation. This strategy can be implemented to increase the efficiency of the existing 3DAB converter. However, it can be seen that the maximum power for TRI/TRAP-CM operation is significantly lower than that for SPS modulation. Additionally, SPS modulation covers a substantially wider operating area than the TRI/TRAP-CM modulation as shown in Fig. 3.2. Slightly lower RMS values of the phase currents are achieved at high power in combination with the DC conversion ratio 'd' around one with SPS modulation, while other modulation methods perform better at lower power levels and high or low DC conversion ratios. The RMS value is related to most resistive losses within the switching devices and also the transformer winding, so its minimisation is an important efficiency optimisation strategy in the investigation. Overall, SPS operation is advantageous in terms of minimisation of RMS current at high powers with 'd = 1'. On the other hand, TRI/TRAP-CM operation performs better at lower powers with higher or lower ratios.

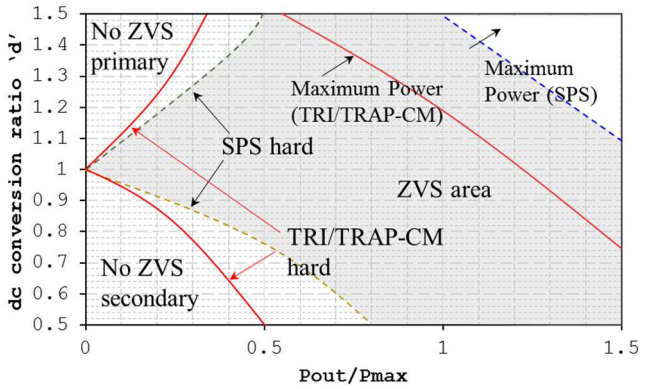


Figure 3. 2 Characteristic operational areas of the 3DAB converter for SPS and TRI/TRAP-CM

For SPS modulation, the capacitor currents I_{Cp} and I_{Cs} show comparably low RMS values and amplitudes. Overall, the reduced filter harmonics and RMS currents achieved with SPS modulation are the key advantages for the 3DAB converter design.

These modulation modes have a substantial impact on the transformer design, in particular for the 3DAB converter. Several comparisons of the given modulation methods are presented in [140, 146-149]. The advantages of the 3DAB converter with SPS modulation are particularly found in transformer volume and output filter. Regarding transformer size, SPS modulation has a slight advantage over TRI/TRAP-CM operation with the 3DAB converter owing to the lower core volume.

Given the scope of this thesis, the SPS modulation strategy was considered for an optimal design strategy because the design of a 3DAB converter for wide voltage and power ranges can be challenging using only SPS operation [135-136]. In this thesis, a design and optimisation assessment of the three-phase transformer is carried out. For the 3DAB transformer design, SPS operation leads to a smaller core size, which is the result of the lower mass of the transformer. Consequently, the SPS operation has a slight advantage over the TRI/TRAP-CM operation for the 3DAB converter design with respect to the transformer size owing to the lower core volume.

3.2 Modelling of 3DAB Converter

3.2.1 Lossless fundamental 3DAB Converter

Here, the steady-state operation of a 3DAB converter is described. In order to simplify the analysis, the transformer can be replaced by its leakage inductor and the voltage-sourced primary and secondary side bridges can be replaced by their fundamental components, as shown in Fig. 3.2 [70]. For simplicity, only a single phase is considered.

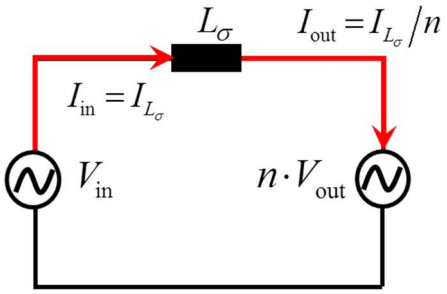


Figure 3. 3 Fundamental model of the 3DAB Converter

n is the turns ratio of the transformer. The steady-state inductor current is calculated by:

$$I_{L_\sigma} = \frac{V_{in} - n \cdot V_{out}}{X_{L_\sigma}} \tag{3.1}$$

where, $X_{L_\sigma} = j\omega_{sw} L_\sigma$.

The RMS fundamental values of input and output voltage are given as:

$$V_{in_rms} = \frac{2\sqrt{2}V_{in}}{\pi}, \; v_{out_rms} = n \cdot \frac{2\sqrt{2}V_{out}}{\pi} \tag{3.2}$$

where, V_{in} and V_{out} are peak amplitudes of input and output voltage. Hence, the output power is calculated by:

$$P_o = V_{\text{out}} \cdot i_{L_\sigma} = \frac{V_{\text{in_rms}} \cdot n \cdot V_{\text{out_rms}}}{\omega_{sw} L_\sigma} \sin(\varphi) = \frac{V_{\text{in_rms}}^2}{\omega_{sw} L_\sigma} d \sin(\varphi) \tag{3.3}$$

where, $d = n \frac{V_{\text{out_rms}}}{V_{\text{in_rms}}}$ is DC conversion ratio of the 3DAB converter.

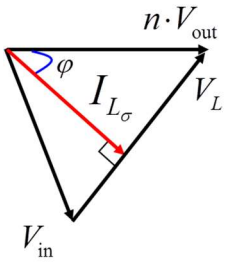


Figure 3. 4 Phasor diagram for the fundamental model

Phasor diagrams for the fundamental model can be helpful to appreciate the relationship between the phase-shift angle φ and DC conversion ratio d for the soft-switching condition. Fig. 3.4 shows a phasor diagram for the fundamental model for d =1. The secondary side voltage is leading the primary voltage by the φ and the inductor current is perpendicular to the voltage difference. In [70], in the ZVS condition, the inductor current, I_{L_σ} lags the input voltage and leads the output voltage. The ZVS analysis strategy in this thesis has been verified by simulation investigation using balanced three-phase coupling networks that were built using symmetric inductances with a transformer's turn ratio of 1:2. The input voltage is set to 500 VDC and the output is 1000 VDC. As shown in Fig. 3.5, the ac voltage is in six-step mode with discrete levels of $\pm V_{pri}/3$ and $\pm 2V_{pri}/3$. A ZVS switching transition occurs for the primary bridge when the phase current i_a is negative, as shown in Fig. 3.5 (a). In the ZVS condition, the active semiconductor devices turn on under zero voltage when the anti-parallel diodes are conducting. As seen in Fig. 3.5 (b), for the secondary bridge, a ZVS turn-on occurs when the phase current i_r is positive.

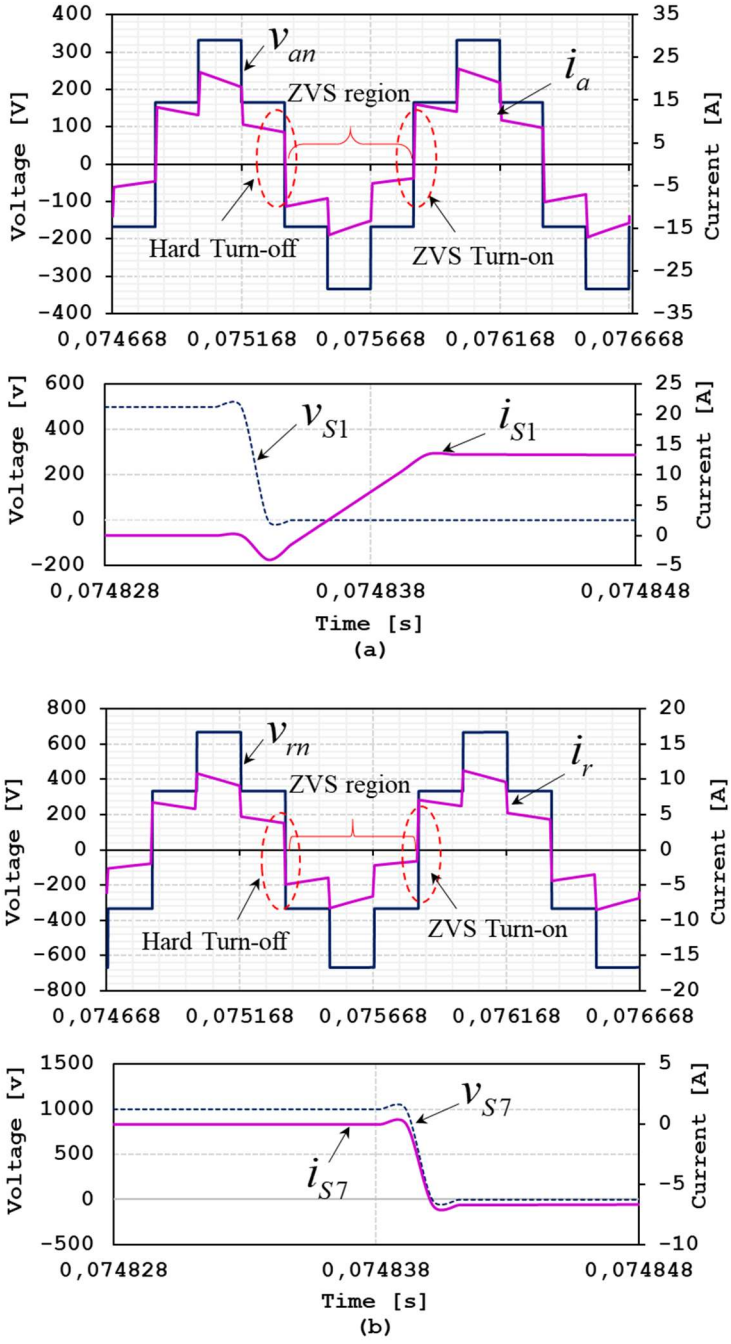


Figure 3. 5 Simulation waveforms with SPS modulation: (a) primary bridge and (b) secondary bridge

3.2.2 Analysis of steady-state model

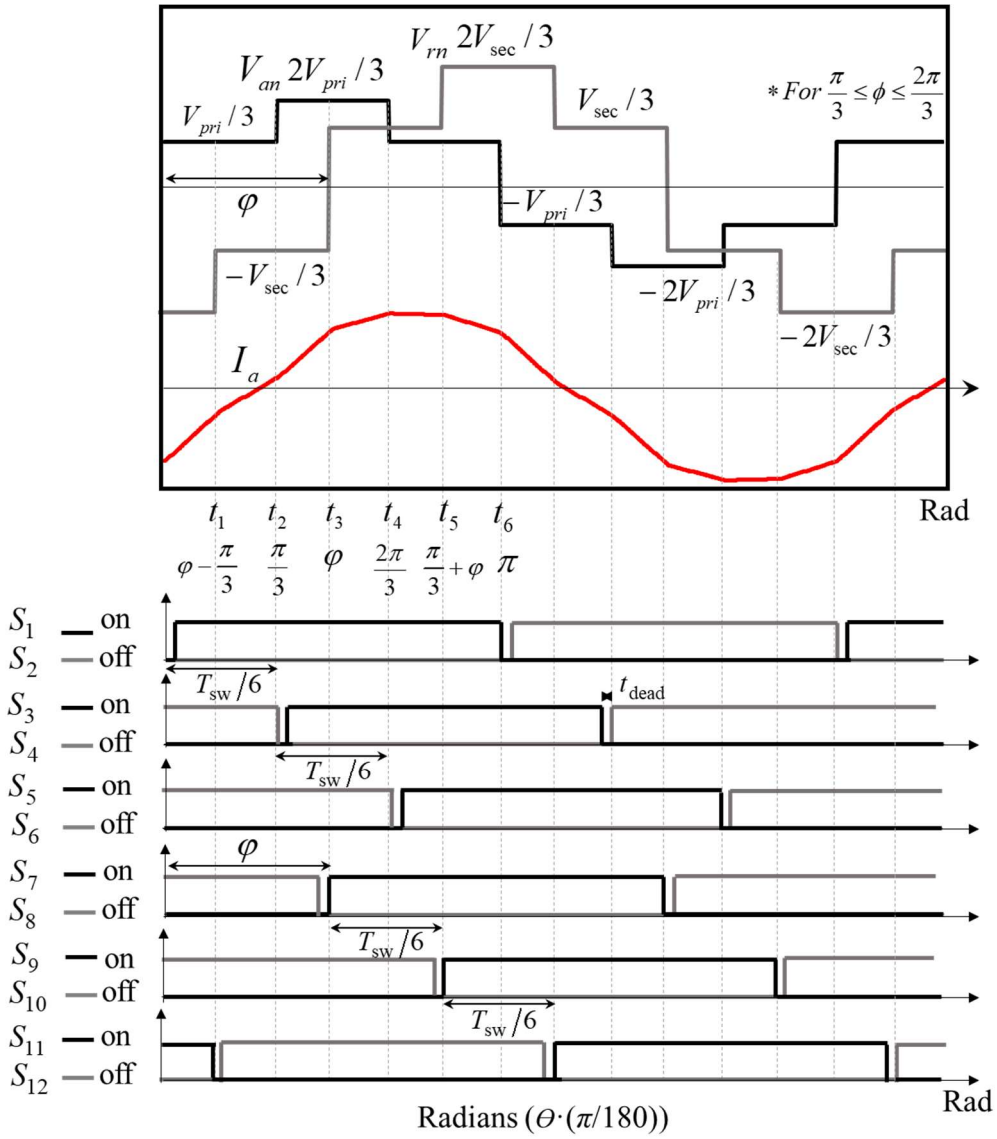


Figure 3. 6 Characteristic waveforms in the 3DAB converter and respective gate signals inclusive dead time intervals.

Fig. 3.6 illustrates the resulting typical waveforms in the 3DAB converter in the case of a boost application, where the magnitude of V_{rn} is higher than that of V_{an}. The notations refer to the circuit diagram in Fig. 3.1. The characteristic waveforms of the voltage and currents of the 3DAB converter are depicted with SPS modulation. A phase-shift angle of φ is introduced, which controls the power flow between the voltages applied at the primary and secondary terminals of the transformer. The

piece-wise linear description of the phase current i_a is introduced using the phase-shift angle and a duty cycle of D = 50%. The three half bridges of each side are operated with a phase-shift of 120°. For example, the second leg switches S3 and S4 are delayed by 120° with respect to the half bridge (S1 and S2) for phase 'a'. The third leg switches S5 and S6 lag by 240°. This operation creates a six-step voltage for the phase voltages. Each of the six voltage steps has a duration of $T_{sw}/6$.

Fig. 3.7 shows the Y-Y connection model of the transformer of the 3DAB converter. Since the phase current is inversely proportional to the leakage inductance, the symmetric inductance will lead to balanced phase current. To simplify the analysis, a reduced transformer model, as shown in Fig. 3.7 (b), is used in the following calculations. The magnetising inductance and winding resistance are neglected and only the leakage inductances are considered. The phase voltages differ compared to the Y-Y connection model. Hence, an impedance variation between the phases of ±5% can be considered.

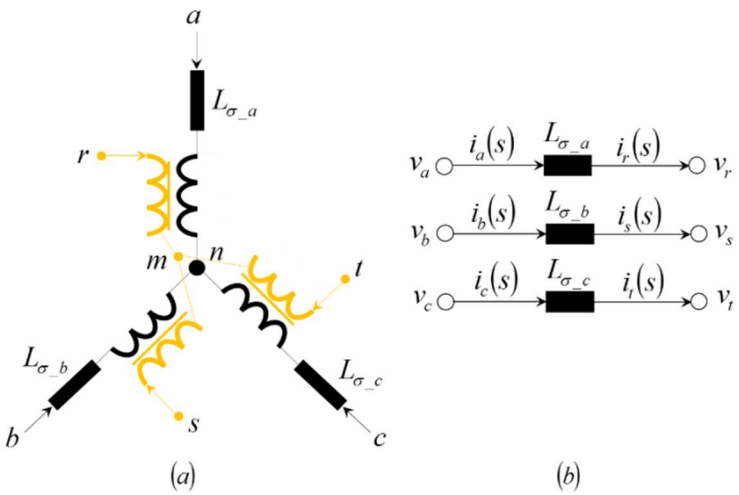


Figure 3. 7 Transformer connection type: (a) Y- model and (b) simplified equivalent model

Piecewise analytical characteristics of the transformer current waveform at each time interval of the switching period can be found in Appendix A. Using the piecewise linear description for the 3DAB, shown in Appendix A, the transformer

currents of primary $i(0)$ and secondary $i(\varphi)$ windings for steady-state analysis can be calculated as:

$$\begin{aligned} i(0) &= \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[\frac{2}{3}\pi d - d\varphi - \frac{2}{3}\pi\right] \qquad \text{for} \left(0 \le \varphi \le \pi/3\right) \\ i(0) &= \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[\pi d - 2d\varphi - \frac{2}{3}\pi\right] \qquad \text{for} \left(\pi/3 \le \varphi \le 2\pi/3\right) \end{aligned} \tag{3.4}$$

$$\begin{aligned} i(\varphi) &= \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[\frac{2}{3}\pi d + \varphi - \frac{2}{3}\pi\right] \qquad \text{for} \left(0 \le \varphi \le \pi/3\right) \\ i(\varphi) &= \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[\frac{2}{3}\pi d + 2\varphi - \pi\right] \qquad \text{for} \left(\pi/3 \le \varphi \le 2\pi/3\right) \end{aligned} \tag{3.5}$$

where, $\omega_{sw} = 2\pi \cdot f_{sw}$ is the switching frequency, L_{σ} is the leakage inductance of the transformer, and $d\left(= n\frac{V_{\text{out_rms}}}{V_{\text{in_rms}}}\right)$ is the DC conversion ratio of the 3DAB converter. The output power characteristics of the 3DAB converter for values of φ between 0 and 120º are given by:

$$P_o = \frac{V_{pri}^2}{\omega_{sw}L_{\sigma}} \cdot d \cdot \varphi\left[\frac{2}{3} - \frac{\varphi}{2\pi}\right] \quad \text{for} \left(0 \le \varphi \le \pi/3\right) \tag{3.6}$$

$$P_o = \frac{{V_{pri}}^2}{\omega_{sw}L_{\sigma}} d\left[\varphi - \frac{\varphi^2}{\pi} - \frac{\pi}{18}\right] \quad \text{for} \left(\pi/3 \le \varphi \le 2\pi/3\right) \tag{3.7}$$

Equations (3.6) and (3.7) are calculated for positive phase-shift angles. At negative angles, the direction of power flow is reversed. Output power characteristics versus φ for both forward and reverse power flow are shown in Fig. 3.8 using *d* as a parameter. The per-unit (p.u) results are normalised to the base power. In this case, 4 MW is considered the base value for power. Using (3.6) and (3.7), the base value of power can be calculated by:

$$P_{base} = \frac{V_{pri}^2}{\omega_{sw}L_{\sigma}} \tag{3.8}$$

For the base value of 4-MW power and using a nominal voltage of 4 kV (DC) for the input bridge side of the 3DAB converter, the base inductance can be calculated. During forward flow, the input side bridge leads the output side bridge. In the reverse mode, the output bridge leads the input side bridge. For d = 1, it can be seen that full control range under soft-switching is achievable, giving control from zero power for $\varphi = 0$ to maximum power for $\varphi = 90$; hence, 'd =1' is usually chosen as the optimal design point.

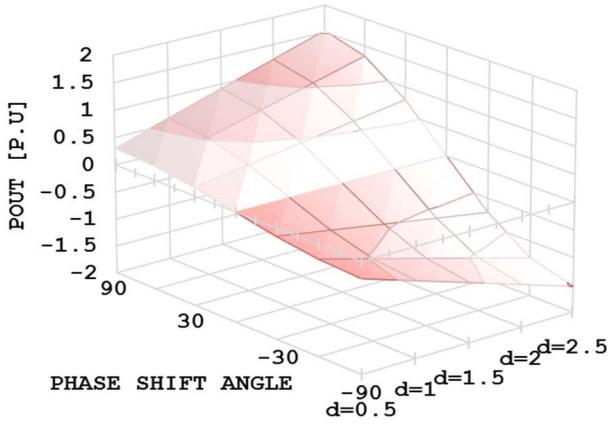


Figure 3. 8 Output power with different values of φ and d

3.2.3 Soft-switching ranges

To derive the soft-switching manner of the primary bridge, $i(0)$ needs to be negative so that current flows through its anti-parallel diodes for ZVS at turn-on. For the secondary bridge, $i(\varphi)$ needs to be positive so that its diodes are conducting at turn on of the corresponding switches. The input bridge boundary for this operation mode can be calculated according to the equation A.13 in Appendix A, $i(0) = 0$:

$$d_i = \frac{1}{1-\frac{3\varphi}{2\pi}} \quad \text{for } \left(0 \le \varphi \le \pi/3\right)$$
$$d_i = \frac{1}{\frac{3}{2}-\frac{3\varphi}{\pi}} \quad \text{for } \left(\pi/3 \le \varphi \le 2\pi/3\right) \tag{3.9}$$

Where, d_i is the DC conversion ratio of the input bridge for soft switching boundary. Similarly, the output bridge boundary can be calculated according to the equation A.14 in Appendix A, $i(\varphi) = 0$:

$$d_o = 1-\frac{3\varphi}{2\pi} \quad \text{for } \left(0 \le \varphi \le \pi/3\right)$$
$$d_o = \frac{3}{2}-\frac{3\varphi}{\pi} \quad \text{for } \left(\pi/3 \le \varphi \le 2\pi/3\right) \tag{3.10}$$

Where, d_o is the DC conversion ratio of the output bridge for soft switching boundary. Fig. 3.9 plots the variation of output power as a function of φ with different values of d. The input bridge and output bridge boundaries enclosing the soft switching area are shown the figure. For d =1, it can be seen that the input and output bridges can operate in the soft-switching region with φ enabling overall ranges from zero to full power rating.

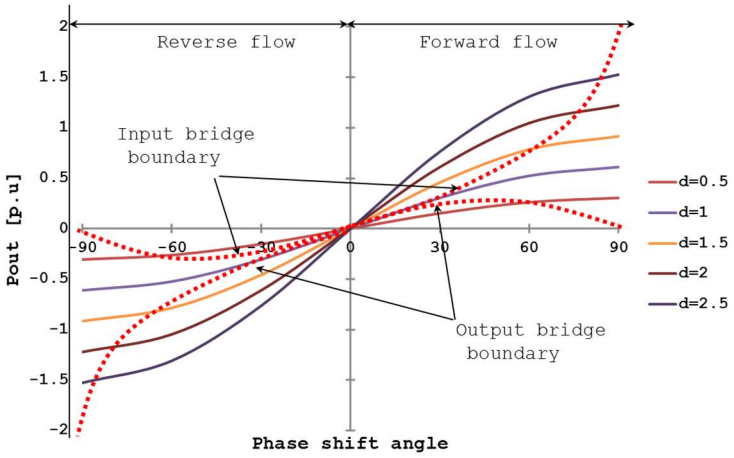


Figure 3. 9 Output power versus φ, with d as parameter of the bidirectional power flow characteristics and calculated soft-switching boundaries.

3.3 Lossless snubber circuit's influence on 3DAB converter

In the 3DAB converter, different switching conditions (hard and soft-switching) can be considered to characterise the switching transition. Generally, ZVS refers to a switching transition during which the voltage across the switch is zero or close to zero. More specifically, this ZVS has been defined for a turn-on process in voltage-source converters [169,170] because the anti-parallel diode conducts the current of the transformer and then the switch is gated on. For the ZVS, the voltage of the switch has to decay to zero before the switch is turned on. The switch cannot be triggered by itself at the ZVS turn-on, so on-switching losses occur as the voltage is nearly zero. On the other hand, hard switching happens for turn-off processing. During turn-off, the voltage of the switch is initially built up before the current decays. In the hard-switching transition, the overlapping area of the voltage and current leads to switching losses. The switching transitions of the ZVS snubber circuit are depicted in Fig. 3.10 with a relevant snubber circuit. The ZVS snubber can limit the dv/dt during turn-off, corresponding to the hard switching with an external snubber capacitor. Without the snubber capacitor, the turn-off process corresponds to the hard switching. However, the snubber capacitance influences the overlapping area of voltage and current; therefore, switching losses can be reduced.

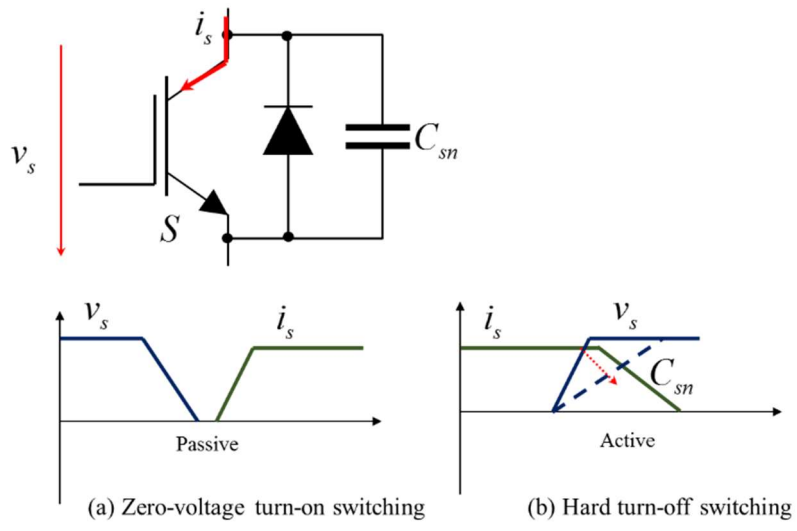


Figure 3. 10 Hard and soft-switching commutations with ZVS snubber circuit

In ZVS operation, turn-on losses are eliminated and turn-off losses are significantly reduced. Furthermore, a reduced dv/dt rate can be beneficial to a series connection of power semiconductor devices. Since the stored energy in snubber capacitors is not dissipated, the installation of lossy resistors is unnecessary. This is an advantage over the conventional RC turn-off snubber, where the stored energy is dissipated in a resistor [170]. Furthermore, the low-side parallel-connected snubber capacitor is switched on while the high-side snubber capacitor is recuperated before the parallel-connected capacitor is fully discharged.

3.3.1. Snubber capacitor commutations

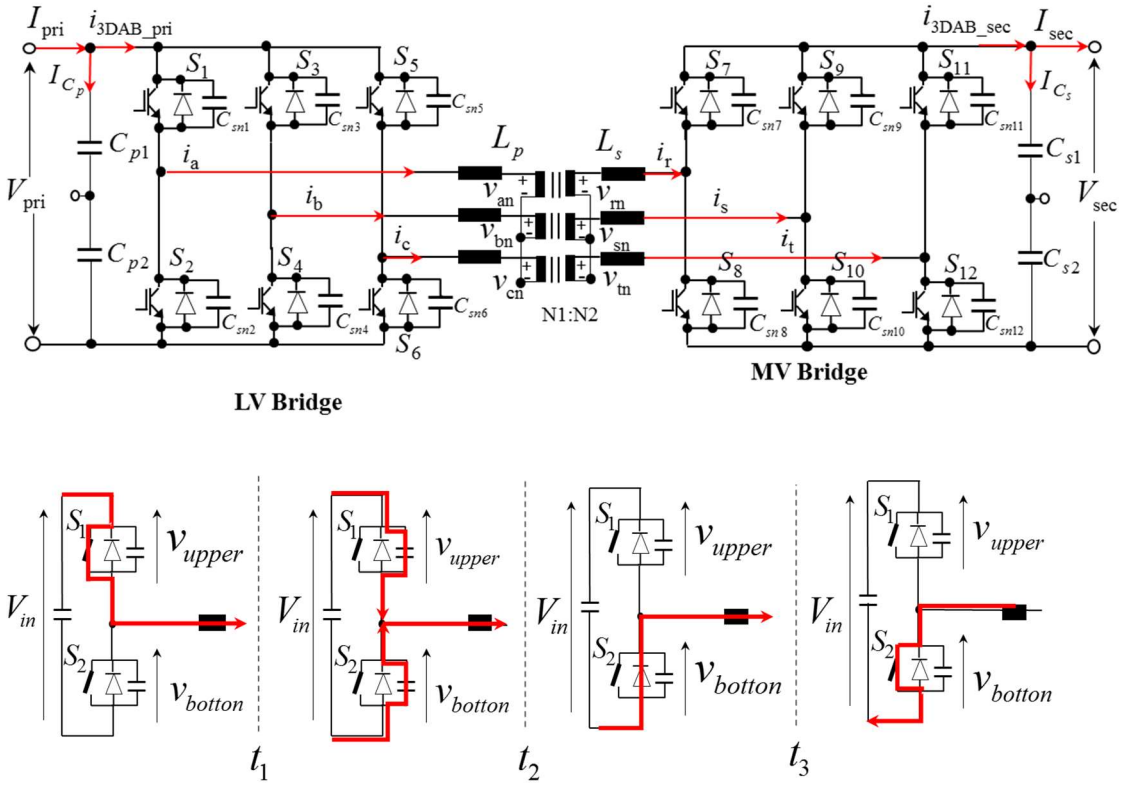


Figure 3. 11 Commutation in a half-bridge of a 3DAB Converter

The general commutation characterising of ZVS operation of a 3DAB converter half-bridge with lossless snubber capacitors is illustrated in Fig. 3.11. In the case of a high-voltage system, a series connection of several switches per switch branch is required to meet the connected high DC-link voltage. The snubber capacitor is

connected in parallel to each power semiconductor switch. A brief description is given in the following:

- At the beginning of the commutation cycle, the upper switch S_1 is turned-on. Assuming the S_1 is in the on state from the upper diode interval, the S_1 is conducting the switched current.
- At t_1, the high-side switch S_1 is switched off. The turn-off of the current forces the load current to commutate entirely to the upper and lower snubber capacitors.
- At stage (t_1 - t_2), the upper snubber capacitor begins to charge while the bottom capacitor starts to discharge. The dv/dt slope on the switch is determined by the size of the leakage inductance of the transformer, which is large enough to maintain the output current, and by the size of the snubber capacitor during the commutation. Furthermore, if the size of the snubber capacitor is sufficiently large, the switch current will have decreased rapidly until it reaches zero during the increase in the power semiconductor voltage. At the time, the turn-off losses are significantly reduced compared to the hard-switching operation.
- At t_2, the lower snubber capacitor is fully discharged. Afterwards, the lower anti-parallel diode becomes forward biased and takes over the phase current. Hence, the conducting current of the diode flows into the leakage inductance of the transformer. During the switching commutation, the low side switch S_2 is turned-on under a ZVS condition. Therefore, the turn-on losses are theoretically zero during the ZVS operation. The switched transformer current is negative when the low-side diode is conducting.
- At t_3, the polarity of the transformer current is forced to change while the lower diode is conducting and the low side switch S_2 is gated on. After the process, S_2 is already conducting the current and one switching cycle is complete.

3.3.2 Description of the capacitive commutation process

A simplified equivalent circuit of the commutation from half-bridge switch of ‘phase a’ on the primary bridge converter is derived in Fig. 3.12.

In the representative circuit, the 3DAB converter is limited to operating with a phase-shift angle of $0 \le \varphi \le \pi/3$. The parallel-connected snubber capacitors are

endowed with twice the capacitance. At the beginning of the switching cycle, the $v_{c_{sn}}$ is zero, and one switching cycle is completed when the $v_{c_{sn}}$ becomes equal to the input DC-link voltage $V_{\mathrm{DC.}}$ The switching commutation cycle of the 3DAB converter is represented by six-step time intervals. Finally, the simplified secondary circuit comprises a constant series-connected voltage. The value of the series voltage is dependent on the transformer turn ratio or the charging time of the $2C_{sn}$ capacitance during the switching commutation. For the analytical solution, a constant capacitance is assumed:

$$C_{sn1} = C_{sn2} = C_{sn} = \text{const.} \tag{3.11}$$

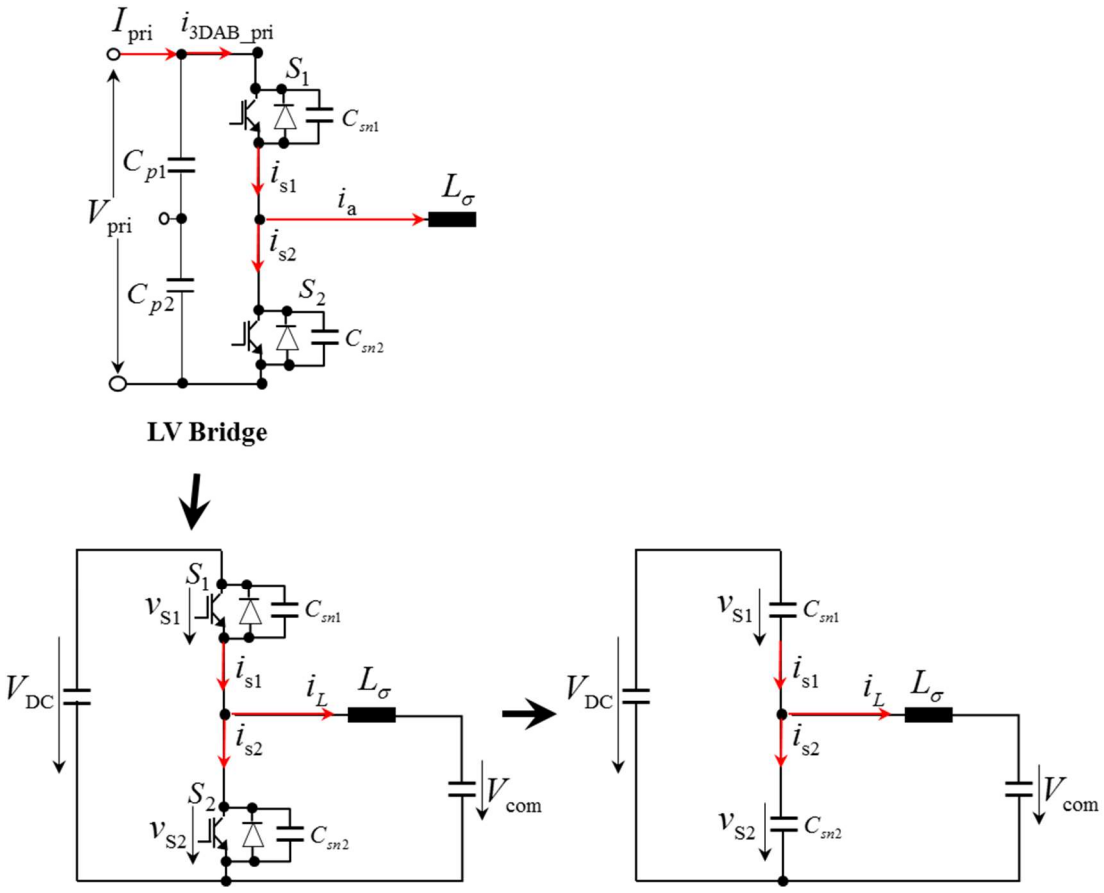


Figure 3. 12 Equivalent circuit of half-bridge ‘phase a’ on the primary bridge of 3DAB converter

The equivalent circuit shows that the switching cycle is determined by an oscillation between the $2C_{sn}$ and the resonant inductance of L_{σ}. Using the diagram, the associated resonant characteristics are calculated as

$$\omega_r = \frac{1}{\sqrt{L_\sigma \cdot 2C_{sn}}} \tag{3.12}$$

$$Z_r = L_\sigma \cdot \omega_r = \sqrt{\frac{L_\sigma}{2C_{sn}}} \tag{3.13}$$

where, ω_r is the resonant frequency and Z_r is the resonant impedance. To estimate the commutation time for a variable snubber capacitance, using Eq. (3.13), an equivalent value with respect to the snubber capacitances will be referred to the base value C_{sn_b}, defined as

$$C_{sn_b} = \frac{1}{2 \cdot {\omega_r}^2 \cdot L_\sigma} \tag{3.14}$$

The mathematical expression for the commutation process is derived in Appendix D. Usually, the analysis of switching transients is carried out with an analytical assumed constant capacitance [135]. However, this method enables an accurate calculation only with sufficiently high snubber capacitance values. Using equivalent capacitance, the mathematical expression for the commutation time is given by (D.10):

$$t_{\text{com}} = \frac{1}{\omega_r} \cdot \left[\arcsin\left(\frac{V_{\text{DC}} - V_{\text{com}}}{\sqrt{\left(I_0 \cdot Z_r\right)^2 + {V_{\text{com}}}^2}} \right) - \arctan\left(\frac{V_{\text{com}}}{Z_r \cdot I_0} \right) \right] \tag{3.15}$$

Where, the required initial current I_0 for a fixed dead time can be calculated with (D.11):

$$I_0 = -\frac{V_{DC} + V_{com} \cdot \left[\cos\left(\omega_r t_{dead}\right) - 1\right]}{Z_r \cdot \sin\left(\omega_r t_{dead}\right)} \qquad \text{for } t_{dead} < \frac{\pi/2 - \arctan\left(\dfrac{V_{com}}{I_0 \cdot Z_r}\right)}{\omega_r} \tag{3.16}$$

It should be noted that the commutation time and the initial current using the equivalent capacitance is an estimated value. As the current waveforms are not equal for a constant capacitance, the commutation times will differ slightly.

Figure 3.13 shows the equivalent switching cell with the resonance capacitors and the commutation elements such as resonant inductance L_σ and commutation voltage V_{com}, which contribute to the oscillation during the switching process. The resonance capacitors represent an external ZVS snubber. The inductance L_σ corresponds to the inductance of the AC-coupling circuit within the current path of the commutation current. The voltage V_{com} depends on the switching states and is usually a combination of input and output voltages or zero states. The commutation process shown in Figure 4.4 is based on a fixed dead time and same capacitances and only differs in the V_{com} and the initial current I_0. During the turn-on process from S_2 to S_1, the capacitance C_{sn1} is discharged to zero while C_{sn2} is charged to the DC-link voltage V_{DC}. For supporting the commutation process, a negative voltage V_{com} requires a higher initial current than the minimum offset value (D.9), which means higher energy is stored in the inductance.

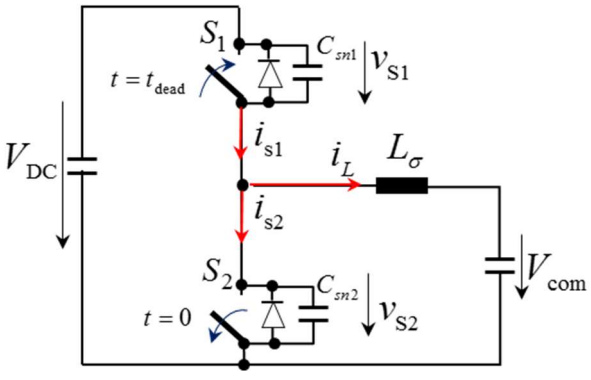


Figure 3. 13 Equivalent circuit of capacitive commutation of a half bridge

The waveforms for the commutation process of the half bridge shown in Fig 3.13 with different initial current and dead times are illustrated in Fig 3.14. The

commutation from S_2 to S_1 is considered. At $t = 0$, the switch S_2 is turned off and then switch S_1 is turned on after the dead time. Again, the current I_0 is negative for the turn-on process in the input-side bridge to support the soft-switching commutation.

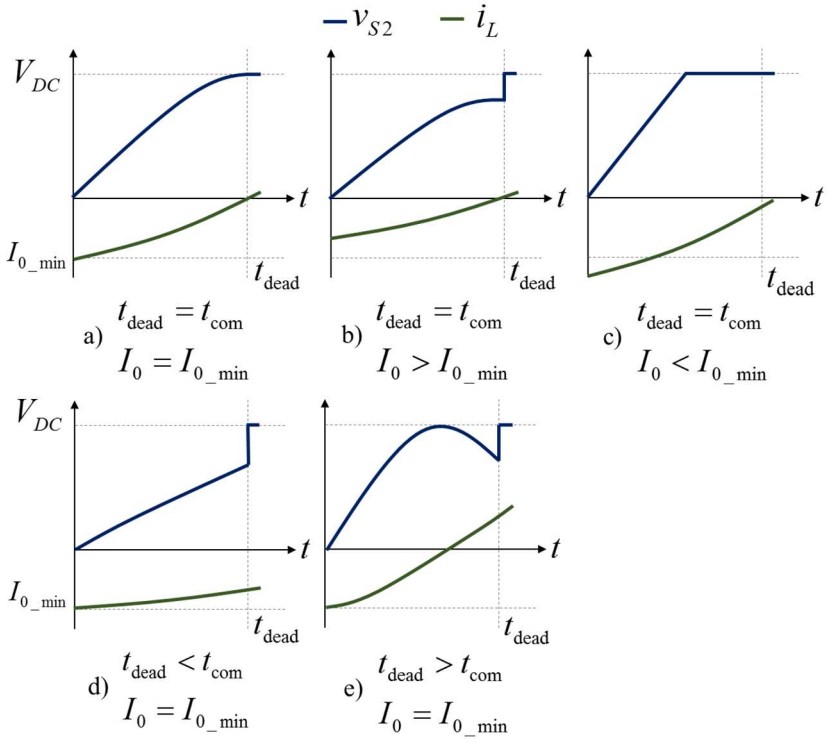


Figure 3. 14 Waveforms of switch voltage and phase current for different commutation conditions

In case of $t_{dead} = t_{com}$, the first example ($I_0 = I_{0_min}$) corresponds to the ideal ZVS border. The switch voltage v_{S2} reaches the value of the DC-link voltage V_{DC} ideally after the dead time. On the other hand, with a higher value of I_0 (b), the rising shape of the v_{S2} does not reach the value of the V_{DC} and after the switch S_1 is turned on, a step-voltage rise, which leads to switching losses due to the high current pulse, occurs. Using a smaller value ($I_0 < I_{0_min}$) leads to higher energy stored in the inductance (c). With the higher energy provided by the inductance, the voltage increase is ramped up and the charge process is completed earlier than the dead time. With a lower dead time, the voltage v_{S2} does not reach V_{DC} before the switch S_1 is turned on (d) and a step voltage rise occurs at the dead time. In contrast, using a higher dead time (e), the voltage V_{DC} is reached before the end of the dead time. The

oscillation can continue to value $v_{S2} < V_{DC}$ at the turn-on transition depending on the magnitude of the phase current i_L. It should be noted that the oscillations during the commutations are normally not considered in the simulation model owing to their significantly lower simulation time constant than that of the real converter.

The ZVS at turn-off operation can be achieved with sufficiently large snubber capacitances to reduce switching losses. In addition, snubber capacitor minimises the effect of turn-off commutation dv/dt. Lower dv/dt results in higher switching losses. While the higher gate resistor gives a very slow turn-on and almost no recovery peak in the anti-parallel diode, the active switch turn-on loss is increased considerably. The sizing of the snubber capacitor can be carried out by the initial maximum turn-off current conditions in an ideal snubberless 3DAB converter circuit as shown in Fig. 3.1. Using a piecewise modelling for steady-state analysis as shown in Appendix A, the switch currents for the primary and secondary side are derived as follows:

$$i_a(0) = \frac{V_{\text{pri}}}{3\omega_{sw}L_\sigma}\left[\frac{2}{3}\pi d - d\varphi - \frac{2}{3}\pi\right] \qquad \text{for}\left(0 \le \varphi \le \pi/3\right) \tag{3.17}$$

$$i_a(\varphi) = \frac{V_{\text{pri}}}{3\omega_{sw}L_\sigma}\left[\frac{2}{3}\pi d + \varphi - \frac{2}{3}\pi\right] \qquad \text{for}\left(0 \le \varphi \le \pi/3\right) \tag{3.18}$$

The maximum turn-off currents on the primary and secondary side converters, in case of an ideal snubberless 3DAB converter, and under the condition that the phase-shift angle range is limited to $\phi \le \pi/3$, can be calculated using Eq. (3.17) and (3.18)

$$I_{\text{OFF_max_p}} = \frac{\frac{2\pi}{3}\cdot V_{\text{pri}} - \left(\frac{2\pi}{3} - |\varphi|\right)\cdot n \cdot V_{\text{sec}}}{6\pi f_{sw}\cdot L_\sigma} \tag{3.19}$$

$$I_{\text{OFF_max_s}} = \frac{\frac{2\pi}{3}\cdot n \cdot V_{\text{sec}} - \left(\frac{2\pi}{3} - |\varphi|\right)\cdot V_{\text{pri}}}{6\pi f_{sw}\cdot L_\sigma} \tag{4.4}$$

where, n is the turns ratio between the primary side and secondary side of the AC-link transformer. The maximum current for each bridge is calculated by the maximum voltage of the primary side, minimum value of the secondary bridge voltage, and phase-shift angle (φ) corresponding to nominal transferring power. The calculated turn-off currents are used to estimate the sizing of the resonant snubber capacitances. Considering the snubber capacitance increases the turn-off *dv/dt* resulting from the increased capacitor current, the maximum turn-off current should be determined in reference to the specified capacitor circuit conditions. Thus, the maximum turn-off current for the ideal snubberless 3DAB converter provided in Eq. (3.17) and (3.18) can be rewritten as follows.

$$I'_{\mathrm{OFF_p|max}} = \frac{\frac{2\pi}{3}\cdot V_{\mathrm{pri}} - \left(\frac{2\pi}{3} - \left|\varphi'\right|\right)\cdot n\cdot V_{\mathrm{sec}}}{6\pi f_{sw}\cdot L_{\sigma}} \tag{3.20}$$

$$I'_{\mathrm{OFF_s|max}} = \frac{\frac{2\pi}{3}\cdot n\cdot V_{\mathrm{sec}} - \left(\frac{2\pi}{3} - \left|\varphi'\right|\right)\cdot V_{\mathrm{pri}}}{6\pi f_{sw}\cdot L_{\sigma}} \tag{3.21}$$

3.4 Compensate phase shift angle with dead time

In general, certain values of the snubber capacitor have an influence on the limitation of the *dv/dt* slopes and the increase in commutation times in the switch branches. Hence, these have a strong impact on the operated waveform's characteristics for the 3DAB converter with a snubber capacitor circuit. A comparison of the theoretical AC-link transformer voltage and current waveforms of a 3DAB converter operated in boost operation is illustrated in Fig. 3.15. As can be seen, the ramp-shaped voltages have been defined as linear for illustration. On the contrary, the voltage slopes in a real converter have high-frequency damped oscillation caused by parasitic components during the turn-off commutation, which has been neglected for the ideal illustration purpose. Besides, the commutation times as well as the value of the snubber capacitors may be generally different between the primary and secondary bridges in a real converter system, unless the converter is

operating under a unity ratio condition. For that reason, the individual turn-off times $t_{\text{off_p}}$ and $t_{\text{off_s}}$ are determined for each bridge. As the secondary bridge voltage v_{rn} has been set higher than the primary voltage v_{an}, the AC-link transformer current is negative at the turn-off commutation stage to ensure ZVS. Generally, snubber capacitances lead to different commutation times for the primary- and secondary-side converters, resulting in a different phase-shift angle.

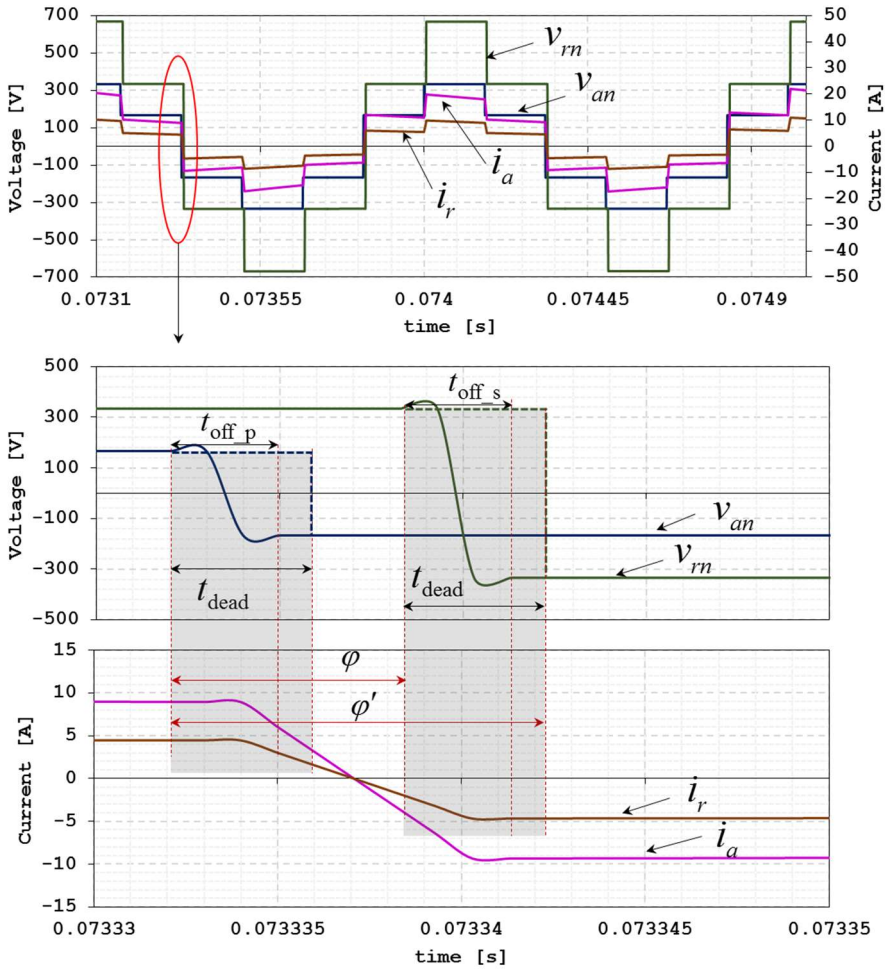


Figure 3. 15 Comparison of simulated AC-link transformer voltage and current waveforms of a 3DAB converter in case of turn-off commutation resulting from the step-up mode

In a practical system, a sufficient dead time is important to avoid a short circuit in the half bridge during the commutations. Furthermore, the dead time is required to avoid a reduction in the transferred power. The minimum value for dead time must

be larger than the sum of turn-on, turn-off, and rising and falling times depending on the used semiconductor:

$$(t_{\mathrm{f}} + t_{\mathrm{r}} + t_{\mathrm{d(on)}} + t_{\mathrm{d(off)}}) < t_{dead} < 0.01 \cdot \frac{1}{f_{sw}} \tag{3.22}$$

The impact of dead time on single phase-shift (SPS) modulation has been studied for single-phase dual active bridge (1DAB) converters [171-173]. For SPS modulation, the dead time impact becomes significant on the current waveforms at hard-switching operation or when the current crosses zero during the dead time. Also, with the increase in the dead time, the performance of any control scheme will deteriorate. A comprehensive theoretical analysis and verification for dead time effect of the 1DAB converter has been introduced in [173]. For SPS modulation, the initial phase-shift angle can be distorted by the dead time. Therefore, it needs to be compensated in order to maintain the desired output power and output voltage. An additional phase-shift angle needed to compensate the initial angle is given by:

$$\varphi_{\mathrm{dead}} = \omega_{sw} \cdot t_{\mathrm{dead}} \tag{3.23}$$

With the additional phase-shift angle, which corresponds to the dead time, the compensation-shift angle can be calculated with:

$$\varphi' = \varphi + \varphi_{\mathrm{dead}} = \varphi + \omega_{sw} \cdot t_{\mathrm{dead}} \tag{3.24}$$

where, $\omega_{sw} = 2\pi f_{sw}$ and initial control angle φ can be calculated as (Appendix B)

$$\varphi = \frac{2\pi}{3} - \sqrt{\left(\frac{2\pi}{3}\right)^2 - 2\pi \cdot \frac{P_o \cdot \omega_{sw} \cdot L_\sigma}{V_{pri} \cdot V'_{\mathrm{sec}}}} \tag{3.25}$$

Influence of dead time on 3DAB operation

To validate the influence of dead time on phase-shift modulation, a 3DAB converter as shown in Fig. 3.11 was simulated transferring 10-kW power. The model

operated with a switching frequency of 1 kHz. PLECS software was used as the simulation tool. In this simulation, the 3DAB model was connected to a resistive load. The input DC-link voltage was set to 500 V. The DC conversion ratio '*d*' was set to 1. The turns ratio of the transformer was 1:2; hence, the output voltage needed to be maintained to constant output voltage of 1000 V. Fig. 3.16 shows the influence of dead time on the phase-shift angle. The ideal angle and compensated angle affected by the dead time are compared. With the increase in transferred power, the dead time effect becomes significant. It can be seen that under heavy load conditions (a), the dead time effect is more severe than that under light load conditions (b). For phase-shift modulation, the ideal phase-shift angle distorted by the dead time needs to be compensated in order to maintain the desired output voltage.

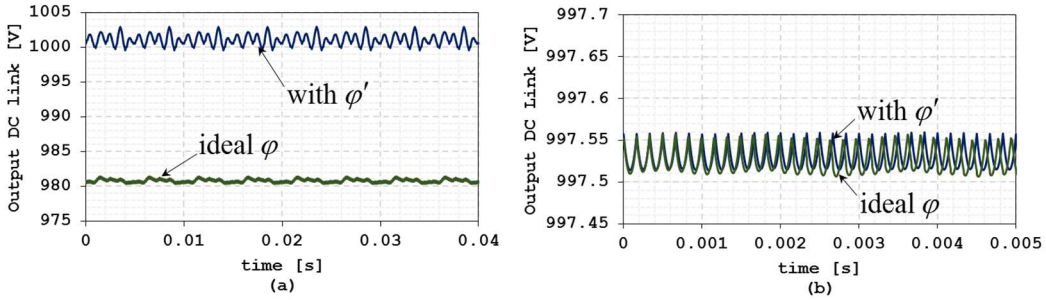


Figure 3. 16 Comparison of output DC-link voltage in the steady state: (a) Pout = 10kW at full load condition and (b) Pout = 1.5 kW at light load condition

Switching commutations can be evaluated during the dead time [173]. The two possible commutation conditions during the turn off are shown in Fig. 3.17. In hard commutation, the current in the inductance of the transformer is not large enough to reduce the bottom switch voltage and is not sufficient to charge and discharge both snubber capacitors. Finally, after the dead time, the switches are turned off and on and the top capacitor is charged; however, the bottom capacitor is still not discharged, and it can be short circuited by the bottom switch. There are additional losses. On the other hand, the transformer current is enough to reduce the voltages to zero during the dead time. Therefore, there is soft switching commutation.

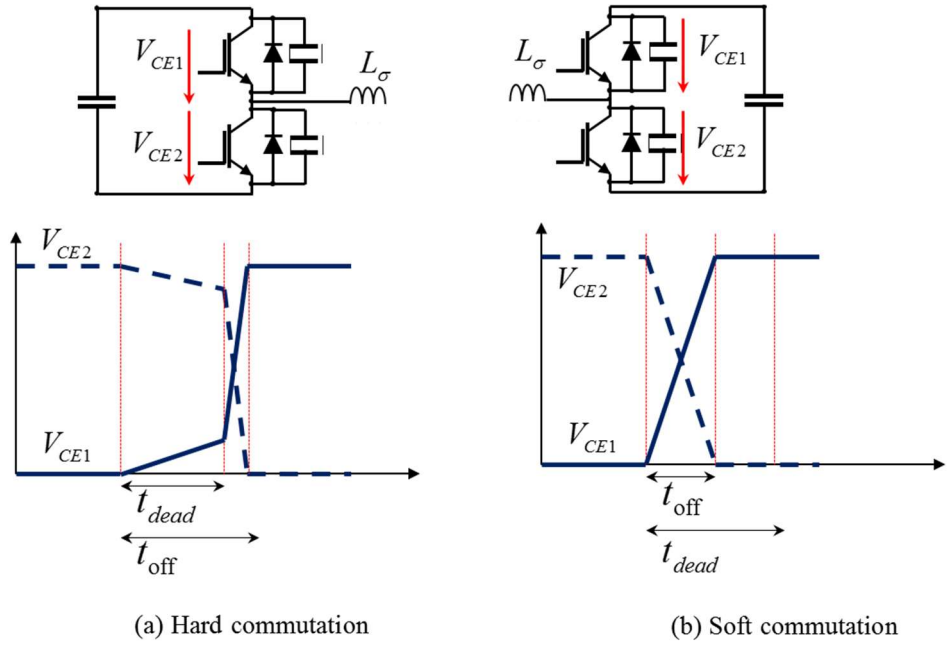


Figure 3. 17 Hard and soft commutation waveforms in a half bridge with ZVS snubber circuit

3.5 Soft switching range with dead time compensation

Generally, a wide range of low-load operations is required for DC-DC conversion applications, such as renewable energy sources and DC distribution girds. Therefore, the use of snubber capacitors contributing to a further extension of the soft switching operating range of the 3DAB converter needs to be investigated. This section focused on the investigation into the extension of the ZVS over the full power range.

Considering turn-off commutation times presented in previous sections, in case of positive values of φ, the primary bridge as the 'leading' side requires an increase in the turn-off current for entering the ZVS range, while the secondary bridge as the 'lagging' side does not require a higher turn-off level of the transformer current. The values of the equivalent switching cell for the 3DAB converter with single phase-shift modulation can be determined (cf. Fig. 3.13). The commutation voltage V_{com} depends on the switching states. For SPS modulation, these voltages have been derived for the primary bridge [168]:

$$V_{\text{com}} = \begin{cases} \dfrac{\left(V_{pri} - n \cdot V_{\text{sec}}\right)}{2} & \text{for } 0 \le \varphi \le \pi/3 \\ \dfrac{\left(V_{pri} - n \cdot 2V_{\text{sec}}\right)}{2} & \text{for } \pi/3 \le \varphi \le \pi/2 \end{cases} \tag{3.26}$$

This expression is also valid for the secondary bridge by changing the sign of the phase-shift angle and exchanging V_{pri} and V_{sec}. If $V_{\text{com}} = \left(V_{\text{pri}} - n \cdot V_{\text{sec}}\right)/2$ remains below $V_{\text{DC}}/2$, $i_a(0)$ will not be sufficient to charge the snubber capacitance. Therefore, the required current level of $i_a(0)$ for enabling ZVS operation is calculated using Eq. (D.7):

$$V\frac{V_{\text{pri}} - \text{n} \cdot V_{\text{sec}}}{2} + \sqrt{\left(\frac{V_{\text{pri}} - \text{n} \cdot V_{\text{sec}}}{2} + (Z_{\text{r}} \cdot i_{\text{a}}(0))^2\right)} = V_{\text{pri}} \tag{3.27}$$

Where, Z_{r} is resonnat impedance. For the primary bridge, this equation sets equal to the appropriate formula of $i_a(0)$ and solving for $i_a(0)$ as:

$$\begin{aligned} i_a(0) &= \frac{V_{\text{pri}}}{3\omega_{sw}L_\sigma}\left[\frac{2}{3}\pi d - d\varphi - \frac{2}{3}\pi\right] = \frac{\sqrt{V_{\text{pri}} \cdot V'_{\text{sec}}}}{\text{Z}_r} \qquad \text{for}\left(0 \le \varphi \le \pi/3\right) \\ &\frac{V_{\text{pri}}}{3\omega_{sw}L_\sigma}\left[\frac{2}{3}\pi d - d\varphi - \frac{2}{3}\pi\right] = \frac{\sqrt{V_{\text{pri}} \cdot V'_{\text{sec}}}}{\text{Z}_r} \end{aligned} \tag{3.28}$$

To obtain the ZVS limits, with d'_{pri} of the DC conversion ratio as snubber capacitance influence and dead time in the primary bridge, eq.(3.28) can be solved for the d_{pri} as follows:

$$d'_{\text{pri}} = \frac{\left[\dfrac{\left(\sqrt{V_{\text{pri}} \cdot n \cdot V_{\text{sec}}}/\sqrt{L_\sigma/2 \cdot C_{sn_p}}\right) \cdot 6 \cdot \pi \cdot f_{sw} \cdot L_\sigma}{V_{\text{pri}}}\right] + \dfrac{3\pi}{2}}{\dfrac{3\pi}{2} - \varphi'} \tag{3.29}$$

The corresponding d'_{sec} for the secondary bridge is obtained from symmetry by referring to $i_a(\varphi)$ as the primary side current instead. Hence, the following expression is used for ZVS limits d'_{sec} in the secondary bridge.

$$d'_{\text{sec}} = \frac{\left[\frac{\left(\sqrt{V_{\text{pri}} \cdot n \cdot V_{\text{sec}}} \Big/ \sqrt{L_\sigma / 2 \cdot C_{sn_s}}\right) \cdot 6 \cdot \pi \cdot f_{sw} \cdot L_\sigma}{V_{\text{pri}}}\right] + \frac{3\pi}{2} - \varphi'}{\frac{2\pi}{3}} \tag{3.30}$$

As can be seen, the ZVS regions vary as a function of the primary and secondary DC-link voltages, AC-link impedances, snubber capacitance, transformer winding turns ratio of the AC link, and phase-shift angle between the two bridges. For the particular case where the AC-link can be simplified to a series inductance represented by the leakage inductance of the transformer, the ZVS boundaries are described by Eq. (3.29) and (3.30).

ZVS areas with dead time effects can be evaluated, as shown in Fig. 3.18. Fig 3.18 shows the operational area for positive power flow from the primary bridge to the secondary bridge along with the areas affected by dead time effects and two exemplary DC conversion ratios for '*d*" = 0.5 and '*d*" = 1.5. These areas show hard switching and ZVS for the primary and secondary bridges as the transferred power ratings, the compensated phase-shift angle φ' and the DC conversion ratio d' vary.

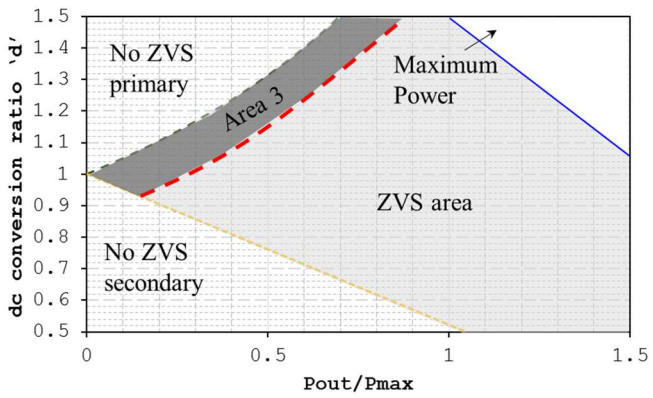


Figure 3. 18 ZVS boundaries with dead time effects.

Fig. 3.19 shows the simulation model of a 3DAB converter that is used for the validation. The maximum power rating is set to 10 kW and turns ratio of the transformer is 1:2. The analytical three-phase transformer has symmetrical leakage inductances. This results in symmetrical ZVS boundaries for the primary and secondary bridge. As a consequence, since the two bridges are operated with symmetry-shifted six-step square modulation, the switched three-phase currents will be balanced and ZVS for each phase leg will be maintained as the same value of d' and φ'.

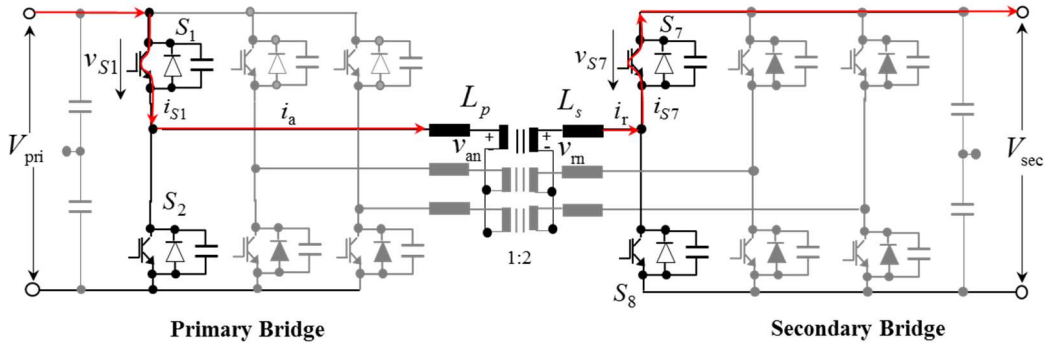


Figure 3. 19 3DAB converter simulation model with maximum power rating of 10kW, 1:2 turns ratio, and 1kHz switching frequency

No ZVS secondary area

Characteristic waveforms of no ZVS secondary area are depicted in Fig. 3.20. This area corresponds to the hard switching operation of the secondary bridge and the conditions where the primary bridge voltage is higher than the secondary bridge voltage. The dead time delays the voltage v_{rn}. In the turn-on process, the secondary bridge switches are hard switched on while the primary bridge switches are ZVS ON since the current flows through the anti-parallel diode, not in $S7$. On the other hand, during the turn-off commutation, the switch $S7$ has negative turn-off current. The current i_{S7} commutates to its anti-parallel diode during the dead time, which leads to positive voltage $v_{rn} = V_{sec}/3$ (100 V) until $S8$ is turned on. The ideal phase-shift angle is extended by the dead time, which corresponds to the compensated phase-shift calculated with (3.24).

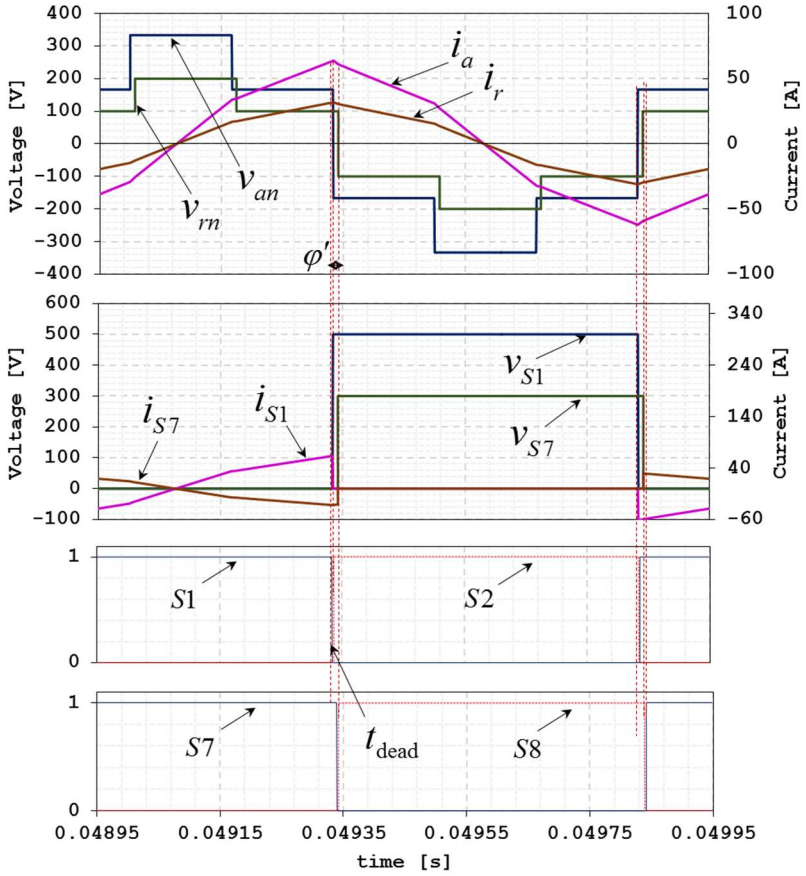


Figure 3. 20 3DAB converter operation waveforms with dead time for hard switching secondary bridge

No ZVS primary area

The dead time also influences the phase-shift modulation at the hard switching operation of the primary bridge, which is covered by the no ZVS primary area in Fig. 3.17. The characteristic waveforms are depicted in Fig. 3.21. The area corresponds to the conditions where the primary bridge voltage is smaller than the secondary bridge voltage. It can be seen from Fig. 3.21 that $S1$ is hard switched on while $S7$ is switched on at ZVS. In the turn-on process, all the turn-on actions on the primary bridge switches are hard-switched, while all secondary bridge switches are ZVS ON. Therefore, the loss of the secondary bridge occurs in the anti-parallel diodes and there is no current in the active switches. On the other hand, during the turn-off commutation, the negative turn-off current of switch $S1$ results in positive voltage v_{an} = $V_{\text{pri}}/3$ (100 V) during the dead time. This leads the current i_{S1} to commutate to its anti-parallel diode during the dead time until $S2$ is turned on.

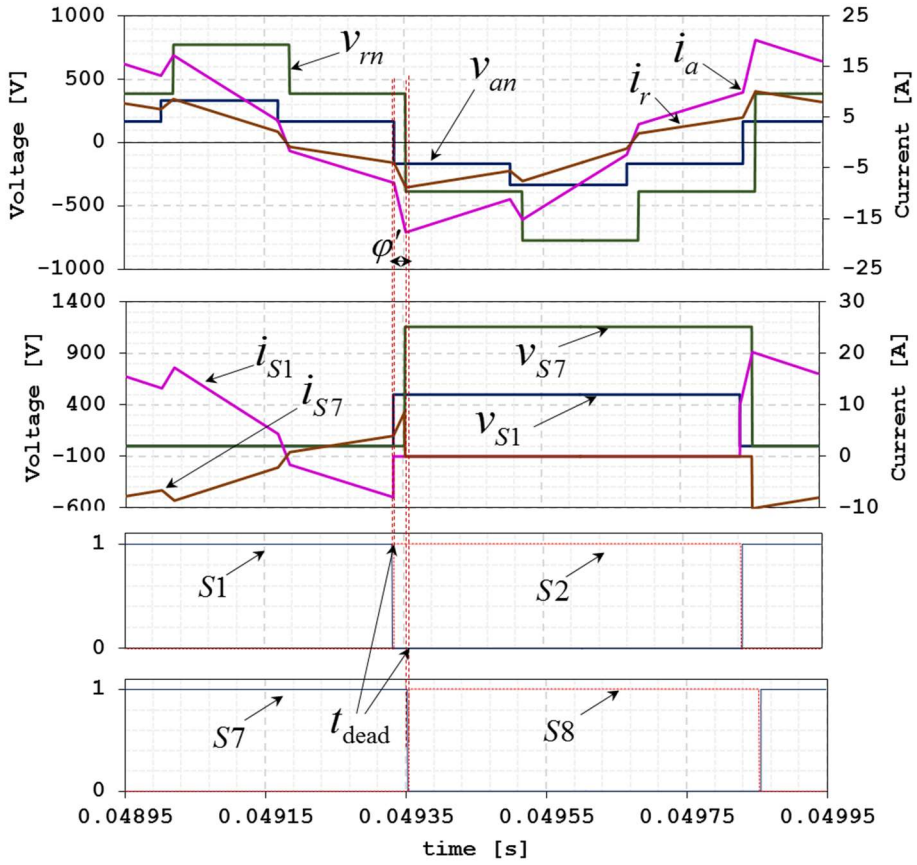
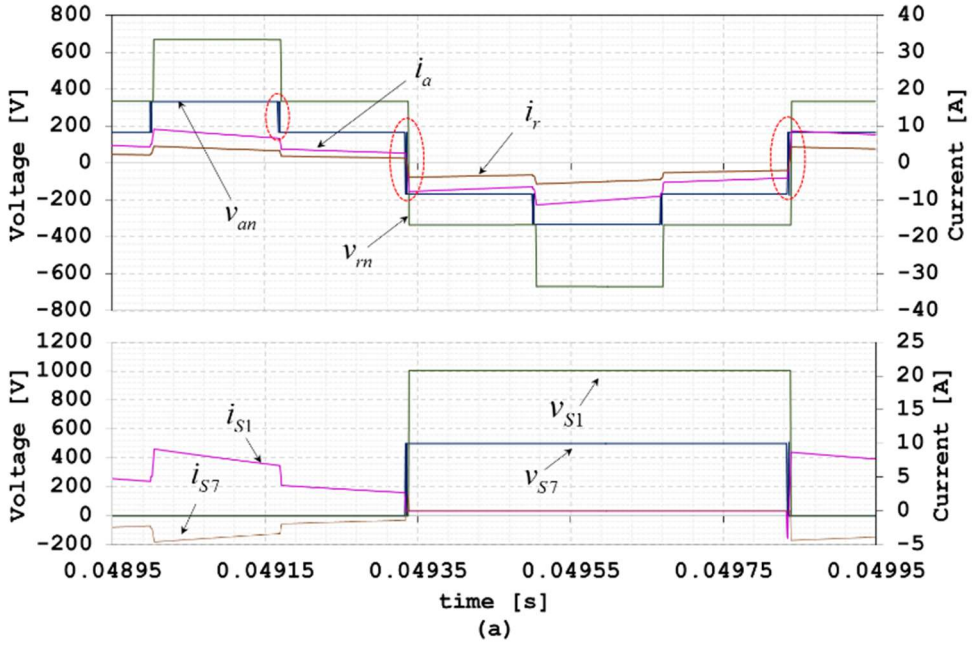
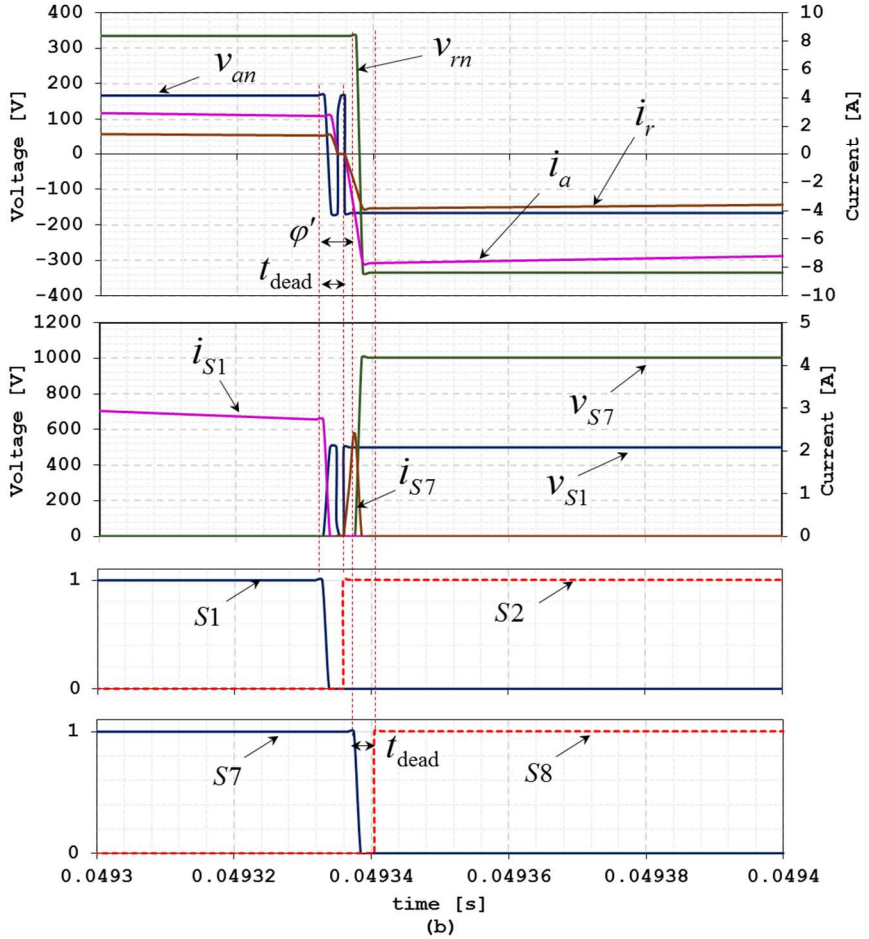


Figure 3. 21 3DAB converter operation waveforms with dead time for hard switching primary bridge

Area 3 (example: '*d*'= 1.0 case)

An example of the altered voltage shapes of area 3 for phase 'a' is shown in Fig. 3.22. In this area, the voltage shapes of the transformer voltages v_{an} and v_{rn} differ from the six-step interval waveform. As can be seen, the transformer-phase current crosses zero during the dead time of $S1$ and $S2$. This leads to an additional time span with a different voltage. This phenomenon occurs six times during one fundamental period: at the zero crossing of the phase 'a' current i_a and the other phase currents. The area can be divided into two parts: one for $0 < d' \leq 1$ and one for $d' > 1$. While the characteristic waveform of the first part is similar to the one for no ZVS primary area, the condition of the second one does not correspond to the condition for no ZVS secondary area.


Voltage [V]
Current [A]
i_a
i_r
v_{an}
v_{rn}
i_{S1}
i_{S7}
v_{S1}
v_{S7}
time [s]
(a)


Voltage [V]
Current [A]
v_{an}
v_{rn}
i_r
i_a
φ'
t_{dead}
i_{S1}
v_{S7}
i_{S7}
v_{S1}
S1
S2
S7
S8
time [s]
(b)

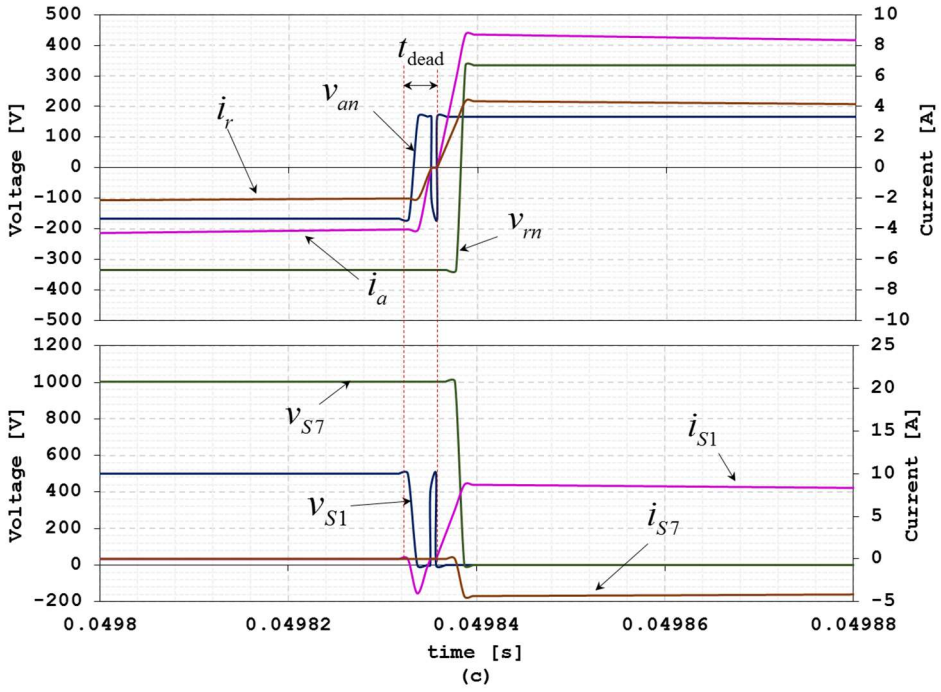


Figure 3. 22 3DAB converter operation waveforms with dead time for area 3: (a) waveforms for one period, (b) turn-off commutation, and (c) turn-on commutation

In area 3, the primary bridge is not operated under ZVS conditions. Nevertheless, this operation is not purely hard switching. For $V_{\text{pri}} \geq nV_{\text{sec}}$, ideally the turn-off current is zero, which means that the switch can be operated under ZCS. It can be seen in Fig. 3.22(b) that the turn-off current is greater than zero; however, comparably low current levels (almost close to zero) occur. Thus, the turn-off losses can be low even when the primary bridge is operated under hard-switching condition. For this range, it has to be noted that the turn-off losses depend on the optional snubber capacitors of the switches. During turn-on, the primary bridge is operated under ZVS conditions.

3.4 Summary

This chapter presented an overview of the 3DAB converter. The operating principle of the 3DAB converter was explained using the simplified FHA converter model. Expressions of the RMS values of switch currents, along with peak and RMS currents of the leakage inductance of the transformer were obtained from the model.

These mathematical models are useful for predicting power losses and studying the converter characteristics. This work aimed to achieve ZVS of the converter across a considerable range of voltages (up to 40 kV DC) and power ratings (4 MW). The ZVS operating can be combined with a reduction in *dv/dt* stress during turn-on switching action, which contributes significantly to reducing switching losses of the semiconductors.

The snubber circuit topology for the high-power 3DAB converter that utilises the advantages of the aforementioned ZVS switching scheme was investigated. The snubber capacitors are required in order to achieve the desired reduction in voltage transients during turn-off switching commutation. Employing higher capacitances leads to extra power dissipation, resulting from longer voltage transients. How the ZVS range can be extended with snubber capacitances was investigated in this work. Analytical results show that the snubber capacitor size must be adjusted to a specified minimum commutation time for each bridge, while employing higher capacitances led to extra power dissipation due to longer voltage transients. Furthermore, the results show that increasing values of the snubber capacitor have an extending effect on the primary bridge ZVS boundary.

Chapter 4

Three-phase medium frequency transformer for 3DAB Converter

One of the key components of the 3DAB converter is a high-power galvanic transformer enabling isolation with the MV line for safe operation and also the change of the voltage levels for efficient power transfer. Previous research in the optimal design of a 50/60 Hz conventional transformer was introduced in [84-93]. Most of the studies in the literature focus on medium/high frequency transformer design for high-power applications. The main advantage of using a high-frequency transformer is that it can lead to significant reduction in the transformer's size and weight, which leads to a reduction in not only the manufacturing cost but also the overall volume of the whole system. However, these studies only considered sinusoidal excitations. For non-sinusoidal high power applications, studies focused on the design for medium/high frequency; especially in [94-110], the design considerations are related to high-power DC-DC applications. These studies, however, presented only the design procedure of a single-phase transformer. More recently, in [111-113], a three-phase transformer for 3DAB topology has been studied while focusing on losses.

This chapter presents not only the power loss analysis but also design optimisation of a three-phase 1kHz transformer. Design optimisation enables the identification of the optimum parameters for a given object's functions (i.e. efficiency, leakage, inductance, and volume). Moreover, by comparing the two possible design scenarios, the optimisation can be carried out to find a better solution to develop the proposed configurations of the MVDC grid.

4.1 Modeling of transformer

In a conventional sinusoidal transformer, apparent power is usually calculated by assuming referred voltages on the primary and secondary windings. However, in the 3DAB converter, the amplitudes of the winding voltages are determined by the voltage conversion ratio d corresponding to the turns ratio of the transformer. According to [70], the apparent power (S_T) of the 3DAB converter is calculated as

$$S_T(VA) = \frac{V_{pri} \cdot (d+1)}{\sqrt{2}} \cdot I_{prms} = 3 \cdot V_{pn} \cdot I_{prms} \tag{4.1}$$

In the present study on modelling and design, the transformer is Star-Star (Yy) connected, and three-phase symmetric leakage inductances are used as power transfer elements. For high-voltage operation, a three-phase transformer with star connection offers the benefits of reducing the voltage level on individual windings, circulating currents, and unbalanced currents [85]. The transformer size and reactive power are the important parameters that can be determined by the apparent power of a Yy-connected transformer. In Fig. 4.1, the calculated transformer apparent power (kVA) versus output power, P_o, of the 3DAB converter for different values of d are plotted. It can be seen that S_T exceeds P_o for $d \leq 1.5$ and forward higher power levels. This is an important aspect in transformer design, as the transformer size is inversely proportional to the operating frequency. For instance, the minimum S_T is required at 1.3 p.u of output power of 4 MVA at d = 1, corresponding to a wide range of soft-switching operations. Now, for the same kVA at d = 1, the maximum power transfer

can be increased to 1.5 p.u at d = 2.0 (boost mode); however, the 3DAB converter will be operated under the hard-switching mode. In addition, the control phase-shift angle would need to be adjusted to avoid unnecessary overrating of the transformer leading to larger voltage imbalances.

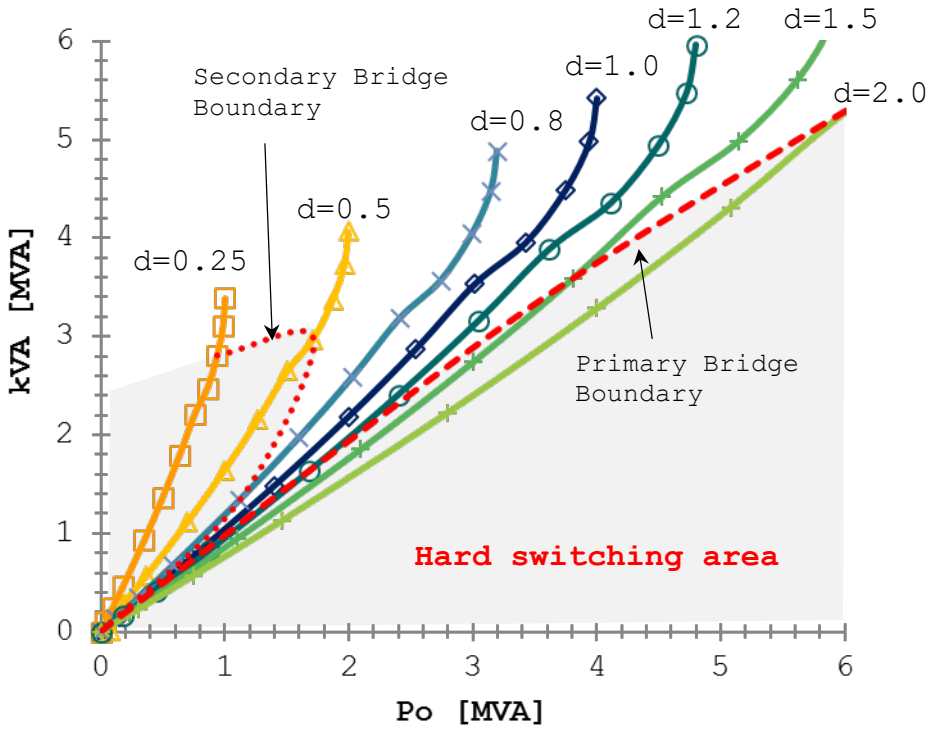


Figure 4. 1 Transformer apparent power $S_T\,(kVA)$ versus output power of 3DAB converter

As mentioned above, the transformer's apparent power, S_T, exceeds the nominal output power Po of the 3DAB converter. The apparent power for the three-phase transformer is calculated from the RMS values of the phase voltages and currents on the primary winding. From Chapter 3, the RMS values of the phase current of the primary-side transformer are derived as

$$I_{prms} = \frac{V_{pri}}{6\pi \cdot f_{sw} \cdot L_\sigma} \cdot \varphi \cdot \sqrt{\frac{2\pi - \varphi}{\pi}} \quad \text{for} \left(0 \le \varphi \le \pi/3\right) \tag{4.2}$$

$$I_{prms}=\frac{V_{pri}}{12\pi\cdot f_{sw}\cdot L_{\sigma}}\cdot\varphi\cdot\sqrt{\frac{8\pi-6\varphi}{\pi}}\quad \text{for}\left(\pi/3\le\varphi\le 2\pi/3\right) \tag{4.3}$$

Substituting Eq. (4.2), (4.3) and $V_{pn}=\frac{\sqrt{2}}{3}V_{pri}$ into Eq. (4.1), the apparent power of the transformer can be calculated as

$$S_T = 3\cdot V_{pn}\cdot I_{prms} = \frac{\sqrt{2}\cdot V_{pri}^2}{6\pi\cdot f_{sw}\cdot L_{\sigma}}\cdot\varphi\cdot\sqrt{\frac{2\pi-\varphi}{\pi}} \qquad \text{for } \left(0\le\varphi\le\pi/3\right) \tag{4.4}$$

$$S_T = \frac{\sqrt{2}\cdot V_{pri}^2}{12\pi\cdot f_{sw}\cdot L_{\sigma}}\cdot\varphi\cdot\sqrt{\frac{8\pi-6\varphi}{\pi}} \qquad \text{for } \left(\pi/3\le\varphi\le 2\pi/3\right) \tag{4.5}$$

The transformer size and reactive power loss are determined by the apparent power. The ratio of P_o/S_T, which can be simplified as the PF of the transformer on the 3DAB converter, can be derived as

$$\begin{aligned} PF&=\frac{P_o}{S_T}=\frac{\frac{V_{pri}^2}{\omega L_{\sigma}}\cdot d\cdot\varphi\left[\frac{2}{3}-\frac{\varphi}{2\pi}\right]}{\frac{\sqrt{2}\cdot V_{pri}^2}{6\pi\cdot f_{sw}\cdot L_{\sigma}}\cdot\varphi\cdot\sqrt{\frac{2\pi-\varphi}{\pi}}}=\frac{2d-\frac{3\varphi}{2\pi}}{\sqrt{4-\frac{2\varphi}{\pi}}} \quad \text{for}\left(0\le\varphi\le\pi/3\right)\\ PF&=\frac{6d\left[\varphi-\frac{\varphi^2}{\pi}-\frac{\pi}{18}\right]}{\varphi\cdot\sqrt{\frac{16\pi-12\varphi}{\pi}}} \quad \text{for}\left(\pi/3\le\varphi\le 2\pi/3\right) \end{aligned} \tag{4.6}$$

Fig. 4.2 shows the power curves of the 3DAB converter. The power factor curve versus the output power is also plotted in this figure. As shown, the PF in the 3DAB transformer is always high until the phase-shift angle, φ ,is close to 60°; therefore, less reactive power loss and higher as efficiency are achieved with the 3DAB converter. The analysis of the plots indicates that the reactive power loss increases with increasing φ . In practice, higher PF, which has a smaller φ , can be obtained

due to optimised low leakage inductance. Therefore, owing to the large reactive power generated above $\varphi > 60°$, the controlled phase-shift angle φ is usually limited below 60° for efficient operation [135, 154, 174, 176, 181].

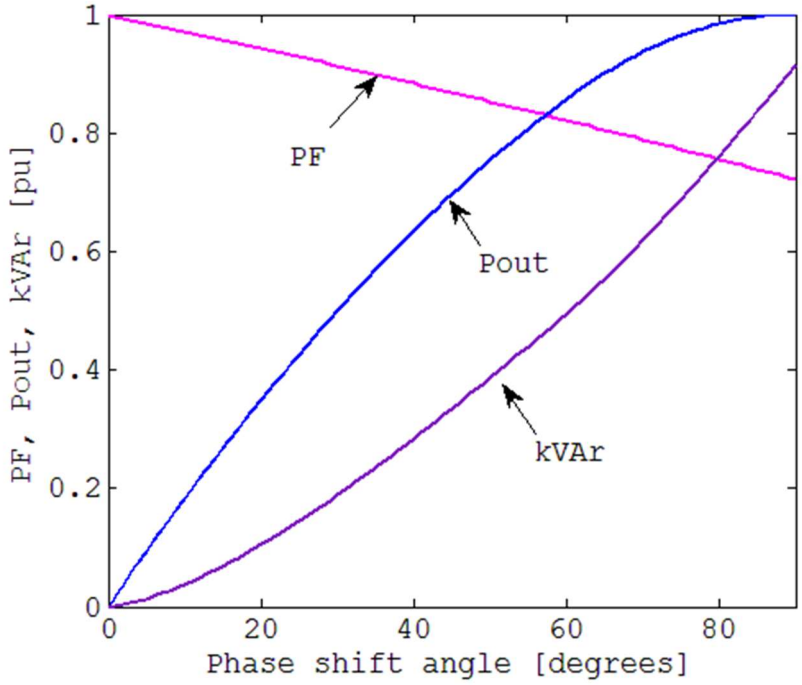


Figure 4. 2 Comparison of output power and reactive power and power factor for 3DAB (V_{pri} = 1.1kVDC, V_{sec} = 40kVDC, d=1, symmetric leakage inductance of $L_\sigma = 29.41\,\mu H$, switching frequency = 1kHz and Base power P_{base} = 4MW)

4.2 Design of 3DAB transformer

4.2.1 Design procedure

In high-power MV systems, power electronics devices are operated with a switching frequency of about 1 kHz–5 kHz [78, 135, 176]. Generally, IGCT devices are available for high-power medium-voltage applications with operating voltage ratings of 4.5, 5.5, 6.0. and 6.5 kV [135, 179]. The IGBTs for megawatt scale applications are currently offered with 2.5, 3.3, 4.5, and 6.5 kV working voltage ratings [135, 178]. The IGCT devices are allowed to operate at medium-frequency ranges up to 5 kHz. However, the typical operating frequency of the IGCTs is optimised up to 1 kHz due to high switching losses [78, 135]. Therefore, a target switching frequency of 1 kHz was selected for the system evaluation carried out in

this thesis. Considering high-voltage power electronics devices, the layout of medium-frequency transformers for high power DC-DC converters presents new challenges on overall size and core and insulation materials, necessitating the construction of units up to megawatt scale. In this thesis, a new combined technique of design from both power electronics and large-scale transformer structure was investigated for a 1 kHz high-power transformer, mainly for the megawatt scale.

The choice of the core material mainly depends on the operating frequency of the magnetic flux. In this work, the fundamental frequency of the magnetic flux is limited to approximately 1 kHz by the power electronic semiconductor switches (IGCT and IGBT). In medium-frequency, high-power applications, silicon steel and amorphous iron are considered common magnet materials [135, 176, 177]. Silicon steel is commercially used in large transformers and power distribution transformers of high power rating up to gigawatt range because of comparatively low price [135]. Besides, silicon steel is used in 400 Hz aircraft and traction applications [19-20]. The large saturation flux density (around B_m = 1.5T) promises a compact core design. Amorphous iron has the lower hysteresis losses but the saturation flux density of amorphous iron is lower than that of silicon steel [177]. The drawbacks of amorphous material is the higher manufacturing price as well as high magnetostriction, especially at high power levels [152]. Due to the cost effect and operation frequency of 1 kHz, silicon steel material was selected for the design and prototype construction in this work.

The proposed design procedure for the 3DAB MF transformer is shown in Fig. 4.3 and described in [114]. In the pre-design phase, the 3DAB converter system specifications are defined and the basic parameters (turns ratio, expected efficiency, apparent power, and the maximum flux density set to $\widehat{B}_m$ =1.2 T) for the transformer are selected. In addition, the transformer current waveform is not sinusoidal because the transformer is connected through power electronics switches, so the current waveforms must be determined. In this procedure, five degrees of freedom are selected to optimise the transformer design for highest efficiency and minimum volume. $N1$ is the number of turns on the primary winding. The secondary winding turns can be calculated automatically using the turns ratio. J_p and J_s are the current density [A/m^2] for each winding. In order to optimise the geometry of the

transformer, the window area ratio (w / h) and core sectional area ratio (d_{core} / a_{core}) are optimised.

To start the procedure, silicon steel core, copper conductor, and insulation material specifications are defined. In this case, non-oriented silicon steel, M-19 29 Ga, with a lamination thickness of 0.36 mm was used. In the first step, the geometry parameters were assigned with the free parameters in order to obtain an optimum result. The sinusoidal core loss and I^2R loss in copper were calculated with the geometry parameters. The calculated efficiency must be compared with the expected value to generate a high-performing design. If both geometry and performance parameters are not satisfactory for the given design requirements, the results are discarded and the free parameters are modified for reanalysis. If the results are satisfactory, leakage inductance is calculated because the leakage inductance value is an important parameter for the 3DAB converter operation. Once all design steps have been analysed, the results are stored for validation of silicon steel core and copper losses and a given objective functions (i.e. efficiency, efficiency versus volume) can be established. In order to explain the design procedure, a three-phase core-type transformer is illustrated in Fig. 4.4.

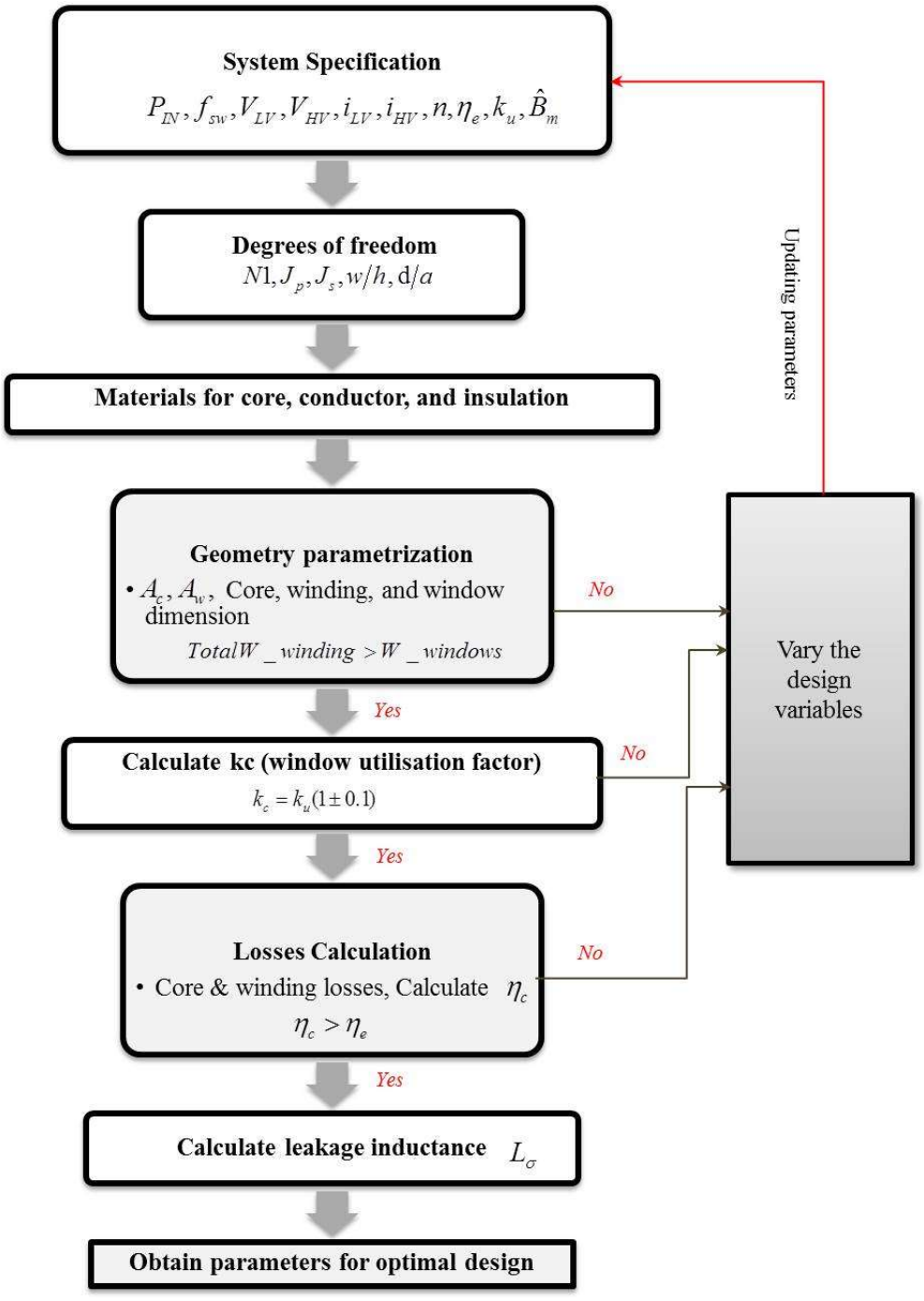


Figure 4. 3 Design flow-chart of the 3DAB transformer

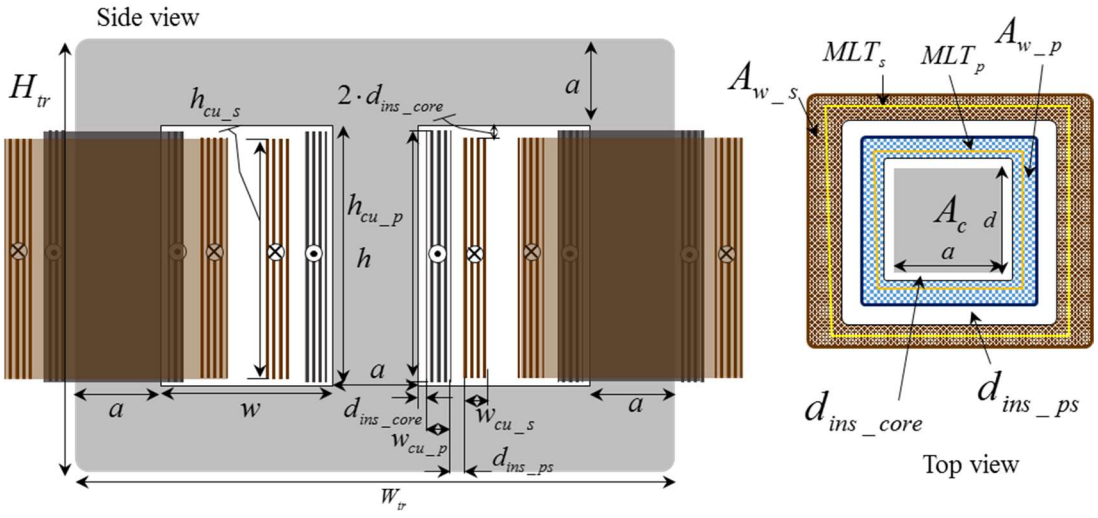


Figure 4. 4 Dimension of the transformer

4.2.2 Core design

Using the peak flux density equation in [85], the core sectional area, A_c can be calculated as

$$A_c = \frac{V_{an}^{\ 2}}{k_f \cdot f_{sw} \cdot \hat{B}_m \cdot N_1} \tag{4.7}$$

where, k_f is the waveform coefficient, equal to 4.0 for square waveform or 4.44 for sine waveform [85, 153]. To calculate the waveform coefficient, a sinusoidal AC current is applied to the input terminal of an ideal transformer without considering copper loss, as shown in Fig. 4.5.

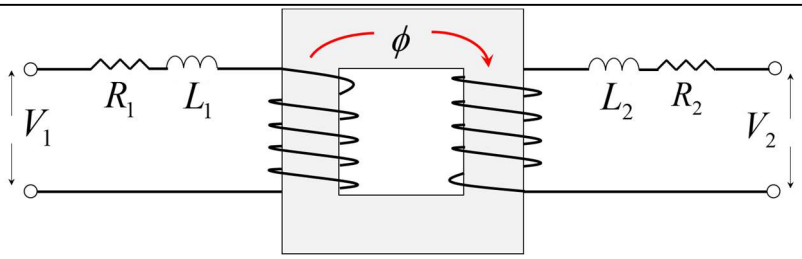


Figure 4. 5 Ideal transformer equivalent circuit on no load

According to Faraday's law of electromagnetic induction, the corresponding primary voltage is $v_1 = \mathrm{d}\phi / \mathrm{d}t = N_1 \omega_{sw} \hat{B}_m \cos \omega_{sw} t$ and RMS value of the voltage is calculated as:

$$V_1 = \left(\frac{1}{\sqrt{2}} \right) \cdot N_1 \omega_{sw} \hat{B}_m \cos \omega_{sw} t = 4.44 N_1 f_{sw} \hat{B}_m \tag{4.8}$$

where, the waveform coefficient of the sine waveform can be defined as $k_f = \left(1/\sqrt{2}\right) \cdot 2\pi \approx 4.44$. Similarly, the waveform coefficient of the square waveform can be calculated according to the Fourier series as $k_f = \left(4\sqrt{2}/2\pi\right) \times \left(2\pi/\sqrt{2}\right) = 4$.

To simplify the calculation, the geometry ratio of A_c is used. By using the ratio and solving for *a,d* shown in Fig. 4.4, distance 'a_{core}' can be calculated as

$$a_{core} = \sqrt{\frac{A_c}{n_{da}}} \ , d_{core} = A_c / a_{core} \tag{4.9}$$

4.2.4 Winding area design

To determine a suitable american wire gauge (AWG), the basic parameters of current and current density can be calculated as follows:

$$A_{cu} = \frac{I}{J} \tag{4.10}$$

Using this reference value, one of AWGs is selected and the new effective conductor area is calculated. The conductor diameter is given as:

$$d_{cu} = 2 \cdot \sqrt{\frac{A_{cu}}{\pi}} \tag{4.11}$$

Using the calculated diameter, the conductor cross section area can be expressed as

$$A_{cu_p} = \frac{\pi}{4} \cdot d_{cu}^{\,2} \tag{4.12}$$

Substituting Eq. (4.12) with (4.10), the effective current density can be derived as:

$$J_p = \frac{I_p}{A_{cu_p}} \tag{4.13}$$

The effective conductor area can be calculated using number of turns in the windings. The primary conductor area can be calculated as:

$$A_{w_p} = N1 \cdot A_{cu_p} \tag{4.14}$$

Similarly, the secondary conductor area is calculated as:

$$A_{w_s} = N2 \cdot A_{cu_s} \tag{4.15}$$

The total conductor area can be calculated by summing Eq. (4.14) and (4.15).

$$A_{w_cu} = A_{w_p} + A_{w_s} \tag{4.16}$$

In the three-phase core-type transformer depicted in Fig. 4.4, conductor windings for two phases are arranged in the one-window area. Using Fig. 4.4, the window area for the three-phase transformer is given as follows:

$$A_a = 2 \cdot \frac{A_{w_cu}}{k_u} \tag{4.17}$$

where, k_u is the window utilisation factor. The window utilisation factor is the number of conductor windings in the window area and must be less than 1. In this case, 0.4 is applied for the factor. The dimensions of the window area can be calculated using the *w/h* ratio as follows:

$$w = \sqrt{\frac{A_a}{n_{wh}}} \ , h = A_a / w \tag{4.18}$$

In power electronics applications, increasing the operating frequency enables significant reduction of the core size of the transformer, but the power losses are increased. Consequently, it makes the cooling more difficult. Furthermore, skin and proximity effects are increased, resulting in increased winding losses. The current density is based on the specified cooling system. The calculated conductor diameter must be kept smaller than twice the skin depth of the operating frequency in order to keep the skin effect to the minimum. If the calculated diameter is larger than twice

the skin depth, parallel strands are added to satisfy the condition. The skin depth can be calculated as follows:

$$\delta = \sqrt{\frac{\rho_{cu}}{\pi \cdot f_{sw} \cdot \mu_r \cdot \mu_0}} \tag{4.19}$$

where, ρ_{cu} is the resistivity of the conductor and for copper, this value is 1.68×10^{-8}. μ_r is the relative magnetic permeability of the conductor and μ_0 is the permeability of free space, which has the value of $4\pi \times 10^{-10}$ H/mm. In terms of copper, $\mu_r = \mu/\mu_0 = 0.999994$. where the permeability of copper is $\mu = 1.256627 \times 10^{9}$[H/mm]. Using above equations and Fig.4.4, the overall dimension of the transformer can be calculated as:

$$\begin{aligned} W_{tr} &= 2 \cdot w + 3 \cdot a_{core} \\ H_{tr} &= 2 \cdot a_{core} + h \\ D_{tr} &= d_{core} \end{aligned} \tag{4.20}$$

Finally, the volume of the core used to derive the core loss is calculated as:

$$vol_{core} = \left(A_c \cdot (3 \cdot h + 4 \cdot w) + 6 \cdot a_{core}^2 \cdot d_{core}\right) \cdot 10^{-9} \quad [\mathrm{m}^3] \tag{4.21}$$

4.2.5 Isolation layer's calcuation

The designed isolation level's influence on the power density must be included in the design process. Furthermore, the isolation level must meet the international standards. Partial discharge (PD) must be considered at the medium voltage level above 3 kV. The PD can destroy the isolation layers over time. In this design, DUPONT™ NOMEX PAPER TYPE 401[41] was considered. This manufacturer recommends that continuous dielectric stress level of isolation material not exceed

1.6 kV/mm to avoid the risk of PD. The required isolation level can be expressed with a minimum clearance distance as shown in Fig. 4.6.

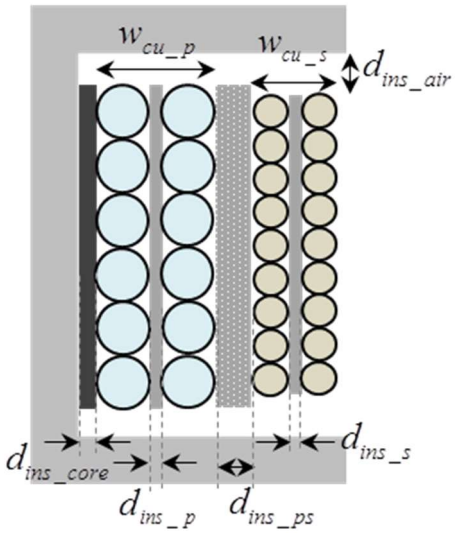


Figure 4. 6 Winding width dimensions

The required isolation distance between the core and primary conductor area can be calculated as follows:

$$d_{ins_core}=k_s\cdot\left(V_{pn}/E_{s_ins}\right) \tag{4.22}$$

where E_{s_ins} is dielectric strength of the isolation material given by the manufacturer and k_s is the safety factor, typically 1.2 – 1.5 in this case. V_{pn} is the voltage applied in the isolation layers. Eq. (4.22) can be similarly used for calculating the insulation thickness between the conductors as follows:

$$d_{ins_ps}=k_s\cdot\left((V_{pn}+V_{sn})/E_{s_ins}\right) \tag{4.23}$$

where the voltage applied to the insulation layers is equal to the sum of the primary side and secondary side voltages. An isolation layer is also required on each winding

turn of both conductors. For primary side turns, the isolation distance can be derived as:

$$d_{ins_p} = k_s \cdot \left((V_{pn} / N1) / E_{s_ins} \right) \tag{4.24}$$

Whereas the isolation distance for secondary side turns can be derived as:

$$d_{ins_s} = k_s \cdot \left((V_{sn} / N2) / E_{s_ins} \right) \tag{4.25}$$

The calculated window utilisation factor, k_c, with a 10% increase for safety should not be greater than the estimated value of $k_u = 0.4$, which is fixed in this case. If the estimated value is greater, the calculated value is taken as the initial value and the design is repeated. The resulting isolation distances need to be recalculated and total width of conductor area must be smaller than the width of the window area. If this condition is not fulfilled, the design is discarded and new free parameters are set up to execute a new design iteration. The total width of the conductor area can be expressed as:

$$\begin{aligned} w_{cu_tot} &= 2 \cdot (d_{ins_core} + w_{cu_p} + d_{ins_ps} + w_{cu_s}) \\ &= 2 \cdot \left(d_{ins_core} + \underbrace{\frac{A_{w_p}}{h_{cu_p}} + d_{ins_p} \cdot N1}_{\text{width of primarycu}} + d_{ins_ps} + \underbrace{\frac{A_{w_s}}{h_{cu_s}} + d_{ins_s} \cdot N2}_{\text{width of secondary cu}} \right) \\ &= 2 \cdot \left(d_{ins_core} + \underbrace{\frac{A_{w_p}}{h - 2 \cdot d_{ins_core}}}_{h_{cu_p}} + d_{ins_p} \cdot N1 + d_{ins_ps} + \underbrace{\frac{A_{w_s}}{h - 2 \cdot \left(\frac{d_{ins_core}}{n} \right)}}_{h_{cu_S}} + d_{ins_s} \cdot N2 \right) \end{aligned} \tag{4.26}$$

4.3 Power losses

With the defined geometric dimensions, it is required to calculate power losses in the transformer. Power loss is split in two sections.

4.3.1 Copper losses

In order to calculate copper loss, winding resistance must be calculated using mean length per turns (MLT) and number of turns as follows:

$$\begin{aligned} R_p &= \frac{\rho_{cu} \cdot N1 \cdot MLT_p}{A_{cu_p}} \\ R_s &= \frac{\rho_{cu} \cdot N2 \cdot MLT_s}{A_{cu_s}} \end{aligned} \tag{4.27}$$

where ρ_{cu}, the resistivity of the copper and MLT, for each windings can be calculated as shown in Fig. 4.4. By substituting Eq. (4.11), (4.12), and (4.27), primary and secondary side copper losses can be calculated as:

$$P_{cu_tot} = P_{cu_p} + P_{cu_s} = 3 \cdot R_p \cdot I_{prms}^2 + 3 \cdot R_s \cdot I_{srms}^2 = 3 \cdot \left(R_p \cdot I_{prms}^2 + R_s \cdot I_{srms}^2 \right) \tag{4.28}$$

4.3.2 Core loss

Core loss can be expressed using Steinmetz equation. The core loss [W/kg] consists of hysteresis and eddy current loss and is given as:

$$P_{s0} = \underbrace{k_h \cdot f_{sw}{}^{\alpha} \cdot B_m{}^{\beta}}_{\text{hysteresis}} + \underbrace{k_e \cdot \left(f_{sw} \cdot B_m\right)^2}_{\text{eddycurrent}} \tag{4.29}$$

Finally, to determine the transformer core loss, the weight of the core is multiplied with the specific core losses calculated and is given as:

$$P_s = P_{s0} \cdot weight_{core} = P_{s0} \cdot \rho_s \cdot vol_{core} \tag{4.30}$$

where ρ_s is the mass density of the core material given by the manufacturer. Now, it is possible to calculate the efficiency of the transformer using the power losses. The resulting efficiency must be higher than the expected design value. If this performance is not fulfilled, the design is discarded and new free parameters are set up to execute a new process.

4.4 Calculation magnetising current

Magnetising current is required to saturate the core to the peak operating flux density. In the analytical simulation model of the 3DAB converter, only the leakage inductance of the high-power MF transformer was used and the effect of the magnetising inductance was neglected. However, in practice, the magnetising inductance has an impact on the transformer and converter losses. In fact, the ratio of the magnetising inductance is not large owing to design optimisation and manufacture of the transformer. In the 3DAB converter, the magnetising current leads to additional reactive current in order to achieve the ZVS operation in low-power transfer conditions. An example of the effect of magnetising current on switching states in the 3DAB converter is shown in Fig. 4.7. As seen in Fig. 4.7, magnetising current lags the phase voltage in the primary bridge, and secondary current leads to the phase voltage in the secondary bridge. As a consequence, the power electronics switches in the primary bridge turn on with a lagging current. Therefore, the anti-parallel diode conducts the current prior to the turn-on of the active semiconductor switch (IGBT), resulting in ZVS turn-on. For the secondary

bridge, the switch is turning on with ZVS, and turn-off with quasi-ZVS owing to the leading current. Consequently, the magnetising current needs to be determined in the design aspects, such as enabling ZVS operation and additional loss in the transformer.

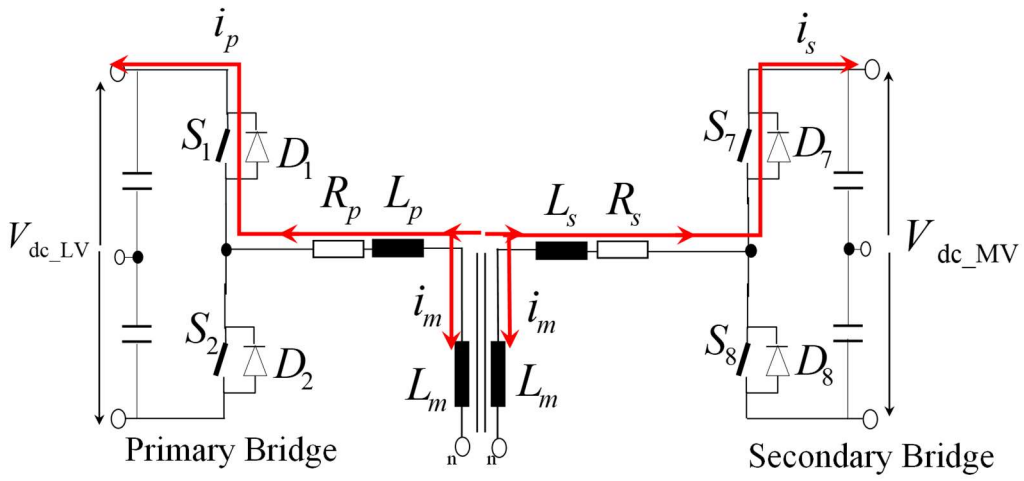


Figure 4. 7 The effect of magnetising current on switching state

The non-oriented silicon steel M-19 29-gauge material was selected for the 2D FEA design. This material is suitable for large-size and dry-type transformers as well as for operations in the medium frequency ranges (up to 2000 Hz). Using the B-H curve of the material as shown in Fig. 4.8, the magnetising force H (at_{core}, at/m) corresponding to flux density B_m in the core and H (at_{yoke}, at/m) corresponding to flux density in the yoke can be calculated.

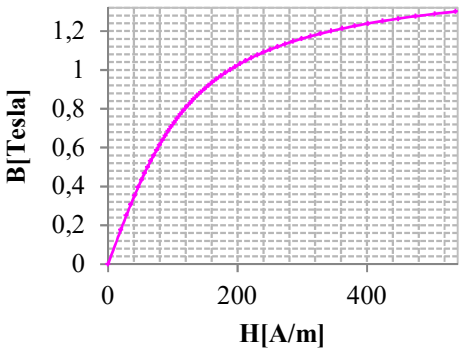


Figure 4. 8 Magnetisation curves: M-19 29 Ga Silicon steel

The required magnetomotive forces (MMF) for the core and yoke can be calculated as:

$$\begin{aligned} MMF_{core} &= 3 \cdot h_W \cdot \mathrm{at}_s \\ MMF_{yoke} &= 4 \cdot w_W \cdot \mathrm{at}_{yoke} \end{aligned} \tag{4.31}$$

The MMF drop at the edges is 5–10% higher than the theoretical value, so the total MMF can be calculated as:

$$MMF_{tot} = 1.1 \cdot \left(MMF_{core} + MMF_{yoke} \right) \tag{4.32}$$

Peak value of the magnetising current is

$$I_{m_peak} = \frac{MMF_{tot}}{3 \cdot N1} \tag{4.33}$$

Finally, the RMS value of the magnetising current is

$$I_{m_rms} = \frac{I_{m_peak}}{\sqrt{2}} = \frac{1.1 \cdot \left(MMF_{core} + MMF_{yoke} \right)}{3 \cdot N1 \cdot \sqrt{2}} \tag{4.34}$$

In this case, a 10% increase in the value of MMF is considered owing to flux concentration at the corners of the window.

4.5 Calculation of leakage inductance

In order to ensure soft switching of the 3DAB converter, a specific value of series inductance is required. Therefore, the leakage inductance, L_σ, has a strong impact on the performance of the 3DAB converter, e.g. the power flow and the range of the phase-shift angle. Since leakage inductance directly impacts the transferring of energy, it is important to determine the required value of the inductance to optimise the medium-frequency transformer for a high-power density design. In the 3DAB converter, the phase-shift angle φ should be kept as small as possible to avoid unnecessary reactive power circulation in the AC-linked parts, which may reduce the efficiency [175]. A smaller L_σ offers a wide range of soft-switching controls, which can be obtained at different voltage ranges [134, 135]. Furthermore, since φ is reduced by the smaller L_σ, the turn-off current on the switches will be reduced. Hence, the switching losses can be minimised. In practical application, the phase-shift angle φ cannot be too large in order to reduce the current stress and the circulating energy [154, 181]. The maximum ratio of the power factor to the reactive power, kVAr, is obtained in the range with a smaller phase-shift angle φ as shown in Fig. 4.2. A large phase-shift angle φ results in a reduced power factor, which indicates increased switch conduction losses and decreased converter efficiency. Therefore, typically, the maximum phase-shift angle of the 3DAB converter, corresponding to the full load, should be limited to 60°. However, its value must be enough to be able to generate active power and retain the desired output voltage level.

High switching frequency at high-power levels can significantly reduce the transformer size as well as the size other passive components, including inductors and capacitors. The small-size components can also reduce parasitic parameters and improve the power density. However, with increased switching frequency, the resolution of the phase-shift angle may become an issue for a digital modulator in a digital controller [173]. High-resolution digital phase-shift modulation solutions for high-switching frequencies (100 and 50 kHz) are introduced in [173]. For example, to generate 500-kHz switching frequency with a 150-MHz DSP clock frequency that generates a 6.67-ns clock period for the high-power DAB converter, the resolution of

the phase-shift modulation is 4.0% when $\varphi_{\max} = 30°$ which is insufficient to regulate the power flow and voltage of the DAB converter because the phase-shift angle is divided into around 20 steps. Typically, 500 steps for the phase-shift angle can be considered acceptable for the high-resolution digital PWM modulator. With this criterion, the effective switching frequency should be in the medium-frequency range below 25 kHz for $\varphi_{\max} = 30°$. In practical application, therefore, a sufficient resolution methodology for a switching frequency of 1 kHz and $\varphi_{\max} = 30°$ will be required to achieve accurate power and voltage control. From Eq. (A.10) and (A.11) in Appendix A, the targeted value L_σ for the 3DAB converter can be calculated as:

$$L_\sigma = \frac{V_{pri}^2}{\omega_{sw} P_o} \cdot d \cdot \varphi \left[\frac{2}{3} - \frac{\varphi}{2\pi} \right] \qquad \text{for} \left(0 \le \varphi \le \pi/3 \right) \tag{4.35}$$

This inductance is defined by the leakage inductance of the transformer design. As published in [37], Eq. (4.36) represents a calculation of L_σ using geometry depicted in Fig. 4.4.

$$L_\sigma = \mu_0 \cdot N1^2 \cdot \frac{MLT_p}{h} \cdot \left(\frac{w_{cu_p}}{3} + d_{ins_ps} + \frac{w_{cu_s}}{3} \right) \tag{4.36}$$

From the transformer design specification, the resulting L_σ must be validated for the soft switching performance. Also, the calculated L_σ must be not higher than the allowed maximum value calculated from Eq. (4.35). From the design consideration of 3DAB converter, the required φ is calculated as:

$$\varphi \le \frac{\pi}{3} \tag{4.37}$$

For a 4-MVA rated transformer for the 3DAB converter with 1100-VDC input rating, the allowed maximum value of L_σ is calculated to be $25.2\mu H$. Finally, the resulting L_σ is used to calculate the required phase-shift angle, corresponding to the full load. Using Eq. (4.36), the required phase-shift angle can be calculated as:

$$\varphi = \frac{2\pi}{3} - \sqrt{\left(\frac{2\pi}{3}\right)^2 - 2\pi \cdot \frac{P_o \cdot \omega \cdot L_\sigma}{V_{pri} \cdot V'_{\text{sec}}}} \tag{4.38}$$

where, $V'_{\text{sec}} = n \cdot V_{\text{sec}} = \frac{w_{pri}}{w_{\text{sec}}} \cdot V_{\text{sec}}$

4.6 Optimisation of the trasformer

4.6.1 Optimisation process

Once all analytical designed parameters have been defined, they must be sorted for defined object function and also be validated. Fig. 4.9 shows an optimisation process for the analytical design. In this design, a set of five degrees of freedom is selected for optimisation. The optimisation loop consists of three steps. In the first step shown in Fig. 4.9, all calculated parameters must be compared with the required criterion to be met by the developed design. In the next step, accepted geometric designs with the calculated leakage inductance L_σ are validated using the 2D FEA simulation for sinusoidal excitation. Once the FEA validations are satisfactory for all the requirements, 3DAB converter simulation using PLECS is carried out using the calculated L_σ and control phase-shift angle. In this step, the PLECS simulation generates the actual non-sinusoidal waveforms. Using this actual waveform, 2D FEA is performed to compute the losses of the non-sinusoidal transformer. In the final

step, the resulting performance must be compared with the requirements and if the design does not meet the expectations then it is discarded. Again, all the designs that deliver the expected performance are sorted for a defined objective function to determine the optimum design.

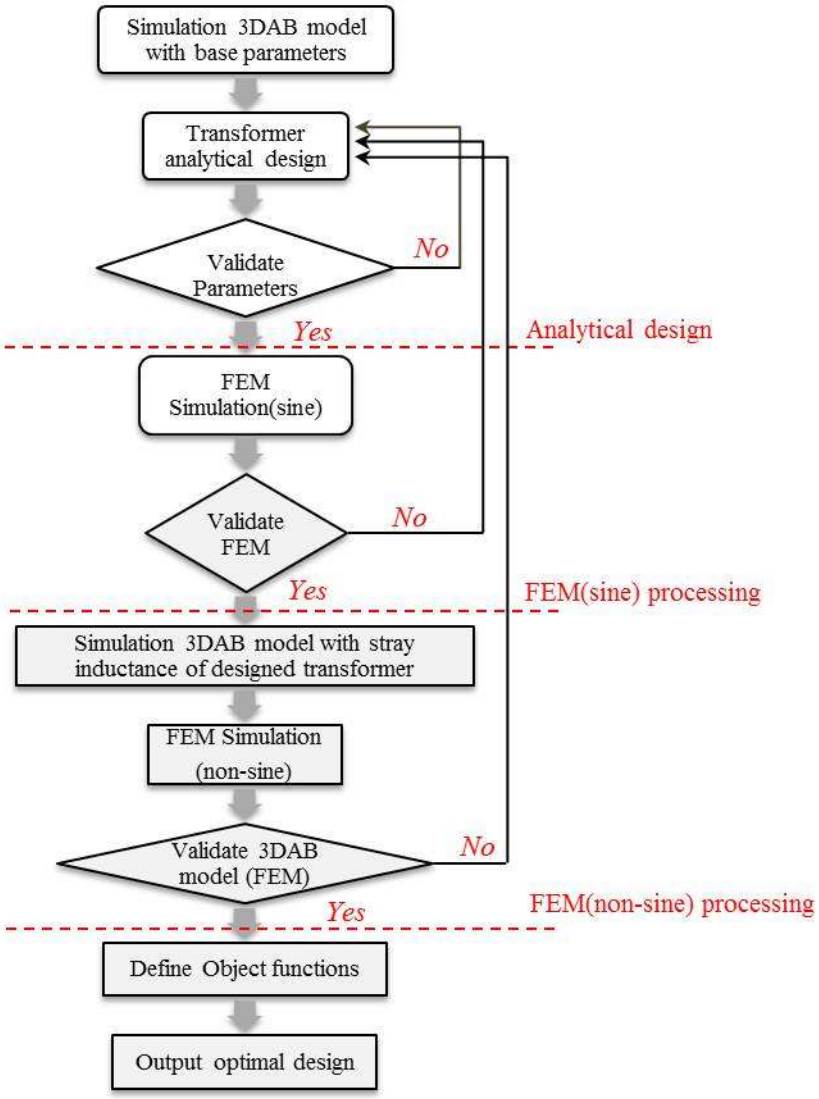


Figure 4. 9 Optimisation process

4.6.2 Objective Functions

For the transformer design optimisation approach under consideration, efficiency, total weight, and leakage inductance need to be maximised for the minimisation of

the overall cost. For performance optimisation, the maximal efficiency is obtained according to:

$$\eta_{\max} = \min(P_{core}, P_{cu}, I_{mag}) \text{ and} \geq \eta_{e} \tag{4.39}$$

$$obj_{\text{fun}} = \frac{\eta_{e}}{P_{core} \cdot P_{cu} \cdot I_{mag} \cdot W_{tot} \cdot L_{\sigma} \cdot T_{rise}} \tag{4.40}$$

The presented optimisation employs the minimal L_{σ} in order to determine the minimal φ for low switching loss. In general, for a cost-optimised design, the minimal total weight [kg] is required to obtain the lowest material cost. The total weight (W_{tot}) is the sum of the weight of the LV ($weight_{LV}$), HV windings($weight_{HV}$) and the weight of the core magnetic material. The total manufacturing cost is equal to the sum of the total weight of the transformer and the labor cost to manufacture the transformer. For the design process, the cost of material is taken as the total production cost of the transformer. The cost of transformer materials (CTM) is expresses as:

$$\text{CTM} = (uc_{LV} \cdot weight_{LV} + uc_{HV} \cdot weight_{HV} + uc_{core} \cdot weight_{core}) \tag{4.41}$$

where, uc_{LV} is the unit cost (£ or €/kg) of the LV winding, uc_{HV} is the unit cost of the HV winding, and uc_{core} is the unit cost of the core material. For example, core is one of the most costliest material of the transformer. In medium-frequency, high-power applications, silicon steel and amorphous iron are considered common magnet materials [135, 176, 177]. However, amorphous iron material is the higher manufacturing unit cost ((£ or €/kg), especially at high power levels [152].

The magnetic materials and windings are the principal sources of losses and result in temperature rise of the transformer. The heat converted from the losses in the transformer is transmitted by conduction, convection, and radiation. The heat must be dissipated without reaching a temperature that will deteriorate the insulation. In 4-MVA rating transformer, the Oil Natural and Air Natural (ONAN) method can be applied. In the oil-immersed transformer, in addition, the paths of the heat flow are as

follows: from the internal hot spot to the outer surface in contact with oil, from the outer surface to the oil, from the oil to the tank surface area, finally transmitted to the cooling medium-air directly. The allowable temperature rise of the oil and windings depends on the ambient temperature, geometry design, cooling system, and loading conditions. According to IEC 60076-2 [42], a limit on top oil temperature rise of 60°C is recommended with a maximum ambient temperature of 40°C. The windings temperature rise of 65°C is specified for ON (Oil Natural) cooling arrangements. In the ONAN transformer, convection is mainly responsible for heat dissipation generated by the losses occurring in the core and windings. Heat dissipation of the transformer oil due to convection is:

$$P_c = h_c A(T_{surface} - T_{oil}) \tag{4.42}$$

where, h_c is specific heat dissipation coefficient (W/m^2), and A is surface area (m^2). The heat transfer coefficient for convection is given as:

$$h_c = k_c \left(\frac{\Delta T}{H} \right)^{0.25} \quad W/m^2\ ^\circ C \tag{4.43}$$

where, ΔT is the temperature rise of the surface relative to oil (°C), H is height of the dissipating surface (m), and k_c is the coefficient of oil, which is estimated to be 40.3. The transformer tank may be able to dissipate heat in radiation and natural convection. The heat dissipation by radiation is expressed as:

$$P_r = k_r \varepsilon S_t (T_s^4 - T_a^4) \tag{4.44}$$

Where, $k_r = 5.7 \times 10^{-8} W/m^2$ is the Stephan-Boltzmann constant, ε is the surface emissivity factor, S_t is the surface area, and T_s and T_a are absolute temperature of radiating surface and ambient air, respectively. The tank surface area is determined in order to establish specific dissipation of the transformer tank. According to [11],

specific heat dissipations due to radiation and convection account for about 6 W/m^2 and 6.5 W/m^2 of surface area, per °C between the tank and ambient respectively. If the dissipations are insufficient, cooling tubes can be added to increase the area. The cooling tubes increase the circulation of oil and hence improve the convection heat dissipation. However since the cooling tubes are added, the heat dissipation is increased. For a temperature rise of 60°C above the ambient temperature of 40°C, the specific heat dissipations are as follows: h_r is specific heat dissipation by radiation (=6 W/m^2) and h_c is specific heat dissipation by convection (=6.5 W/m^2). Finally, the temperature rise of oil on the tank can be calculated as:

$$\Delta T = \frac{P_s + P_{cu}}{(h_r + h_c) \cdot S_t} [°C] \tag{4.45}$$

4.6.3 Optimisation results

This optimisation was required to design a three-phase transformer with a 3DAB converter for 4 MVA-rated offshore wind farms. For the present work, two configurations were considered, depending on the output voltage of wind generators as shown in Fig. 4.10. Generally, a 690 VAC-rated generator is considered. However, it has high line current as well as high cost and power dissipation in the cable. An alternative solution of 3.3 kVAC was considered to improve the system efficiency.

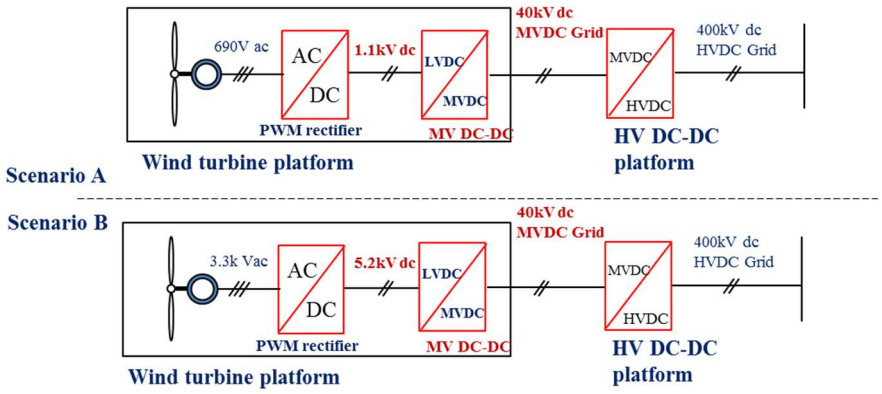


Figure 4. 10 Possible configurations of MVDC grid for 4MW offshore wind farms

The process of finding the optimum transformer parameters was implemented with the combination of suitable software programmes (Matlab and Infolytica MagNet), which use five input parameters in order to make the transformer optimisation as parametric as possible. The software programmes allow many variations in design variables. These variations permit the evaluation of sufficient candidate functions. For each one of the candidate functions, it is necessary to check if all the design specifications are satisfied; then, a 2D FEA programme is implemented and the function is characterised as 'acceptable'. Finally, among the acceptable functions, the transformer with the maximum efficiency is selected, which is the optimum transformer. The search algorithm (loops of the software programme) of the optimisation is presented as below.

Update of degrees of freedom

```
For N1 = 1:1:200
    For Jp = 1:1:10
        For Js = 1:1:10
            For hw_ratio = 0.1:0.1:2.5
                For da_ratio = 0.1:0.1:2.5

                        Calculation of numer of secondary widing turns
                        Core design
                        Winding design
                        Calculation Effective Skin depth
                        Overall dimensions of transformer
                        Transformer Core Volume [m^3]
                        Calculation insulation
                        Calculate total winding width using insulation layer
                        Calculate window utilisation factor, ku
                        Calculation mean length of turns
                        Calculation leakage inductance
                        Calculation Power losses
                        Calculation Transformer efficiency
                        Calculation Temperature rise
```

If (the calculated width of the window are is higher than the total winding width) and (0.9*estimated value <= the calculated window utilisation factor <= 1.1*estimated value) and (the final calculated efficiency is higher than the required minimum value of 95%)

When all conditions are accepted, then the next loop for a 2D FEA solution is started. On the other hands, if one of these conditions is violated, then the solution is rejected and the next loop is executed.

```
2D FEA running
2D FEA Input Parameters (The number of turns on primary winding, current density
for each windings, window area ratio, and core cross sectional area ratio)
2D FEA Analysis Outputs
2D FEA Magnetizing Current Outputs

end
            end
          end
        end
      end
   end
end

Save Input Parameters
Save Analytical 3DAB converter simulation outputs
Save 2D FEA Analysis Outputs
Save 2D FEA Magnetizing Current Outputs

for i = 1:1:45
   for j = 1:1:row_res
      Make optimisation results table
   end
end

Exit the 2D FEA program
Close the 2D FEA program file
```

The complete software for the optimisation can be found in Appendix H. The optimisation programme calculates and simulates a number of candidate cases are acceptable or rejected.

The result of the optimisation for each degree of freedom, which in this case consists of the five free parameters where the maximum, minimum, and step values, can be seen in Fig. 4.11. Fig. 4.11 shows the dependence of the optimisation output figures, i.e. efficiency, weight, and leakage inductance, for each of the free parameters. These figures were obtained from the for loop function of the programme. For example, the next inner loops of the four free parameters change

with each iteration of the loops in order to provide a unique value for the individual iterations of the outer loop (N1). In case of N1 = 20, 113 candidate solutions for the free parameters corresponding to the accepted sets of the optimisation outcome showing the efficiencies are analysed. From the step values, one can determine where the maximum and minimum efficiencies are recorded. In the same way, the optimisation programme finds that a total of 30 solutions are acceptable for the case of Jp = 6 A/mm^2. From the graphs, optimised efficiency and weight are found at [N1=20, Jp=6, Js=6, hw_ratio = 2.5, da_ratio=0.5] and [N1=20, Jp=10, Js=9, hw_ratio=2.5, da_ratio=0.5], respectively. As a result, the objective functions are optimised at N1 = 20. From this plot (number of turns in Fig. 4.11), it can be observed that there is more design flexibility (and possibility of maximising the performance) for a smaller number of turns in the primary winding. Also, it is worth noting that all the designs have their peak flux density in close proximity of 1.2T which is the assumption placed at the beginning of the design process.

Fig. 4.12 shows the result of optimisation for each degree of freedom. From the Fig. 4.12, the optimised efficiency, cost, and leakage inductance are determined at [N1=70, Jp=6, Js=6, hw_ratio = 2.5, da_ratio=0.5], [N1=74, Jp=10, Js=9, hw_ratio=2.5, da_ratio=0.5], and [N1=70, Jp=6, Js=6, hw_ratio=2.5, da_ratio=0.5], respectively. Thus, the performance (efficiency and leakage inductance) of the transformer can be optimised for 70 primary turns (N1). On the other hand, the cost can be optimised for 74 primary turns of the transformer.

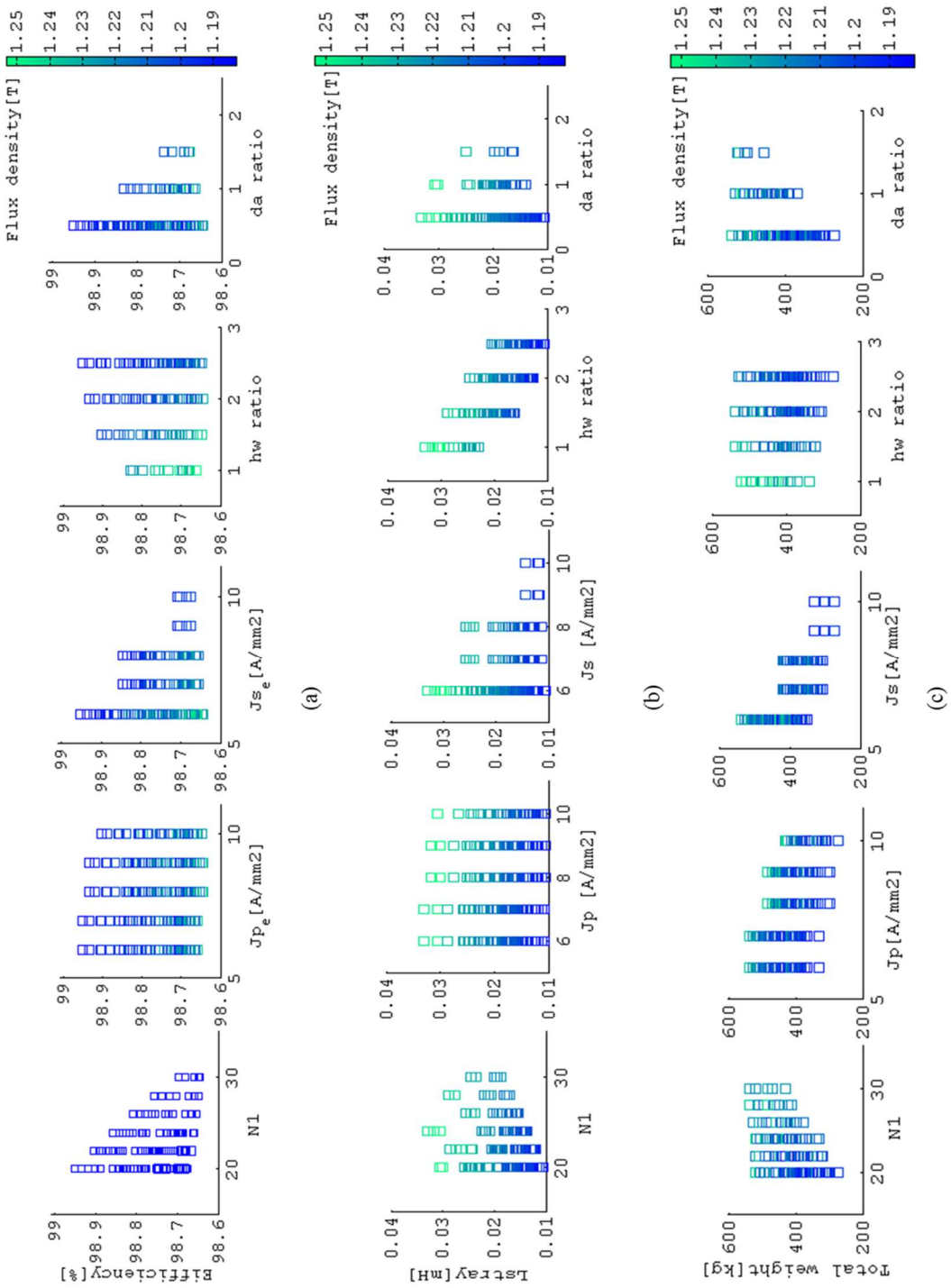


Figure 4. 11 Efficiency, total weight and leakage inductance versus degrees of freedom of 1.1kVDC input rating

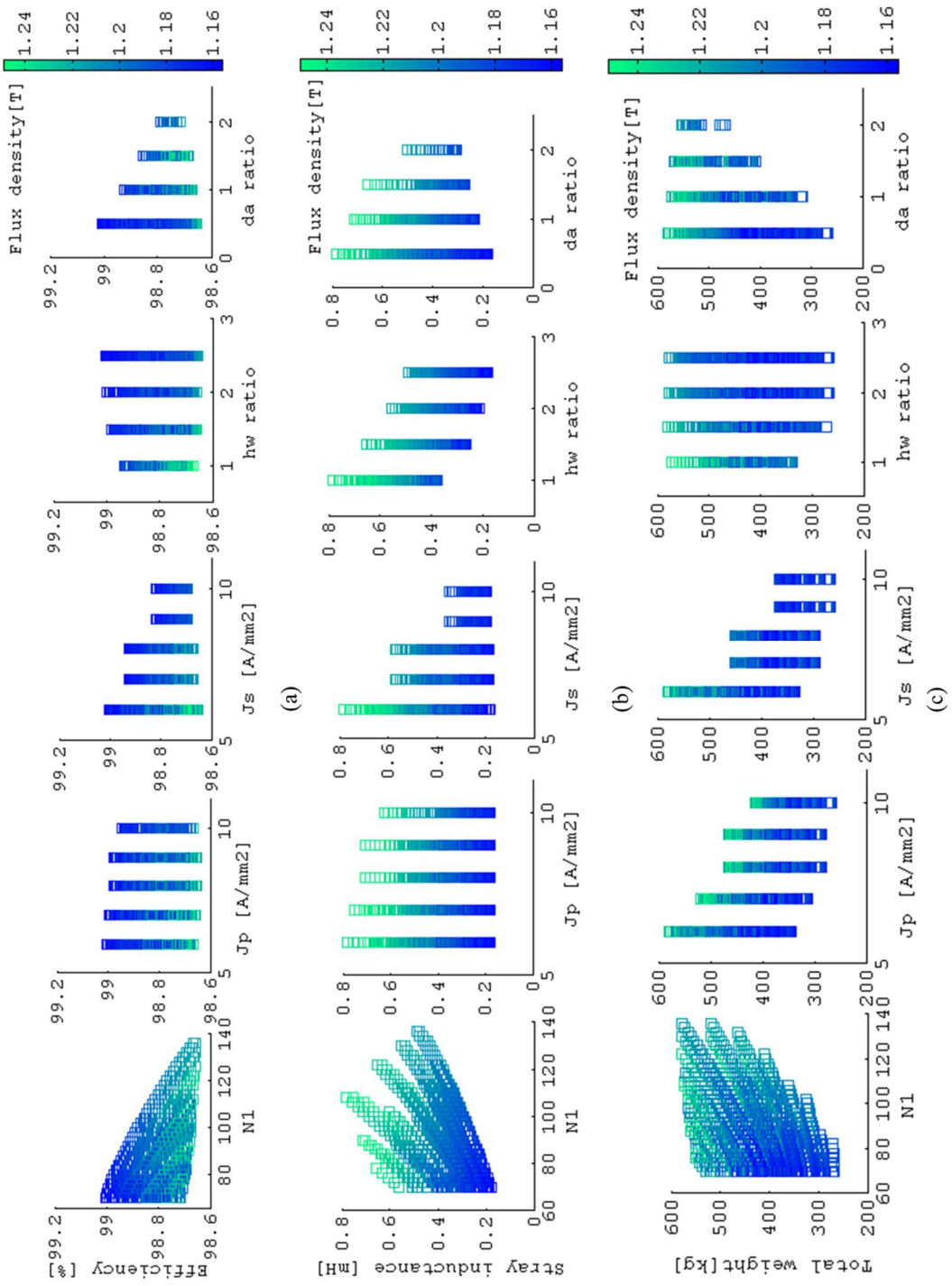


Figure 4. 12 Efficiency, total weight and leakage inductance versus degrees of freedom of 5.2kVDC input rating

A comparison of the different scenarios is illustrated in Fig. 4.13. Each dot represents a design case of the 3DAB transformer and the dots show in terms of efficiency is over 98.6%. Its colour shows the achieved temperature rise of the top oil. The maximum allowed temperature rise for the top oil is 60°C with a maximum ambient temperature of 40°C. If the temperature rise exceeds the allowed value, the suitable number of cooling tubes or radiators must be mounted additionally on the vertical sides of the transformer. The cooling tubes would be not proportional to the increase in surface area because the tubes prevent the radiation from the tank surface area. However, the cooling tubes increase circulation of oil, so the convection would be improved. As can be seen, the maximum temperature rise of top oil for each of the scenarios is achieved at lower than 50°C. It is worth noting that the temperature of oil increased with weight reduction of the transformer (with this construction, the power density of the transformer is increased). For 1.1-kVDC converter design, the maximum achievable efficiency of the transformer is 98.95% with a total weight of 412 kg. It should be noted that the design considerations must meet the requirements. In addition, increasing the transformer size has a higher cost impact owing to the increase in the weight of the transformer. Therefore, it is important to identify which case must be given the best design in terms of efficiency and manufacturing cost. The obtained results for the 4-MVA transformer with the 5.2 kVDC-rated 3DAB converter are shown in Fig. 4.13(b) in terms of the efficiency with respect to total weight. The maximum reachable efficiency is 99.00% with a weight of 415 kg, whereas the minimal weight is achieved as 268 kg which 98.75% achievable efficiency.

It can be seen that the 3DAB transformers designed with 5.2 kVDC input rating have higher efficiency for the same weight in both the cases. From the graph, the maximum efficiency is 99.00% in the case of 5.2 kVDC input rating whereas the maximum efficiency is 98.95% with 1.1 kVDC rating. Furthermore, it is obvious that many more available design considerations can be achieved with the 5.2 kVDC input rating.

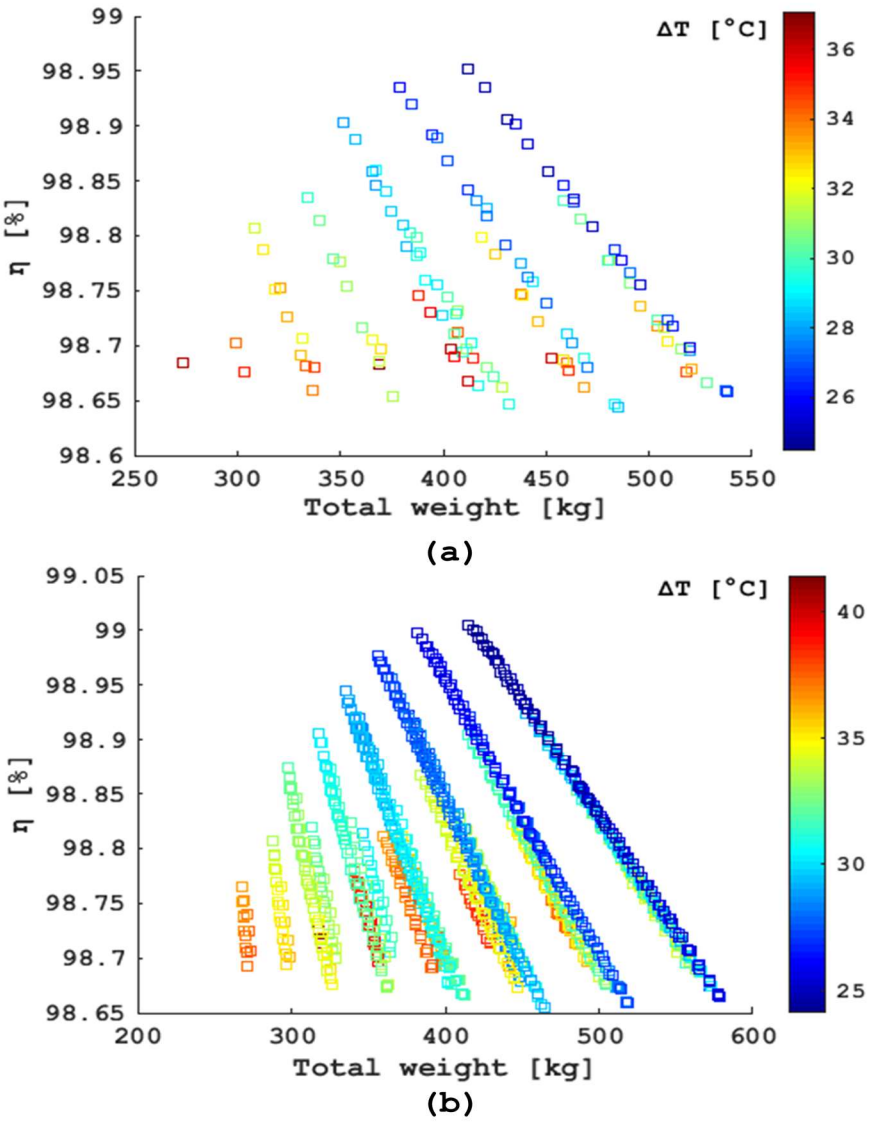


Figure 4. 13 Comparison of efficiency versus total weight for the two scenarios: (a) a transformer design for 4MW 3DAB converter with 1.1kVDC rated input voltage and (b) a transformer design for 4MW 3DAB converter with 5.2kVDC rated input voltage

4.6.4 Comparison of non-sinusoidal and sinusoidal excitations

For use in the high-power DC-DC conversion system, losses under non-sinusoidal and sinusoidal excitation need to be evaluated. In order to compare both excitations, the same RMS value of the current was applied to the proposed design procedure to achieve a designed geometry parameter. Fig. 4.14 shows the simulated primary side current waveforms of 4 MVA transformers of 1.1 kVDC input for 2 applied excitations with the same condition.

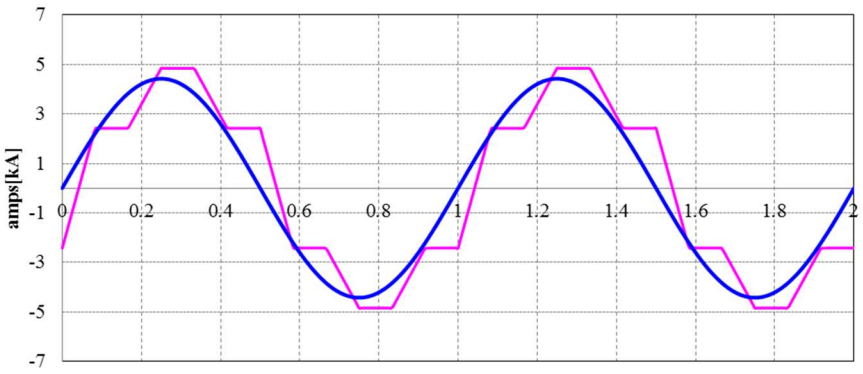


Figure 4. 14 Comparison between simulated primary current waveforms of non-sinusoidal and sinusoidal excitations for a 4MVA transformer of 3DAB converter having 1.1kVDC input

Table 4. 1 Comparison of losses between non-sinusoidal and sinusoidal excitation for a 4MVA transformer of 3DAB converter having 1.1kVDC input rating

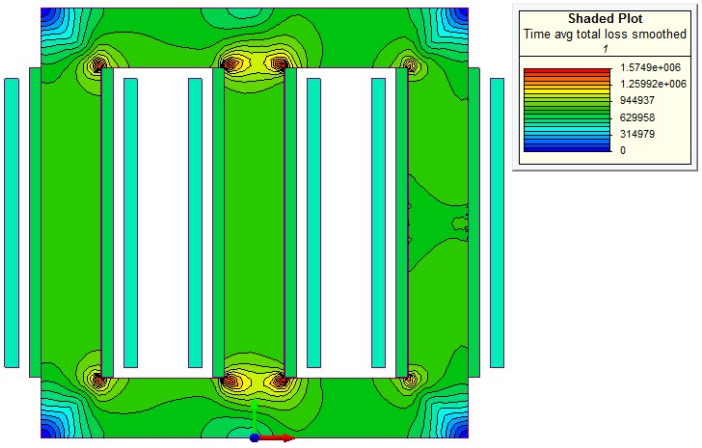
4MVA, N1=20		Non-sinusoidal	Sinusoidal
Core loss [kW]		13.159	11.811
Cu loss [kW]	Primary	9.376	7.813
	Secondary	17.861	14.887

Table 4. 2 Comparison of losses between non-sinusoidal and sinusoidal excitation for a 4MVA transformer of 3DAB converter having 5.2kVDC input rating

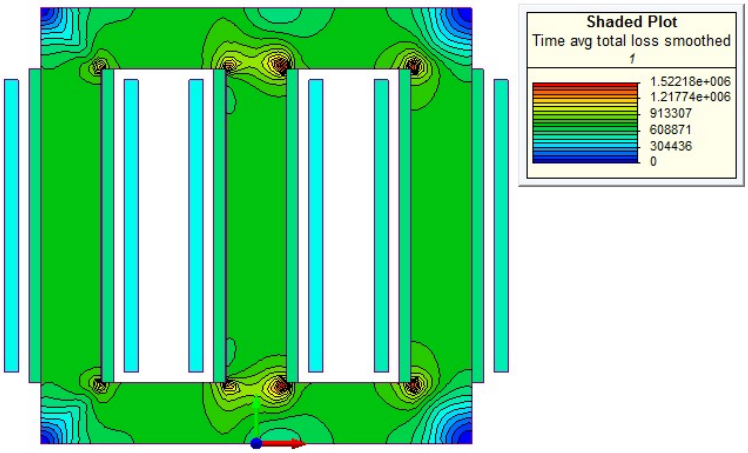
4MVA, N1=70		Non-sinusoidal	Sinusoidal
Core loss [kW]		16.654	14.993
Cu loss [kW]	Primary	6.982	5.818
	Secondary	14.706	12.207

Comparisons between power losses of the non-sinusoidal excitation applied from the switched current waveforms of the 3DAB converter and sinusoidal waveforms are given in Table 4.1. 2D FEA-simulated total average losses of core and windings

of both cases are also shown in Fig. 4.15. The unit of the evaluated average losses is in W/m^3. It is clear that the sinusoidal approach leads to good performance-oriented design results. Table 4.2 and Fig. 4.16 show the comparison results in case of the high primary voltage condition (5.2 kVDC).

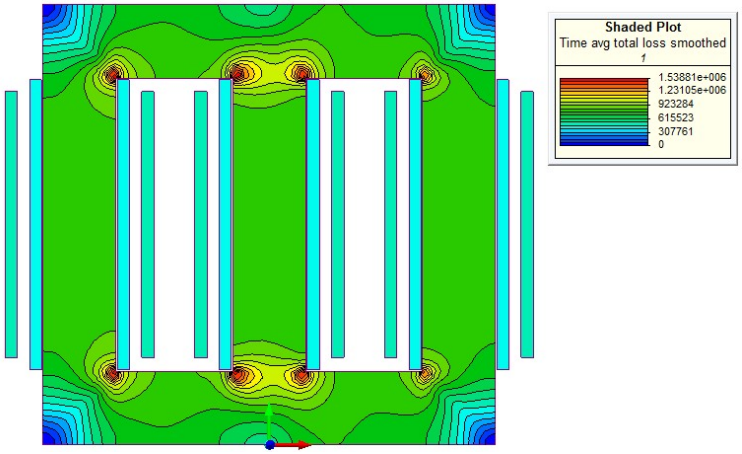


(a)

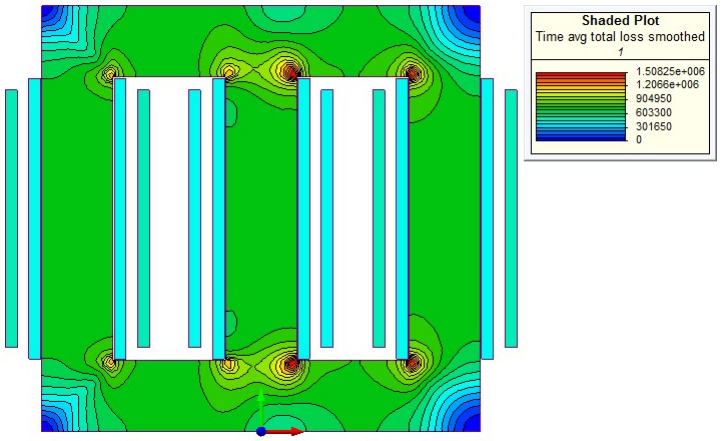


(b)

Figure 4. 15 Comparison of average losses in W/m^3 between simulated primary current waveforms of non-sinusoidal and sinusoidal excitations for a 4MVA transformer of 3DAB converter having 1.1kVDC input



(a)



(b)

Figure 4. 16 Comparison between average losses in W/m^3 of (a) non-sinusoidal and (b) sinusoidal excitations for a 4MVA transformer of 3DAB converter having 5.2kVDC input rating

4.7 Discussion of optimised transformers

Optimal design of transformer is generated for 1.1 kVDC and 5.2 kVDC rated input voltage using the design optimisation algorithm discussed in section 4.2. In order to validate the proposed optimised-design methodology, two 4 MVA rated transformers (rated 1.1kVDC and 5.2kVDC input) were validated using 2D FEA and compared. The design details for these transformers, for 1.1 kVDC and 5.2 kVDC, are given in Table 4.3.

Table 4. 3 Design Details of Optimal Transformers

		Input rating	
		1.1kVDC	5.2kVDC
Winding	*Jp[A/mm²]*	6	6
	Js[A/mm²]	6	6
	N1:N2	20:727	70:538
Geometry [mm]	*d/a*	0.5	0.5
	w/h	2.5	2.5
	a [mm]	103.9376	120.7936
	d [mm]	51.9688	60.3968
	w [mm]	214.7704	192.2856
	h [mm]	536.9261	480.7140
	Wtr [mm]	741.3536	746.9520
	Htr [mm]	744.8013	722.3012
	Dtr [mm]	51.9688	60.3968
	L_σ [μH]	10.79	178.71
	Volume [m³]	0.0167	0.02142
	Total [kg]	412.33	415.23

The designed transformers are validated using 2D transient FEA. Table 4.4 shows the comparison between the results obtained analytically and those obtained by 2D transient FEA.

Table 4. 4 Performance Comparison of Optimal Transformers

			Input rating	
			1.1kVDC	5.2kVDC
Losses	Core[kW]	Analytical	12.85	16.53
		FEA	11.81	14.99
	Winding [kW]	Analytical	27.30	21.66
		FEA	27.24	21.69
	Imag[A]	Analytical	226.54	60.17
		FEA	234.73	46.34
	η[%]	Analytical	98.90	98.92
		FEA	98.95	99.01
Bm [T]		Assumed	1.2	1.2
		FEA	1.1829	1.1565

The performance comparison presented here shows a good match between the analytical and the FEA results. The leakage inductances of the optimised transformer are used for the 3DAB converter simulation. The resulting waveforms are shown in Fig. 4.17 for both 1.1 kVDC and 5.2 kVDC rated input voltages. The non-sinusoidal excitation waveforms, generated from 3DAB converter simulation, are then used to perform a 2D transient FEA to determine the performance of the designed transformer for the actual (non-sinusoidal) excitation.

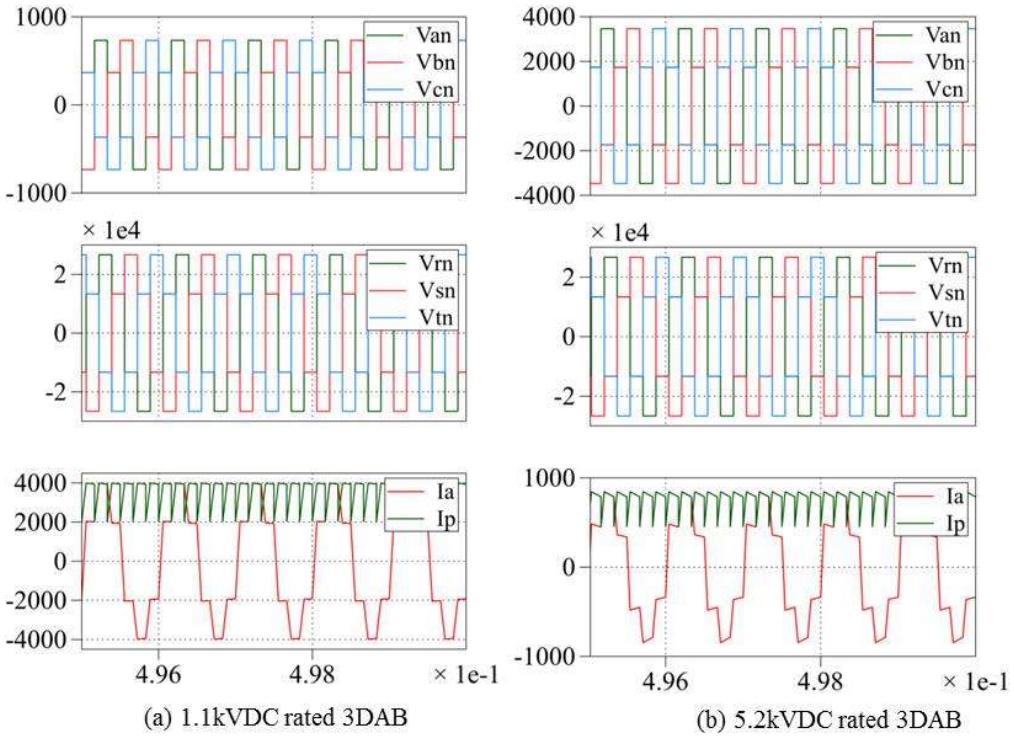


Figure 4. 17 3DAB simulation for the optimised transformer (a) 1.1kVDC rated voltage and (b) 5.2kVDC rated voltage

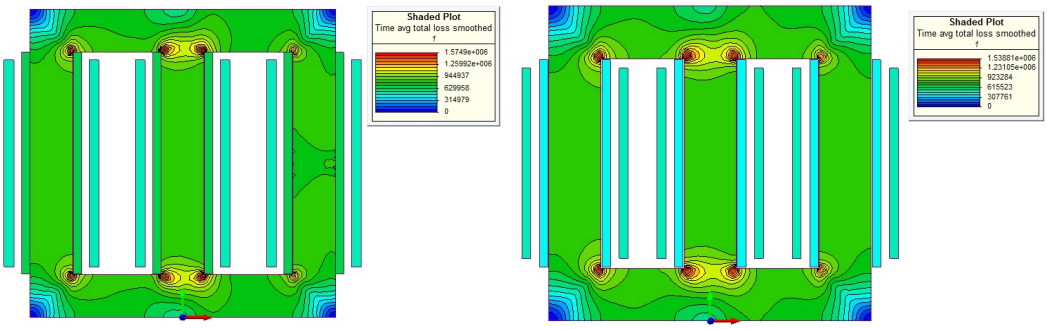
4.7.1 Comparison of 2D FEA results

To determine the copper loss using the 2D FEA simulation, Eq. (4.46) is applied.

$$P_{cu_tot} = 3 \cdot P_{\max_p} \cdot \sqrt{2} \cdot \frac{MLT_p}{d_{core}} + 3 \cdot P_{\max_s} \cdot \sqrt{2} \cdot \frac{MLT_s}{d_{core}} \tag{4.46}$$

Fig. 4.18 shows the distribution of core loss and copper loss in the selected two scenarios, respectively. For the evaluation of the power losses, the DC input voltages rated at 1.1 kV and 5.2 kV were chosen for the simulation. The total losses in the transformer mainly comprised core and copper losses in the primary and secondary windings. At the full load condition, the copper loss in the secondary winding is considerably high compared to other losses in case of the 1.1 kVDC 3DAB owing to high winding resistance. The core loss is close to 13 kW and the primary winding has

approximately 9 kW of copper loss. On the other hand, the core loss is significantly higher than both the copper loss, in primary and secondary, for part loading condition of 25%, 50%, and 75% of transferred load. For the 25% load condition, it can be seen that the power dissipated in the core with a loss of over 90% is the main loss compared to other losses. The situation results are similar in case of the 5.2 kVDC 3DAB system. Only around 5% of the total loss occurs in both windings during the 25% load condition since over 90% of the total loss is produced in the core. In case of Fig. 4.19(b), the core loss is the main loss at all the operating load points. The core loss proportion deceases with increasing load to approximately 50% of the total loss at the full-load condition. On comparing core loss of configuration Fig.4.19(b) to Fig. 4.19(a), it can be observed that the core loss increases more (5–20%) than that in the configuration Fig. 4.19(a). This is mainly due to the fact that a rise with input voltage level and the voltage drop across the leakage inductances can reduce the magnetising voltage. Fig. 4.20 shows a comparison of the efficiency of the two cases. It can be observed that at the full-load, a better performance is achieved in the case of 5.2 kVDC rating. However, the performance of the 3DAB transformer operated by the 5.2 kVDC input rating is worse than with the 1.1kVDC rating in all the other load conditions (apart from the full load condition).



(a) (b)

Figure 4. 18 Comparison between average losses in W/m^3 of (a) 1.1kVDC rated and (b) 5.2kVDC rated a 4MVA transformers of 3DAB converter

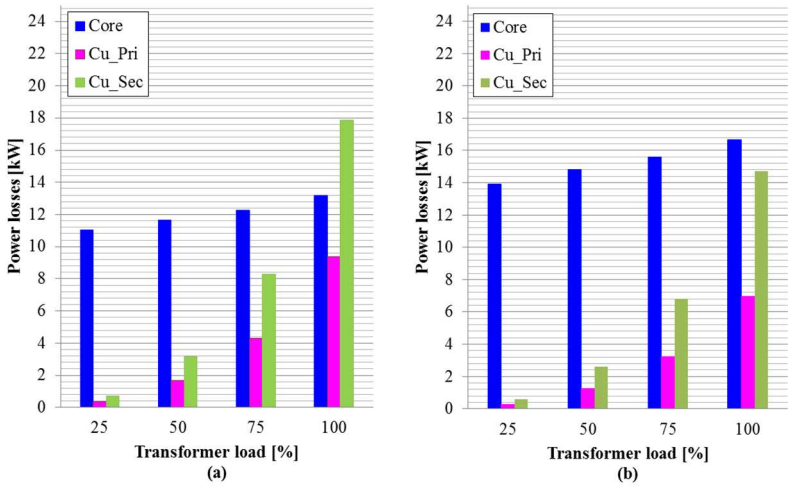


Figure 4. 19 Power losses of the transformer with (a) 1.1kVDC and (b) 5.2kVDC input rating

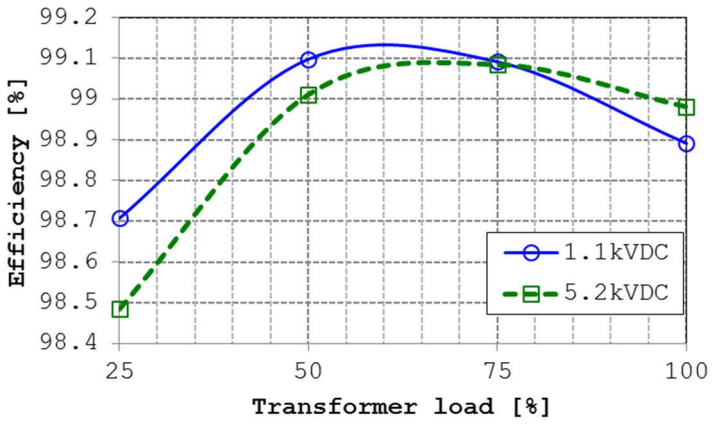


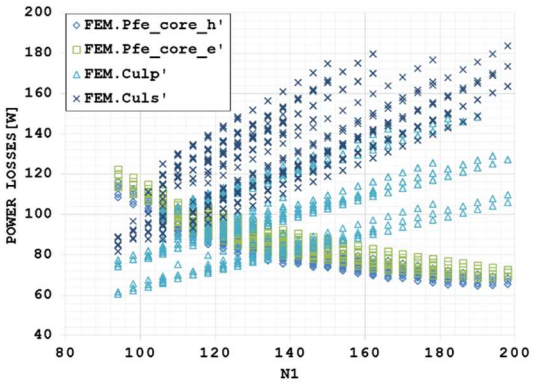
Figure 4. 20 Efficiency of the transformer (a) 1.1kVDC, (b) 5.2kVDC input ratings.

4.8 Scaled down version of the designed transformer for testing

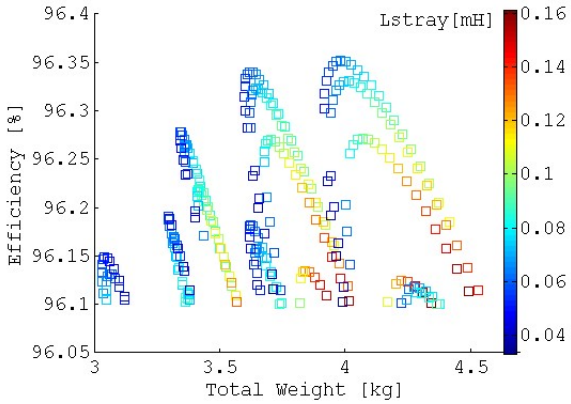
4.8.1 Design specifications of the scaled down version

The proposed design and optimisation presented in the previous sections is used to set the dimensions for a medium frequency prototype transformer. The design inputs were specified for the 10 kW 3DAB DC-DC converter with V_{in} = 500VDC, V_{out} = 1000 VDC, turns ratio = 0.5, and frequency = 1 kHz. A silicon steel lamination E core was chosen for the core design because of low hysteresis losses and for

minimising the use of expensive finite elements. Fig. 4.21 shows the performance prediction of the 10 kW transformers, which were optimised before the mentioned procedure. As can be seen from Fig. 4.21(a), winding loss increased with the increasing number of turns of the primary winding whilst core loss decreased. The efficiency graphs in Fig. 4.21(b) are very helpful, since they allow optimum selection of the transformer for the given transformer VA rating and frequency and in terms of leakage inductances, which could be used for 3DAB DC-DC converter optimisation as well. Using these results, the optimum parameters were chosen in order to be assembled and tested.



(a)



(b)

Figure 4. 21 Performance prediction of the 10kW transformer: (a) power losses versus N1, (b) efficiency versus total kg of the transformer

Design details of the optimised transformer are listed in Table 4.5. All the results were calculated and validated from the above procedure. Using these results, an optimised transformer prototype was manufactured for experimental characterisation and validation. Fig. 4.22 shows a picture of the three-phase prototype transformer. This transformer consists of two silicon steel-laminated sections (E-core and D-core) and two thermocouples, which are used to monitor the temperature in the windings. The primary and secondary windings are star connected.

Table 4. 5 Optimised transformer specification at 1kHz

Winding	*Jp[A/mm²]*	6
	Js[A/mm²]	6
	N1:N2	94:188
Geometry [mm]	*d/a*	0.5
	w/h	2.5
	a [mm]	31.7
	d [mm]	16.5
	w [mm]	35.3
	h [mm]	88.2
	Wtr [mm]	165.5
	Htr [mm]	744.8
	Dtr [mm]	51.9
Loss	Core [W]	237.4
	Winding [W]	147.6
	Imag[A]	2.4
	Efficiency [%]	96.1
L_σ [μH]		33.9
Bm [T]		1.02
Volume [m³]		3.11e-4
Total weight [kg]		4



Figure 4. 22 A 10kW/1kHz prototype of 3DAB transformer

4.8.2 Experimental characterisation of the 1kHz transformer

Injection of actual excitation waveforms

In order to measure the B-H loop and consequently the core loss, the transformer prototype is connected with a high precision testing facility. The measurement setup can be seen in Fig. I.1 (Appendix I) in which the transformer prototype is used as the step-up transformer.

To validate the influence of the non-sinusoidal excitation in the transformer, piecewise linear excitation of the winding current, shown in Fig. 4.23 obtained from a 3DAB converter simulation model, is applied to the manufactured prototype using BROCKUAUS measurements [180]. High-precision test equipment is used to carry out core material characterisation of the transformer. The obtained waveforms of the converter are saved into the operating software parameters for the measuring programmes. The software enables programme-controlled operation for the start of the measurement of the transformer. The shapes of the current can be introduced by six-step time intervals. For each interval, the terminal voltages are constants. The shapes of the current can also be changed depending on the phase-shift angle between the two bridges of the 3DAB converter. Using these excitation waveforms, the specific losses for the transformer used in the 3DAB converter are determined.

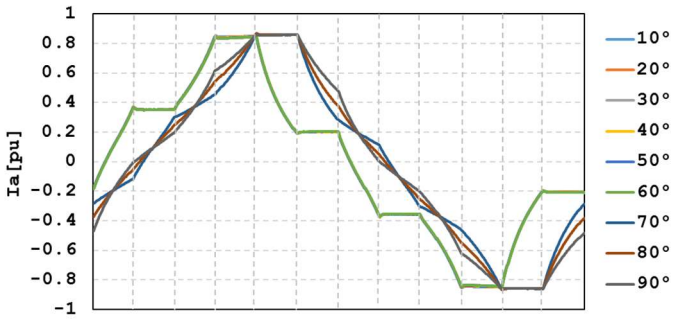
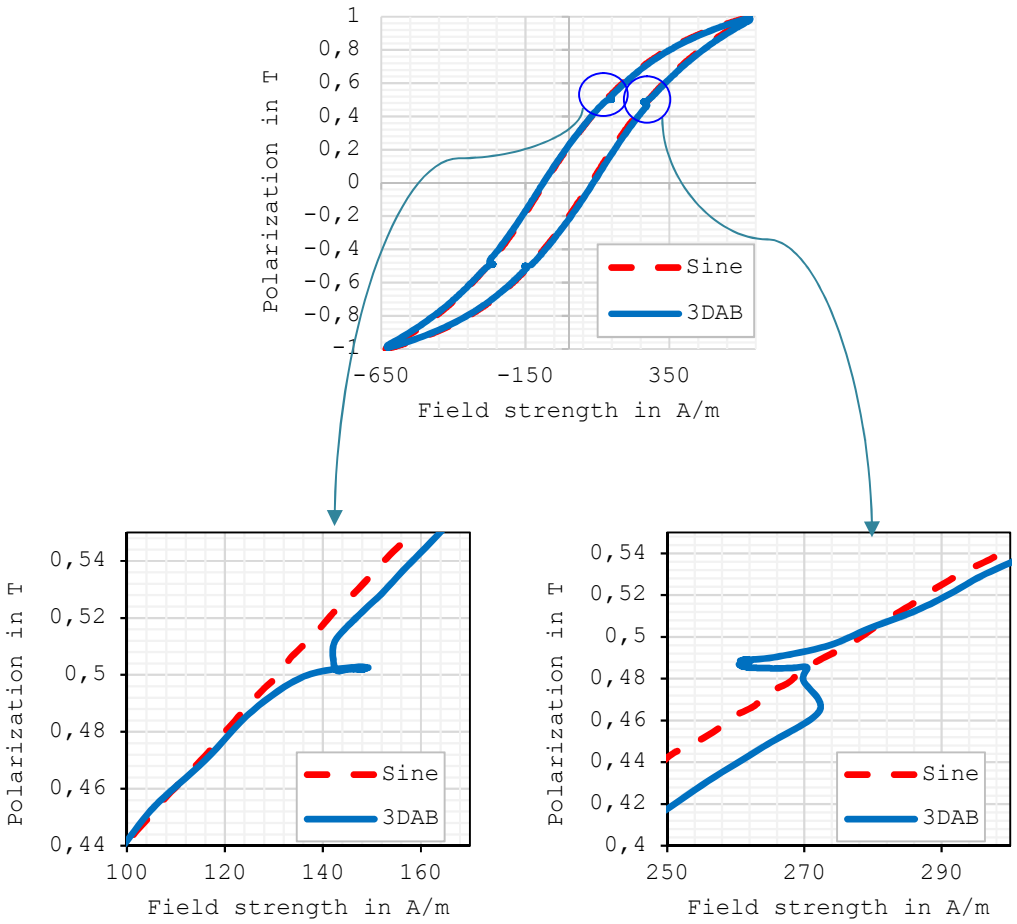
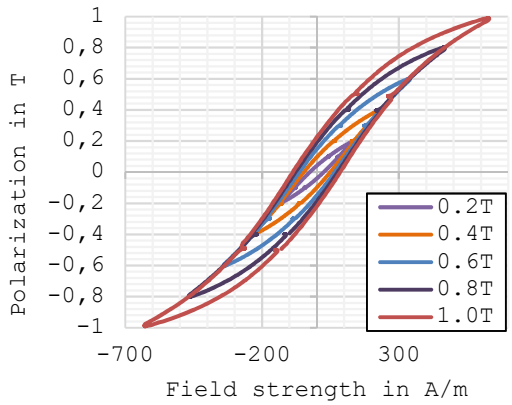


Figure 4. 23 Nonsinusoidal excitation waveforms of currents on primary winding

4.8.3 Measured hysteresis loops



(a)



(b)

Figure 4. 24 Hysteresis loops: (a) comparison between sinusoidal and 3DAB excitation at 1.0 T, (b) at between different polarizations

To determine the performance of the manufactured transformer for the actual non-sinusoidal excitation of the 3DAB converter, the core losses for the actual waveforms of the converter need to be determined. The measured hysteresis loops at two different excitations and by different polarisations are shown in Fig. 4.24. In Fig. 4.24(a), the blue solid graph represents non-sinusoidal 3DAB excitation whereas the red-dashed graph represents sinusoidal excitation. It can be seen that the area spanned by the hysteresis loop of the 3DAB excitation is slightly larger; as a result, the specific core losses for the 3DAB excitation tend to be higher than those for pulse sinusoidal excitation.

4.8.4 Core loss characterisation

Fig. 4.25 shows the measured transformer core losses in an actual piecewise waveform of 3DAB for different peak flux densities and the phase-shift angle. It can be seen that the losses as well as the peak flux density decreases with an increasing phase-shift angle.

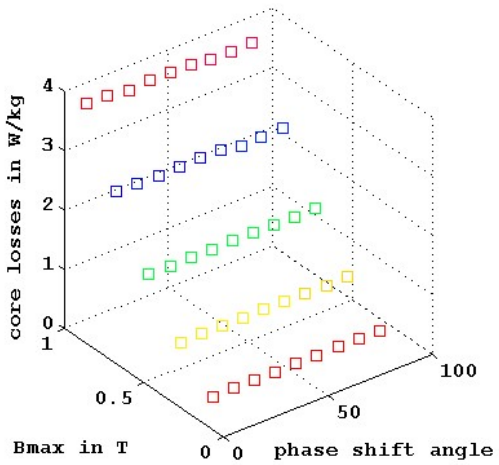


Figure 4. 25 Measured core losses in the 3DAB transformer

4.8.5 Transformer's efficiency measurement in a 10kW prototype converter

The developed transformer was evaluated with a 10-kW prototype 3DAB converter. Experimental validation was carried out in the voltage operating range, i.e. at nominal primary DC voltage of 500 V and secondary DC voltage of 1000 V as well as fundamental frequency of 1 kHz. The prototype converter was investigated under open-loop conditions. Only the positive phase-shift angles were implemented, since power is flowing from the low-voltage primary bridge to the high-voltage bridge. For the efficiency measurement, two precision PPA 2530 power analysers were connected with the primary winding and secondary winding. The primary winding resistance values of 0.0916 Ω and 0.3781 Ω in the secondary windings were measured using a winding precision ohm meter and RLC meter. The winding losses were calculated based on the measured resistance values.

Fig. 4.26 shows the loss distribution diagram of the developed three-phase MF transformer. The illustrated losses were interpolated from the selected power levels of rated power. The losses were separated into primary winding, secondary winding, and core. From the diagram, it can be seen that the core loss clearly dominates overall transformer losses owing to the low current rating on the transformer windings at the high-voltage levels. It has further been illustrated that a transformer designed with high-efficiency amorphous material can potentially reduce core losses to one-third that of the conventional silicon steel-laminated core. Fig. 4.27 shows the relative efficiency in relation to the transferred power levels. The transformer efficiency rises with 65% power level and drops slightly towards the rated power. From the plot, the transformer shows the best performance at 6.5 kW transferred power with the maximum efficiency of 96.84%. At rated power, the efficiency is aproximately 96.51%. It can be observed that efficiencies above 91% are achieved at all the power levels. Table 4.6 shows the comparison between the analytical and measured losses of the designed transformer. The obtained values are a close match.

Table 4. 6 Comparison of the analytical and measured losses

Parameter		Analytical	Experimental	% Variation
Loss	Core [W]	237.4	215.6	10.12%
	Winding [W]	147.6	138.7	6.42%
	Imag[A]	2.4	2.26	6.19%
	Efficiency [%]	96.3	96.6	0.32%
$L_\sigma[\mu H]$		30.6	33.9	9.74%

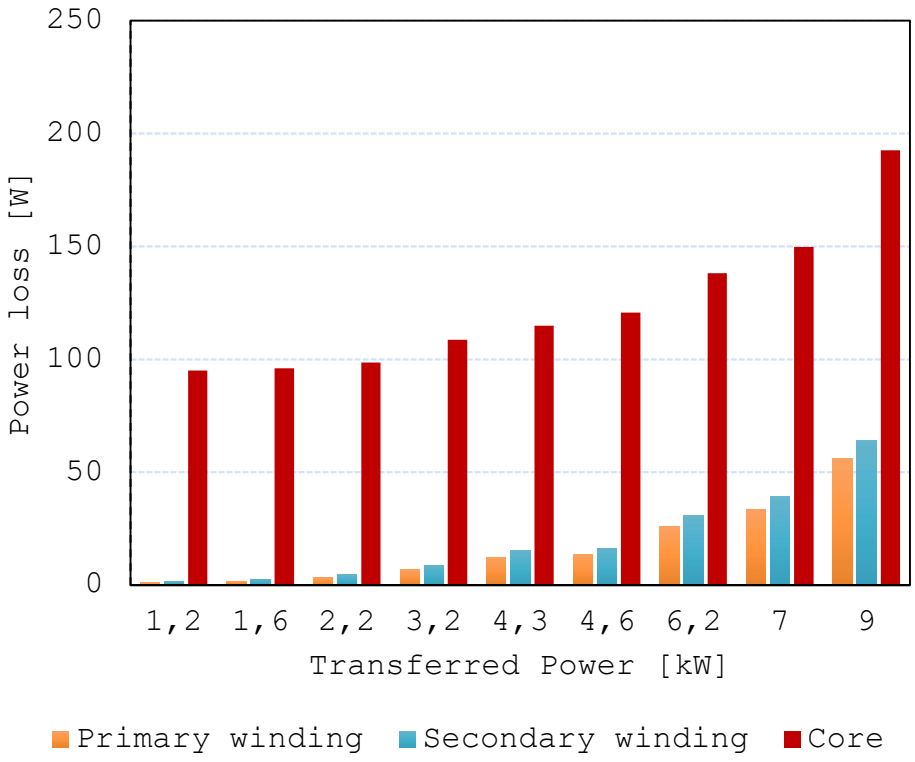


Figure 4. 26 Loss distribution diagram of the 3DAB transformer in the 10kW prototype converter at Vin = 500V and Vout = 1000V with operating frequency = 1k Hz.

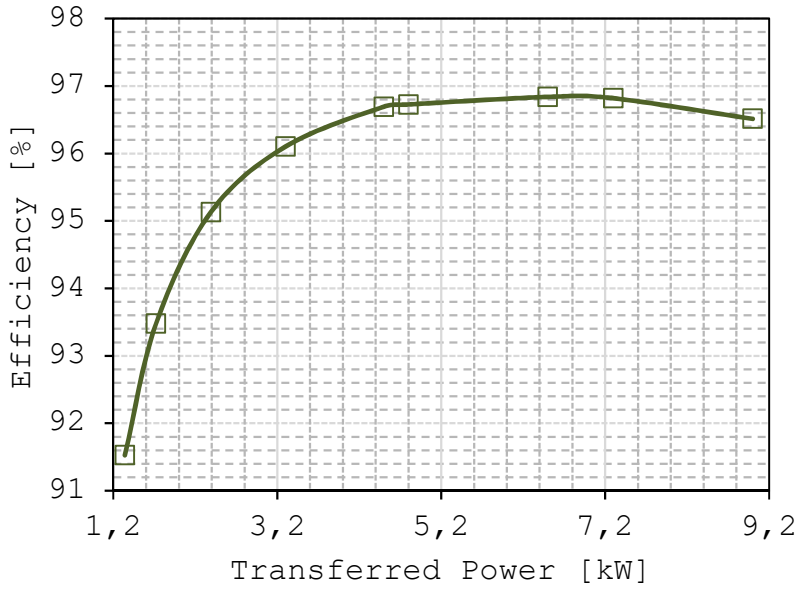


Figure 4. 27 Measured efficiency of the 3DAB transformer in the 10kW prototype converter at Vin = 500V and Vout = 1000V with operating frequency = 1kHz.

4.9 Summary

This chapter presented a design approach and optimisation routine for a three-phase 4 MW/1 kHz transformer in a 3DAB DC-DC converter for a 40-kV MVDC grid. Analytical calculations indicate that the transformer could be designed with over 98.5% efficiency. The main objective of the design and optimisation methodology is not only to determine optimal geometric parameters and calculate maximum efficiency during the optimisation but also to implement it on high-power conversion applications operated at medium frequency range. Furthermore, this methodology contributes to the design of a three-phase high-power transformer operating under non-sinusoidal excitation.

The procedure for optimum design was applied on a core-type transformer designed with a non-oriented silicon steel core. The investigation on the optimisation loop shows efficiency versus volume and the sensibility of degrees of freedom such as the number of turns on the primary winding. Finally, the optimisation was validated by 2D FEA simulation. Measurements show that the measured peak flux density is lower than the expected value. Also, the 2D FEA results of core loss and

copper losses in both windings confirm that the core loss is higher than the winding losses since the transformer operates below full-load condition.

A 10kW prototype transformer on a 1000 V DC supply system at rated power of 10kW was manufactured in order to validate the proposed optimum design procedure. The measurements from experimental validation indicate that the developed transformer, which forms the magnetic link in 3DAB converter topology, reached the maximum efficiency of 96.84%.

Chapter 5

Design of a small-scale experimental converter

5.1 Introduction

Considering that the 3DAB Converter is intended for MVDC applications, an ideal validation would have been an implementation at comparable high power (4MW) and medium voltage (up to 40kV) operating conditions. However, as a consequence of laboratory experimental limitations, a scaled 500/1000V (DC), 10kW prototype has been developed.

This chapter introduces design details for a small scale experimental prototype that has been constructed to evaluate the design methods of the developed 3DAB converter and its operating characteristics. The chapter discusses details of the structure of the prototype converter including the hardware components, passive components, digital control units and control software implementation. In Section 5.4, the implementation of the control software is presented.

5.2 Design components

The small scale converter arrangement requires a three phase transformer with isolated winding on the ac linking side to provide isolation between the each bridge. The design process of the transformer has been presented in chapter 4. Fig. 5.1 shows a half bridge converter unit used for the prototype converter. Varistors are used to protect the IGBT half bridge circuit from a variety of overvoltage conditions. The H-bridge circuit board is designed for single phase converter experiments in the each bridge.

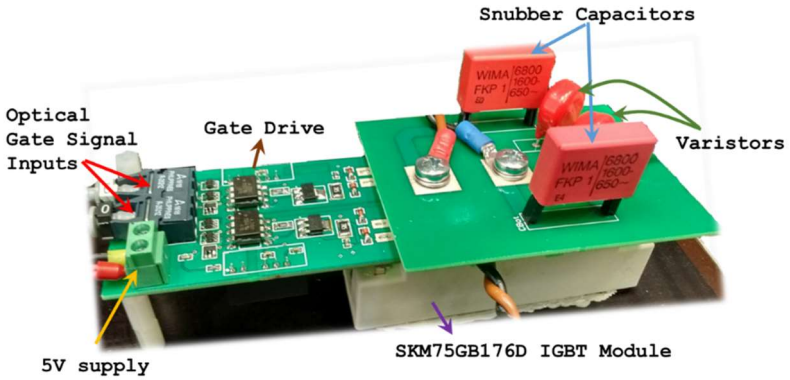
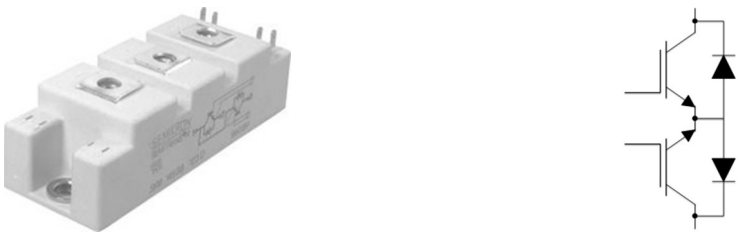


Figure 5. 1 A picture of the half-bridge converter

The H-bridge circuit consists of IGBT module (SKM75GB176D) rated at 1700V, 80A and its associated gate drive circuitry with snubber capacitors. A picture of the IGBT module and the associated diagram of the H-bridge IGBT module are shown in Fig. 5.2



(a) (b)

Figure 5. 2 A IGBT trench module (Model: SKM 75GB176D [117]): (a) picture of SKM75GB176D and (b) schematic of the half bridge IGBT module

5.2.1 Gate drive circuit

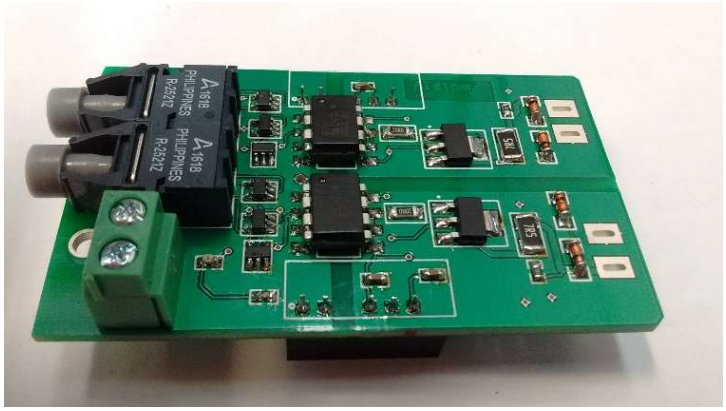


Figure 5. 3 A picture of the bridge gate drive

A picture of the half bridge IGBT gate drive circuit is shown in Figure 5.3 and a schematic of the gate drive circuit is given in Figure 5.4.

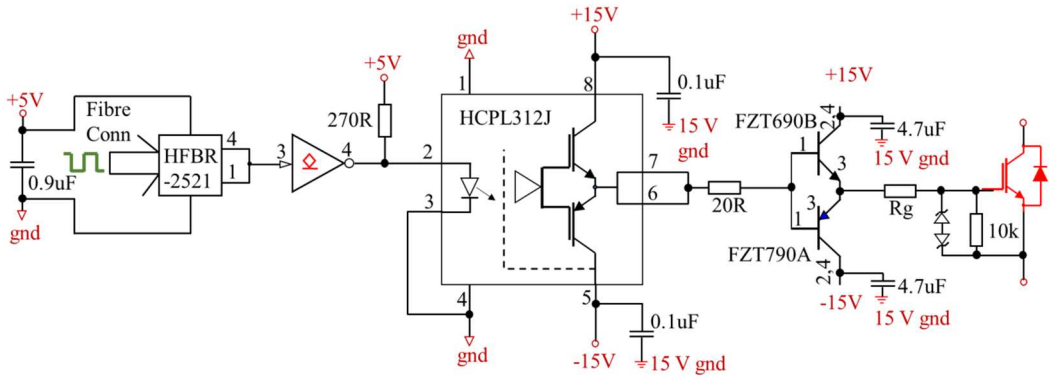


Figure 5. 4 Schematic of the gate drive

The gate drive performs two main functions; drive the IGBT modules using the control signals generated from the FPGA and provide the isolation between the low voltage digital control part and the high voltage power part. The gate drive must be located very close to the IGBT module to minimise leakage inductance between the gate drive and IGBT module. A dual output 2W NMH0515SC DC-DC Converter is used to provide the ±15V IGBT gate drive supply voltage. This converter also provides galvanic isolation between the 5V Low-Voltage Low-Power (LVLP)

control circuit and the ±15V IGBT gate drive power supply voltage. The gate signals from the FPGA are transmitted via an optic interface which has 12 fibre optic transmitters to provide high noise immunity. On the gate drive circuit, the optic signals are received by a 5MBd high performance fibre optic receiver. An HCPL-3150 IGBT Gate Drive Opto-coupler provides isolation between the high operating voltage circuit and the LVLP digital control circuit to meet safety requirements and because the voltage of the IGBT emitters will move relative to the LVLP control common node. The opto-coupler includes Under Voltage Lock Out (UVLO) protection to prevent switching at low gate voltages. The ±15V high operating voltage range of the output stage provides the IGBT drive voltages required by gate controlled devices. On the boost stage of the IGBT operating voltage circuit, a push-pull transistor circuit is used to increase the current to drive the IGBT gate. The selection of the gate resistance affects the turn ON delay and turn OFF time of the IGBT module and the gate resistance must be specified for peak gate drive current and this power level. For the H-bridge Trench IGBT module, a gate resistance (R_g) of 7.5 Ω has been selected. The two zener diodes are used for protecting the IGBT gate circuit against transient overvoltage. A small value capacitor which is connected across the ±15V operating voltage of the drive is to protect the effect of the leakage inductance in the half bridge circuit. it is recommend that a 10k Ω resistor be placed between the gate and emitter in order to ensure IGBT protection even if the gate drive supply voltage is removed and voltage is still being applied to the power circuit.

5.2.2 Snubber capacitors

For SKM 75GB176D trench IGBT Modules, t_{off} can be calculated as

$$t_{\text{off}} = t_{\text{d(off)}} + t_{\text{f}} + t_{d(on)} + t_r \tag{5.1}$$

where, $t_{\text{d(off)}}$ and t_{f} are determined from datasheet [117]. From the datasheet, $t_{\text{d(off)}}$ and t_{f} can be assumed 590 ns and 135 ns respectively. Using Eq. (3.20) and (3.21) in

chapter 4, maximum turn-off currents on primary and secondary side converter are calculated to be approximately 10A. Finally the minimum required values of the $C_{sn,p,s}$ can be assumed as

$$C_{sn,p_\min} \approx \frac{t_{\text{off_p}\min}}{V_{\text{in}}/N} \cdot I_{\text{OFF_p}\max} \approx \frac{725\times10^{-9}\cdot 10.002}{500} = 14.503(nF) \tag{5.2}$$

$$C_{sn,p_\min} \approx \frac{t_{\text{off_s}\min}}{V_{\text{sec}}/N} \cdot I_{\text{OFF_s}\max} \approx \frac{725\times10^{-9}\cdot 10.002}{1000} = 7.25(nF) \tag{5.3}$$

For the experimentation, the designed converter is tested with different snubber capacitance values and without any snubber to verify the range of ZVS during the turn-off commutations. For the commutation evaluation, the experimental results are discussed in chapter 6.

5.2.3 DC link components

From [77], the minimum required DC link capacitance to limit a voltage ripple across the capacitors of the 3DAB Converter at the rated power can be estimated as

$$C_{dc} = \frac{V_{pri}}{6\omega_{sw}^2 L_\sigma \Delta V}\cdot(2-d)\cdot\left[3d\varphi\left(\frac{2}{3}-\frac{\varphi}{2\pi}\right)-\varphi\right]^2 \tag{5.4}$$

The electric charge on the capacitors is caused by the voltage ripple, ΔV across the capacitors of the primary DC link and the secondary DC link. The capacitor has the effect of smoothing the DC voltage. If the capacitance is sufficiently large, the DC link voltage will be almost as smooth as DC. The charging voltage has been evaluated by integrating the DC current ripple plotted in Fig. 5.5. In the 10kW prototype, the capacitances C_{dc} are connected in parallel to the DC resistance load. Within this work, C_{dc}=500 μF is assumed. It can be seen that the dc link capacitance

of the secondary side is 500 μF ensuring to be less than 5 %, so the ripple would be satisfactory for the application.

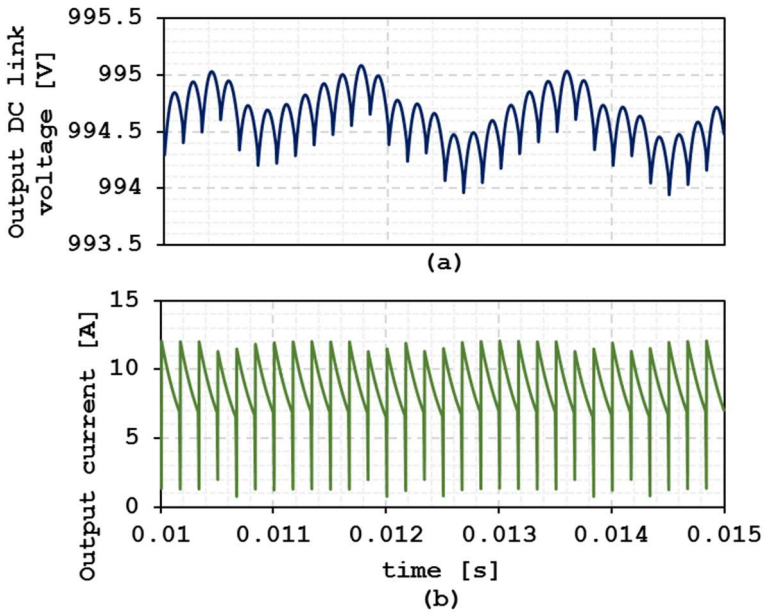


Figure 5. 5 Evaluated waveforms of the 1000V output DC link in the 10kW small scale prototype converter at full load condition: (a) the DC link capacitor voltage and (b) the DC current

5.2.4 Medium-frequency transformer

The design and optimisation process of the 10kW prototype transformer is proposed in chapter 4 in detail. A silicon steel laminated core was chosen as the core material in the transformer. To validate the influence of the non-sinusoidal excitation in the transformer, piecewise linear excitation of winding current in the 3DAB Converter is applied. Using the excitation waveforms, the specific losses for the 3DAB converter excitation are determined. The laminated cores are made from thin gauge steel (0.1mm thickness) and is fully instrumented for monitoring temperature in the windings. The primary and secondary windings are star connected. The transformer prototyped in this design is able to operate at the given frequency with natural convention cooling.

5.3 Data acquisition system

In order to protect the converter circuit from abnormal operating conditions such as over voltage, over current, and short circuit, a data acquisition system has been designed. The data acquisition system provides real time information of the converter. It consists mainly of voltage and current transducers and their associated data sampling circuits.

5.3.1 Voltage measurement circuit

To achieve voltage protection control of the secondary bridge DC link capacitor voltages, voltage transducers (LEM LV 25-P) are used to measure and feedback the capacitor voltages to the digital control system (DPS/FPGA board). The voltage transducers also provide isolation between the high power bridge converter and the digital control platform. Fig 5.6 shows the concept of measurement circuit of the voltage transducer used.

Measurement signals from transducers are transmitted using a current and will therefore be converted to a voltage on the FPGA board using a burden resistor (R_m). In this case a measurement voltage, HV, the primary side resistor (R_p) of the transducer is used to reduce the current through the device to a maximum of 10mA. For this transducer the HV side current through the HV side is set using the R_p. The FPGA side current on the secondary side of the transducer is then produced which is proportional to this measurement side current. The voltage measured across the R_m is then interfaced to the A2D converter via the data sampling circuit.

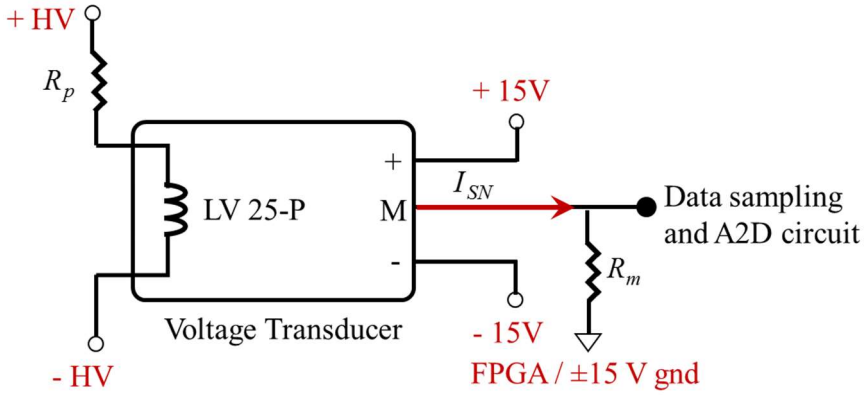


Figure 5. 6 Concept of measurement circuit for the LEM LV 25-P voltage transducer

5.3.2 Current measurement circuit

The current measurement circuit has three current transducers which provide knowledge of the connected secondary windings of the ac-linked transformer and one current transducer used to measure the input DC source current for converter synchronisation and protection control respectively. The current transducers (LEM LA 55-P) have a nominal RMS current rating of 50A and a conversion ratio of 100:1. The current transducers require ±15V DC power supply and a burden resistor (R_m) to converter the measured secondary side current to a voltage on the FPGA board. Fig. 5.7 shows the concept of measurement circuit for the LA 55-P current transducer. The maximum voltage range that can be measured across the burden resistor is ± 5V. A measured voltage higher than this will saturate the A2D circuit input and may result in damage to the circuit.

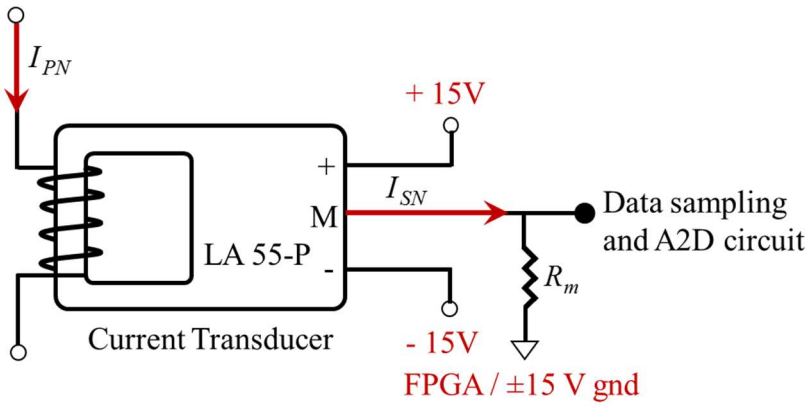


Figure 5. 7 Concept of measurement circuit for the LA 55-P current transducer

5.4 Digital control unit

In order to control the power flow between the primary bridge and the secondary bridge converters, a phase shift modulation scheme is required in the experimental system. This has been achieved using a high performance 32 bit floating point digital signal processor (DSP) TMS3206713 from Texas Instrument (TI) [118] and a field programmable gate array (FPGA) card.

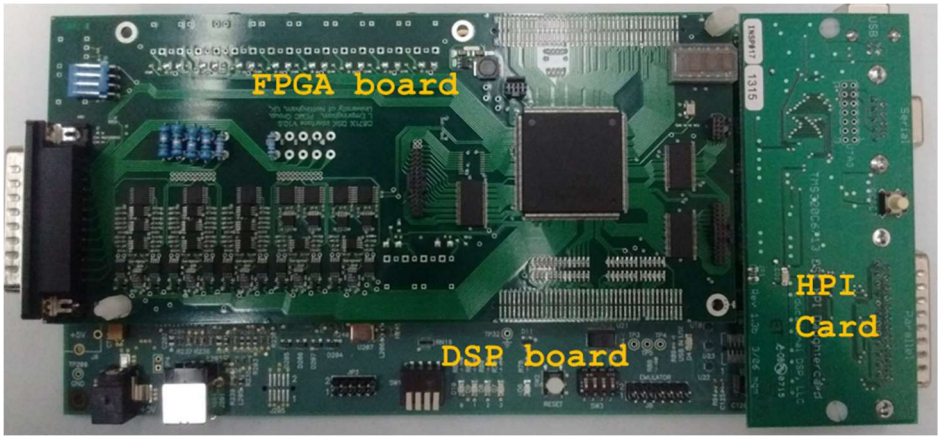


Figure 5. 8 A picture of the digital control unit (DSP. FPGA, and HPI card)

Fig. 5.8 shows a picture of the used digital control unit; a FPGA board, a 6713 DSK DSP board, and a HPI card. A value of phase shift modulation is calculated in the DSP and then this modulation is implemented onto the Actel ProAsic 3 FPGA [119]. The FPGA card, designed by Power Electronics, Machines, and Control (PEMC) Group at the University of Nottingham, provides 10 Analogue to Digital (A/D) conversion channels for converter data acquisition on the FPGA card. All measurements from the transducers are converted to digital values using the 14 bit A2D channels and transferred to the DSP via the FPGA.

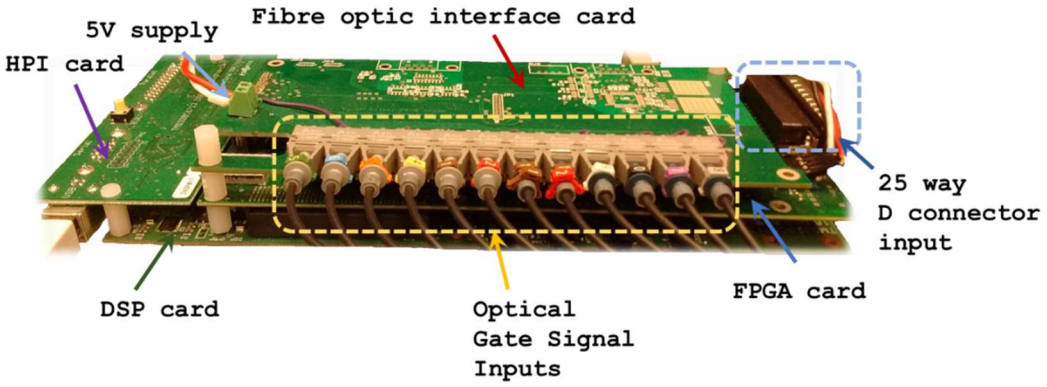


Figure 5. 9 A picture of the digital control unit connected with fibre optic interface card for generating 12 gate signals

The FPGA card is interfaced to the 3DAB converter through an extended fibre optic interface card as shown in Fig 5.9. Using the fibre optic card, transmission of logic signals to the associated gate drives of the IGBT modules are achieved. A host port interface (HPI) card is used to access the DSP memory. Besides, the HPI card allows bidirectional data transfer between the host PC and the DSP and to change variables during the converter is running.

A function diagram for the overall control scheme implemented using the DSP/FPGA to operate the 3DAB converter comprises several sub-systems as shown in Fig. 5.10. The input & output dc link voltages and also the input & output dc currents are sampled at the fundamental operating frequency of 1000 Hz of the transformer using A/D converters on the FPGA card. The sampled data is then read and latched into a register.

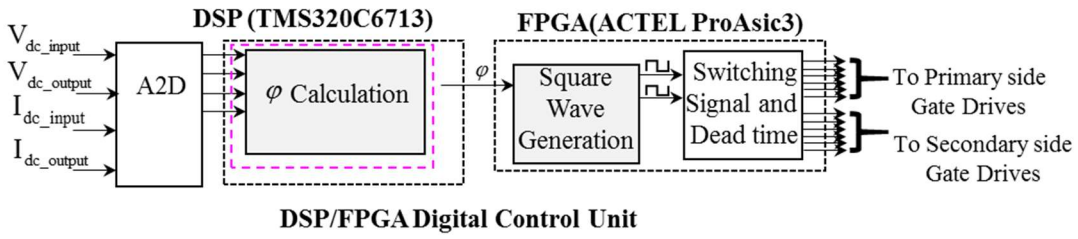


Figure 5. 10 Diagram of the DSP/FPGA digital control unit

The phase shift controller in the DSP calculates a value of phase shift which will be implemented in the next control cycle. The control part of the FPGA involves the generation of two square-waves at 1000 Hz, phase shifted by the calculated value. In addition, this sub-system of the FPGA also produces the switching signals for the gate drives and also implements the dead-time of the gate signal. The control values are loaded from the DSP to the FPGA via the External Memory Interface (EMIF) during the converter system initialisation.

Phase shift modulation for the converter is implemented in an FPGA based PWM modules. The interrupt block on the FPGA generates interrupt signals for the DSP. This interrupt signal triggers the execution of the interrupt service routine (ISR) in the DSP and the modulation sequence in the FPGA. A switching vector for the primary bridge and the secondary bridge is computed during the ISR. The PWM vector for each bridge is held on a 32 bit First-in First-Out (FIFO) memory register. The first sixteen bits are used to hold the timer count and the next three bits are used to hold the logic states of the three switches in each bridge. Fig. 5.11 shows the memory register of the 'master' PWM vectors used for the primary bridge switches. The structure of a memory register used for the 'slave' PWM vectors corresponding to the secondary bridge switches is described in Fig. 5.12. To turn the upper IGBT device a state logic of 1 is written to the corresponding switch memory map (S_i i=1,2,3) and 0 to turn off the upper device (turn on the lower).

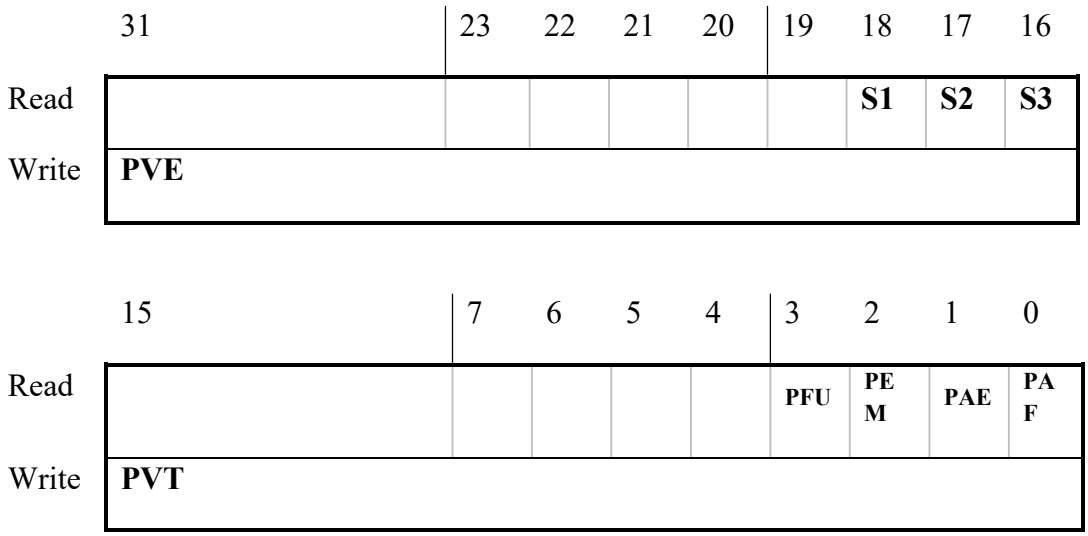


Figure 5. 11 FPGA memory register used for the primary bridge PWM vectors

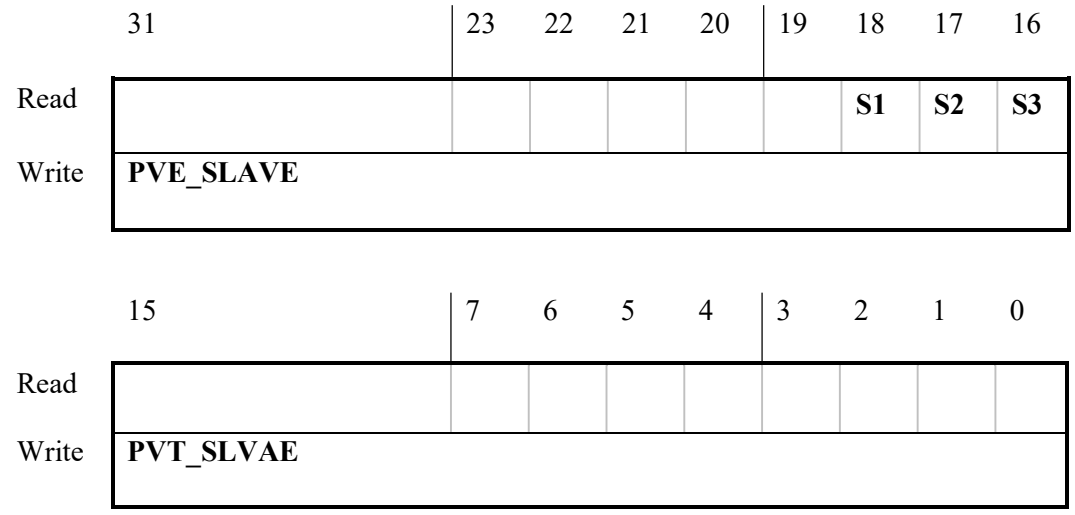


Figure 5. 12 FPGA memory register used for the secondary bridge PWM vectors

Legend information for the FPGA memory register distributions is illustrated as below.

PVE	PWM_VECTOR	
PVT	PWM_VECTOR_TIME	
PAF	PWM_FIFO_Almost Full	No. of words in FIFO > 250, Active High
PAE	PWM_FIFO_Almost Empty	No. of words in FIFO < 2, Active High
PEM	PWM_FIFO_EMPTY	Active High
PFU	PWM_FIFO_FULL	Active High

The implementation of the provided modulation method is proven in the following. The appropriate transition control angle φ for the switching event is determined as illustrated in Fig. 5.13. Table 5.1 lists the switching states $S1, S2, S3 \in \{0,1\}$ of the corresponding the three half-bridges in relation to the switching state S of the three phase bridge. A value of 1 indicates that the upper switch of the corresponding half bridge is ON and the lower switch is OFF, whereas 0 means that the upper switch is OFF and the lower switch is ON. Accordingly, the provided modulation principle is the so-called six step mode, where the fundamental switching period $T_{sw} = 1/f_{sw}$ is divided by the six time intervals (60°). In the steady state, the

square waves of the phases of the individual bridges are phase shifted with respect to each other by 120° as shown in Fig. 5.13.

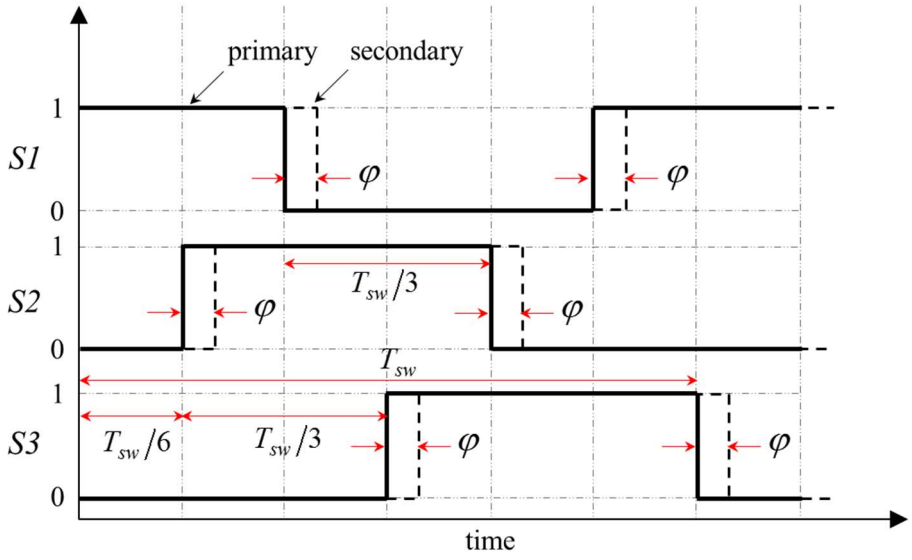


Figure 5. 13 Switching pattern and control angle according to the phase shift modulation method

Table 5. 1 Switching states of a three phase half bridge

s	1	2	3	4	5	6
S1	1	1	0	0	0	1
S2	0	1	1	1	0	0
S3	0	0	0	1	1	1

The modulation generator is required to produce two square-waves, one for each bridge in the 3DAB converter. One of these (Primary bridge signal) is produced with the fixed time intervals, whereas the other has a phase shift which is controlled using the DSP. Fig. 5.14 shows the concept of this square-wave generation method for the dual active bridge (DAB) control.

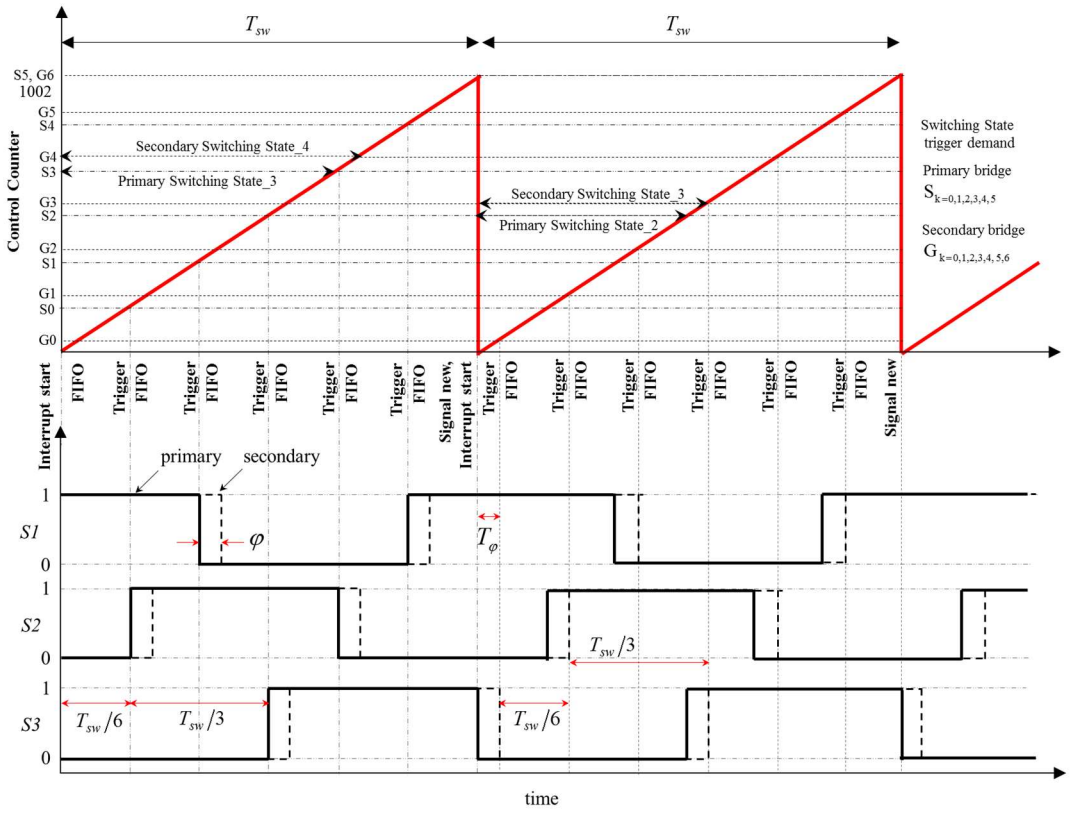


Figure 5. 14 Method of DAB Phase Shifted Square-Wave generation using an FPGA

A counter is used to generate a sawtooth wave at the fundamental switching frequency. This frequency refers to the fundamental operating frequency of the transformer and is set during initialization. A2D samples are latched into the phase shift controller at the ISR start point. When the interrupt signal is received, the ISR is triggered. The phase shift controller then computes the corresponded control angle for the next period of modulation. A switching demand for primary bridge is set in a register $S_{k=0,1,2,3,4,\ 5}$ with a value which is six time intervals of the peak counter value as shown in Fig. 5.14. This counter value is used to set the switching frequency of the converter. The counter value is then compared with the demand value using a digital comparator. When the two signals are equal, an FIFO is toggled. Another slave comparator is used to create the secondary bridge square-wave using a switching demand which is set in a register $G_{k=0,1,2,3,4,5,6}$. The first value of $G_{k=0}$ is derived from the phase shift controller in the DSP. Other switching demands used as the comparator trigger points are created from six time intervals of the peak counter value as same the primary bridge method.

The final step in the square-wave generation process is to create pulses for all IGBT devices in each bridge whilst adding dead time to them to avoid short circuit in the half bridge during the commutations. A rising edge delay mechanism is implemented in the FPGA logic to achieve the dead time. In this experiment, the value of a register of dead time was set to 2.5*u*s which is more than the sum of the turn on, turn off, rising, and falling time of the IGBT device.

5.5 Closed-loop control strategy

In multi-terminal applications, the output voltage V_{output} of the 3DAB converter must be controlled to regulate the output voltage. The block diagram of the suggested closed control system is depicted in Fig. 5.15. The control system consists of a cascaded DC voltage regulator and a feed-forward block. The cascaded constant-voltage control is achieved by a PI controller [155]. The input of the controller is the voltage error between the reference value of the output voltage and the measured value of the output voltage. The output of the controller is the control phase-shift angle, which is the only actively variable parameter. The feed-forward block contains the phase-shift angle equation (3.25). The nominal value of φ can be resolved by the equation (3.24) for dead time compensation. The feed-forward serves to compensate steady-state errors occurring due to parameter variations in the cascade control structure.

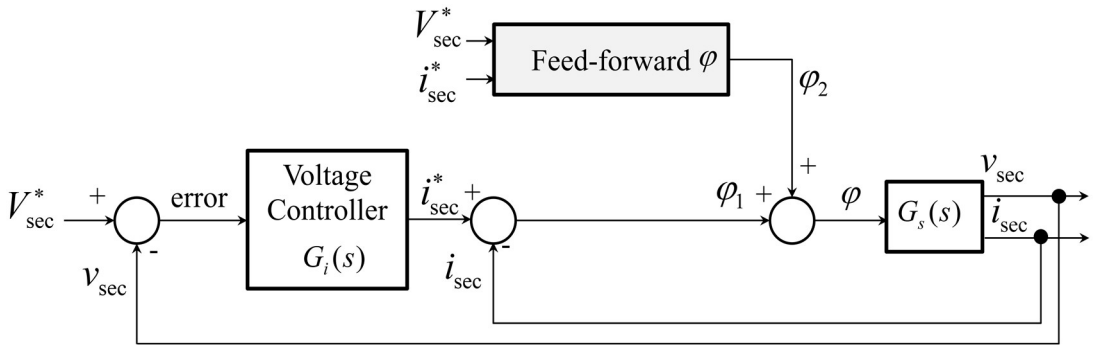


Figure 5. 15 Schematic of the output voltage controller

5.5.1 Output voltage control

The output voltage of the 3DAB converter needs to be controlled by regulation of the phase-shift angle φ. The schematic of the output voltage controller is shown in Fig. 5.16. The value of φ is calculated with equation (3.25) by measuring the output voltage and the load current I_{sec}. The adjustment of the value of φ was implemented by a PI controller, taking as input the output voltage and the error between the output voltage reference V_{ref} and the measured voltage v_{sec}.

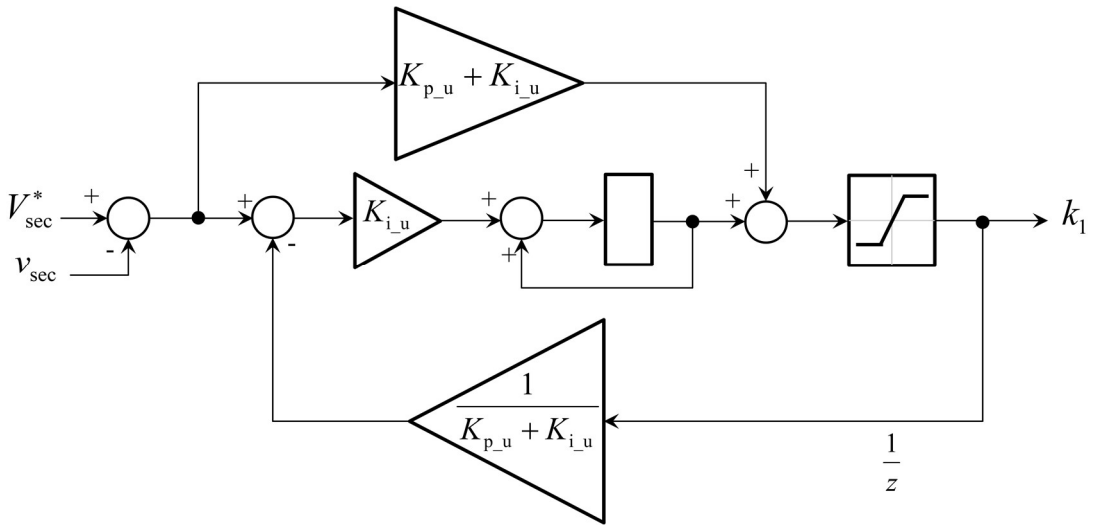


Figure 5. 16 Proposed PI controller for the voltage control

The block contains the small time constant of the system and represents the reference value of the load current i^*_{sec} with a certain proportional factor when the value of φ is changed. Each φ will generate a reference current i^*_{sec} , with a certain integral controller compensating factor K_i and a time delay constant T_{delay}. The closed control loop $G_i(s)$ is modelled by a delay of T_{sampling}. The function block in the control structure is represented as:

$$G_i(s) = \frac{K_i}{1 + sT_{\text{i}}} \tag{5.5}$$

The time delay constant (T_{delay}) consists of all system delays like sampling time of the processor T_{sampling} and delay time caused by the modulator $T_{\text{modulator}}$. The T_{i} can be expressed as:

$$T_{\text{delay}} = \frac{T_{\text{sampling}}}{2} + T_{\text{modulator}} = \frac{T_{\text{sampling}}}{2} + \frac{1}{5 \cdot f_{sw}} \tag{5.6}$$

The integral controller compensating factor K_i can be given by:

$$K_i = \frac{T_{\text{sampling}}}{2T_{\text{delay}}} \tag{5.7}$$

In theory, the current controller is not necessary, as the control phase-shift angle can be directly set by the feed-forward, but steady-state errors would occur owing to parameter variations. The secondary bridge voltage V_{sec} is generated through an integration of the output current flowing into the output capacitor $C_{\text{sec}} = C_{\text{s1}}+C_{\text{s2}}$. Therefore, for designing the control parameters, the transfer function $G_s(s)$ of the system is expressed as:

$$G_s(s) = \frac{1}{s \cdot C_{\text{sec}}} \tag{5.8}$$

5.5.2 Design of the controller parameters

A PI controller is used as the voltage controller. The PI controller can be achieved using two controller gains, $K_{\text{i_u}}$ and $K_{\text{p_u}}$. The voltage controller was designed using two different time constants of the controller represented by $T_{\text{delay_u}}$ and $T_{\text{i_u}}$. The sampling time T_{sampling} was set to 5 times the switching period of a conventional approach [82]. The time $T_{\text{i_u}}$ was affected by the value of the output capacitance. The two time constants of the controller can be expressed by:

$$T_{\text{delay_u}} = 4 \cdot T_{\text{delay}} \tag{5.9}$$

$$T_{\text{i_u}} = \frac{8 \cdot K_i \cdot T_{\text{delay}}^2}{C_{\text{sec}}} \tag{5.10}$$

Finally, the two gain values of the voltage controller $G_u(s)$ resulting from the symmetrical optimal method are as follows:

$$K_{\mathrm{i_u}} = \frac{T_{\mathrm{sampling}}}{T_{\mathrm{i_u}}} \tag{5.11}$$

$$K_{\mathrm{p_u}} = \frac{T_{\mathrm{delay_u}} - \dfrac{T_{\mathrm{sampling}}}{2}}{T_{\mathrm{i_u}}} \tag{5.12}$$

The voltage control system was designed using only one PI controller element with the values given in equation (5.11) and (5.12) as shown in Fig. 5.16.

The controller has a discrete time element z^{-1} with the sampling time. The controller generates a modulation degree k_1. The value of this modulation degree is limited within the boundaries [-1, 1]. Owing to a high voltage overshoot possibility when the converter is started, the integration gain $K_{\mathrm{i_u}}$ can be improved as:

$$K_{\mathrm{i_u}} = \begin{cases} K_{\mathrm{i_u}} \\ \dfrac{K_{\mathrm{i_u}}}{2} \ \text{if} \ \left|\mathrm{error}(v_{\mathrm{sec}})\right| > 0.02 \cdot V_{\mathrm{sec}}^{*} \\ \dfrac{K_{\mathrm{i_u}}}{10} \ \text{if} \ \left|\mathrm{error}(v_{\mathrm{sec}})\right| > 0.04 \cdot V_{\mathrm{sec}}^{*} \end{cases} \tag{5.13}$$

5.5.3 Closed-loop simulation results

The closed-loop control system design presented in this thesis was verified by simulation investigation for the 10-kW 3DAB converter. The control design was implemented in PLECS circuit simulation to evaluate the performance of the control. To validate the functionality, the input DC link voltage was set to 500 V. Using the presented control strategy, a PI controller for the output voltage, V_{sec} was implemented. The response of the converter to step in the reference voltage at full load is shown in Fig. 5.17 and 5.19. The reference voltage rapidly increased from 0 V to 1000 V (100% of the nominal voltage). Fig. 5.17 shows the simulated transient voltage response achieved by this control system for the output voltage. In this case,

the actual value of the output voltage increased without overshoot by the closed-loop controller in order to reach the reference value. Fig 5.18 shows the simulation result of the average output power controlled by the closed-loop control system for a step change in voltage reference. The presented control system allows to set a maximum output current. The output power can respond rapidly to the reference power in only a few switching cycles. However, the oscillation is produced by the abrupt change in the control phase-shift angle φ. For good tranisent response, a more sophisticated control design is needed to solve this problem.

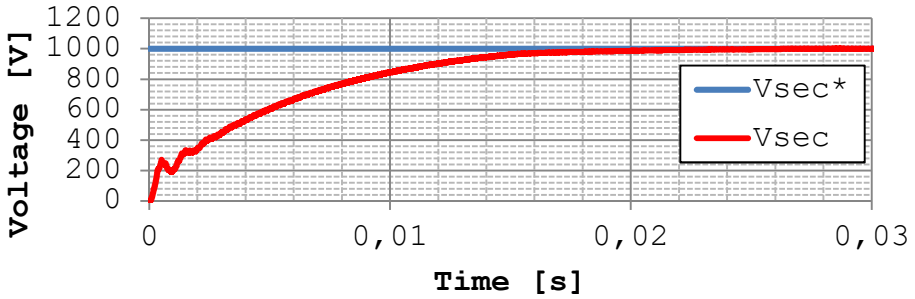


Figure 5. 17 Simulated the output voltage of the 3DAB converter with the demand value of V_{sec}.

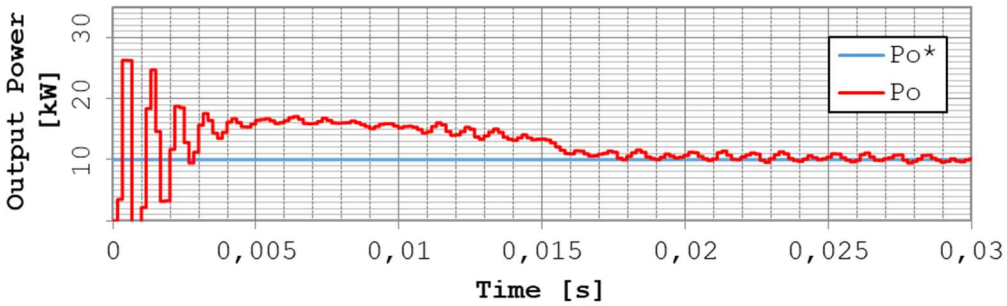


Figure 5. 18 Simulated the output power of the 3DAB converter with the demand value of V_{sec}.

The dynamic performance of the converter was validated by applying step changes to the commanded secondary side voltage, as shown in Fig. 5.19. Fig. 5.19 (a) shows the output voltage response to a reference voltage change of 500 V–1000 V. The reference voltage rapidly decreased with 50% of the nominal value in Fig. 5.19(b). In both cases, the converter is operated neither in unstable nor oscillatory manner. The actual output voltage increased and/or decreased, without an under-damp or overshoot by the closed-loop controller. For the step-up change condition

(500 V to 1000 V), the transient response was achieved rapidly in the voltage reference. However, Fig. 5.19(b) shows the step-down voltage response is slightly slower than for the step-up change.

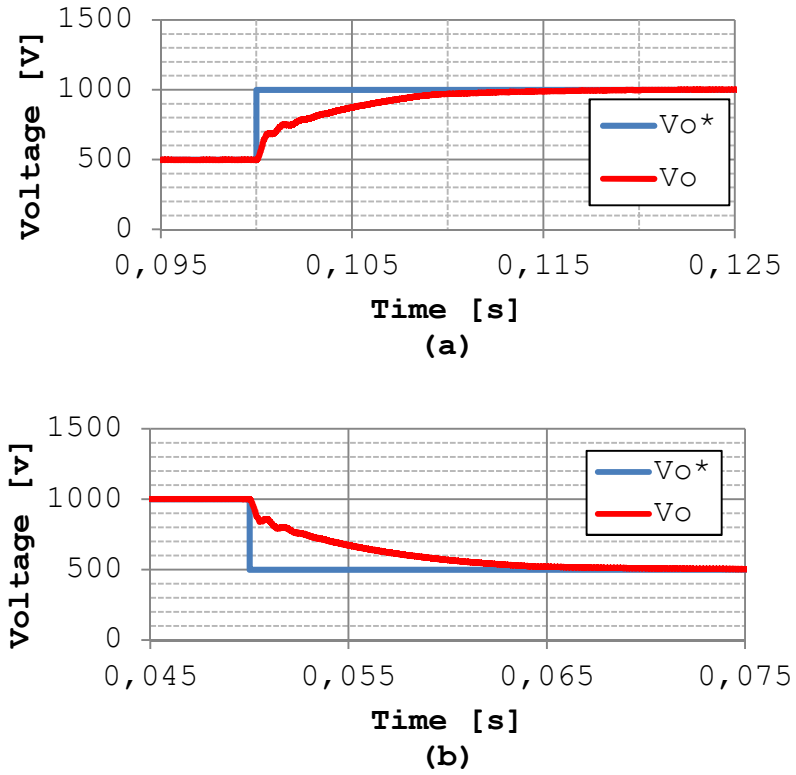


Figure 5. 19 Simulated waveforms illustrating the operation of the 3DAB converter with changes of the demand value of V_{sec}: (a) 1000V to 500V and (b) 500V to 1000V.

5.6 Summary

A small-scale laboratory prototype of the 3DAB converter was discussed to validate its operation. Hardware design considerations for the selection of components for the converter have also been presented. In order to control the power flow, a digital control unit was presented. The sequence of phase-shift control algorithm implementation in the DSP and the phase-shifted square-wave generation in the FPGA have also been discussed. A simple voltage controller with a fee-forward has been presented. The controller controls the output voltage of the 3DAB converter to regulate the phase-shift angle φ.

Chapter 6

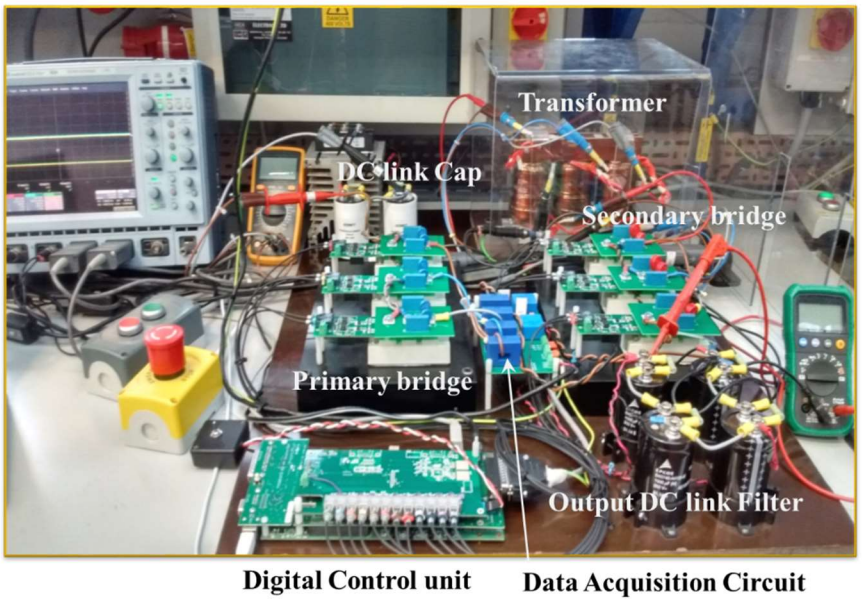
Experimental Results

This chapter presents the experimental results from the 10 kVA small-scale 3DAB converter developed in Chapter 5.

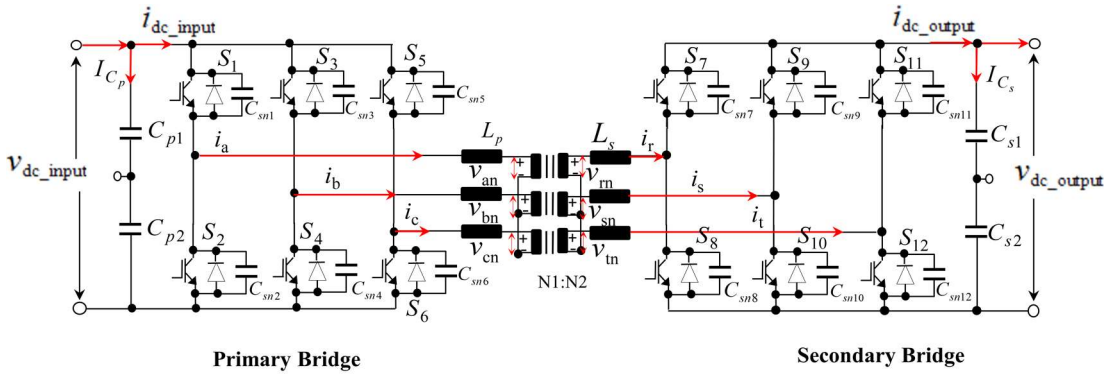
For practical implementation, the 3DAB converter uses 'SKM75GB176D' Trench IGBT modules from SEMIKRON and operates at a switching frequency of 1000 Hz. The input DC-link voltage was set to 500 V. The leakage inductance of the transformer was found to be approximately $L_\sigma = 92uH$. The turns ratio of the transformer was 1:2; hence, the output DC-link voltage was set to 1000 V. In the following experiments, the converter is operating in the boosting mode into an R load with phase-shift modulation control and the results have been obtained at various load conditions.

A simulation of the small-scale converter described in Chapter 5 is undertaken using PLECS software. A two-level IGBT half-bridge modelled with ideal switches and anti-parallel diodes was implemented as a single leg for both bridge converters. Passive components and an ideal three-phase transformer were used in the simulation model. On the other hand, experimentally parasitic components were expected to be present in the developed power electronics circuit. For the bipolar power semiconductors, the parasitic inductance not only induces overvoltage but also

causes oscillation; hence, it generates much higher losses. The experimental results are measured using a LeCroy WaveSurfer 424 200 MHz oscilloscope and current and differential voltage probes. The efficiency results are measured using two precision PPA 2530 Power Analyzers. The two bridges in the 3DAB converter were controlled in open-loop modulation to obtain these results, with a control phase-shift angle for each load condition calculated manually by the controlling DSP for the desired power. The developed converter of the experimental system is shown in the structure of the experimental rig in Fig. 6.1.



(a)



(b)

Figure 6. 1 Experimental setup rig showing the main developed converter: (a) the experimental rig and (b) the schematic of the developed converter

6.1 Converter operation with load conditions

Experimental results for the 3DAB converter converting into a resistive load are presented to validate the steady-state operation of the converter under various load conditions. Two 500-V voltage-source DC supplies are connected in parallel to the input DC bus of the 3DAB converter via 1000-μF capacitors, which serve as the DC link capacitor. At the receiving bridge (i.e. secondary bridge), the 1000-V output DC bus is connected to paralleled or series load resistors to allow energy to be absorbed. The AC coupling phases were arranged as a 'Y', connected with the three-phase transformer between primary and secondary IGBT-based bridges.

The expected results for the AC link voltages and currents from the simulation model are presented in Fig. 6.2 and 6.3, respectively. The simulation results of the DC voltages and currents of the input and output terminals are shown in Fig. 6.8.

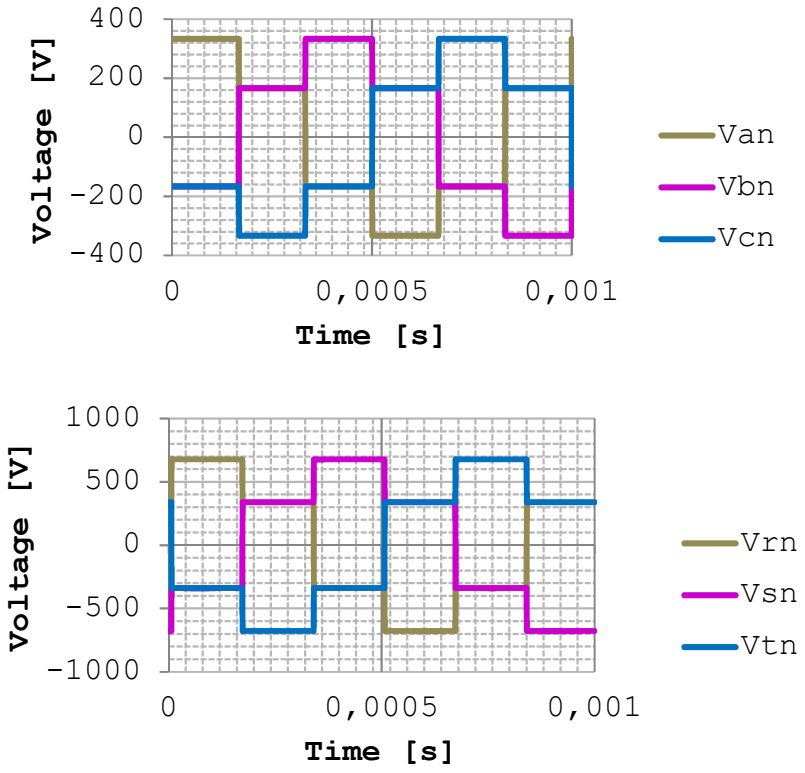


Figure 6. 2 Simulation results of the 3DAB converter at 9.5kW during boost mode: Voltages generated by the primary and secondary bridges

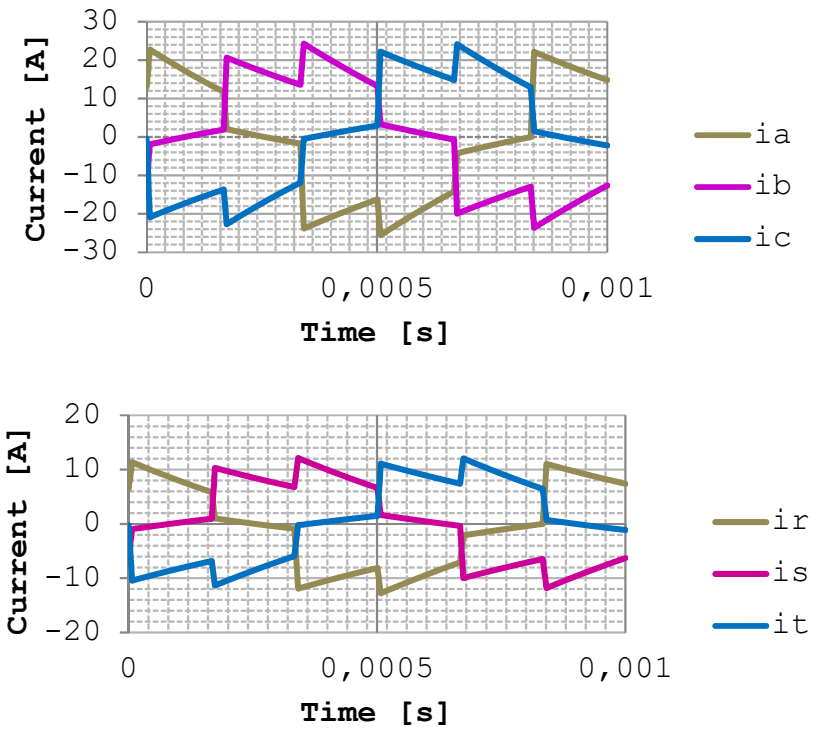


Figure 6. 3 Simulation results of the 3DAB converter at 9.5kW during boost mode: Currents through the primary and secondary windings of the transformer

These results show six-step square waves at the primary and secondary windings of the transformer acting as AC magnetic coupling. It is worth noting that the high frequency-damped oscillation caused by the transistor turning 'on' in the experimental results is negligible in simulation results owing to the use of ideal components. For the first validation, the simulation and experimental results were captured in the steady-state operation.

Fig. 6.4 to Fig. 6.7 and Fig. 6.9 show the results for full-rated power operation of the converter. Fig. 6.4 and 6.5 show the primary and secondary bridge-switched voltages, respectively. These plots confirm this validation with matching simulation and experimental results for the steady-state condition. In this experiment, the control phase-shift is optimised to $\varphi = 2.8°$ owing to the low value of the leakage inductance. As can be seen, high-frequency oscillations occur during the turn-on and off transients when the drain voltage changes.

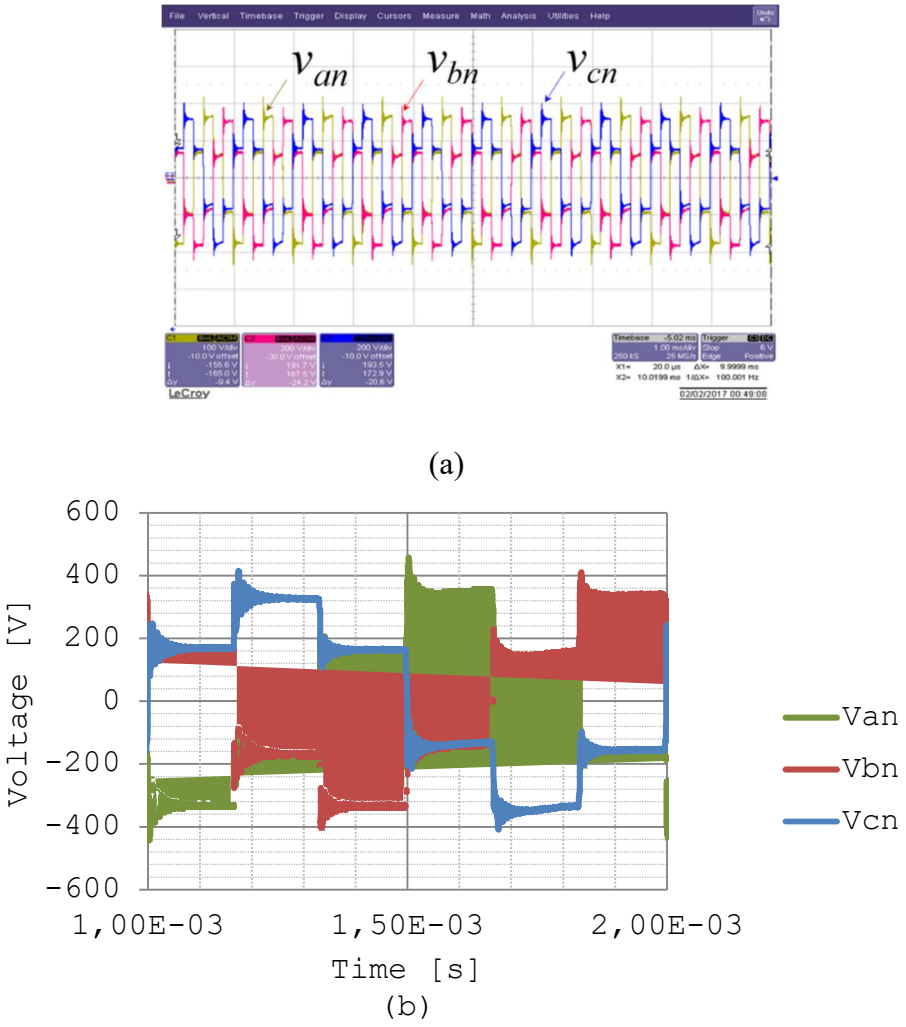
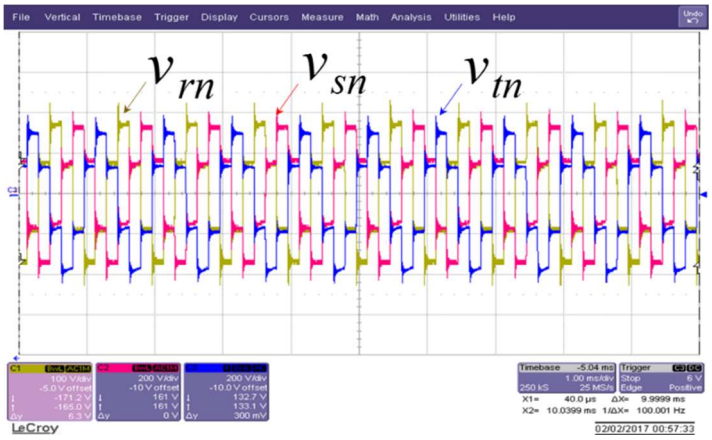


Figure 6. 4 Experimental results of the 3DAB converter at 9.5kW during boost mode; (a) voltages generated by the primary bridges (v_{an}: 100V/div, v_{bn}, and v_{sn}: 200V/div). Timescale: 1000μs/div and (b) voltages generated for 1 switching period.

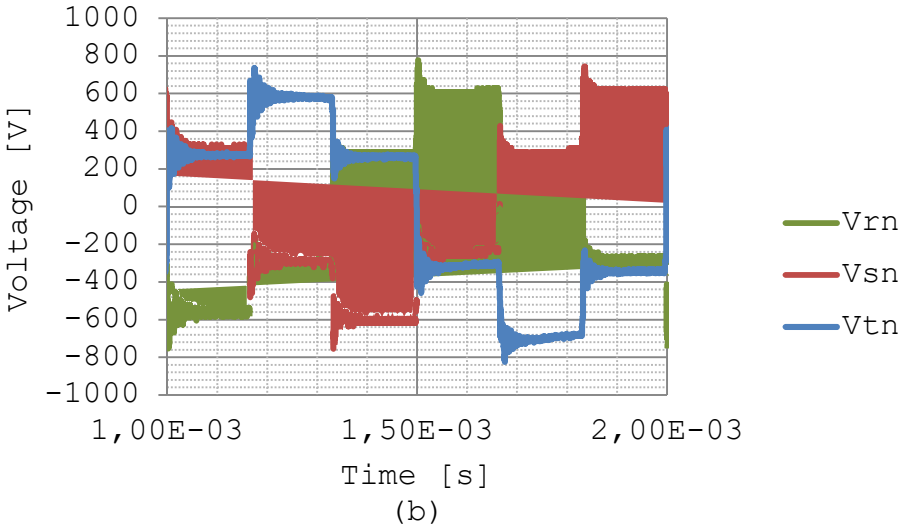
The parasitic oscillation frequency is typically in the range of 50 MHz to 250 MHz and parasitic inductance is present in the IGBT modules. The oscillations can lead to over voltage transients and high switching losses. Thus, the overvoltage at diodes and IGBTs increase the stress by peak power, which limits the switching speed. Increasing the gate resistance is often effective in preventing the oscillation owing to reduced dv/dt. However, higher gate resistance also slows down the switching time which results in high switching losses.

It is natural to consider about improving the gate driver to damp this turn-on oscillation. Many studies have considered using active gate driver to solve the issues related to di/dt and dv/dt and the current and voltage overshoots that may affect the

safe operation of IGBT module [182]-[197]. Applying the active gate driver solutions, the current overshoot during the turn-on interval can be reduced. In [191], a method of optimizing the gate resistance of the low side switch is proposed to improve the damping of turn-on oscillation. In [192]-[194], possible additional damping circuits are suggested for improving the oscillation.



(a)



(b)

Figure 6. 5 Experimental results of the 3DAB converter at 9.5kW during boost mode: (a) voltages generated by the Secondary bridges (v_{rn}: 100V/div, v_{sn} and v_{tn}: 200V/div). Timescale: 1000μs/div and (b) voltages generated for 1 switching period.

The switched-phase currents of the primary and secondary windings of the transformer are plotted in Fig. 6.6 and 6.7, respectively. In the case of the small control phase-shift angle, the switched harmonics of the transformer currents are generated clearly by the six-step time intervals. For the boost mode, the turns ratio of

the transformer is set to 1:2, so the secondary side currents should be less than the primary side by 50%. For the full load condition, the measured RMS currents of the primary winding and secondary winding are 14.03 A and 7.37 A with the optimised phase-shift modulation scheme, respectively. In the simulation, the switched currents of the transformer windings show RMS values of 14.57 A and 7.28 A, respectively. In both simulation and experimental results, the phase currents are well matched.

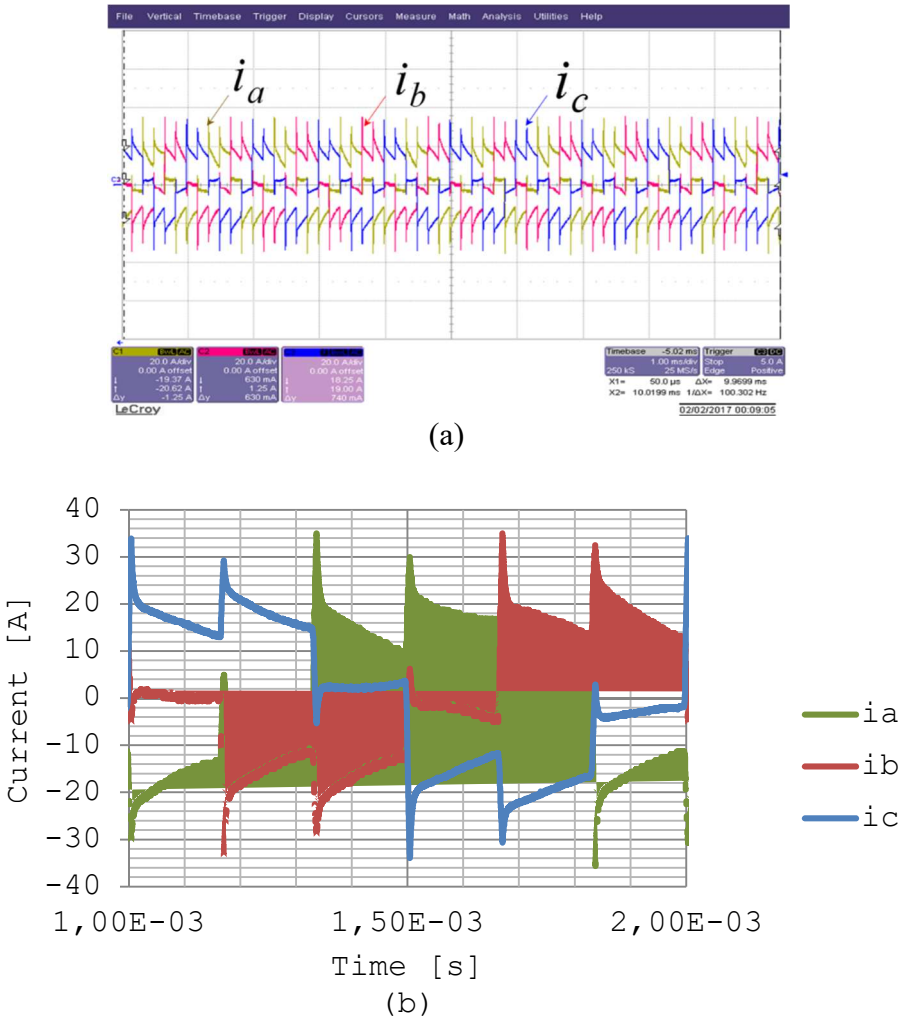


Figure 6. 6 Experimental results of the 3DAB converter at 9.5kW during boost mode: (a) currents through the primary windings of the transformer (i_a, i_b, and i_c: 20A/div). Timescale: 1000μs/div and (b) currents generated for 1 switching period.

The corresponding DC voltage and current waveforms for 9.5-kW power transfer from the experimental rig are presented in Fig. 6.9. The input DC voltage is set to 500 V. This plot corresponds to the condition where the output DC link voltage is

constant at 998 V with an average output current demand of 9.0 A. It can be observed that the output DC link capacitor current is positive and power transfer is taking place from the parallel connected 500V DC supplies to the load resistor. This shows that the capacitor is charging and the bridge on the LV side performs inverter operation, whereas the bridge on the HV side performs rectification.

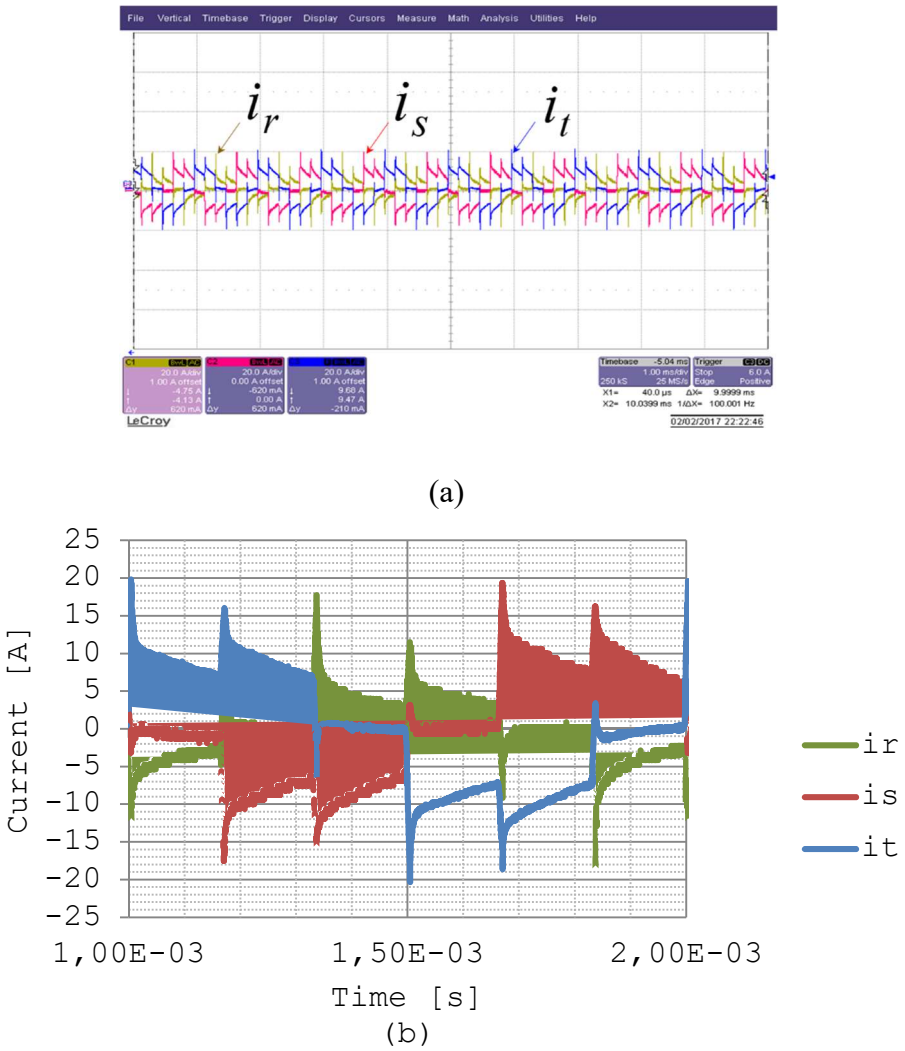


Figure 6. 7 Experimental results of the 3DAB converter at 9.5kW during boost mode: (a) currents through the secondary windings of the transformer (i_r, i_s, and i_t: 20A/div). Timescale: 1000μs/div and (b) currents generated for 1 switching period.

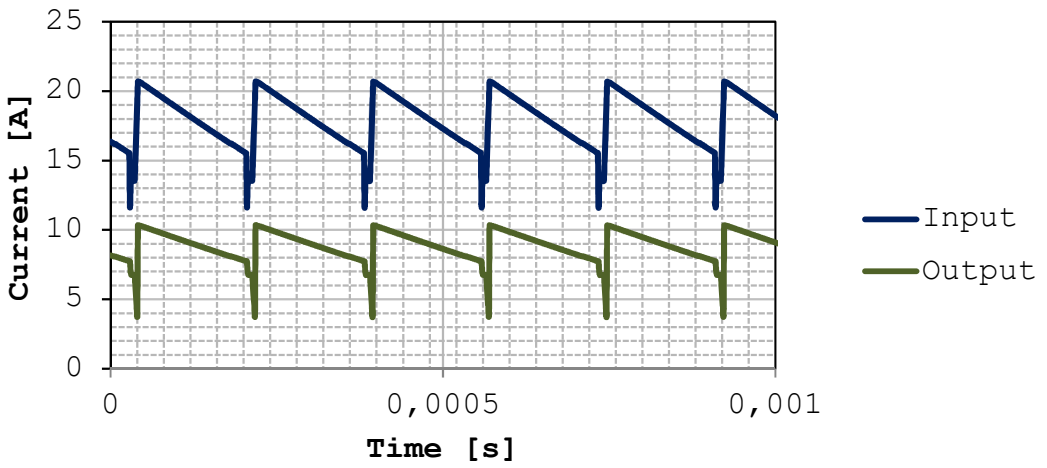


Figure 6. 8 Simulation results of the 3DAB converter at 9.5kW d`uring boost mode. DC input current and output current

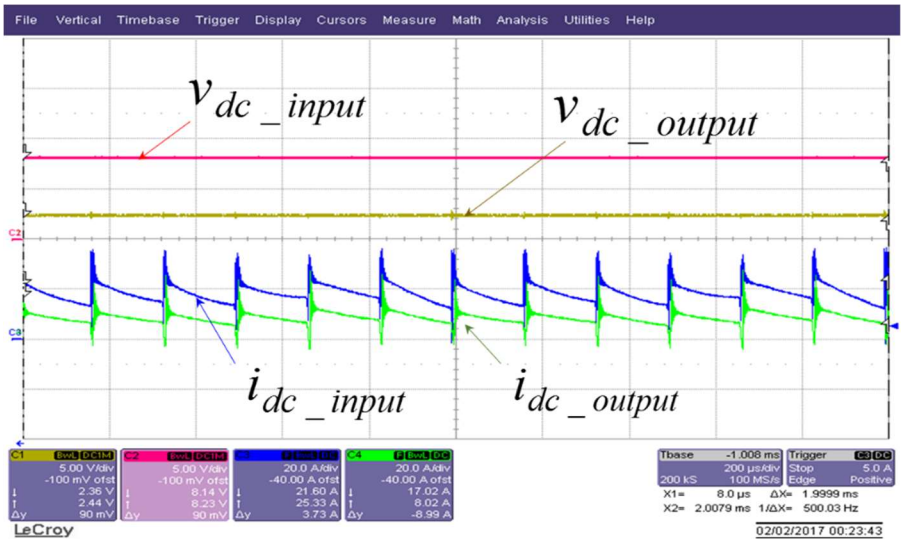


Figure 6. 9 Experimental results of the 3DAB converter at 9.5kW during boost mode. DC input voltage (V_{input} : 5V/div), DC output voltage (V_{output} : 5V/div), input current (I_{input}: 20A/div), and output current (I_{output}: 20A/div). Timescale: 200μs/div.

Experimental steady-state waveforms for the 3DAB converter with the optimised modulation scheme when various phase-shift angles (load conditions) are shown in Fig. 6.11 to 6.14. In order to validate the effectiveness of the phase-shift modulation, the experimental measurement system is shown in Fig. 6.10. Each graph illustrates the voltages and winding currents in phase ‘a’ and ‘r’ of the transformer. The DSP is used to control the output power of the converter while the phase-shift modulation is implemented. For the modulation scheme, a slow variation in input and output

voltages is assumed; hence, the amount of transferred power is defined by the transformer current. Therefore, the DSP calculates the phase-shift angle for the modulation scheme in order to achieve the demand of power transfer. In this experiment, a small phase-shift can be seen between the primary and secondary winding terminals and it is equal to the control phase-shift angle.

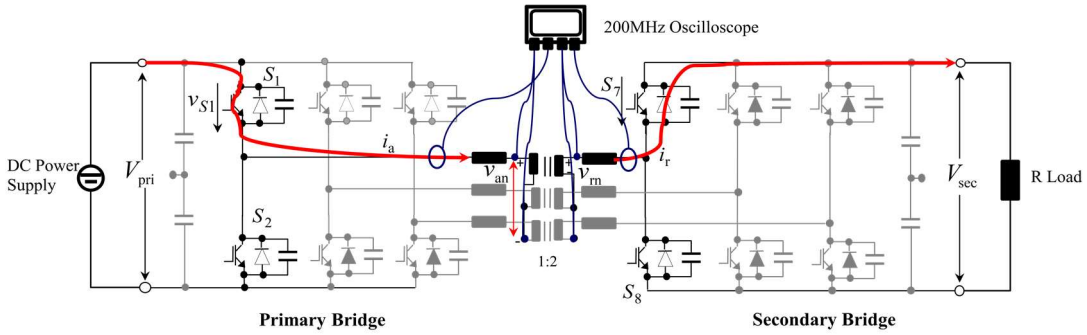


Figure 6. 10 Schematic of test circuit used for validating waveforms of the 3 DAB converter

The measured waveforms for $V_{dc\,1} = 500\ V$, $V_{dc\,2} = 998\ V$, and output power of 9.5 kW are presented in Fig. 6.11. For this operating point, a phase-shift angle of 2° was calculated; however, owing to output voltage drop and converter losses, an optimised angle of 2.8° was required. In this situation, the measured RMS phase currents of the primary and secondary windings are 14.57 A and 7.28 A, respectively. Fig. 6.12 shows the measured waveforms for an output power of 6.5 kW with $V_{dc1} = 500V$, $V_{dc2} = 999V$ with an optimised angle of 2.2°. It can be observed that the measured RMS primary and secondary winding currents are 9.76 A and 5.17 A, respectively, under these conditions. As shown in Fig. 6.13 for $V_{dc2} = 998.5V$, the measured RMS primary winding currents are 5.02 A and secondary winding currents are 2.77 A with the optimised phase-shift modulation. For these conditions, an optimal angle of 1.3° is applied. Fig. 6.14 illustrates the voltages and currents of the transformer with 1.3-kW transmission power, where the output voltage is maintained at 1001 V. Accordingly, the corresponding phase-shift angle is optimised to 0.4°. The RMS currents were 1.95 A and 1.25 A for primary and secondary windings, respectively, during the low power level.

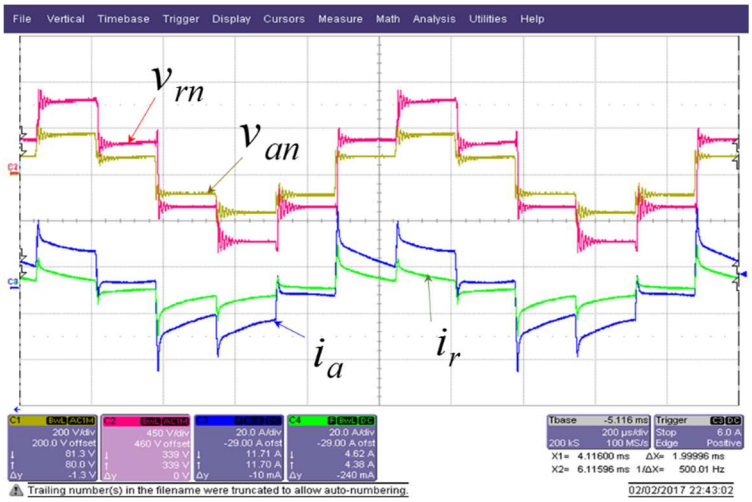


Figure 6. 11 Experimental results of the 3DAB converter at 9.5kW with control phase shift angle φ= 2.8°. Voltages generated by the primary bridges v_{an} (v_{an}: 200V/div), voltage generated by the Secondary bridges v_{rn}(v_{rn}: 450V/div), Currents through the primary winding of the transformer (i_a: 20A/div), and current through the secondary windings of the transformer (i_r: 20A/div). Timescale: 200μs/div.

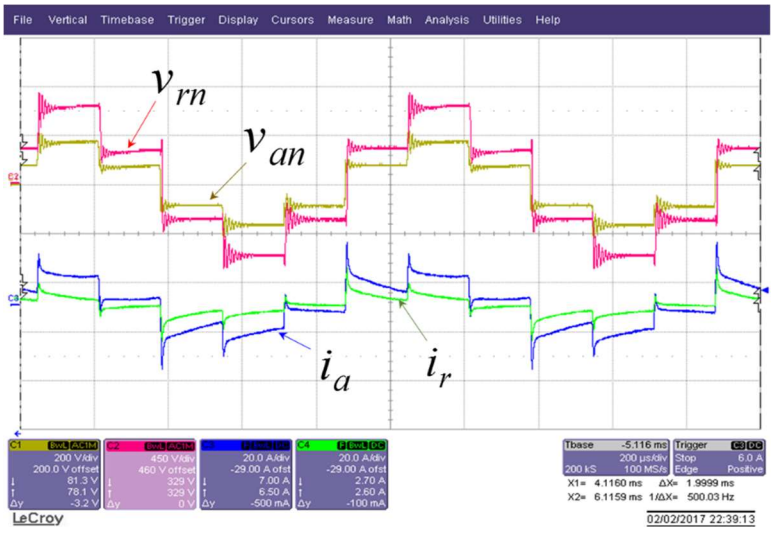


Figure 6. 12 Experimental results of the 3DAB converter at 6.5kW with control phase shift angle φ= 2.2°. Voltages generated by the primary bridges v_{an} (v_{an}: 200 V/div), voltage generated by the Secondary bridges v_{rn} (v_{rn}: 450V/div), Currents through the primary winding of the transformer (i_a: 20A/div), and current through the secondary windings of the transformer (i_r: 20A/div). Timescale: 200μs/div.

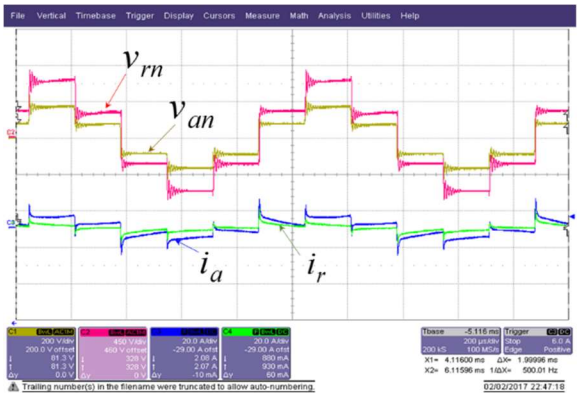
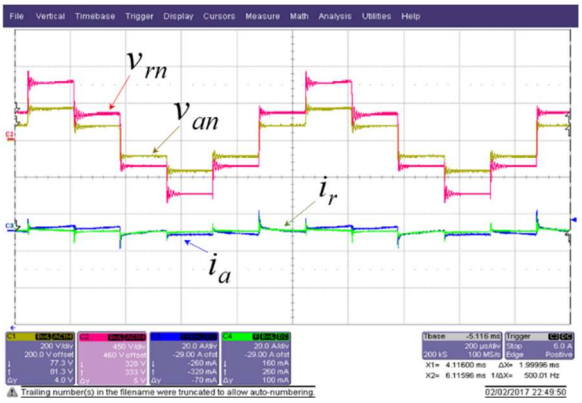
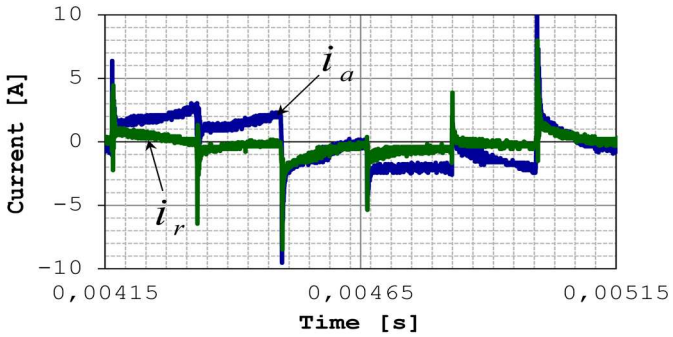


Figure 6. 13 Experimental results of the 3DAB converter at 3.3kW with control phase shift angle φ= 1.3°. Voltages generated by the primary bridges v_{an} (v_{an}: 200V/div), voltage generated by the Secondary bridges v_{rn} (v_{rn}: 450V/div), Currents through the primary winding of the transformer (i_a: 20A/div), and current through the secondary windings of the transformer (i_r: 20A/div). Timescale: 200μs/div.



(a)



(b)

Figure 6. 14 Experimental results of the 3DAB converter at 1.3kW with control phase shift angle φ= 0.4°: (a) voltages generated by the primary bridges v_{an} (v_{an}: 200V/div), voltage generated by the Secondary bridges v_{rn} (v_{rn}: 250V/div), Currents through the primary winding of the transformer (i_a: 20A/div), and current through the secondary windings of the transformer (i_r: 20A/div). Timescale: 200μs/div. (b) currents generated for 1 switching period.

6.2 Comparison of calculated control angle and optimised control angle

To verify the theorectical analysis in Chapter 3, the 10-kVA laboratory prototype was implemented. For these results, a snubber value of 10 nF in the low voltage level bridge was used. For the 9.5-kVA power transfer, an initial control angle of 2.0° was calculated with (3.25) and compared to an optimised control angle adjusted by (3.24). The transferred power was adjusted by shifting the switching times of the primary bridge to the secondary bridge with the control angle. The initial value was calculated from the symmetric leakage inductance of the practical transformer. However, in real operation conditions, the dead time effect becomes significant. In this circumstance, it is not sufficient to obtain the desired output power as it can lead to voltage drop in the output DC bus. Therefore, it is reasonable to compensate a sufficiently high value to achieve a desired power transfer in real operation conditions.

Fig. 6.15 (a) shows the normalised output DC voltages for different values of φ. For φ = 2.0° (calculated value), it can be seen that at the maximum power tansfer, approximately 1.5% of the generated voltage is lost acoss the resistive load. However, under compensated phase-shift modulation, the voltage drop is substantially smaller than for the fundemental modulation. The trend in the experimental curve shows that for the low power transfer points, the output voltage drop is close to zero. Fig. 6.15 (b) plots the output power rating against the calculated and optimsied control phase-shift values. Clearly, given the operating range of the 3DAB converter, output power increases with optimised phase-shift control angles.

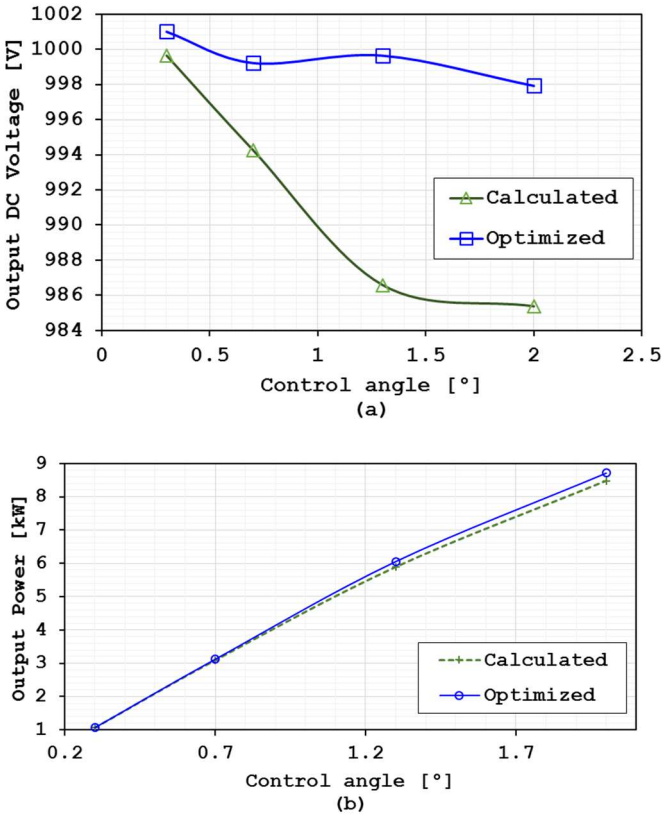


Figure 6. 15 Experimental results of output voltages & output powers of the 3DAB converter operated by optimised phase shift angles compared with calculated values.

6.3 Comparison of turn-off commutation time comparison for different snubber values

The different values of snubber capacitors and the consequent changes in turn-off commutation times have an influence on the characteristics of the 3DAB converter operation as illustrated in Chapter 4. Since snubber capacitances may generally differ between the primary bridge and secondary bridge, individual turn-off times are defined for each bridge. The main evaluation of the prototype carried out in this section is to deliver a comparison of the measured commutation times and waveform characteristics of the converter concept presented in Chapter 3. Furthermore, this experimental validation serves to verify the developed analytical descriptions for the commutation processes in the lossless snubber-equipped 3DAB converter presented in Chapter 3. As the influence of snubbers and parasitic elements on switching transients is accounted for by the experimentation, more accurate results are obtained.

The turn-off times for the converter are measured for a power range from 1.3 kW to 9.5 kW. For validation, the optimised values of the phase-shift angle were used to meet the demand of the power transfers. For all the measurements, the power flow in the 3DAB converter was from the primary bridge, with a 500-VDC input voltage, to the secondary bridge, with 1000-VDC link voltage.

6.3.1 Turn-off Commutation time in primary bridge

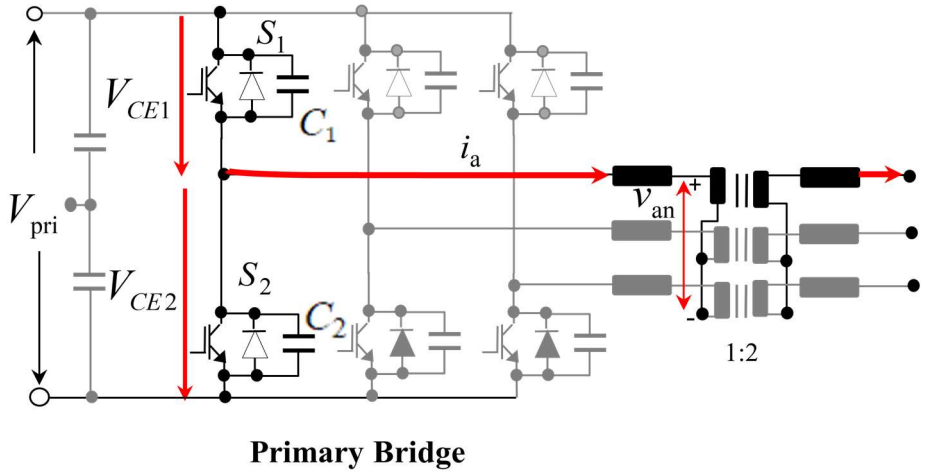


Figure 6. 16 Schematic of test circuit used for validating turn-off commutation time in the primary bridge of the 3 DAB converter

In order to validate turn-off commutation times, the experimental measurement system is shown in Fig. 6.16. Regarding Fig. 6.17(a) and (b), the collector–emitter voltages in the primary bridge IGBT module and AC-link waveforms of the primary winding of the transformer with two different snubber capacitances of 22 nF and 10 nF, running under open loop conditions and at 9.5 kW, are shown. As can be seen, the measured commutation times during the turn off of the IGBTs are larger than the defined dead time. The proposed dead time was calculated using Eq. (3.22). In this equation, the defined parameters can be found in datasheet of the IGBT module [117]. According to the datasheet, the minimum value for the dead time must be larger than 910 ns. The calculated dead time was limited by 1% of the f_{sw} (1 kHz) to avoid a reduction of the transferred power. Therefore, a dead time can be set between 910 ns and 10µs to insure that both high-side leg and low-side leg of the IGBT half bridge are not enabled at the same time during the commutations. For the

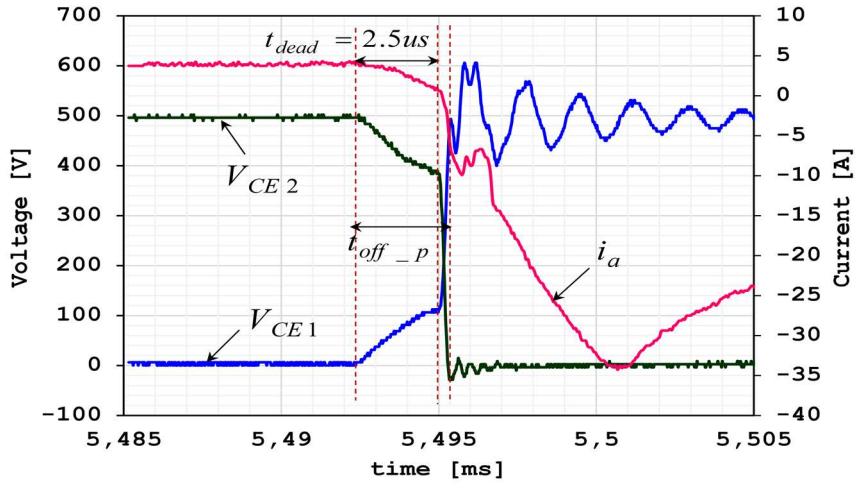
implementation, a typical value of 2.5 μs for the dead time was selected to verify the effect of different snubber values. As already mentioned above, the dead time should be chosen one as large as or as small as possible to satisfy the need of avoiding short-circiut in the IGBT half bridge.

In these situations, the primary side converter, having 500-VDC input voltage, is operated in hard switching mode because the primary winding current i_a is not sufficient to reduce the primary winding terminal voltage V_{an} to zero during the dead time. During hard commutations, the significant slow voltage ramp changes have been measured with the both capacitance values at the dead time interval. This is due to the low tail current on the IGBT device. When the dead time is over, the voltages experience a shorter rise at the ending of the dead time. As a consequence, the high dv/dt transients can cause increased losses in the IGBT module.

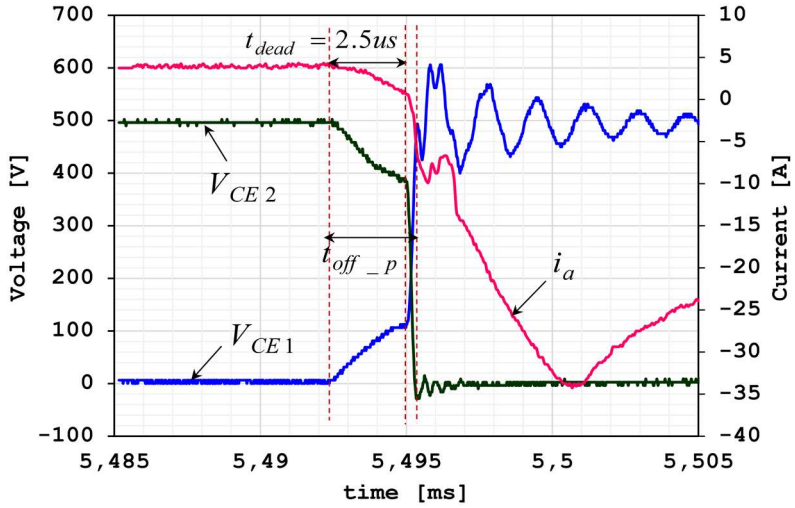
Fig. 6.17 (c) shows a comparison of commutation times of the primary side converter at the two different snubber capacitance values. From the measurement, it can be noted that low capacitance has the function to reduce the commutation time in the semiconductor, so that the voltage times are approximately proportional to the capacitance values.

The following figures show the measured commutation waveforms in the primary side with 500-VDC input voltage for different levels of power transfer in the prototype. In Fig. 6.18, the turn-off transient waveforms for 6.5 kW in one IGBT module of the primary bridge with snubber capacitor values of 22 nF and 10 nF are illustrated. In the primary bridge, hard commutation is already appearing at 6.5-kW power transfer. As can be seen, by reducing the snubber value, the turn-off time at the power transfer is also reduced.

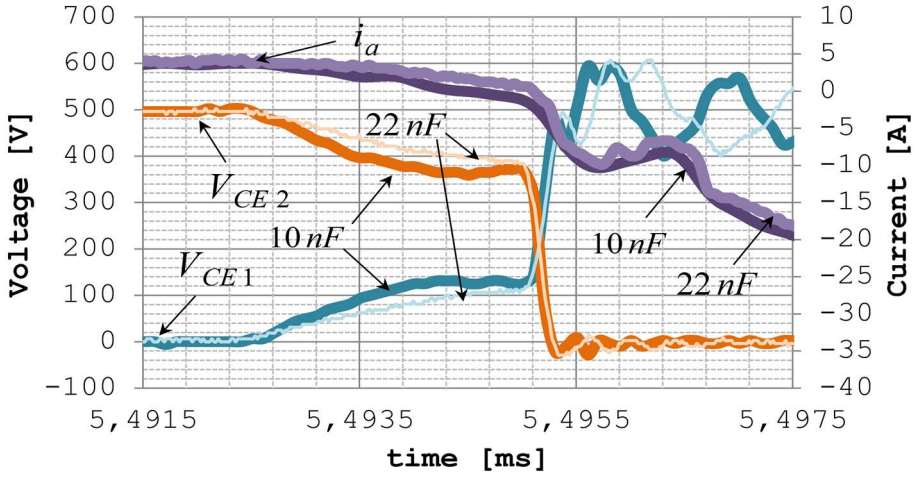
Fig. 6.19 and 6.20 show hard-switched turn-off transients obtained with the two different capacitances at lower power levels. It can be seen from these figures that hard-switching can occur also in the primary side bridge while the 3DAB converter is operating at power lower than 3.3 kW. This can be explained since the hard-switched turn-off was carried out with the higher used snubber capacitances of 22 nF and 10 nF for all power levels.



(a)

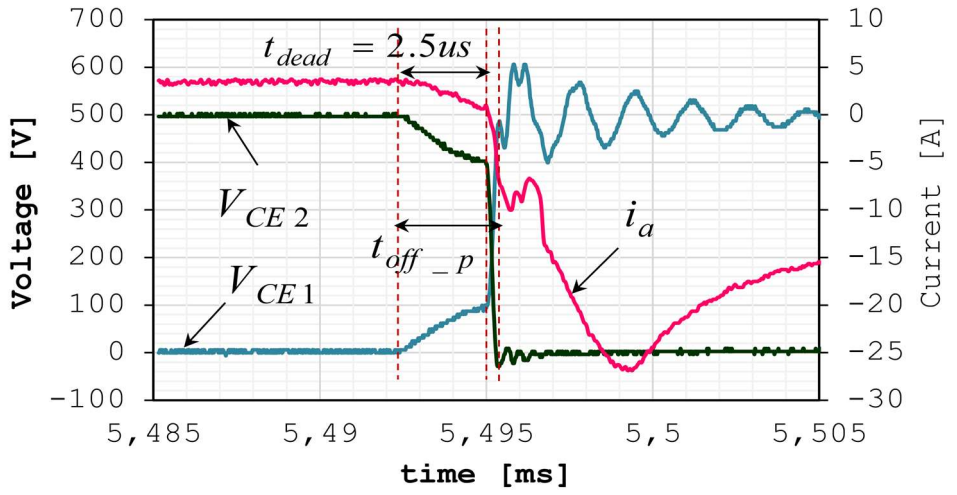


(b)

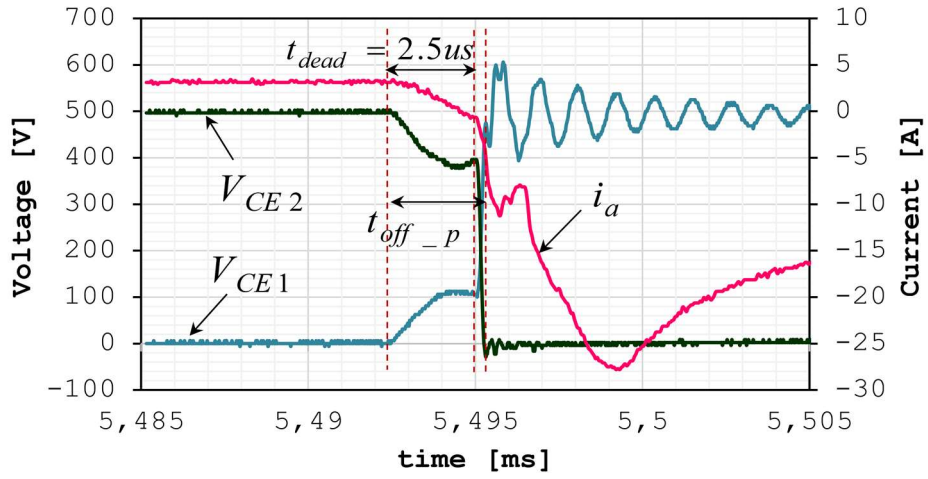


(c)

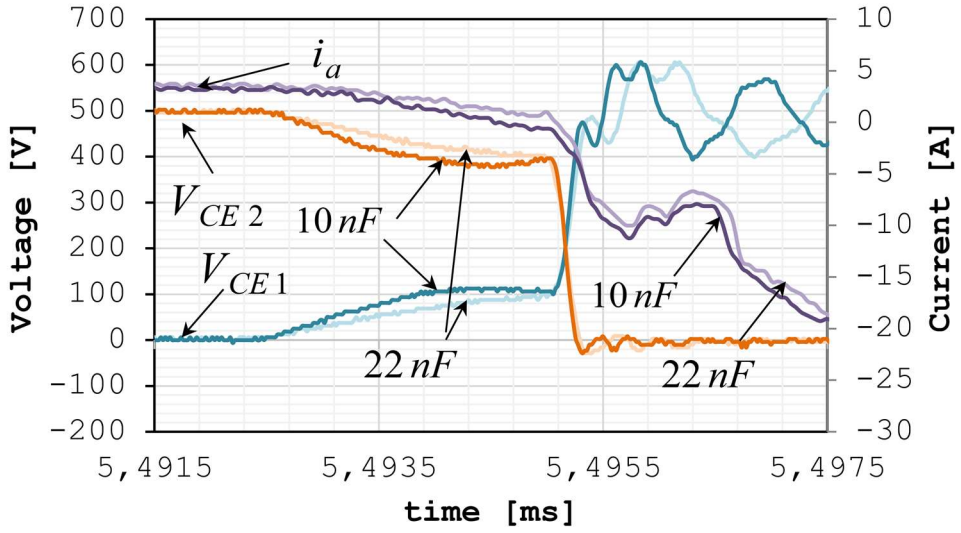
Figure 6. 17 Turn-off Commutation in secondary bridge at 9.5kW: collector – emitter voltages in half-bridge IGBT module, voltage generated by the primary bridges v_{an} and currents through the primary winding of the transformer (a) with 22nF snubber, (b) with 10nF snubber, and (c) comparison.



(a)



(b)



(c)

Figure 6. 18 Turn-off Commutation in primary bridge at 6.5kW: collector – emitter voltages in half-bridge IGBT module, voltage generated by the primary bridges v_{an} and currents through the primary winding of the transformer (a) with 22nF snubber, (b) with 10nF snubber, and (c) comparison.

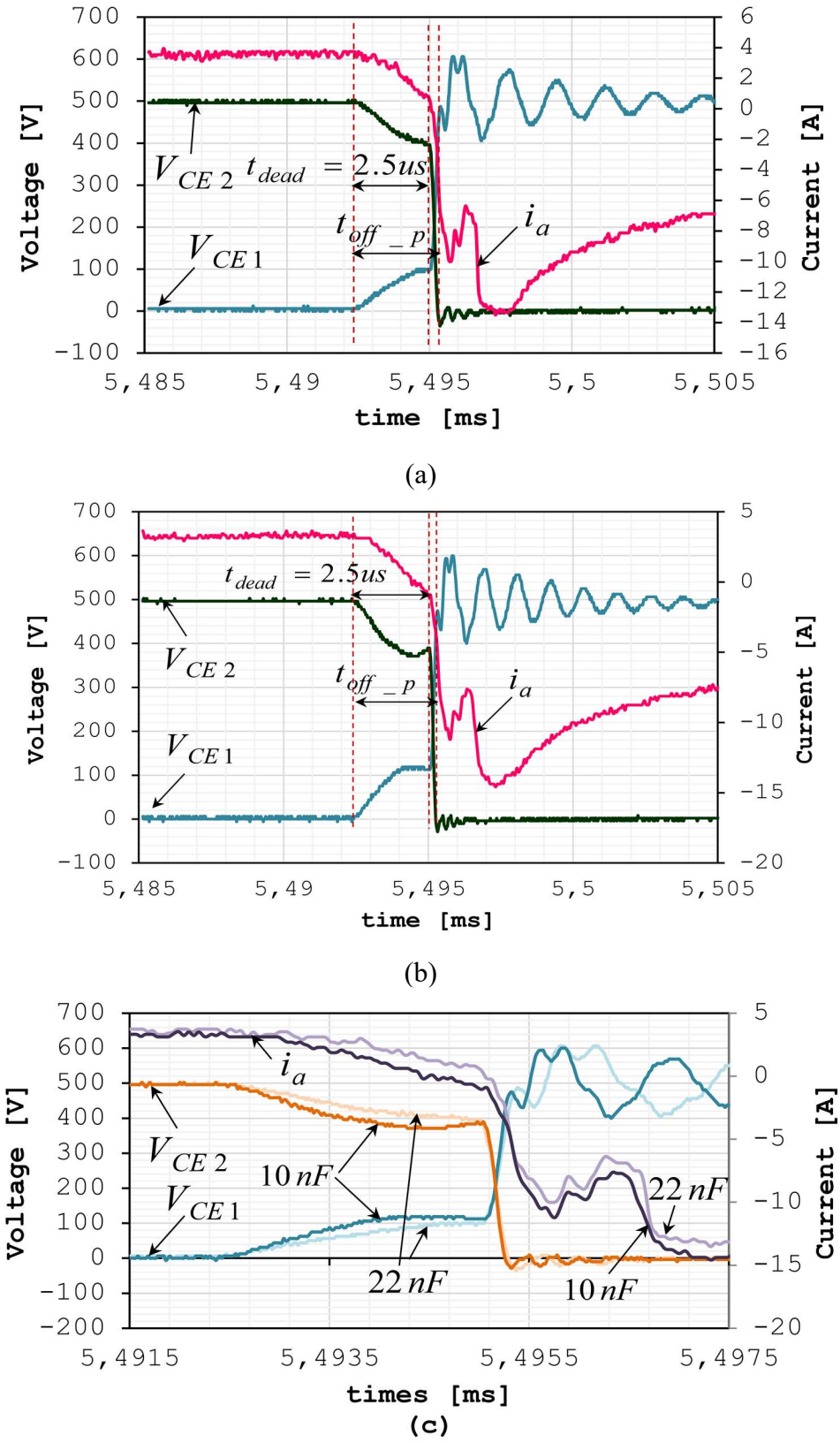
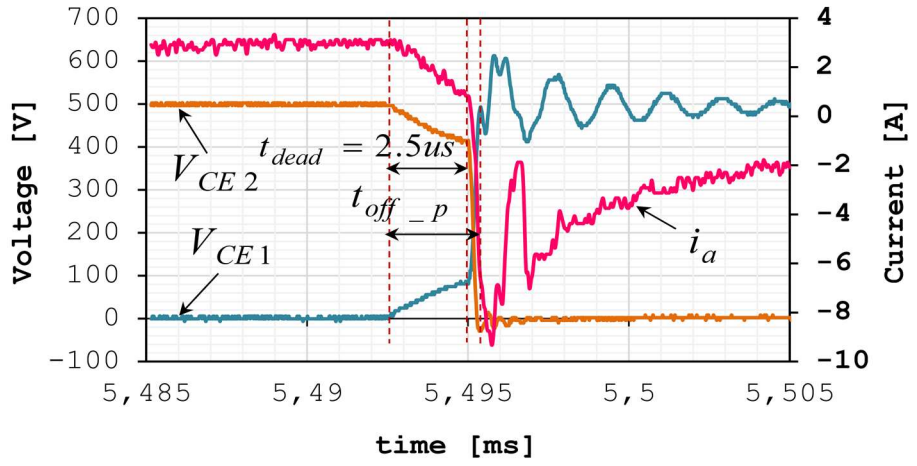
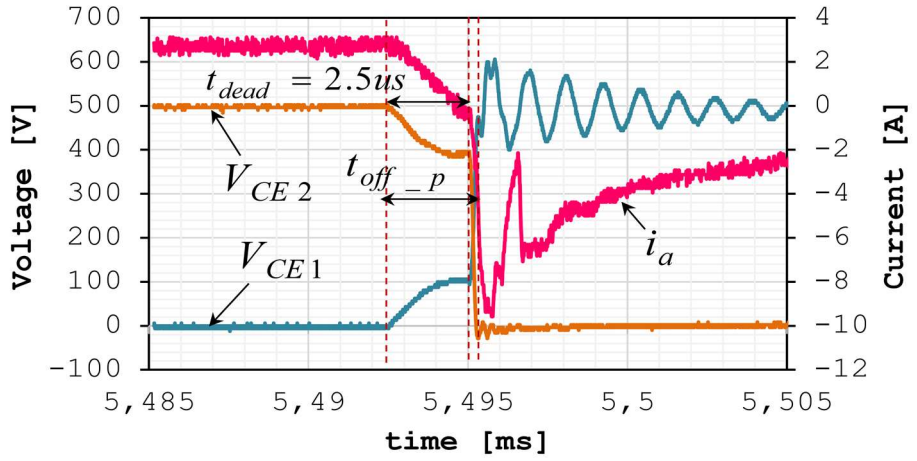


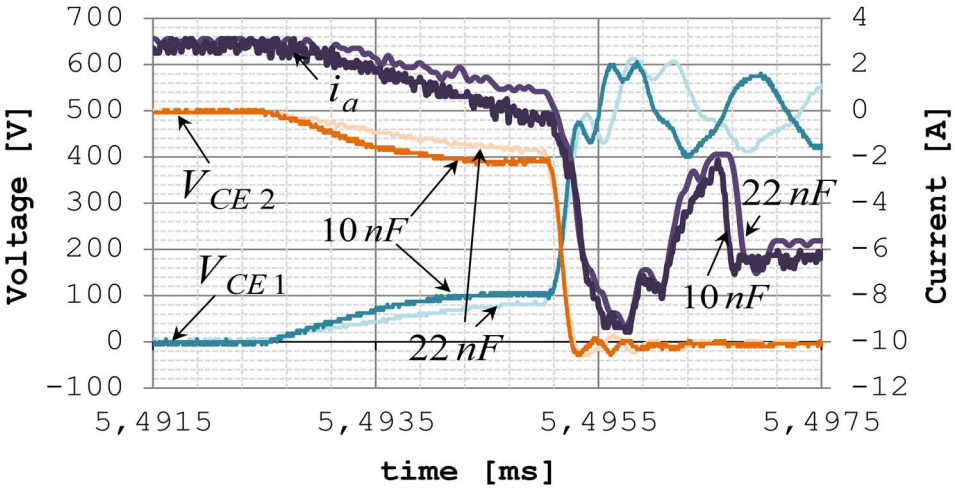
Figure 6. 19 Turn-off Commutation in primary bridge at 3.3kW: : collector – emitter voltages in half-bridge IGBT module, voltage generated by the primary bridges v_{an} and currents through the primary winding of the transformer (a) with 22nF snubber, (b) with 10nF snubber, and (c) comparison.



(a)



(b)



(c)

Figure 6. 20 Turn-off Commutation in primary bridge at 1.3kW: collector – emitter voltages in half-bridge IGBT module, voltage generated by the primary bridges v_{an} and currents through the primary winding of the transformer (a) with 22nF snubber, (b) with 10nF snubber, and (c) comparison.

6.3.2 Turn-off Commutation time in secondary bridge

The following figures illustrate the turn-off commutation waveforms in the secondary side bridge connected with 1000-VDC load for different power levels. These turn-off transients were obtained with capacitances of $C_{sn_s} = 10\,nF, 6.8\,nF$.

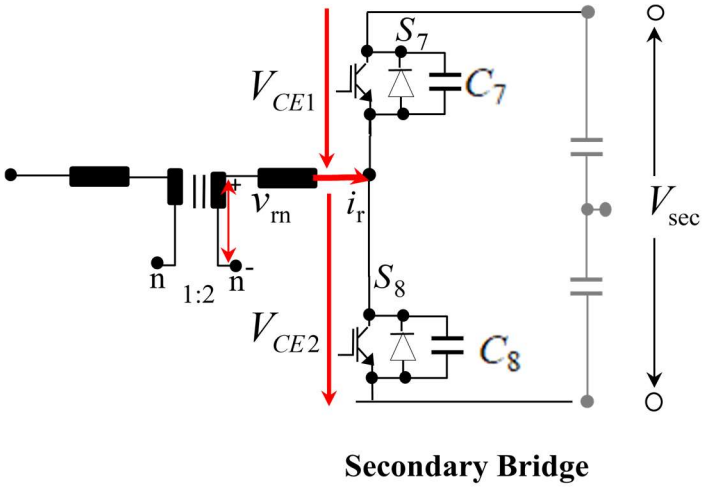


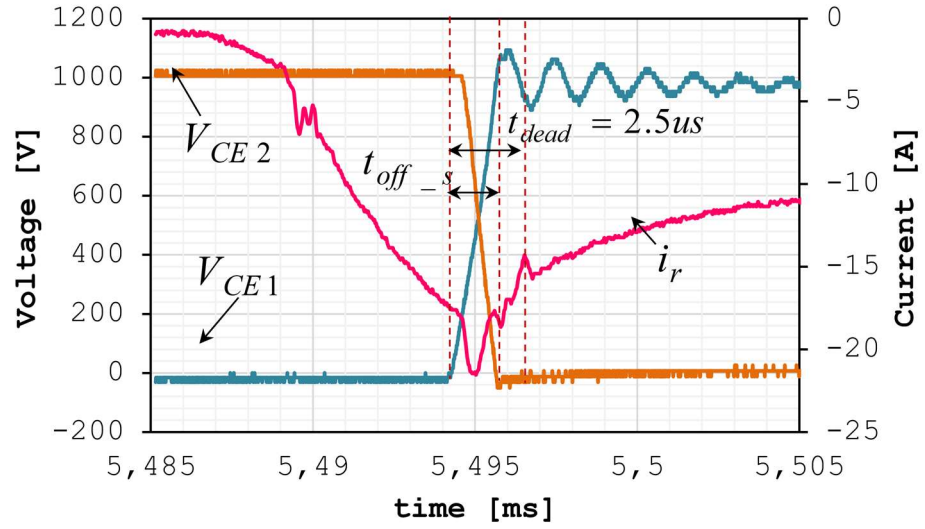
Figure 6. 21 Schematic of test circuit used for validating turn-off commutation time in the secondary bridge of the 3 DAB converter

In Fig. 6.22, the measured commutation waveforms for 9.5 kW are shown. As the secondary side bridge voltage has been set higher than the primary side voltage, the secondary winding current is negative at the turn-off switching. Theoretically, a ZVS switching transition occurs when the switched AC-link current is negative for a positive turn-off switched output transition. As can be seen, the measured waveforms confirm that the ZVS is appearing in the real converter. For the different capacitor values, the ZVS always appears at 9.5 kW. In the ZVS switching situation, the secondary winding current is enough to reduce the V_{CE2} of *S*7 to zero during the dead time. As a consequence, the turn-off commutation time is faster than the dead time. After the dead time is elaped, *S*8 is turned on, and the voltage V_{CE2} reaches zero. According to Fig. 6.22 (c), when using a smaller snubber capacitor value of 6.8 nF, the turn-off commutation time is reduced.

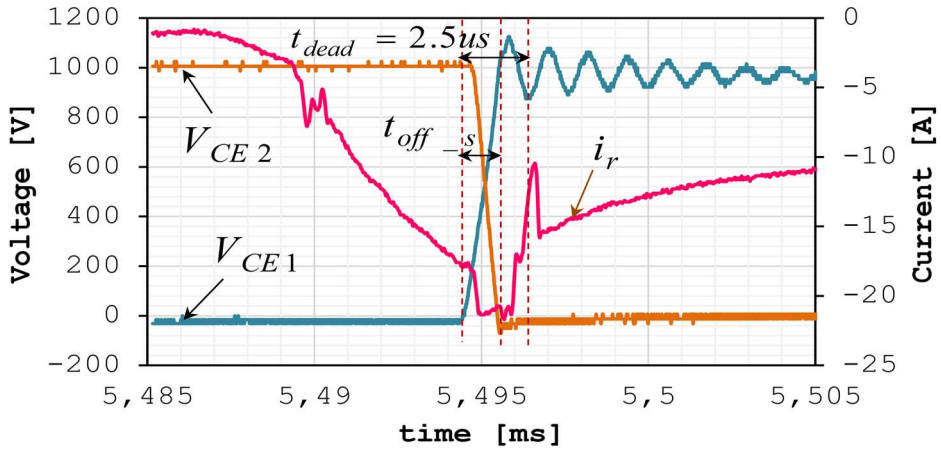
The following figures show the measured commutation waveforms for the secondary side having 1000-VDC output voltage for different power levels in the 3DAB converter. Fig. 6.23 shows the measured turn-off commutation waveforms for 6.5 kW in one IGBT half bridge of the secondary side. In the secondary bridge, ZVS commutation is already appearing at 6.5-kW power transfer. As can be seen, reduction in the capacitance value of $C_{sn_s} = 6.8nF$ also reduced the turn-off commutation time.

Fig. 6.24 depicts the measured turn-off commutation waveforms for 3.3 kW. There is still ZVS switching for the secondary bridge at 3.3 kW. As a consequence of the smaller capacitance, the transient time during turn-off commutation is faster than in case of a higher value. In the experimental validation, ZVS has been always present at certain power levels.

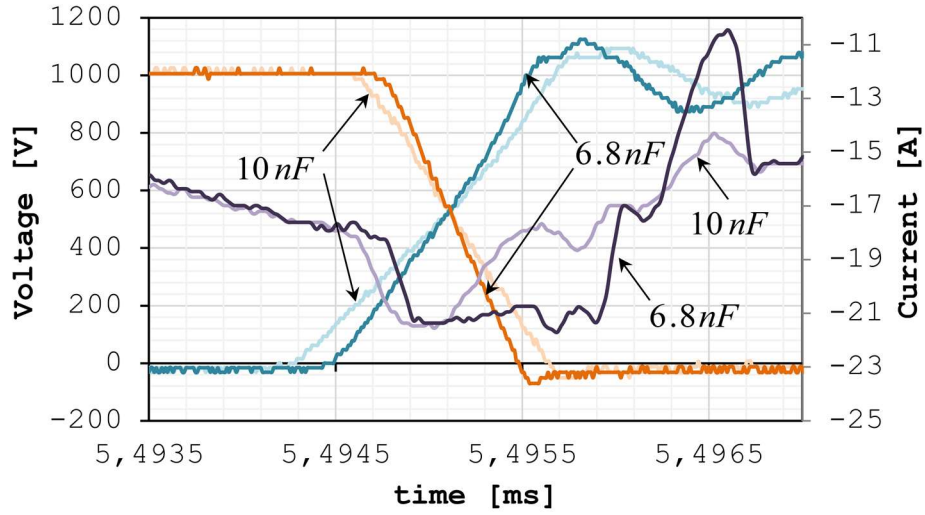
In Fig. 6.25, hard-switched turn-off transients are obtained in the secondary bridge with the two different capacitances at a lower power level. It can be seen that hard-switching appears in the secondary side bridge while the 3DAB converter is operating at substantially light load conditions. From the evaluation, it can be assumed that the urn-off commutation duration is reduced by reducing the snubber capacitance value for the different power ranges.



(a)

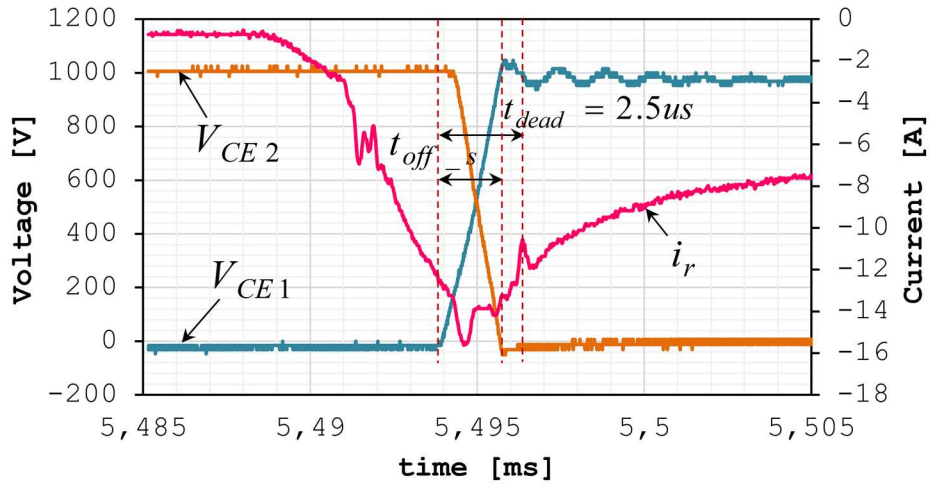


(b)

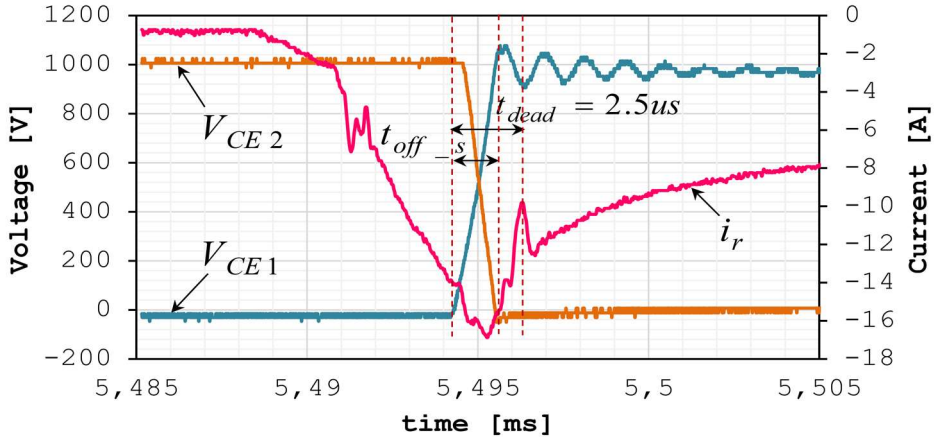


(c)

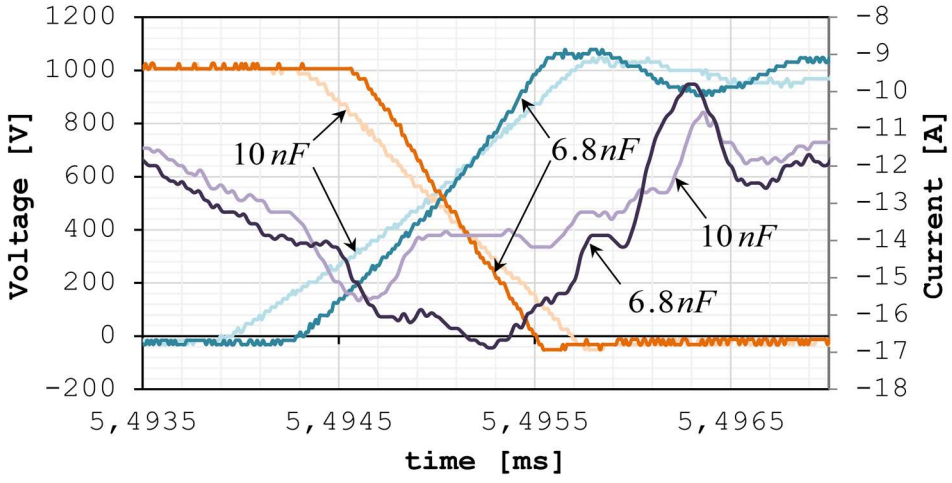
Figure 6. 22 Turn-off Commutation in secondary bridge at 9.5kW: collector – emitter voltages in half-bridge IGBT module, voltage generated by the secondary bridges v_{rn} and currents through the secondary winding of the transformer (a) with 10nF snubber, (b) with 6.8nF snubber, and (c) comparison



(a)

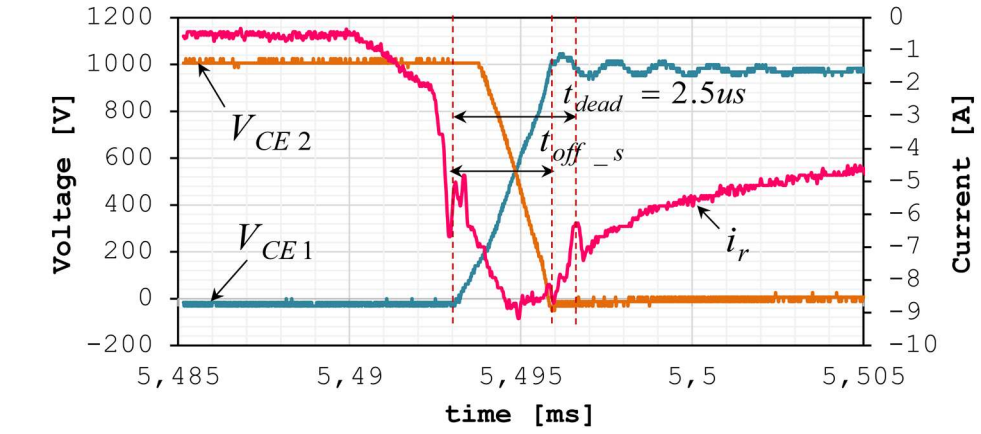


(b)

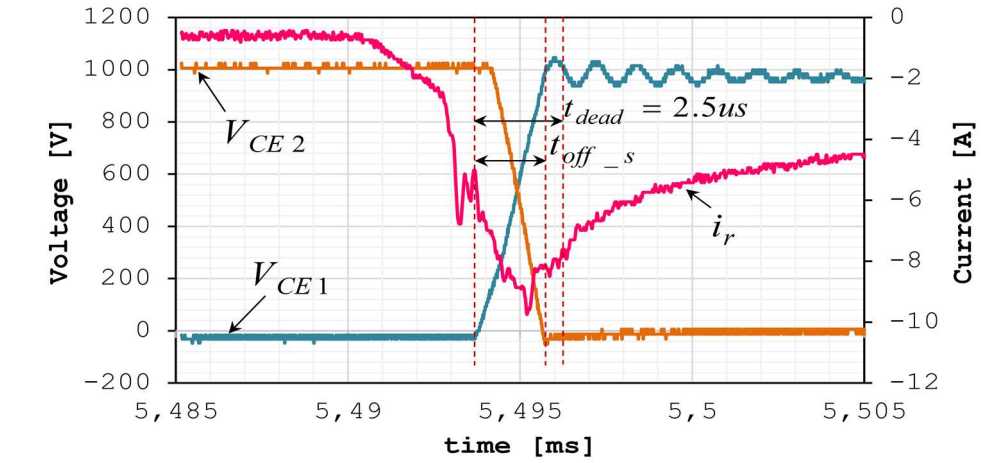


(c)

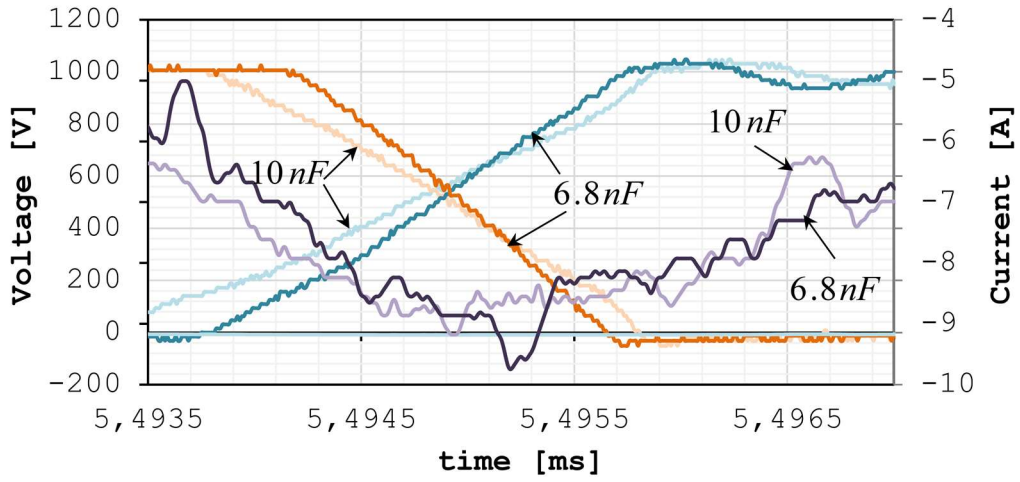
Figure 6. 23 Turn-off Commutation in secondary bridge at 6.5kW: collector – emitter voltages in half-bridge IGBT module, voltage generated by the secondary bridges v_{rn} and currents through the secondary winding of the transformer (a) with 10nF snubber, (b) with 6.8nF snubber, and (c) comparison



(a)

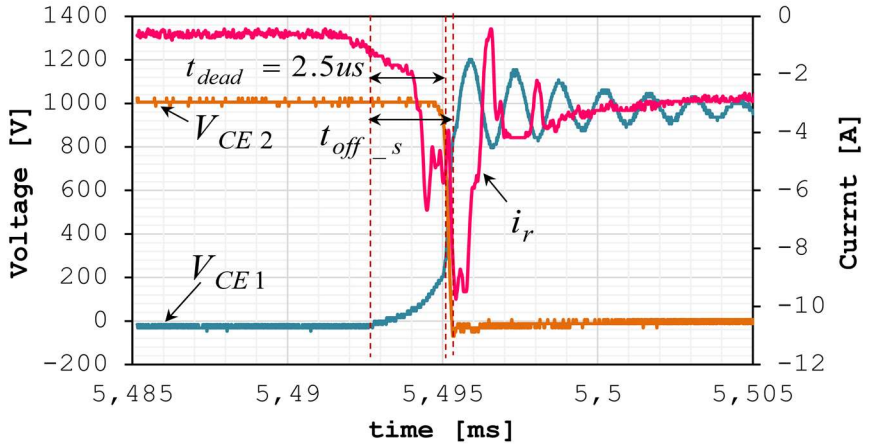


(b)

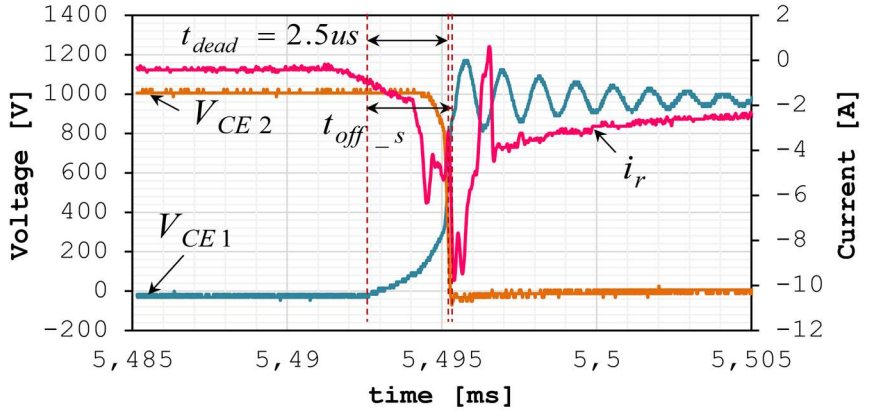


(c)

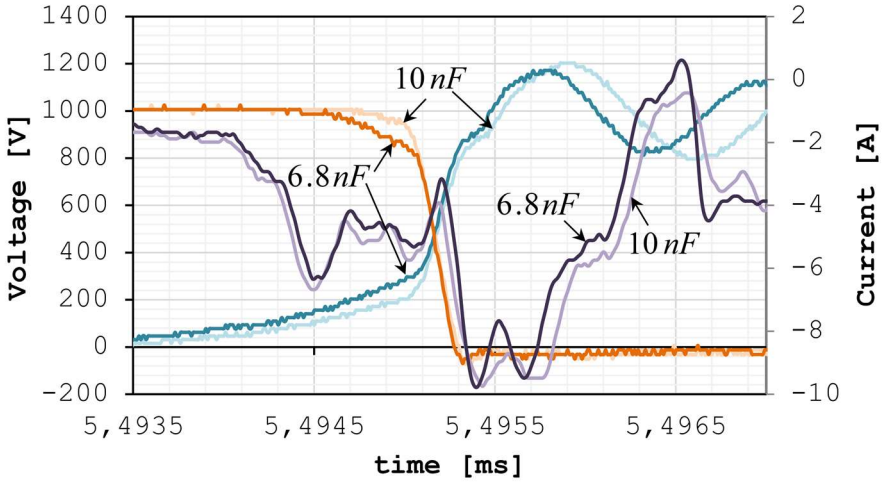
Figure 6. 24 Turn-off Commutation in secondary bridge at 3.3kW: collector – emitter voltages in half-bridge IGBT module, voltage generated by the secondary bridges v_{rn} and currents through the secondary winding of the transformer (a) with 10nF snubber, (b) with 6.8nF snubber, and (c) comparison



(a)



(b)



(c)

Figure 6. 25 Turn-off Commutation in secondary bridge at 1.3kW: collector – emitter voltages in half-bridge IGBT module, voltage generated by the secondary bridges v_{rn} and currents through the secondary winding of the transformer (a) with 10nF snubber, (b) with 6.8nF snubber, and (c) comparison

6.4 Measurement of converter efficiency

Fig. 6.26 and 6.27 show the power loss/efficiency characteristics for the 3DAB converter which have been measured with different values for the snubber capacitor and without any snubber. The converter's efficiency was measured from 1.3 kW to 9.5 kW for power flow from the DC power source to the converter. In the experiments, the same value of capacitance for the snubber circuit was applied in both sides of the converter. At low power levels, efficiencies drop rapidly when using a snubber capacitor of 22 nF, remaining above 80% for power levels above 15% of the converter rating. Conversely, for low power, the efficiency in the converter is higher when using no snubber capacitor. At increased power levels to 50% of rated power, the efficiencies increase with higher capacitance. Relatively flat efficiency plateaus form above 50% of rated power in all cases of different snubber capacitor values and without snubber capacitors. The maximum efficiency of 94.86% when using a snubber capacitor of 10 nF was obtained at 4.8 kW. The maximum efficiency of 94.58% without snubber capacitor is reached at 4.5 kW. The efficiencies remain above 90% for a power higher than 3 kW of the converter transferred power rating for all snubber capacitance values and without a snubber.

Based on these results, a snubber capacitor of 10 nF was selected for the primary side bridge. For the secondary high voltage bridge, smaller capacitances were applied. Fig. 6.28 shows the measured efficiencies at different snubber values in the secondary bridge. All measurements were carried out with a snubber capacitance of 10 nF for the primary bridge. In case of the smallest used secondary bridge snubber capacitance of 1 nF, efficiency at the low power transfer point (i.e. 1.3 kW) already increased by 2.5 % in the case of capacitance of 6.8 nF and 1% in the case of 3.3 nF capacitance. It can be seen from the figure that a further increase in the capacitance leads to further loss at increasing power levels. This can be explained by the influence of increasing snubber capacitances taking low tail currents of the IGBT device as well as a fast turn-off commutation time. In consequence, a 6.8-nF capacitance for the secondary bridge can be considered an optimal value for the corresponding power level.

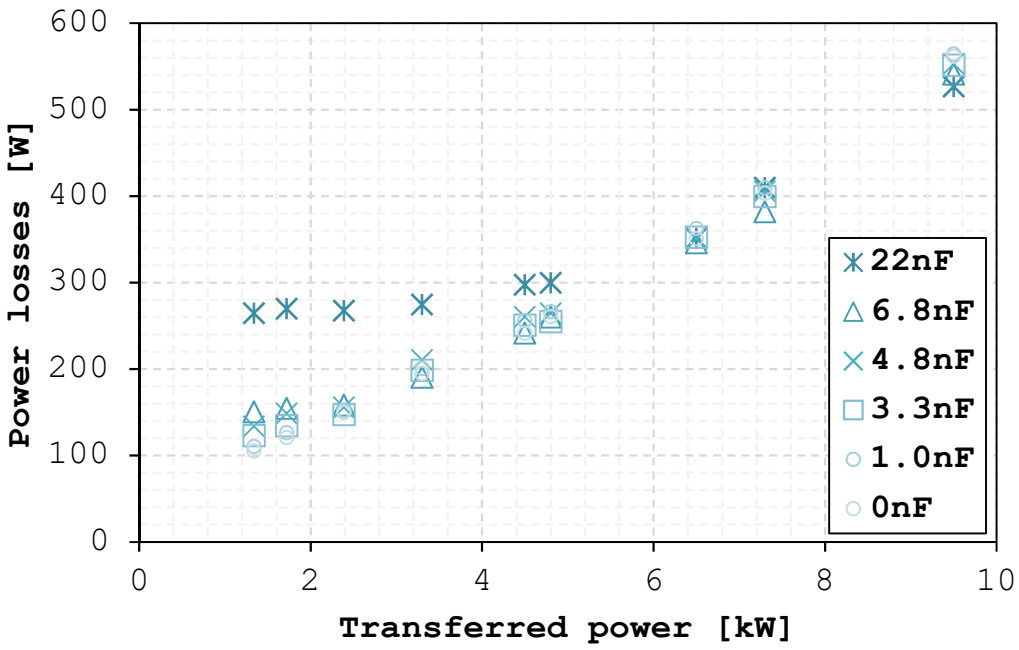


Figure 6. 26 The 3DAB converter's loss comparison with different snubber capacitors.

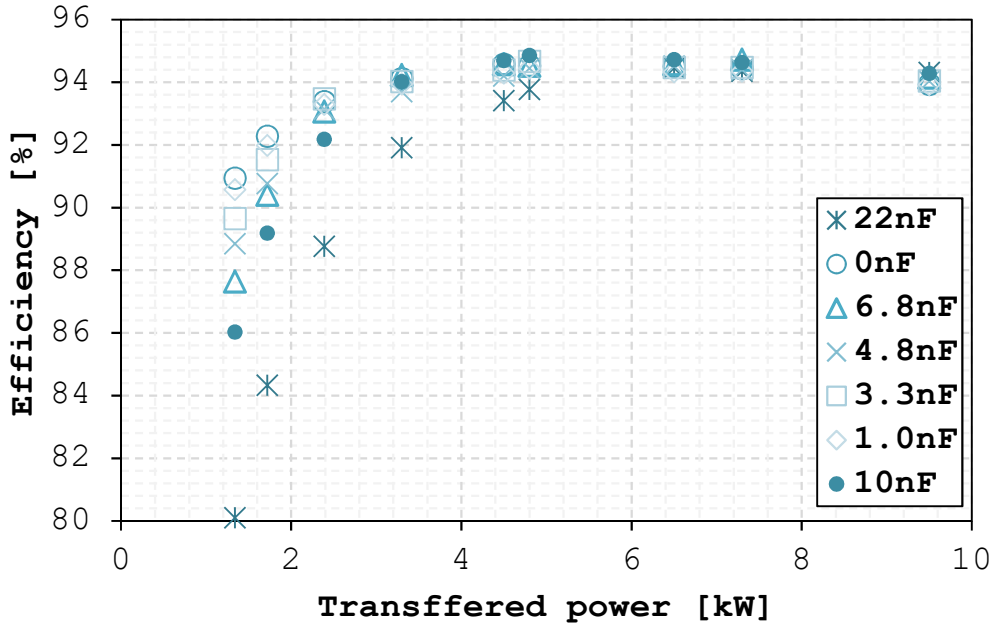


Figure 6. 27 The 3DAB converter's efficiency comparison with different snubber capacitors.

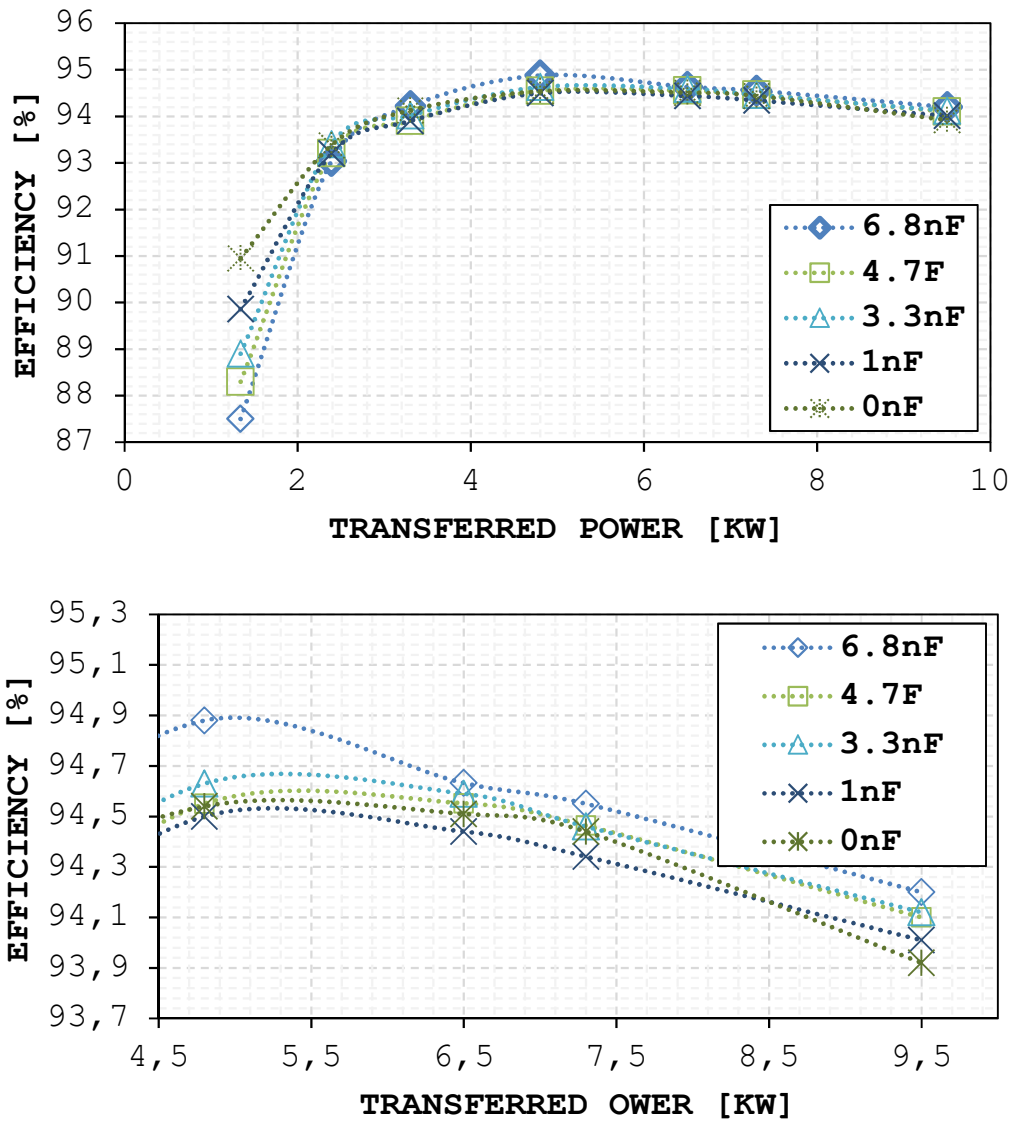


Figure 6. 28 The 3DAB converter's efficiency comparison with 10nF snubber in the primary bridge and different snubber capacitors in the secondary bridge

The snubber capacitors were individually optimised according to the above experimental procedures. As a consequence, a snubber capacitor size of 10 nF was selected for the 500-VDC primary side bridge and 6.8 nF capacitance was chosen for the 1000-VDC secondary bridge. Fig. 6.29 shows the power loss characteristics of the 3DAB converter obtained with the optimised snubber capacitances. The results take conduction losses and switching losses of the IGBTs into account as well as core and winding losses of the transformer. Legend information for loss distribution diagrams of simulation results is illustrated below. A IGBT trench module (SKM75GB176D) rated at 1700 V and 80 A were used to measure the losses of the used semiconductor switches in the

system considering the 3DAB converter. The measured values of IGBTs_pri and IGBTs_sec indicate the losses of the IGBT module included the anti-parallel diode.

- Core : Transformer core loss,
- Cu_Pri : Transformer primary winding loss
- Cu_Sec : Transformer secondary winding loss
- IGBTs_Pri : IGBT module losses on primary side
- IGBTs_Sec : IGBT module losses on secondary side

On comparing the HV secondary bridge, one generally finds the losses in the IGBT modules in the LV primary bridge switches are drastically increased towards higher power level (over 50% full level). Hence, conduction losses are increased with an increase in the transferred power. On the other hand, the switching losses at HV level are slightly higher than the LV bridge switches. The core loss is considered the main part of the power dissipation for the prototype. It has further been illustrated that using a high-efficiency core material can potentially increase the overall performance of the 3DAB converter. The measured efficiencies are presented against transferred power in Fig. 6.30. As can be seen, the efficiency of the 3DAB converter generally increases towards higher powers. Here, a 94.2% efficiency of the converter is reached at the full load amount to 9.5 kW. The maximum efficiency of 94.88 % is reached at 4.8 kW. It can be seen that efficiencies above 90% can be achieved when operated above 20% of the rated power level. This is mainly due to the lower turn-on and turn-off energy losses of the IGBT module in relation to the 3DAB converter. Of note, the developed transformer with measured peak efficiency of almost 97% at rated power was used in the converter. Hence, from the measured results, it can be seen that the transformer losses clearly dominate overall converter losses. The experimental results for the converter efficiency are comparable to the simulation results in Fig. 6.30. It can be observed that the variation between the experimental results and the simulation results is below 1%.

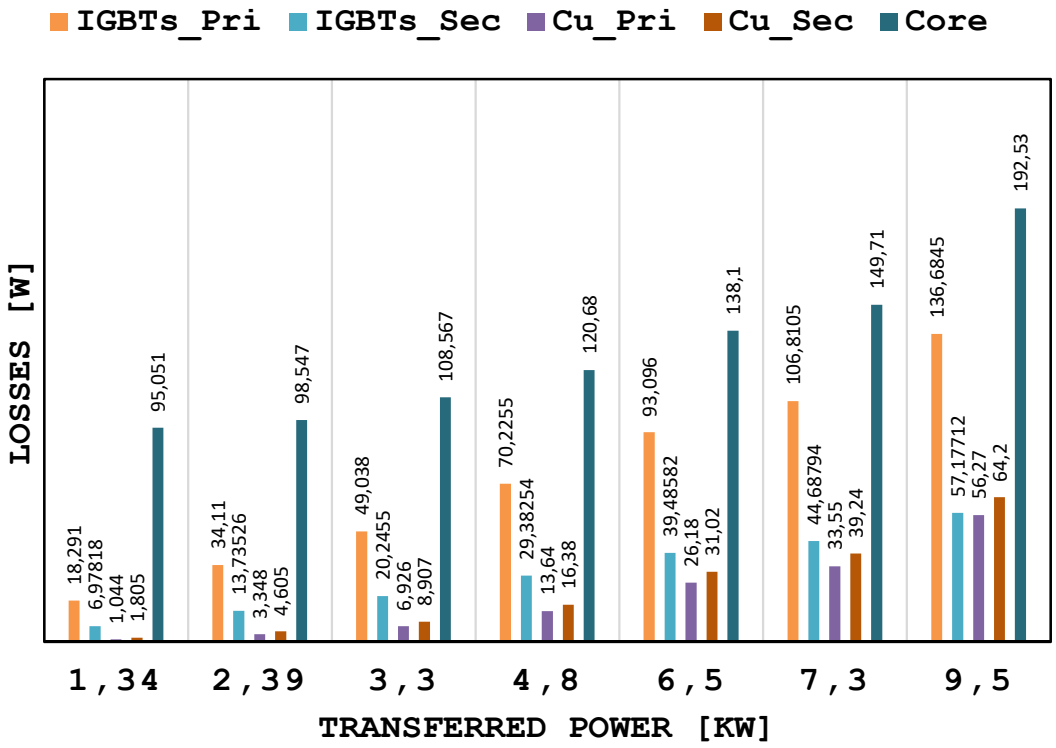


Figure 6. 29 Power losses distribution of the 3DAB converter with10nF snubber in the primary bridge and 6.8nF snubber capacitors in the secondary bridge

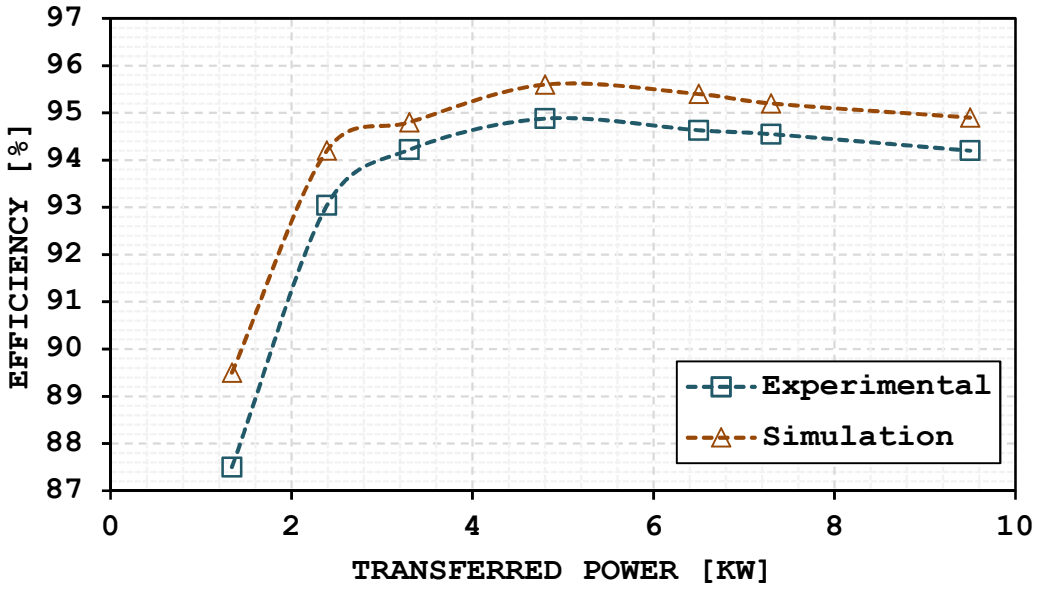


Figure 6. 30 Efficiency of the 3DAB converter with10nF snubber in the primary bridge and 6.8nF snubber capacitors in the secondary bridge

6.5 Reverse direction of the power flow

6.5.1 Reverse power flow control in 3DAB converter

In order to validate the reverse power flow of the developed IGBT-based 3DAB converter device, the simplified schematic of the converter is shown in Fig. 6.31. The 3DAB converter can transfer power in both directions, so the input and output sides are arbitrary.

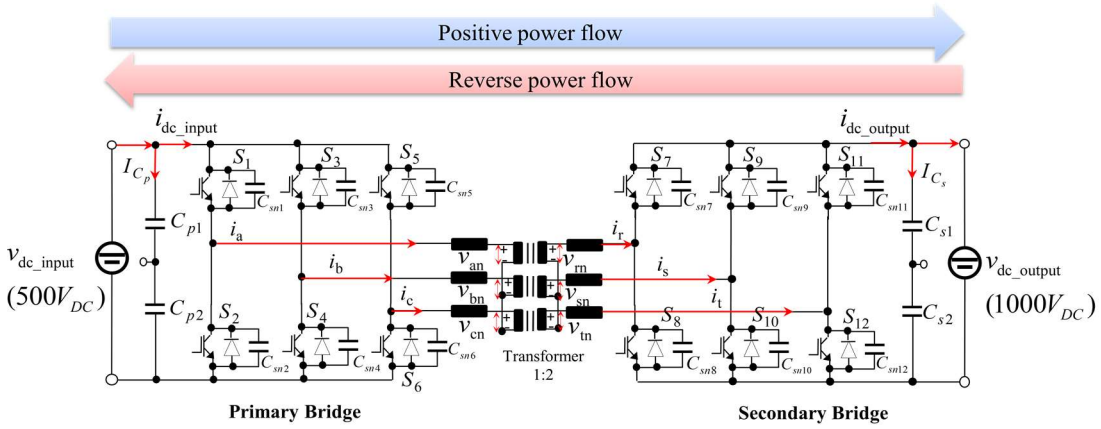


Figure 6. 31 IGBT based 3 DAB converter

Equation (6.1) indicates that the power flow in the AC-link terminals can be calculated using voltage magnitudes at the DC terminals of primary and secondary bridge and the phase-shift angle φ between these voltages, as shown in Fig. 6.31.

$$P_o = \frac{V_{pri}^2}{\omega_{sw} L_\sigma} \cdot d \cdot \varphi \left[\frac{2}{3} - \frac{\varphi}{2\pi} \right] \quad \text{for} \left(0 \le \varphi \le \pi/3 \right) \tag{6.1}$$

Here, the phase -shift angle is the only available degree of freedom that can be used to control power flow direction. To simplify analysis, the common way of operating the 3DAB converter consists of using positive values of the phase-shift angle to validate the power transfer characteristics of the 3DAB converter as per (6.1). With negative phase-shift angles, the direction of power flow is inverted.

6.5.2 Validation in Simulation model

Adopting a 3DAB for unidirectional power flow is not a sensible choice. Reverse power flow was ensured in the simulation and comments were added on whether it affects the proposed design procedure.

In the following section, transfer characteristics of the 3DAB converter developed as in chapter 7 are also valid for the reserve direction of the power flow. Taking phase '*a*' and '*r*' as an example, operation waveforms are shown in Fig. 6.32. For the positive power flow condition, simulated waveforms of V_{an}, V_{rn}, i_a, and i_r are shown in Fig. 6.32 (a). Additionally, Fig. 6.32(b) shows the reverse power flow condition. As can be seen, the terminal voltages of the transformer are leading or lagging at the different power flow modes.

Fig. 6.33 (a) shows the simulated waveforms of the DC link current of the secondary bridge at the different power flow modes. The peak current when the secondary DC voltage is 1000 V while the primary DC voltage is 500 V at P_o = 10 kW from primary bridge to secondary is close to 10 A. Under reverse power flow mode of P_o from secondary bridge to primary, the peak current is also limited below 10 A. The magnitude of the secondary DC link current at the reverse power flow mode is the same as that in the positive power flow mode. Fig. 6.33 (b) shows rated transferable power when the peak current in the DC link of the secondary bridge, i_{dc_output}, is limited under 10 A. As can be seen, the power transfer P_o is limited below 10 kW under different power flow modes.

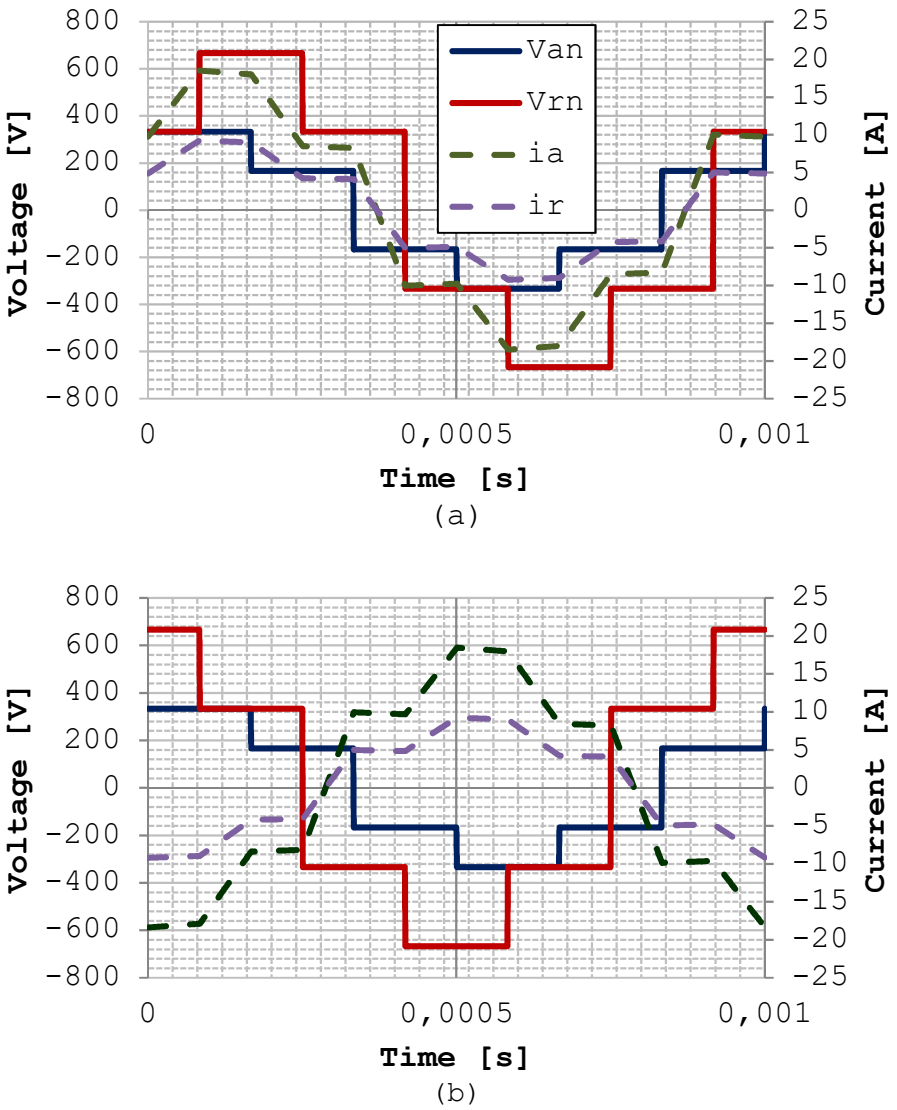


Figure 6. 32 Simulated waveforms at the ac-link terminals of the 3DAB converter (fundamental frequency = 1kHz): (a) positive power flow mode (the power flow is from primary bridge to secondary bridge) and (b) reverse power flow mode (the power flow is from secondary bridge to primary bridge).

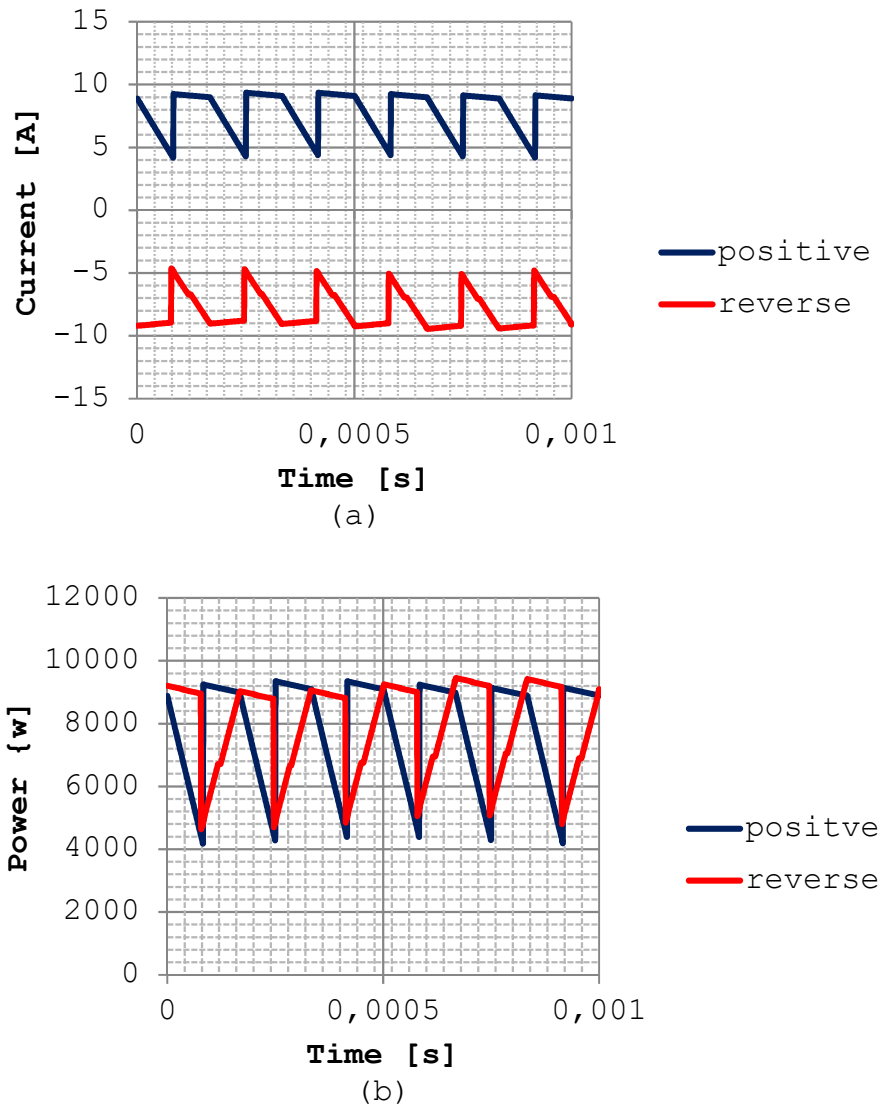


Figure 6. 33 Simulated waveforms illustrating the power flow in the dc link of the 3DAB converter (fundamental frequency = 1kHz: (a) currents in the dc link of secondary bridge at the different power flow modes and (b) transferable powers in the dc link of secondary bridge at the different power flow modes

6.6 Summary

This chapter presented experimental results from the 10-kW scale laboratory prototype as well as simulation results. The experimental results were compared with the simulation results. Ideal IGBT modules and passive components were used in the simulation model implemented with the PLCES software. Based on these results, a snubber capacitor of 10 nF was selected for the primary side bridge; 6.8 nF capacitance for the secondary bridge was found to obtain optimal value for the

corresponding power transfer. The power loss characteristics of the prototype converter obtained with the optimised snubber capacitances were discussed. Consequently, 94.2% efficiency of the converter was reached at the full load amount of 9.5 kW. The maximum efficiency of 94.88% was achieved at 4.8-kW load with the optimised snubber capacitors. Overall, efficiencies above 90% were achieved when the converter operated above 20% of the rated power level. The comparison of results for the measured and the simulated efficiencies showed that the efficiency variation was below 1% for the power levels. Hence, the measured efficiencies match well with the simulated values.

Chapter 7

Conclusion

This work was dedicated to the design and implementation of an isolated 3DAB converter for MVDC applications. A general overview of different DC-DC converters is discussed in the literature but attention is focused on galvanically isolated DC-DC converter. This work presents a step-by-step design for passive components such as three-phase MF transformer and snubber circuit that enable the identification of the optimum design parameters for a 3DAB converter.

Special attention was paid to the effect of low leakage inductance and low phase-shift angle on efficiency and high power density of the transformer design. Also, low leakage inductances resulted in small values of the phase-shift angle. Using small phase-shift angles, these converters can be operated to avoid unnecessary reactive power circulation in the magnetic coupling components. To reduce the current stress and the circulating energy in the magnetic components, the phase-shift angle cannot be set too high in the practical system. Therefore, this low inductance requirement has an important impact on the design optimisation of the magnetic transformer.

However, problems in digital modulation of the digital controller were encountered, which in case of high switching frequencies led to low resolution of the digital modulator. In high switching frequency applications, the low phase-shift angle can be insufficient for achieving the full power flow and relative voltage rate of the system. To control the hardware design for the 3DAB converters in dynamic

operation, a resolution of digital modulator will need to be addressed in further developments. In the developed converters with a switching frequency of 1 kHz, the used phase-shift angle range of below 30° corresponds to a maximum delay of 100 µs of gate signals between the primary and secondary. Therefore, a sufficient resolution scheme in the low delay time will be required to achieve accurate power control.

The main contribution of this work was concluded in Chapter 5, with the design and optimisation of the three-phase MF transformer in 3DAB converter. A novel design and optimising methodology for MF isolated transformers for determining the optimal geometric design parameters and estimating efficiency limits was proposed in this work. The design procedure gives special attention to the isolation layer and leakage inductance reached by this transformer and its influence over geometric design parameters. A combined design structure with a 2D FEA optimisation used low free parameters (only five parameters: $N1$, J_p, J_s, window area ratio, and core sectional area ratio) to eliminate time-consuming calculations. Nevertheless, the combination of the 2D FEA optimisation was found to be very attractive for the verification of important design constraints of the transformer, both internal and external, including winding voltages and currents, core material magnetic saturation, temperature rise, and winding and core losses.

2D FEA simulations and loss calculations were undertaken for two different configurations of the 3DAB converter setup. The outcome showed that the first configuration with a layout for a 1.1 kVDC rated 3DAB converter yielded a peak efficiency of up to 98.95% with a total weight of 412 kg. The second configuration represented a layout for a higher voltage rating, featuring a DC input voltage of 5.2 kVDC and a nominal converter power level of 4 MW. This led to the attractive peak efficiency of 99.0% with a weight of 415 kg.

The proposed optimum design was limited to a core-type transformer. A shell-type transformer can be considered for high-power medium-frequency conversion systems because with the shell-type transformer, it would be easier to produce liquid isolation without convective cooling than with the core-type transformer. A future design modification of the shell-type transformer will be required to verify the

proposed design optimisation performance. Also, future implementations of transformer units for DAB systems based on MMC or 1DAB structure will be a key step in verifying the design methodology of the transformer and identifying additional modification and implementation issues.

Finally, the investigations on the experimental transformer could not be applied to a 4-MW full-scale prototype. In order to verify the system performance, a future implementation of a full-scale system should be considered. A major task would consist of the layout and construction of an insulation system comprising the implementation of an oil-immersed cooling system at medium frequencies and in the 4-MW rating demonstrators.

7.1 Summary of this work

In Chapter 2, an overview of possible future power distribution applications was presented. Interesting application fields can be identified in medium-voltage DC-based power transmission grids and distribution networks, with potential advantages for the urban power networks between a number of renewable energy generation and loads.

A promising application of the multi-megawatt scale DC-DC conversion systems is the efficient electrification of large-scale renewable energy sources for the medium-voltage DC collector access points. With respect to the DC-DC converters, all surveyed DC-DC converter platforms require multi-megawatt and tens of hundreds of kilovolt ratings. Furthermore, successful converter developments may be required to be galvanically isolated from the medium-voltage point to the low-voltage point for safety reasons.

To meet the requirement of multi-megawatt and tens of kilovolt applications, a three-phase dual active bridge DC-DC (3DAB) converter was found to be the most promising topology with respect to high achievable conversion efficiency. Accordingly, the 3DAB converter was investigated in detail.

In Chapter 3, the operating principle of the 3DAB converter was explained with a simplified piecewise linear description of the converter model. Expressions for the RMS values of switch currents, along with peak and RMS currents of the leakage inductance of the transformer were obtained from the model. These mathematical models are useful in predicting power losses and facilitate the study of the converter characteristics. This work aimed to investigate zero-voltage switching (ZVS) converter concepts in a considerable voltage range (up to 40kV DC) and power rating (4 MW). The ZVS operation can be combined with a reduction in *dv/dt* stress during switching action, which contributes significantly to reducing the switching losses of semiconductors.

Chapter 3 investigated the snubber circuit topology for a high-power 3DAB converter that merges the advantages of the ZVS switching scheme. The working of the 3DAB converter equipped with snubber capacitors in parallel to the switching semiconductor devices was investigated. The snubber capacitors are required to achieve the desired reduction in voltage transients during turn-off switching commutation. How their capacitor size can be adjusted to a specified minimum commutation time for each bridge was determined. Employing higher capacitances led to extra power dissipation, owing to longer voltage transients. The snubberless 3DAB circuit showed that the natural ZVS range is restricted to higher power levels. It has therefore been investigated how the ZVS range can be extended with snubber capacitances. The analytical results of the 3DAB converter were verified in conditions of power flowing from the primary into the secondary side and boost mode. The results showed that increasing values of the snubber capacitor have an extending effect on the primary bridge ZVS boundary. The secondary bridge ZVS ranges are limited to higher capacitance values.

Chapter 4 presents the design consideration and optimisation strategy for a three-phase 4 MW/1 kHz transformer in a 3DAB DC-DC converter for a 40-kV MVDC grid. Analytical calculations for the design indicate that the transformer could be designed with over 98.5% efficiency. The main benefits of the design and optimisation methodology are that it can determine the optimal geometric parameters and calculate maximum efficiency during the optimisation and be implemented in high-power conversion applications operated at medium-frequency range.

Furthermore, this methodology contributes to the design of a three-phase high-power transformer operating under non-sinusoidal excitation.

The procedure for optimum design was applied on a core-type transformer designed with a non-oriented silicon steel core. The investigation on the optimisation loop shows efficiency versus volume and the sensibility of degrees of freedom such as the number of turns on the primary winding. Finally, the optimisation was validated by 2D FEA simulation. The measurements show that the measured peak flux density is lower than the expected value. Also, the 2D FEA results of core loss and copper losses in both windings confirm that the core loss is higher than the winding losses since the transformer operates below full-load condition.

A 10-kW prototype transformer on a 1000-V DC supply system at rated power of 10 kW was manufactured in order to evaluate the proposed optimum design procedure. The measurements from experimental validation indicate that the developed transformer with a recorded maximum efficiency of 96.84% can be proposed as a magnetic link component in the 3DAB converter topology.

Chapter 5 introduced the design details for a 10-kW laboratory prototype converter that was constructed to evaluate the design methods of the developed 3DAB converter and the operating characteristics of the converter. The input DC-link voltage was set to 500 V. The turn ratio of the designed transformer was 1:2; hence, the output DC-link voltage was set to 1000 V. Details of the structure of the prototype including the hardware components, passive components, thermal management, digital control units, and control software implementation were introduced. The laboratory converter was controlled from a DSP/FPGA control platform.

Finally, the experimental results validated the operation of the 3DAB converter in Chapter 8. Based on these results, a snubber capacitor of 10 nF was selected for the primary side bridge, whereas 6.8 nF capacitance for the secondary bridge could obtain an optimal value for the corresponding power transfer. The power loss characteristics of the prototype converter obtained with the optimised snubber capacitances were discussed. Consequently, 94.2% efficiency of the converter was reached at the full load amount of 9.5 kW. The maximum efficiency of 94.88% was

achieved at 4.8 kW load with the optimised snubber capacitors. Overall, efficiencies above 90% were achieved when the converter operated above 20% of the rated power level.

7.2 Suggestions for further work

The following aspects may be considered in future research on the high-power 3DAB converter:

- The contribution made by this work could not be applied to a full-scale practical system. Future investigation of a commercial-scale MVDC system will be key to verifying system performance as the number of hardware increases and to identifying possible issues and technical solutions related to the performance of the control method on an installed full-scale converter.
- The proposed design optimisation for MF transformers in a 3DAB converter can be investigated for other high-power high-voltage DC-DC converters based on the MMC structure.
- Asymmetric stray inductance of three-phase large-scale transformers led to unbalanced phase currents. Consequently, it will lead to more current ripple in the DC current on the primary and secondary bridge. It might be necessary to investigate the influence of imbalanced currents and validate a suitable balance control scheme for the asymmetry 3DAB converters on dynamic operation.
- With respect to converter operation, additional research is required to identify the extended soft switching operation of 3DAB converters with imbalanced stray inductances on the three-phase transformer.
- A number of design aspects have been considered for the realisation of high-power transformers that operate at kilohertz frequencies. A major task would be the layout and construction of an insulation system comprising an oil-immersed cooling system at medium frequencies and in the 4-MW rating demonstrators.

  Advanced control schemes for 3DAB converters will be proposed for extension of the ZVS operating range.

Appendix A

Piecewise modelling of 3DAB currents

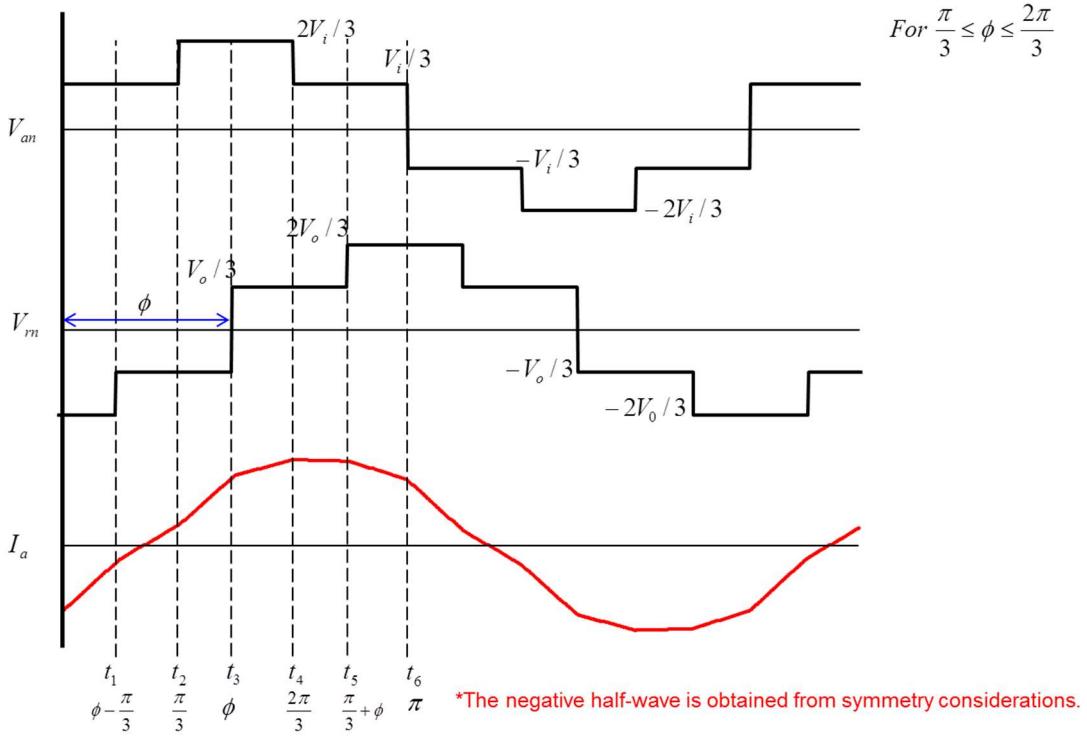


Figure A. 1 Characteristic waveforms in the 3DAB DC-DC Converter

Fig. A.1 illustrates the resulting typical waveforms in the 3DAB converter for the case of the magnitude of V_{rn} is higher than that of V_{an}. For the depicted case of $\varphi \geq \pi/3$, the leakage inductance current at the transformer introduced by a six-step voltage at the transformer terminals. The terminal voltage on the transformer is the difference between the V_{an} and V_{rn}. For each time interval, the voltages are constants. The leakage inductance current can be expressed as:

$$i(\omega t) = i(\omega t_0) + \frac{V_{an} - V_{rn}}{\omega_{sw} L_\sigma}(\omega t - \omega t_0) \tag{A.1}$$

Solving (A.1) for $i(\theta)$ for each time intervals and over a half period 0 to π.

Mode 1: $\frac{\pi}{3} \leq \varphi \leq \frac{\pi}{2}$

When $0 \leq \theta \leq \varphi - \frac{\pi}{3}$:

$$i_1(\theta) = i(0) + \frac{\frac{V_{in}}{3} + \frac{2V_{in}}{3}d}{\omega_{sw} L_\sigma}(\theta - 0) = i(0) + \frac{V_{in}(1+2d)}{3\omega_{sw} L_\sigma}\theta \tag{A.2}$$

When $\varphi - \frac{\pi}{3} \leq \theta \leq \frac{\pi}{3}$:

$$i_2(\theta) = i(\varphi - \frac{\pi}{3}) + \frac{\frac{V_{in}}{3} + \frac{V_{in}}{3}d}{\omega_{sw} L_\sigma}(\theta - \varphi + \frac{\pi}{3}) = i(\varphi - \frac{\pi}{3}) + \frac{V_{in}(1+d)}{3\omega_{sw} L_\sigma}(\theta - \varphi + \frac{\pi}{3}) \tag{A.3}$$

When $\frac{\pi}{3} \leq \theta \leq \varphi$:

$$i_3(\theta) = i(\frac{\pi}{3}) + \frac{\frac{2V_{in}}{3} + \frac{V_{in}}{3}d}{\omega_{sw} L_\sigma}(\theta - \frac{\pi}{3}) = i(\frac{\pi}{3}) + \frac{V_{in}(2+d)}{3\omega_{sw} L_\sigma}(\theta - \frac{\pi}{3}) \tag{A.4}$$

When $\varphi \le \theta \le \frac{2\pi}{3}$:

$$i_4(\theta) = i(\varphi) + \frac{\frac{2V_{in}}{3} - \frac{V_{in}}{3}d}{\omega_{sw}L_\sigma}(\theta - \varphi) = i(\varphi) + \frac{V_{in}(2-d)}{3\omega_{sw}L_\sigma}(\theta - \varphi) \tag{A.5}$$

When $\frac{2\pi}{3} \le \theta \le \frac{\pi}{3} + \varphi$:

$$i_5(\theta) = i(\frac{2\pi}{3}) + \frac{\frac{V_{in}}{3} - \frac{V_{in}}{3}d}{\omega_{sw}L_\sigma}(\theta - \frac{2\pi}{3}) = i(\frac{2\pi}{3}) + \frac{V_{in}(1-d)}{3\omega_{sw}L_\sigma}(\theta - \frac{2\pi}{3}) \tag{A.6}$$

When $\frac{\pi}{3} + \varphi \le \theta \le \pi$:

$$i_6(\theta) = i(\frac{\pi}{3} + \varphi) + \frac{\frac{V_{in}}{3} - \frac{2V_{in}}{3}d}{\omega_{sw}L_\sigma}(\theta - \frac{\pi}{3} - \varphi) = i(\frac{\pi}{3} + \varphi) + \frac{V_{in}(1-2d)}{3\omega_{sw}L_\sigma}(\theta - \frac{\pi}{3} - \varphi) \tag{A.7}$$

$i(\pi)$ is calculated by:

$$\begin{aligned} i(\pi) &= i_{a1}(\theta) + i_{a2}(\theta) + i_{a3}(\theta) + i_{a4}(\theta) + i_{a5}(\theta) + i_{a6}(\theta) + i_{a7}(\theta) \\ &= \frac{V_{in}}{3\omega_{sw}L_\sigma}\left[-d\pi + 2d\varphi + \frac{2}{3}\pi \right] \end{aligned} \tag{A.8}$$

Equating $i(0) = -i(\pi)$ and solving for $i(0)$:

$$i(0) = \frac{V_{in}}{3\omega_{sw}L_\sigma}\left[d\pi - 2d\varphi - \frac{2}{3}\pi \right] \tag{A.9}$$

With $i(0)$, the average output power can be calculated as:

$$P_o = \frac{{V_{in}}^2}{\omega_{sw} L_\sigma} d\left[\varphi - \frac{\varphi^2}{\pi} - \frac{\pi}{18}\right] \tag{A.10}$$

For $0 \le \varphi \le \pi/3$, a similar set of equations can be derived. The average output power can be calculated as:

$$P_o = \frac{V_{in}^2}{\omega_{sw} L_\sigma} \cdot d \cdot \varphi\left[\frac{2}{3} - \frac{\varphi}{2\pi}\right] \quad \text{for } \left(0 \le \varphi \le \pi/3\right) \tag{A.11}$$

The base power can be calculated by

$$P_{base} = \frac{V_{in}^2}{\omega_{sw} L_\sigma} \tag{A.12}$$

To sum up, the leakage inductance currents of primary $i(0)$ and secondary $i(\varphi)$ can be calculated by

$$\begin{aligned} i(0) &= \frac{V_{in}}{3\omega_{sw} L_\sigma}\left[\frac{2}{3}\pi d - d\varphi - \frac{2}{3}\pi\right] && \text{for } \left(0 \le \varphi \le \pi/3\right) \\ i(0) &= \frac{V_{in}}{3\omega_{sw} L_\sigma}\left[\pi d - 2d\varphi - \frac{2}{3}\pi\right] && \text{for } \left(\pi/3 \le \varphi \le 2\pi/3\right) \end{aligned} \tag{A.13}$$

$$\begin{aligned} i(\phi) &= \frac{V_{in}}{3\omega_{sw} L_\sigma}\left[\frac{2}{3}\pi d + \varphi - \frac{2}{3}\pi\right] && \text{for } \left(0 \le \varphi \le \pi/3\right) \\ i(\phi) &= \frac{V_{in}}{3\omega_{sw} L_\sigma}\left[\frac{2}{3}\pi d + 2\varphi - \pi\right] && \text{for } \left(\pi/3 \le \varphi \le 2\pi/3\right) \end{aligned} \tag{A.14}$$

Appendix B

Calculation of phase shift angle

The power transfer characteristics of the 3DAB converter are explained in chapter 3. For the case of a small phase shift angle ($\varphi \le \pi/3$), the transformer current harmonics introduced by the six-step operation are clearly visible. In this appendix, a maximum phase shift angle requirement of $\varphi \le \pi/3$ is considered because larger values of φ will lead to increased turn-off current. From (3.6), the average output power can be calculated as:

$$P_o = \frac{V_{pri}^2}{\omega_{sw} L_\sigma} \cdot d \cdot \varphi \left[\frac{2}{3} - \frac{\varphi}{2\pi} \right] \quad \text{for} \left(0 \le \varphi \le \pi/3 \right) \tag{B.1}$$

When the voltage is increased, the control phase angle φ needs to be reduced to keep the output power constant to Eq (B.1). The control angle, φ, can be calculated in terms of converter operating parameters from (B.1). Eq (B.1) can be solved using a quadratic equation as follows:

$$\begin{aligned} \varphi\left[\frac{2}{3}-\frac{\varphi}{2\pi}\right] &= \frac{P_o \cdot \omega_{sw} \cdot L_\sigma}{V_{pri}^2 \cdot d} \\ -\frac{1}{2\pi}\varphi^2 + \frac{2}{3}\varphi - \frac{P_o \cdot \omega_{sw} \cdot L_\sigma}{V_{pri}^2 \cdot d} &= 0 \end{aligned} \tag{B.2}$$

Where, $a = -\frac{1}{2\pi}, b = \frac{2}{3}, c = -\frac{P_o \cdot \omega_{sw} \cdot L_\sigma}{V_{pri}^2 \cdot d}$.

The quadratic equation can be solved using the quadratic formula as:

$$\begin{aligned} ax^2 + bx + c &= 0 \\ x &= \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \end{aligned} \tag{B.3}$$

Using the quadratic formula as expressed in (B.3), solve Eq(B.2), for $\varphi$by using the completing the square method:

$$\begin{aligned} \varphi &= \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \\ \varphi &= \frac{-\frac{2}{3} \pm \sqrt{\left(\frac{2}{3}\right)^2 - 4 \cdot \left(-\frac{1}{2\pi}\right) \cdot \left(-\frac{P_o \cdot \omega_{sw} \cdot L_\sigma}{V_{pri}^2 \cdot d}\right)}}{2 \cdot \left(-\frac{1}{2\pi}\right)} \\ \varphi &= \frac{2}{3}\pi - \sqrt{\left(\frac{2}{3}\pi\right)^2 - 2\pi \cdot \left(-\frac{P_o \cdot \omega_{sw} \cdot L_\sigma}{V_{pri}^2 \cdot d}\right)} \end{aligned} \tag{B.4}$$

Where, $d = n \cdot \frac{V_{\text{sec}}}{V_{pri}} = \frac{w_{pri}}{w_{\text{sec}}} \cdot \frac{V_{\text{sec}}}{V_{pri}}$ is dc conversion ratio. w_{pri} is the number of turns in the primary winding and w_{sec} is the number of turns in the secondary winding.

Appendix C

Analytical Modelling of conducting RMS currents

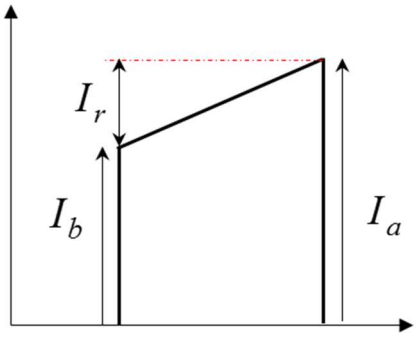


Figure C. 1 Trapezoidal waveform

Trapezoidal current waveforms are commonly found in diodes and active semiconductors, hence we can calculate average value and RMS value of current using the trapezoidal method [2].

$$I_{ave} = \frac{1}{T}\int_0^T I(t)dt = \frac{t}{T}\left(I_a - \frac{I_r}{2}\right) \tag{C.1}$$

$$I_{rms}=\sqrt{\frac{1}{T}\int_0^T I^2(t)dt}=\sqrt{\frac{t}{T_s}\left[I_a^2+\frac{I_r^2}{3}-I_aI_r\right]} \tag{C.2}$$

Where, $I_r=I_a-I_b$

C.1 RMS currents of primary side bridge

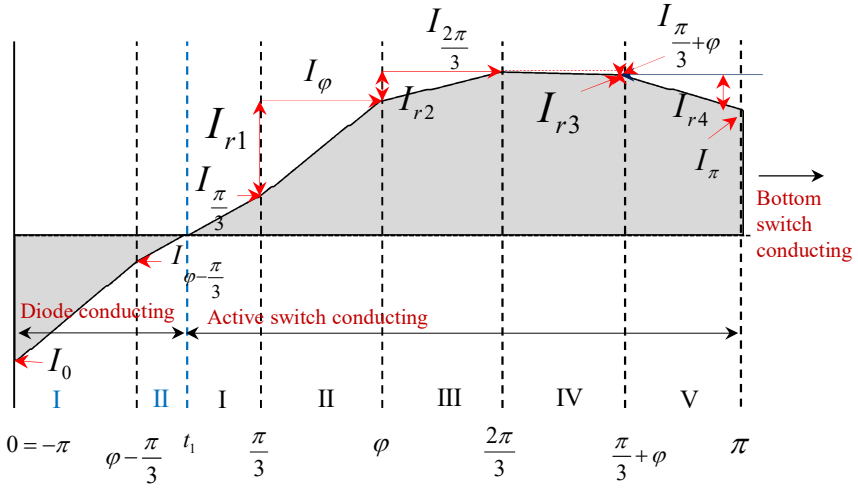


Figure C. 2 Waveform of conducting current of the primary side bridge

C.1.1 RMS value of diode current

According to Fig. C.2, the conducting current of the diode can be expressed by two steps.

- For time interval , I

The magnitude of $i(0)$ is calculated as

$$I_0=I_a(0)=\frac{V_{pri}}{3\omega_{sw}L_\sigma}\left[d\pi-2d\varphi-\frac{2}{3}\pi\right] \tag{C.3}$$

The magnitude of the current at $\theta=\varphi-\pi/3$ is calculated as

$$I_{\varphi-\frac{\pi}{3}} = I_0 + \frac{V_{pri}(1+2d)}{3\omega_{sw}L_\sigma}(\varphi-\frac{\pi}{3}) = \frac{V_{pri}}{3\omega_{sw}L_\sigma}\left[d\pi - 2d\varphi - \frac{5}{3}\pi + 3\varphi\right] \quad \text{(C.4)}$$

The total current change during the interval I, where the current is increased from $\theta = 0(-\pi)$ to $\theta=\varphi-\pi/3$, can be written as follows

$$I_{d_r} = I_0 - I_{\varphi-\frac{\pi}{3}} \quad \text{(C.5)}$$

- For time interval , II

The maximum magnitude of the current is at $\theta=\varphi-\pi/3$ and the minimum magnitude is zero hence, the RMS value for the time interval can be calculated as

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^{t_1-(\varphi-\frac{\pi}{3})} i^2(\varphi-\frac{\pi}{3})t^2dt} = \sqrt{\frac{t_1-(\varphi-\frac{\pi}{3})}{T_s}\left[\frac{I^2_{\varphi-\frac{\pi}{3}}}{3}\right]} \quad \text{(C.6)}$$

Where, t_1 is time to diode conducting current is to zero and active switch starts to conducting, Assuming half interval between $\frac{\pi}{3}$ and $\varphi-\frac{\pi}{3}$ for the transfer of current from diode to active switch device , total RMS value of the diode current can be calculated by

$$\begin{aligned} I_{d_rms_\text{pri}} &= \sqrt{\frac{1}{T_s}\int_0^{\varphi-\frac{\pi}{3}} I^2(t)dt + \frac{1}{T_s}\int_0^{t_1-(\varphi-\frac{\pi}{3})} I^2(t)dt} \\ &= \sqrt{\frac{\varphi-\frac{\pi}{3}}{T_s}\left[I_0^2 + \frac{I_{d_r}^2}{3} - I_0\cdot I_{d_r}\right] + \frac{t_1-(\varphi-\frac{\pi}{3})}{T_s}\cdot\frac{I^2_{\varphi-\frac{\pi}{3}}}{3}} \end{aligned} \quad \text{(C.7)}$$

C.1.2 RMS value of active semiconductor current

On the other hand, the conducting current of the active device can be expressed by five steps as shown in Fig. C.2. For each five time intervals, the RMS value can be calculated below as:

- For time interval , I

The instantaneous current at $\theta = \pi/3$ is represented as follows

$$I_{\frac{\pi}{3}} = I_{\varphi-\frac{\pi}{3}} + \frac{V_{pri}(1+d)}{3\omega_{sw}L_{\sigma}}(\theta - \varphi + \frac{\pi}{3}) = \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[\frac{5d}{3}\pi - \pi + 2\varphi - 3d\varphi\right] \quad \text{(C.8)}$$

Therefore, solving for the RMS equation based on the current slope during the interval gives

$$I_{rms_\mathrm{I}} = \sqrt{\frac{\frac{\pi}{3} - t_1}{T_s}\left[\frac{I_{\frac{\pi}{3}}^2}{3}\right]} \quad \text{(C.9)}$$

- For time interval , II

The instantaneous current at $\theta = \varphi$ is represented as follows

$$I_{\phi} = I_{\frac{\pi}{3}} + \frac{V_{pri}(2+d)}{3\omega_{sw}L_{\sigma}}(\theta - \frac{\pi}{3}) = \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[\frac{4}{3}d\pi - \frac{5}{3}\pi + 4\varphi - 2d\varphi\right] \quad \text{(C.10)}$$

Solving for the RMS equation based on the current slope during the interval gives

$$I_{rms_\mathrm{II}} = \sqrt{\frac{\varphi - \frac{\pi}{3}}{T_s}\left[I_{\varphi}^2 + \frac{I_{r_\mathrm{II}}^2}{3} - I_{\varphi}\cdot I_{r_\mathrm{II}}\right]} \qquad \text{Where, } I_{r_\mathrm{II}} = I_{\varphi} - I_{\frac{\pi}{3}} \quad \text{(C.11)}$$

- For time interval , III

$$I_{\frac{2\pi}{3}} = I_{\varphi} + \frac{V_{pri}(2-d)}{3\omega_{sw}L_{\sigma}}(\theta-\varphi) = \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[\frac{2}{3}d\pi - \frac{\pi}{3} + 2\varphi - d\varphi\right] \quad \text{(C.12)}$$

$$I_{rms_\mathrm{III}} = \sqrt{\frac{\left(\frac{2\pi}{3}-\varphi\right)}{T_s}\left[I_{\frac{2\pi}{3}}^2 + \frac{I_{r_\mathrm{III}}^2}{3} - I_{\frac{2\pi}{3}}\cdot I_{r_\mathrm{III}}\right]} \qquad \text{Where, } I_{r_\mathrm{III}} = I_{\frac{2\pi}{3}} - I_{\varphi} \quad \text{(C.13)}$$

- For time interval , IV

$$I_{\frac{\pi}{3}+\varphi} = I_{\frac{2\pi}{3}} + \frac{V_{pri}(1-d)}{3\omega_{sw}L_{\sigma}}(\theta-\frac{2\pi}{3}) = \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[d\pi - \frac{2}{3}\pi + 3\varphi - 2d\varphi\right] \quad \text{(C.14)}$$

$$I_{rms_\mathrm{IV}} = \sqrt{\frac{\left(\phi-\frac{\pi}{3}\right)}{T_s}\left[I_{\frac{2\pi}{3}}^2 + \frac{I_{r_\mathrm{IV}}^2}{3} - I_{\frac{2\pi}{3}}\cdot I_{r_\mathrm{IV}}\right]} \qquad \text{Where, } I_{r_\mathrm{IV}} = I_{\frac{2\pi}{3}} - I_{\frac{\pi}{3}+\phi} \quad \text{(C.15)}$$

- For time interval , V

$$I_{\pi} = I_{\frac{\pi}{3}+\varphi} + \frac{V_{pri}(1-2d)}{3\omega_{sw}L_{\sigma}}(\theta-\frac{\pi}{3}-\varphi) = \frac{V_{pri}}{3\omega_{sw}L_{\sigma}}\left[-d\pi + 2d\varphi + \frac{2}{3}\pi\right] \quad \text{(C.16)}$$

$$I_{rms_\mathrm{V}} = \sqrt{\frac{\left(\frac{2\pi}{3}-\varphi\right)}{T_s}\left[I_{\frac{\pi}{3}+\varphi}^2 + \frac{I_{r_\mathrm{V}}^2}{3} - I_{\frac{\pi}{3}+\varphi}\cdot I_{r_\mathrm{V}}\right]}$$

$$\text{Where, } I_{r_\mathrm{V}} = I_{\frac{\pi}{3}+\varphi} - I_{\pi} \quad \text{(C.17)}$$

Hence, total RMS value of the active semiconductor is calculated by

$$I_{Q_rms_\mathrm{pri}}=\sqrt{\frac{1}{T_s}\left[\begin{array}{l}\left(\frac{\pi}{3}-t_1\right)\cdot\left(\frac{I_{\frac{\pi}{3}}^2}{3}\right)+\left(\varphi-\frac{\pi}{3}\right)\cdot\left(I_\varphi^2+\frac{I_{r_1}^2}{3}-I_\varphi\cdot I_{r_1}\right)+\left(\frac{2\pi}{3}-\varphi\right)\cdot\left(I_{\frac{2\pi}{3}}^2+\frac{I_{r_2}^2}{3}-I_{\frac{2\pi}{3}}\cdot I_{r_2}\right)\\+\left(\varphi-\frac{\pi}{3}\right)\cdot\left(I_{\frac{2\pi}{3}}^2+\frac{I_{r_3}^2}{3}-I_{\frac{2\pi}{3}}\cdot I_{r_3}\right)+\left(\frac{2\pi}{3}-\varphi\right)\cdot\left(I_{\frac{\pi}{3}+\varphi}^2+\frac{I_{r_4}^2}{3}-I_{\frac{\pi}{3}+\varphi}\cdot I_{r_4}\right)\end{array}\right]}$$

Where, $I_{r_1}=I_\varphi-I_{\frac{\pi}{3}}$, $I_{r_2}=I_{\frac{2\pi}{3}}-I_\varphi$, $I_{r_3}=I_{\frac{2\pi}{3}}-I_{\frac{\pi}{3}+\varphi}$, and $I_{r_4}=I_{\frac{\pi}{3}+\varphi}-I_\pi$

(C.18)

C.2 RMS currents of secondary side bridge

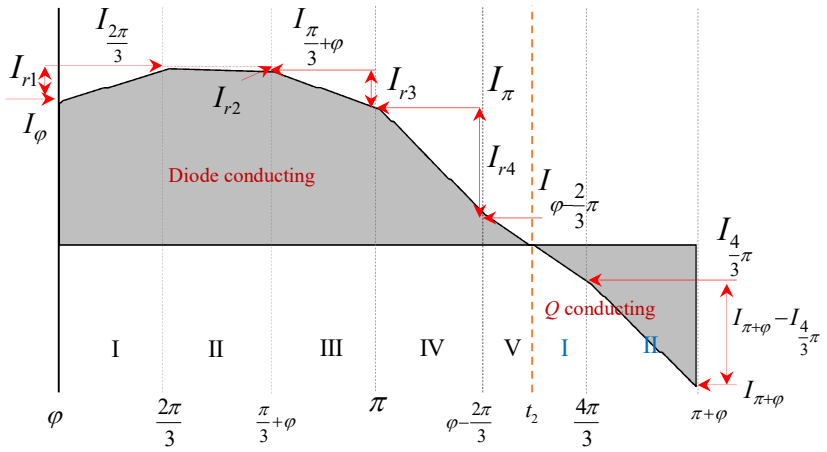


Figure C. 3 Waveform of conducting current of the secondary side bridge

Similarly, the RMS currents of secondary side bridge can be calculated. RMS value of the active semiconductor diode current is calculated as

$$I_{Q_rms_\mathrm{sec}}=\sqrt{\frac{\left(\frac{4\pi}{3}-t_2\right)}{T_s}\cdot\frac{I_{\frac{4\pi}{3}}^2}{3}+\frac{\varphi-\frac{\pi}{3}}{T_s}\left[I_{\pi+\varphi}^2+\frac{\left(I_{\pi+\varphi}-I_{\frac{4}{3}\pi}\right)^2}{3}-I_{\pi+\varphi}\cdot\left(I_{\pi+\varphi}-I_{\frac{4}{3}\pi}\right)\right]}$$

(C.19)

RMS value of the diode current is calculated as

$$I_{d_rms_\sec}=\sqrt{\frac{1}{T_s}\left[\begin{array}{l}\left(\frac{2\pi}{3}-\varphi\right)\cdot\left(I^2_{\frac{2\pi}{3}}+\frac{I^2_{r_1}}{3}-I_{\frac{2\pi}{3}}\cdot I_{r_1}\right)+\left(\varphi-\frac{\pi}{3}\right)\cdot\left(I^2_{\frac{2\pi}{3}}+\frac{I^2_{r_2}}{3}-I_{\frac{2\pi}{3}}\cdot I_{r_2}\right)\\ +\left(\frac{2\pi}{3}-\varphi\right)\cdot\left(I^2_{\frac{\pi}{3}+\varphi}+\frac{I^2_{r_3}}{3}-I_{\frac{\pi}{3}+\varphi}\cdot I_{r_3}\right)+\left(\varphi-\frac{5\pi}{3}\right)\cdot\left(I^2_{\pi}+\frac{I^2_{r_4}}{3}-I_{\pi}\cdot I_{r_4}\right)+\left(\frac{4\pi}{3}-t_2\right)\cdot\left(\frac{I^2_{\varphi-\frac{2\pi}{3}}}{3}\right)\end{array}\right]}$$

Where, $I_{r_1}=I_{\frac{2}{3}\pi}-I_{\varphi}$, $I_{r_2}=I_{\frac{2\pi}{3}}-I_{\frac{\pi}{3}+\varphi}$, $I_{r_3}=I_{\frac{\pi}{3}+\varphi}-I_{\pi}$, and $I_{r_4}=I_{\pi}-I_{\varphi-\frac{2}{3}\pi}$

(C.20)

Fig. C.4 shows calculated and simulated RMS currents of primary side semiconductor devices. For the simulation verification, a detailed circuit simulation is conducted using PLECS. In the simulation model, the primary dc-link voltage is 5.2kV DC and the secondary bridge is connected a 40kV resistive load. Comparing the diagram, the differences between simulated and calculated losses are likely due to the effect of resistive load, winding resistance, etc on the simulation model. However, the trend in the simulation curve of the RMS currents is seen to closely match that of the theoretical analysis.

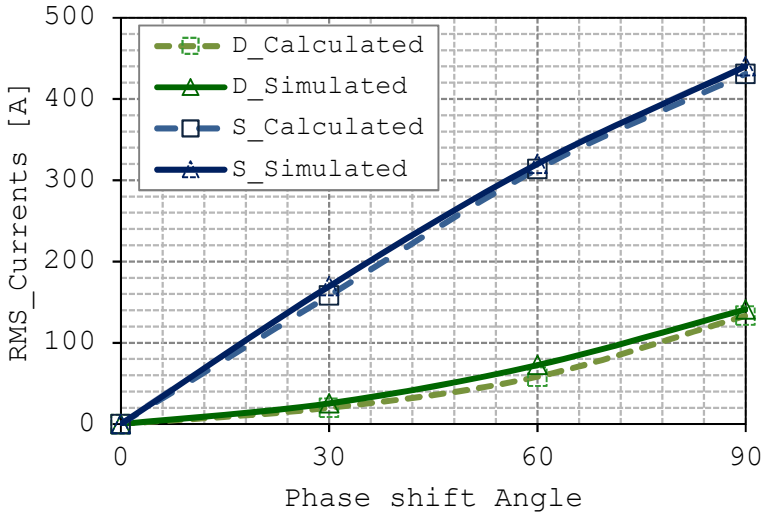


Figure C. 4 Primary side RMS currents versus φ , with d as parameter

Appendix D

Mathematical expression of capacitive commutations

A description method for the capacitive commutation process is derived. The simplified equivalent circuit of the commutation process with a fixed dead time is shown in Fig. D.1. A derivation of analytical expression for the commutation of 3DAB converters for single phase shift operation can be found in [**ref**]. The following derivation aims to describe a more general commutation process allowing for different commutation voltages and a fixed dead time influence.

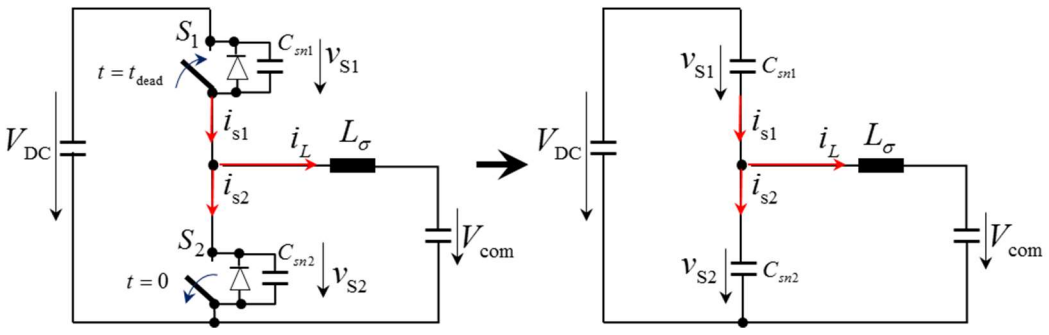


Figure D. 1 Simplified circuit for capacitive commutation process of a half bridge circuit

Firstly, a fixed capacitance is assumed:

$$C_{sn1} = C_{sn2} = C_{sn} = \text{const} \tag{D.1}$$

Using the diagram, the associated resonant characteristics are calculated as

$$\omega_r = \frac{1}{\sqrt{L_\sigma \cdot 2C_{sn}}} \tag{D.2}$$

$$Z_r = L_\sigma \cdot \omega_r = \sqrt{\frac{L_\sigma}{2C_{sn}}} \tag{D.3}$$

where, ω_r is resonant frequency and Z_r is resonant impedance. For the switching transition from S_2 to S_1, the current $i_{s2}>0$ for t<0. After the dead time ($t=t_{dead}$), the S_1 is turned on. The equation for v_{s2} is:

$$v_{s2}(t) + \frac{1}{\omega_r} \cdot \frac{d^2 v_{s2}(t)}{dt^2} + V_{com} = 0 \tag{D.4}$$

Solve for $v_{s2}=0$ and $i_L(0)= I_0$ is:

$$v_{s2}(t) = -I_0 Z_r \cdot \sin(\omega_r t) - V_{com} \cdot \cos(\omega_r t) + V_{com} \tag{D.5}$$

Solving trigonometric equation of the following equation :

$$a\sin(\alpha) + b\cos(\beta) = \sqrt{a^2 + b^2} \cdot \sin\left[\alpha + \arctan\left(\frac{b}{a}\right)\right] \qquad \text{for } a > 0 \tag{D.6}$$

The expression of Eq. D.5 can be solved by:

$$v_{s2}(t) = V_{com} + \sqrt{(I_0 Z_r)^2 + V_{com}{}^2} \cdot \sin\left(\omega_r t + \arctan\left(\frac{V_{com}}{I_0 Z_r}\right)\right) \tag{D.7}$$

The maximum of the resonance is:

$$\omega_r t + \arctan\left(\frac{V_{com}}{I_0 Z_r}\right) = \frac{\pi}{2} \tag{D.8}$$

The inductor current is given by:

$$i_L(t) = I_0 \cdot \cos(\omega_r t) - \frac{V_{com}}{Z_r} \cdot \sin(\omega_r t) \tag{D.9}$$

The minimum offset current $I_{0_min,}$ which is required to charge the capacitors to the V_{DC} at the maximum of the resonance can be calculated using (D.7) and (D.8):

$$\begin{aligned} V_{DC} &= V_{com} + \sqrt{(I_{0_min} \cdot Z_r)^2 + V_{com}{}^2} \\ I_{0_min} &= -\frac{\sqrt{V^2{}_{DC} - 2V_{DC} \cdot V_{com}}}{Z_r} \qquad \text{for } V_{com} < \frac{V_{DC}}{2} \end{aligned} \tag{D.9}$$

Using higher voltages ($V_{com} \geq \frac{V_{DC}}{2}$) and I_0=0, the charge voltage is reached at the V_{DC} before the maximum of the resonance. Again, solving (D.7) for commutation time:

$$t_{\text{com}} = \frac{1}{\omega_r} \cdot \left[\arcsin\left(\frac{V_{\text{DC}} - V_{\text{com}}}{\sqrt{\left(I_0 \cdot Z_r\right)^2 + {V_{\text{com}}}^2}} \right) - \arctan\left(\frac{V_{\text{com}}}{Z_r \cdot I_0} \right) \right] \tag{D.10}$$

For a fixed dead time, the condition for a successful soft commutation is $t_{\text{dead}} > t_{\text{com}}$, i.e., that the switch voltage has to be reached at the V_{DC} within t_{dead}. Solving (D.5) for the initial current I_0 after the dead time (t_{dead}):

$$\begin{aligned} V_{\text{DC}} &= V_{\text{com}} + \sqrt{\left(I_{0_\min} \cdot Z_r\right)^2 + {V_{\text{com}}}^2} \\ I_0 &= -\frac{V_{\text{DC}} + V_{\text{com}} \cdot \left[\cos\left(\omega_r t_{\text{dead}}\right) - 1\right]}{Z_r \cdot \sin\left(\omega_r t_{\text{dead}}\right)} \qquad \text{for } t_{\text{dead}} < \frac{\pi/2 - \arctan\left(\frac{V_{\text{com}}}{I_0 \cdot Z_r} \right)}{\omega_r} \end{aligned} \tag{D.11}$$

Appendix E

Design of Heat sink

E.1 Design of Heat sink

Thermal management is an essential aspect of power electronics systems and is becoming more critical as demands for compact packaging and high power density increase. Thermal performance of power semiconductors in its conjunction to the thermal properties of the cooling system must be known in order to provide a suitable cooling system for each particular application. For selecting a suitable IGBT module for the 3DAB Converter, it is essential to define specific thermal characteristics of the IGBT module for the heat sink design. Main issues for the specification of thermal characteristics of IGBT module are:

- Module packaging technologies with/without baseplate and with integrated heat sink
- Manufacturer specific and references of measuring points for temperatures.
- Specification thermal resistances per module or per switch including measuring conditions and modelling
- Identify thermal resistances with or without thermal coupling between switches
- Thermal conductivity and thickness of thermal interface material between IGBT module and heat sink

In this section, specification method for thermal characteristics of power semiconductor is described. It outlines the modelling method for thermal resistance (R_{th}) of the power semiconductors. In this section, a detailed overview of the physical principles of heat transfer is given.

E.2 Thermal resistance specification and modelling

For the 3DAB converter prototype, two aluminium heat sinks are used. One heat sink for the IGBT modules of the primary bridge and another heat sink for the IGBT modules of the secondary bridge converter is used. The heat conduction of the semiconductors of the primary bridge can be simulated as an electric circuit as shown in Fig. E.1. The thermal model shown in Fig. E.1 is the same for the secondary bridge heat sink. The important parameter to define in this section is the thermal resistance of the heat sink - ambient ($R_{th(s-a)}$).

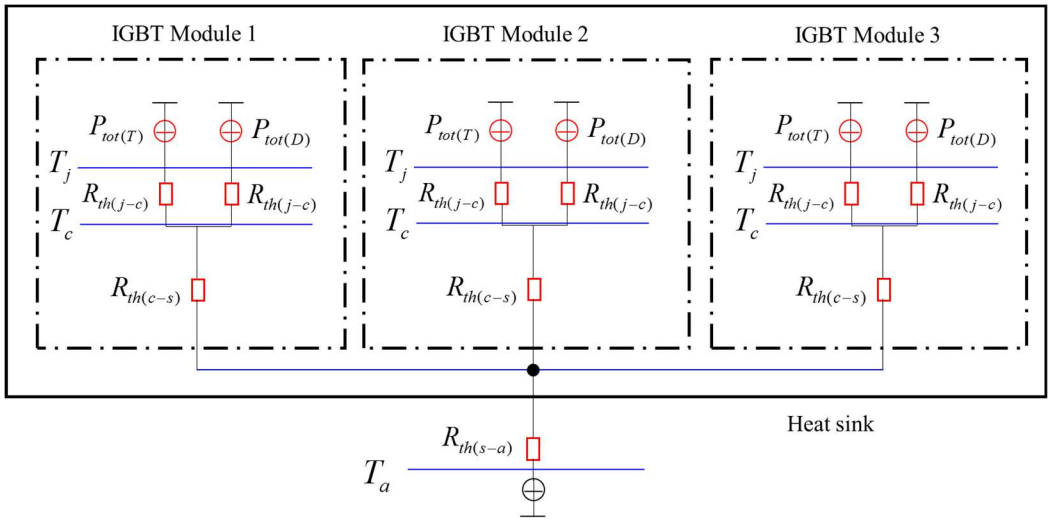


Figure E. 1 Thermal model for heat sink for the 3DAB Converter

Using the equivalent circuit, the heat sink, case, and junction temperature can be calculated using the following thermal equation. By considering the power losses of each IGBT and diode, the dissipated power in the thermal resistances is known. Heat sink temperature:

$$T_s = \left(P_{tot\,(T)} + P_{tot\,(D)}\right) \cdot R_{th\,(s-a)} + T_a \tag{E.1}$$

Case Temperature:

$$T_c = \left(P_{tot\,(T)} + P_{tot\,(D)}\right) \cdot R_{th\,(c-s)} + T_s \tag{E.2}$$

Junction Temperature:

$$T_{j(T)} = P_{tot\,(T)} \cdot R_{th\,(c-s)} + T_c \tag{E.3}$$

where, $R_{th(j-c)}$ is junction- case, $R_{th(c-s)}$ is case-heat sink, and $R_{th(s-a)}$ is heat sink-ambient thermal resistance. The calculated junction temperature $T_{j(T)}$ of the IGBT module should not exceed the maximum value for given $T_{j(T)}$ from the manufacturer. It needs to be taken into calculation consideration of power loss sources in the modules and on the heat sink as following equations.

$$T_c = n_2 \cdot \left(P_{tot\,(T)} + P_{tot\,(D)}\right) \cdot R_{th(c-s)} + T_s \tag{E.4}$$

$$T_s = n_1 \cdot \left(P_{tot\,(T)} + P_{tot\,(D)}\right) \cdot R_{th\,(s-a)} + T_a \tag{E.5}$$

where, n1 is all components of power loss on the heatsink. For example, amounts of IGBT modules on the heatsink. n_2 is all components of power loss in the module.

E.3 Semiconductor conduction loss

The conduction loss of a semiconductor device can be determined by applying the operating condition to the equations derived from the steady-state model of the device. For instance, Fig. E.2 shows the variation of conduction losses of the

semiconductor devices on primary side bridge for different values of φ. Firstly, the diode conducts negative current and then the active switch conducts positive currents. The conduction losses increase with an increase in the phase shift angle, which results in an increase in instantaneous inductor current.

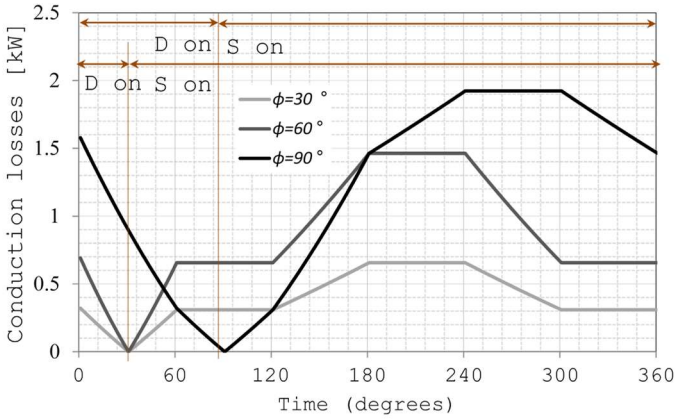


Figure E. 2 Instantaneous conduction losses of primary side bridge for steady-state condition

The instantaneous conduction loss for an IGCT can be calculated from

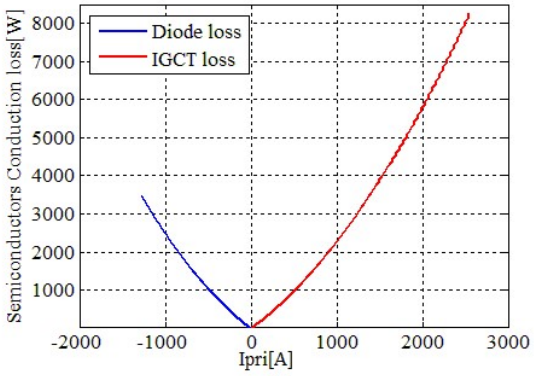
$$P_{con_igct}(t) = v_T \cdot i_T(t) = v_{T0} \cdot i_T(t) + r_T \cdot i_T^2(t) \tag{E.6}$$

The instantaneous conduction loss of the diode can be calculated from

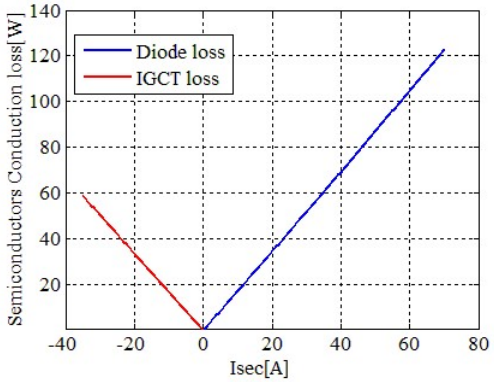
$$P_{con_d}(t) = v_F \cdot i_F(t) = v_{D0} \cdot i_F(t) + r_T \cdot i_F^2(t) \tag{E.7}$$

where, v_T and v_F are the calculated on-state voltages of IGCT and diode respectively. Threshold voltages $v_{T0} = 1.66V$ for the IGCT, $v_{D0} = 1.70V$ for the diode and slope resistances $r_T = 0.620\ m\Omega$ for IGCT, $r_T = 0.80\ m\Omega$ for diode are obtained from the datasheets. Fig. E.3 shows the instantaneous conduction loss curve

for semiconductor devices on the primary side bridge of a 3DAB converter which is transferring 4MVA of power with an input (LV) voltage of 1.1 kV and a nominal output (HV) voltage of 40 kV. At this operating condition, *d* is assumed to be 1 and $\varphi = \pi/3$ is applied.



(a)



(b)

Figure E. 3 Instantaneous conduction loss versus (a): primary side switched current and (b): secondary side switched current

The conduction loss is determined by applying the operating condition to the equations derived from the steady-state model of the inductor current. Average conduction losses can be calculated from

$$P_{avg_con_igct}(t) = \frac{1}{T_{sw}} \int_0^{T_{sw}} (v_{T0} \cdot i_c(t) + r_T \cdot i_c^2(t))dt = v_{T0} \cdot I_{avg_igct} + r_T \cdot I_{rms_igct}^2 \quad \text{(E.8)}$$

$$P_{avg_con_diode}(t) = \frac{1}{T_{sw}} \int_0^{T_{sw}} (v_{D0} \cdot i_D(t) + r_T \cdot i_D^2(t))dt$$
$$= v_{D0} \cdot I_{avg_diode} + r_T \cdot I^2_{rms_diode} \quad \text{(E.9)}$$

where, v_{T0} and v_{D0} are the threshold voltages of the IGCT/IGBT and diode respectively. Calculated and simulated conduction losses versus operation currents are given in Fig. E.4. Comparing the lines on the diagram, one can conclude that the differences between simulated and calculated losses are likely due to the effect of the resistive load and winding resistance on the simulation model.

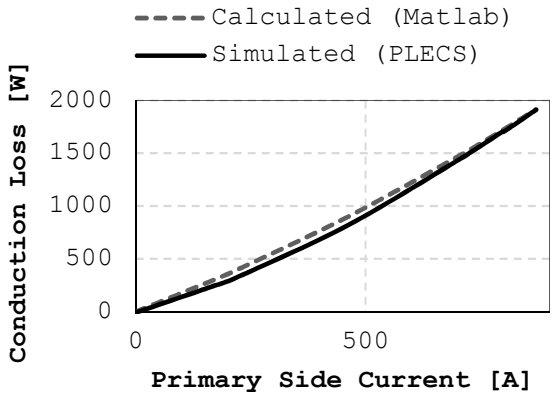


Figure E. 4 Comparison of calculated and simulated power losses of primary side IGCTs

E.4 Semiconductor switching loss

During the switching process of the semiconductor, a significant amount of the stored energy may be dissipated in the switch. This switching loss can amount to a significant part of the total losses. In steady-state operation, each switch of the 3DAB converter is turned-on and turned-off for one half-cycle respectively. If the 3DAB converter operates in the zero voltage switching (ZVS) range, turn-on losses of the semiconductors can be minimised. Under ZVS operation, conduction and turn-off switching losses can be expected to be the main source of semiconductor losses. In a

future step, an analysis of switching loss in each hard-switching and soft-switching range will be required in order to accurately determine the power dissipated in the semiconductor. In this work, a simple calculation is applied to estimate the loss during the ZVS operation. Turn-off loss is calculated from the turn-off energy loss curve given in the datasheet for the corresponding turn-off current and voltage. The total switching losses are calculated by summing the losses of the individual switching events

$$P_{sw_off} = \frac{1}{t_{off}} \sum E_{OFF} \tag{E.10}$$

Similarly, the calculation of the turn-on loss corresponds to the turn-off loss

$$P_{sw_on} = \frac{1}{t_{on}} \sum E_{ON} \tag{E.11}$$

Average switching losses of IGCTs and Diodes are calculated from

$$P_{sw_LV} = n\left[(E_{OFF_igct} + E_{OFF_diode}) \times f_{sw} \times \frac{V_{CE}}{V_{CC}} \right] \tag{E.12}$$

$$P_{sw_HV} = n\left[(E_{OFF_igct} + E_{OFF_diode}) \times f_{sw} \times \frac{V_{CE}}{V_{CC}} \right] \tag{E.13}$$

where, *n* is the number of devices, f_{sw} is the switching frequency, V_{CE} is the operating voltage, and V_{CC} is the maximum voltage defined from the energy loss curves. Fig. E.5 shows analysed turn-off losses in Joules for selected high-power IGCT and IGBT devices for the two scenarios. Turn-off losses E_{OFI} are valid at the selected value of the 3DAB converter currents and at the limited devices' junction temperature

($T_j = 125°C$). As can be found from Fig. E.5(a), the asymmetric IGCT device with higher voltage rating is in tendency worse than the Hipak IGBT device. However, for an equal voltage level assessment as Fig. E.5(b), the 4.5kV IGCT device allows the selection of more efficient devices with respect to the target rating power than the HiPak IGBT device. In case of 40kVDC application, depicted in Fig. E.5(c), it indicates also that the 5.5kV IGCT device requires increased device physical layout resulting in higher switching losses than the 4.5kV StakPak IGBT device.

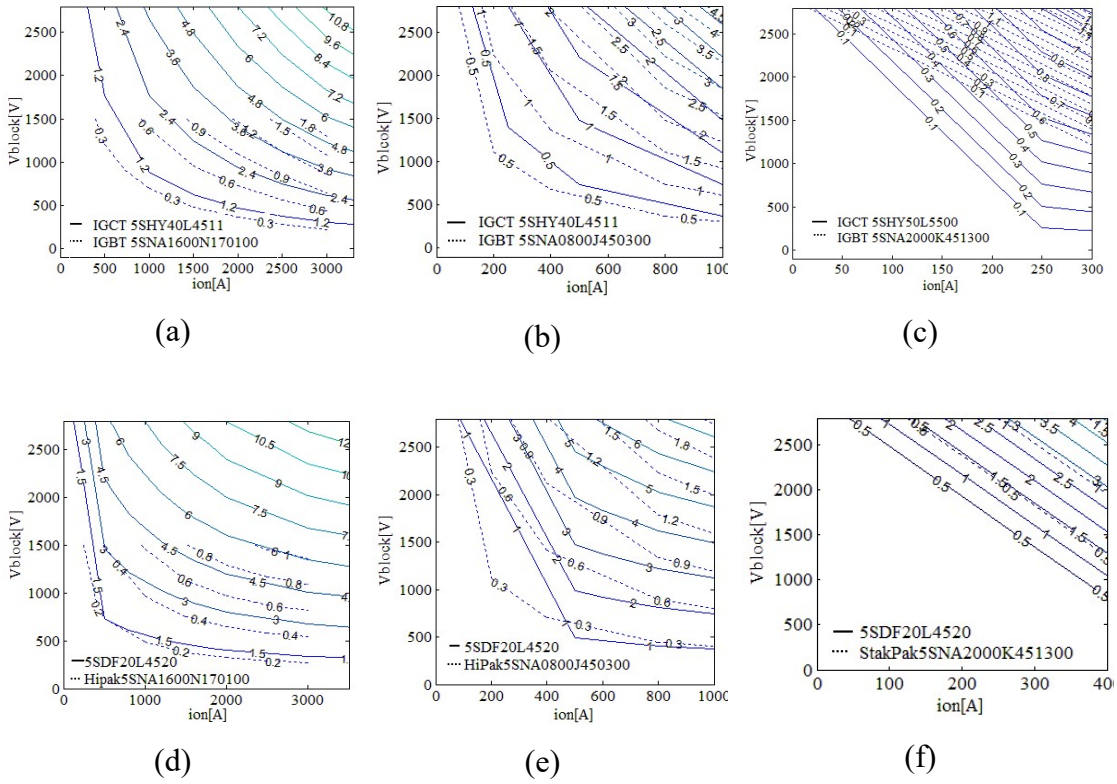


Figure E. 5 Turn-off losses in J of high power semiconductors: (a) active switches for 1.1kVDC level, (b) active switches for 5.2kVDC level, (c) active switches for 40kVDC level, (d) diodes for 1.1kVDC level, (e) diodes for 5.2kVDC level, (f) diode for 40kVDC level

E.5 Heat sink design

For higher power semiconductors (e.g. more than 15A), its cooling plates are no longer sufficient to fully conduct the carrying capacity. Hence, heat sinks are used to

increase in area for convection and heat radiation which spreads the heat flow. Fig. E.6 shows the proposed design flow chart of the heat sink. The goal of the heat sink design is to calculate the thermal resistance of the heat sink. In the design process, the semiconductor junction temperatures, $T_{j(T)}$ should not exceed their designed temperature limits under worst-cast operating conditions. The heat sink temperature, T_s is selected as the reference point for the worst-case operating point of the converter, since it maintains a relatively constant temperature compared to the IGBT and diode junctions. The design process involves calculating the IGBT module losses under full load condition for the chosen the surface temperature of heat sink with the desirable cooling method, then calculating the required heat sink-ambient thermal resistance, $R_{th(s-a)}$ to allow the heat sink to maintain the surface temperature at the full load.

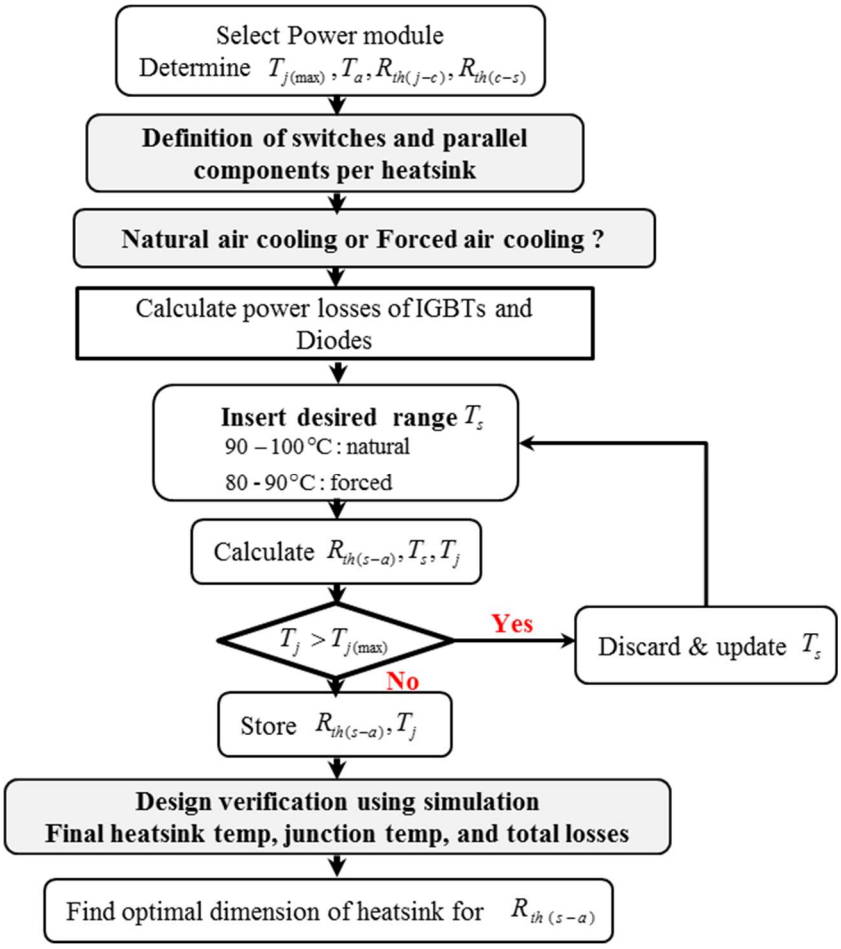


Figure E. 6 Design flow chart of the heat sink

As a starting point, assume an ambient temperature of 40°C. Using the manufacturer's datasheet, determine the maximum temperatures of the semiconductors. Also set the junction-case thermal resistance, $R_{th(j-c)}$ and case-heat sink thermal resistance, $R_{th(c-s)}$. The number of heat sources spread across the heat sink has a crucial impact on the $R_{th(s-a)}$. Therefore, it is important that the number of heat sources *n* is specified in the design process. Also a semiconductor device may consist of a parallel connection of several chosen components. This must also be defined. In this case, a three phase converter comprising 3 half-bridge modules is applied into the primary and secondary bridges. As a consequence, 6 switches are mounted on the each bridge heat sink without parallel connection. Natural air cooling is used in low power application up to 50W and even high power applications if sufficiently large cooling surfaces are available. The heat sink temperature is usually higher than with forced cooling system. For example, the heat sink temperature is about 90-100°C with natural air cooling whereas the rated surface temperature of forced air-cooled heat sink should not exceed 80-90°C. Using the calculated losses, it is possible to calculate the thermal resistance that is required to keep the heat sink temperature at or below the chosen cooling system and also the junction temperatures of the IGBT and diode. The calculated junction temperatures should not exceed the maximum values for $T_{j(T)}$ given from the manufacturer. For example, in case of the SKM75GB176D IGBT module, the maximum temperature $T_{j(T)}$ is 150°C.

To verify the design, simulate the combined electrical-thermal model of the 3DAB Converter and measure the heat sink and junction temperatures for each component The resulting $R_{th(c-s)}$ from the thermal design can be used to find the heat sink dimensions . From the design, the allowed value of 0.43 °C/W for $R_{th(c-s)}$ is calculated. For the experimentation, an aluminium heat sink shown in Fig. E.7 has been dimensioned with a lower value of 0.36 °C/W. To verify the chosen heat sink, run the PLECS simulation for steady-state analysis and measure the heat sink temperature and junction temperatures of the diodes and IGBTs. The measured temperatures of the chosen heat sink and the semiconductors for the final converter are given in Fig. E.8. The maximum junction temperatures of the IGBTs and diodes

for the primary and the secondary bridge are simulated for an ambient temperature of 45°C. Accordingly, the maximum junction temperature of the secondary bridge semiconductors is lower than the one of the primary bridge semiconductors.

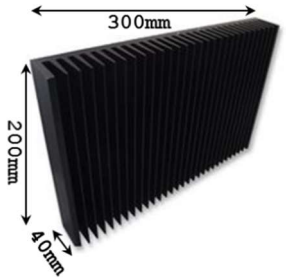


Figure E. 7 Heat sink layout for IGBT modules applied in the primary and secondary bridge converter.

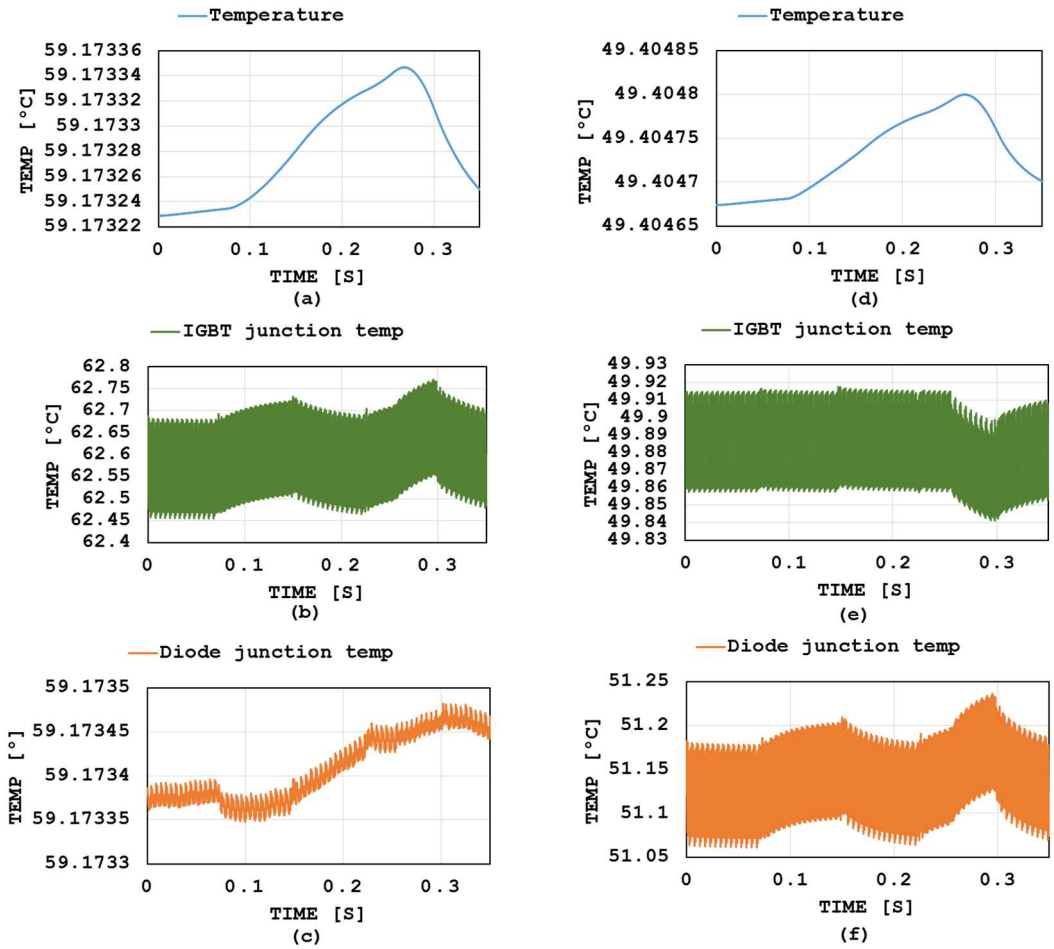


Figure E. 8 Steady-state analysis results with natural air cooling: (a) heat sink temperature of the primary bridge, (b) IGBT's junction temperature of the primary bridge, (c) junction temperature of diode in the primary bridge, (d) heat sink temperature of the secondary bridge, (e) IGBT's junction temperature of the secondary bridge, (f) junction temperature of diode in the secondary bridge

Appendix F

System evaluation for 4MW, 40kV MVDC Grids

F.1 Configuration of offshore wind farms

The most important advantages of DC grids for offshore wind farm are low power losses and small-size cables for carrying large amounts of power over long distances. The offshore DC grid considered is as shown in Fig. F.1. This is composed of several DC wind turbine drives connected to a MV/HVDC collector bus. The DC turbine is assumed here to include a PWM rectifier that converts the output voltage of AC wind turbine generator into Low-Voltage (LV) DC and a DC-DC converter to step the rectifier voltage up to the MVDC grid voltage for interconnection with the MV/HVDC collector bus.

Using a 3DAB conversion system, the bulky 50/60Hz transformer found in the conventional AC system can be replaced by a MF transformer operating in the kilo-hertz range, resulting in considerable reduction in transformer weight and size. Two possible turbine configurations are considered; the first with V_1 = 690V and another

with V_1 = 3.3kV. Considering the maximum voltage obtainable from a space vector modulation scheme for the maximum modulation index of 0.9, the DC-Link voltage V_2 in this phase of work is set as 1.1kV and 5.2kV (DC) respectively.

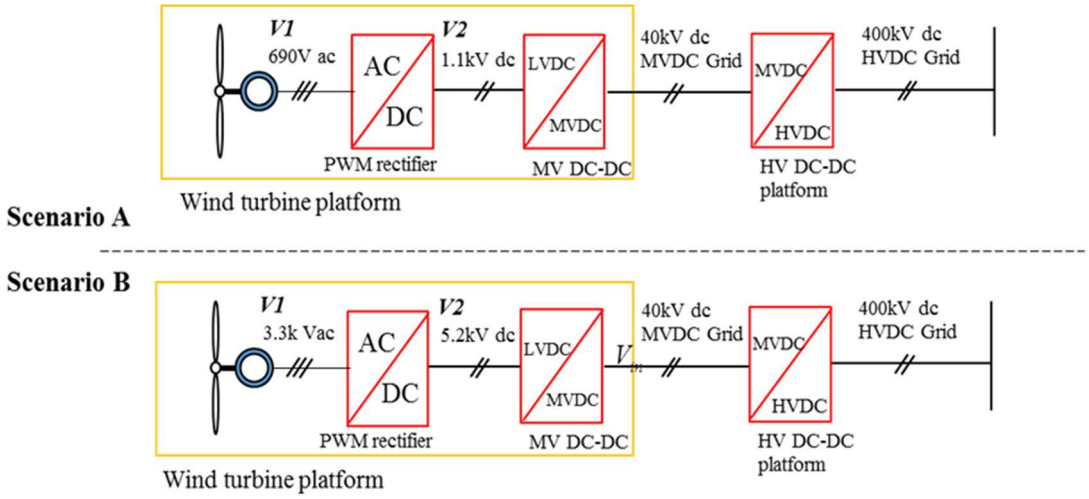
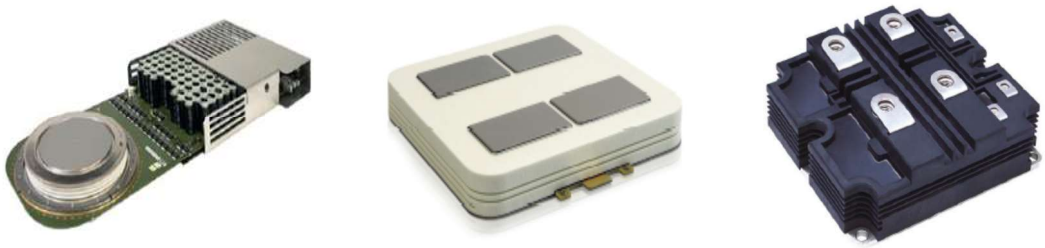


Figure F. 1 DC Grid for offshore wind farm

F.2 High power semiconductors

The recent developments of semiconductor devices has enabled significant progress for high power applications. The advanced technology has enabled developments to increase switching frequency, reduce device power losses, and integrate the gate drive circuit. Since MVDC system applications are considered, insulated gate bipolar transistor (IGBT) and integrated gate commutated thyristor (IGCT) are likely to be the suitable devices for these applications. In general, IGCT devices can be considered for multi-megawatt MV converters due to its snubberless operation, lower conduction and switching losses compared to an IGBT. As shown in Fig. F.2 (a), the asymmetric IGCT driver with ring-gate packaging provides very low gate inductance, typically below 5 nH. Under the circumstances, it allows the IGCT to operate without snubber circuits. Generally the asymmetric IGCT is applied in high power voltage source converters with anti-parallel diodes where the reverse voltage-blocking capability is not needed. The major design concern for IGBTs used in the high power converter applications is the modular packaging, as shown in Fig.

F.2 (c). In case of the press-pack IGBT, as shown in Fig. F.2 (b), assembly cost reduction and optimised efficient cooling are available in advanced modular packaging technology. The IGBT module features a low voltage gate drive circuit, a snubberless circuit, and high switching frequency operation. More importantly, a number of aspects such as efficiency, thermal management and optimal physical pathway design, reducing the effect of parasitic elements, should be considered in series connection of IGBT modules for a medium voltage converter. In contrast, the press-pack IGBTs allow direct series connection.



(a) (b) (c)

Figure F. 2 high power semiconductors: (a) Asymmetric IGCT, (b) StakPak IGBT module, and (c) HiPak IGBT module (Source: ABB [115])

F.2.1 Semiconductor device consideration

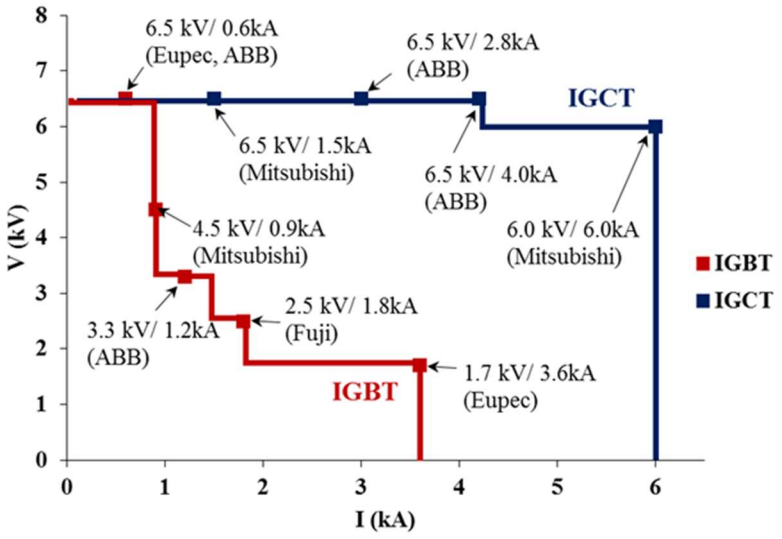


Figure F. 3 Voltage and current ratings of high-power IGBT and IGCT semiconductors

A comparison for the IGBT and IGCT is given in Table F.1. It refers to considerations on voltage, current, switching characteristics, and loss level of high-power semiconductor switching devices. Fig. F.3 shows the voltage and current ratings of major IGBT and IGCT devices commercially available for high-power applications. Generally, IGCTs are available with nominal voltage ratings of 4.5, 5.5, and 6.5 kV. On the other hand, IGBTs are for medium-voltage applications with nominal voltage ratings of 2.5, 3.3, 4.5, and 6.5 kV.

Table F. 1 Overview of high-power IGCT and IGBT devices

	IGBT	**IGCT**
Maximum Voltage and current ratings	High (6500V) Medium (3000A)	High (6500V) High (5500A)
Packaging	Module & press-pack	Press pack
Gate drive	Simple, low voltage, compact	Complex, integrated
Switching frequency	Fast	Medium
di/dt snubber circuit	Not required	Required
dv/dt snubber circuit	Not required	Not required
Active short-circuit protection	Yes	No

F.3 Analysis of two scenarios for MVDC collector grid

F.3.1 Evaluation circuit model for the scenarios

In these scenarios, a MV DC-DC collector based on the 3DAB Converter operated with different nominal input voltages V_{in} = 1.1kVDC and 5.2kVDC with a rated power of 4MW is interconnected with the MVDC grid. These models are operating with a switching frequency of 1000 Hz. In chapter 4, the allowed value of

the leakage inductance that ensures ZVS of the 3DAB converters has been calculated. In the two different scenarios, two MV DC-DC collectors applied using different semiconductor devices are compared in terms of the number of semiconductors, power losses and expense on transformer. For the given scenarios, the comparison of appropriate high-voltage, high-power IGBTs and IGCTs are carried out. To compare the dc-dc converters, the different devices would had the highest as possible blocking voltage ratings at acceptable conduction and switching properties. Conducting current ratings are several kA with low conduction and switching losses in specific ZVS operation ranges. Besides, high integration ability for series connection is proposed in multiple configurations. To investigate these scenarios, high power density semiconductors are considered as shown in Table F.2.

Table F. 2 Circuit parameters of the converters for the given scenarios

		Scenario A	**Scenario B**
Input Voltage [kDC]		1.1	5.2
Output Voltage [kDC]		40	
Switching Frequency [kHz]		1	
Leakage Inductance [uH]		10.79	178.71
Control Phase Shift Angle		21°	15°
IGBT based	Primary bridge	ABB Hipak 5SNA 1600N170100[115]	ABB HiPak 5SNA 0800J450300[115]
	Secondary bridge	ABB StakPak 5SNA 2000K451300[115]	
IGCT based	Primary bridge	ABB asymmetric IGCT 5SHY40L4511[115] Diode 5SDF20L4520[115]	
	Secondary bridge	ABB asymmetric IGCT 5SHY50L5500[115] Diode 5SDF20L4520[115]	

Fig. F.4 and F.5 show connection of semiconductors on the primary side (LV) converter. In scenario A, a total of 12 HiPak IGBT modules are applied in the primary bridge while 12 asymmetric IGCT modules are applied with 12 fast recovery diodes in the primary bridge. In scenario B, a parallel connection of semiconductors is not considered due to the low current. Since the devices are rated with a 2.8kV

blocking dc voltage, a series connection of semiconductors is required at the 5.2kV dc bus. In the contrary, the secondary bridge that operates on 40kVDC requires 108 StakPak IGBT modules to achieve the MV level and energise the peak power demand in IGBTs based converter. On the other hand, the secondary bridge requires 96 asymmetric IGCT modules with fast recovery diodes in the IGCT based system due to the high voltage capability of the IGCTs.

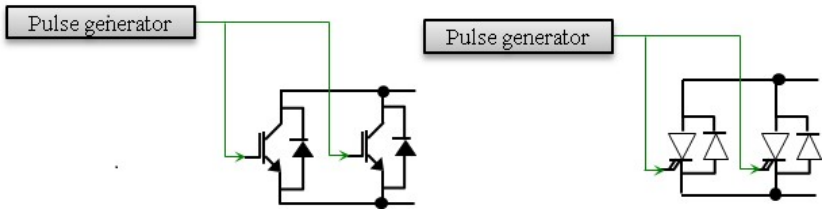


Figure F. 4 Active switching device configurations of primary side converter at 1.1kVDC$_{input}$

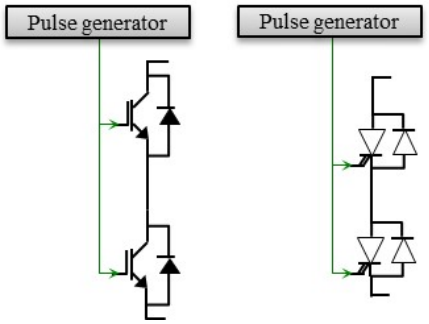


Figure F. 5 Active switching device configurations of primary side converter at 5.2kVDC$_{input}$

Fig. F.6 and F.7 show the simulated current and voltage waveforms of the 3DAB converter in steady-state operation as a function of dc conversion ratio *d.* The soft switching and hard switching of the converter can be analysed according to these waveforms.

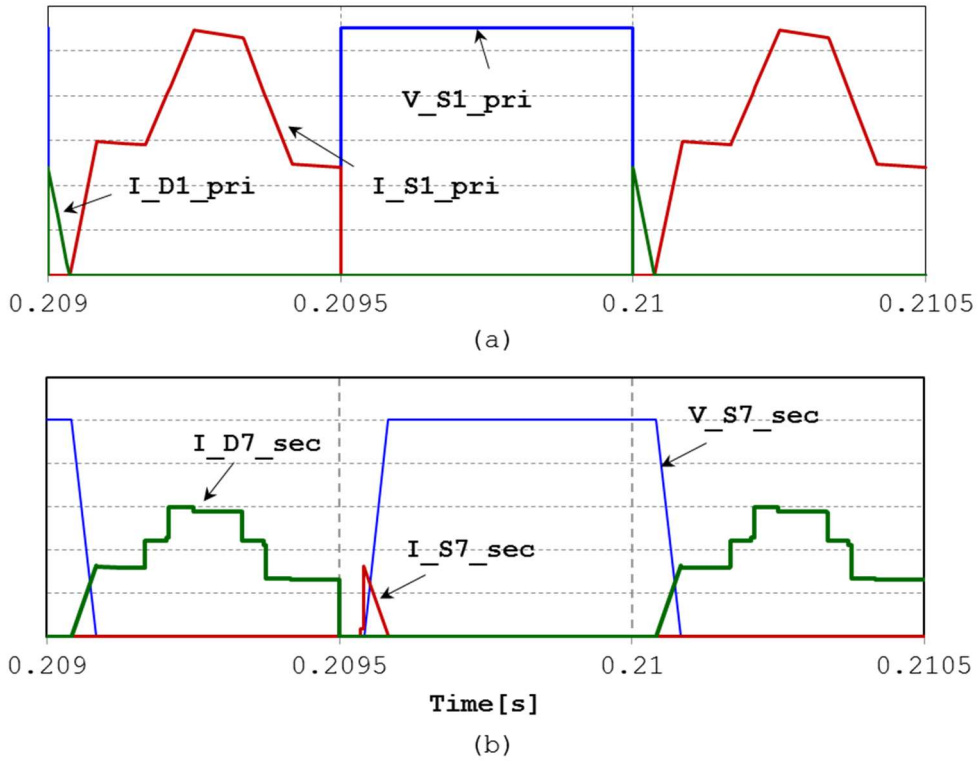


Figure F. 6 Voltage & Current waveforms under soft-switching area: (a) primary bridge and (b) secondary bridge (Vpri = 1100VDC, Vsec = 40kVDC, $\varphi = 30°$, $d = 1 (n = 1.1/40)$

Fig. F.6 shows simulated voltage and current waveforms under soft-switching on both bridges. On the primary bridge, S1 is turned on at zero voltage (ZVS) ON since current flows through the anti-parallel diode, D1, while there is zero current (ZC) at S1. The switched current commutates form the D to the S. And similarly, for the secondary bridge, S7 is turned on at zero voltage (ZVS) so that diode, D7, is conducting when corresponding switches are triggered on. At the turn-off actions, S1 and S7 are switched OFF at quasi ZVS. If a lossless snubber with capacitor is applied, the switches turn off virtually under ZVS, since the voltage rise is limited by the capacitor. During the soft switching, the turn-on losses can be eliminated since there is no current in the switches. Furthermore, the turn-off loss of IGCTs can be reduced compared with hard-switching operating. Fig. F.7 shows a hard-switching action on the secondary bridge. To drive this condition, the dc conversion ratio should be decreased to 0.5. In this condition, the S7 on the secondary side are hard-switched ON while the S1 on the primary bridge still can be achieved ZVS ON. In the turn-on process, turn-on loss of S7 is occurred since current flows through the main switches.

When the secondary side is turned off, hard-switched losses of the diodes are higher than soft-switched losses of main switches.

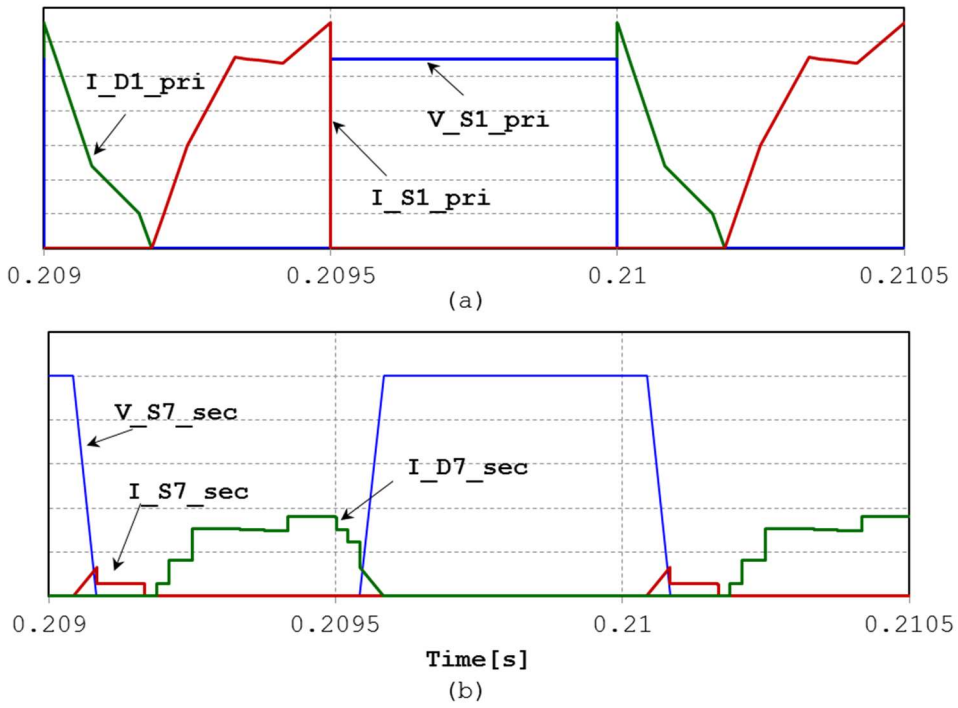


Figure F. 7 Voltage & Current waveforms under hard-switching area of Secondary side: (a) primary bridge and (b) secondary bridge (Vpri = 5200VDC, Vsec = 40kVDC, $\varphi = 30°$, $d = 0.5(n = 0.55/40)$

F.3.2 Power loss evaluation

The results take conduction losses and switching losses of the semiconductors into account as well as core losses and winding losses of the transformers. To verify the analytical calculation of the semiconductor losses, simulation models of the scenarios have been developed using the PLECS software [116]. The simulation models consist of PLECS-based electrical circuit of the 3DAB converter, phase shift angle modulator, and thermal loss monitoring functions. Power semiconductors have been electrically modelled as idealised IGBT and IGCT with anti-parallel diodes. The three-phase transformers have been modelled using a two-winding, three-leg, star-star connection with step up turn ratio and symmetric leakage inductances on the both windings. In the simulation models, magnetising current has been neglected, corresponding to an infinite magnetising impedance.

To analyse thermal performance, the converter model is simplified by modelling the input and output dc-buses as constant voltage sources and using an open-loop control scheme to set the steady-state operation. In addition, to simulate the thermal performance of the converter circuit and analyse the power semiconductor losses, thermal loss descriptions of the semiconductors in terms of conduction, switching losses, and thermal impedances are required. For example, using the given characteristics from the data sheets of these semiconductors, thermal descriptions for the devices have been created as given in Appendix G. During a switching cycle, the cycle-average losses of semiconductor can be calculated by summing the losses, generating an average dissipation pulse. The average loss calculation procedure is shown in Fig. F.8. To determine the average conduction losses, PLECS uses a periodic average model. This block periodically averages a continuous conduction loss over the specified switching time t_{sw}. A periodic impulse average model averages a switching energy loss consisting of a series of dirac impulses. The output of the block is updated at the end of each switching time t_{sw}. In the simulation, the PLECS C-Script block is used to perform averaging operations on the conduction and switching losses of the power semiconductors. Finally, using sum blocks, average losses are added to obtain the total IGBT/IGCT losses, total diode losses, and total overall losses.

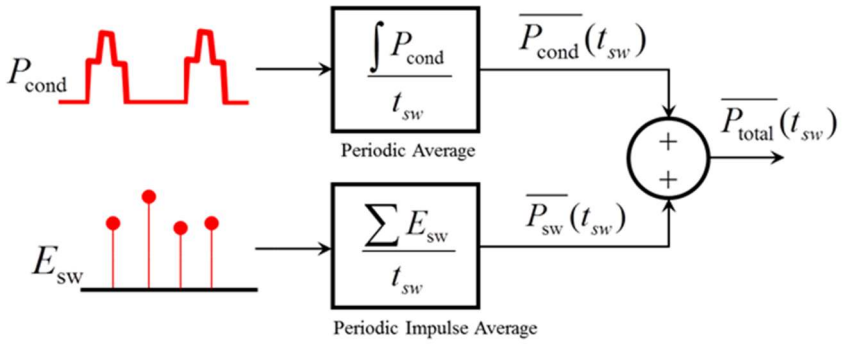


Figure F. 8 Calculation of total cycle-average losses

For the ac-linking magnetic losses, the non-sinusoidal excitation waveforms, generated from the PLECS simulation, are used to perform a 2D transient FEA to

determine the losses of the transformers as presented in chapter 4. Legend information for loss distribution diagrams of simulation results is illustrated as below.

- Core : Transformer core loss,
- Cu_pri : Transformer primary winding loss
- Cu_sec : Transformer secondary winding loss
- S_IGBTp : IGBT switching losses on primary side
- C_IGBTp : IGBT conduction losses on primary side
- S_IGBTs : IGBT switching losses on secondary side
- C_IGBTs : IGBT conduction losses on secondary side
- S_IGCTp : IGCT switching losses on primary side
- C_IGCTp : IGCT conduction losses on primary side
- S_IGCTs : IGCT switching losses on secondary side
- C_IGCTs: IGCT conduction losses on secondary side
- C_Dp : Diode conduction losses on primary side
- C_Ds : Diode conduction losses on secondary side

The breakdown of the losses in Fig. F.13 and F.14 show increasing semiconductor losses (switching loss and conduction loss) with transferred power, whereas the percentage of the transformer losses are smaller. The breakdown of an amount of conduction and switching losses in Fig. F.13 and F.14 shows increasing loss in both devices with increasing transferred power rating. Comparing semiconductor loss of configuration A to configuration B, the application of the IGBTs on the 1.1kV primary bridge shows a slightly lower loss compared to the IGCTs. However, the 5.2kV primary bridge IGCT devices show a better performance. It is found that the conduction losses of the IGCT modules on secondary side are higher than the IGBT modules at all points. This is mainly due to the higher threshold value of the IGCT device compared to the collecter-emitter voltage of the IGBT module corresponding to zero current. Note that the switching losses of IGCTs and IGBTs are a more significant issue for the efficiency of the 3DAB converter. In scenario A, considering the IGBTs switching losses on 1.1kV primary bridge, it can be found that the switching losses of the IGCTs are higher than the IGBTs at all points. Comparing the IGBTs switching losses to IGCTs, the switching losses of the IGBTs of primary bridge are found to be 6kW, which is much lower than the IGCTs. However, the switching losses of IGBTs are significantly higher than the IGCTs on the 5.2kV primary bridge as well as 4kV secondary bridges in both cases. It seems to that the

IGCTs show a better performance for turning-off switching on the high voltage levels. From the comparison, the IGCT based 3DAB converter shows a slightly lower efficiency than the IGBT based converter in the scenario A. However, the IGCT based converter shows a better performance if the converter is operated in scenario B as shown in Fig. F.14, corresponding to 5.2kV input voltage for primary converter and 40kV output voltage for secondary side converter. This is mainly because of an increase in the IGBT turn-off switching losses on the primary and secondary bridge.

Regarding the transformer loss, it can be seen that the winding losses clearly dominate the overall transformer losses at full load. On the other hand, the core loss can be considerable as main power dissipation source at lower transferred power level up to 75 % of the full power condition. At the 25% transferred power condition, it is seen that the loss in the core material is over 90 % of the transformer loss. On the contrary, it is clearly that the simulated winding losses in the primary and secondary sides contribute below 10 % of the total losses due to reduced conducting current levels. Considering scenario B, it is found that the core loss is increased with higher voltage level and towards higher transferred powers.

Considering the measured efficiency of the scenario B, the efficiency of IGCTs based converter is about 98.2 % while the losses of the IGBTs based converter are higher at the full power leading to a lower efficiency of about 97.4% due to high turn-off losses. For both scenarios, the MV DC-DC collector based on the two different semiconductors can be operated with greater than 97 % efficiency. At a load of 25%, core loss is considered as the main part of the power dissipation for the MV DC-DC collector. For the case of 40kVDC grids, the IGBT based converter requires a slightly higher quantity of semiconductors. Consequently, the efficiency of the IGBTs based converter becomes lower than the efficiency of the 3DAB converter designed with IGCT devices. For the 1.1kVDC primary side converter, however, it has been shown that the condition performance of the IGBTs is higher compared to the condition performance of the IGCTs, because the switching loss of the IGCTs becomes high resulting in a low efficiency.

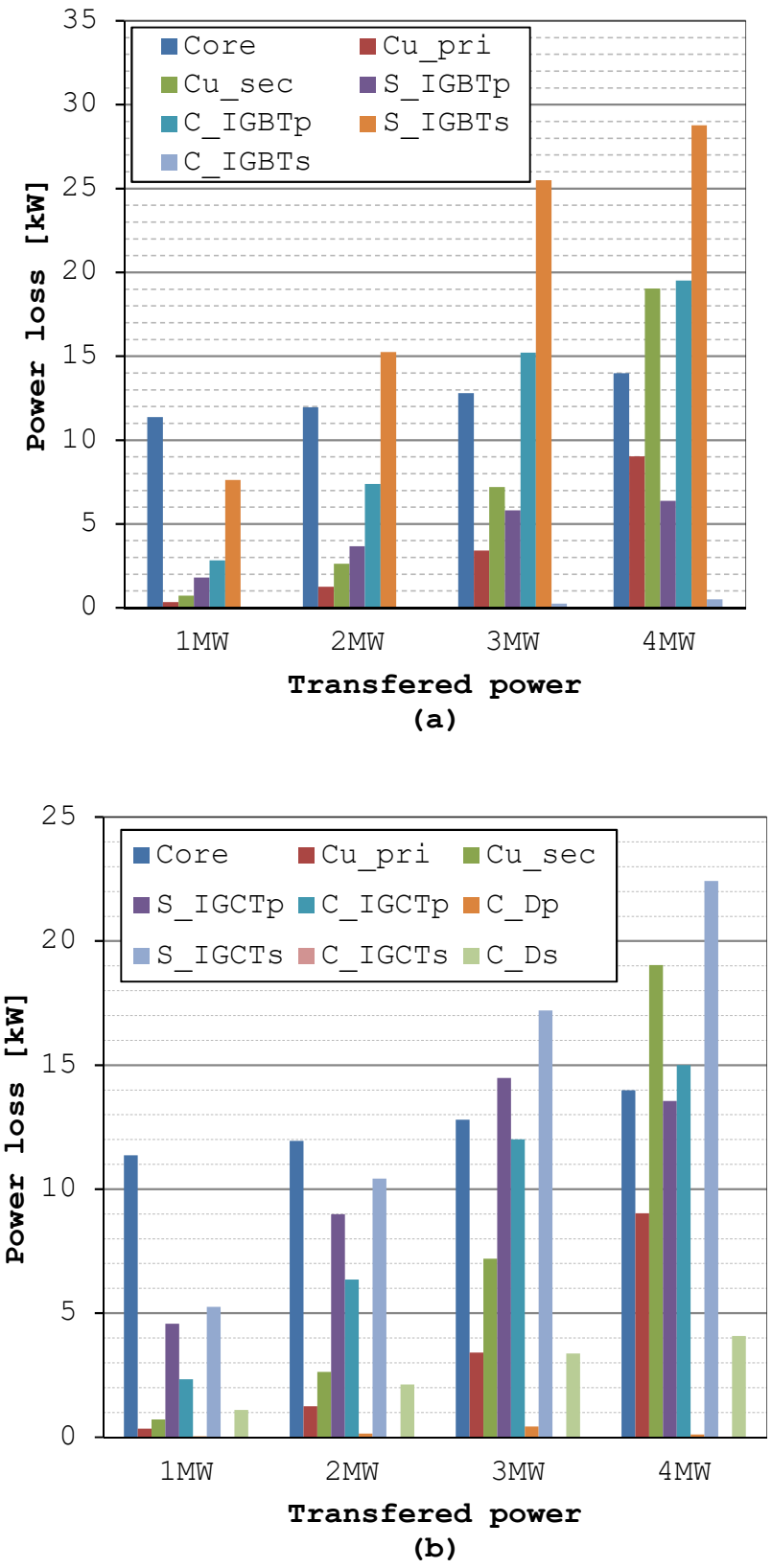
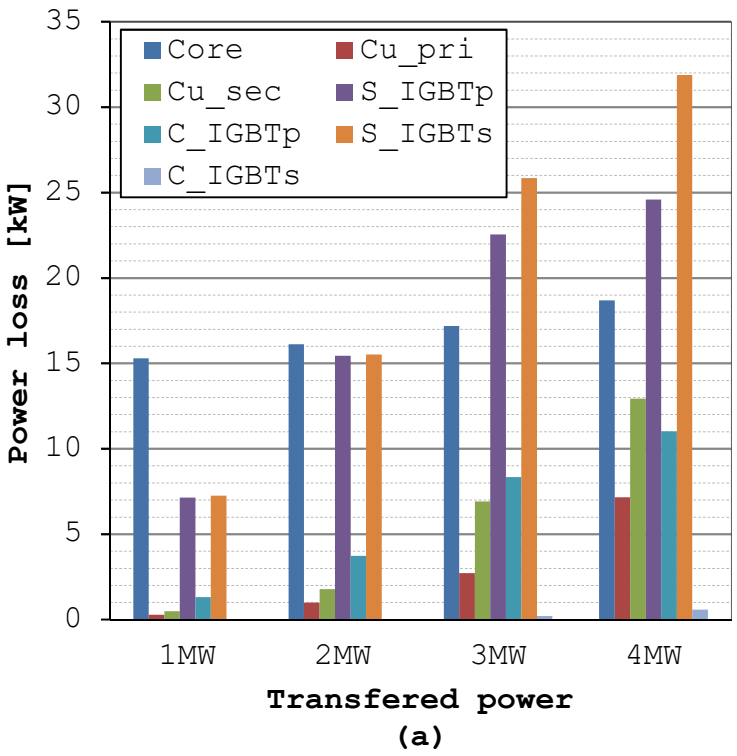


Figure F. 9 Loss distributions: (a) Scenario A with IGBT based converter, (b) Scenario A with IGCT based converter



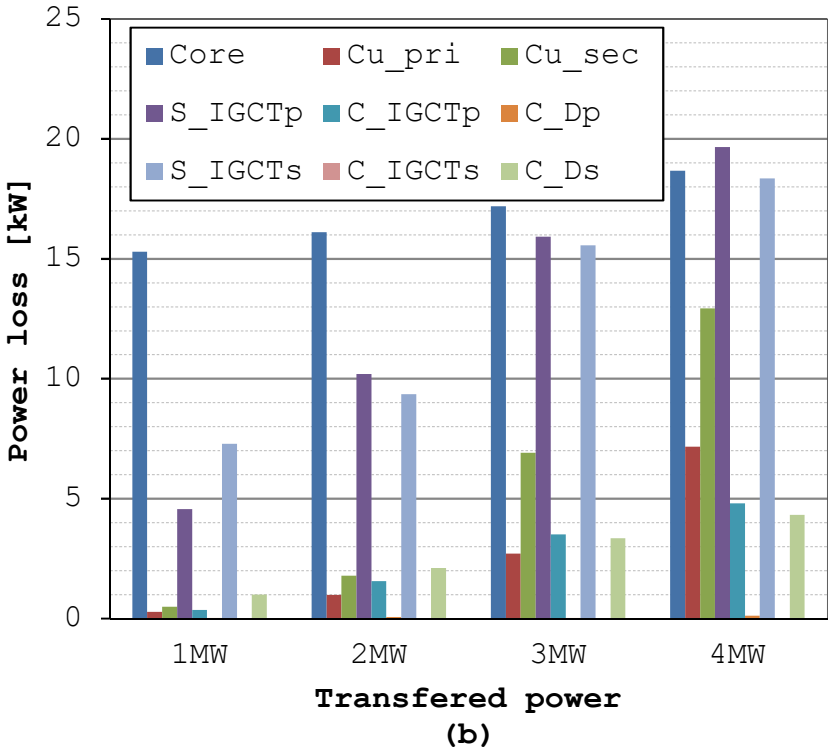


Figure F. 10 Loss distributions: (a) Scenario B with IGBT based converter, and (b) Scenario B with IGCT based converter.

Appendix G

Thermal description of power-semiconductor

To simulate the semiconductor losses, it is necessary to create a thermal description for the semiconductor. Using the data sheet, the following lookup tables for conduction losses, turn-on losses, turn-off losses, and thermal impedance between junction and case are considered.

G.1 Hipak 5SNA1600N170100

G.1.1 Conduction losses

Table G. 1 Conduction losses lookup table of 5SNA1600N170100

Diode									
	-3000A	**-2500A**	**-2000A**	**-1500A**	**-1000A**	**-500A**	**-200A**	**-100A**	**0A**
25 °C	-2.069	-1.918	-1.768	-1.617	-1.465	-1.279	-1.102	-0.672	0
125 °C	-2.256	-2.058	-1.86	-1.634	-1.408	-1.13	-0.878	-0.524	0
IGBT									
	0A	**100A**	**200A**	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**
25 °C	0	1.006	1.194	1.476	1.851	2.174	2.497	2.807	3.117
125 °C	0	0.881	1.106	1.522	2.035	2.479	2.923	3.372	3.82

G.1.2 Turn-on losses

Table G. 2 Turn-on switching energy loss lookup table of 5SNA1600N170100

Tc = 25 °C							
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**
0V	0	0	0	0	0	0	0
900V	0	0.123	0.232	0.355	0.479	0.644	0.896
1500V	0	0.205	0.387	0.592	0.798	1.073	1.493
Tc = 125 °C							
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**
0V	0	0	0	0	0	0	0
900V	0	0.177	0.333	0.511	0.688	0.925	1.288
1500V	0	0.295	0.556	0.851	1.147	1.542	2.147

G.1.3 Turn-off losses

Table G. 3 Turn-off switching energy loss lookup table of 5SNA1600N170100

Diode							
Tc = 25 °C							
	-3000A	**-2500A**	**-2000A**	**-1500A**	**-1000A**	**-500A**	**0A**
900V	0.371	0.347	0.313	0.268	0.208	0.137	0
1500V	0.619	0.579	0.521	0.447	0.346	0.228	0
Tc = 125 °C							
	-3000A	**-2500A**	**-2000A**	**-1500A**	**-1000A**	**-500A**	**0A**
900V	0.661	0.618	0.557	0.477	0.37	0.244	0
1500V	1.102	1.03	0.928	0.795	0.616	0.406	0
IGBT							
Tc = 25 °C							
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**
900V	0	0.172	0.298	0.433	0.568	0.738	0.96
1500V	0	0.287	0.497	0.722	0.947	1.23	1.601
Tc = 125 °C							
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**
900V	0	0.224	0.388	0.564	0.74	0.961	1.25
1500V	0	0.374	0.647	0.94	1.233	1.601	2.084

G.1.3 Thermal impedance

Table G. 4 Thermal impedances lookup table of 5SNA1600N170100

IGBT				
R K/W)	0.00759	0.0018	0.00074	0.00037
$\tau(s)$	0.202	0.0203	0.00201	0.00052
Diode				
R(K/W)	0.0126	0.00289	0.0013	0.00126
$\tau(s)$	0.21	0.0296	0.00701	0.00149

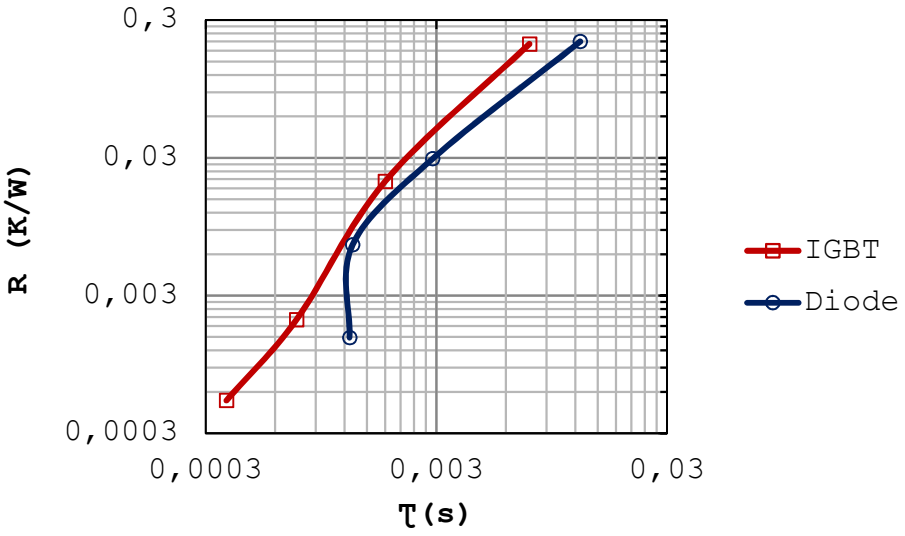


Figure G. 1Thermal impedances of 5SNA1600N170100 versus time (s) for Foster equivalent circuit

G.2 HiPak 5SNA0800J450300

G.2.1 Conduction losses

Table G. 5 Conduction losses lookup table of 5SNA0800J450300

Diode												
	-1600A	**-1300A**	**-1100A**	**-1000A**	**-900A**	**-800A**	**-600A**	**-400A**	**-200A**	**-100A**	**-50A**	**0A**
25 °C	-3.935	-3.664	-3.486	-3.395	-3.3	-3.2	-2.978	-2.703	-2.307	-1.996	-1.784	0
125 °C	-4.641	-4.255	-3.973	-3.824	-3.665	-3.5	-3.133	-2.702	-2.156	-1.79	-1.555	0
IGBT												
	0A	**50A**	**100A**	**200A**	**400A**	**600A**	**800A**	**900A**	**1000A**	**1100A**	**1300A**	**1600A**
25 °C	0	1.052	1.211	1.476	1.906	2.27	2.6	2.756	2.909	3.059	3.353	3.789
125 °C	0	1.046	1.345	1.794	2.476	3.04	3.55	3.794	4.033	4.27	4.741	5.464

G.2.2 Turn-on losses

Table G. 6 Turn-on switching energy loss lookup table of 5SNA0800J450300

Tc = 25 °C						
	0A	**200A**	**400A**	**800A**	**1200A**	**1600A**
2800V	0	0.4782	0.8555	1.85	3.165	4.799
Tc = 125 °C						
	0A	**200A**	**400A**	**800A**	**1200A**	**1600A**
2800V	0	0.703	1.169	2.58	4.631	7.926

G.2.3 Turn-off losses

Table G. 7 Turn-off switching energy loss lookup table of 5SNA0800J450300

Diode						
Tc = 25 °C						
	-1600A	**-1200A**	**-800A**	**-400A**	**-200A**	**0A**
2800V	1.811	1.524	1.14	0.6606	0.3848	0
Tc = 125 °C						
	-1600A	**-1200A**	**-800A**	**-400A**	**-200A**	**0A**
2800V	2.849	2.409	1.88	1.184	0.7502	0
IGBT						
Tc = 25 °C						

	0A	200A	400A	800A	1200A	1600A
2800V	0	1.041	1.746	3.15	4.548	5.94
Tc = 125 °C						
	0A	**200A**	**400A**	**800A**	**1200A**	**1600A**
2800V	0	1.258	2.042	3.778	5.738	7.922

G.2.4 Thermal impedances

Table G. 8 Thermal impedances lookup table of 5SNA0800J450300

IGBT			
R (K/W)	0.00954	0.00317	0.00156
$\tau(s)$	0.193	0.0214	0.00278
Diode			
R(K/W)	0.0187	0.00656	0.00323
$\tau(s)$	0.192	0.0226	0.0031

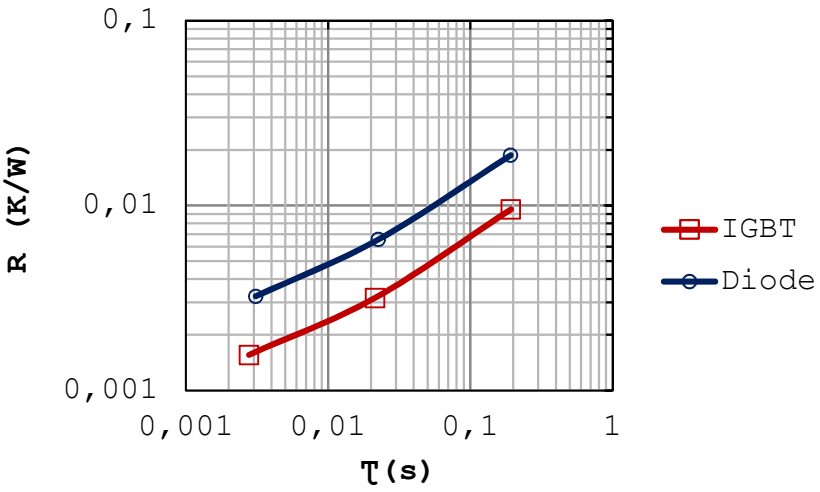


Figure G. 2 Thermal impedances of 5SNA0800J450300 versus time (s) for Foster equivalent circuit

G.3 StakPak 5SNA2000K451300

G.3.1 Conduction losses

Table G. 9 Conduction losses lookup table of 5SNA2000K451300

Diode									
	-3500A	**-3000A**	**-2500A**	**-2000A**	**-1500A**	**-1000A**	**-500A**	**-250A**	**0A**
25 °C	-3.1	-2.9	-2.75	-2.6	-2.4	-2.2	-1.8	-1.6	0.6
125 °C	-3.7	-3.5	-3.25	-3	-2.75	-2.34	-1.8	-1.4	0.6
IGBT									
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**	**3500A**	**4000A**
25 °C	0.6	1.55	2.1	2.5	2.85	3.2	3.55	3.95	4.3
125 °C	0.6	1.59	2.6	3.2	3.65	4.15	4.6	5.2	5.7

G.3.2 Turn-on losses

Table G. 10 Turn-on switching energy loss lookup table of 5SNA2000K451300

Tc = 25 °C						
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**
2800V	0	1.78	3.55	5.7	8.11	10.99
Tc = 125 °C						
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**
2800V	0	2.5	4.9	7	9.96	13.5

G.3.3 Turn-off losses

Table G. 11 Turn-off switching energy loss lookup table of 5SNA2000K451300

Diode						
Tc = 25 °C						
	-2500A	**-2000A**	**-1500A**	**-1000A**	**-500A**	**0A**
2800V	3.37	2.93	2.4	1.75	1	0
Tc = 125 °C						
	-2500A	**-2000A**	**-1500A**	**-1000A**	**-500A**	**0A**
2800V	5	4.69	3.9	3	2	0
IGBT						
Tc = 25 °C						
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**
2800V	0	2.16	3.84	5.65	7.67	9.8

Tc = 125 °C						
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**
2800V	0	2.96	5.05	8.02	9.79	

G.3.4 Thermal impedances

Table G. 12 Thermal impedances lookup table of 5SNA2000K451300

IGBT				
R (K/W)	0.0018	0.00223	0.0004	0.00037
$\tau(s)$	0.581	0.059	0.006	0.0001
Diode				
R(K/W)	0.00361	0.00396	0.00803	0.00727
$\tau(s)$	0.584	0.059	0.006	0.0001

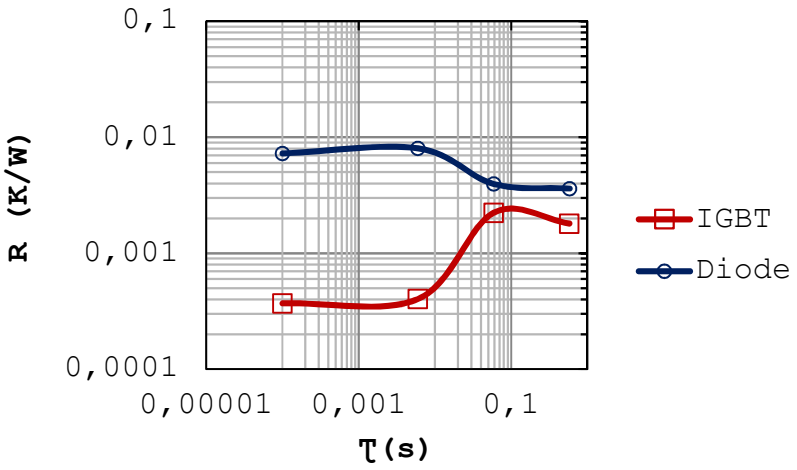


Figure G. 3 Thermal impedances of 5SNA2000K451300 versus time (s) for Foster equivalent circuit

G.4 Asymmetric 5SHY40L4511

G.4.1 Conduction losses

Table G. 13 Conduction losses lookup table of 5SHY40L4511

IGCT									
	0A	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**	**3400A**	**3800A**
25 °C	0	1.388	1.713	1.988	2.213	2.388	2.513	2.577	2.609
125 °C	0	1.45	1.8	2.1	2.3	2.55	2.75	2.9	3.1

G.4.2 Turn-on losses

Table G. 14 Turn-on switching energy loss lookup table of 5SHY40L4511

Tc = 125 °C			
	-50A	**0A**	**3300A**
0V	0	0	0
2800V	0	0	1.5

G.4.3 Turn-off losses

Table G. 15 Turn-off switching energy loss lookup table of 5SHY40L4511

IGCT									
Tc = 25 °C									
	0A	**250A**	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**	**3300A**
-100V	0	0	0	0	0	0	0	0	0
0V	0	0	0	0	0	0	0	0	0
2800V	0	0.88	1.67	3.34	4.74	6.32	7.9	9.66	10.54
Tc = 125 °C									
	0A	**250A**	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**	**3300A**
-100V	0	0	0	0	0	0	0	0	0
0V	0	0	0	0	0	0	0	0	0
2800V	0	1	1.9	3.8	5.4	7.2	9	11	12

G.4.4 Thermal impedances

Table G. 16 Thermal impedances lookup table of 5SHY40L4511

IGCT				
R (K/W)	0.0056	0.0015	0.0009	0.0005
$\tau(s)$	0.5119	0.0896	0.0091	0.0024

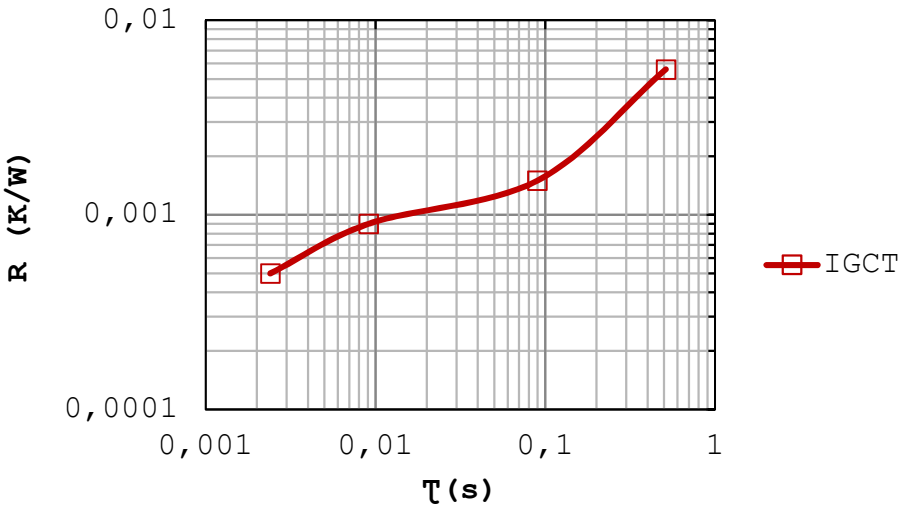


Figure G. 4 Thermal impedances of 5SHY40L4511 versus time (s) for Foster equivalent circuit

G.5 Asymmetric 5SHY50L5500

G.5.1 Conduction losses

Table G. 17 Conduction losses lookup table of 5SHY50L5500

IGCT									
	0A	**600A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**	**3500A**	**4000A**
25 °C	0	2	2.3	2.53	2.8	3	3.15	3.34	3.5
125 °C	0	1.7	2.1	2.44	2.7	3	3.22	3.5	3.72

G.5.2 Turn-on losses

Table G. 18 Turn-on switching energy loss lookup table of 5SHY50L5500

Tc = 125 °C			
	-50A	**0A**	**3300A**
0V	0	0	0
2800V	0	0	2

G.5.3 Turn-off losses

Table G. 19 Turn-off switching energy loss lookup table of 5SHY50L5500

IGCT									
Tc = 25 °C									
	0A	**250A**	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**	**3300A**
-100V	0	0	0	0	0	0	0	0	0
3300V	0	1.125	2.25	4.5	6.75	9	11.25	13.5	14.85
Tc = 125 °C									
	0A	**250A**	**500A**	**1000A**	**1500A**	**2000A**	**2500A**	**3000A**	**3300A**
-100V	0	0	0	0	0	0	0	0	0
3300V	0	1.1	2.9	5.4	8.1	11	13.5	16.1	18

G.5.4 Thermal impedances

Table G. 20 Thermal impedances lookup table of 5SHY50L5500

IGCT				
R (K/W)	0.00556	0.00153	0.00087	0.00055
$\tau(s)$	0.5119	0.0896	0.0091	0.0024

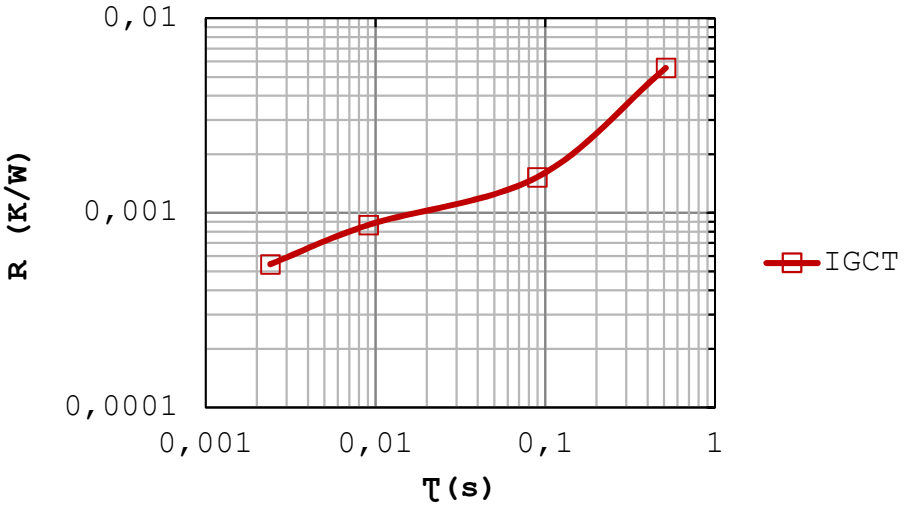


Figure G. 5 Thermal impedances of 5SHY50L5500 versus time (s) for Foster equivalent circuit

G.6 Diode 5SDF20L4520

G.6.1 Conduction losses

Table G. 21 Conduction losses lookup table of Diode 5SDF20L4520

Diode									
	400A	**450A**	**500A**	**550A**	**600A**	**650A**	**700A**	**750A**	**800A**
25 °C	2.158	2.249	2.334	2.415	2.492	2.566	2.637	2.705	2.771
125 °C	1.72	1.793	1.863	1.929	1.992	2.053	2.112	2.169	2.225
	850A	**900A**	**950A**	**1000A**	**1050A**	**1100A**	**1150A**	**1200A**	**1250A**
25 °C	2.835	2.897	2.957	3.016	3.074	3.13	3.185	3.239	3.292
125 °C	2.279	2.332	2.384	2.434	2.484	2.533	2.581	2.628	2.675

G.6.2 Turn-off losses

Table G. 22 Turn-off switching energy loss lookup table of Diode 5SDF20L4520

Diode							
Tc = 140 °C							
	0A	**500A**	**600A**	**800A**	**1000A**	**1200A**	**1400A**
-2800V	0	5.7	6.1	6.9	7.5	8.2	8.8
0V	0	0	0	0	0	0	0
Tc = 140 °C							
	1600A	**1800A**	**2000A**	**3000A**	**4000A**	**5000A**	
-2800V	9.4	9.9	10.5	12.5	13.8	15	
0V	0	0	0	0	0	0	

G.6.3 Thermal impedances

Table G. 23 Thermal impedances lookup table of Diode 5SDF20L4520

Diode				
R(K/W)	0.00371	0.00143	0.00069	0.00018
$\tau(s)$	0.5336	0.067	0.0074	0.0011

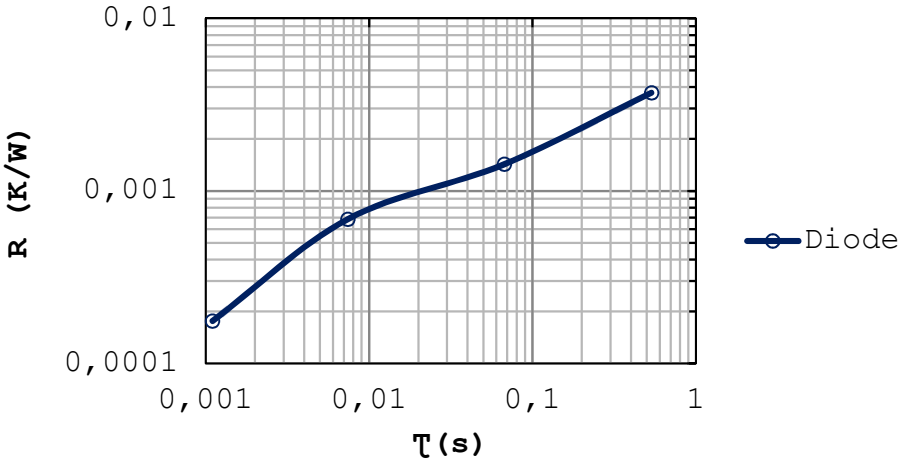


Figure G. 6 Thermal impedances of Diode 5SDF20L4520 versus time (s) for Foster equivalent circuit

Appendix H

Matlab script for the optimisation

```
clear all
clc
warning off

%% Setting the Temporary Directory

FileName = 'Temp';
path = [cd '\', num2str(FileName)];
setenv('TEMP', path)
% setenv('TMP', path)

%% Model Building

MN6 = actxserver('Magnet.application');              % Building a virtual machine
set(MN6, 'Visible', 1);
% path = [cd,'\transformer_model.mn'];               % Magnet file name definition
% invoke(MN6,'openDocument',num2str(path));          % Opening the Magnet file

addpath Magnet_Script
addpath Matlab_Script

ires = 0;

% MF Frequency Transformer for 3 DAB DC-DC Converter

%% DC-DC converter parameters
```

```
Vin_dc = 5.2e3;             % DC input voltage [V]
Vout_dc = 40e3;             % DC output voltage [V]
Pin = 4e6;                  % Converter rating power [W]
fsw = 1000;                 % operating frequency [Hz]
degrees = -360:1:360;
omega=2*pi*fsw;

radians = degrees*(pi/180);
phaseAngle = radians;

Eeff = 0.98;                % expected efficiency
Duty = 0.5;                 % Duty cycle
Et = 0.45*sqrt(4000);       % Voltage per turns
% N1 = Vpn/Et = 89.9..
Nt = 1.1/40;                % Turn ratio


delta = 1;                  % dc conversion ratio
theta = 60*(pi/180);

%% Calculate kVAt - transformer apperent rating

% St = sqrt(2)*Pin;       % apparent transformer power for soft switching [W]
St = 1.33*Pin;            % apparent transformer power for 3DAB

%% Calculation of Base leakgae inductance for 3DAB
L = (Vin_dc^2/(2*pi*fsw*Pin))*1*((pi/2)-((pi/2)^2/pi)-pi/18);              % for full
Poutput
% L =(Vin_dc^2/(2*pi*fsw*Pin))*delta*(theta-(theta^2/pi)-pi/18);
% L =(Vin_dc^2/(2*pi*fsw*Pin));                   % for Base inductance - Po is 0.6pu

Vpn = (sqrt (2)/3)*Vin_dc;    % Vac_pri RMS 3DAB
% Vpn = (2/3)*Vin_dc;         % Max Vac_pri 3DAB
Vsn = Vpn/Nt;

%% Calculate current versus d and theta as parameter
% theta < pi/3
Ip = (Vin_dc/(3*2*pi*fsw*L))*theta*sqrt((2*pi-theta)/pi);
% theta >= pi/3
% Ip = (Vin_dc/(6*2*pi*fsw*L))*theta*sqrt((2*(4*pi-3*theta))/pi);
% Ip = St/(3*Vpn);                        % Iac Y-Y connection sinewave
% Ip = (1.21/sqrt(2))*(Pin/Vin_dc);       % Iac_pri RMS 3DAB

Is = Ip*Nt;

%% Calculate Average output power
% theta < pi/3
 Pout = (Vin_dc^2/(2*pi*fsw*L))*delta*theta*(2/3-theta/(2*pi));
```

```
% theta >= pi/3
% Pout = (Vin_dc^2/(2*pi*fsw*L))*delta*(theta-(theta^2/pi)-pi/18);

%% Calculation V, I and St for star-star connection transformer
 BaseCurrent = Vin_dc/(3*omega*L);

 PrimaryCurrent=PriCurrent(phaseAngle,BaseCurrent,theta,delta);

 MaxC = max(PrimaryCurrent);

savefile = 'ex_w.mat';
ex_w=PriCurrent(phaseAngle,BaseCurrent,theta,delta);
save(savefile,'ex_w')

plot(phaseAngle,PrimaryCurrent,'r','LineWidth',2)
xlabel ('Phase angle')
ylabel ('primary side Ia')
grid on
hold on

%% Transformer parameters
Bm = 1.2;              % Peak flux density [T]

Kf = 4;               % Waveform coefficient, squre wave=4, sine wave=4.44
Ku = 0.4;              % Window utilization factor

%% Core material parameters
%- Metglas 2605SA1 amorphous alloy for MF
Core_th = 0.025;       % lamination thickness [mm]
K_core = 0.75;         % core stacking factor
Den_core = 7180;       % density of core [kg/m^3]

% M-19 29 Ga
kh = 0.00968569;
alpha = 1.19792;
belta = 1.79564;
ke = 4.12318e-005;
s = 1;
Den_M19 = 7650;

%% Copper parameters
Rho = 1.678e-8;        % the resistivity of conductor in ohm.m
% Rho = 1.8e-8;
Mu0 = 4*pi*10^-10;
Mur = 0.9999935849;
Mu = Mu0*Mur;          % the absolute magnetic permeability of the conductor

%% Insulation material parameters
Eins_gf = 1.6;         % Dielectric strength of glass fiber [kV/mm]
Eins_pap = 1.6;        % Dielectric strength of paper [kV/mm]
```

```
S_ 1 = 1.5;              % safe factor #1
S_ 2 = 1.5;              % safe factor #2

% fprintf ('Vol,Weight,Pcore,Pcon,eff,N1,N2,Jp,Js,d/a,w/h:\n')
%% Optimal for loop function
% update of degrees of freedom

 for N1 = 1:1:200                    % Number of primary turn
    for Jp_e = 1:1:10                % Current density of primary side
       for Js_e = 1:1:10             % Current density of secondary side
          for hw_ratio= 0.1:0.1:3.0      % WH ratio of windonw area
            for da_ratio = 0.1:0.1:3.0   % da ratio of core cross sectional area

               N2_cal = N1/Nt;        % Numer of secondary widing turns
               N2 = round(N2_cal);
               Et = Vpn/N1;

%% Core design
% Ac = (Vpn*1e6)/(Kf*Bm*N1*fsw*K_core);      % core sectional area [mm^2]
Ac = 1e6*(Et/(Kf*fsw)/Bm);

Core_a = sqrt(Ac/da_ratio);              % width of core sectional area [m]
Core_d = Ac/Core_a;

% length of core sectional area [mm]
%% Winding design
% Calculation conductor area
[AWG_primary, diameterConductor_primary, Rconductor_primary,
AreaConductor_primary] = PrimaryCopperAWG(Ip, Jp_e);  % Selection AWG size -
from HV,LV copper AWG functions

[AWG_secondary, diameterConductor_secondary, Rconductor_secondary,
AreaConductor_secondary] = SecondaryCopperAWG(Is, Js_e);

%% Calculation Effective Skin depth
SkinDepth = sqrt(Rho/(pi*fsw*Mu))*1000;

%% Calculation conductor areas
% New primary conductor cross section [mm^2]
NewAcp = (pi*diameterConductor_primary^2)/4;

NewJp = Ip/NewAcp;               % New current density for primary side [A/mm^2]
PrimaryAcu = N1*NewAcp;      % Conductor area of primary [mm^2]

% New secondary conductor cross section [mm^2]
NewAcs = (pi*diameterConductor_secondary^2)/4;

NewJs = Is/NewAcs;               % New current density for secondary side[A/mm^2]
SecondaryAcu = N2*NewAcs;   % Conductor area of primary [mm^2]
```

```
TotalAcu = PrimaryAcu + SecondaryAcu;    % Total conductor area

%% Calculation window area
Wa = 2*(TotalAcu/Ku);                    % Window area for 3 phase [mm^2]
Window_w = sqrt(Wa/hw_ratio);            % width of window area [mm]
Window_h = Wa/Window_w;                  % height of window area [mm
]
%% Overall dimensions of transformer
Wtr = 2*Window_w+3*Core_a;               % Overall width of transformer [mm]
Htr = 2*Core_a+Window_h;                 % Overall height of transformer [mm]
Dtr = Core_d;                            % Overall lenght of transformer [mm]

%% Core Volume [m^3]
Vol_tr = (Ac*(3*Window_h+4*Window_w)+6*Core_a*Core_a*Core_d)*1e-9;

%% Calculation insulation - using paper
% Paper insulation layer - core/primary winding [mm]
dins_cp _paper = S_ 1*(Vpn/(Eins_pap*1000));

 % Paper insulation layer - primary/secondary windings [mm]
dins_prisec _paper = S_ 1*((Vpn+Vsn)/(Eins_pap*1000));

% Paper insulation layer - primary turns [mm]
dins_priturns _paper = S_ 2*((Vpn/N1)/(Eins_pap*1000));

% Paper fiber insulation layer - secondary turns [mm]
dins_secturns _paper = S_ 2*((Vsn/N2)/(Eins_pap*1000));

%% Calculate total winding width using paper
HPrimaryWinding_paper = Window_h - 2*dins_cp _paper;
WPrimaryWinding_paper = (PrimaryAcu/HPrimaryWinding_paper)+dins_priturns
_paper*N1;

HSecondaryWinding_paper = Window_h - 2*(dins_cp _paper/Nt);
WSecondaryWinding_paper =
(SecondaryAcu/HSecondaryWinding_paper)+dins_secturns _paper*N2;

TotalWindingWidth_paper = 2*(dins_cp
_paper+WPrimaryWinding_paper+dins_prisec  _paper+WSecondaryWinding_paper);

%% Calculate window utilisation factor, ku
Cu_winding =
(PrimaryAcu/HPrimaryWinding_paper)+(SecondaryAcu/HSecondaryWinding_paper
);

Kc = 2*(Cu_winding/Window_w);
%% Calculation length of turns
D1 = Core_d+2*dins_cp _paper;
D2 = D1+2*WPrimaryWinding_paper;
D3 = D2+2*dins_prisec _paper;
```

```
D4 = D3+WSecondaryWinding_paper;

% Design for conventional 4-stepped Core
% MLTp = pi*(D1+D2)/2;
% MLTs = pi*(D3+D4)/2;

% Design for Square Section Core
MLTp = 2*(D1+D2);
MLTs = 2*(D3+D4);

TLWp = N1*MLTp;                          % Total length of primary turns [mm]
TLWs = N2*MLTs;                          % Total length of secondary turns [mm]

%% Calculation leakage inductance

u0 = 4*pi*1e-10;                         % Permeability [H/mm]

Ll1_paper =(u0*N1^2*MLTp)/HPrimaryWinding_paper;
Ll2_paper = dins_prisec _paper/2+WPrimaryWinding_paper/3;

% Leakage inductance of primary side [mH]
Ll_paper = Ll1_paper*Ll2_paper*1e3;

L21_paper = (u0*N2^2*MLTs)/HSecondaryWinding_paper;
L22_paper = dins_prisec _paper/2+WSecondaryWinding_paper/3;

L2_paper = L21_paper*L22_paper*1e3;

% L_leakage = Ll1_paper*(dins_prisec
_paper+(WPrimaryWinding_paper+WSecondaryWinding_paper)/3)*1e3;

Lleakage =
((N1^2*u0*MLTp)/Window_h)*(WPrimaryWinding_paper/3+dins_prisec
_paper+WSecondaryWinding_paper/3)*1e3;

Lm = (u0*N1*N2*Ac*1e3)/Window_h;
% Lm = 0.3*sqrt(Ll_paper*L2_paper);

%% Calculation Power losses
% Calculation conductor weight
WpriConductor =
3*(diameterConductor_primary^2*0.006676*1.0517*TLWp)*0.001;

WsecConductor =
3*(diameterConductor_secondary^2*0.006676*1.0517*TLWs)*0.001;

%% Core weight
Wcore = Den_core*Vol_tr;                 % Core weight
% Wcore_m19 = Den_m19*Vol_tr;
Wcore_M19 = Den_M19*Vol_tr;
```

```
TotalW = WpriConductor + WsecConductor + Wcore_M19;

%% Calculation DC conductor resistance
% Rcopper = 1.68*1e-8;

Rp_dc = (Rho*1e-3*TLWp)/(NewAcp*1e-6); % DC resistance of primary conductor
Rs_dc = (Rho*TLWs*1e-3)/(NewAcs*1e-6);   % DC resistance of secondary

%% AC conductor resistance
Rp_ac = 1.5*Rp_dc;                      % AC resistance of primary conductor
Rs_ac = 1.5*Rs_dc;                      % AC resistance of secondary conductor

%% Calculation conductor loss

Pcon_p = 3*Rp_ac*Ip^2;                  % Primary conductor loss
Pcon_s = 3*Rs_ac*Is^2;                  % Secondary conductor loss
Pcon = Pcon_p+Pcon_s;                   % Total conductor loss

%% Calculation core loss
[K1, K2, K3] = SteinmetzFiting(fsw);            % Steinmetz fiting coeffciency
% Reference core loss using modified steinmetz equation [W/kg]
% Pfeo = K1*(fsw^K2)*(Bm^K3)*(Duty^(1-K2));
% Pfeo = 45.9577;          % Measured specific core loss for 1kHz, Bm>0.1. [W/kg]

% Pfeo_m19 = kh*fsw^alpha_m19*Bm^belta_m19;     % USS  % M19 Core
Pfeo_M19 =kh*(fsw^alpha)*(Bm^belta)+ke*(s*fsw*Bm)^2;  % M-19

% Pcore = Pfeo*Wcore_m19;                 % Core loss
% Pcore = Pfeo_m19*Wcore_m19;             % M19 core loss
Pcore = Pfeo_M19*Wcore_M19;

%% Calculation magnetizing current
% find out magnetizing force H(Amps/m) corresponding to Bm in the core and yoke
from B-H curve
% Bm_rms = 1.2 so calculate Bm = 1.2*sqrt(2) = 1.697. find out H
% correspondng to Bm = 1.697 from B-H curve

 at_core = 5653.058;                % magentizing force H corresponding in the core
 at_yoke = 5653.058;                % magentizing force H corresponding in the core

 MMF_core = 3*(Window_h+Core_d)*1e-3*at_core;    % MMF for the core
 MMF_yoke = 4*(Window_w+Core_d)*1e-3*at_yoke;  % MMF for the yoke

TotalMMF = 1.0*(MMF_core+MMF_yoke);    % Total MMF, we account 10% at
for joints

Im_peak = TotalMMF/(3*N1);              % Peak Value of Magentizing current
Im_rms = Im_peak/sqrt(2);               % RMS value of Magnetizing current
```

```
Ic = Pcore/Vpn;                          % Core loss current
Io = sqrt(Im_rms^2+Ic^2);                % No load current

%% Transformer loss & efficiency

Ptr_loss = Pcon + Pcore;                 % Transformer loss
eff_Tr = (Pout/(Ptr_loss+Pout))*100;     % Transformer efficiency

Ef_final = eff_Tr - Im_rms/Ip;           % final efficiency

%% Temperature rise
At = 2*(Wtr*Dtr+Wtr*Htr+Htr*Dtr);

Trise = 450*(Ptr_loss/At)^0.826;

 if (Window_w > TotalWindingWidth_paper) && (Kc <= 1.1*Ku) && (Kc >=
0.9*Ku) && (Ef_final >= 100) % Ef = 98.8
% fprintf ('% d[m^3], % d[kg], % d[W] % d[W], % d[W], % d[percent], % d, % d, %
d[A/mm^2], % d[A/mm^2], % d, % d \n',...
   %
Vol_tr,TotalW,Pcore,Pcon,Ptr_loss,Ef_final,N1,N2,Jp_e,Js_e,da_ratio,hw_ratio)

Transformer_Drawing
ires = ires + 1;
eval(['Results_Final.Result_', num2str(ires), ' = Results;']);
eval(['Results_Final.Bm_mag_', num2str(ires), ' = Bm_mag;']);

% Objective2= Ef_final/Vol_tr;
% Objective3= Ef_final/(Vol_tr*Trise);
% Objective4=
(Results.Pfe_core_h+Results.Pfe_core_e)/(Results.Culp+Results.Culs);
% Objective5_ 1=
(Results.Pfe_core_h+Results.Pfe_core_e)/(Results.Culp+Results.Culs)+(Lstray/Ef_fi
nal)/max(Lstray/Ef_final);
% Objective5_ 2=
(Results.Pfe_core_h+Results.Pfe_core_e)/(Results.Culp+Results.Culs)+(Lm/Ef_final
)/max(Lm/Ef_final);
% Objective6= Lstray/Trise;

% Input Parameters
Results_Final _Table(ires,1) = N1;
Results_Final _Table(ires,2) = Jp_e;
Results_Final _Table(ires,3) = Js_e;
Results_Final _Table(ires,4) = hw_ratio;
Results_Final _Table(ires,5) = da_ratio;
% Analytical Design Outputs
Results_Final _Table(ires,6) = Vol_tr;
Results_Final _Table(ires,7) = MLTp;
Results_Final _Table(ires,8) = MLTs;
Results_Final _Table(ires,9) = TLWp;
```

```
Results_Final _Table(ires,10) = TLWs;
Results_Final _Table(ires,11) = Ll_paper;
Results_Final _Table(ires,12) = L2_paper;
Results_Final _Table(ires,13) = Lstray;
Results_Final _Table(ires,14) = Lm;
Results_Final _Table(ires,15) = TotalW;
Results_Final _Table(ires,16) = Rp_ac;
Results_Final _Table(ires,17) = Rs_ac;
Results_Final _Table(ires,18) = Pcon_p;
Results_Final _Table(ires,19) = Pcon_s;
Results_Final _Table(ires,20) = Pcore;
Results_Final _Table(ires,21) = Im_peak;
Results_Final _Table(ires,22) = Im_rms;
Results_Final _Table(ires,23) = eff_Tr;
Results_Final _Table(ires,24) = Ef_final;
Results_Final _Table(ires,25) = Trise;
% FE Analysis Outputs
Results_Final _Table(ires,26) = Results.Bpeak;
Results_Final _Table(ires,27) = Results.BpeakA;
Results_Final _Table(ires,28) = Results.Brms;
Results_Final _Table(ires,29) = Results.Pfe_core_h;
Results_Final _Table(ires,30) = Results.Pfe_core_e;
Results_Final _Table(ires,31) = Results.Bmax;
Results_Final _Table(ires,32) = Results.Resp;
Results_Final _Table(ires,33) = Results.Ress;
Results_Final _Table(ires,34) = Results.Ipp;
Results_Final _Table(ires,35) = Results.Ips;
Results_Final _Table(ires,36) = Results.Epp;
Results_Final _Table(ires,37) = Results.Eps;
Results_Final _Table(ires,38) = Results.Culp;
Results_Final _Table(ires,39) = Results.Culs;
Results_Final _Table(ires,40) = Results.Fluxp;
Results_Final _Table(ires,41) = Results.Fluxs;
% FE Magnetizing Current Outputs
Results_Final _Table(ires,42) = Bm_mag.max1;
Results_Final _Table(ires,43) = Bm_mag.max2;
Results_Final _Table(ires,44) = Bm_mag.max;
Results_Final _Table(ires,45) = Imag_FE;

 end
            end
          end
        end
    end
end

% Input Parameters
Results_Final _Table _Disp(1,1) = {'N1'};
Results_Final _Table _Disp(1,2) = {'Jp_e'};
Results_Final _Table _Disp(1,3) = {'Js_e'};
```

```
Results_Final _Table _Disp(1,4) = {'hw_ratio'};
Results_Final _Table _Disp(1,5) = {'da_ratio'};
% Analytical Design Outputs
Results_Final _Table _Disp(1,6) = {'Vol_tr'};
Results_Final _Table _Disp(1,7) = {'MLTp'};
Results_Final _Table _Disp(1,8) = {'MLTs'};
Results_Final _Table _Disp(1,9) = {'TLWp'};
Results_Final _Table _Disp(1,10) = {'TLWs'};
Results_Final _Table _Disp(1,11) = {'Ll_paper'};
Results_Final _Table _Disp(1,12) = {'L2_paper'};
Results_Final _Table _Disp(1,13) = {'Lstray'};
Results_Final _Table _Disp(1,14) = {'Lm'};
Results_Final _Table _Disp(1,15) = {'TotalW'};
Results_Final _Table _Disp(1,16) = {'Rp_ac'};
Results_Final _Table _Disp(1,17) = {'Rs_ac'};
Results_Final _Table _Disp(1,18) = {'Pcon_p'};
Results_Final _Table _Disp(1,19) = {'Pcon_s'};
Results_Final _Table _Disp(1,20) = {'Pcore'};
Results_Final _Table _Disp(1,21) = {'Im_peak'};
Results_Final _Table _Disp(1,22) = {'Im_rms'};
Results_Final _Table _Disp(1,23) = {'eff_Tr'};
Results_Final _Table _Disp(1,24) = {'Ef_final'};
Results_Final _Table _Disp(1,25) = {'Trise'};
% FE Analysis Outputs
Results_Final _Table _Disp(1,26) = {'Results.Bpeak'};
Results_Final _Table _Disp(1,27) = {'Results.BpeakA'};
Results_Final _Table _Disp(1,28) = {'Results.Brms'};
Results_Final _Table _Disp(1,29) = {'Results.Pfe_core_h'};
Results_Final _Table _Disp(1,30) = {'Results.Pfe_core_e'};
Results_Final _Table _Disp(1,31) = {'Results.Bmax'};
Results_Final _Table _Disp(1,32) = {'Results.Resp'};
Results_Final _Table _Disp(1,33) = {'Results.Ress'};
Results_Final _Table _Disp(1,34) = {'Results.Ipp'};
Results_Final _Table _Disp(1,35) = {'Results.Ips'};
Results_Final _Table _Disp(1,36) = {'Results.Epp'};
Results_Final _Table _Disp(1,37) = {'Results.Eps'};
Results_Final _Table _Disp(1,38) = {'Results.Culp'};
Results_Final _Table _Disp(1,39) = {'Results.Culs'};
Results_Final _Table _Disp(1,40) = {'Results.Fluxp'};
Results_Final _Table _Disp(1,41) = {'Results.Fluxs'};
% FE Magnetizing Current Outputs
Results_Final _Table _Disp(1,42) = {'Bm_mag.max1'};
Results_Final _Table _Disp(1,43) = {'Bm_mag.max2'};
Results_Final _Table _Disp(1,44) = {'Bm_mag.max'};
Results_Final _Table _Disp(1,45) = {'Imag_FE'};
[row_res,col_res] = size(Results_Final _Table);

for i = 1:1:45
   for j = 1:1:row_res
      Results_Final _Table _Disp(j+1,i) = mat2cell(Results_Final _Table(j,i));
```

```
    end
end

%% Exit the Magnet

invoke(MN6, 'Exit');                                % Close the Magnet file
```

Appendix I

Measurement setup for core material characterisation

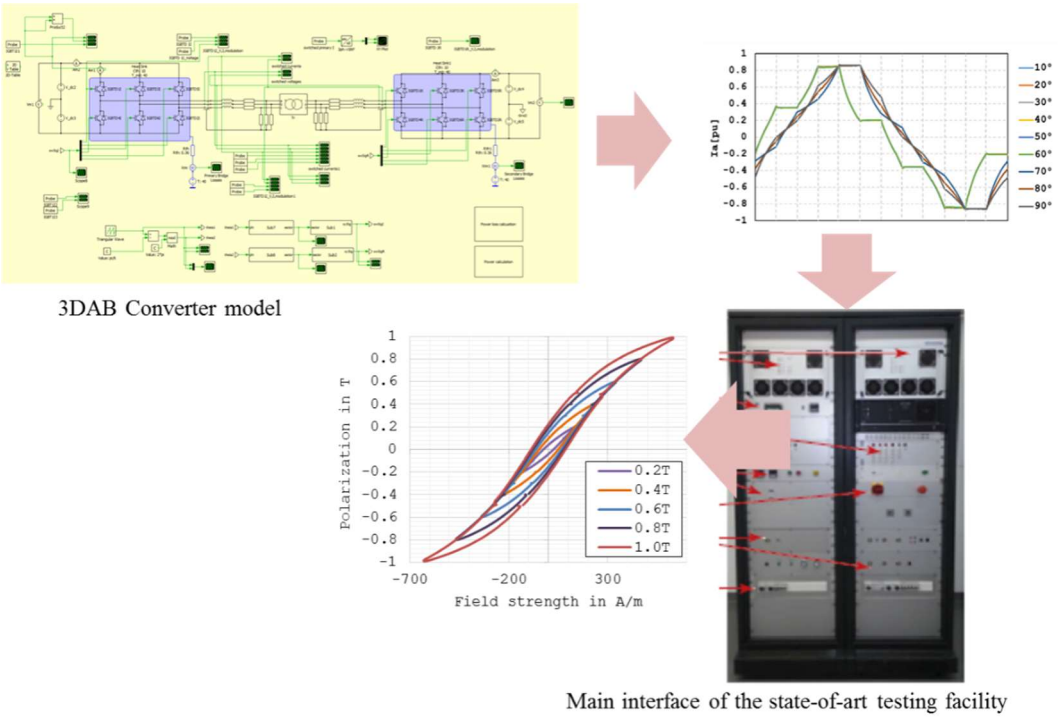


Figure I. 1 Core material characterisation measurement setup.

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