

Performance Improvement of Three-Level Neutral-Point-Clamped Electric-Starter-Generator System for More Electric Aircraft

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Abstract

The more-electric-aircraft concept is receiving more and more attention in the development of next-generation large, commercial aircraft due to its high reliability, low maintenance costs and good environmental impact. To satisfy these expectations, aerospace systems are undergoing a transition from pneumatic, hydraulic and mechanical power to electrical counterparts. With the help of cutting-edge active rectification technology, a cutting-edge aircraft electric starter-generator system tends to substitute the typical three-stage wound-field synchronous generator for avoiding mechanical failures, especially for high-speed operation. Since the three-level neutral-point-clamped (3L-NPC) converter plays an essential role in the energy conversion path, this thesis primarily focuses on the following advanced pulse-width-modulation (PWM) strategies that aim to enhance the reliability and efficiency of the entire system without any additional hardware.

- A fast PWM implementation approach is studied to simplify dwell-time calculation and sector/subsector identification, which is significant for lowing the cumbersome computational effort of the space vector modulation technique. Thus, all proposed modulation strategies are established based on this method.

- Because of the split DC-link capacitors, the 3L-NPC topology has an inherent neutral-point voltage imbalance problem. To address the disadvantage, a capacitor voltage balancing control method is developed based on the virtual-space-vector concept which exhibits superior neutral-point voltage balance performance compared with other modulation strategies.

- Given that voltage stress of the motor would be substantially increased when the common-mode voltage is imposed on machine terminals, and also its steep changes can induce damaging ground leakage, bearing currents and emission of common-mode noise, a modified virtual-space-vector modulation strategy is proposed, which can reduce the common-mode voltage in the drive systems.

- Considering the wide-speed range operation of the electric starter-generator system, a hybrid modulation process is designed according to the operating points of the target systems, which can attain switching loss reduction in motoring mode and common-mode voltage suppression in generation mode.

- In order to improve the three-level converter-fed high-speed aerospace drives' output electromagnetic torque capability and reduce additional machine copper losses caused by the large flux-weakening current, an advanced overmodulation strategy is proposed, together with the analysis of achievable modulation index, and the incorporation of an effective neutral-point voltage balancing control method.

Finally, the correctness of the theoretical analysis and the effectiveness of the proposed approaches are proved by both simulations and experimental results.

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List of Publications

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Conference Papers

[1] **F. Guo**, T. Yang, S. Bozhko and P. Wheeler, "3L-NPC AC-DC power converter using virtual space vector PWM with optimal switching sequence based

on *g-h* coordinate," in *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, Nottingham, 2018, pp. 1-7. doi: 10.1109/ESARS-ITEC.2018.8607586.

[2] **F. Guo**, T. Yang, S. Bozhko and P. Wheeler, "Open-Switch fault diagnosis for three-phase AC-DC power converter with Park's vector method considering modulation schemes," in *IEEE 12th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED)*, Toulouse, France, 2019, pp. 405-411. doi: 10.1109/DEMPED.2019.8864839.

[3] **F. Guo**, T. Yang, S. Bozhko and P. Wheeler, "A novel virtual space vector modulation scheme for three-level NPC power converter with neutral-point voltage balancing and common-mode voltage reduction for electric starter/generator system in more-electric-aircraft," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 1852-1858. doi: 10.1109/ECCE.2019.8913186.

[4] **F. Guo**, T. Yang, A. M. Diad, S. S. Yeoh, S. Bozhko and P. Wheeler, "A simple PWM strategy for 3L-NPC converters in aircraft electric starter/generator system with improved DC-link voltage utilization and reduced common-mode voltage," *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, Vancouver, BC, Canada. (*Accepted*)

List of Acronyms

AC	Alternating Current
AEGART	Aircraft Electrical Generation with Active Rectification Technology
AFE	Active-Front-End
AI	Artificial Intelligence
ANN	Artificial Neural Network
APU	Auxiliary Power Unit
AR	Active Rectifier
ATS	Air Turbine Starter
CBPWM	Carrier-Based Pulse-Width-Modulation
CFD	Computational Fluid Dynamics
CM	Common Mode
CSD	Constant Speed Drive
CF	Constant Frequency
CCS	Code Composer Studio
DC	Direct Current
DSVM	Discrete Space Vector Modulation
DPWM	Discontinuous Pulse-Width-Modulation
DNPC	Diode Neutral-Point-Clamped
DSK	Development Starter Kit

EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMF	Electromotive Force
ESG	Electric Starter-Generator
EV	Electric Vehicle
FE	Finite Element
FW	Flux-Weakening
FFT	Fast Fourier Transform
GUI	Graphic User Interface
HP	High Pressure
HVDC	High-Voltage Direct Current
HDL	Hardware Description Language
HPI	Host Port Interface
HBSVM	Hybrid Space Vector Modulation
HBC	Hexagonal-Boundary Compression
IGBT	Insulated-Gate Bipolar Transistor
IPM	Interior Mounted Permanent Magnet
IM	Induction Machine
IPBC	Inscribed Polygonal-Boundary Compression
KVL	Kirchhoff's Voltage Law
KCL	Kirchhoff's Current Law
LP	Low Pressure

LVRT	Low-Voltage-Ride-Through
LM	Linear Modulation
MEA	More-Electric-Aircraft
MTPA	Maximum Torque Per Amp
M^2PC	Modulated Model Predictive Control
MPPT	Maximum Power Point Tracking
MPC	Model-Predictive-Control
MI	Modulation Index
NP	Neutral-Point
NTV	Nearest-Three-Space-Vector
NTV^2	Nearest-Three-Virtual-Space-Vector
$OM-I$	Overmodulation Mode-I
$OM-II$	Overmodulation Mode-II
PI	Proportional-Integral
PF	Power Factor
PMSM	Permanent Magnet Synchronous Machine
PMM	Permanent Magnet Machine
PWM	Pulse-Width-Modulation
PV	Photovoltaic
RMS	Root Mean Square
R	Resistance Value
STV	Selected Three Vector

SPM	Surface Mounted Permanent Magnet
SRM	Switched Reluctance Machine
S/G	Starter/Generator
SPWM	Sinusoidal Pulse-Width-Modulation
SVD	Space Vector Diagram
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
TNPC	T-Type Neutral-Point-Clamped
VSV	Virtual Space Vector
VF	Variable Frequency
VSD	Variable Speed Drive
VSCF	Variable Speed Constant Frequency
VSVF	Variable Speed Variable Frequency
WFSM	Wound Field Synchronous Machine
WBG	Wide-Band-Gap
WTHD	Weighted Total Harmonic Distortion
ZSV	Zero-Sequence Voltage

List of Symbols

$A_{c.c}$	Active control capability
C	DC-Link capacitor
ΔQ	Compensated electric charge
i_{dc}	DC-Link current
L_d	d-axis inductance
L_q	q-axis inductance
$T_{\boldsymbol{em}}$	Electromagnetic torque
ω_e	Electrical angular frequency
θ_c	Crossover angle
λ	Compression coefficient
θ_h	Holding angle
ψ_f	Magnet flux linkage
i_{np}	Neutral-point current
n_p	Pole pairs
i_{ch}	Characteristic current
V_{ref}	Reference space voltage vector
$3L - NPC$	Three-level neutral-point-clamped
$V_{DC} - H$	Upper-side DC-link capacitor
$V_{DC} - L$	Lower-side DC-link capacitor

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Chapter 1

Introduction

In this Chapter, the motivations and objectives of this research work are presented. The conventional aircraft and the more-electric-aircraft (MEA) are compared ranging from the framework of electrical power systems to power source distribution. In addition, the cutting-edge starter-generator concept is briefly introduced for future MEA applications.

1.1 Research Background

Over past decades, commercial aircraft has been widely chosen as the favourite way of long distance travel, and high-speed flight becomes an attractive trend of transportation. As a result, the aerospace industry is growing at an increasing rate. Although the aviation industry has been impacting greatly by the spread of Covid-19, by the year 2030, it is estimated that there will be around 27,000 new aircraft in the sky [1].

However, it should be noted that aircraft have environmental and climate impacts that depend on their fuel efficiency. Aircraft are also relatively noisy compared with other forms of travel. In the competitive world of airline economics, where low-cost carriers are driving down profit margins on airline seat-miles, techniques for reducing the environmental impact and direct operating costs of aircraft are in

great demand [1].

The aerospace industry is continuing with its plans to make the aircraft more-electric aiming for increasing fuel efficiency, reliability and reducing audible noise [2]. Therefore, onboard aircraft electrical systems have substituted mechanical, hydraulic and pneumatic systems in cutting-edge commercial aircrafts, such as the Boeing 787 and the Airbus A380 [3–5].

Electrical systems are now employed for aircraft actuation systems, wing ice protection systems, environmental control systems and fuel pumping [6]. This increase in electrical energy use has led to a demand for rapid technology development, particularly in power electronics which is one of the most essential technologies for the MEA [5, 7–9]. Without the use of power electronics to convert and control electrical energy, few of the desirable benefits would be realized. Currently, aerospace applications present some challenging operating conditions for power electronics, and there are still a number of areas where performance improvements of power converters must be made. The operating environment on an aircraft can be very harsh, and the hours of operation and expected lifetime are long compared with many industrial and automotive applications. It implies the reliability issue is vital for the systems.

Consequently, the MEA concept can potentially lead to a significant reduction in the dependency on fossil fuels and pollutant emissions as the electrification technologies expedite a paradigm shift towards more sustainable air travel. More detailed information will be presented in the following Sections.

1.2 Conventional Aircraft

The primary power source of the existing aircraft comes from the gas turbine engines shown in Figure 1.1. As can be seen, the energy sources required to drive onboard power systems are produced by the aircraft engine. The jet fuel is used for producing propulsive power, and a small percentage of the fuel energy is converted into mechanical, pneumatic, hydraulic, and electrical power. These different types of power sources are used for loads onboard the aircraft as follows:

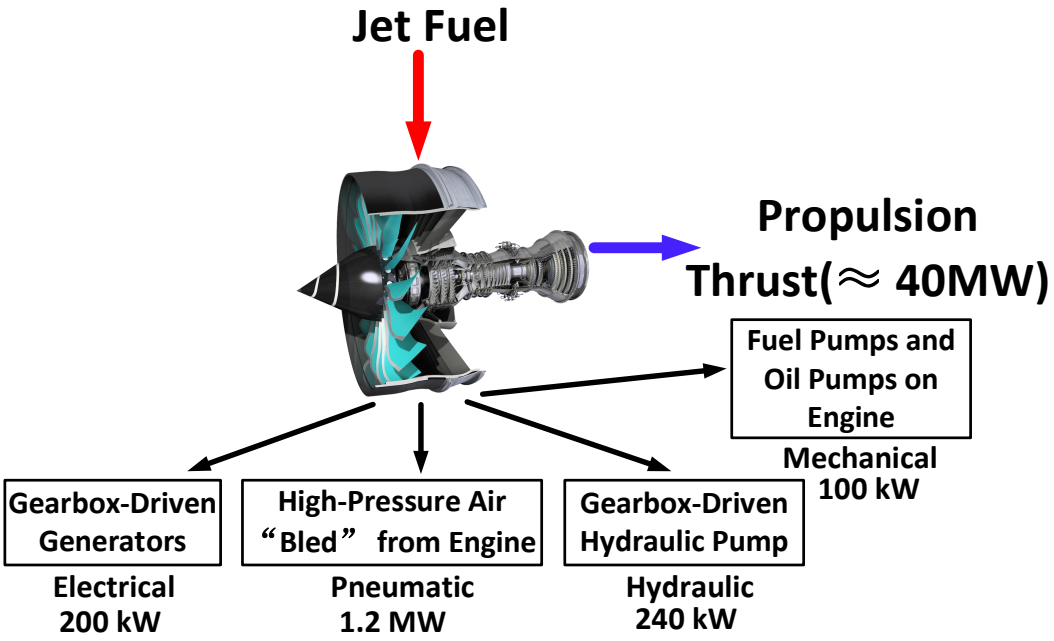


Figure 1.1: The power systems on a typical large commercial aircraft [1]

- Pneumatic power drives the environmental control system and supplies hot air for wing ice protection systems that include two working modes: anti-icing and de-icing [10]. The former one is pre-emptive and is turned on before the flight enters icing conditions. The latter one is the de-icing mode, which is reactive and used after there has been significant ice built up. It should be pointed out that the main drawbacks of pneumatic power are high installation cost and difficulty in detecting leaks [11].

- Mechanical power is extracted via a shaft that is driven by the aircraft engine, and then distributed via a gearbox. This gearbox drives hydraulic pumps to generate hydraulic power that is then distributed to the flight actuators and landing gears, etc. [10].

- Hydraulic power is transferred from the central hydraulic pump to the actuation systems for primary and secondary flight control and to the landing gear for deployment, reaction and braking. Hydraulic systems have a very high power density and are very robust. However, heavy and inflexible infrastructure and the potential leakage of dangerous and corrosive liquids are the main drawbacks.

- Electrical power is generated from electrical machines coupled to an accessory gearbox. It is utilized to power electrical loads, such as flight control equipment, lighting and galleys. An auxiliary power unit (APU) generator is located at the rear of the aircraft to provide electrical power when the aircraft is on the ground, and also is applied to assist during the main engine startup process. It is known from Figure 1.1 that electrical power in conventional aircraft accounts for a small volume amongst all power sources in conventional aircraft.

In contrast to the deficiencies of pneumatic, hydraulic and mechanical power, the electrical power system has many superiorities, such as low maintenance, high efficiency and good controllability, etc. With the help of the above advantages, the use of more electrical power becomes an inevitable trend. The more-electric-aircraft (MEA) concept is therefore proposed, which aims at increased penetration of electrical power in aircraft systems and becoming a major trend in the next-generation aerospace industry [6].

1.3 More Electric Aircraft

A possible electric power flow distribution of the MEA is shown in Figure 1.2. As can be seen, the aim is that all of the onboard loads are driven by the electric power from an electrical system. It is clear that by integrating all secondary power sources into one, not only the hydraulic pipes and gas ducts are removed from the aircraft, but also the electrical power source simplifies the aircraft engine structure. More importantly, electrical systems offer far more options for reconfigurability as well as for advanced prognostics and diagnostics. These prognostics and diagnostics systems could help improve aircraft availability and reduce the need for unscheduled maintenance [5].

According to this novel system architecture, the essential benefits of the MEA, compared with the traditional aircraft, can be summarised as follows:

1) Due to the removal of hydraulic and pneumatic systems, these bulky systems in the traditional aircraft are simplified and costly maintenance fees are decreased

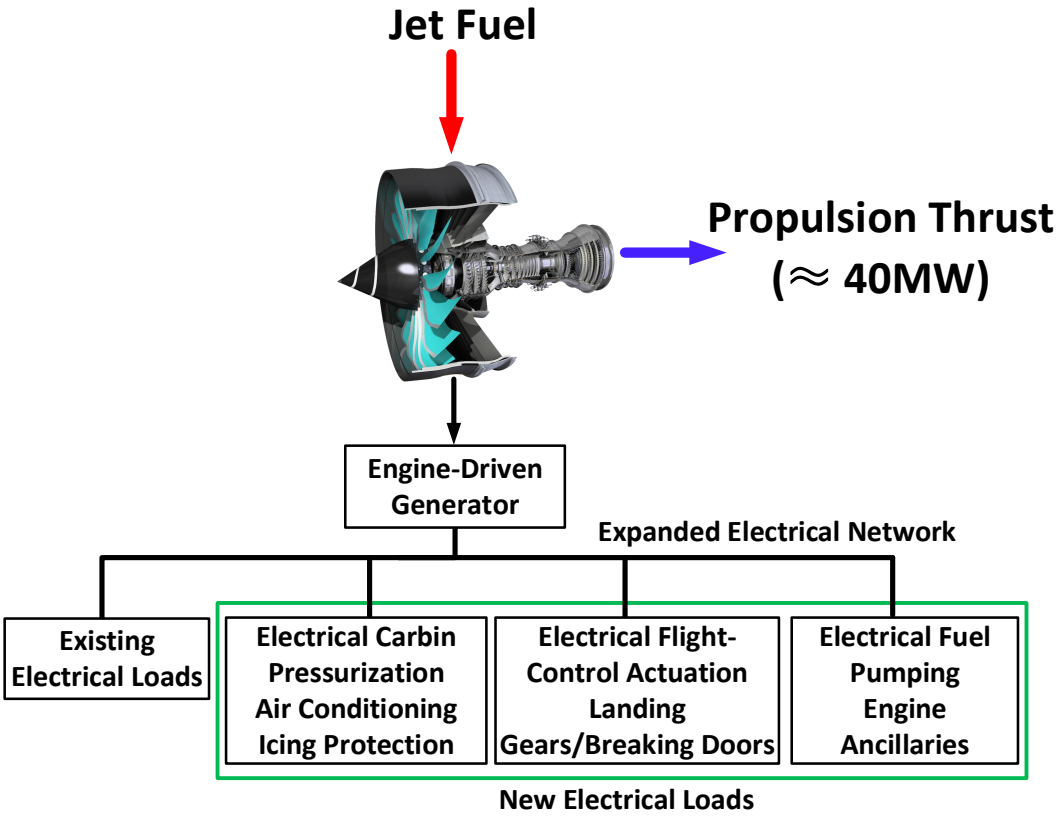


Figure 1.2: The power sources distribution of the MEA

to an acceptable level. Hence, this method reduces the overall weight, extra cost and complexity of the existing systems [11]. As a consequence, the efficiency of the entire system is improved and the flight range is expanded.

2) A fan shaft generator is employed for emergency power generation rather than an inefficient ram air turbine (RAT). This can enhance system reliability and robustness against the engine contingency.

3) Replacement of the engine-bleed system by electric motor-driven pumps reduces the complexity and installation cost, and improves the engine startup efficiency.

4) Use of an electrical starter/generator (S/G) for the starting process of the aero-engine. If the S/G is embedded in the engine, this eliminates the engine tower shaft and gears, power take-off shaft, accessory gearboxes and reduces the engine starting power, particularly in cold conditions and aircraft front area.

Table 1.1: Comparison of typical power levels between a conventional aircraft and the MEA [3, 4]

Power User	Thrust (MW)	Electrical (kW)	Pneumatic (kW)	Hydraulic (kW)	Mechanical (kW)
Airbus A330	40	200	1200	240	100
MEA	40	1000	0	0	0

It can conclude that adopting the MEA will reform the aerospace industry thoroughly. With the help of the enhancements regarding weight, cost, and fuel consumption, better maintainability and high reliability will be attained at the same time. On the other hand, the electrical S/G system investigated in this study will determine the performance improvement for the MEA.

The comparison of typical power levels between a conventional aircraft (e.g. Airbus A330) and the MEA is detailed in Table 1.1. The result indicates that the total non-thrust power of conventional aircraft is approximately 1.74MW, 74% higher than that of the MEA, while both thrust power equals 40MW [4].

1.3.1 Starter-Generator Concept

The state-of-the-art aircraft S/G systems normally use a three-stage wound-field synchronous generator. This type of machine has been extensively employed in fixed-wing and rotorcraft applications. It has been demonstrated to be highly reliable and safe. Within aircraft, the exciter is adopted as a starter [12], and stator windings of the exciter are designed for higher currents than the required power generation [2]. Therefore, this design cannot be regarded as optimal. The typical three-stage S/G possesses several disadvantages and constraints as follows [3]:

1. It utilises a very different control algorithm for processing both the starter mode and the power generation mode, thereby constraining the system design and leading to complexity issues.

2. It can hardly operate over a rotation speed of 20krpm under power generating conditions as its wound rotors are embedded with rotating diodes. Operating

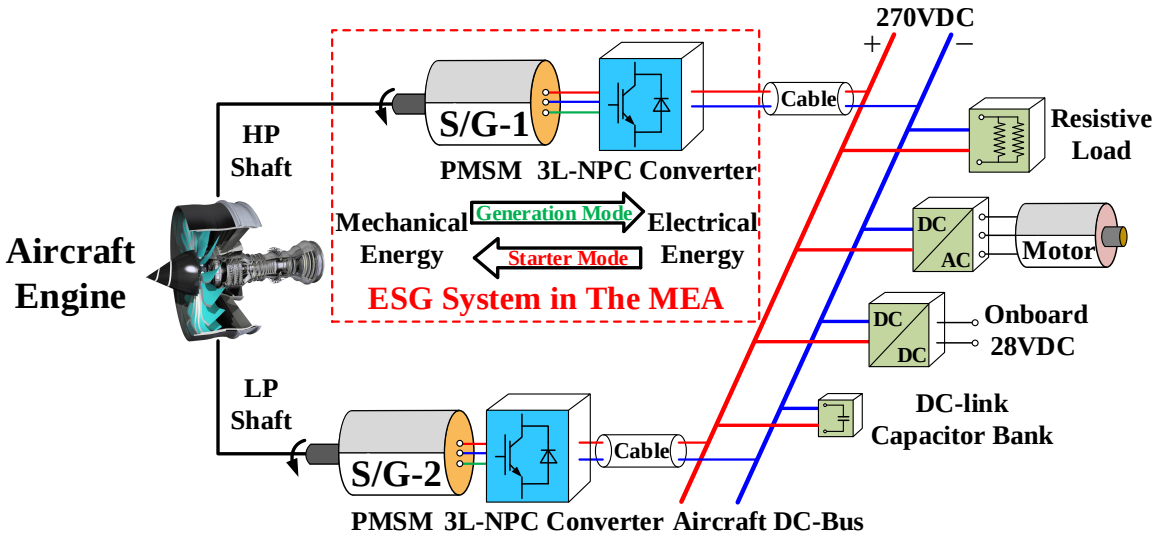


Figure 1.3: Configuration of the ESG system for the MEA

at a high speed might cause mechanical failure of the S/G systems.

The startup process of the current large civil aircraft jet engine needs assistance from a starter to provide a smooth acceleration until the engine achieves a self-sustaining speed. For example, air starter motors run with air supplied from a ground cart or APU to rotate the starter turbine which drives the aircraft engine. When the engine obtains a certain threshold speed, the air compressors can channel sufficient bleed air for the ignition process to accelerate the engine speed further. The engine power is then harnessed and distributed through the accessory gearbox for different types of power sources.

In contrast, the most core idea of the power generation unit for the MEA is the integration of multiple functions in one system for reducing aircraft mass that would result in additional fuel consumption [11, 13], where a key development brought by this concept is the aircraft S/G scheme. With the help of the advanced active rectification technology, the next-generation electric S/G (ESG) system involves a simpler connection between the electrical machine and the engine [2], which has the potential to greatly reduce the complexity of the power system. By using active rectifiers (ARs), two sets of S/G directly take power from the main engine through high pressure (HP) shaft and low pressure (LP) shaft, and operate in parallel to

transfer the power to future aircraft direct-current (DC) bus, as illustrated in Figure 1.3. Besides, it is known that high-voltage DC (HVDC) distribution systems, owing to reduced power loss and bipolar transmission, are applied in many industrial applications. Therefore, different architectures have been proposed, such as single bus, multi-bus and ring bus configuration. Due to the simplicity, such a "single bus" electrical power system (EPS) architecture is one of the promising candidates for future MEA [6]. Twin engine-driven generators provide electrical power to the single DC bus through AR-controlled S/G.

To be more specific, a high-speed machine is mechanically coupled to the engine shaft via a gearbox, and electrically connected with a bi-directional converter that interfaces the S/G system to the onboard EPS. For our case, a 6-poles 36-slots permanent magnet synchronous machine (PMSM) is chosen due to its high torque-to-current ratio, high power density and the lowest eddy-current losses on the rotor [2]. Thanks to lower voltage stress across switching devices, mitigated electromagnetic interference (EMI) emission, reduced dv/dt and better output harmonics, compared with two-level converter, the three-level neutral-point-clamped (3L-NPC) topology is chosen as an energy conversion kit for the developed S/G systems [2].

During the engine startup process, the converter runs as an inverter that drives the PMSM to crank and accelerate the engine shaft. When rotation speed reaches a self-sustained speed, the engine is ignited. After that, the ESG system goes into standby mode, followed by generation mode when the PMSM shaft speed (linked to the engine speed via gearbox ratio) approaches 20krpm. In generation mode, the engine drives the PMSM to generate electrical power, and the 3L-NPC converter is operated as a rectifier to convert this variable-frequency alternating current (AC) power into DC and to supply the onboard EPS. It is clear that the functionality of the starter has been electrically replaced by a high-speed electric motor, therefore, the weight and volume can be effectively reduced. The research work of this thesis is part of the AEGART project and more specifications can be found in [14].

Detailed explanation of aircraft starter and power generation systems will be presented in Chapter 2.

1.4 Aims and Objectives of the Thesis

Since the 3L-NPC converter serves as a significant component in the main path of energy flow in the aircraft ESG system, its operating performance has a significant influence on the reliability and efficiency of the onboard EPS. On the other hand, it is worth noting that the output variables of the converter highly depend on the switching patterns turning on and off the semiconductors. Thus, the aims of this thesis lie in the investigation of enhanced pulse-width-modulation (PWM) strategies for future three-level neutral-point-clamped electric S/G systems of the MEA.

The specific objectives are elaborated as follows:

1. To develop an advanced modulation technique that can successfully tackle the problem of capacitor voltage imbalance. As the selected topology has an inherent problem of unbalanced neutral-point (NP) voltage due to the split DC-link capacitor bank, the diverged capacitor voltages and low-frequency NP potential fluctuation lead to the distorted line-to-line voltage on the motor side and extra over-stress across switching devices. Even though the self-balancing phenomenon might take effect sometimes, its strength is constrained by system parameters, PWM patterns and sampling frequency, etc.

2. To develop an advanced modulation technique that can successfully address the issue of high common-mode voltage (CMV) in aerospace motor drive systems. This is due to the CMV generated by modulation scheme with switching states is the source of motor shaft voltage, its high magnitude causes a winding insulation problem by resultant bearing currents. It indicates that the CMV should be reduced to improve the reliability of the high-speed aerospace drives.

3. To develop an advanced modulation technique that can successfully resolve the problem of converter's limited output capability and extra motor's copper loss with a lower DC bus voltage. According to the standard of MIL-STD-704F, referred to [15], the 3L-NPC converter interfaced with a definite 270VDC bus might be subjected to large back electromotive force (EMF) in the high-

speed operation region. Also, the output electromagnetic torque is constrained. Although the flux-weakening control can allow that EMF is within the converter limits, large copper losses are inevitable. Therefore, it is of interest to design a novel modulation algorithm to extend the ESG system's operating points into the overmodulation region.

4. To develop a simple PWM calculation approach that can successfully improve the algorithmic efficiency of the introduced strategies. The simplified modulation strategy is a crucial task for overcoming the computational burden in digital control systems. Although the resultant firing pulses are the same as those traditional determination solutions, the modulation process can be executed in a simple way, which is particularly favourable for high switching frequency applications.

   Despite the fact that the research work focuses on aircraft onboard AC/DC power conversion systems, the techniques proposed in this thesis can be applied in other industrial applications as well, such as grid-connected power conversion systems and electric vehicles (EVs), etc.

1.5 Structure of Thesis

This thesis is structured as follows:

Chapter 2 presents detailed information on the aircraft electric starter-generator system addressed in this study. The adopted variable speed variable frequency topology is discussed. Since a bi-directional power electronics converter serves as a key component in the target systems, a literature review of the commonly-used multilevel topologies is carried out. Moreover, the functionality of the applied 3L-NPC converter is investigated from space vector generation to mathematical model in detail.

Chapter 3 presents the conventional modulation schemes. The source of capacitor voltage imbalance and NP potential ripple are analysed. These demerits become a motivation for the performance improvement of the proposed methods presented in

the following Chapters. Besides, the existing NP voltage balancing control methods are reviewed, together with a plotted map of the modulation tree.

Chapter 4 introduces a fast calculation approach to reduce the massive computational burden caused by complex PWM algorithms under the α-β reference frame. The optimization embraces the simple implementation of dwell time determination and sector/subsector identification. With this new space vector plane, the algorithmic efficiency can be significantly improved. Noted that the proposed modulation strategies in this thesis are all established based on this solution.

Chapter 5 proposes two types of the modified modulation schemes for enhanced performance of the 3L-NPC converter. The first one manipulates the duty cycles of small vectors for keeping two capacitor voltages balanced in case an initial NP voltage imbalance exists. To reduce CMV magnitude, the original virtual-space-vector PWM scheme is optimized from a lower CMV-related switching state perspective, which forms the basis of the second-type modified modulation strategy.

Chapter 6 considers a hybrid modulation algorithm for the wide-speed range operation of ESG system starting from standstill to the power generating conditions. To reduce the switching losses of the three-level modulation mode, the seven-segment PWM pulse trains are adopted in motoring mode. This is because, during this period, the modulation index and power factor do not fulfill the conditions for the NP voltage imbalance-prone region. In accordance with the operational characteristics of the developed ESG system, however, the NP voltage deviation and fluctuation problems become worse in power generation mode, i.e., for high modulation index and low power factor operating points. Thus, these deficiencies must be overcome in generation mode. Similar to the CMV reduction technique presented in Chapter 5, CMV suppression is also considered for the proposed hybrid PWM strategy.

Chapter 7 explores an overmodulation technique for this converter-fed aerospace drives. This is due to the DC-link voltage utilization ratio of current onboard EPS is limited by 270VDC. If overmodulation conditions are satisfied, a higher modulation index can be achieved. The boosted DC-link voltage utilization ratio benefits for lowering large flux-weakening current, gaining better output electromagnetic torque

and reducing copper losses on the machine. To obtain a higher fundamental component for the converter's output voltage, the trajectory of reference voltage vector is carefully designed, together with a corresponding NP voltage balancing control method. A representative overmodulation algorithm is chosen as the benchmark to compare and evaluate the modulation performance of the proposed technique.

Chapter 8 summarises the main conclusions and contributions of this thesis. The possible future work is also presented in this Chapter.

In order to validate the correctness and feasibility of the advanced modulation strategies proposed in Chapters 5-7 of the thesis, firstly, the PWM algorithms are tested by simulation, followed by the experimental verification that is conducted on the laboratory-built aircraft ESG prototype system. All results are given in the last Section of each Chapter.

1.6 Conclusions

In this Chapter, the onboard EPS of the conventional aircraft and the MEA concept has been introduced. Since the secondary power sources are substituted by electrical counterparts, future aircraft brings an opportunity to gain low fuel consumption, better environmental impact, less maintenance cost and comfortable flighting experience. Considering the disadvantages of the present S/G system, one of the promising tendencies is to electrify aircraft. Therefore, in order to realize onboard electrification more efficiently and reliably, the power electronics converter of the ESG system playing as a crucial component must work in a high-performance way, and the thesis shall focus on the dedicated PWM algorithms for the studied 3L-NPC converter-fed aerospace drive applications. In addition to presenting the aims and objectives of this thesis, the structure of the thesis has been detailed in this Chapter.

Chapter 2

Electric Starter-Generator Systems in the MEA

This Chapter discusses the state-of-the-art in aircraft S/G systems and introduces the developed ESG system for the MEA, which is based on a PMSM controlled by an active rectifier. Since the 3L-NPC converter is selected as a core topology candidate for the target systems, the operational principle, space vector generation, commutation paths and mathematical model for this topology are presented before introducing the improved modulation techniques developed in this work.

2.1 Aircraft Engine Starter

The primary source of power for an aircraft comes from the engine, which makes human beings' dreams of flight become true. In the early of 19^{th} century, the steam-powered engine was considered for aircraft as it has been successfully applied to ships, trains and vehicles. But, steam-powered engines did not flourish because of power density issues and problems related to keeping the burner operational with high wind speeds. In the late 19^{th} century, the combustion aircraft engine was invented to address these problems since this type of engine provides much better power density than the steam variant, which secured the future of manned flight.

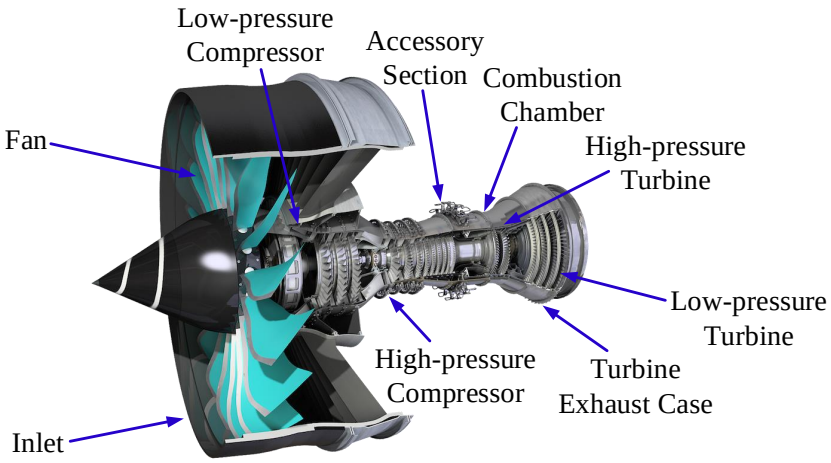


Figure 2.1: Typical aircraft turbofan engine

At that time, the engines were driven by pistons, much like the ones in modern automotive vehicles [16]. At the end of World War-II, the jet engine emerges and provides good performance because the flight speed and range were both increased [17]. Nowadays, aircraft turbofan and turbojet type gas turbine engines are two commonly-used power sources of aircraft. It should be pointed out that the main discrepancy of these jet engines is that turbofan engines do not fully use all of the air that flows into the engine. This structure mainly consists of air compressors, a combustion chamber and a turbine, as shown in Figure 2.1. The operational procedures are listed as follows:

1. In order to increase the kinetic energy, air passing through the engine is accelerated by the compressor. Its functionality is to increase the air pressure for improving the speed of the air. The part of air flows into the engine by passing through the low-pressure (LP) compressor. After that, the air is compressed further through the high-pressure (HP) compressor. Eventually, it will be sent to the combustion chamber.

2. The compressed air flows into the combustion chamber along with mixed jet fuel and is ignited. As a result, the combustion process generates propulsive force, thus accelerating the aircraft forward [18].

3. The combusted air then expands and goes into the turbine which then causes

it to rotate faster which is attached to the input fan which in turn compresses more air. With the help of a nozzle, the exhaust is channelled out of the engine. This turbine provides mechanical power to the compressor in order to keep it spinning, and to the accessory gearbox for power distribution.

2.1.1 Aircraft Engine Startup Process

When the engine compressors are rotating, the desired thrust can be generated with the three steps mentioned above. However, air needs to be forced into the engine at standstill for starting air compression and combustion. As a result, a starter system is required to assist with the engine for the startup process [18]. Noteworthy, the function of the starter system is to bring the engine to a certain speed, in which the startup process can proceed more efficiently. For traditional civil aircraft, the starter motor aims to provide high torque and accelerate the engine speed to a self-sustaining speed.

Typically, an aircraft engine requires two steps to accomplish the startup process [18]. First of all, the air compressor and turbine are needed for the speed acceleration so that the fuel to air ratio is optimal. Secondly, the mixture of air and fuel is ignited in the combustion chamber.

The sequence of engine startup process in conventional aircraft can be summarized as follows:

1) Engine compressor spools are rotated by the action of a large volume of compressed air acting directly on the compressor blades, then air starts to flow into the engine from the inlet.

2) When the speed approaches approximately 10% of the engine's maximum speed, jet fuel is injected into the combustion chamber.

3) The air and fuel mixture is ignited in order to aid the engine to reach self-sustaining speed.

4) The starter mission is completed when a self-sustaining speed is attained. After

that, the engine continues to accelerate by itself until the idle speed that is about 60% of the engine's maximum speed is reached.

2.1.2 Aircraft Engine Startup Method

In terms of the conventional engine startup, pneumatic power is widely applied in aircraft [18]. To be more exact, the APU is employed to inject a compressed air for the main engines to accelerate it. This process is done through air ducts. It is notable that there is an air turbine starter (ATS) inside the engine nacelle which serves as a pneumatic motor to spin the engine. When the rotation speed reaches a certain speed, the air and fuel mixture in the combustion chambers is ignited to aid the engine to reach self-sustaining speed. After that, the starter circuit is disabled. The engine continues to accelerate by itself until the idle speed is reached. This completes the engine startup process [19]. With the pneumatic connection between other engines, air ducts are used to start them. However, the APU may not work properly with the reduced air density due to high altitudes. Furthermore, it may not have enough power generation to supply such compressed air. To handle this issue, the ground cart is adopted as an alternative approach for the APU, which can provide compressed air to the main engine while on the ground.

The gas-powered starter is another choice to drive the engine until it reaches the desired speed. It works through combusting fuel. At the same time, the exhaust which is produced as a result of combustion is channelled to a free-power turbine. When a self-sustaining speed is achieved, a mechanism will disconnect the starter. Because it has its own fuel and ignition system, starting system and self-contained oil systems. This type of starter system is economical to operate and provides a high power output for a comparatively low weight [18].

In addition, aircraft engines can be driven by an electrical starter. Typically, a DC motor is adopted and operates by means of an onboard DC bus or ground power supply. When the engine approaches a self-sustaining speed, the power supply of the electrical starter is cut off [18]. The merit of using an electrical-based starter is that also the power generated as a result of being driven by the engine could be sent back

to the aircraft bus. Consequently, this can enable the S/G concept that is based on a single electrical machine performing both starter and generator functions.

2.2 Aircraft Engine Power Generation

Electrical power generation has made significant progress ever since aircraft become more dependent on electrical loads. DC machines were introduced as generators when aircraft started using electrical-powered flight controls. The DC power output is transferred via a device called a commutator which enables the output power to the loads and is supported by on-board batteries to maintain the voltage level. Then, the introduction of V-Bombers during World War-II, with their greater electrical power requirements, led to a radical change in aircraft power generation systems [3]. It utilised four AC generators connected to four separate engines, which were used to power loads such as radar and electronic jamming equipment. The AC generators generated sine wave output voltages at constant frequency and were distributed to the electrical loads directly.

For commercial aircraft, each engine employs one generator to achieve electrical generation when it reaches normal operation during the cruise. However, there could be more than one generator connected to each engine in some type of aircraft. Another source of onboard electrical power is the APU which is essentially a small gas turbine-driven generator, thereby using it as an additional (or secondary) aircraft power source. Typically, the APU provides power when the aircraft is on the ground and can also deliver power in case emergency conditions unexpectedly occurs in the air.

The next subsection will review the electric power generation system topologies and operational principles for the existing and future MEA.

2.2.1 Power Generation Topologies

- Constant Frequency (CF)

  In the 1960s, the 115VAC at 400Hz constant frequency (CF) aircraft electri-

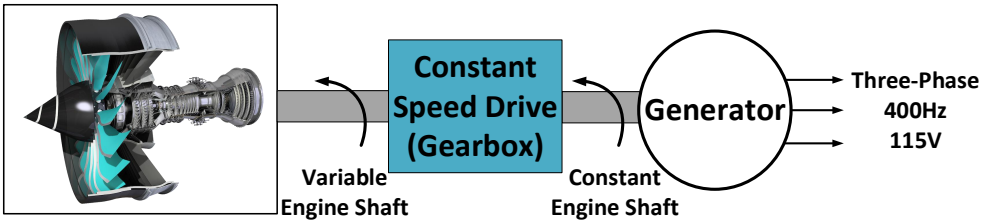
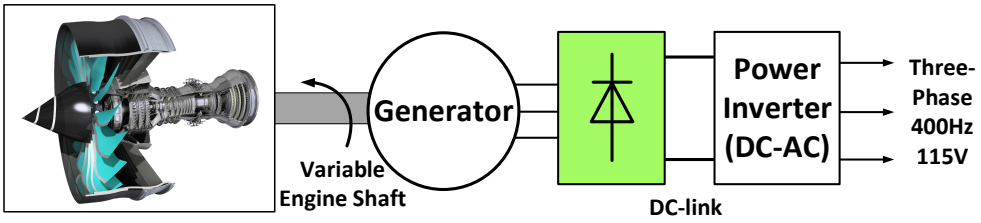
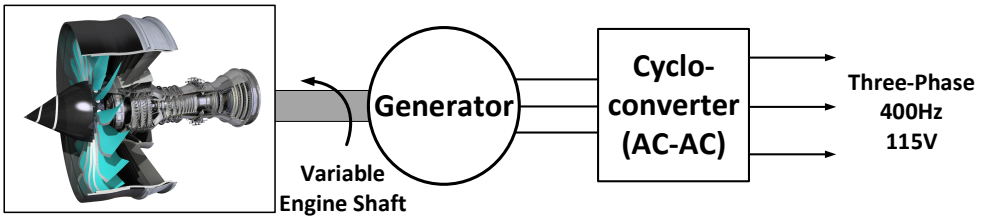


Figure 2.2: Constant frequency generation system topology



(a)



(b)

Figure 2.3: Variable speed constant frequency generation system topology with (a) diode rectifier and (b) cycloconverter

cal system appears. This topology has been widely used in many commercial aircraft, such as A320, A330 and B747 [3]. As the aircraft engine is operating at a wide-speed range, the generator is connected to the main engine via the accessory gearbox, as shown in Figure 2.2, which ensures constant output speed irrespective of the engine speed. The generated AC power is distributed to the aircraft electrical loads. However, extra cost and maintenance fees of this gearbox would be expected. Hence, this complex configuration is not economical for future aircraft.

- Variable Speed Constant Frequency (VSCF)

  The VSCF topology is similar to the CF topology as three-phase AC power with constant frequency is produced regardless of variable shaft speed. The difference is that a power electronics converter is applied to improve efficiency.

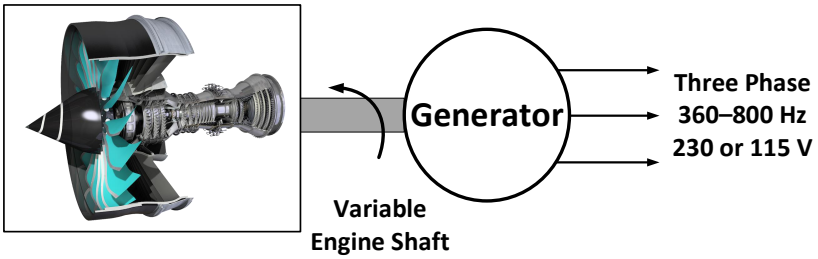


Figure 2.4: Variable speed variable frequency topology

As shown in Figure 2.3(a), in order to feed the DC-link, the diode rectifier is used to convert the variable AC electrical power. After that, a DC-AC inverter converts this DC into a three-phase AC of the onboard power system. To simplify the structure of the system, AC-AC converter, such as cycloconverter shown in Figure 2.3(b), matrix converter and back-to-back converter, can be directly applied to convert variable frequency electrical power coming from generator into fixed-frequency AC power. Currently, the VSCF topology with a cycloconverter mainly serves on military aircraft.

This power generation topology with a DC-link has been used in existing aircraft [3], such as the B777 and MD-90. Since the DC-link is beneficial for feeding high voltage loads, it provides an opportunity to charge onborad batteries through DC/DC converters. Nonetheless, the bulky DC-link capacitor makes the system become larger and weightier.

Noteworthy, the topology has the advantage due to the removal of the constant speed drive (CSD) gearbox between the gas turbine shaft and the generator. However, it should be pointed out that the power electronics converter must process all the generated power. Thus, full power rating and high reliability are needed in order to get the required level of safety from the aircraft design.

- Variable Speed Variable Frequency (VSVF)

  As shown in Figure 2.4, the generator is directly linked to the engine shaft via a variable speed drive (VSD), thus, the electrical system and loads can be adapted to operate with a variable frequency (VF), which is also known

as "frequency-wild" systems. The electrical output of the generator supplies a variable-frequency power with 360∼800Hz and the frequency is related to the speed of the gas turbine [20]. Such a wide VF range affects frequency sensitive aircraft loads, such as the AC electric motors. When fed electrical power directly from the generator, the motor speed is dependent on the frequency of the AC power. Obviously, the advantage of VSVF is the direct connection between the generator and the electrical power system, thereby offering a very simple and reliable potentiality for the implementation [3]. However, its drawback is that nearly all aircraft loads will require power converters for control as the VF supply cannot be used directly by some onboard loads.

In order to provide suitable electrical power for some onboard loads, the variable-frequency AC voltages need to be controlled by a high-performance AC-DC power converter. The VSVF topology has been widely used for business jets and has recently been adopted for larger-sized commercial aircraft, such as the A350, A380 and B787. Among them, the voltage is regulated at either 115VAC (A380 & A350) or 230VAC (B787), and its frequency changes with the engine speed and typically ranges from 320Hz to 800Hz. The above changes result in establishing power conversion for many loads, including motor drives. As a consequence, localised power electronic converters are needed.

2.2.2 Electrical Machines

The electrical machine plays an essential role in the energy conversion from the aircraft engine into the electrical power required by onboard systems and loads. According to the harsh operating conditions and undesirable environment, several types of electrical machines have been considered for aircraft power systems. There are wound field synchronous machine (WFSM), induction machine (IM), switched reluctance machine (SRM) and permanent magnet machine (PMM) [21], [22].

- Wound Field Synchronous Machine (WFSM)

  With the evolution of AC generators over the decades, the three-stage wound

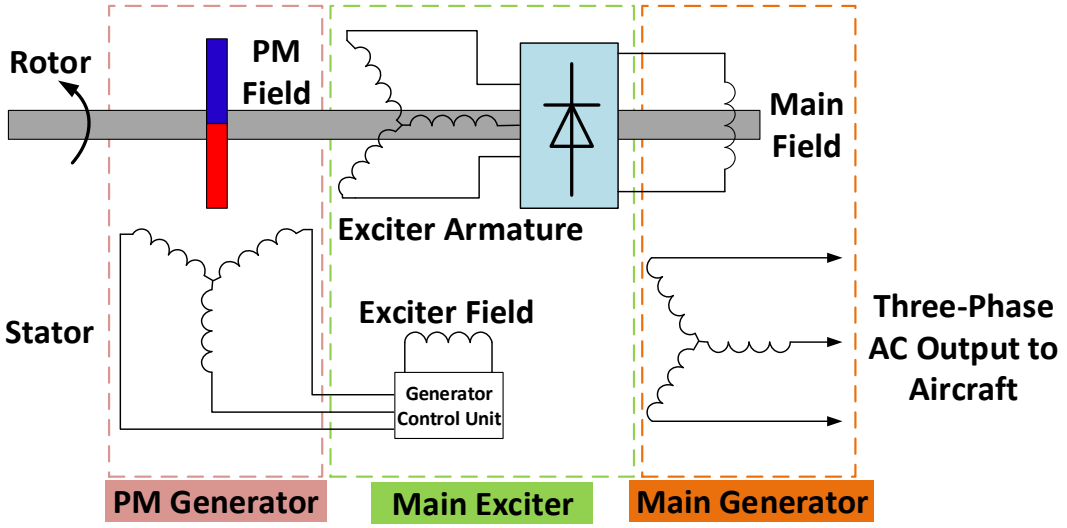


Figure 2.5: Diagram of three-stage wound field synchronous machine

field synchronous machine is not the present state-of-the-art for generating power. In accordance with the equivalent electrical circuit, as shown in Figure 2.5, it can be decomposed by three machines that share the same rotor.

This structure consists of a PMM (Stage-1), an exciter (Stage-2) and the main generator (Stage-3). The PMM generator determines a variable frequency voltage which is associated with the engine speed. As the rotor spins, the PMM generates AC power. The generator control unit detects the voltage levels at the PMM generator armature, and provides main generator excitation via a DC/DC converter. The voltage level of the exciter armature is therefore controlled according to the exciter field. Since the exciter rotor windings are three-phase, the output power generated is continuous three-phase AC. With a rotating diode rectifier, the exciter AC output is converted into DC for presentation to the main generator. The main generator has a stator with an AC winding and a rotor with a DC winding. As a result, when the rotor rotates, it generates an EMF and produces electrical power [23].

- Induction Machine (IM)

  The IM is one of the most commonly-used electrical machines in industry due to

its robust and fault-tolerant capability. Also, since its techniques are mature for many years, the purchase is low cost. Basically, the IM can be grouped into two types, the squirrel cage and the wound type. The first one is widely accepted owing to its reliability and economic build. Its rotor core is manufactured using steel laminations and is slotted with aluminum or copper conductors. Although the IM is suitable for the EV or hybrid EV (HEV) applications in the automotive industry [24, 25], induction generators have not been adopted in aircraft power generation systems [26, 27]. This is because, for typical IM topologies, there would be mechanical constraints when operating at a high speed. The rotor cage starts to expand when the rotation speed increases which may result in conflict with the stator component [28]. Therefore, this structure may not be reliable for aerospace applications. Another limitation of this topology might be the complex cooling system design since the heat is generated both in the rotor and stator.

- Switched Reluctance Machine (SRM)

  The SRM is an electric motor that operates by reluctance torque. Unlike the brushed DC motor types, the power is delivered to windings in the stator rather than the rotor. Since the power does not have to be delivered to a moving part, SRM mechanical design is drastically simplifed. The main features of SRM-based systems include fault tolerance, the capability to operate in harsh environments and magnet free design. However, its complicated electrical design should be considered for the entire systems. The main disadvantages of SRM are the large torque ripple, low power density and low power factor [29,30]. The existing literature about SRM for the S/G system can be found in [31–33], in which the sensorless control, iron loss calculation and extended speed range are studied for SRM-fed S/G systems. Considering the SRM performance in terms of acoustic noise and torque pulsations, application of SRMs for the aerospace industry is still constrained to some extent.

- Permanent Magnet Machine (PMM)

The PMM is a type of electric motor that uses permanent magnets rather than windings on its rotor. It is more efficient than IM or motor with field windings for certain high-efficiency applications, such as traction drives [34]. The magnets are usually attached to the rotor of the machine. PMMs can be categorized as either surface-mounted permanent magnet (SPM) or interior-mounted permanent magnet (IPM) machine. The PMM is characterized by high efficiency, high output torque performance, high power density and good flux-weakening (FW) capability [35].

In [36], an advanced control strategy of an open-winding PMM with the inverter-rectifier topology is proposed to overcome the shortcomings of traditional PMM-based S/G systems, such as narrow speed range and low power factor. In [37], a high-performance design and control for a PMM-based S/G system are proposed to allow a wide constant power region and higher efficiency operation. In [38] and [39], dedicated modulation strategies and control algorithms have been thoroughly studied for PMM-fed high-speed S/G systems.

However, there are still some shortcomings waiting to be overcome for current PMMs, such as the inability to disable the magnetic field, if they are applied in the high-speed aerospace drive systems. Apart from that, another problem is its vulnerability to high temperatures. Therefore, cooling systems are mostly required to ensure that the magnets are within safe operating temperatures. The upper limit temperature of the permanent materials is about 300°C. Furthermore, compared with the multiphase machine, the PMM relies on control algorithms to gain the capability of fault-tolerant [40].

2.2.3 Generator Control

For the conventional power generation systems, the main objectives are to control the output voltage and to supply aircraft system loads. Normally, the low power DC voltage is 28VDC, while 270VDC is for high power loads and further power conversion [3]. For example, with respect to the separately excited DC generator systems,

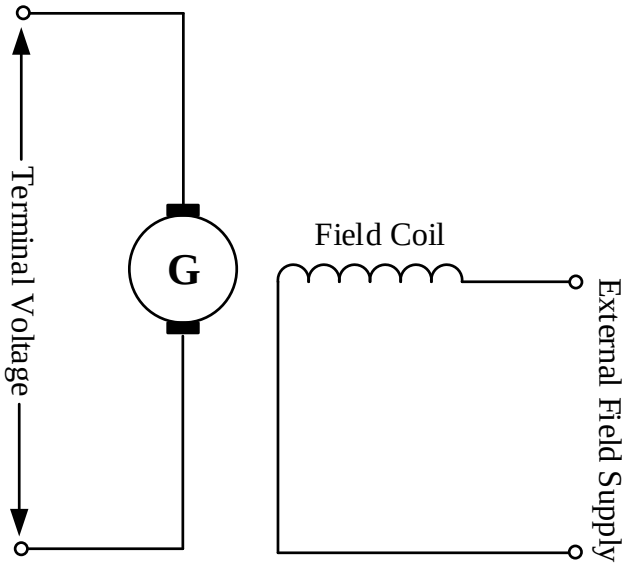


Figure 2.6: Separately excited DC generator voltage regulator

the terminal voltage can be controlled by controlling the field through the external field supply, as shown in Figure 2.6. The DC generators are controlled to supply constant DC voltage even with varying engine speeds and electrical loads. Besides, to ensure the capability onboard EPS and other loads, the voltage regulation needs to fulfill aircraft electric power quality standard, as stated in MIL-STD-704F [15]. For AC generation systems, its control features a similar way apart from a separate DC source for field excitation. As a result, additional devices are required to control this DC source which makes the overall control system a bit more complicated.

In terms of multi-engine aircraft, more than one generator is normally available to operate at the same time, which brings a chance for parallel control. The benefit of paralleling operation is that both active and reactive power from each generator can be controlled to achieve effective load sharing [3]. Another advantage of the parallel control is that the required electrical power can be supplied to the S/G in case any failure occurs during the flight unexpectedly.

The parallel control could be applicable for the CF and VSCF topologies [3]. In order to realise effective load sharing for the CF topology, both active and reactive power from each generator would need to be controlled, simultaneously. Neverthe-

less, the parallel control performance highly relies on the accuracy of the constant speed drives. Active load sharing is equally distributed by using the current error sensed from current transformers, whereas reactive load sharing is established by altering the DC excitation current that determines the generator output voltage [3]. Since their power outputs are constant frequency, the parallel control could be deployed to the VSCF topology in a similar way. However, the paralled control method is impossible to apply for the VSVF topology since it needs to adapt to the effect of wide varying frequencies between multiple generators by regulating the active and reactive loads. Although it still can be attained by employing power electronics converters on the generator output, different control strategies must be taken into consideration for the target system. Obviously, it is safer and easier to operate without paralleling.

2.2.4 Electrical Power Distribution

Not only for the 28VDC, but also for the 230VAC variable frequency of AC system, the voltage level of power generation tends to increase so as to satisfy the load demands on the aircraft. The output of 115VAC with 400Hz for commonly-used civil aircraft design has not changed since the 50's decade in the last century. The electrical power system in conventional aircraft often uses two or more engine-driven generators to supply AC loads. That structure is connected to the distribution buses in some civil aircraft configurations. When one generator fails, it is automatically isolated from its respective busbar, and all busbar loads are then taken over by the alternative generator [3].

More recently, higher voltage level electrical systems have been realized by using a high voltage DC power distribution system in the MEA. 230VAC variable frequency systems have been adopted on the Boeing 787 dreamliner, while 270VDC systems have been developed for military aircraft, such as Lockheed Martin F-22 and F-35 [11,41]. With the improvement of control, modulation and topology of multilevel power electronics converters, higher voltage levels provide a chance of lower current transfer at the same power level. As a consequence, the size, weight and copper

losses of onboard distribution wires can be reduced.

For example, there is 2×250kVA S/G per engine to form the power distribution system in B787, thereby giving 500kVA of generated power per channel. Besides, 2×250kVA APU S/G are on board. The main bus is 230VAC with variable frequency ranging from 360Hz to 800Hz. By contrast, four variable generators are driven by four engines of A380. More specifically, two APU generators are driven by their respective APUs. With the control of the generator control unit, each main generator supplies power to the appropriate AC bus. While each AC bus can also be supported by a ground power input. Considering that these generators operate at a different frequency determined by the speed of the aircraft engine, the primary AC buses cannot be paralleled for that case.

2.2.5 Starter-Generator System

Novel S/G topologies of the MEA, with the help of the development of the electrical power system (EPS), have been demonstrating for several decades [42]. The S/G layout combines both the motoring and generating function into one machine which aims to save weight and size [43]. Normally, the S/G system needs to meet two basic requirements, accelerating the engine and generating electrical power. When serving as a starter, the S/G accelerates the engine to a self-sustaining speed. In turn, during the power generating mode, the S/G driven by the aircraft engine can supply power to the onboard loads. There are four dedicated S/G systems in accordance with applied machine types:

1. IM and SRM have been investigated as an S/G in [29]. The IM is implemented with a resonant converter and can perform in starter and generator mode. A 250kW SRM has been tested on the aircraft S/G system requirements in [44]. Also, this type of machine can operate in both starter and generator mode (up to 13.5krpm). In addition, the dynamic loading of 102.5kW has also been carried out.

2. Three-stage brushless synchronous starter-generator has been proven to be a

mature candidate as the S/G. It possesses a high power factor in a wide-speed range and reliable de-excitation ability in the case of post-fault operation [45]. However, due to the rotating diodes and windings on the rotor, the structure of the rotor suffers from higher speed rotation, thus compromising its reliability.

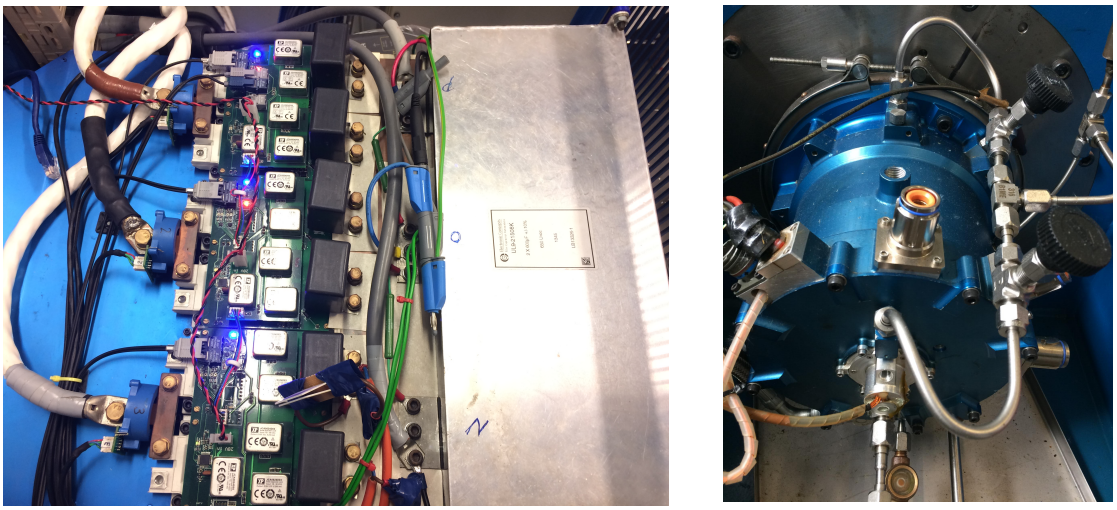
3. PMSM has been widely considered in EV applications because of its high power density, high efficiency and high-speed ability, particularly with respect to the IPM [46–48]. Nevertheless, a few disadvantages of this structure need to be solved before applying to the aerospace industry because of the inability to disable the magnetic field and the risk of irreversible demagnetization at high temperatures. With the help of the development and application of the rare earth permanent magnet materials and wide-band-gap (WBG) switching devices [49], many research works have been done to overcome the disadvantages of this configuration [50, 51]. Besides, even though multilevel topologies feature superior performance in many aspects, there is still a lack of comprehensive study of high-performance PWM strategy for the multilevel converter-fed high-speed S/G system.

2.3 AEGART Project

The research work presented in this thesis is based on the "Aircraft Electrical Generation with Active Rectification Technology" (AEGART) project, a part of the Clean Sky JTI EcoDesign ITD EU FP7 framework program [14]. The aim of this project is to improve aircraft overall efficiency from weight, volume, and power losses viewpoint. Apart from that, safety and reliability are taken into consideration. Figure 2.7 shows the laboratory-built prototype of the AEGART project for the aircraft electric S/G system studies.

The novelties of our designed system are as follows:

(i) The constant speed gearbox can be removed from the aircraft, the reliability of the S/G system would expect to be significantly enhanced.



(a) (b)

Figure 2.7: Laboratory prototype of the AEGART project (a) 3L-NPC converter (b) high-speed surface-mounted PMSM

(ii) As the PMSM's performance of torque-to-current ratio and power density are better than other machine types and surface-mounted one is easy for manufacturing, SPM is used as the S/G for the target system. More details about this machine design can be found in [52].

(iii) The 3L-NPC converter is chosen as the bi-directional active-front-end (AFE) due to lower voltage stress across semiconductor devices, lower harmonics, better electromagnetic compatibility (EMC) compared with two-level converter [53]. It can serve as the inverter and rectifier for the startup and power generation process, respectively.

This Ph.D study is a part of the AEGART project. The primary research is to explore the modulation strategy to make the AEGART S/G system operating in high-performance states during both starter and generator mode. Our ESG system is designed to fulfill the following technical specifications:

- In starter mode, the engine should be driven up to a self-sustaining speed at ambient temperatures that vary between -40^{o}C$\sim+55^{o}$C [16].
- The SPM speed in motoring mode is up to 10krpm while its speed is within the range of 19.2krpm$\sim$32krpm in generation mode.

- The power rating of the system is 45kW which delivers electrical power to the 270VDC bus.
- The electric power quality should satisfy the standard of MIL-STD-704F [15].
- The output DC current should be controlled based on the voltage droop characteristic, i.e., current-voltage droop characteristic. The current-mode approach uses the measured voltage to calculate the desired injecting DC current [6].

2.3.1 AEGART Electrical Machine

For the developed S/G system, the PMSM is mechanically coupled to the engine shaft and electrically connected with a power electronics converter. This machine runs as a starter in motoring mode, and work as an electrical generator in power generating conditions. The PMSM mathematical model equations in the d-q reference frame are expressed as follows:

$$T_{em} = \frac{3}{2} n_p \cdot [\varphi_f \cdot i_q + (L_d - L_q) i_d i_q] \tag{2.1}$$

$$V_d = R \cdot i_d + L_d \frac{di_d}{dt} - \omega_e \cdot L_q \cdot i_q \tag{2.2}$$

$$V_q = R \cdot i_q + L_q \frac{di_q}{dt} + \omega_e \cdot L_d \cdot i_d + \omega_e \cdot \varphi_f \tag{2.3}$$

where T_{em} represents the electromagnetic torque, n_p refers to the number of pole pairs, φ_f is the permanent magnet flux linkage, V_d, V_q and i_d, i_q indicate the direct and quadrature components of motor voltage and current, respectively, L_d and L_q are the dq-axis inductances, ω_e denotes machine electrical speed, and R is the stator winding resistance.

In terms of the SPM used in the target S/G system, L_d equals L_q. Therefore, the electromagnetic torque of the machine is only provided by permanent magnet torque, which is the first term in equation (2.1). Since the maximum voltage value, indicated by V_{lim}, is determined by DC-link voltage and the applied PWM strategy,

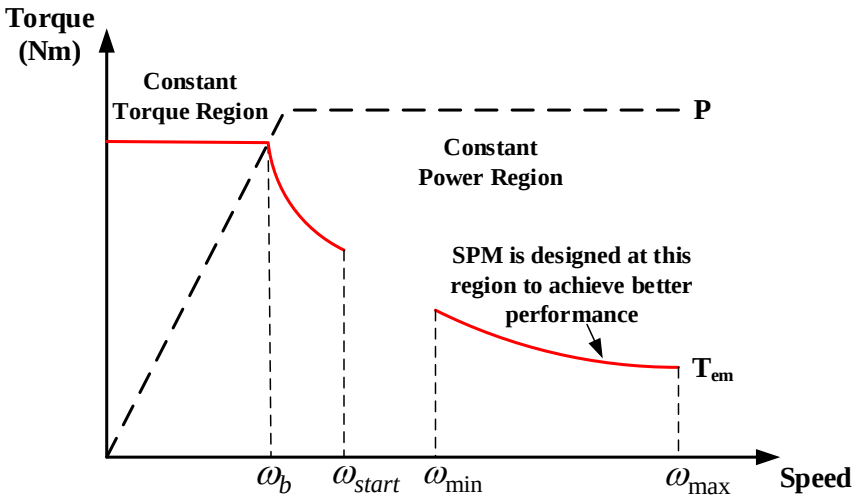


Figure 2.8: The torque-speed characteristics of the AEGART SPM [2]

the corresponding limitation can be written as:

$$(i_d + \frac{\varphi_f}{L_d})^2 + i_q^2 = (\frac{V_{lim}}{\omega_e L_q})^2 \tag{2.4}$$

Considering the designed machine/converter capacity, the maximum current value, manifested by I_{max}, should meet:

$$i_d^2 + i_q^2 \leq I_{max}^2 \tag{2.5}$$

Therefore, the solution of equations (2.4) and (2.5) which is an overlapped area of voltage and current limit circle restrict the allowable operating points of the studied ESG system.

On the other hand, the motor is designed to obtain a dedicated torque-speed characteristic [2], as illustrated in Figure 2.8. This includes the constant torque region and the constant power region. ω_b refers to the base speed of the machine, which is defined as the last speed that can utilize the maximum torque. After that, in order to maintain a constant power output, the torque output is reduced. In accordance with the requirement of S/G system, ω_{max} and ω_{min} denote the maximum and minimum generation speed of the machine, respectively. In the startup process, the SPM provides constant torque, whereas constant power is required when the system operates in generator mode. When the SPM operates in motoring mode,

positive torque is required. If the engine torque is negative, the SPM runs in generator mode. It is notable that the maximum machine torque output should be selected to meet the torque requirement of the aircraft engine. Normally, the S/G operates as an electric generator for most of the time, therefore, the machine has been optimized in the high-speed region.

In the design process, fault tolerance is considered by adopting a redundancy solution in the event of a failure [54]. This allows a distributed winding to be adopted, consequently minimizing rotor losses in both the permanent magnet and the rotor back iron. As high pole numbers result in the high fundamental frequency scenario, the converter's switching frequency has to be set at a higher value in order to increase the sampling points over a line cycle. However, this will render extra switching losses. Based on the above reasons, the number of designed machine rotor poles is limited to 4, 6 and 8. For our case, a 6-pole electrical machine design is considered as the best candidate which also attains the lowest eddy-current losses [2]. The AEGART machine parameters are detailed in Table 2.1.

Since the magnets are surface mounted on the rotor, carbon fibre is utilized as a sleeve to keep the magnets in place at high-speed operation. The sleeve thickness calculation is based on an over-speed safety margin (i.e. designed at 32krpm$\times$110% =35.2krpm). With the help of the special design of the machine housing, the cooling oil can be channelled between the slots and along the stator outer diameter for the purpose of better efficient cooling. The electromagnetic losses, including copper/iron losses and eddy current losses in magnets, have been verified by using the simulation of finite element (FE) machine model and power converter in MATLAB/SIMULINK with PLECS toolbox [55].

2.3.2 Thermal Management System

The thermal design of the developed electric S/G has been investigated in the work of [56]. The primary principle used for the machine cooling is to use ducts through the stator core along the stator outer diameter and the slots existing between stator teeth. The AEGART machine was designed to be oil-cooled and the nominal

Table 2.1: AEGART machine parameters

Parameters	Value
Stator inductance ($L_d = L_q$)	99μH
Pole pairs	3
Stator resistance	0.1Ω
PM flux	0.03644V$_s$/rad
Rated power	45kW
Combined machine and engine inertia	0.403kgms^2

oil temperature is 120°C. There are two main methods for distributing oil, indirect and direct cooling. The simulation results identify the better performance of direct oil cooling because significant temperature reduction can be achieved [16]. With numerical simulation, the fluid flow within the SPM can be conducted by computational fluid dynamics (CFD). Through the analysis, it can demonstrate that the machine cooling system is capable of maintaining the SPM temperature within the safety range.

In terms of the power electronics converter, the thermal management system was designed according to the estimated maximum power losses under the worst case condition. This scenario represents the unsuccessful start, followed by the second restart attempt after 3 minutes [2]. A forced air-cooled approach was employed and the heatsink for the power modules was carefully designed to ensure an acceptable temperature. With the simulations of CFD, the results verify that the cooling system of the converter can dissipate the heat during both starter and generation mode. Thus, the temperature from the converter side satisfies the thermal requirement.

These cooling systems are employed to make sure high power density and high reliability of the laboratory-developed aircraft ESG prototype system during the performance test.

2.3.3 Control Strategies of S/G Systems

In order to obtain high steady-state and dynamic performance, the control strategies play a significant role in the target S/G system. In the startup process, the speed

and torque controls are used to rotate the air compressors of the aircraft engine. In generation mode, the speed of the engine is controlled externally. Also, the DC link bus power is controlled as the primary objective. It should be noted that starter and power generation modes are two independent control objectives. Hence, there is no need to control them at the same time.

Due to the fact that the S/G operates at a high speed in the steady-state, the converter may be subjected to very high back EMF on the machine side. In order to increase the machine speed further, flux-weakening (FW) control is required to ensure back EMF is within the converter's limits [57]. If a stand-alone system is considered for the ESG system, DC-link voltage is fixed at 270VDC to provide uninterrupted electrical power for onboard loads. When multiple S/G systems or electrical power sources are connected in parallel, based on the current-voltage droop characteristics, droop control is employed to allow power-sharing among each system [58, 59].

According to these considerations, the specific control diagram of the ESG system, referred to [2], is shown in Figure 2.9. As can be seen, the outer control loop incorporates FW control, machine speed control and DC-link current control. The vector control technique is applied in order to decouple torque and flux producing current, which allows controlling flux and torque independently. Meanwhile, the PMSM mathematical model featured with non-linearity can be greatly simplified under the dq rotating reference frame. Therefore, machine torque represented as active power can be controlled by q-axis current. Considering high-speed operating conditions within a limited DC-link voltage utilization ratio, large negative current needs to be injected into d-axis, which causes a lower power factor. The starter mode activates speed control, and DC-link current should be regulated based on the droop characteristics under power generating conditions. The inner control loop is designed for current control. Although model-predictive-control (MPC) schemes based current controller can improve system dynamic response [60], the sensitivity of system parameter cannot be neglected. Hence, the magnitude of space vector employed at the AC-side terminal of power converter is still calculated from the

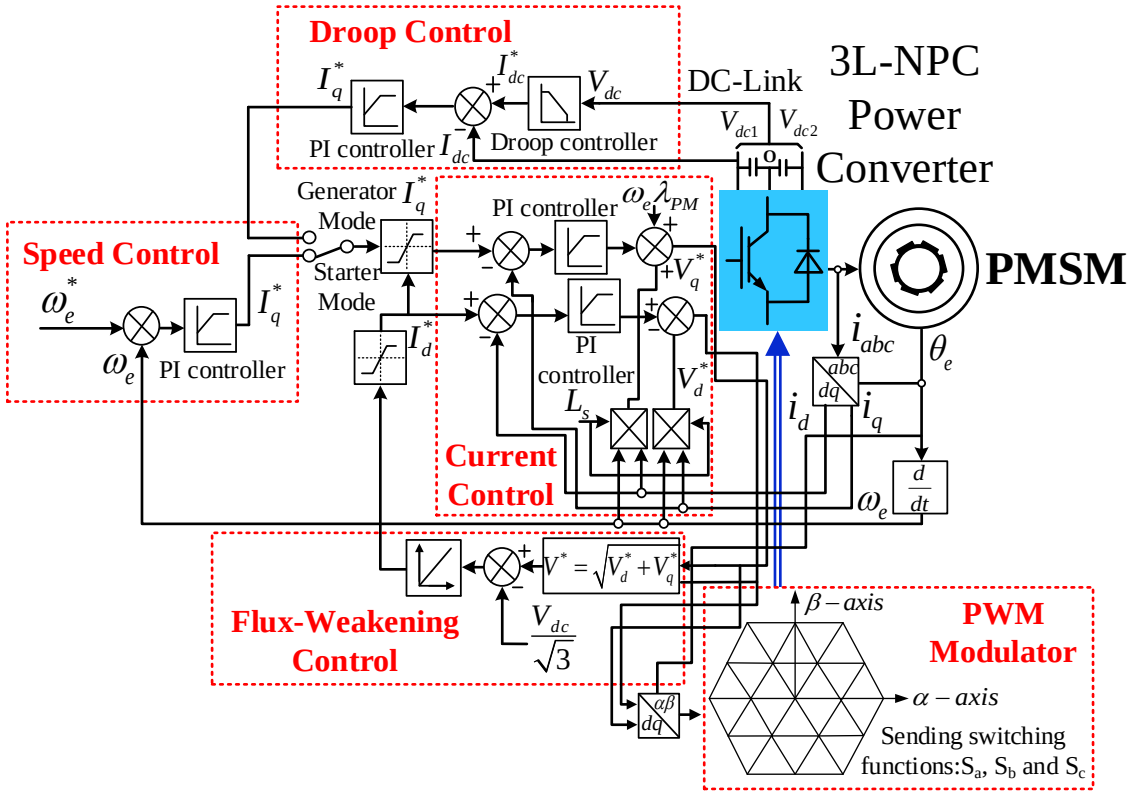


Figure 2.9: Control diagram of the designed ESG system [2]

classic current proportional-integral (PI) controller. Finally, V_α and V_β commands are sent to PWM modulator for turning on and off semiconductor devices periodically. The reference frame transformation is presented in Appendix A. More detailed specifications for starter and generation modes will be elaborated in the following subsections.

2.3.4 Starter Mode Operation

In this mode, two key factors should be carefully considered. Otherwise, they will limit the performance of the S/G electrical system.

- The first one is the maximum current flowing through the converter's insulated-gate bipolar transistors (IGBTs). The control algorithm needs to guarantee that the current demand does not go beyond a safe limit. In accordance with the AEGART converter design [2], the maximum current is 400A. Hence, the

current limitation should fulfill to meet equation (2.5).

- The second one is the AC side voltage limitation which is applied to avoid converter operating in the overmodulation region. When the PMSM operates at a high speed, the machine back EMF can be very high. In this case, the S/G system constantly requires deep FW currents to ensure that the converter's output voltage is within $|V_{ref}|_{max}$ [61]. By using the principle of the traditional space vector PWM (SVM) scheme in the linear modulation range, together with the given DC-link voltage, $|V_{ref}|_{max}$ can be calculated by:

$$|V_{ref}|_{\max} = \frac{270}{\sqrt{3}} = 155.88V \tag{2.6}$$

It is assumed that the stator winding resistance is ignored and the high-speed machine operates in the steady-state, the PMSM electrical equations given by equations (2.2) and (2.3) can be re-expressed as:

$$V_d = -\omega_e \cdot L_q \cdot i_q \tag{2.7}$$

$$V_q = \omega_e \cdot L_d \cdot i_d + \omega_e \cdot \varphi_f \tag{2.8}$$

Then, along with the following equation:

$$|V_{\max}| = \sqrt{V_d^2 + V_q^2} \tag{2.9}$$

Therefore, the voltage and current limit circles can be plotted based on equations (2.6)-(2.9) on the *dq*-axis current plane. As seen from Figure 2.10, the radius of the green voltage circle decreases as the motor speed increases from 8krpm to 32krpm. The red circle represents the machine speed is 14krpm while the other dashed circles are the voltage limits at different operating speeds. The centre point of this circle is the characteristic current (i_{ch}) at $-\varphi_m/L_q$ or -367.67A according to the AEGART machine's parameters. Theoretically, a machine can run at infinite speed which is in the centre point of the voltage limit circle. The blue circle represents the current limit. Point B is at the

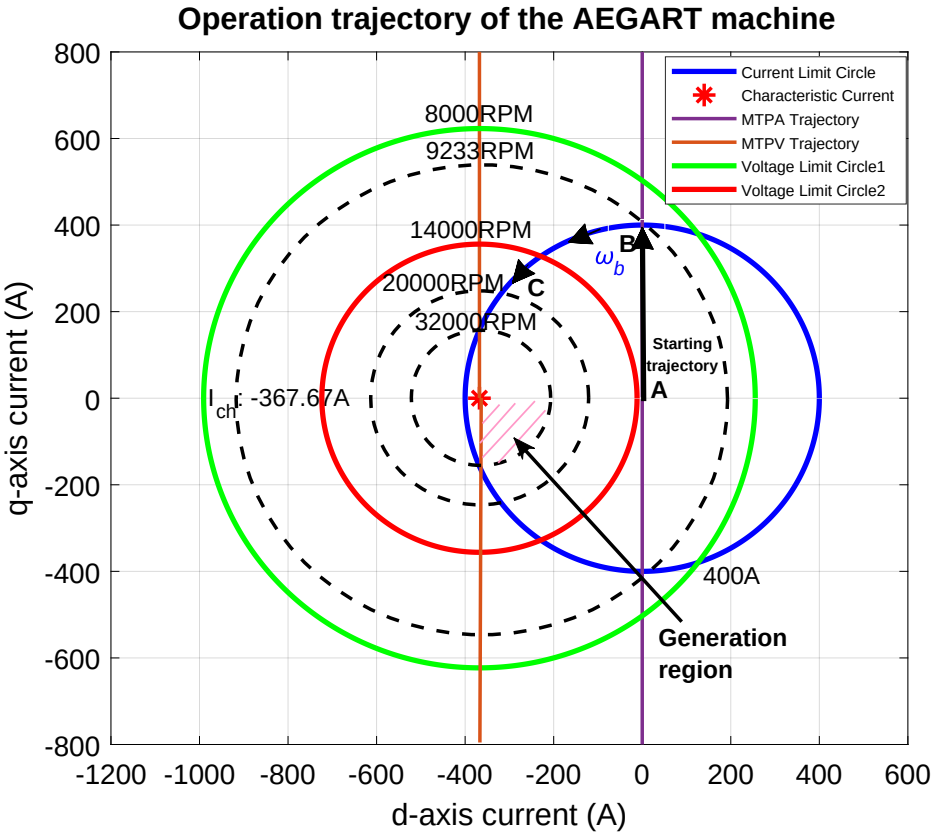


Figure 2.10: Operating trajectory of the designed ESG system

intersection point when i_q is maximum and i_d is zero. At that time, the machine's base speed represented as ω_b is 9233rpm according to the voltage limit equation. If the PMSM speed needs to be further ramped up, the FW control should be employed. As can be seen, the red circle indicates that FW current always needs to be injected during its whole operation.

In terms of the starter mode, the current trajectory of the PMSM has been depicted in Figure 2.10. When operating conditions range from standstill to the base speed (ω_b), the AEGART machine will run in the constant torque region and enable to utilize the maximum torque, which features a straight line moving from point A to point B. When the motor further accelerates to a higher speed, the voltage limit circle will constrain the current trajectory. When the speed is above ω_b, the PMSM will operate in the constant power region. It is noted that the current operating point needs to be within the overlapped

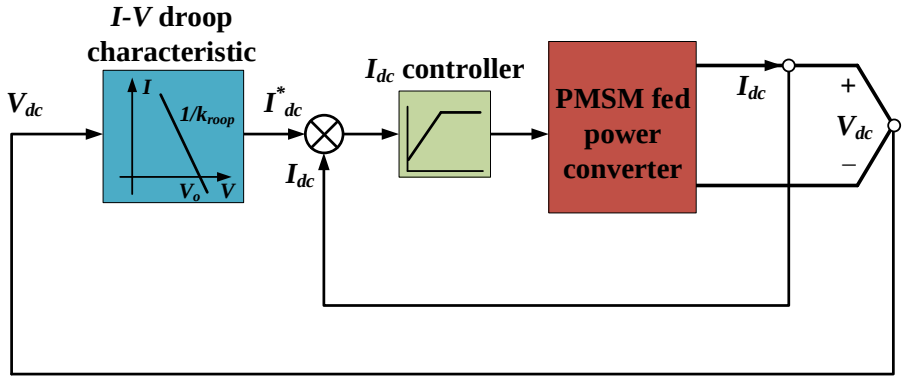


Figure 2.11: Current-mode droop control scheme in the generation mode

area of both current and voltage limit circles. As a consequence, the current trajectory moves along its limit circle from point B to point C.

2.3.5 Generation Mode Operation

In power generation mode, active power flow is directed toward the onboard DC bus. When the electrical machine functions as a generator, the output voltage has to be controlled to maintain appropriate voltage levels for the electrical loads. Therefore, the DC-link controller plays an essential part for possible parallel operation with multiple controlled power sources [59, 62], which substitutes speed control used in motoring mode. For the studied S/G system, a droop control scheme is utilized to achieve power-sharing among the sources in the EPS [63]. Here, the current-mode droop method is chosen as a representative example to explain. It can be seen from Figure 2.11 that, in order to generate an appropriate value of DC current reference denoted as I^*_{dc}, the following equation can be expressed as:

$$I^*_{dc} = \frac{V_o - V_{dc}}{k_{droop}} \tag{2.10}$$

where k_{droop} indicates a droop gain. V_o refers to the rated DC-link voltage reference, which is normally 270VDC. However, the acceptable steady-state voltage level is within 250∼280VDC as it is stated by the standard of MIL-STD-704F [15].

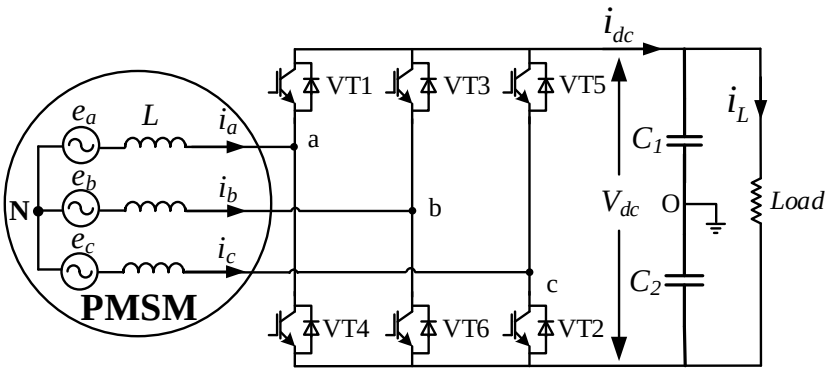


Figure 2.12: Circuit diagram of a two-level converter-fed PMSM drives

2.3.6 Power Electronics Converter

According to the machine design, the applied power converter limits are defined as a peak output current of 400A. The DC-link voltage could possibly reach 1.2kV at max speed without the FW control and if IGBT power modules are fully rectified. These sets limit for converter's switching devices. The fundamental frequency is up to 1.6kHz when the machine runs at 32krpm. There are two commonly-used topologies for the converter setup, the two-level and three-level neutral-point-clamped (NPC) power converter. The first one consists of two switches in each arm, while there are several variants for the second type. A more detailed elaboration is given in the following text.

Two-level converter-fed PMSM drive systems shown in Figure 2.12 feature simplicity and the minimal number of switching devices which reduce the risk of faults, such as open or short circuit faults. In contrast, the three-level topology becomes a competitive candidate due to its much lower EMI emissions and better power quality. Additionally, the voltage across the switching devices is only half the DC-link voltage in comparison with two-level counterpart where devices should withstand full DC-link voltage. These features effectively double the power rating of the converter for a given semiconductor device. As a result, three-level converters are preferable for motor drive applications with 270VDC buses. It is also noticeable that good power quality on the AC-side can simplify filter design and avoid the bulky issue,

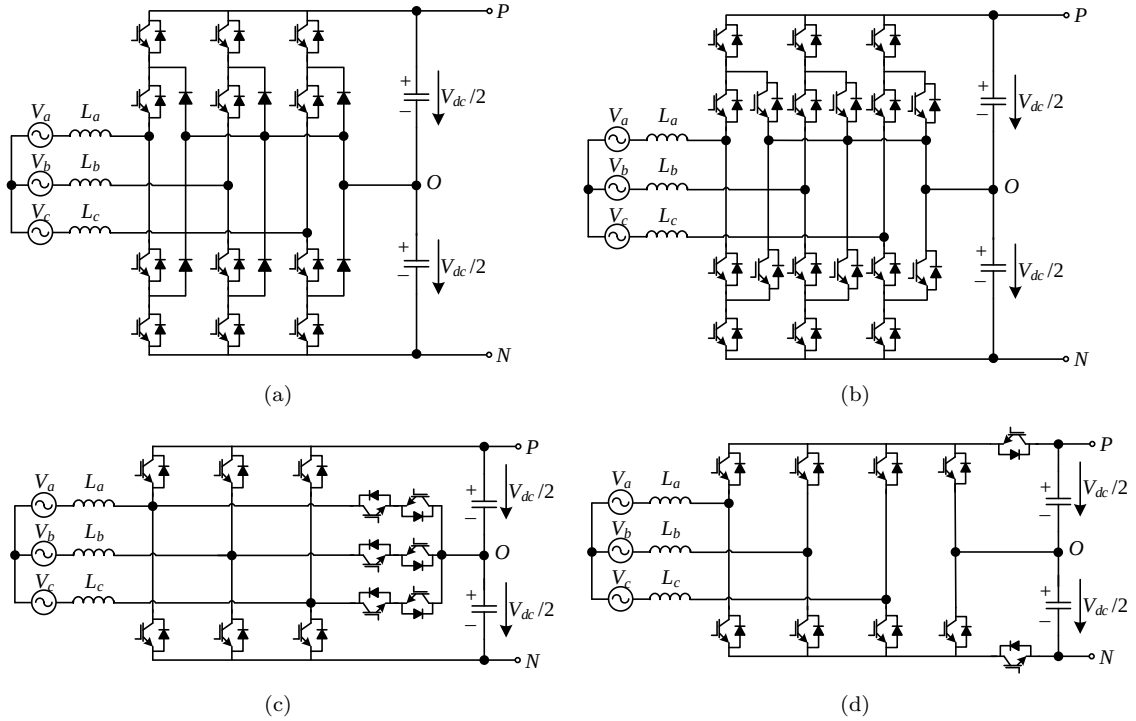


Figure 2.13: Three-level topology with the structure of (a) DNPC (b) ANPC (c) TNPC (d) SNPC

which is beneficial for the purpose of high power density.

The first NPC topology possessed with clamping diodes (DNPC) was proposed in [64] by Hirofumi Akagi *et al.* in 1981, as shown in Figure 2.13(a). This topology uses uncontrollable semiconductors for clamping the midpoint of the DC-link. In 1993, A simplified 3L-NPC converter (SNPC) was proposed in the work of [65], as shown in Figure 2.13(d), which has only ten switching devices with anti-parallel connected diodes. Since medium space vectors (introduced later in this thesis in Section 2.4.2) do not exist according to the limited switching state [66], output voltage/current quality is distorted as compared to the original three-level topology. As a result, this converter is rarely used in present industrial applications. In 2005, the active NPC (ANPC) topology shown in Figure 2.13(b) was introduced in [67] to evenly distribute losses among switching devices by selecting upper and lower neutral-point clamping paths, which brings a substantial increase in inverter output power and switching frequency. In 2013, Johann W. Kolar presented another three-level topology named T-type NPC (TNPC) [68] illustrated in Figure 2.13(c). In

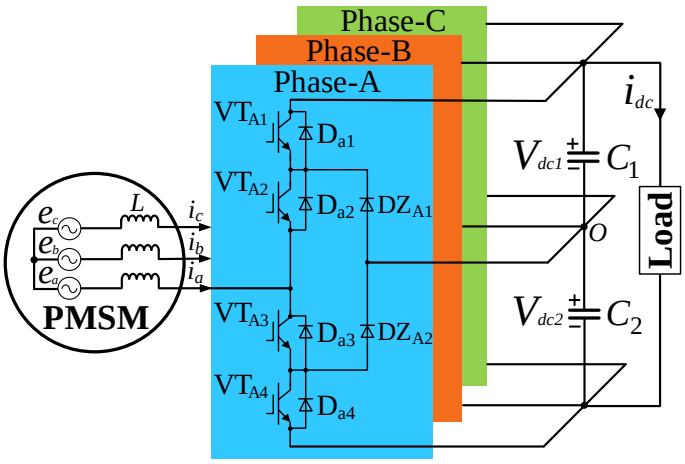
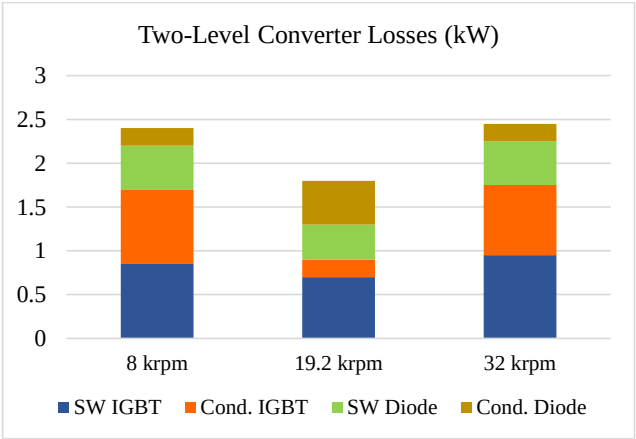


Figure 2.14: Circuit diagram of the 3L-NPC converter-fed PMSM drives

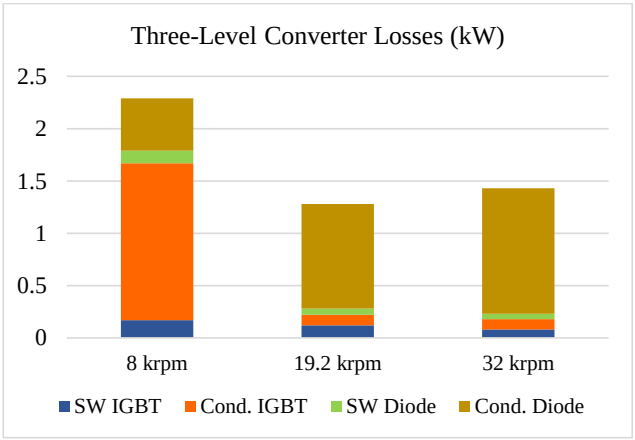
comparison with six switch positions per phase by the classic NPC topology, T-type three-level topology only has four switch positions per phase though two of these semiconductors need to withstand higher voltage stress.

With respect to AEGART project, a higher switching frequency is required due to the high fundamental frequency under high-speed operation. In this regard, the findings in [66, 69] verify that more efficiency can be achieved by the DNPC operating with a higher switching frequency (>30kHz). Though ANPC structure gains the advantage of more commutation paths, thereby attaining evenly distributed losses among switching devices. However, additional devices and complicated gate driver design are adverse for the laboratory-developed converter at the initial stage. TNPC topology features the minimum amount of semiconductors, but outer switches must be rated to block full DC-link voltage. It means that this topology is normally applied in low-power applications, such as three-level inverters for grid-tied photovoltaic (PV) systems. Hence, in this thesis, the DNPC topology is considered as the first-generation prototype to demonstrate the three-level NPC starter-generator system for the MEA applications, as shown in Figure 2.14. For sake of the convenience, the 3L-NPC converter refers to the DNPC structure in the following text.

Considering that more power losses indicates stringent requirement of cooling system capacity, thereby increasing more weight and size of the whole systems. As a result, power losses are another crucial aspect to compare the performance of two-



(a)



(b)

Figure 2.15: Converter losses comparison at different speed of designed S/G system (8krpm refers to starter mode while 19.2krpm and 32krpm refer to generation mode) with (a) two-level topology and (b) three-level topology

level and 3L-NPC converter. It is known that the total losses consist of switching and conduction losses [70]. There are two normal methods to calculate the converter's losses, thermal simulation and corresponding loss formulae shown in Appendix B. Here, the power loss analysis is carried out by using the PLECS toolbox with the thermal characteristics of semiconductor devices imported and implemented in the simulation modules. Infineon FF450R12IE4 (450A/1.2kV) [71] and F3L400R07ME4 (400A/650V) [72] modules are chosen the losses comparison of these two topologies. The switching frequency is set to be 16kHz and the DC-link voltage is 270VDC.

The power losses in these two topologies at the ESG system's different rotation speeds is shown in Figure 2.15. As can be seen, the conduction loss of IGBT takes

the majority part for three-level topology at 8krpm, whereas power distribution of two-level converter is more even except diode conduction loss. For power generation mode (over 19.2krpm), diode conduction loss of three-level topology accounts for the main distribution as current predominantly flows through diodes under rectifying mode. More importantly, the total losses of three-level topology are less than two-level counterpart, particularly for the power generating conditions.

Because of the aforementioned advantages provided by the 3L-NPC converter, this topology is selected as the prototype of aircraft S/G's energy conversion circuit for manufacturing and development.

2.4 Three-Level NPC Power Converter

2.4.1 Operational Principle

As illustrated in Figure 2.14, each phase of the 3L-NPC power converter consists of four switches (VT_{x1}~VT_{x4}) and two clamping-diodes (DZ_{x1} and DZ_{x2}), where $x \in \{A, B, C\}$. Two equal capacitors (C_1 and C_2) are series-connected to form the DC bus. VT_{x1} is complimentarily switched with VT_{x3}, while VT_{x2} and VT_{x4} follow the same manner. The switching state [P] indicates gating signal (S_{x1},S_{x2}) is (1, 1), which represents an output voltage of $V_{dc}/2$. The switching state [N] manifests gating signal (S_{x1},S_{x2}) is (0, 0), which denotes an output voltage of $-V_{dc}/2$, in which V_{dc} denotes the DC-link voltage. Otherwise, the gating signal (S_{x1},S_{x2}) is chosen as (0, 1), the resultant output voltage is zero and the switching state is expressed as [O]. Table 2.2 summarises the switching principle.

The four operational intervals of the converter's one phase leg are shown in Figure 2.16, where V_{xo} and I_x are the pole voltage and phase current of phase-x, respectively, while φ represents the power factor angle. In the following analysis, assuming that the current flowing into the converter is defined as a positive direction. It can be seen that, when phase current is positive, some of the output voltage switches between $V_{dc}/2$ and 0, whereas the other output voltage switches between $-V_{dc}/2$ and 0.

Table 2.2: Switching states and output voltages of 3L-NPC converters

Switching States	Gating Signals (S_{x1},S_{x2})	Output Voltages
[P]	(1, 1)	$V_{dc}/2$
[O]	(0, 1)	0
[N]	(0, 0)	$-V_{dc}/2$

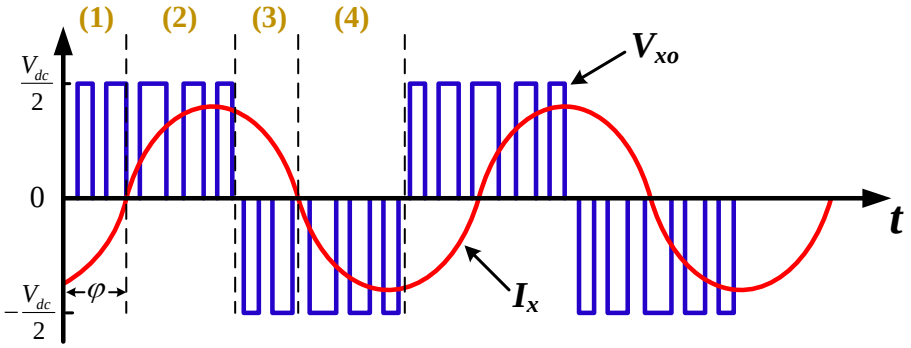


Figure 2.16: Four operational intervals of 3L-NPC converter phase leg

Taking phase-A as a representative example to analyse the operational mode over a fundamental period. Four groups are elaborated in detail as follows:

- For the area (1) in Figure 2.16, phase current is negative while the polarity of pole voltage is 0 and +. Two commutations occur for this case. The former indicates that phase current flows out of the midpoint of DC-link through DZ_{A1} and VT_{A2}, as shown in Figure 2.17(b.2). The latter represents that phase current flows through positive DC-rail, VT_{A1} and VT_{A2}, as shown Figure 2.17(b.1).

- For the area (2) in Figure 2.16, phase current is positive while the polarity of pole voltage is + and 0. In this case, $V_{dc}/2$ and 0 are periodically generated. The former output means that phase current flows into the converter through freewheeling diodes of VT_{A1} and VT_{A2}, as shown in Figure 2.17(a.1). The latter output indicates that phase current flows into the midpoint of DC-link through VT_{A3} and DZ_{A2}, as shown in Figure 2.17(a.2).

- For the area (3) in Figure 2.16, phase current is still positive while the polarity

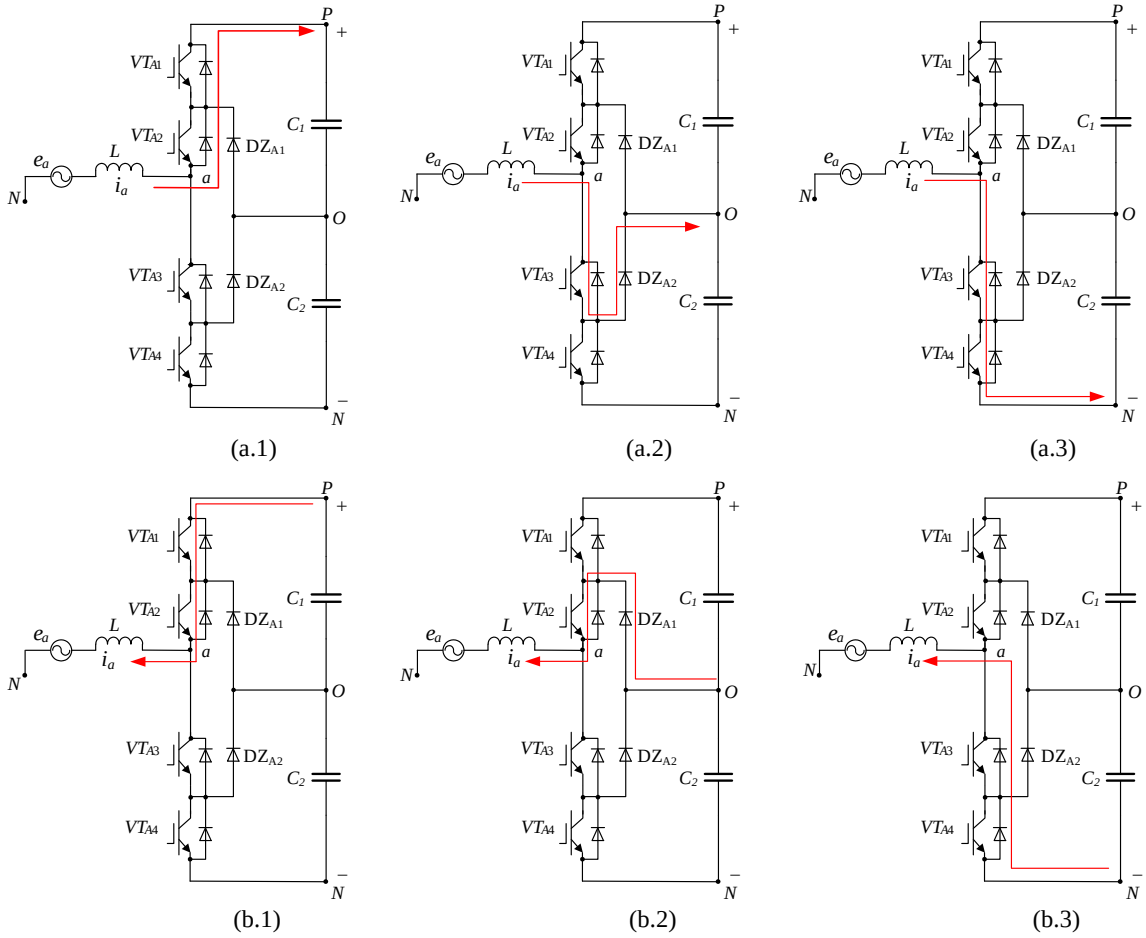


Figure 2.17: Three-level states associated with phase currents and output voltages

of pole voltage is 0 and −. For this case, output voltages are 0 and $-V_{dc}/2$. The former value indicates that phase current flows into the midpoint of DC-link through VT_{A3} and DZ_{A2}, as shown in Figure 2.17(a.2). The latter denotes that phase current flows into negative DC-rail through lower-arm series-connected IGBTs, i.e., VT_{A3} and VT_{A4}, as shown in Figure 2.17(a.3).

- For the area (4) in Figure 2.16, phase current is negative while the polarity of pole voltage is 0 and −. For this case, the output voltage of $-V_{dc}/2$ is generated when phase current flows out of the converter through the freewheeling diodes of VT_{A3} and VT_{A4}, as shown in Figure 2.17(b.3), whereas zero output voltage indicates that phase current flows out of the midpoint of DC-link through VT_{A2} and DZ_{A1}, as shown in Figure 2.17(b.2).

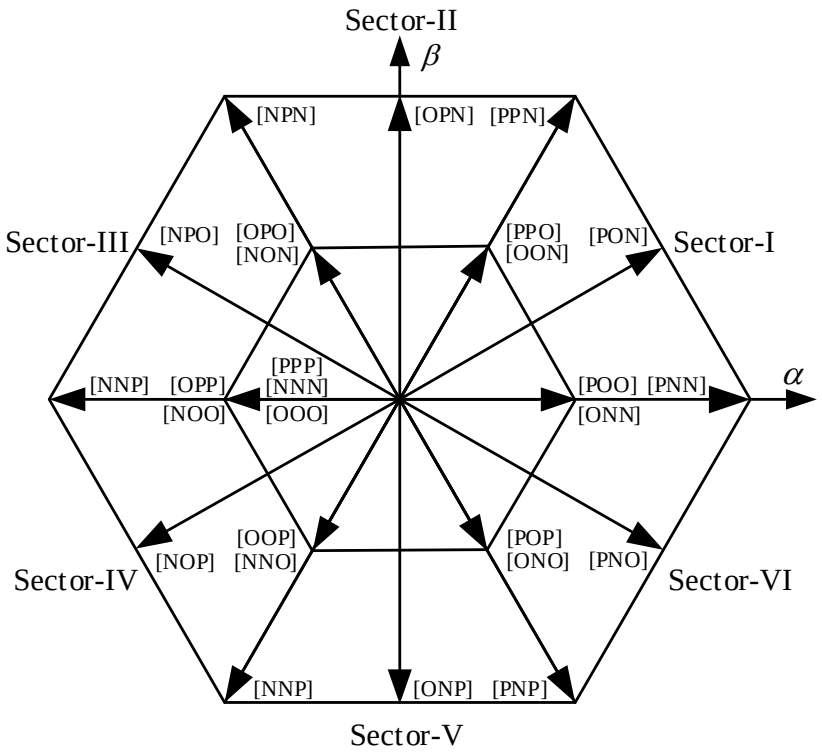


Figure 2.18: Space vector generation diagram

2.4.2 Space Vector Generation

Based on the above analysis, each output voltage of three-level can be expressed as a function of S_a, S_b and S_c:

$$\begin{cases} V_{AO} = \dfrac{V_{dc}}{2} \cdot S_a \\ V_{BO} = \dfrac{V_{dc}}{2} \cdot S_b \\ V_{CO} = \dfrac{V_{dc}}{2} \cdot S_c \end{cases} \tag{2.11}$$

where S_x (x refers to the phase-A, B or C) is defined as:

$$S_x = \begin{cases} 1 & if \text{ swithing state is [P]} \\ 0 & if \text{ swithing state is [O]} \\ -1 & if \text{ swithing state is [N]} \end{cases} \tag{2.12}$$

Moreover, all basic space vectors produced by a 3L-NPC converter can be deter-

Table 2.3: The magnitude of space vectors

Space Vectors	Magnitude
Zero Vector	0
Small Vector	$V_{dc}/3$
Medium Vector	$\sqrt{3}V_{dc}/3$
Large Vector	$2V_{dc}/3$

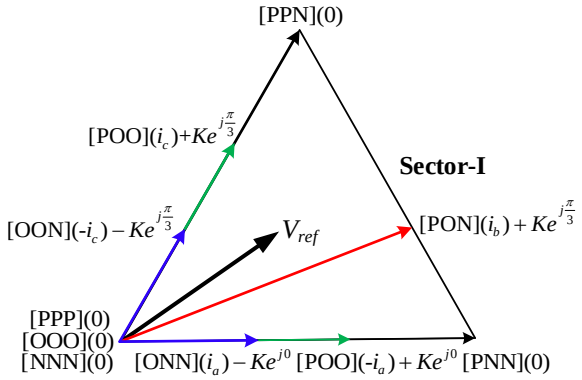
mined by:

$$\overrightarrow{V}_{basic} = \frac{1}{3}V_{dc}(S_a + S_b e^{j\frac{2\pi}{3}} + S_c e^{j\frac{4\pi}{3}}) = \frac{1}{6}V_{dc}\left[(2S_a - S_b - S_c) + j\sqrt{3}(S_b - S_c)\right] \tag{2.13}$$

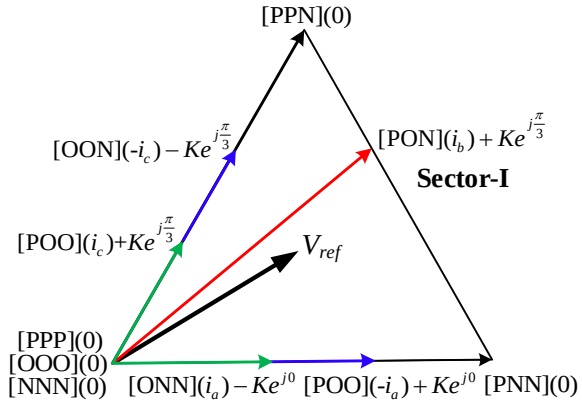
This indicates that each combination of switching states can identify a space vector and 3^3=27 voltage vectors are allocated in the complex plane, as shown in Figure 2.18. According to the magnitude of space vectors given in Table 2.3, all switching states generated by a 3L-NPC converter are classified into four categories: zero, small, medium and large vectors, wherein 12 are small ones, the number of large ones and medium ones are both 6 and the rest belongs to zero vectors [70].

Nevertheless, the space vector diagram (SVD) shown in Figure 2.18 is based on an assumption that two capacitor voltages are perfectly balanced. If not, the partition of this diagram will be changed accordingly [73,74]. It has been well known that the DC-link capacitor voltages need to be regulated asymmetrically in some application fields to improve the entire system's efficiency [75, 76]. For example, the 3L-NPC converter-fed grid-tied generation system with upper and lower PV modules' independent maximum power point tracking (MPPT) control can save extra DC/DC converter [77]. Furthermore, if the MPC technique is deployed, due to the optimized variable predictions and cost function evaluations, the 3L-NPC converter-fed PMSM drive's dynamic performance can be significantly enhanced for unbalanced DC-link voltage applications by using the capacitor voltages as one of the inputs to the fitness functions [78].

The output voltage of the 3L-NPC converter relies on two capacitor voltages which are key control objectives in this study. Therefore, before analysing the con-



(a)



(b)

Figure 2.19: SVD for Sector-I under unbalanced DC-link capacitor voltages (a) $V_{dc1}>V_{dc2}$ (b) $V_{dc1}<V_{dc2}$

sequence of unbalanced NP voltage scenario, the following variables are defined as:

$$\begin{cases} V = 0.5 \times (V_{dc1} + V_{dc2}) \\ K = 0.5 \times (V_{dc1} - V_{dc2}) \end{cases} \tag{2.14}$$

where V_{dc1} and V_{dc2} refer to upper and lower-side capacitor voltages, respectively.

Taking Sector-I as an example, the new output space vectors superscripted with (*) can be expressed as:

$$\begin{cases} V^*_{[\mathrm{ONN}]} = (V-K)e^{j0} = V_{[\mathrm{ONN}]} - Ke^{j0}, V^*_{[\mathrm{POO}]} = (V+K)e^{j0} = V_{[\mathrm{POO}]} + Ke^{j0} \\ V^*_{[\mathrm{OON}]} = (V-K)e^{j\frac{\pi}{3}} = V_{[\mathrm{OON}]} - Ke^{j\frac{\pi}{3}}, V^*_{[\mathrm{PPO}]} = (V+K)e^{j\frac{\pi}{3}} = V_{[\mathrm{PPO}]} + Ke^{j\frac{\pi}{3}} \\ V^*_{[\mathrm{PON}]} = V^*_{[\mathrm{OON}]} + V^*_{[\mathrm{POO}]} = (V-K)e^{j\frac{\pi}{3}} + (V+K)e^{j0} = V_{[\mathrm{PON}]} + Ke^{-j\frac{\pi}{3}} \\ V^*_{[\mathrm{PNN}]} = V_{[\mathrm{PNN}]}, V^*_{[\mathrm{PPN}]} = V_{[\mathrm{PPN}]} \end{cases} \tag{2.15}$$

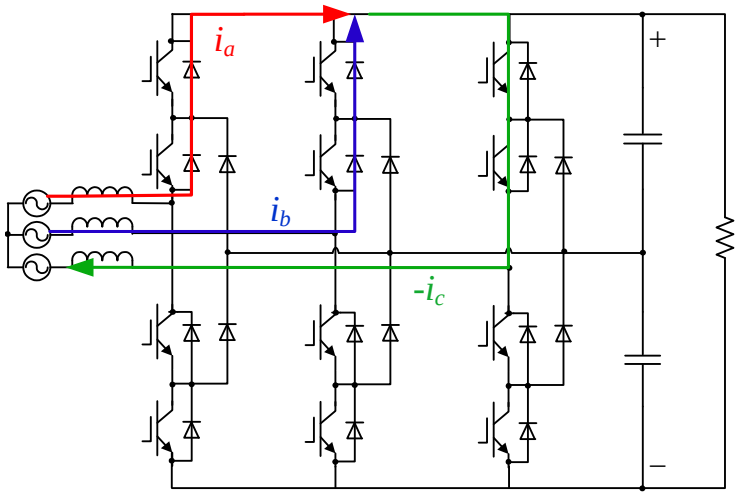


Figure 2.20: Commutation circuit of [PPP]

As seen from Figure 2.19, the position of basic space vectors in this sector varies based on the unbalanced range. Under this circumstance, the space vector synthesis process becomes complex. In this thesis, the space vector approximation method for keeping two balanced capacitor voltages is investigated for the designed three-level aircraft S/G system, rather than maintain their voltage difference intentionally.

To analyse the specific commutation circuit for the space vector synthesis process, assuming that i_a>0, i_b>0 and i_c<0, and zero vector [PPP] & [OOO], large vector [PPN], two small vectors [POO] & [ONN] and medium vector [PNO] are considered.

It should be pointed out that red, blue and green lines represent the current flowing path of phase-A, B and C in the following description, respectively.

- Zero vector [PPP] and [OOO]

  As shown in Figure 2.20, i_a and i_b flow through freewheeling diodes, while i_c flows out of the converter through upper arm IGBTs. The primary function of this switching state is to charge the energy stored in the inductors, which makes preparation for boosting voltage from AC to DC. It can be clearly seen that [PPP] has no impact on the NP voltage.

  As shown in Figure 2.21, i_a and i_b flow through IGBTs and clamping diodes into the NP, while i_c flows out of the NP. For a three-phase balanced system,

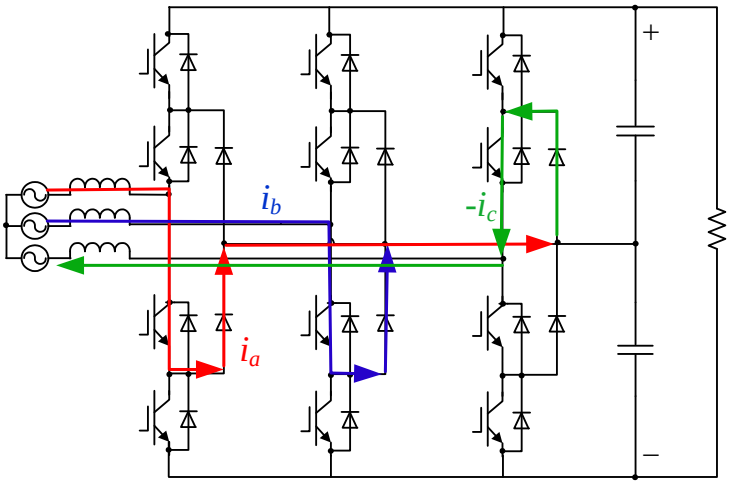


Figure 2.21: Commutation circuit of [OOO]

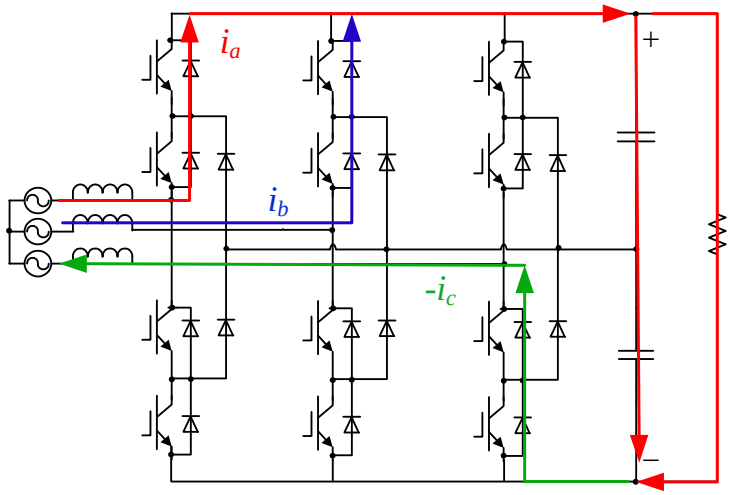


Figure 2.22: Commutation circuit of [PPN]

i_a+i_b+i_c=0, [OOO] is able to balanced capacitor voltage.

- Large vector [PPN]

  As shown in Figure 2.22, i_a and i_b flows through freewheeling diodes, while i_c flows out of the converter through lower arm IGBTs' freewheeling diodes. For this case, the phase currents charge the DC-link voltage and provide load current. Since two capacitor voltages are charged at the same time, the NP voltage still maintains balanced.

- Medium vector [PON]

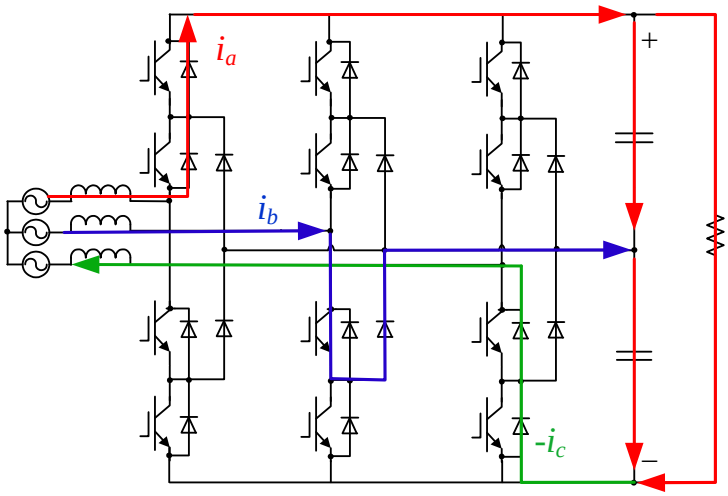


Figure 2.23: Commutation circuit of [PON]

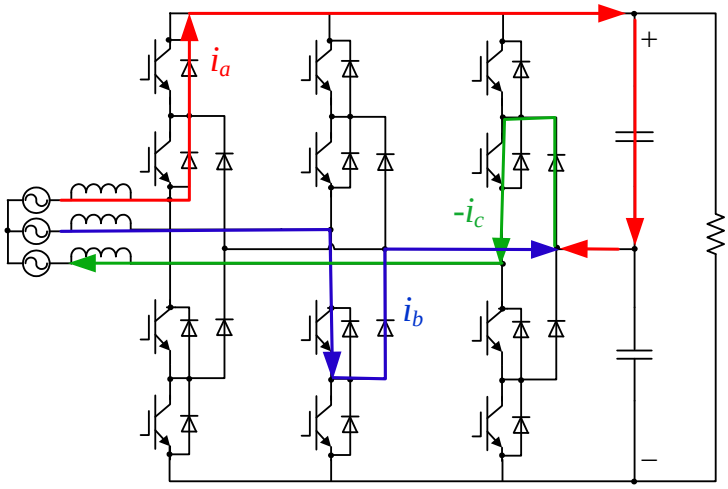


Figure 2.24: Commutation circuit of [POO]

As shown in Figure 2.23, i_a flows through freewheeling diodes of upper arm IGBTs for clamping phase voltage to the positive DC-rail, while i_b flows through IGBT and clamping diode to the NP, and i_c flows out of the converter through freewheeling diodes of lower arm IGBTs. As a result, NP voltage drifts away and the electric charge of the bottom capacitor is raised.

- Small vector [POO] and [ONN]

  As shown in Figure 2.24, i_a flows toward positive DC-rail through upper arm IGBT's freewheeling diodes. Both i_b and i_c flow through IGBT and clamping

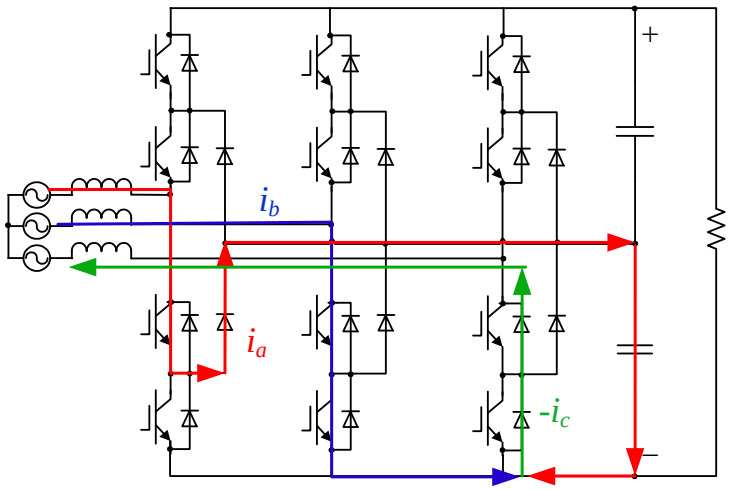


Figure 2.25: Commutation circuit of [ONN]

diode, whereas their directions are opposite. It can be clearly seen that i_a charges the upper-side capacitor.

As shown in Figure 2.25, i_a flows into the NP through IGBT and clamping diode, and i_b flows to the negative DC-rail through lower arm IGBTs, while i_c flows back through freewheeling diodes of lower arm IGBTs. It can conclude that the lower-side capacitor is charged by i_a in this situation.

From the above discussion, it can conclude that multilevel topology brings multiple choices of the switching state for producing the desired space vectors. This impacts the current flow path which is highly related to neutral-point voltage. Apart from that, it is known from the work of [79] and [80] that the commutation path also gives insight into the design of thermal management and busbar optimization, etc. The busbar design is important as it can be affected by the parasitic elements in the commutation path.

2.4.3 Mathematical Model

Figure 2.26 shows the equivalent circuit of the 3L-NPC converter that consists of three single-pole triple-throw switches. Similar to equation (2.12), for each phase leg-x ($x \in \{a, b, c\}$) of the converter, the switching function S_x determines the polarity of

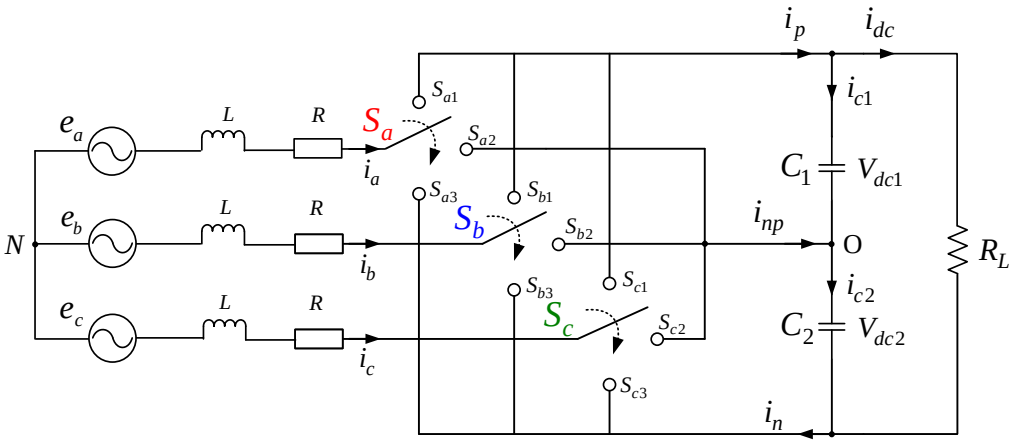


Figure 2.26: Equivalent circuit of the 3L-NPC converter with switching functions

the output terminal. If S_x =+1, the corresponding switching functions are expressed as: S_{x1}=1, S_{x2}=0 and S_{x3}=0. Similarly, if S_x = 0, then S_{x1}=0, S_{x2}=1 and S_{x3}=0 and If S_x =−1, then S_{x1}=0, S_{x2}=0 and S_{x3}=1.

V_{dc1} and V_{dc2} represent capacitor voltage of C_1 and C_2, respectively. e_x denotes the three-phase voltage source of power-grid or the back EMF of machine. L and R refer to machine inductance and winding resistance. Assuming that three phases are balanced, i.e., $e_a + e_b + e_c = 0$ and $i_a + i_b + i_c = 0$. Based on the Kirchhoff's voltage/current law (KVL/KCL), the mathematical equations of the 3L-NPC converter are given by:

$$\begin{cases} L\dfrac{di_a}{dt} + Ri_a = e_a - (V_a + V_{NO}) \\ L\dfrac{di_b}{dt} + Ri_b = e_b - (V_b + V_{NO}) \\ L\dfrac{di_c}{dt} + Ri_c = e_c - (V_c + V_{NO}) \end{cases} \tag{2.16}$$

where V_{NO} represents the voltage between the midpoint of AC source and the neutral-point of DC-link. V_x denotes the pole voltage of the converter, which can be expressed as follows:

$$\begin{cases} V_a = S_{a1}V_{dc1} - S_{a3}V_{dc2} \\ V_b = S_{b1}V_{dc1} - S_{b3}V_{dc2} \\ V_c = S_{c1}V_{dc1} - S_{c3}V_{dc2} \end{cases} \tag{2.17}$$

With equations (2.16) and (2.17), the V_{NO} can be yielded as:

$$V_{NO} = -\frac{S_{a1} + S_{b1} + S_{c1}}{3} V_{dc1} + \frac{S_{a3} + S_{b3} + S_{c3}}{3} V_{dc2} \tag{2.18}$$

Then, two capacitor currents (i_{c1} & i_{c2}) are derived as:

$$\begin{cases} i_{c1} = C\dfrac{dV_{dc1}}{dt} = i_p - i_{dc} = S_{a1}i_a + S_{b1}i_b + S_{c1}i_c - i_{dc} \\ i_{c2} = C\dfrac{dV_{dc2}}{dt} = i_n - i_{dc} = -S_{a3}i_a - S_{b3}i_b - S_{c3}i_c - i_{dc} \end{cases} \tag{2.19}$$

As a consequence, the state equation for the 3L-NPC converter in the static reference frame can be expressed by:

$$\dot{X} = AX + BU \tag{2.20}$$

where $X = \begin{bmatrix} i_a & i_b & i_c & V_{dc1} & V_{dc2} \end{bmatrix}^T$

$$A = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & -\frac{1}{L}(S_{a1} - \frac{S_{a1}+S_{b1}+S_{c1}}{3}) & -\frac{1}{L}(S_{a3} - \frac{S_{a3}+S_{b3}+S_{c3}}{3}) \\ 0 & -\frac{R}{L} & 0 & -\frac{1}{L}(S_{b1} - \frac{S_{a1}+S_{b1}+S_{c1}}{3}) & -\frac{1}{L}(S_{b3} - \frac{S_{a3}+S_{b3}+S_{c3}}{3}) \\ 0 & 0 & -\frac{R}{L} & -\frac{1}{L}(S_{c1} - \frac{S_{a1}+S_{b1}+S_{c1}}{3}) & -\frac{1}{L}(S_{c3} - \frac{S_{a3}+S_{b3}+S_{c3}}{3}) \\ \frac{S_{a1}}{C} & \frac{S_{b1}}{C} & \frac{S_{c1}}{C} & 0 & 0 \\ -\frac{S_{a3}}{C} & -\frac{S_{b3}}{C} & -\frac{S_{c3}}{C} & 0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L} \end{bmatrix}$$

$$U = \begin{bmatrix} e_a & e_b & e_c & i_{dc} & i_{dc} \end{bmatrix}^T$$

It can be clearly seen that the switching function produced by a modulation strategy determines the converter's output variables, such as phase current and line voltage, as well as the voltage between neutral-point of the load and midpoint of DC bus, i.e., the common-mode voltage that will be discussed in Chapter 5. Consequently, the PWM technique studied in this thesis is significant for the high-performance operation of the 3L-NPC converter applied in the aircraft S/G system.

2.5 Conclusions

This Chapter overviews the MEA electric starter-generator system. Before fulfilling the take-off condition, air needs to flow into the engine with the help of compressors. When the engine speed reaches 10% of its maximum speed, fuel will be injected into the combustion chamber, along with igniting its mixture with the air. Compared with the conventional engine startup methods, the electric starter is operated by an onboard DC bus or ground power supply. Electrical power generation has been conventionally performed by electric machines interfaced to an accessory gearbox which is typically very costly, requires intensive maintenance, thus leading to reliability problems. By contrast, variable speed variable frequency is a novel solution offered by the MEA concept, which provides the possibility of a direct connection between generator and engine, thereby reducing unnecessary bulky gearbox in the aircraft. This technique has been applied in the latest wide-body commercial aircraft, such as the Airbus 350 and the Boeing 787. In order to converting energy from mechanical to electrical, a high-performance electric motor is required. Nowadays, increasing application fields focus on PMMs because of high-efficiency and high-robustness compared with other machine types. As a consequence, it allows the PMM to be utilised as a S/G by controlling the electrical power flow into and from the aircraft electrical bus, depending on the operational modes.

Our own developed AEGART project provides a new power generation unit for the MEA. Different types of three-level topologies are reviewed, together with power loss comparison between two-level and three-level DNPC for the design. The general

requirements of starter and generation modes have been outlined in this Chapter. The laboratory implementations are based on a high-speed PMSM and a 3L-NPC converter. Also, the VSVF power generation type is adopted. This design layout brings opportunities to drive aircraft engines in the startup process and generate electrical power to onboard loads in generation mode. The speed of machine has to be controlled in the startup process while DC-link power is controlled in power generating conditions. The FW control is important for both cases in order to maintain controllability of the power system. Moreover, the PWM modulator with a dedicated modulation strategy sends firing pulses to the converter during the entire-speed range operation. In order to have a better understanding of the adopted 3L-NPC topology, the converter's configuration, commutation mode, space vector generation and mathematical model have been introduced. Given that high-performance pulse trains enable the multilevel converter-fed aerospace motor drives operating in the high-speed region with fewer power losses, reduced common-mode voltage, balanced capacitor voltages and a higher DC-link utilization ratio, the modulation technique improvement for the aircraft three-level power generation unit within the AEGART project form the subject of this thesis. Overall, this Chapter has elaborated the essential research background and established the methodologies and topologies which will be used as a basis for the study in the following Chapters.

Chapter 3

Conventional Modulation Strategies and Capacitor Voltage Control Methods for Three-Level NPC Converter

In this Chapter, the conventional modulation strategies and capacitor voltage control methods for the 3L-NPC converter are introduced. The effect of neutral-point current is studied based on the nearest-three-space-vector modulation scheme. The source of neutral-point voltage ripple is analysed from the carrier-based pulse-width-modulation scheme viewpoint. The nearest-three-virtual-space-vector scheme that features average zero neutral-point currents is also discussed. In addition, the literature review of existing capacitor voltage control methods is presented.

3.1 Introduction

Since the 3L-NPC converter serves as a crucial component in the main path of energy flow in the aircraft S/G systems, it has a significant influence on the reliability and efficiency of the onboard EPS [2]. However, the selected power electronics converter has the inherent problem of unbalanced NP voltage due to split DC-link capacitor bank [81–83]. The NP voltage drift and oscillation issues lead to extra

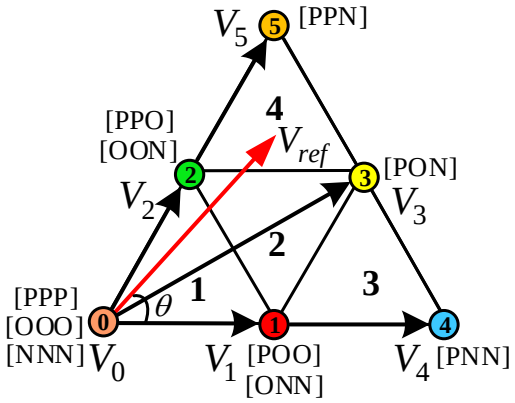


Figure 3.1: Space vector diagram of the conventional NTV modulation scheme

over-stress across switching devices. Also, in order to alleviate low-order harmonics, the filter size and weight have to be compromised in the design and manufacturing [84–86]. Even though the self-balancing phenomenon can be observed and analysed, its strength is constrained by system parameters, PWM pattern and sampling frequency, etc. [87–89]. Based on the above reasons, a modulation technique with superior capacitor voltage balancing control becomes a simple but powerful alternative to overcome these deficiencies.

3.2 The Nearest-Three-Space-Vector Modulation Scheme

3.2.1 The Modulation Principle

To generate three-level output voltages, the converter's switches need to be periodically turned on and off over a line cycle. Thus, the PWM algorithm is essential for the whole system. The nearest-three-space-vector (NTV) modulation scheme divides each sector into four parts [81, 82], as shown in Figure 3.1. Taking the first sector as an example, assuming that the reference voltage vector is located in subsector 4. this method uses V_2, V_3 and V_5 to synthesize V_{ref}. According to the volts-second principle, the corresponding duty cycle of these space vectors can be calculated. Then, the next step is to arrange switching sequence based on the

Table 3.1: The relationship among space vectors, switching states and NP currents

Space Vector	Switching States		NP Currents	
Zero Vector	[PPP] [OOO] [NNN]		–	
Small Vector	P-type	N-type	P-type	N-type
	[POO]	[PNN]	$-I_a$	I_a
	[PPO]	[ONN]	I_c	$-I_c$
	[OPO]	[NON]	$-I_b$	I_b
	[OPP]	[NOO]	I_a	$-I_a$
	[POP]	[ONO]	I_b	$-I_b$
	[OOP]	[NNO]	$-I_c$	I_c
Medium Vector	[PON]		I_b	
	[OPN]		I_a	
	[NPO]		I_c	
	[NOP]		I_b	
	[ONP]		I_a	
	[PNO]		I_c	
Large Vector	[PNP] [PPN] [NPN] [NPP] [NNP] [PNP]		–	

optimal commutation principle [70]. By doing so, when the output voltage vector produced by the inner current loop rotates over a fundamental cycle, all firing pulses can be hence generated as the gating signals, and sent to each switching device.

3.2.2 The Effect of Neutral-Point Current

When these semiconductor devices operate, the AC-side current will flow through them. This indicates the adopted modulation method has an influence on the flowing direction of phase current. In terms of the space vector modulation (SVM) method, the switching states signify different types of switches connecting to the DC-link terminals, which in turn determines the magnitude and direction of NP currents [70]. For the conventional NTV scheme, a space vector can be composed of one or more combinations of different switching states.

Table 3.1 details the corresponding relationship among space vectors, switching

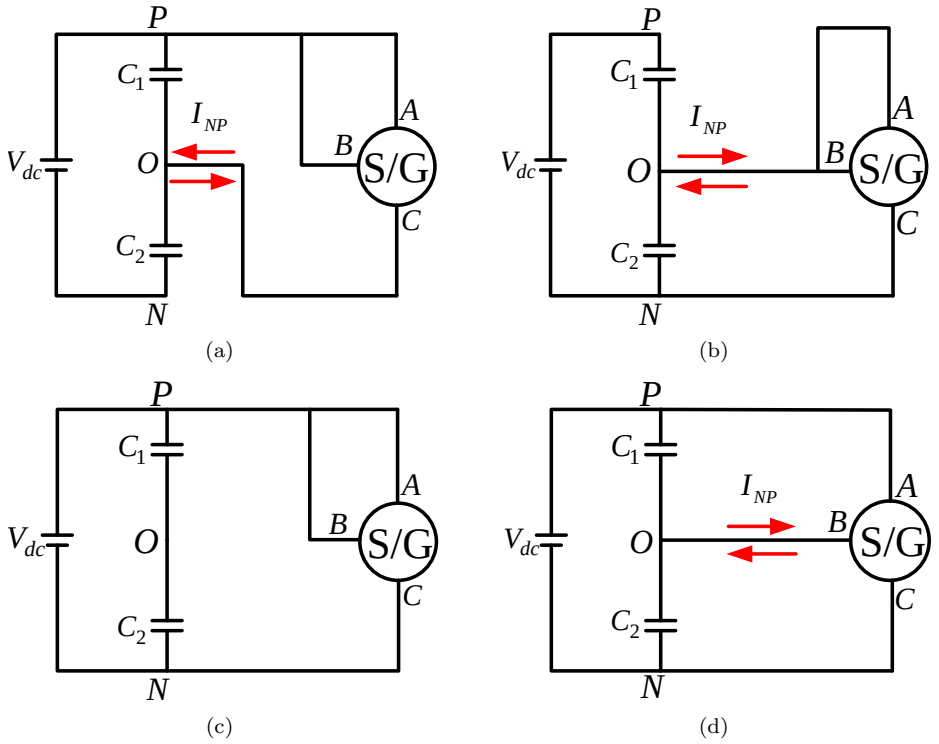


Figure 3.2: The effect of space vectors on NP current (a)[PPO] (b) [OON] (c) [PPN] (d) [PON]

states and NP currents. It can be seen that zero and large vectors have no impact on NP voltage since there is no current associated with the centre tap of DC-link. For small vectors, their NP currents produced by two redundant switching states are complimentary with opposite directions. Each medium vector is only associated with one switching state and therefore one type of NP current. This implies that the medium vector has a special impact on two capacitor voltages, which cannot be offset by itself.

Taking the case of Figure 3.1 as an example, the specific switch connections used to approximate the reference voltage vector denoted as V_{ref} are shown in Figure 3.2. As shown, except for the large vector [PPN], other space vectors affect NP voltage. In terms of Sector-I, the average NP current over a switching cycle is given by [90]:

$$\overline{I_{NP}} = D \cdot I_{abc} \tag{3.1}$$

where D= $[(d_{onn} - d_{poo})\ d_{pon}\ (d_{ppo} - d_{oon})]$ and I_{abc}= $[i_a\ i_b\ i_c]^T$

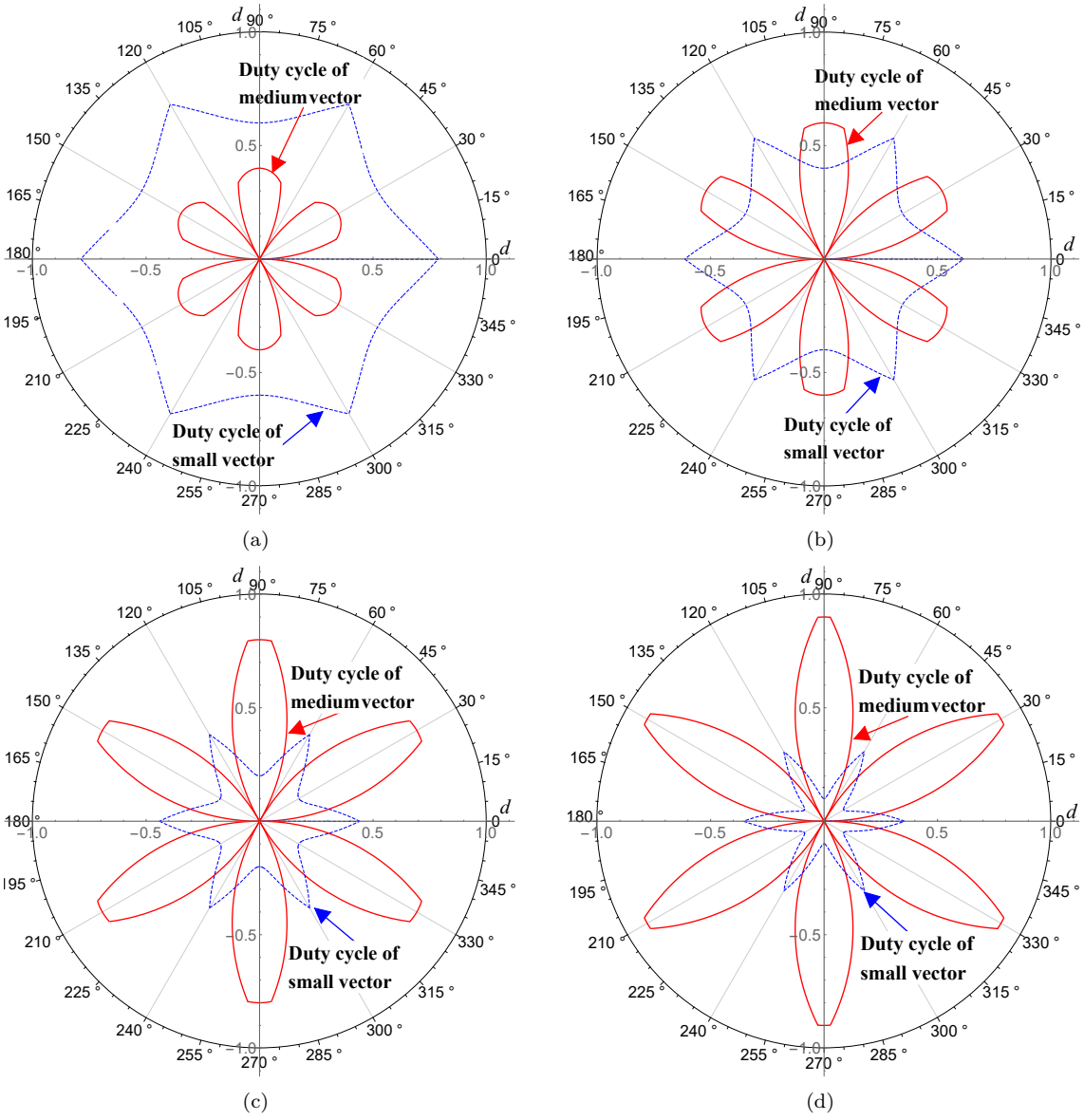
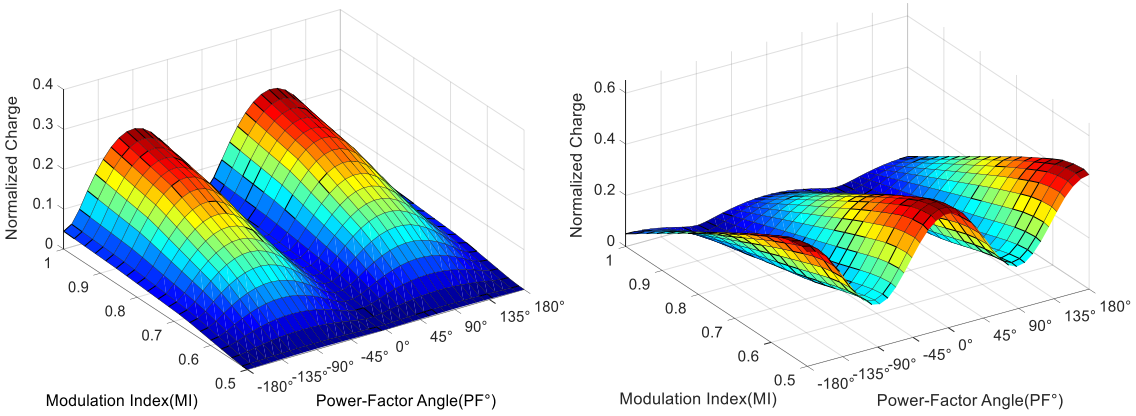


Figure 3.3: The duty cycle polar plot of small and medium vectors under (a) MI=0.7 (b) MI=0.8 (c) MI=0.9 (d) MI=0.95

With the corresponding switching states and NP currents listed in Table 3.1, the following equation can be attained as:

$$\overline{I_{NP}} = \mu \cdot d_{ppo} \cdot i_c + d_{pon} \cdot i_b + (1-\mu) \cdot d_{oon} \cdot (-i_c), \quad \mu \in [0,1] \tag{3.2}$$

In equation (3.2), μ represents the allocation ratio of the small vector [PPO] and [OON] in the dwell-time domain. Therefore, the capacitor voltage deviation within



(a) (b)

Figure 3.4: Normalized charge in the NP by: (a) medium vectors (b) small vectors

a PWM period can be calculated as:

$$\Delta V_{dc} = \frac{1}{C} \int_{t=0}^{t=T_s} \overline{I_{NP}} \cdot dt \tag{3.3}$$

where C refers to the capacitance of DC-link and T_s denotes a switching cycle.

In the case of an average non-zero NP current, by using the allocation coefficient μ in equation (3.2) properly, two small vectors can be proportionally employed to compensate for extra NP electric charge produced by medium vectors.

To reveal the participation of small and medium vectors over a fundamental cycle, the duty cycles of these space vectors are plotted in Figure 3.3. As shown, medium vectors become predominant in the high modulation index region. Together with equations (3.2) and (3.3), it can conclude that capacitor voltage balancing control capability by small vectors is weakened when a converter's output voltage is high.

According to equations (3.1)-(3.3), the normalized amplitude of NP charge produced by small and medium vectors can be calculated and displayed in Figure 3.4. As can be seen, along with increasing modulation index and directing toward zero power factor, medium vector shows its significant impact on charging NP potential, as opposed to small vector. In addition, Figure 3.5 presents the total normalized NP electric charge caused by the NTV scheme. It can be observed that the net amount of NP electric charge is much accumulated when the modulation index rises and power factor angle towards to $\pm 90°$. Consequently, such operation scenarios are the

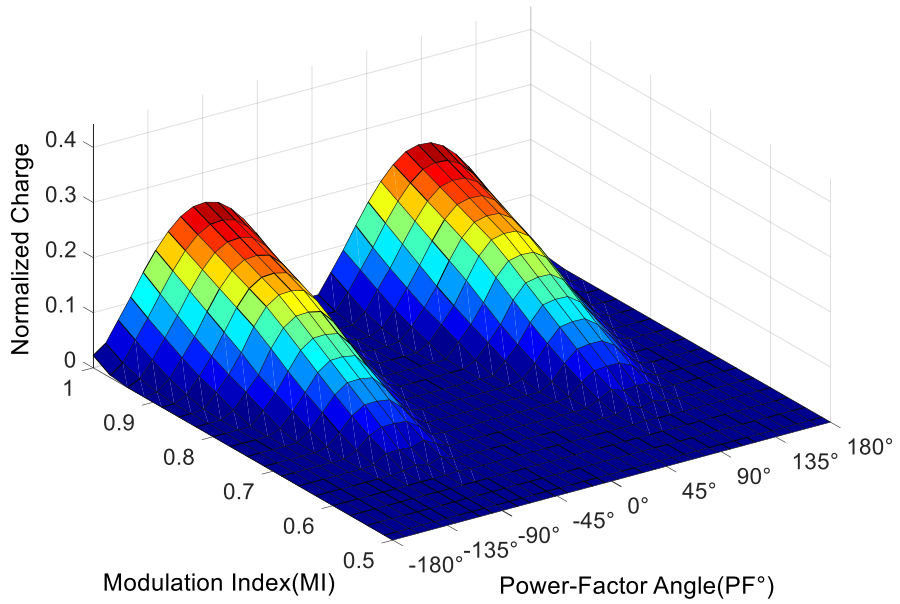


Figure 3.5: Total normalized NP charge as a function of modulation index and power factor

worst working conditions for the aircraft ESG system, and therefore require special attention. This thesis will carefully consider that issue and handle the NP voltage fluctuation and deviation properly by advanced modulation techniques proposed in the following Chapters.

3.3 Carrier-Based Modulation Scheme

3.3.1 The Modulation Principle

The carrier-based pulse-width-modulation (CBPWM) scheme utilizes the equivalence between modulation signals and a series of PWM pulses in each fundamental period [91–93]. The mechanism can be elaborated in Figure 3.6. That is, three-phase modulated waveforms V_{mx} ($x \in \{A, B, C\}$) are compared with two carrier waveforms (V_{c1} & V_{c2}). More specifically, when V_{mx}'s magnitude is larger than V_{c1} and V_{c2}, binary value of S_{x1} and S_{x2} are both '1'; when V_{mx}'s magnitude is larger than V_{c2} but smaller than V_{c1}, binary value of S_{x2} and S_{x3} are both '1'; when V_{mx}'s magnitude is smaller than V_{c1} and V_{c2}, binary value of S_{x3} and S_{x4} are both '1'. It is noted that S_{x1} and S_{x3} are complimentary and this principle is also applicable to S_{x2} and S_{x4},

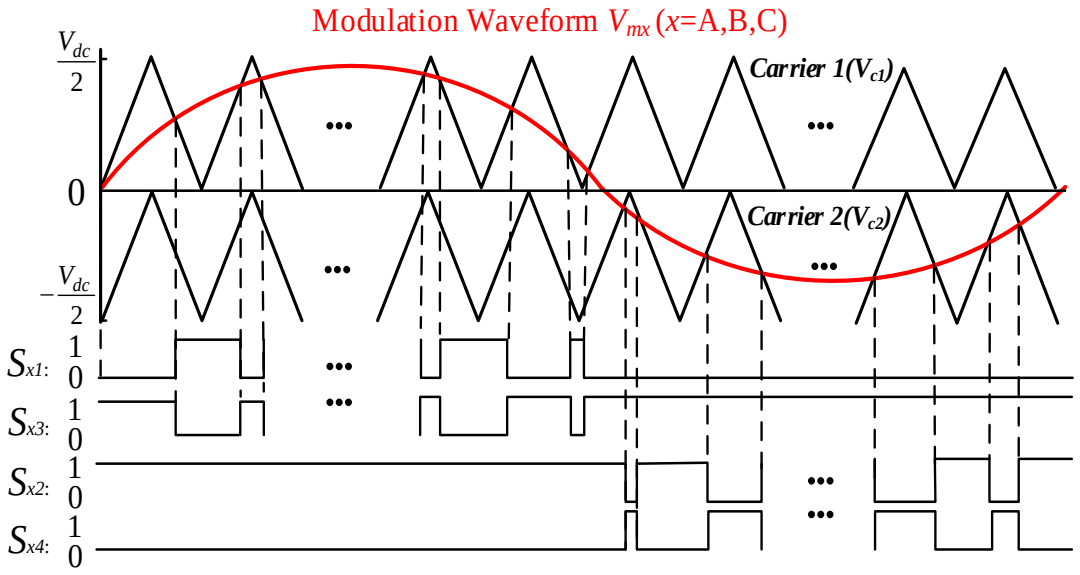


Figure 3.6: Modulation signals and their corresponding switching functions

in which $S_{x1\sim x4}$ refer to the gating signals of $VT_{x1\sim x4}$ shown in Figure 2.14.

3.3.2 The Source of Neutral-Point Voltage Oscillation

For the consideration of simplicity, the commonly-used sinusoidal PWM (SPWM) scheme with third-order harmonic injection [94–96] is taken as an example to analyse in the following text. It can be clearly seen from Figure 3.7 that the modulation signals of the SPWM scheme determine switching states, thereby generating three-level output voltages presented in Table 2.2.

To reveal the NP voltage fluctuation caused by the modulation method, it is assumed that the ESG system is electrically symmetrical and balanced. Then, the three-phase modulation signals can be expressed as follows:

$$\begin{cases} V'_{ma} = V_{ma} + V_z = m \cdot \cos(\theta) + V_z \\ V'_{mb} = V_{mb} + V_z = m \cdot \cos(\theta - 2\pi/3) + V_z \\ V'_{mc} = V_{mc} + V_z = m \cdot \cos(\theta + 2\pi/3) + V_z \end{cases} \tag{3.4}$$

where m is the modulation index and V_z refers to the zero-sequence voltage (ZSV) component calculated by [92, 93]:

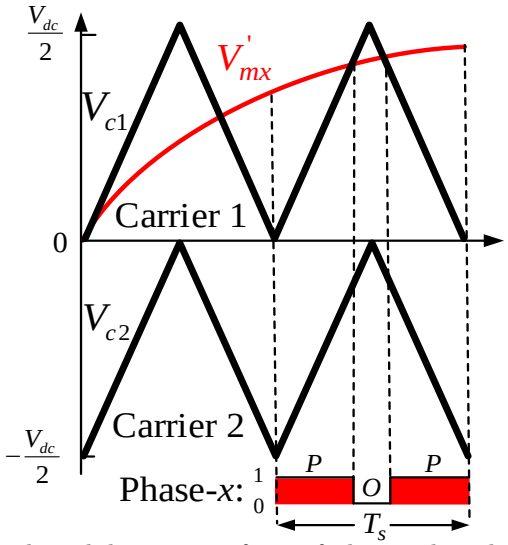


Figure 3.7: Carrier and modulation waveform of phase-x based on the CBPWM scheme

$$V_z = -\frac{\max(V_{ma}, V_{mb}, V_{mc}) + \min(V_{ma}, V_{mb}, V_{mc})}{2} \tag{3.5}$$

Similarly, the relationship of three-phase currents meets:

$$\begin{cases} i_a = I_o \cos(\omega t - \varphi) \\ i_b = I_o \cos(\omega t - \varphi - 2\pi/3) \\ i_c = I_o \cos(\omega t - \varphi + 2\pi/3) \\ i_a + i_b + i_c = 0 \end{cases} \tag{3.6}$$

where ω represents the angular frequency, I_0 denotes the magnitude of phase current and φ indicates power factor angle.

With regards to the CBPWM scheme, the average current flowing to the centre tap of DC-link within a carrier period satisfies [97]:

$$\begin{cases} \overline{I_{NP}} = \sum\limits_{x=a,b,c} d_{xo} \cdot i_x \\ 0 \le d_{xo} \le 1 \end{cases} \tag{3.7}$$

where d_{xo} denotes the phase duty cycle of switching state [O].

Moreover, the authors in [97] pointed out that if the frequency of carrier waveform

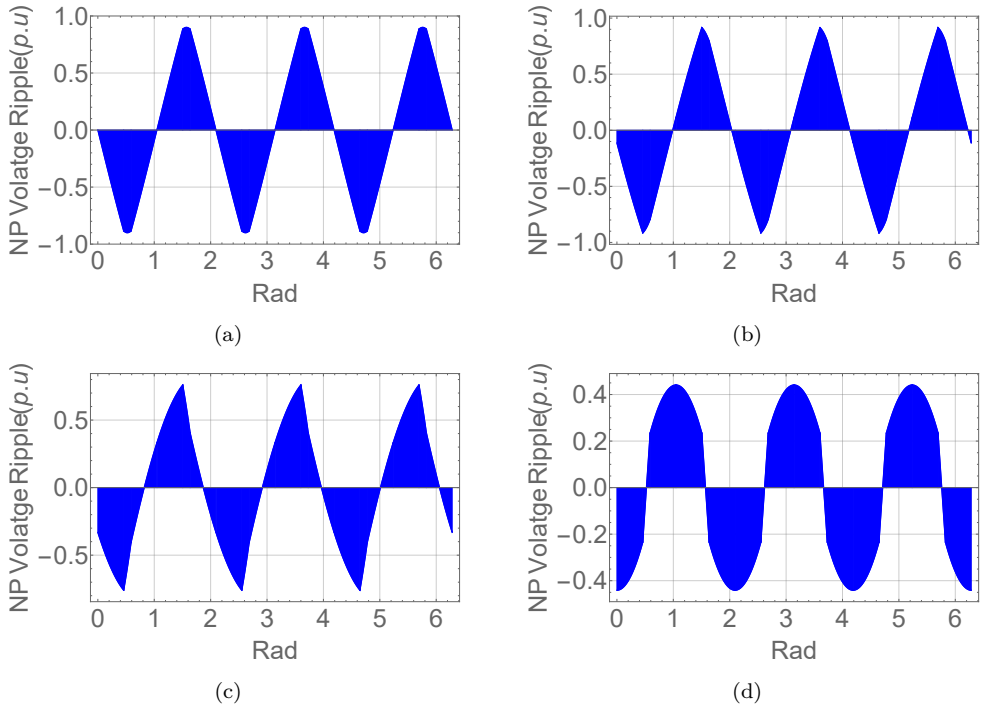


Figure 3.8: Normalized NP voltage oscillation: (a) MI=0.90 and PF=0 (b) MI=0.90 and PF=0.25 (c) MI=0.90 and PF=0.75 (d) MI=0.90 and PF=1

is much higher than that of modulation waveform, the relationship between d_{xo} and V'_{mx} can be given by:

$$d_{xo} = 1 - \left|V'_{mx}\right|, \quad x = \{a,\ b,\ c\} \tag{3.8}$$

By substituting equations (3.6) and (3.8) into equation (3.7), the general expression of NP currents can be derived as:

$$\begin{aligned} \overline{I_{NP}} &= \sum_{x=a,b,c} (1 - \left|V'_{mx}\right|) \cdot i_x \\ &= -m \cdot I_o \cdot [|\cos(\omega t) + V_z| \cos(\omega t - \varphi) + \\ &|\cos(\omega t - 2\pi/3) + V_z| \cos(\omega t - \varphi - 2\pi/3) + \\ &|\cos(\omega t + 2\pi/3) + V_z| \cos(\omega t - \varphi + 2\pi/3)] \end{aligned} \tag{3.9}$$

Then, it is not difficult to quantify the capacitor voltage fluctuation based on equations (3.3) and (3.9). The normalized NP voltage oscillation with a modulation index of 0.90 at different power factor angles (PF=0, 0.25, 0.75 and 1) are shown in Figures 3.8(a)-(d). It can be clearly seen that the frequency of this undesirable NP voltage ripple is characterized by three times of the fundamental frequency. This

might have detrimental effects on the stability of the onboard EPS since each capacitor bank will feed the onboard loads in future bipolar HVDC structure (±270VDC). Although the low-frequency NP voltage oscillation can be suppressed by adding a large capacitor or an isolated DC voltage source [98, 99], extra cost and bulky size are inevitable for such a solution, particularly for aerospace applications.

Furthermore, it is worth noting that the DC component of NP potential fluctuation results in a static voltage error between two capacitors, whereas its AC component results in a capacitor voltage ripple which degrades its lifetime. In summary, balanced capacitor voltages with eliminated NP potential oscillation in the studied 3L-NPC converter-fed motor drive systems are two critical tasks for the employed modulation technique.

3.4 Virtual-Space-Vector Modulation Scheme

3.4.1 The Modulation Principle

Compared with the NTV scheme, the original nearest-three-virtual-space-vector (NTV^2) scheme proposed in [100, 101] divides each sector into five parts, as shown in Figure 3.9. The method applies a series of virtual space vectors (VSVs) which is synthesized by basic space vectors with a specific proportion. The definition of zero and large vectors, denoted as V_0, V_{L1} and V_{L2}, are the same as the NTV scheme, whereas V_{S1}, V_{S2} and V_{M1} are virtual small and medium vectors defined by:

$$\begin{cases} V_{S1} = (V_{[\mathrm{POO}]} + V_{[\mathrm{ONN}]})/2 \\ V_{S2} = (V_{[\mathrm{PPO}]} + V_{[\mathrm{OON}]})/2 \\ V_{M1} = (V_{[\mathrm{ONN}]} + V_{[\mathrm{PON}]} + V_{[\mathrm{PPO}]})/3 \end{cases} \tag{3.10}$$

Similar to the space vector composing process of the NTV scheme, the NTV^2 scheme deploys the nearest-three VSVs to approximate V_{ref}. When V_{ref} is located in subsector 4, V_{L1}, V_{L2} and V_{M1} dotted with numbers '3', '4' and '5' shown in Figure 3.9 are selected. And then, the corresponding pulse trains are symmetrically

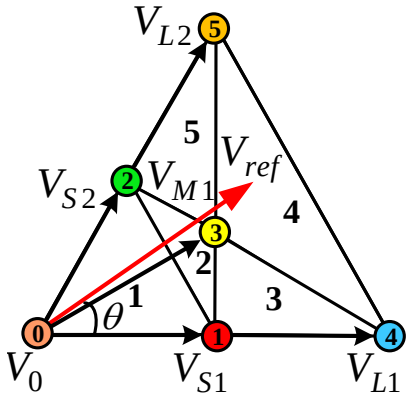


Figure 3.9: Space vector diagram of the conventional NTV^2 modulation scheme

arranged during each PWM cycle.

3.4.2 Average Zero Neutral-Point Current

Here, the reference voltage vector approximation process in Sector-I is chosen as a representative example to explain the superiority of the NTV^2 modulation strategy.

As can be seen from the definition of NTV^2 concept introduced in the last subsection and corresponding NP currents detailed in Table 3.1, it is known that virtual small vectors represented as V_{S1} and V_{S2} evenly employ P-and N-type small vectors, and therefore produce average net-zero NP current. Moreover, according to equation (3.6), the synthesized virtual medium vector, denoted as V_{M1}, also has no impact on NP voltage since the sum of NP currents produced by [ONN], [PON] and [PPO] equals zero [100], i.e., i_a+i_b+i_c=0.

Consequently, unlike the conventional NTV and CBPWM schemes, the NTV^2 scheme can perfectly address the capacitor voltage imbalance problem caused by NP current for all load conditions.

3.5 Existing Capacitor Voltage Balancing Control Methods

In order to resolve the DC-link capacitor voltage deviation problem in the 3L-NPC converter, several advanced modulation techniques have been developed by

researchers in the past few years [100, 102–121]. These methods can be classified into two categories: 1) SVM scheme [100, 102–110, 120, 121] and 2) CBPWM scheme [111–119,122,123]. The map of existing NP voltage balancing control strategies is elaborated in Figure 3.10.

3.5.1 SVM Strategy-Based Approaches

The SVM scheme can be classified into three types. The first one is the NTV scheme [81], which employs the nearest-three space vectors to compose the target. According to the unbalanced range of capacitor voltages, an improved NTV scheme has been proposed in [104, 120], where a NP voltage feedback control loop is added to determine a predefined switching sequence that is only composed of P or N-type small vectors. But, it cannot avoid unfavourable low-frequency NP voltage oscillation generated by the medium vector for the reason of its predominant participation [90]. In order to resolve this problem, the second type method named the selected three vector (STV) scheme is presented in [121]. Furthermore, a modified STV modulation scheme proposed in [105] abandons medium vectors to balance NP potential and suppress the oscillation for high-speed motor drives. The third type is developed on the basis of the classic NTV^2 modulation concept that is firstly proposed by Sergio Busquets-Monge *et al* [100]. This technique aims to produce an average zero NP current in each switching period, thereby gaining balanced capacitor voltages in all range of modulation indices and power factors. Nevertheless, the capacitor voltage balancing control is not considered for the original method, which constrains its application if any disturbance occurs in the DC-link. This shortcoming has been overcome by the study reported in [103]. With the help of DC-link voltage feedback control, the algorithm brings an opportunity to keep two capacitor voltages balanced, but subsector identification and dwell time determination are complicated for the calculation in the α-β reference frame which will be presented in detail in Chapter 4. In the work of [106], an improved NTV^2 scheme has been explored, which features simple subsector repartition.

Besides, the NTV^2 technique has been well developed to incorporate more ad-

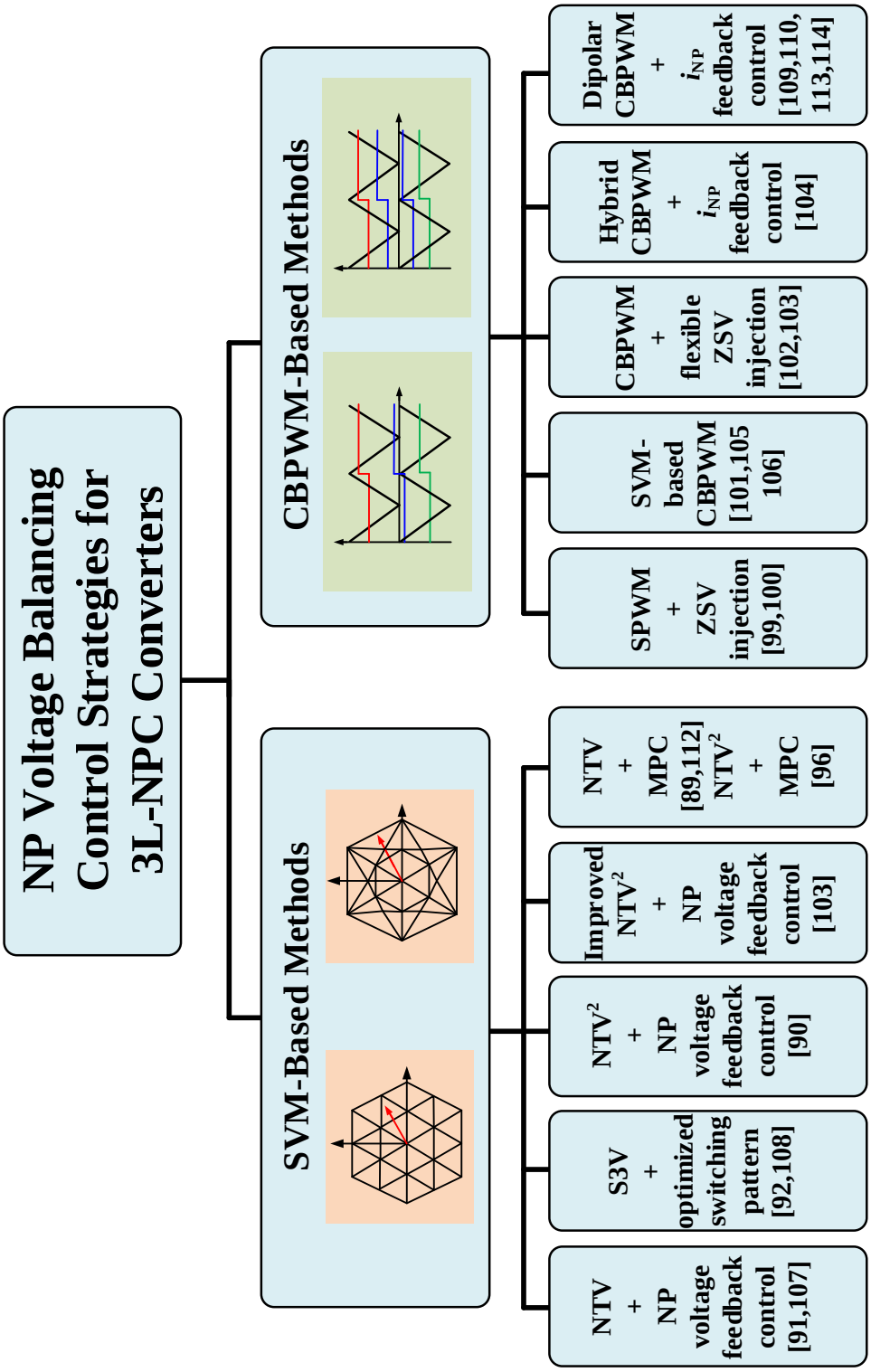


Figure 3.10: Map of existing NP voltage balancing control strategies

vantages, such as CMV suppression [107, 110] and switching losses reduction [108]. In order to select optimal VSVs with a fast dynamic response, a more recent study by [109] proposes a discrete space vector modulation (DSVM) scheme based on the MPC scheme. However, it is notable that total harmonic distortion (THD) of phase current highly depends on the number of virtual switching states [124]. More importantly, the heavy computational burden, with 33 switching states, is another challenge for the method. In order to simplify the calculation process, a vector-shifted model [102] is proposed to reduce execution time taken by the MPC-based implementation. The MPC-based PWM scheme has also been explored for five-level ANPC converter-fed PMSM drive systems [125] and power grid-tied seven-level hybrid inverter systems [126].

3.5.2 CBPWM Strategy-Based Approaches

Compared with the SVM scheme, the CBPWM scheme is carried out due to its simplicity and easy implementation. In [111], a high-performance modulation strategy is proposed to eliminate low-frequency NP voltage fluctuation. In [112], an optimized ZSV injection method is presented for correcting drifted capacitor voltages. In [113], a voltage offset injection solution is reported for a single-phase 3L-NPC converter. A method based on discontinuous PWM (DPWM) strategy has been proposed for mitigated NP voltage oscillation and less switching loss in high-power applications [114]. Despite that, the effectiveness of these modulation schemes is still limited under low power factor conditions. In [115], a novel CBPWM scheme with appropriate ZSV injection offers a chance to operate traction drives in the overmodulation region. To pursuit balanced NP voltage and power loss reduction, a flexible CBPWM method is proposed in [116]. In [117], the NP voltage variation range is narrowed to reduce switching losses. However, it can be seen from the experimental results that, along with the reduction of capacitor voltage variation band under deep modulation index and low load angle, the amounts of power loss become similar to that of the conventional three-level modulation scheme. In [122], a CBPWM featured with double modulation waves is studied for NP voltage ripple elimination

and common-mode voltage reduction. In [123], a dipolar CBPWM scheme is proposed to control two capacitor voltages and mitigate low-frequency oscillation for three-phase four-wire systems. Furthermore, SVM-based CBPWM algorithms have been explored from the ZSV injection viewpoint, thereby settling the imbalance problem [118, 119]. In [127], a dual-mode NP voltage balancing control method is proposed, which analytically calculates compensated NP currents according to the operating conditions of the converter. In [128], a simple PI controller-based NP voltage balance method is proposed for a 3L-NPC inverter with a small DC-link capacitor. The controller output is used to calculate the modified reference signals which are used for carrier-based implementation of the modulation strategy. Nevertheless, the control parameters need to be regulated in advance.

3.6 Conclusions

In this Chapter, the NP voltage imbalance and oscillation problems of the 3L-NPC converter have been comprehensively investigated based on the conventional SVM and CBPWM schemes.

It has been shown that phase current flowing in and out the midpoint of DC-link impacts the state of NP potential. For the NTV modulation method, the NP voltage drift tends to become aggravated under high modulation index and low power factor angle conditions. From the viewpoint of the third-order harmonic injected SPWM scheme, the reason for the low-frequency NP voltage ripple has been explained, which is characterized by three times of fundamental frequency. Since the NTV scheme is essentially equivalent to the conventional CBPWM scheme, both the NTV and CBPWM method lead to degraded converter output performance to some extent.

As the NTV^2 scheme can achieve capacitor voltage balance for all load angles and more choices of output space vector, the VSV-based modulation scheme shows its exceptional performance for 3L-NPC converters, particularly for operating conditions of high modulation index and low power factor. Although this scheme can keep two capacitor voltages' inherent balance, the original approach cannot provide

extra electric charges to compensate for accumulated potential bias in the NP, which is significant for practical applications if the NP voltage initially drifts away.

In addition, the existing capacitor voltage balancing control methods are reviewed, and their advantages and disadvantages are discussed in detail. At last, a full picture of the modulation tree is presented.

In summary, the analysis and investigation in this Chapter show that, in order to enhance the overall performance of the converter-fed high-speed motor drives, more advanced modulation techniques need to be carefully designed for the 3L-NPC converter. Otherwise, the developed ESG system can hardly become competitive for MEA applications.

Chapter 4

A Fast Calculation Method for the Pulse-Width-Modulation

In this Chapter, a fast calculation approach is introduced to simplify the PWM signal generation process, which can benefit the efficiency of the proposed modulation strategy in this thesis.

4.1 Introduction

As presented in Chapter 3, the implementation of a SVM strategy costs a lot of computational time in terms of dwell time calculation and space vector's position identification, particularly for the NTV^2 based approaches [100, 101, 106]. This approach features multi-segment pulse trains and complex subsector reparation. In the literature, there are several methods to simplify modulation process. In [129], the authors proposed a three-phase imaginary coordinate system to ease the computation burden of multilevel converters. This system has two parts: one is the determination of the fundamental components in the output according to reference voltage vector; the other is the selection of redundant switching states to achieve the zero sequence components.

In [102, 125], the authors decompose a three-level/five-level hexagonal system into two-level/three-level system, respectively, to reduce the heavy computational

Table 4.1: Existing simplified PWM methods

Simplification Tools	Characteristics
Three-phase imaginary coordinate system [129]	Independent reference vector synthesis and zero-sequence voltage injection
Shifted hexagonal system [102, 125]	Low execution effort by limiting switching states in a shifted space vector diagram
a-b-c coordinate system [130]	No need to make region judgment and dwell time variation always satisfies certain rules
Two-level equivalent SVD [131]	No trigonometry, coordinate transformation and sector/subsector detection
g-h coordinate system [132, 133]	Dwell time is expressed as a function of algebraic variables

burden of many MPC schemes. In [130], a simplified SVM algorithm based on the *a-b-c* coordinate system for three-level converters has been studied to avoid sector determination and dwell time calculations. The algorithm directly calculates the circuit state change time using the relationship between the coordinate components, which eases the computational effort. In [131], the two-level equivalent space-vector-diagram (SVD) is utilized to overcome computational burden caused by the traditional SVM process. This method avoids trigonometry, coordinate transformation and sector/subsector detection.

The calculation adopted in the thesis for the *g-h* reference frame, by rotating the β-axis 30-degree clockwise and maintaining the α-axis, has been reported in [132, 133]. Compared with the widely-used calculation approach based on the conventional α-β reference frame, this solution abandons the orthogonal reference frame and rotating angle of reference voltage vector, and establishes all the space vectors in a new plane. Meanwhile, the coordinate of all space vectors are expressed as rational numbers, which can greatly reduce the computational efforts with regard to sector/subsector identification and dwell time determination. The gating signal generation in the PWM modulator can then be executed in a simple way. The cumbersome trigonometric functions used by the α-β reference frame may take up extra microcontroller resource during a PWM interrupt routine. As a result, the

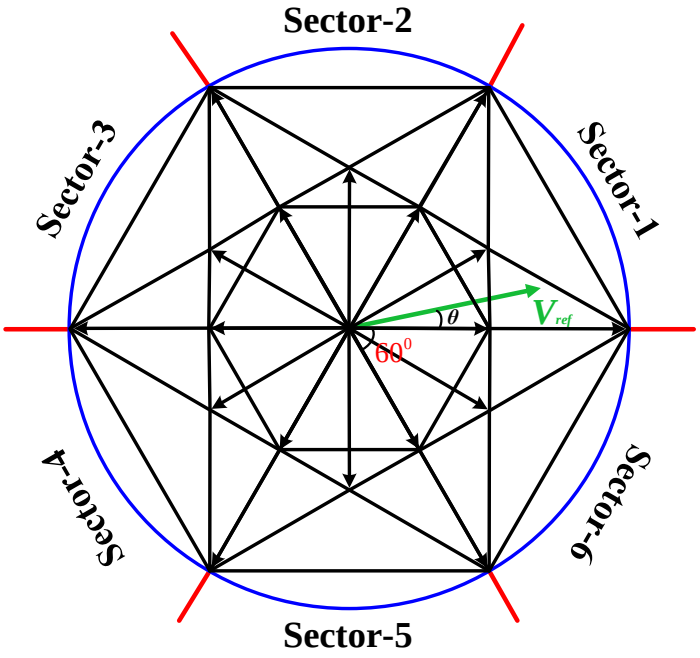


Figure 4.1: Sector identification diagram

g-h reference frame was chosen as a candidate to simplify modulation processes, especially for advanced modulation techniques in this work. Table 4.1 summerises the existing PWM simplification methods.

Considering the complexity of the conventional NTV^2 scheme, the modulation processes based on the α-β reference frame and the g-h reference frame are taken as a representative example to compare in the following section.

4.2 The Conventional α-β Reference Frame

4.2.1 Sector and Subsector Identification

The sector identification method for 3L-NPC converters is similar to the two-level counterpart. It is based on the rotating angle of the reference voltage vector with the sector number that can be defined from I to VI in every 60° of a fundamental period, as shown in Figure 4.1. Thus, multiples of 60° configure the angle range of each sector. For example, the rotating angle associated with Sector-III ranges from 2×60° to 3×60°. In other words, the angle range for Sector-N can be expressed as

Table 4.2: Sector number identification criteria

Rotating Angle	Sector Number
$0° \leq \theta < 60°$	I
$60° \leq \theta < 120°$	II
$120° \leq \theta < 180°$	III
$180° \leq \theta < 240°$	IV
$240° \leq \theta < 300°$	V
$300° \leq \theta < 360°$	VI

(N-1)×60°∼N×60°. The more specific identification criteria have been summarised in Table 4.2. In order to find the sector number N more conveniently, a floor-function can be used:

$$N = floor(\frac{\theta}{\pi/3}) \tag{4.1}$$

where θ is the rotating angle of the reference voltage vector.

Due to the further partition of each sector, subsector numbers indicating a triangle which the reference voltage vector will fall into is also required to identify. The work discussed in [103] provides a method to find the position of the reference voltage vector. As shown in Figure 4.2, V_{ref} can be synthesized by V_{S1}&$V_{\beta 1}$ and V_{L1}&$V_{\beta 2}$, as given by equations (4.2) and (4.3). The introduced two auxiliary angles β_1 and β_2 are helpful for finding the subsector number.

$$\overrightarrow{V_{ref}} \angle \theta_{ref} = \overrightarrow{V_{S1}} \angle 0 + \overrightarrow{V_{\beta 1}} \angle \beta_1 \tag{4.2}$$

$$\overrightarrow{V_{ref}} \angle \theta_{ref} = \overrightarrow{V_{L1}} \angle 0 + \overrightarrow{V_{\beta 2}} \angle \beta_2 \tag{4.3}$$

where $\overrightarrow{V_{\beta 1}}$ and $\overrightarrow{V_{\beta 2}}$ are two auxiliary space vectors.

By splitting equations (4.2) and (4.3) into real and imaginary parts, the value of the angles can be derived individually. For example, if V_{ref} falls into subsector 4 of Sector-I, it can move along the triangle side and boundary conditions of auxiliary angles β_x can be calculated, here, $\beta_1 = 90°$ and $\beta_2 = 150°$. Due to the six-fold symmetry, the criteria for identifying subsectors 1-5 in the first sextant are formed,

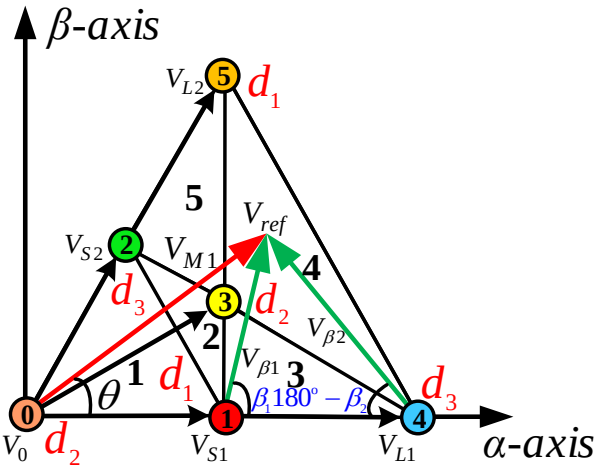


Figure 4.2: Subsector identification diagram in Sector-I

Table 4.3: Subsector number identification criteria

$\beta 1$	$\beta 2$	Subsector
>120°	>150°	1
≤120°&>90°	≥150°	2
≤90°	≥150°	3
≤90°	<150°	4
>90°	<150°	5

as shown in Table 4.3.

4.2.2 Dwell Time Calculation

To approximate the reference voltage vector using the nearest-three vectors, the dwell time for each space vector needs to be determined. According to the volts-second principle, the following equations can be obtained:

$$\begin{aligned} \overrightarrow{V_{ref}} &= \overrightarrow{V_x} \cdot \frac{T_1}{T_s} + \overrightarrow{V_y} \cdot \frac{T_2}{T_s} + \overrightarrow{V_z} \cdot \frac{T_3}{T_s} \\ &= \overrightarrow{V_x} \cdot d_1 + \overrightarrow{V_y} \cdot d_2 + \overrightarrow{V_z} \cdot d_3 \end{aligned} \tag{4.4}$$

$$\begin{cases} T_1 + T_2 + T_3 = T_s \\ d_1 + d_2 + d_3 = 1 \end{cases} \tag{4.5}$$

Table 4.4: Duty cycle expression in different subsector of Sector-I

Subsector	d_1	d_2	d_3
1	$2m\sin(\frac{\pi}{3}-\theta)$	$1-2m\sin(\frac{\pi}{3}+\theta)$	$2m\sin\theta$
2	$2[1-\sqrt{3}m\sin(\frac{\pi}{6}+\theta)]$	$3[2m\sin(\frac{\pi}{3}+\theta)-1]$	$2[1-\sqrt{3}m\cos\theta]$
3	$2[1-\sqrt{3}m\sin(\frac{\pi}{6}+\theta)]$	$3m\sin\theta$	$\sqrt{3}m\cos\theta-1$
4	$\sqrt{3}m\sin(\frac{\pi}{6}+\theta)-1$	$3[1-m\sin(\frac{\pi}{3}+\theta)]$	$\sqrt{3}m\cos\theta-1$
5	$\sqrt{3}m\sin(\frac{\pi}{6}+\theta)-1$	$3m\sin(\frac{\pi}{3}-\theta)$	$2(1-\sqrt{3}m\cos\theta)$

where $\overrightarrow{V_x}$, $\overrightarrow{V_y}$ and $\overrightarrow{V_z}$ denote the nearest-three virtual space vector (VSV). T_{1-3} and d_{1-3} indicate the dwell time and duty cycle of the above vectors, respectively. T_s refers to a switching period.

If the reference voltage vector is located in any position inside the hexagon, it can be composed of a series of VSVs. Then, all the duty cycles for the different vectors can be calculated by splitting reference voltage vector and the nearest-three VSV into real and imaginary frames, namely, the α and β-axis. Using equations (4.4) and (4.5), the specific duty cycle expressions of the original NTV^2 strategy can be calculated, as given in Table 4.4, in which d_1, d_2 and d_3 shown in Figure 4.2 represent the corresponding duty cycles of the nearest-three vector.

4.3 The Fast Calculation Reference Frame

To simplify sector identification and dwell time calculation in the α-β reference frame as shown in the last section, a fast reference frame, known as the 60° frame, is adopted. This can be obtained using a transformation matrix [134]:

$$\begin{bmatrix} V_g \\ V_h \end{bmatrix} = \begin{bmatrix} 1 & -1/\sqrt{3} \\ 0 & 2/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{4.6}$$

By projecting equation (4.4) into this frame, V_g and V_h can be defined as:

Table 4.5: The criteria for sector identification

Sector	Criteria
I	$V_g>0$ & $V_h \geq 0$
II	$V_g \leq 0$ & $V_g+V_h>0$
III	$V_h>0$ & $V_g+V_h \leq 0$
IV	$V_g<0$ & $V_h \leq 0$
V	$V_g \geq 0$ & $V_g+V_h<0$
VI	$V_h<0$ & $V_g+V_h \geq 0$

$$\begin{cases} V_g = X_g d_1 + Y_g d_2 + Z_g d_3 \\ V_h = X_h d_1 + Y_h d_2 + Z_h d_3 \end{cases} \tag{4.7}$$

where (V_g,V_h), (X_g,X_h), (Y_g,Y_h) and (Z_g,Z_h) are the coordinates of V_{ref} and the nearest-three VSVs in the g-h plane, respectively.

For the sake of simplicity, all VSVs and V_{ref} are normalized with respect to the magnitude of large vector $(2/3V_{dc})$. As a consequence, (V_g, V_h) can be expressed as (g, h) in the following analysis.

4.3.1 Sector and Subsector Identification

In accordance with the principle of the VSV synthesis, each sector is divided into five parts [100]. As the vertex of subsector is associated with the g-h coordinate, in order to use linear programming, all the boundary lines of the subsector and hexagon side should be built in the Cartesian coordinates [132]. By fixing all (g, h) in this orthogonal frame, a new hexagon diagram can then be established, as shown in Figure 4.3. It can be clearly seen that the coordinates of the three VSVs determine subsector numbers, including sector numbers.

Taking Sector-I shown in Figure 4.4 as an example, the outer boundary lines of the large triangle are used to obtain sector numbers while the four boundary lines can easily gain subsector numbers through linear programming. This process is easier to implement than Tables 4.2 and 4.3 which are used for the traditional α-β

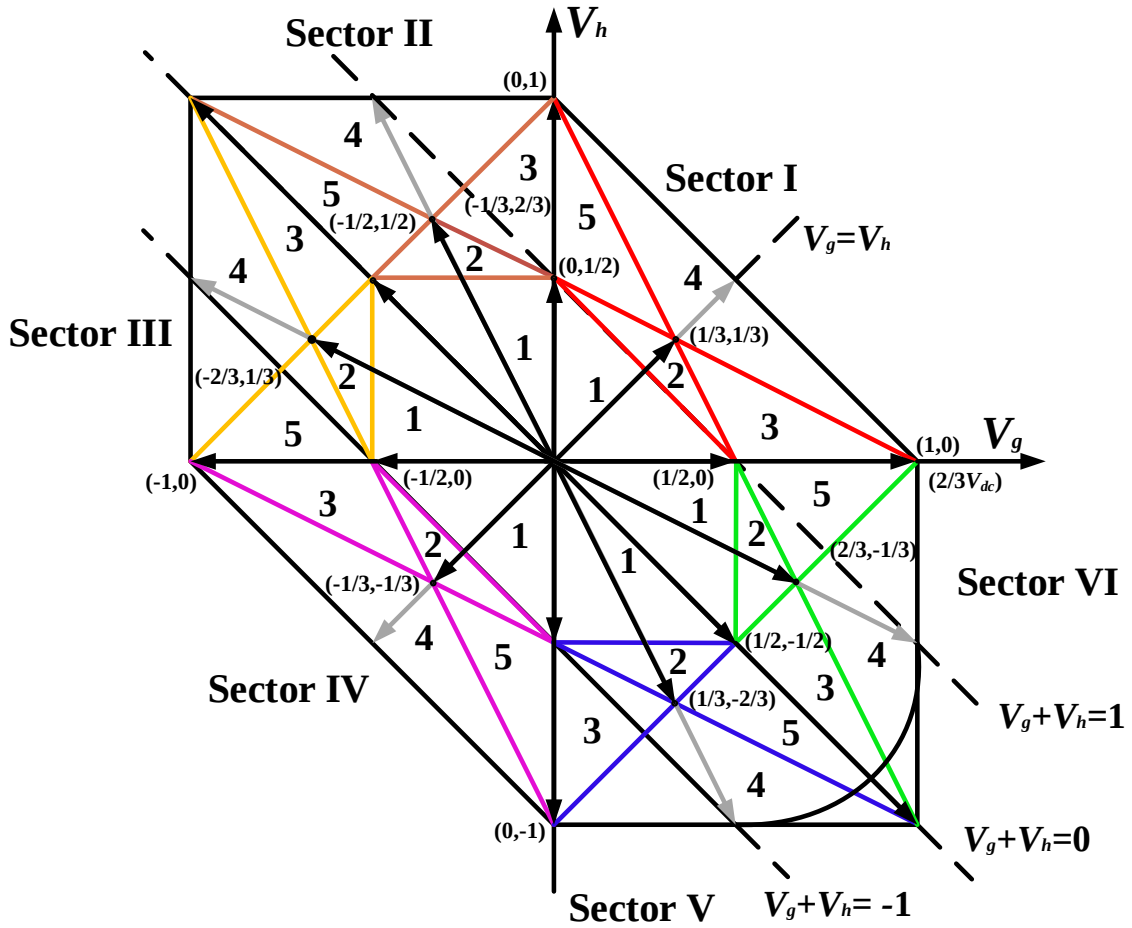


Figure 4.3: SVD of the NTV^2 scheme in g-h plane

reference frame. For the g-h reference frame, the sector/subsector determination criteria are given in Tables 4.5 and 4.6.

In order to deal with the identification of the subsectors in Sectors II-VI, the reference voltage vector can be converted into Sector-I due to the geometrical symmetry. The transformation relationship is given as follows:

$$\begin{bmatrix} V_{gN} \\ V_{hN} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 1 & 1 \end{bmatrix}^{(N-1)} \begin{bmatrix} V_{g1} \\ V_{h1} \end{bmatrix} \tag{4.8}$$

where V_{gN} and V_{hN} denote, if V_{ref} is located in Sectors II-VI, the voltage components of the reference voltage vector in the g-h plane. $N \in [2, 6]$ refers to sector number.

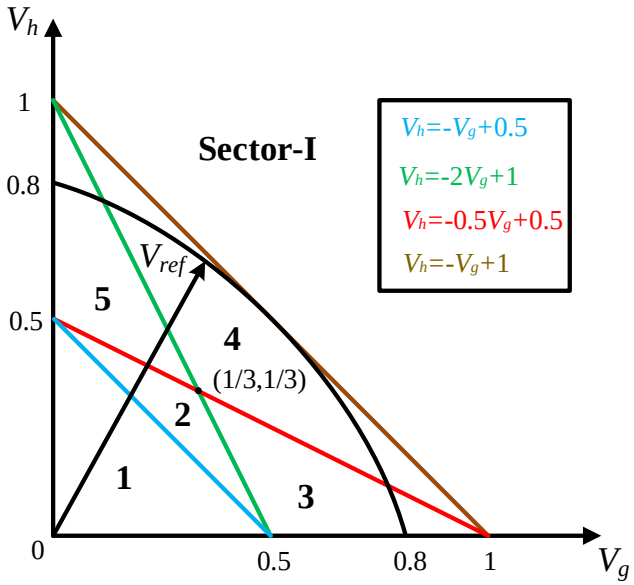


Figure 4.4: Subsector identification criteria in Sector-I

Table 4.6: The criteria of subsector judgment in Sector-I

Subsector	Criteria
1	$0 \leq V_{g1}+V_{h1} \leq 0.5$
2	$V_{g1} + V_{h1} \geq 0.5$, $V_{h1} + 2V_{g1} \leq 1$, $0.5V_{g1} + V_{h1} \leq 0.5$
3	$V_{h1} + 2V_{g1} \geq 1$, $0.5V_{g1} + V_{h1} \leq 0.5$, $V_{h1} \geq 0$
4	$V_{g1} + V_{h1} \leq 1$, $V_{h1} + 2V_{g1} \geq 1$, $0.5V_{g1} + V_{h1} \geq 0.5$
5	$V_{g1} \geq 0$, $0.5V_{g1} + V_{h1} \geq 0.5$, $V_{h1} + 2V_{g1} \leq 1$

Therefore, Table 4.6 provides the subsector identification criteria for the NTV^2 scheme. Comparing Tables 4.2-4.3 with Tables 4.5-4.6, it can be seen that simple linear programming and algebra functions tackle the complex issues caused by two introduced auxiliary angles pre-calculation and detection in the conventional α-β reference frame.

4.3.2 Dwell Time Calculation

Since the reference voltage vector has been converted into Sector-I, the repetitive dwell time determination processes in other sectors can be substituted using the same execution approach as in the first sextant.

Table 4.7: Duty cycle of VSVs in subsectors 1-5 of Sector-I

Subsector	d_1	d_2	d_3
1	$2g$	$2h$	$1-2(g+h)$
2	$2(1-g-2h)$	$2(1-h-2g)$	$3[2(g+h)-1]$
3	$2(1-2h-g)$	$2g+h-1$	$3h$
4	$2h+g-1$	$3(1-g-h)$	$2g+h-1$
5	$2(1-2g-h)$	$2h+g-1$	$3g$

For example, the nearest-three VSVs are V_{S1}, V_{S2} and V_{M1} in subsector-2, and the dwell times for each one are expressed by T_1, T_2 and T_3, respectively. According to equation (4.7), the following equation can be formed:

$$\begin{cases} gT_s = \dfrac{1}{2}T_1 + \dfrac{1}{3}T_3 \\ \\ hT_s = \dfrac{1}{2}T_2 + \dfrac{1}{3}T_3 \end{cases} \tag{4.9}$$

where (g, h) refers to the coordinates of V_{ref} in the g-h frame. (1/2, 0), (0, 1/2) and (1/3, 1/3) are the coordinates of the V_{S1}, V_{S2} and V_{M1}, respectively, as displayed in Figure 4.4.

The relationship between coordinate and duty cycle can be expressed as:

$$\begin{cases} g = \dfrac{1}{2}d_1 + \dfrac{1}{3}d_3 \\ \\ h = \dfrac{1}{2}d_2 + \dfrac{1}{3}d_3 \end{cases} \tag{4.10}$$

Substituting equation (4.10) into equation (4.5), the following equations can be formed:

$$\begin{cases} d_1 = 2[1 - g - 2h] \\ d_2 = 2[1 - h - 2g] \\ d_3 = 3[2(g + h) - 1] \end{cases} \tag{4.11}$$

Similarly, in the rest of subsectors, the duty cycle for each VSV can be formed, as listed in Table 4.7. Comparing Table 4.4 with Table 4.7, it can be seen that the

Table 4.8: Computational efficiency for the NTV^2 strategy

Performance / Method	C-code length	Execution time
α-β reference frame	240 lines	55.6μs
g-h reference frame	150 lines	41.2μs

duty cycle expressions are simplified by using the g-h reference frame approach.

4.4 Comparison of Computational Efficiency

The execution time by the traditional calculation method and the fast calculation solution for the NTV^2 strategy was tested using a TMS320C6713 DSP Starter Kit (DSK) with a 225MHz system clock. The result shows that the algorithm based on the g-h reference frame uses 41.2μs with about 150 lines in C-language code, whereas 55.6μs of computational time and about 240 lines in C-language code are required for the α-β reference frame implementation of the same strategy, which means nearly 35% computational burden reduction. Table 4.8 summarises this comparison.

4.5 Conclusions

In this Chapter, the sector/subsector identification methods based on the conventional α-β and the introduced g-h reference frames were compared.

One of the drawbacks of the NTV^2 scheme, compared with the conventional NTV scheme, is the complexity of subsector identification and and dwell time calculation. The existing judgment method based on the orthogonal plane applies two auxiliary angles to identify the number of subsectors and uses lots of trigonometric functions to determine duty cycles of required switching states, which is cumbersome in digital implementation and can cause an excessive computational burden. In order to solve this issue, a fast calculation approach is adopted to optimize the identification issue and dwell time calculation process in the digital controller system. It can be seen that the aforementioned disadvantages have been overcome, which is beneficial to

improve the algorithmic efficiency of the high-performance PWM schemes proposed in the following Chapters.

Chapter 5

Modified Virtual Space Vector Modulation Strategies for Three-Level NPC Converters

This Chapter presents two modified virtual-space-vector-based modulation schemes that aim to enhance the modulation performance in terms of active neutral-point voltage balancing control and common-mode voltage reduction, respectively.

5.1 Introduction

As discussed in Chapter 3, the NTV^2 scheme can achieve net-zero neutral-point (NP) current in every switching cycle, which guarantees the balanced capacitor voltages if initial NP voltage is in a balanced state. However, the original method cannot generate extra electric charges when NP potential initially drifts away, thereby failing to recover existing capacitor voltage error.

Three-phase PWM converter-fed motor drives have the following disadvantages caused by the CMV:

1) High-frequency leakage current flowing to ground through motor stray capacitor [135].

2) Winding insulation problem induced by bearing current due to motor shaft voltage [136].

3) Radiated EMI issues [137].

With respect to hardware-intensive approaches, a common-mode (CM) choke is generally used to reduce ground leakage current [138]. Motor bearing material erosion and early mechanical failure can be alleviated by adopting insulated bearing [135]. EMI can be suppressed using a CM filter [139]. However, bulky size and extra cost should be carefully considered, especially for aerospace applications.

Topologies and advanced modulation strategies are two solutions that can help lower CMV magnitude. A balanced inverter topology [140] has been proposed for cancelling CMV in variable-speed motor drives. From the PWM algorithm perspective, a CMV-reduced virtual-space-vector modulation method has been studied in [141], but can only be used in two-level inverter applications. As medium and zero vectors do not generate CMV, a reference voltage vector can be synthesized by these vectors for attaining zero CMV [142]. However, the restriction on modulation index makes it hard to be employed in some fields that require a higher DC-link voltage utilization. By using six virtual medium vectors, the shortcoming of this method has been fixed in [143]. Noteworthy, because of the influence of medium vector, NP voltage oscillation becomes severe. Thus, a large DC-link capacitance is required, which leads to the oversize problem. In [144], the authors present a modulation method for a three-level T-type inverter based on the MPC scheme to gain balanced NP voltage and lower CMV. A modified NTV^2-based modulation scheme applied in a variable-speed drive system is presented to keep capacitor voltage balanced and suppress CMV within one-third of DC-link voltage [145]. Since only [OOO] is chosen in the predefined switching sequence, CMVs generated by the other two zero switching states can be avoided. Nevertheless, it is notable that the method may cause two more switches turned on and off in one phase leg. In [146], a technique adopting four vectors with lower CMV is investigated. Besides, a modified sector repartition is employed. Noted that the adjustment of dwell time for small vector might be ineffective for weak NP voltage balance region. In [110], through defining

Table 5.1: Hardware-free common-mode voltage reduction methods

Exisiting methods	Technical details
Balanced inverter topology [140]	Three series-connected devices in each phase-leg
Virtual-space-vector based [141]	Aiming for two-level topology
Medium/zero vector based [142]	Lower DC-link voltage utilization
Virtual medium vector based [143]	Severe capacitor voltage fluctuation
Non [PPP]&[NNN] scheme [145]	Extra two turn-on/off switching actions
Four-vector based [146]	Sector repartition is required
Improved NTV^2 based [110]	Complicated switching sequence
MPC based [144]	CMV is considered in the cost fuction
Virtual small/medium vector based [107]	Low-complexity computation
CBPWM based [147]	Aiming for back-to-back topology
Carrier-based SVPWM [148]	Single-pulse CMV in every switching period

two pairs of virtual small vectors with lower CMV, an advanced NTV^2 strategy is proposed for eliminating NP voltage oscillation and mitigating CMV. However, this algorithm is complicated as the switching sequence varies in each subsector. In [107], a low-complexity virtual-space-vector modulation strategy is proposed to reduce the CMV as low as one-sixth of DC-link voltage for high-speed motor drive applications. Reference [147] and [148] develop advanced CBPWM schemes to mitigate CMV and balance NP voltage for a three-level back-to-back converter. It is noticeable that, through arranging switching sequences, the CMV can be limited as a single pulse over a switching period [148]. Table 5.1 summarises the existing CMV reduction approaches from the topology and modulation perspectives.

In the first part of this Chapter, a high-performance active modulation technique for the original NTV^2 strategy is presented. This modulation scheme keeps the capacitor voltage balanced in a 3L-NPC converter. The fast calculation approach discussed in Chapter 4 is supplemented to ease computational burden of the

proposed modulation process. In the rest of this Chapter, a new modulation strategy based on the virtual-space-vector concept is explored to balance the capacitor voltages and provide CMV reduction, simultaneously.

5.2 Proposed Capacitor Voltage Balancing Control Method

5.2.1 Tendency of NP Voltage Deviation in Drive Systems

As shown in Chapter 3, the NTV^2 scheme can only provide zero NP potential electric charge to realize balanced capacitor voltages over a switching cycle. For that reason, the conventional technique cannot acquire active NP voltage balancing capability by itself. If the capacitor voltage drifts, such as due to initial unbalanced DC-link voltages, the scheme cannot balance the NP voltage.

In this study, a 3L-NPC converter is connected to an aircraft electric generator. Therefore, the tendency of NP potential divergence is related to both motoring or generating modes [70]. More specifically, during the startup process of the S/G systems, the NP potential raises with more participation of the P-type small vector. On the contrary, NP potential drops down with more utilization of the P-type small vector in power generating condition and vice versa.

Here, [PPO] and [OON] are taken as examples. In the motoring mode, the phase current path is denoted as a red dashed arrow, while the green arrow represents generation mode, as shown in Figure 5.1. It can be seen from Figure 5.1(a) that the upper-side capacitor is discharged during the startup process, which implies that NP potential rises, whereas the capacitor is charged in power generating conditions and NP potential drops down. For the case in Figure 5.1(b), the lower-side capacitor is discharged during the motoring mode, which indicates that NP potential decreases, whereas the capacitor is charged in generation mode and NP potential goes up. Table 5.2 summarises the correlation between NP drift tendency and the ESG system operational mode.

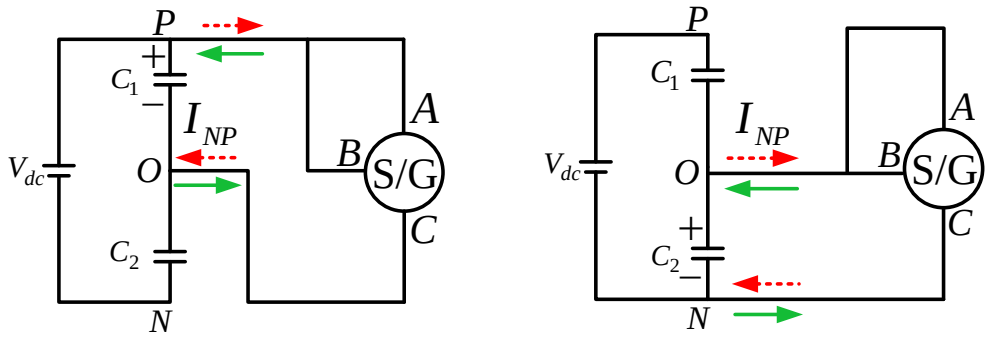


Figure 5.1: NP voltage drift with (a) [PPO] and (b) [OON]

Table 5.2: NP drift tendency with respect to the ESG operational mode

ESG Mode / Small Vector Type	Motoring Mode	Generating Mode
P-type	↑	↓
N-type	↓	↑

5.2.2 Implementation Process

As known from the equation (3.10), the small vectors for the NTV^2 scheme are equally allocated in each subsector. According to the operational mode of the developed ESG system, active NP voltage balancing control can be realized by distributing dwell time of small vectors with a bias-offset. The capacitor voltage deviation factor k is defined by:

$$k = 1 - \frac{V_{dc2}}{V_{dc1} + V_{dc2}} \in [0, 1] \tag{5.1}$$

where V_{dc1} and V_{dc2} represent upper and lower-side capacitor voltages, respectively.

If the two capacitor voltages are balanced, k=0.5. If V_{dc1}>V_{dc2}, k∈(0.5, 1] and if V_{dc1}<V_{dc2}, k∈[0, 0.5). For simplicity, the first sector established in the g-h plane is taken as a representative example to explain the proposed modulation strategy.

- For subsector-1

  In this subsector, two pairs of small vectors ([ONN] & [POO] and [OON] & [PPO]) are involved within each switching period. If V_{dc1}>V_{dc2} in motoring mode, the switching interval of [ONN] and [OON] should be reduced, whereas

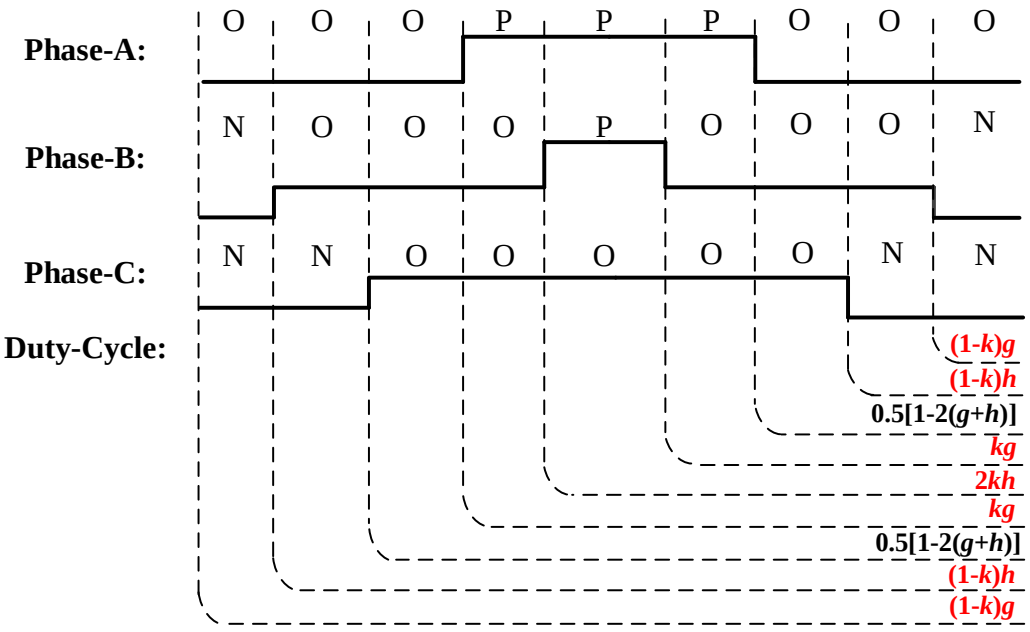


Figure 5.2: Active switching pattern for subsector-1

duty cycles of their counterparts need to be increased. Hence, the allocation ratio for the duty cycle of N-type and P-type small vector can be assigned as 1-k and k, respectively. The modified switching pattern is shown in Figure 5.2.

If V_{dc1}>V_{dc2} in the power generation mode, the switching interval of [ONN] and [OON] should be raised, whereas duty cycle of their counterparts should be reversely regulated. As a result, the allocation ratio for the duty cycle of N-type and P-type small vector are k and 1-k, respectively.

- For subsector-2

  In this subsector, small vectors are the same as those applied in subsector-1. Therefore, the manipulation of duty cycle follows the same manner. That is, if V_{dc1}>V_{dc2} in motoring mode, the duty cycle allocation ratio of N-type and P-type small vector is 1-k and k, respectively, whereas the allocation ratio determined by equation (5.1) will be swapped in generation mode. By doing so, the active switching pattern of subsector-2 is given in Figure 5.3.

- Subsector-3

  In this subsector, one pair of redundant small vectors ([POO] & [ONN]) is

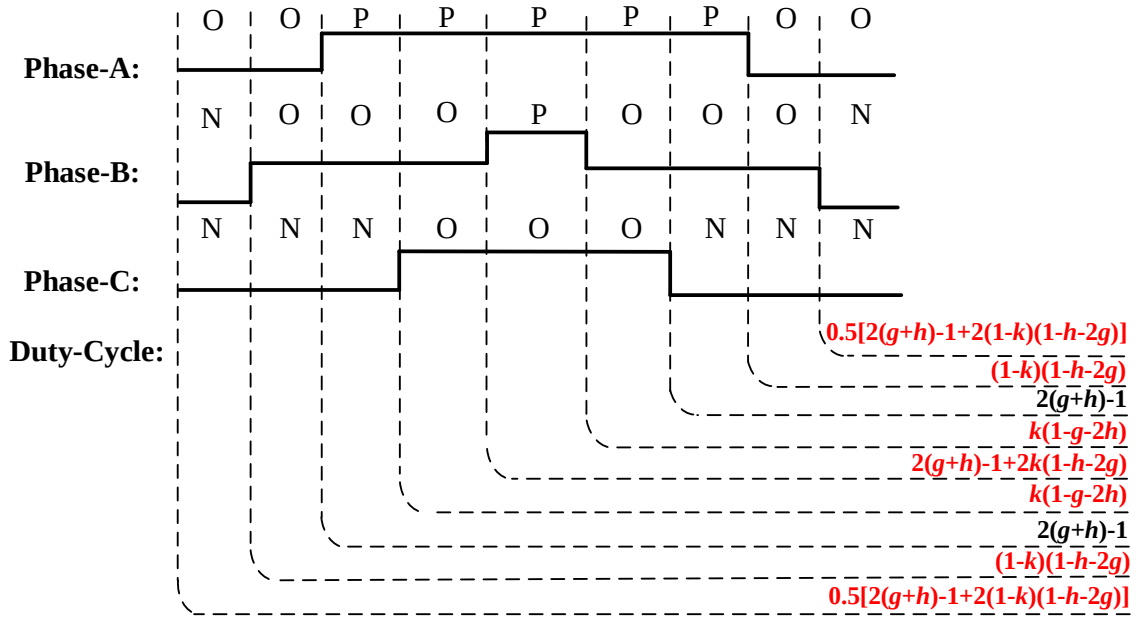


Figure 5.3: Active switching pattern for subsector-2

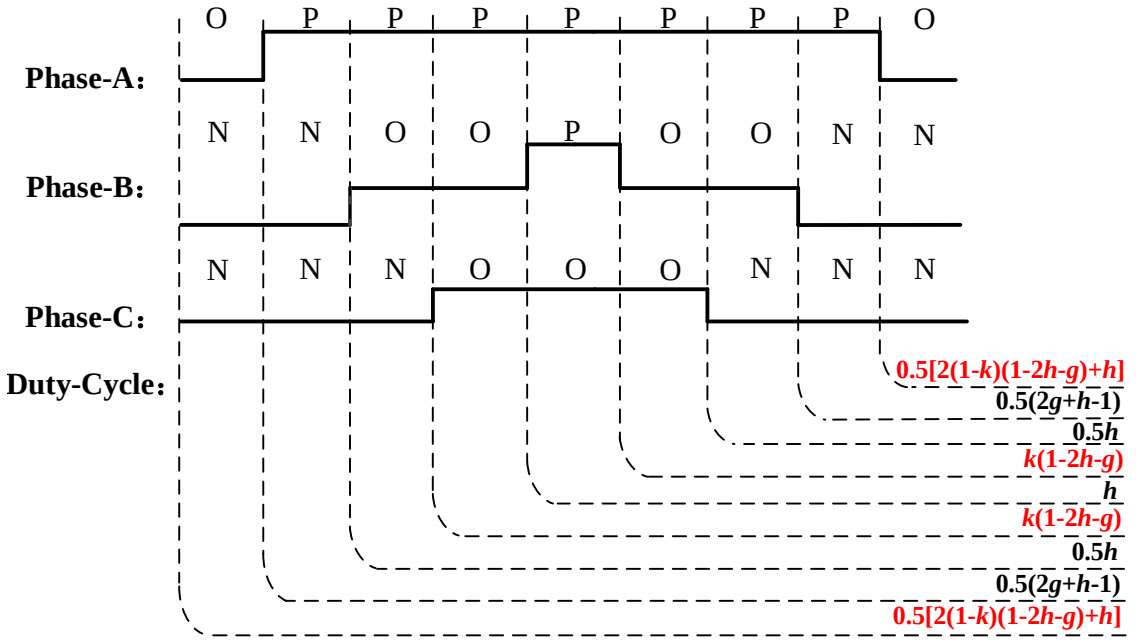


Figure 5.4: Active switching pattern for subsector-3

included in each switching period. If $V_{dc1}>V_{dc2}$ in motoring mode, the switching interval of [ONN] should be decreased, whereas the duty cycle of the counterpart should be increased. Thus, the duty cycle allocation ratio for N-type and P-type small vector is 1-k and k, respectively.

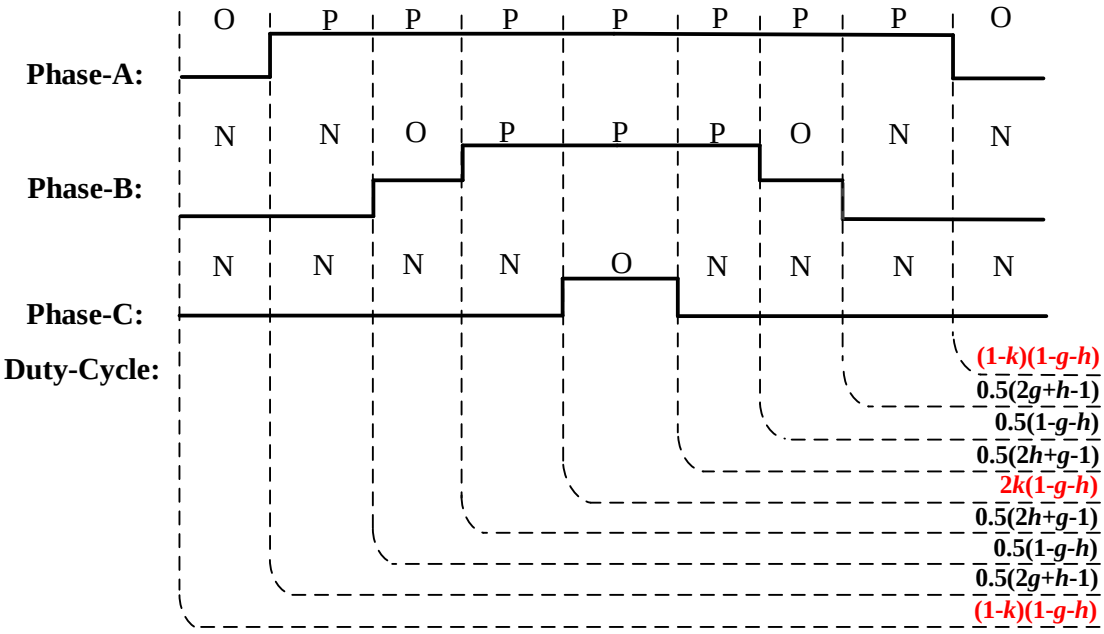


Figure 5.5: Active switching pattern for subsector-4

If $V_{dc1}>V_{dc2}$ in generation mode, the switching interval of [ONN] requires a larger amount, whereas that amount of [POO] should be reduced. The dedicated active switching pattern is shown in Figure 5.4.

- For subsector-4

  In this subsector, two small vectors ([PPO] & [ONN]) are involved in each switching period. If $V_{dc1}>V_{dc2}$ in motoring mode, the switching interval of [ONN] should be decreased, whereas that of [PPO] needs an increased amount. Therefore, the allocation ratio for duty cycle of N-type and P-type small vector is 1-k and k, respectively.

  If the $V_{dc1}>V_{dc2}$ during the generating mode, the duty cycle of [ONN] should be increased, whereas its counterpart needs to be regulated in an opposite way. Figure 5.5 shows the modified switching pattern for subsector-4.

- For subsector-5

  In this subsector, one pair of redundant small vectors ([PPO] & [OON]) is involved in each switching period. If $V_{dc1}>V_{dc2}$ in motoring mode, the switching

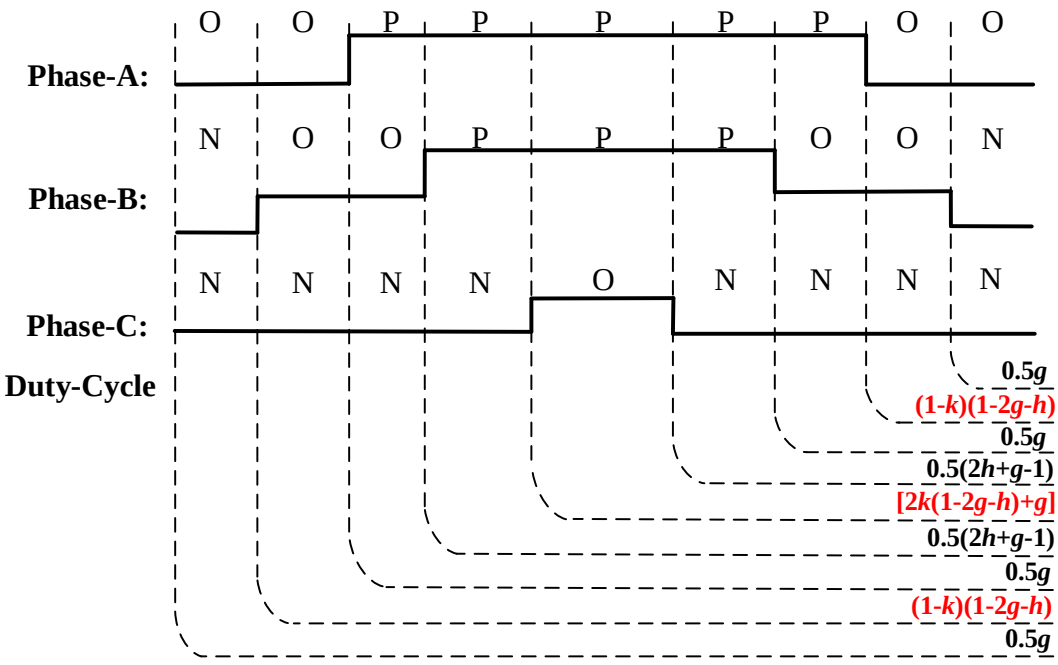


Figure 5.6: Active switching pattern for subsector-5

interval of [OON] should be decreased, whereas the duty cycle of [PPO] needs to be raised. As a result, the duty cycle allocation ratio for N-type and P-type small vector is 1-k and k, respectively.

If V_{dc1}>V_{dc2} in generation mode, the switching interval of [OON] should be regulated to a larger value, whereas the duty cycle of [PPO] should be decreased. Figure 5.6 details the modified switching pattern for subsector-5.

Using Table 5.2, a similar analysis and modified dwell times can be formed for the other sectors.

5.2.3 NP Voltage Balancing Performance

The DC-link capacitor voltage bias is associated with the extra NP electric charge accumulated in every PWM period. In order to balance diverged capacitor voltages, the required NP potential compensation amount within a sampling time can be calculated by equation (3.3):

$$C \cdot \Delta V_{dc} + \Delta Q = 0 \tag{5.2}$$

where ΔQ is defined as the compensated charge.

For example, in subsector-4, the compensated charge with the conventional NTV^2 scheme and the proposed solution can be derived:

- For the NTV^2 scheme

$$\Delta Q_{\mathrm{I}} = (1 - g - h) \cdot (i_a + i_b + i_c) \cdot T_s = 0 \tag{5.3}$$

- For the proposed method:

$$\begin{aligned} \Delta Q_{\mathrm{II}} &= (T_1 + T_{BO}) \cdot i_a + T_3 \cdot i_b + (T_2 - T_{BO}) \cdot i_c \\ &= (1 - 2k) \cdot (1 - g - h) \cdot (i_a - i_c) \cdot T_s \end{aligned} \tag{5.4}$$

where T_1, T_2 and T_3 are the dwell time that phase-A, B and C clamp to the midpoint of capacitor bank. T_{BO} refers to the injected bias-offset in a switching period. The coefficient k indicates capacitor voltages deviation range, as given by equation (5.1).

Comparing equation (5.3) with equation (5.4), it is known that, unlike the conventional NTV^2 scheme, the proposed active capacitor voltage balancing approach is capable of providing extra electric charge to recover NP potential balance. In order to evaluate the active balancing control capability ($A_{c.c}$), the compensation charge by equation (5.4) can be derived:

$$\begin{aligned} A_{c.c} = (1 - 2k) T_s [1 - m \sin\left(\frac{\pi}{3} - \theta\right) - m \sin(\theta)] \\ \cdot I_{rms} [\cos(\theta - \varphi) - \cos\left(\theta + \frac{2\pi}{3} - \varphi\right)] \end{aligned} \tag{5.5}$$

where I_{rms} is the RMS value of the phase current. θ, m and φ denote angular position of V_{ref}, modulation index and power factor angle, respectively.

Similarly, the extra electric charge can be derived for other subsectors. Subsequently, the average active NP voltage control capability can be calculated for a fundamental cycle:

$$\frac{\overline{A_{c.c}}}{I_{rms} T_s} = \frac{1}{2\pi} \int_0^{2\pi} \frac{A_{c.c}(\theta)}{I_{rms} T_s} \cdot d\theta \tag{5.6}$$

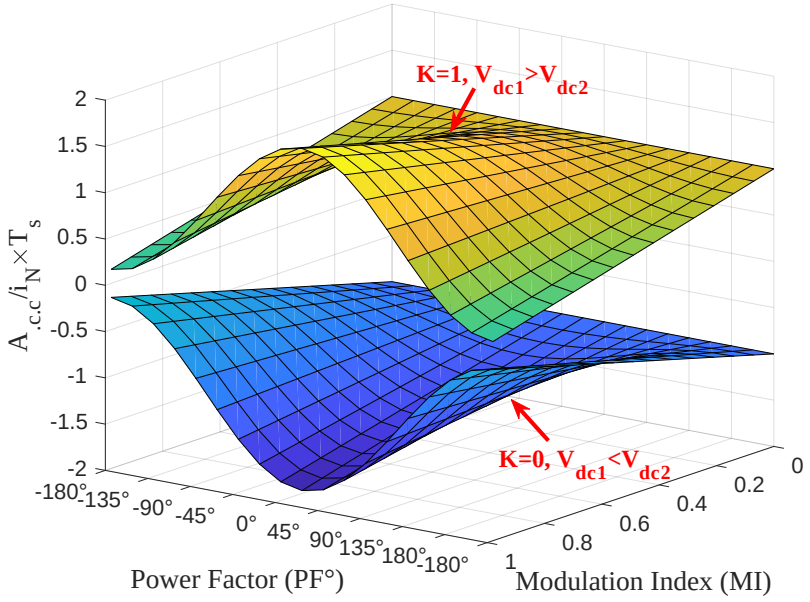


Figure 5.7: NP voltage balancing control capability of the proposed method

For the worst case condition, V_{dc1} or V_{dc2} is equal to the DC-link voltage, which corresponds to $k = 0$ or 1. Through the calculation by the above equations, the results from Figure 5.7 show that the voltage across each capacitor can be actively balanced for the high modulation index and low power factor operating conditions.

5.2.4 Power Loss Analysis

The power losses are performed using a Infineon F3L400R07ME4B22/B23 IGBT module that has the maximum collector-emitter voltage of 650V and continuous collector current of 400A, which is capable of withstanding the required phase current as well as surge voltage for our application. Based on the curves from the manufacturer's datasheet, the energy dissipated can be calculated using the turn-on (E_{on}) and turn-off (E_{off}) energy of the switching devices as a function of the current and voltage. Through the loss equations, the switching losses and conduction losses of the IGBTs and diodes can be estimated for different modulation strategies.

The power losses have been calculated for the ESG system operating in standby mode and for power generation mode with an active power of 25kW at 20krpm.

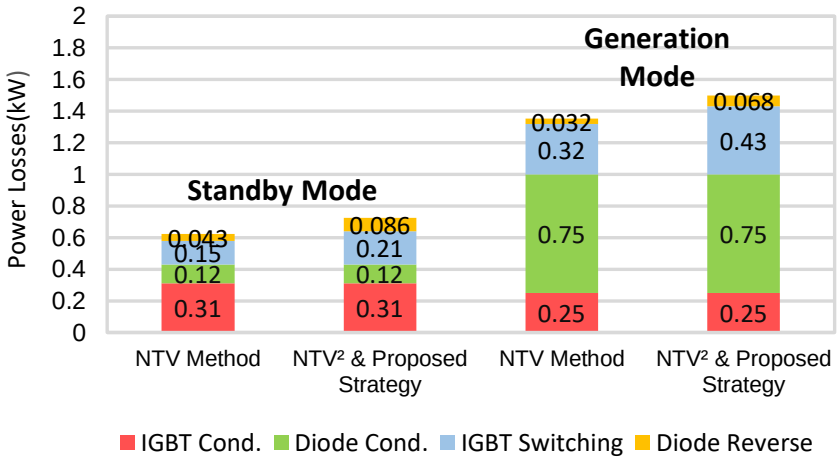


Figure 5.8: Power losses distribution with different modulation strategies for two operating modes

The switching frequency is set at 16kHz. Figure 5.8 shows the total loss breakdown regarding the NTV, NTV^2 and the proposed strategy. It can be seen that the conduction loss produced by these approaches are the same for each case, while the switching losses by the proposed modulation technique are higher than for the NTV method, but the same as for the NTV^2 scheme. This is because both the original NTV^2 scheme and the modified technique allow one of the phase output terminals connecting to the NP and positive/negative rail of the DC-link, thereby increasing the commutation intervals over a switching period. Nevertheless, this comes as a trade-off for actively balancing capacitor voltage and eliminating NP potential oscillations.

5.2.5 Comparison with Other NP Voltage Balance Control-Based Modulation Schemes

Compared with the other NP voltage balance control schemes for motor drives presented in [103] and [105]. The proposed active modulation algorithm brings the following attractive features:

1) The proposed modulation strategy uses NTVs to synthesize the reference voltage vector. As a result, the output distortion by the proposed algorithm is less than that by the method in the work of [105]. In contrast, in order to eliminate the NP

voltage fluctuation caused by medium vectors, the scheme presented in [105] utilizes non-nearest three vectors to configure the dedicated pulse trains.

2) The fast calculation approach adopted in the proposed modulation strategy overcomes the excessive computational burden. Compared with the works in [103], the subsector identification criteria of presented method is simple. Additionally, the technique uses algebraic functions instead of sinusoidal ones, which can save computation resources for the digital controller.

3) The proposed modulation strategy only leads to two switches transition from one switching state to the next in the same phase leg. Nevertheless, the results in [103] and [105] show that the NP voltage balancing control is realized at the expense of directive commutation path through positive to negative DC-rail, particularly for the operating conditions in the high modulation index region. However, similar to [103], the presented solution trades the reduced NP voltage fluctuation against the extra switching losses as compared to [105] because of three-level voltage instants during a switching cycle.

5.3 Proposed Common-Mode Voltage Reduction Method

5.3.1 Common-Mode Voltage Analysis

The voltage stress of the motor would be substantially increased when the CMV is imposed on machine terminals, and also its steep changes can induce damaging ground leakage, bearing currents and emission of common-mode noise, which put the target system's efficiency and reliability at risk.

The CMV is the voltage between the midpoint of load/stator winding and the NP, which is represented as V_{NO} in equation (2.16). Therefore, the value can be calculated as:

$$V_{com} = \frac{1}{3}(V_{ao} + V_{bo} + V_{co}) \tag{5.7}$$

Table 5.3: Common-mode voltage analysis of switching states and space vectors

Space Vectors	Switching States	$\|V_{com}\|$
Zero Vector	[OOO]	0
	[PPP] [NNN]	$V_{dc}/2$
Small Vector	[POO] [OON] [OPO] [NOO] [OOP] [ONO]	$V_{dc}/6$
	[ONN] [PPO] [NON] [OPP] [NNO] [POP]	$V_{dc}/3$
Medium Vector	[PON] [OPN] [NPO] [NOP] [ONP] [PNO]	0
Large Vector	[PNN] [PPN] [NPN] [NPP] [NNP] [PNN]	$V_{dc}/6$

where V_{ao}, V_{bo} and V_{co} are the phase voltage with respect to the NP potential.

Using the calculation shown in equation (5.7), the CMVs of all switching states can be listed, as shown in Table 5.3. It is known that CMV contains a series of DC voltage that contributes to the bearing current in motor drives [70]. In this regard, the magnitude of CMV generated by the conventional NTV^2 scheme is one-third of DC-link voltage as all the small vectors are fully utilized during a fundamental period.

5.3.2 Synthesis Principle of CMV-Reduced Virtual Space Vector

In order to maintain balanced capacitor voltages and reduced CMV at the same time, the principle of switching state selection needs to satisfy the following requirements so that the modified virtual space vectors achieve superiorities over the traditional counterpart.

(i) The sum of NP currents associated with synthesized virtual space vectors should average to net-zero.

(ii) The CMVs produced by the basic space vectors should be minimized.

From Table 3.1 and Table 5.3, it can be seen that one straightforward method is that two pairs of large vectors could be used to compose two virtual small vectors

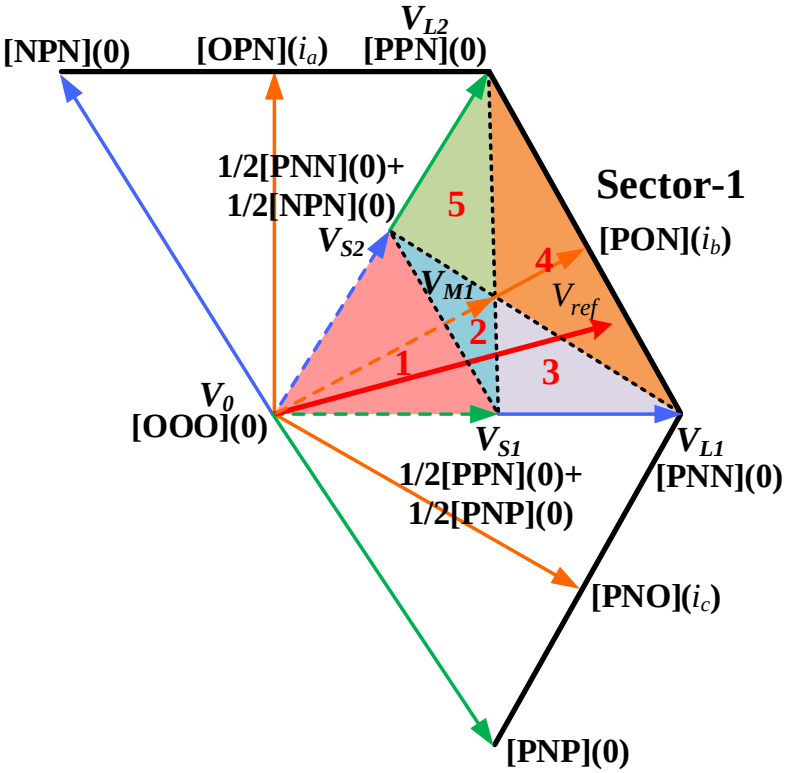


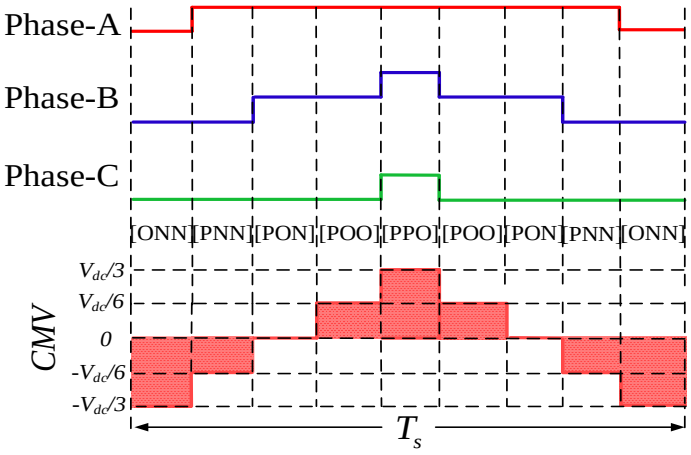
Figure 5.9: SVD of the proposed modulation strategy for Sector-I

and the adjacent three medium vectors synthesize one virtual medium vector. The selection of the zero and large vectors still follows the same rule as the conventional NTV^2 scheme. This method forms the basis of the proposed CMV-reduced virtual space vector modulation approach.

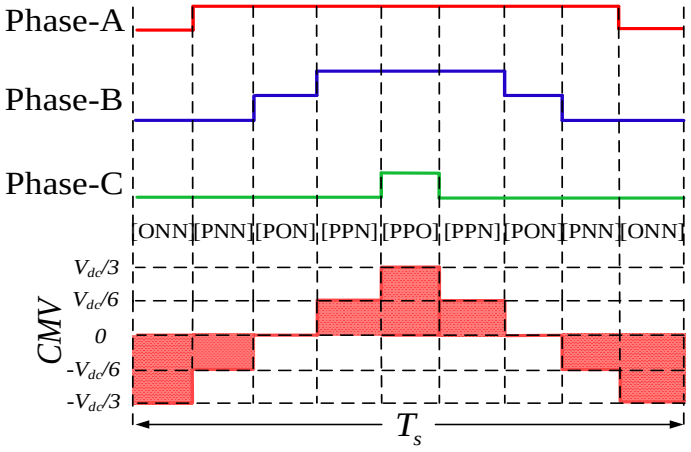
The blue, orange, and green dashed arrow lines shown in Figure 5.9 indicate these modified virtual space vectors defined by:

$$\begin{cases} V_{S1} = (V_{[\mathrm{PPN}]}[0] + V_{[\mathrm{PNP}]}[0])/2 \\ V_{S2} = (V_{[\mathrm{PNN}]}[0] + V_{[\mathrm{NPN}]}[0])/2 \\ V_{M1} = (V_{[\mathrm{OPN}]}[i_a] + V_{[\mathrm{PON}]}[i_b] + V_{[\mathrm{PNO}]}[i_c])/3 \\ V_0 = V_{[\mathrm{OOO}]}[0] \\ V_{L1} = V_{[\mathrm{PNN}]}[0] \\ V_{L2} = V_{[\mathrm{PPN}]}[0] \end{cases} \tag{5.8}$$

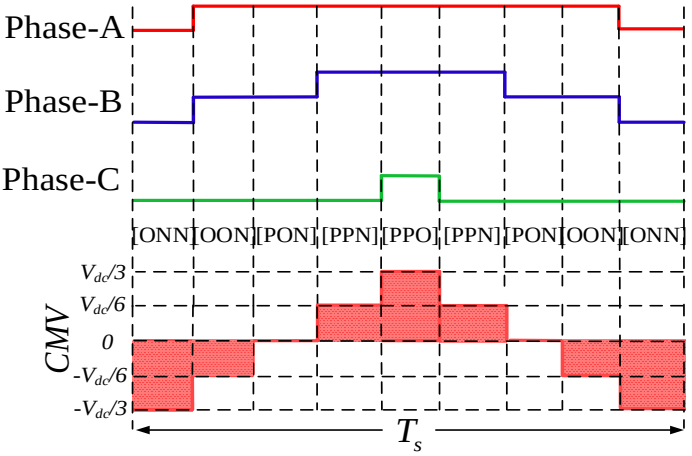
Since generation mode is the steady-state of the ESG system, V_{ref} is mainly



(a)



(b)



(c)

Figure 5.10: Switching sequence and CMVs of the conventional NTV^2 scheme in (a) subsector-3 (b) subsector-4 (c) subsector-5

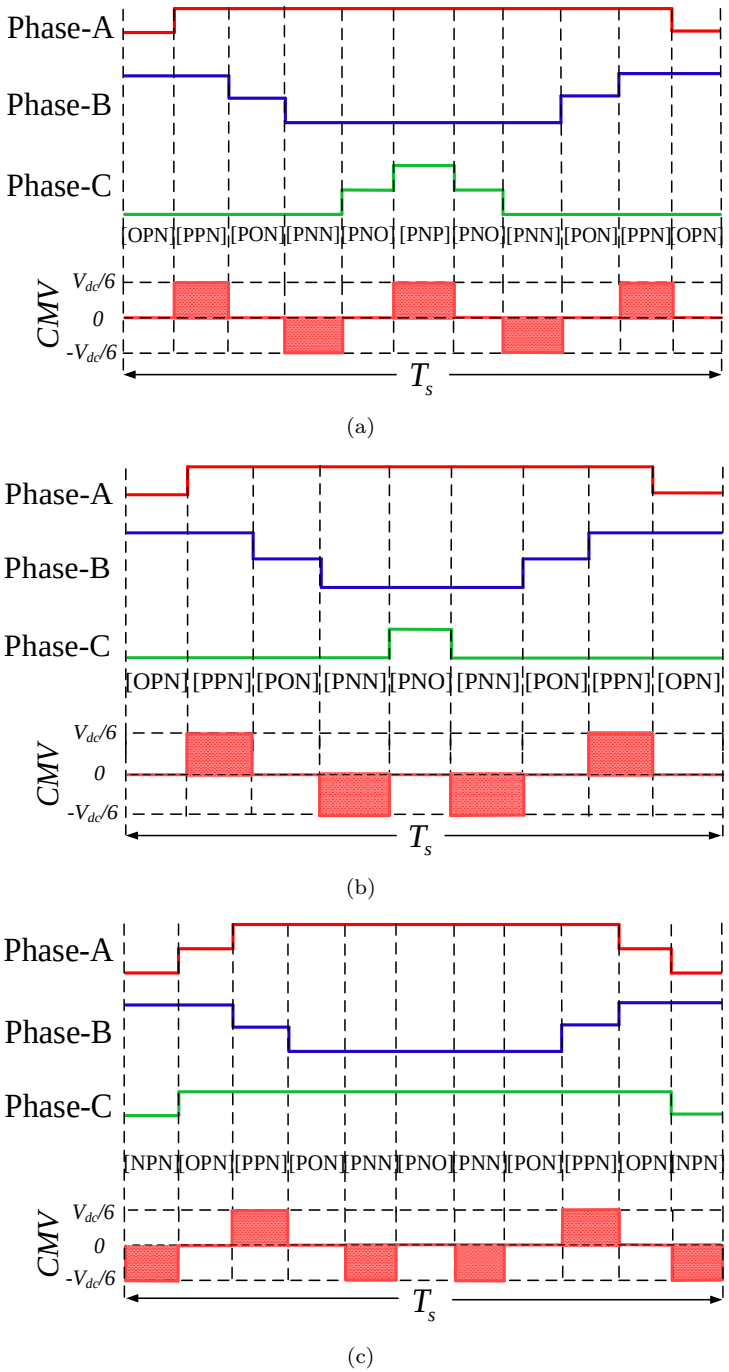


Figure 5.11: Switching sequence and CMVs of the proposed modulation scheme in (a) subsector-3 (b) subsector-4 (c) subsector-5

approximated by modified virtual space vectors distributed in subsectors 3-5 of each sector. For example, if V_{ref} is located in subsector-4 of the first sector, V_{L1}, V_{L2} and V_{M1} are selected. The switching sequence in a switching period can be assigned as

[OPN]→[PPN]→[PON]→[PNN]→[PNO]→[PNN]→[PON]→[PPN]→[OPN].

The CMV generated by the traditional NTV^2 scheme and the proposed modulation strategy are shown in Figures 5.10 and 5.11, respectively. As can be seen, compared with the NTV^2 scheme, the CMV is reduced to 50% using the proposed PWM technique, i.e., to one-sixth of DC-link voltage. Additionally, with the help of the virtual-space-vector concept, the presented strategy brings an opportunity to tackle the capacitor voltage imbalance issue irrespective of the modulation index and load angle.

5.3.3 Torque Ripple Analysis and Comparison

In order to analyse the torque ripple produced by the proposed CMV-reduced VSVs, the conventional NTV^2 scheme is selected as the benchmark method.

Because of the high torque-to-current ratio, high power density and high robustness, the PMSM is preferred for converter-fed high-speed motor drive systems. For our case, a 6-poles 36-slots machine is chosen as the candidate since it has the lowest eddy-current losses. The electromagnetic torque of the applied surface-mounted PMSM can be expressed as follows:

$$T_{em} = \frac{3}{2} n_p \psi_f i_q \tag{5.9}$$

where n_p is the pole pair numbers and ψ_f is the magnet flux.

Since n_p and ψ_f are constant values for a given PMSM, the torque ripple is proportional to q-axis current ripple. As seen from Figure 5.12, the direction of V_{ref} and its clockwise perpendicular line are defined as q- and d-axis, respectively. α is the angle between V_{ref} and V_{L1}. Apart from zero vectors, other virtual space vectors can be expressed based on this predefined reference frame. It is notable that all space vectors are normalized with the magnitude of V_{L1}. Thus, the following expressions can be attained as:

$$V_{S1} = \frac{1}{2}\sin\alpha + \frac{1}{2}\cos\alpha j \tag{5.10}$$

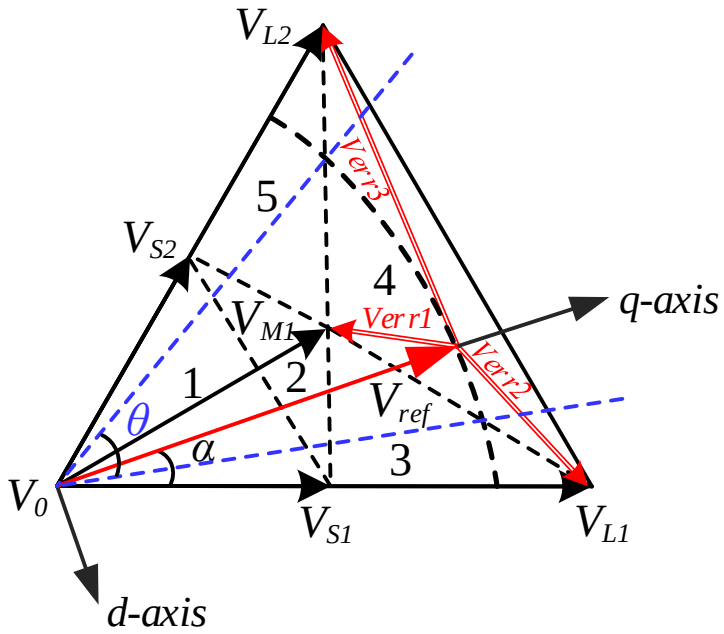


Figure 5.12: The voltage error vectors associated with virtual space vectors

$$V_{L1} = \sin\alpha + \cos\alpha j \tag{5.11}$$

$$V_{S2} = -\frac{1}{2}\sin\Big(60^0 - \alpha\Big) + \frac{1}{2}\cos\Big(60^0 - \alpha\Big)j \tag{5.12}$$

$$V_{L2} = -\sin\Big(60^0 - \alpha\Big) + \cos\Big(60^0 - \alpha\Big)j \tag{5.13}$$

$$\begin{cases} V_{M1} = \dfrac{-\sin(30^0 - \alpha)}{\sqrt{3}} + \dfrac{\cos(30^0 - \alpha)j}{\sqrt{3}} & \alpha \in (0, 30^0] \\ V_{M1} = \dfrac{\sin(\alpha - 30^0)}{\sqrt{3}} + \dfrac{\cos(\alpha - 30^0)j}{\sqrt{3}} & \alpha \in (30^0, 60^0] \end{cases} \tag{5.14}$$

Without loss of generality, subsector-4 is considered as a representative example to analyse the torque ripple in the following text. Hence, α can be confined by:

$$\arcsin(\frac{1}{m\sqrt{3}}) - 30^0 < \theta < 90^0 - \arcsin(\frac{1}{m\sqrt{3}}) \quad m \in [0.67,\ 1] \tag{5.15}$$

The time integral of error space vectors between V_{ref} and three virtual space vectors, as shown in Figure 5.12, refers to stator flux ripple vectors, which is a measurement of ripple in the line current [149]. Then, equations (5.14) and (5.15) are further derived as follows:

$$\begin{cases} \psi_{err1} = -\dfrac{t_1 \sin(30^0 - \alpha)}{\sqrt{3}} + t_1[\dfrac{1}{\sqrt{3}} \cos\Big(30^0 - \alpha\Big) - V_{ref}]j \\ \alpha \in (\arcsin[\dfrac{1}{m\sqrt{3}}] - 30^0, 30^0] \\ \psi_{err1} = \dfrac{t_1 \sin(\alpha - 30^0)}{\sqrt{3}} + t_1[\dfrac{1}{\sqrt{3}} \cos\Big(\alpha - 30^0\Big) - V_{ref}]j \\ \alpha \in (30^0, 90^0 - \arcsin[\dfrac{1}{m\sqrt{3}}]) \end{cases} \tag{5.16}$$

$$\begin{cases} \psi_{err2} = t_2 \sin\alpha + t_2(\cos\alpha - V_{ref})j \\ \psi_{err3} = -t_3 \sin(60^0 - \alpha) + t_3[\cos(60^0 - \alpha) - V_{ref}]j \end{cases} \tag{5.17}$$

where t_{1-3} represent the dwell time of nearest-three virtual space vectors.

For the proposed strategy, flux ripple vectors produced by large vectors are the same as the conventional NTV^2 scheme. Nevertheless, the error vectors generated by medium virtual space vectors are distinct for both schemes. The flux ripple vector produced by [PPO], [ONN] and [PON] can be yielded as:

$$\begin{cases} \psi_{ppo}^{err} = -\dfrac{1}{2} t_1 \sin\Big(60^0 - \alpha\Big) + t_1[\dfrac{1}{2} \cos\Big(60^0 - \alpha\Big) - V_{ref}]j \\ \psi_{onn}^{err} = \dfrac{1}{2} t_1 \sin\alpha + t_1(\dfrac{1}{2} \cos\alpha - V_{ref})j \end{cases} \tag{5.18}$$

$$\begin{cases} \psi_{pon}^{err} = -\dfrac{t_1 \sin(30^0 - \alpha)}{\sqrt{3}} + t_1[\dfrac{1}{\sqrt{3}} \cos\Big(30^0 - \alpha\Big) - V_{ref}]j \\ \alpha \in (\arcsin[\dfrac{1}{m\sqrt{3}}] - 30^0, 30^0] \\ \psi_{pon}^{err} = \dfrac{t_1 \sin(\alpha - 30^0)}{\sqrt{3}} + t_1[\dfrac{1}{\sqrt{3}} \cos\Big(\alpha - 30^0\Big) - V_{ref}]j \\ \alpha \in (30^0, 90^0 - \arcsin[\dfrac{1}{m\sqrt{3}}]) \end{cases} \tag{5.19}$$

Comparing equations (5.18) and (5.19) with equation (5.16), the flexible rotation coefficient R can be defined as equation (5.20), which can be directly used to evaluate the current ripple generated by all virtual space vectors.

$$R = A \times e^{\pm j\zeta} = \left| \frac{V_{basic}}{V_{virtual}} \right| \times e^{\pm j\zeta} \tag{5.20}$$

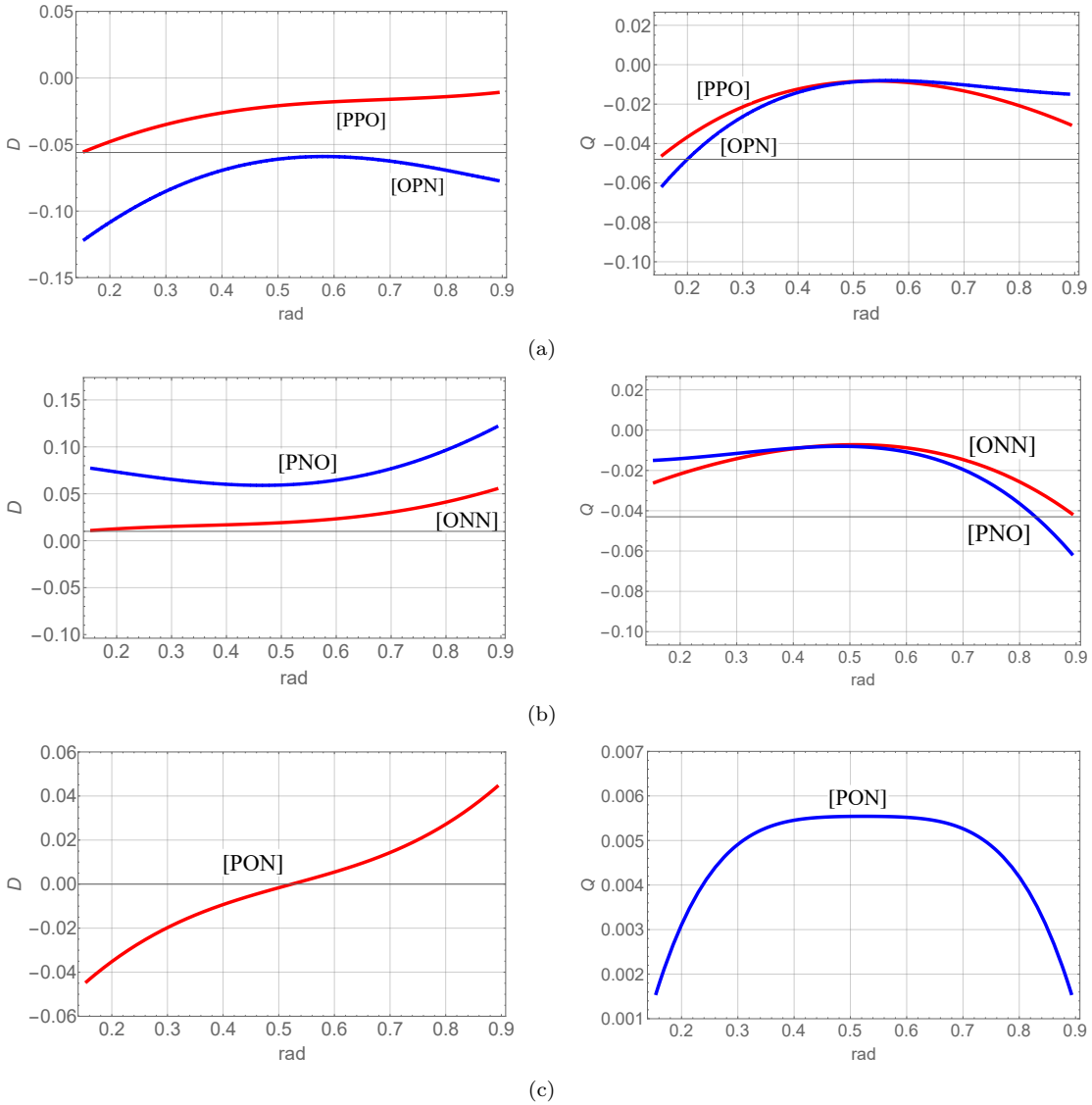


Figure 5.13: D−Q components of stator flux ripple vector caused by different switching states of the benchmark method and proposed scheme in subsector-4 (a) [PPO] and [OPN] (b) [ONN] and [PNO] (c) [PON]

where A and ζ represent length ratio and angle between basic and virtual space vector, respectively. Noted that the counter-clockwise direction corresponds to a positive sign in equation (5.20).

The flux error can be defined by:

$$\psi_{err} = D + Q \cdot j \tag{5.21}$$

Consequently, the current ripple caused by the modulation scheme can be evaluated by D and Q [150]. The amplitude of D−Q component of stator flux ripple

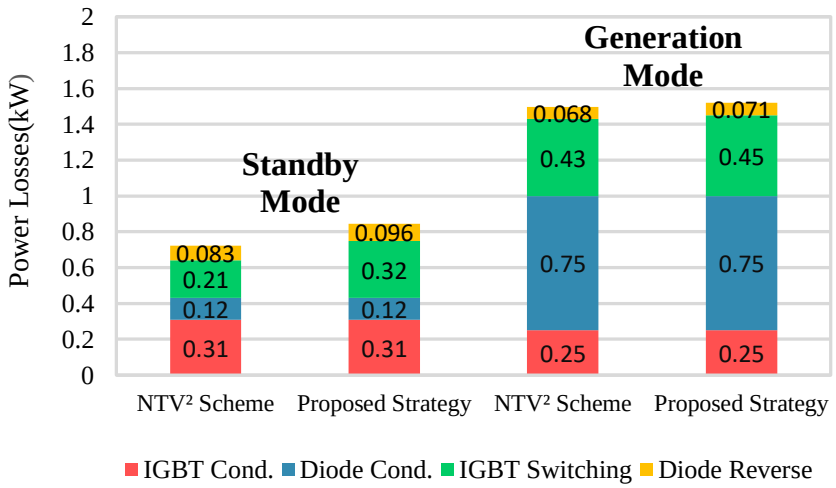


Figure 5.14: Comparison of power losses distribution between the benchmark method and the proposed CMV-reduced VSV-based modulation scheme under two operating conditions

vector is shown in Figure 5.13. It can be observed that the value of the proposed solution is a bit larger, which leads to a higher q-axis current ripple. The similar derivation and analyse can be carried out for other subsectors. Overall, the torque ripple produced by the modified scheme is inevitably increased. It is hence a trade-off to balance NP voltage and reduce CMV for high-speed drives, simultaneously.

5.3.4 Power Loss Analysis

It can be seen from Figure 5.11 that the presented technique forces some phase clamping to the positive/negative rail and the NP of the DC-link. In particular, when the reference voltage vector is synthesized in subsector-2, twelve commutations take place over a switching cycle, which causes 1.5 times switching losses compared with the original NTV^2 scheme. Nonetheless, in the steady-state of the target systems, space vector is primarily composed in subsector-4, which corresponds to eight turn-on/off actions. As a result, it would be expected that power losses of the proposed strategy are similar to that of the benchmark method in generation mode.

The power losses by the NTV^2 scheme and the modified modulation strategy, as shown in Figure 5.14, are calculated when the aircraft ESG system operates in standby mode and generation mode delivering 25kW active power at a speed of

20krpm. To consistent with the same PWM sampling time as the applied test rig's control platform, the switching frequency in the PLECS tools is also set at 16kHz.

5.3.5 Comparison with Other VSV-Based Modulation Methods with CMV Reduction

Compared with other VSV-based modulation methods with a reduced CMV magnitude [103] and [110], the proposed solution has the following advantages:

1) In [103], the commutation in one phase-leg directly changes from positive DC rail to the negative one. However, the proposed method has the optimal switching sequence transition, i.e., [P]→[O]→[N].

2) The method discussed in [103] only suppresses the primary magnitude of CMV. That is, the maximum component of CMVs is still one-third of DC-link voltage. By contrast, the proposed algorithm effectively constrains that value to one-sixth of DC-link voltage.

3) Because of induced multi-segments pulse trains [103] and [110], the computation burden might be a challenging task for calculating the dwell time based on the traditional α-β reference frame. This drawback has been resolved by the adopted fast modulation approach in the g-h plane.

4) Unlike [103] and [110], the presented strategy abandons small vectors, which indicates two capacitor voltages cannot be actively controlled once NP potential drifts away. Thus, further optimization needs to be completed.

5.4 Simulation Results

The model of the ESG system has been built in the Simulink/PLECS environment, the parameters can be found in Table 5.4. As shown in Figure 5.15, initially, the ESG system runs in starter mode, and flux-weakening control operates at approximately 0.5s. With engine ignition, the speed of PMSM reaches 20krpm. Then, the generation mode activates by connecting a 5kW resistive load to DC-link at 1s and the droop control takes over DC-link voltage regulation at the same time.

Table 5.4: ESG system parameters

Parameters	Value
$L_d = L_q$	99μH
Pole pair	3
Dead time	1.4μs
Switching frequency	16kHz
PM flux	0.03644V$_s$/rad
Base speed	9233rpm
Control system sampling frequency	16kHz
Fundamental frequency in generation mode	1∼1.6kHz
Capacitor value (C_1=C_2)	600μF
DC-link voltage	270V

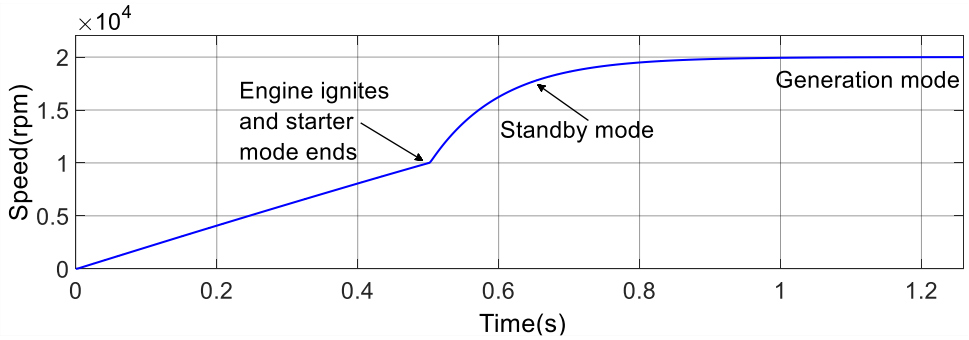


Figure 5.15: ESG speed diagram

5.4.1 Neutral-Point Voltage Oscillation Elimination and Capacitor Voltage Balancing Control

To demonstrate the active capacitor voltage balancing performance, the NTV scheme is chosen as the benchmark method. As seen in Figure 5.16, the benchmark method incurs a large NP voltage oscillation, and even upper and lower-side capacitor voltages (V_{DC}-H&V_{DC}-L) imbalance problem after 0.85s. However, the two capacitor voltages are able to control at a balanced state by using the proposed modulation strategy, activated at 1.1s. In addition, the magnitude of the NP voltage oscillation is also significantly reduced, as shown in Figure 5.17.

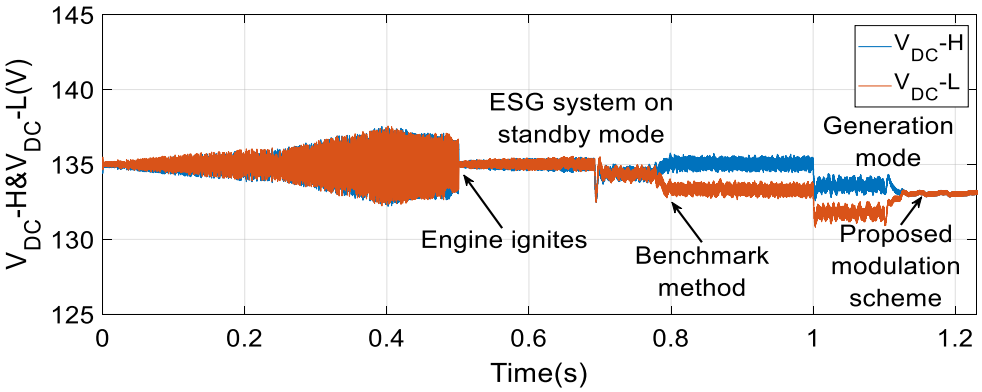


Figure 5.16: DC-link capacitor voltages of the ESG system during entire-speed range operation under the benchmark method and the proposed scheme

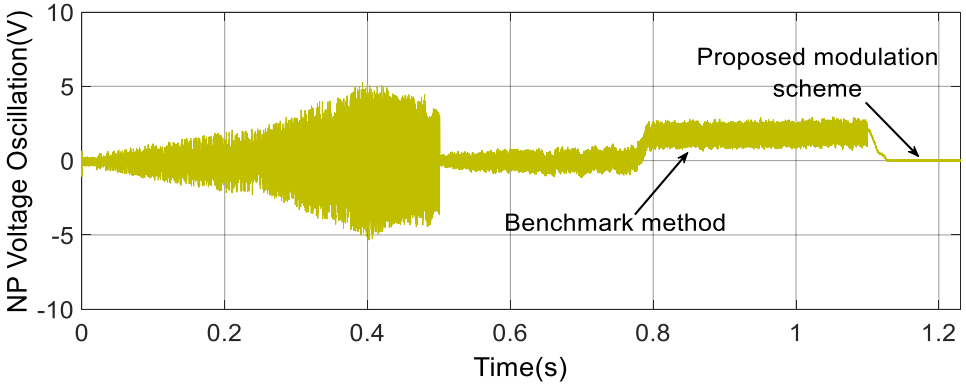


Figure 5.17: NP voltage oscillation of the ESG system under the benchmark method and the proposed scheme

5.4.2 Common-Mode Voltage Reduction

In order to verify the effectiveness of the CMV magnitude reduction using the presented new VSVs, the value produced by the original NTV^2 scheme is chosen as the benchmark and analysed in the following text.

As shown in Figures 5.18 and 5.19, not only can the modified solution balance the NP potential at high modulation indices and low power factor operating points, but also the CMV in the drives is one-sixth of DC-link voltage ($\pm 1/6V_{dc}$), as opposed to one-third of DC-link voltage ($\pm 1/3V_{dc}$) for the conventional NTV^2 scheme. Therefore, with a series of new VSVs, the motor shaft current suppression would be expected to achieve by means of lower ground leakage currents generated by CMVs.

Figure 5.20 shows the line-to-line voltage (V_{AB}) during the algorithm transition

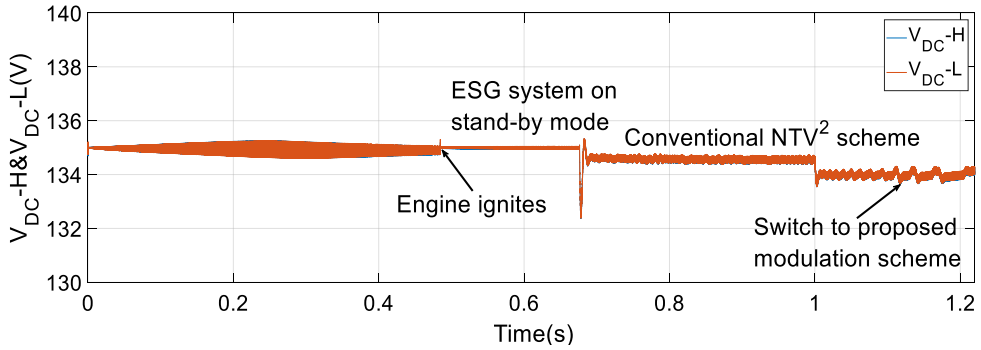


Figure 5.18: DC-link capacitor voltage of the ESG system during entire-speed range operation under the conventional NTV^2 scheme and the proposed modulation scheme

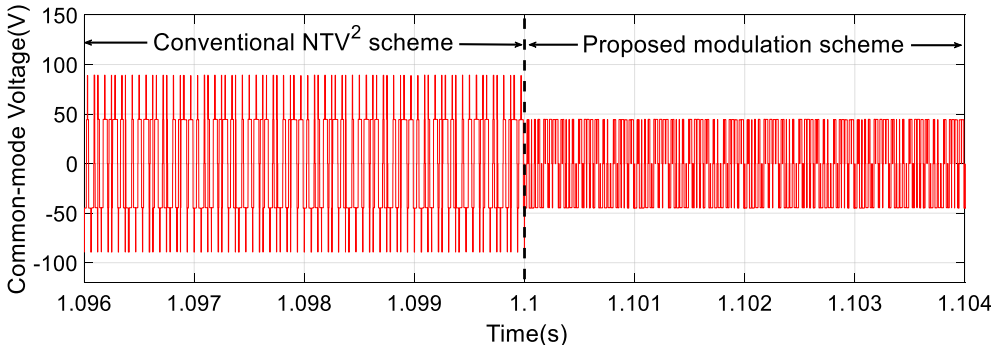


Figure 5.19: CMV comparison of the ESG system under the conventional NTV^2 and the proposed modulation schemes

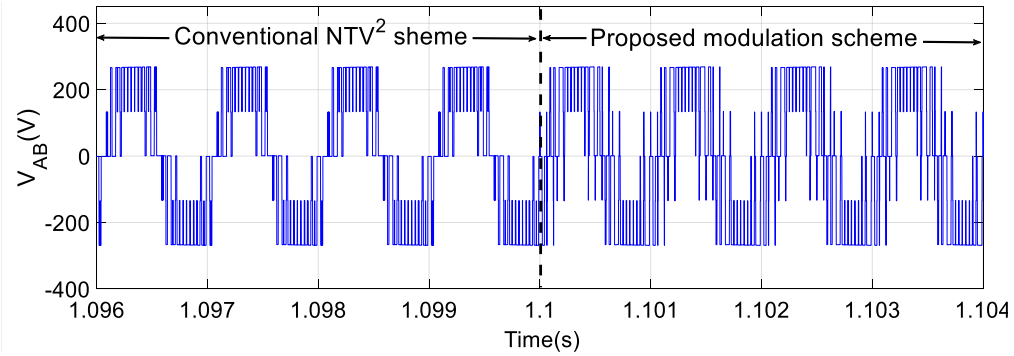
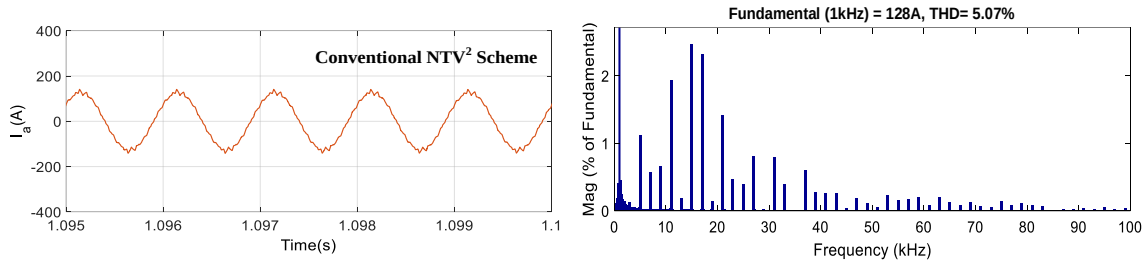


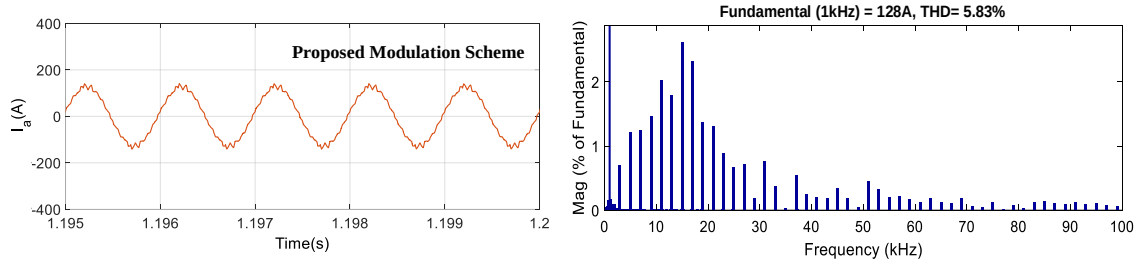
Figure 5.20: The line-to-line voltage during modulation algorithm transition period

period. As can be seen, the three-level switching actions by the proposed modulation scheme are more than for the conventional NTV^2 scheme. This means that equivalent switching frequency and switching losses would be increased.

The harmonic spectrum comparison of phase current (i_a) between the NTV^2 scheme and the proposed method is given in Figure 5.21 for generation mode at a speed of 20krpm. As can be seen, with the proposed PWM strategy, the harmonic



(a)



(b)

Figure 5.21: Phase current (i_a) and its harmonic spectrum in generation mode (a) the conventional NTV^2 scheme (b) the proposed modulation scheme

components are lower than that of the traditional method near the fundamental frequency (1kHz), whereas that value becomes larger near the switching frequency (16kHz). The modified CMV-reduced VSV-based modulation strategy has an output voltage THD of 5.83%, which is higher than the 5.07% for the NTV^2 scheme.

5.5 Experimental Validation

In this section, the simulation results for the two proposed modified modulation techniques are validated using results from a 45kW, 32krpm laboratory-built aircraft ESG prototype system.

5.5.1 Experimental Test-Rig Setup

The hardware of the ESG test rig is shown in Figure 5.22, in which a 150kW torquemeter motor that acts as the prime mover and a high-speed PMSM are connected. The 3L-NPC power converter along with a digital control platform, prime mover controller, host PC and DC source are placed outside the high-speed room. The prime mover mechanically emulates aircraft engine shaft and is coupled to the

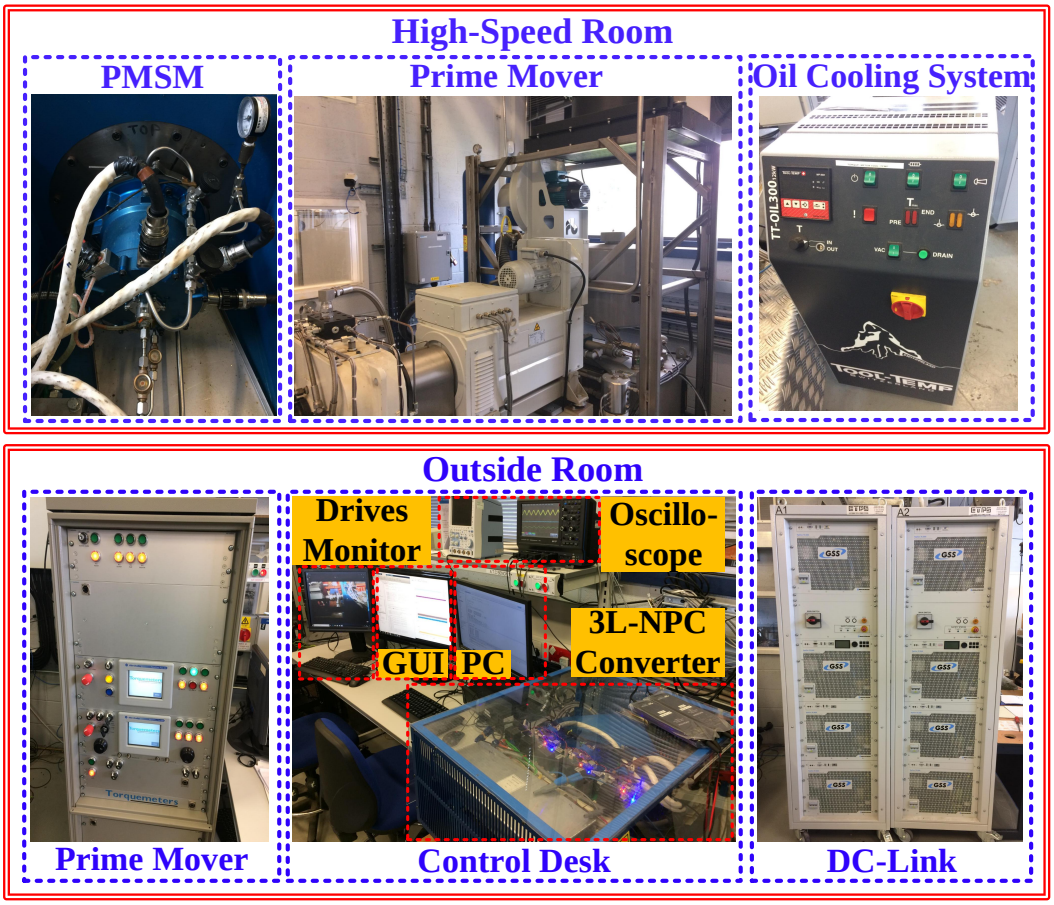


Figure 5.22: The ESG prototype system test-rig setup

PMSM. In order to maintain the machine's winding temperature within the safety range, a TT-OIL300 [151] is used as the cooling system for this aerospace machine. Also, air cooling fans are placed underneath the converter for the purpose of cooling the heat-sink. The grid-tied source sink (GSS) mimics the aircraft electrical power system of 270VDC.

Figure 5.23 shows more details of the 3L-NPC converter within the AEGART project, together with other functional circuits, such as voltage/current sensor board and gate driver. A Development Starter Kit (DSK) with a TMS320C6713 DSP and an Actel FPGA-ProAsic3 A3P400 were used as the control platform, as illustrated in Figure 5.24. The DSP processor can operate up to a frequency of 225MHz and perform eight operations at the maximum per cycle. The control scheme is im-

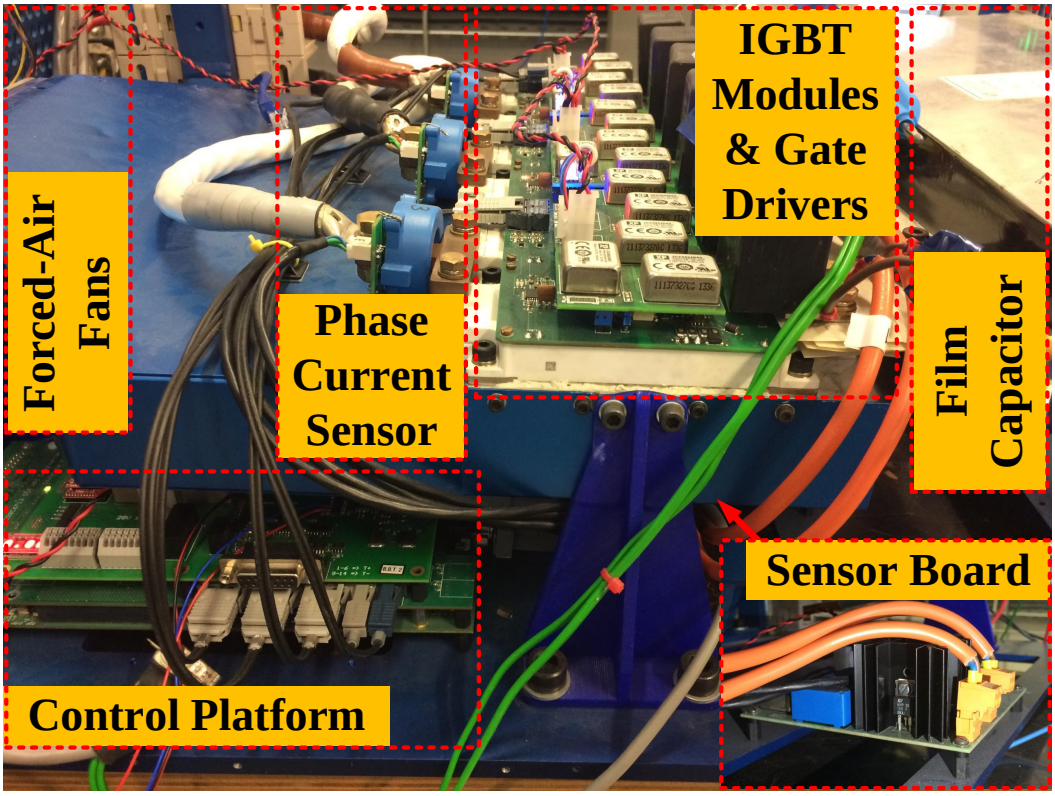


Figure 5.23: 3L-NPC power converter with other functional circuits

plemented in C-language and programmed into the DSP via the Code Composer Studio (CCS) on the computer. The control signal output from the DSP is then sent to the FPGA that is used to interface the hardware by a hardware description language (HDL). This allows the data transfer between both components to be very fast ($\leq 10\mu$s depending on DSP's capabilities). The main functions of the FPGA in this AC drive system are pulse generation for PWM, online data measurement and conversion from the sensors, and hardware circuit protection for overcurrent/voltage. A host port interface (HPI) capture card is connected to the DSP which interfaces to the computer by the Graphic User Interface (GUI) software so that all control variables can be displayed on the host PC. AC-side parameters are monitored using a PPA5530 power analyser. The converter's output variables are measured using high voltage differential voltage probes and CP500 current probes, displayed on a Teledyne LeCroy oscilloscope.

Since the phase current direction changes rapidly under light-load conditions, it

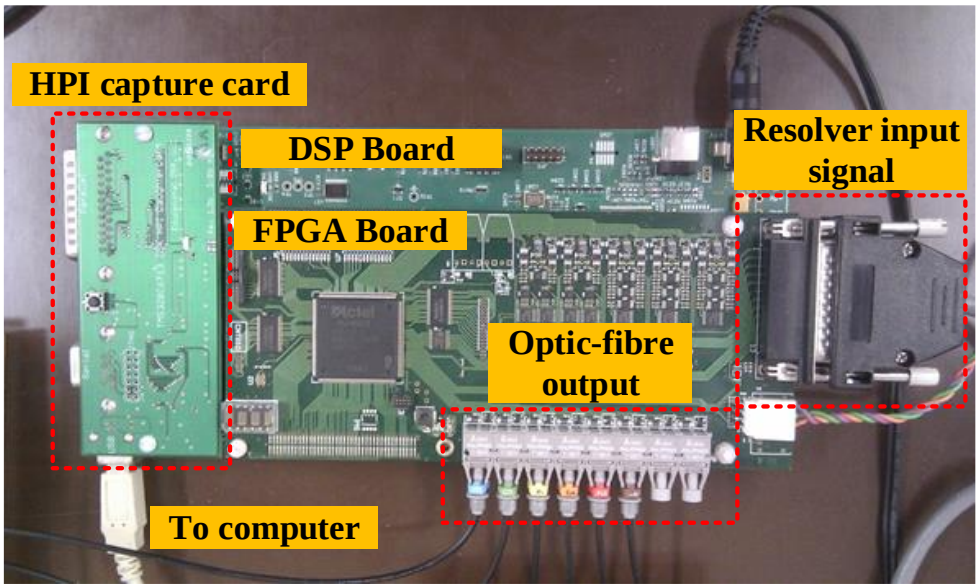


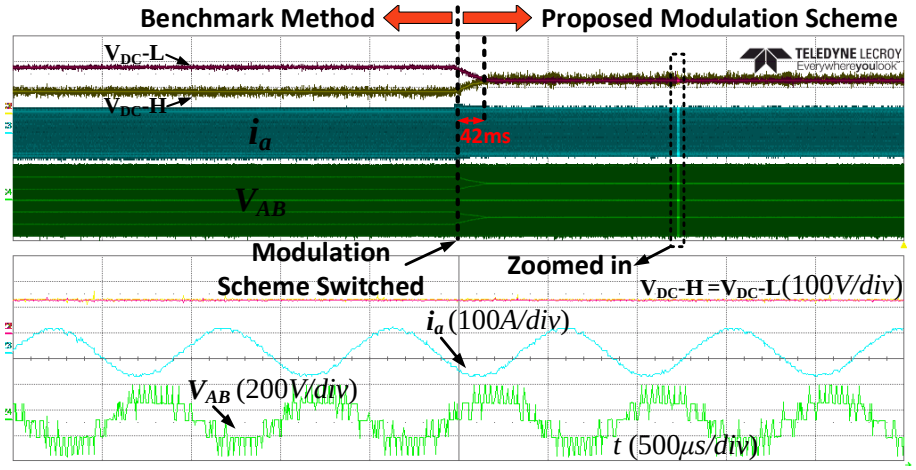
Figure 5.24: Overview of the digital control platform

aggravates the NP voltage imbalance problem, particularly for high modulation index and low power factor operating points [152, 153]. As a result, the experimental tests primarily focus on when the target system operates under the light-load conditions in power generation mode, i.e., the delivered active power is less than 10kW. The startup process is not presented here as motoring mode takes up a short time compared with the ESG system's power generating mode during the flight.

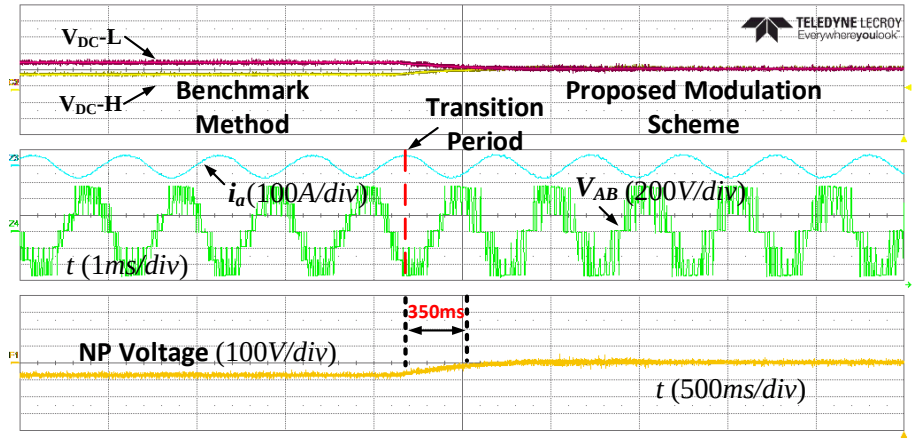
5.5.2 Computational Efficiency

The execution time can be measured by the controller. The results show that, after adopting the fast reference frame, 46.3μs is the time taken by the proposed active NP voltage balancing control method within a PWM interruption service, which is almost 20% lower than the traditional implementation in the α-β reference frame at 55.56μs.

The proposed CMV-reduced VSV-based SVM scheme has an execution time of 58.7μs. Compared with the same algorithm using the α-β reference frame, that time is reduced by 14%. Overall, the computational effort has been significantly reduced.



(a)



(b)

Figure 5.25: Transition from the benchmark method to the proposed modulation scheme at 20krpm (a) MI=0.82, PF=0.46 (b) MI=0.95, PF=0.12

5.5.3 Active Capacitor Voltage Balancing Performance

The experimental validation of the NP voltage balance is carried out when the machine speed is at 20krpm with a q-axis current demand of -20A, in which the average modulation index and power factor are 0.82 and 0.46 in this case, respectively. The conventional NTV scheme is chosen as the benchmark method. As shown in the zoomed-in waveforms in Figure 5.25(a), after switching to the proposed modulation scheme, NP voltage can be quickly maintained balanced again within 42ms. The transition period at an average modulation index of 0.95 and a power factor of 0.12 is shown in Figure 5.25(b). As shown, NP potential drift results in a static voltage

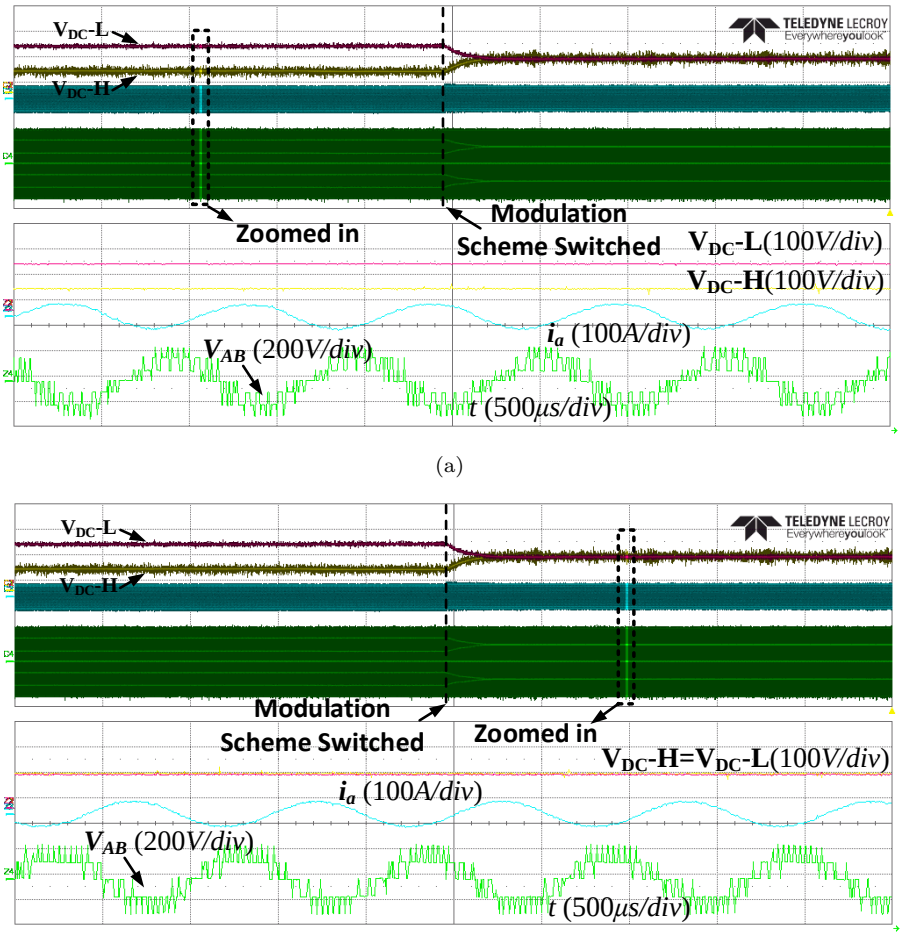
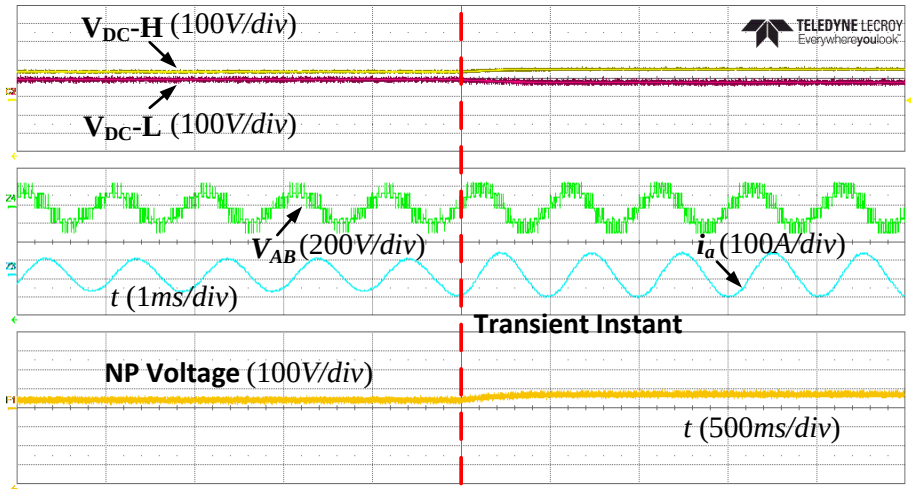


Figure 5.26: Capacitor voltage balancing performance at 20krpm with (a) the conventional NTV^2 scheme (b) the modified modulation strategy

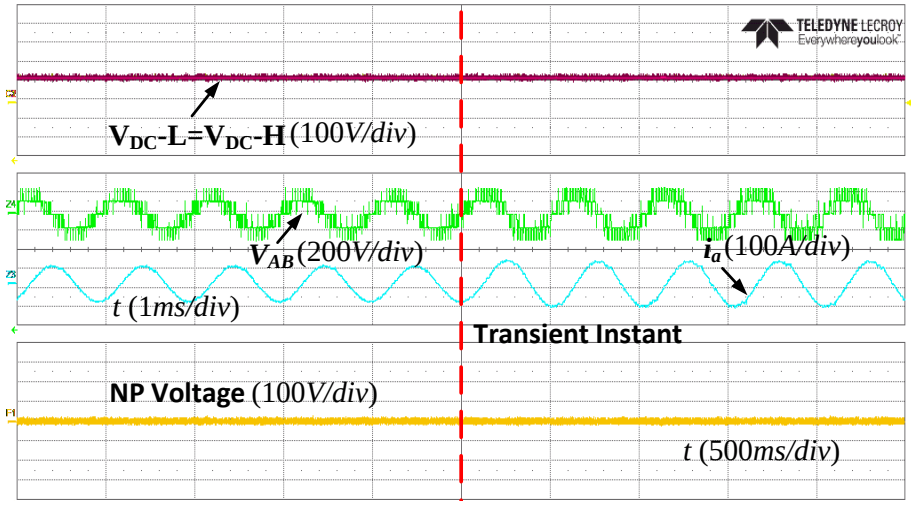
error across two capacitors and the phase voltage is distorted under the benchmark method, while this issue can be resolved within 350ms with the proposed algorithm.

The NP voltage balancing control performance is tested comparing the traditional NTV^2 scheme and the proposed algorithm. In order to validate the provided technical superiority, the lower-side capacitor voltage is initially pre-charged to 185V, with a modulation index of 0.95 and a power factor of 0.12. As shown in Figure 5.26, the original NTV^2 method still maintains the existing voltage error. Nevertheless, the deviated capacitor voltage is corrected when the proposed modulation scheme is activated.

To validate the NP voltage balancing control performance under dynamic condi-



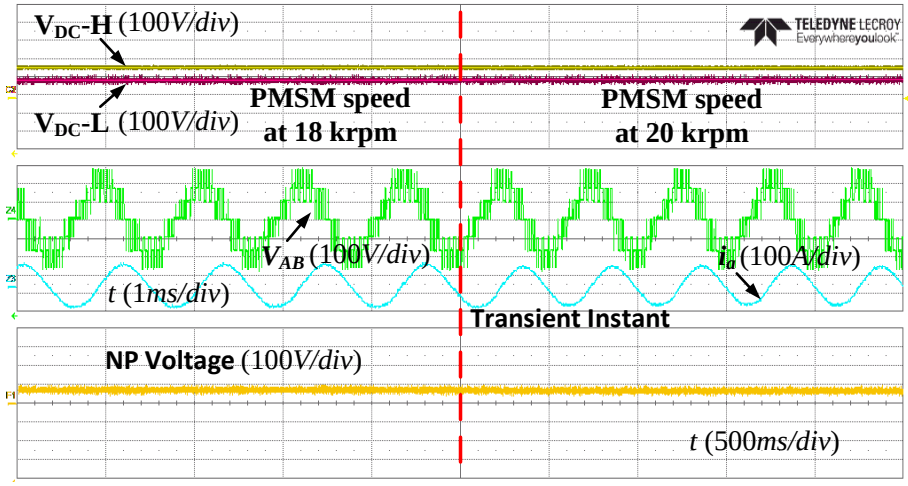
(a)



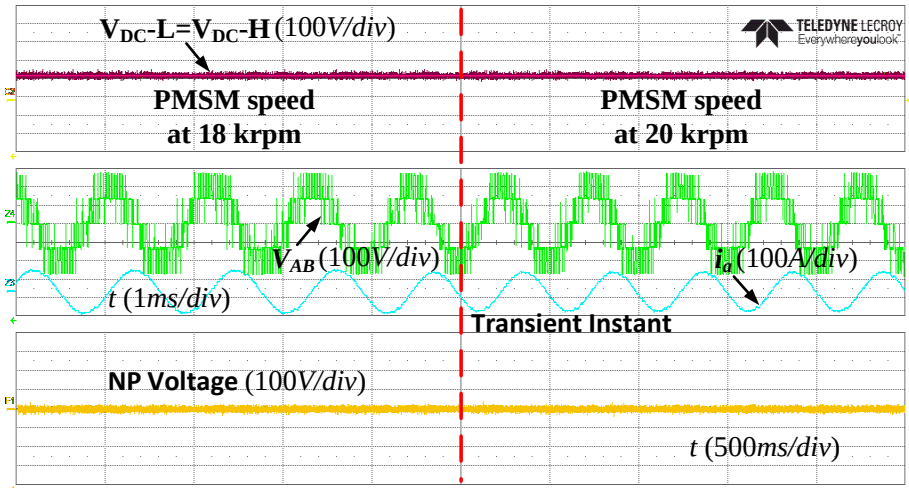
(b)

Figure 5.27: NP voltage control performance during the loading process (a) the benchmark method (b) the proposed modulation scheme

tions, the experimentation is conducted under two situations, load and speed-change conditions. The first scenario is represented as a q-axis command current increasing from -5A to -25A in power generation mode. It can be seen from Figure 5.27(a) that the NP voltage is unbalanced with the benchmark method during the transient process. By contrast, two capacitor voltages can effectively maintain at a balanced state under this situation with the proposed strategy, as shown in Figure 5.27(b). The proposed active capacitor voltage control is also tested when the average machine speed is ramped up from 18krpm to 20krpm. The results in Figure 5.28(a) shows that the benchmark method always causes a NP potential imbalance in the



(a)



(b)

Figure 5.28: NP voltage control performance during the change of speed (a) the benchmark method (b) the proposed modulation scheme

case of a speed-change. Nevertheless, the capacitor voltage can be well controlled by the proposed active modulation technique under this process, as shown in Figure 5.28(b). Thus, the superior dynamic performance of the proposed modulation algorithm has been improved as compared to the conventional NTV scheme.

The harmonic content of NP voltage oscillations using FFT analysis is shown in Figure 5.29. Not only is the DC voltage imbalance effectively eliminated, but also the magnitude of low-frequency NP voltage oscillation, including 3^{rd}-order harmonics, is reduced. The THD of phase current with the benchmark and the proposed method are 4.72% and 5.83%, respectively.

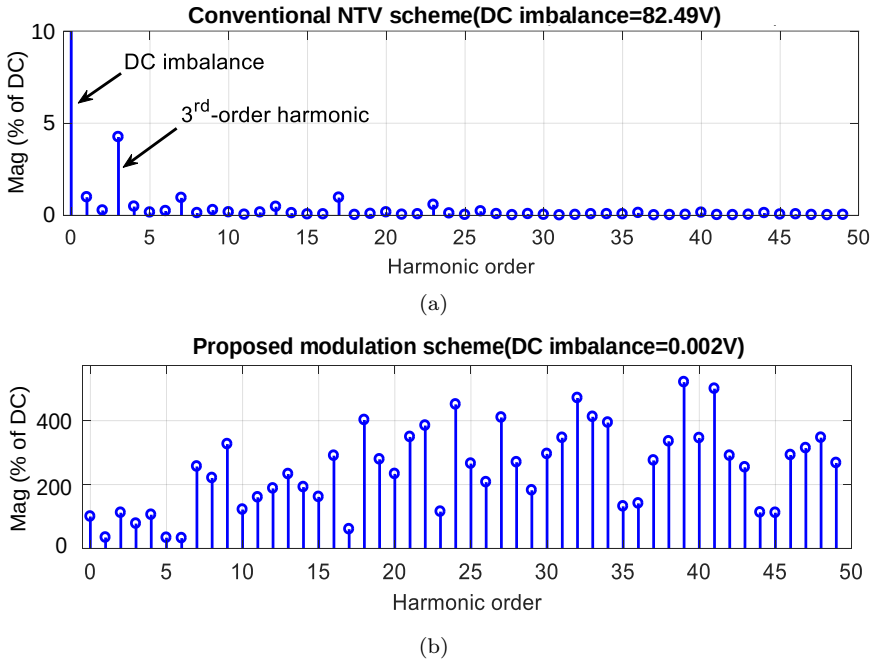


Figure 5.29: FFT analysis of NP voltage oscillation (a) the benchmark method (b) the proposed modulation scheme

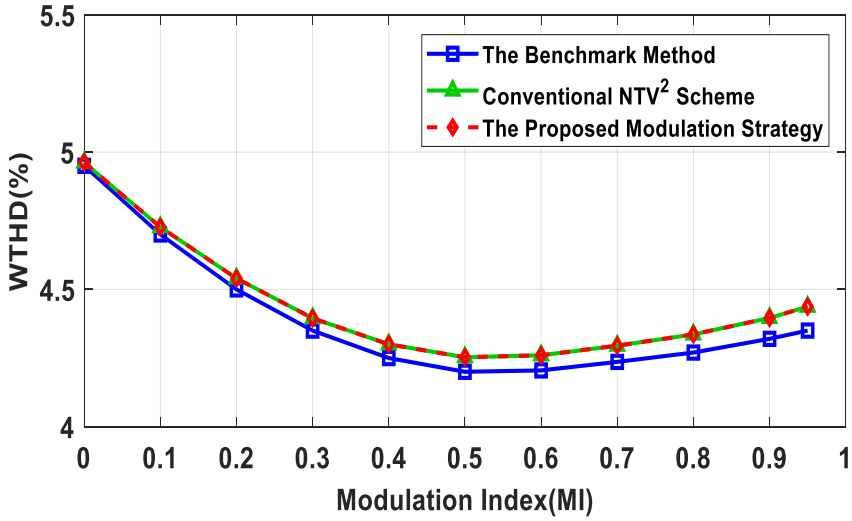
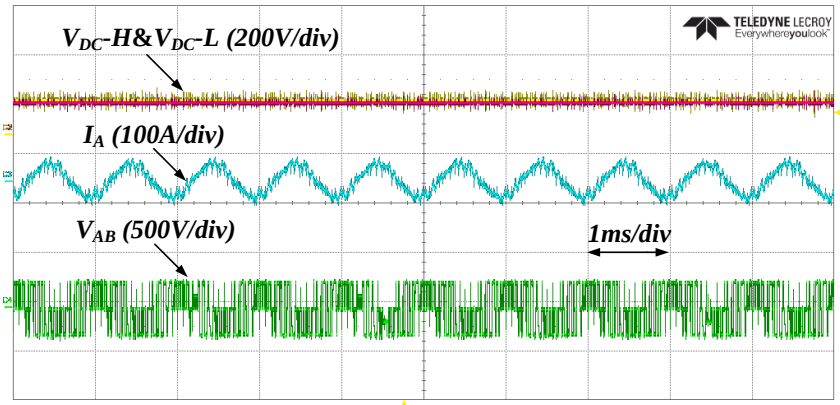
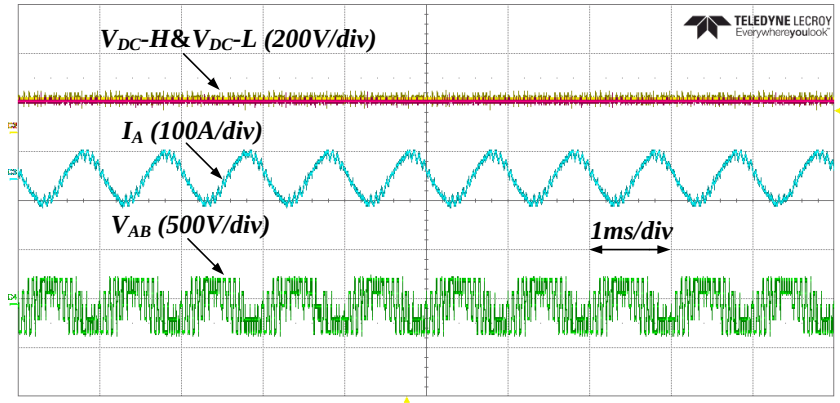


Figure 5.30: WTHD of the line-to-line voltage with different modulation strategies

Figure 5.30 shows the weighted THD (WTHD) comparison for the line-to-line voltages under the different modulation strategies. As can be seen, at lower modulation indices, the curves are similar for each method. When the modulation index increases, compared with the benchmark method, that value by both the NTV^2 and the proposed modulation strategy have slightly higher harmonic distortion. This is



(a)



(b)

Figure 5.31: Experimental results of two capacitor voltages, phase current and the line-to-line voltage at (a) MI=0.45 and PF=0.80 (b) MI=0.95 and PF=0.15

due to the additional three-level switching intervals during some periods.

5.5.4 Common-Mode Voltage Reduction

The CMV in the ESG system is measured with a machine speed of 20krpm in power generation mode. A light-load condition is still taken into consideration for the following verification.

Figure 5.31(a) shows the two capacitor voltages, phase current and the line-to-line voltage when the q-axis current command is -2A and the flux-weakening control is initiated. The average modulation index and power factor are 0.45 and 0.80, respectively. It can be seen that a balanced NP voltage is attained. When the q-axis current command is -20A and a deep d-axis current is injected, with a

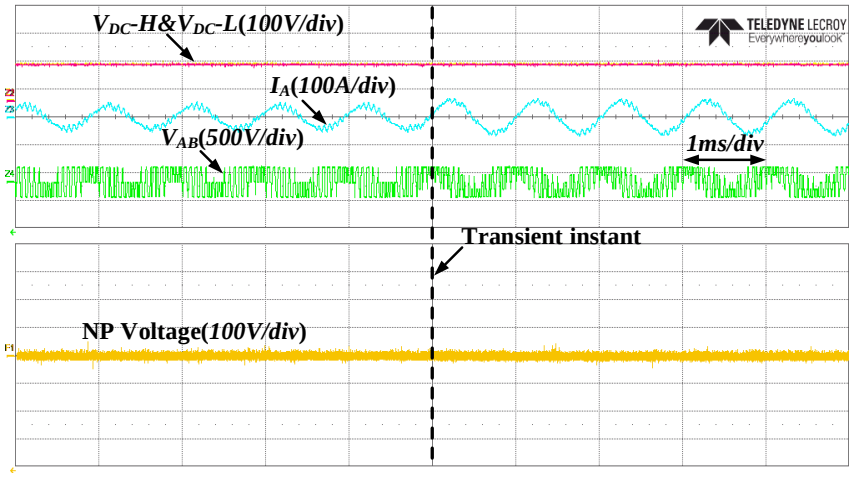


Figure 5.32: Experimental results under modulation index changing from 0.6 to 0.9

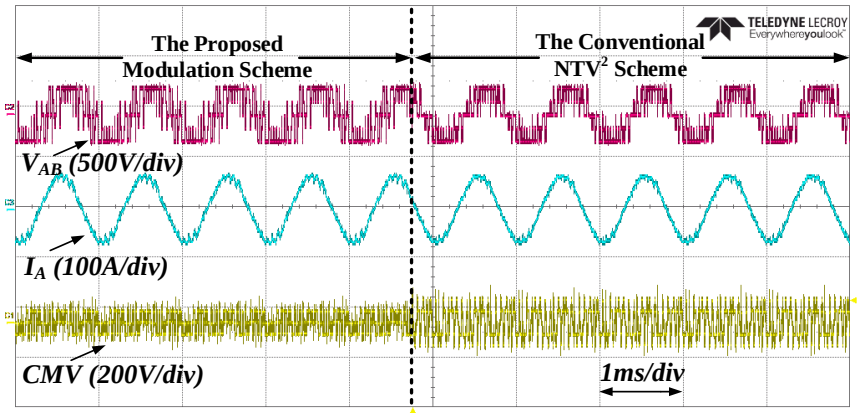


Figure 5.33: Experimental results of the line-to-line voltage, phase current and CMV during modulation strategy transition period

modulation index of 0.95 and power factor of 0.15, the capacitor voltages can be maintained balance as well, as shown in Figure 5.31(b). With respect to the dynamic conditions, the experimental results for the proposed algorithm are shown in Figure 5.32, in which the modulation index is changed from 0.6 to 0.9 instantly. It is shown that NP voltage can be well balanced under this transient demand step.

The line-to-line voltage, phase current and CMV between the conventional NTV^2 method and the proposed scheme are compared when the machine operates at 20krpm in the steady-state, as shown in Figure 5.33. It can be clearly seen that the CMV produced by the proposed solution is half of the CMV for the NTV^2 method. As the selected space vectors are not the nearest three, the THD of phase

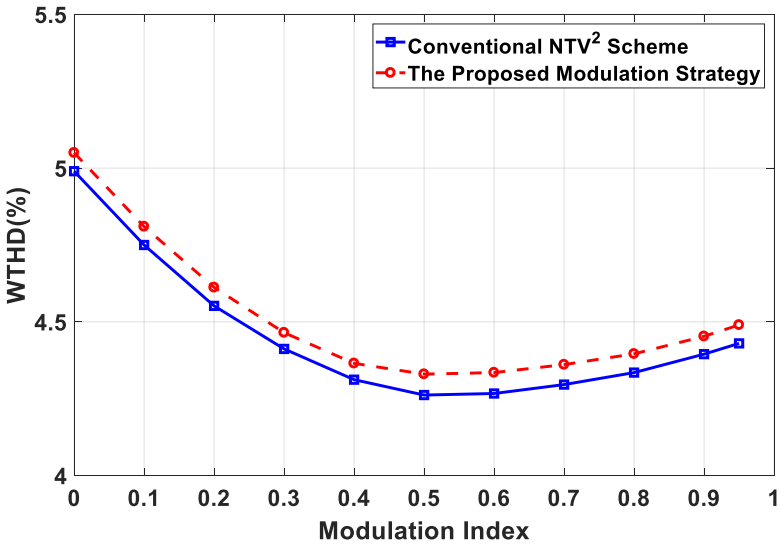
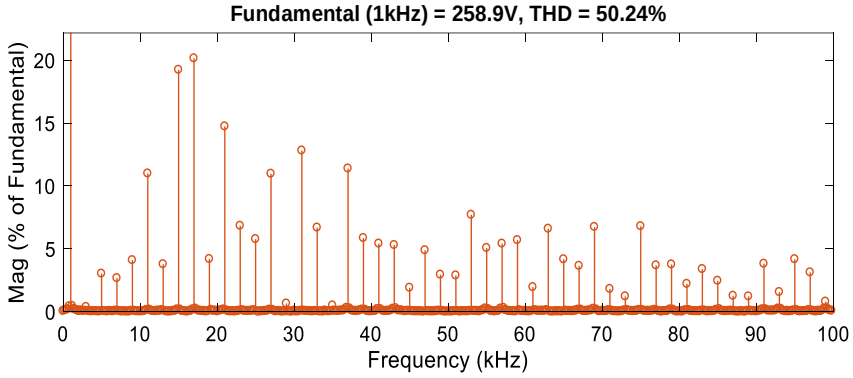
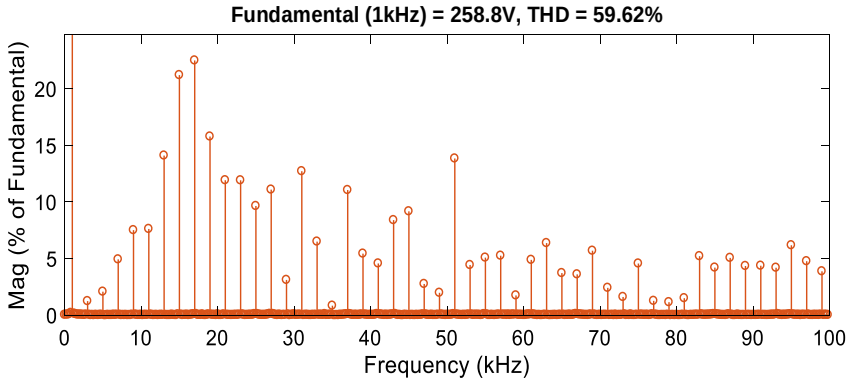


Figure 5.34: WTHD of the line-to-line voltage with different modulation strategies



(a)



(b)

Figure 5.35: Harmonic spectra of the line-to-line voltage at the steady-state operating point with (a) the conventional NTV^2 scheme (b) the proposed modulation scheme

current under the proposed scheme is 5.87%, which is higher than that of the NTV^2 strategy at 5.02%.

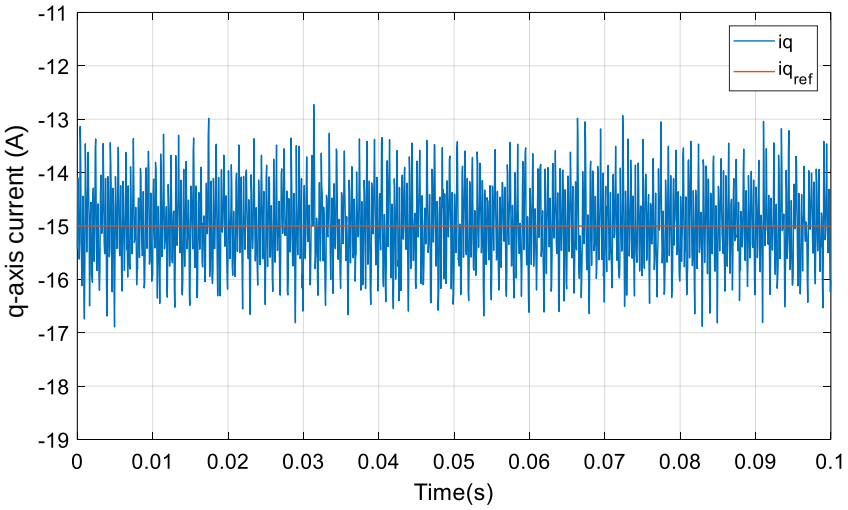
Figure 5.34 shows the WTHD comparison results for the line-to-line voltage by the benchmark method and the proposed modulation technique with different modulation indices. As shown, both of them follow the same trend. For the proposed scheme, this value is larger than for the NTV^2 method, particularly for the high modulation indices. This is because the three-level switching instants occur in two-phase legs for a period of the time.

Figure 5.35 shows the harmonic spectra for the line-to-line voltage under the conventional NTV^2 scheme and the proposed strategy when the ESG system works at the steady-state operating point. It can be seen that, due to the adopted non-nearest space vectors with lower CMVs, a THD of 59.62% with the proposed method is higher than for the original scheme at 50.24%.

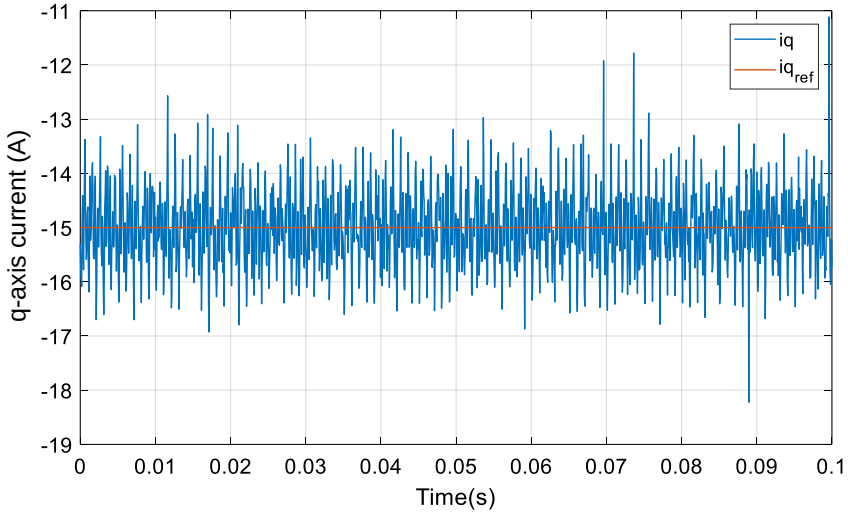
As the pole-pair numbers and magnet flux are constant values for the surface-mounted PMSM, the torque ripple is proportional to q-axis current ripple. Here, in order to evaluate the torque ripple, q-axis current is measured and displayed by the GUI when the ESG system operates in generation mode, in which the q-axis reference current is set to be -15A and the aircraft S/G systems deliver an approximate active power of 6kW. It can be seen from Figure 5.36 that the maximum magnitude of i_q spike caused by the presented modulation technique is around $\pm$3.7A as compared to $\pm$2.1A by its counterpart. Furthermore, the average ripple generated by the proposed strategy ($\pm$1.5A) roughly increases by 3.1% compared with the traditional approach ($\pm$1A). Accordingly, the torque ripple would also be proportionally increased in the motor drives.

5.5.5 Overall Modulation Performance Comparison

Table 5.5 summarises the modulation performance comparison of the PWM methods studied in this Chapter, i.e., the NTV, the NTV^2, the proposed active NTV^2 and the proposed CMV-reduced NTV^2 strategies. As can be seen, in addition to the NTV scheme, the other modulation approaches feature minimized NP voltage fluctuation. Nevertheless, this merit comes as a higher power loss, particularly for the CMV-reduced NTV^2 scheme. With respect to the CMV magnitude, the proposed CMV-



(a)



(b)

Figure 5.36: Quadrature-axis current of the applied surface-mounted PMSM in generation mode with (a) the conventional NTV^2 strategy (b) the proposed modulation strategy

reduced NTV^2 scheme attains a lower value compared with the others. However, this scheme contributes to higher harmonic distortion. In this regard, the NTV scheme performs well, followed by the NTV^2 scheme. In terms of the computational efficiency, the NTV scheme is the simplest algorithm, whereas the other solutions increase the complexity to some extent, in which the CMV-reduced NTV^2 scheme suffers from the most computational burden.

Table 5.5: The comparison of modulation strategies performance

Methods / Performance	NTV scheme	NTV^2 scheme	Proposed active NTV^2 scheme	Proposed CMV-reduced NTV^2 scheme
Neutral-point voltage ripple	large	small	small	small
Common-mode voltage	high	high	high	low
Harmonic distortion	low	medium	medium	high
Power losses	low	medium	medium	high
Complexity	low	medium	medium	high

5.6 Conclusions

In this Chapter, the conventional NTV^2 modulation strategy has been modified to give two new SVM techniques for the 3L-NPC converter-fed high-speed aerospace electrical machine drives.

The first scheme aims to achieve active capacitor voltage balancing for the 3L-NPC topology. It is shown that the conventional NTV scheme causes a large voltage oscillation and even drift in the NP when the ESG system operates at a high modulation index and a low power factor. Although the conventional NTV^2 scheme achieves natural NP voltage balance and reduces the low-frequency NP potential oscillation irrespective of output voltage and load angles, it might be hardly applied directly since this method lacks active capacitor voltage balancing control capability if NP voltage drifts away from zero. With the proposed duty cycle offset, two diverged capacitor voltages can be recovered even though the imbalance issue emerges.

Due to the fact that the CMV generated by the conventional NTV^2 scheme is still high for the target aerospace drives, which puts the system's reliability at risk. Therefore, the purpose of the second approach is to achieve two optimized objectives. That is, NP voltage balance and CMV reduction at the same time. In order to meet the above requirements, the proposed modulation technique is designed by modifying a series of VSVs with lower CMV magnitude. Good performance is attained at

the expense of more switching actions, particularly for a higher modulation depth region. This facilitates a trade-off in terms of THD of phase voltage and the phase current/torque ripple.

The computational burden has been significantly overcome by implementing these two modified approaches in the g-h reference frame, which is beneficial for the computational efficiency of digital controllers in high switching frequency applications. The simulation and experimental results shown in this Chapter proved the effectiveness and feasibility of the proposed modulation strategies.

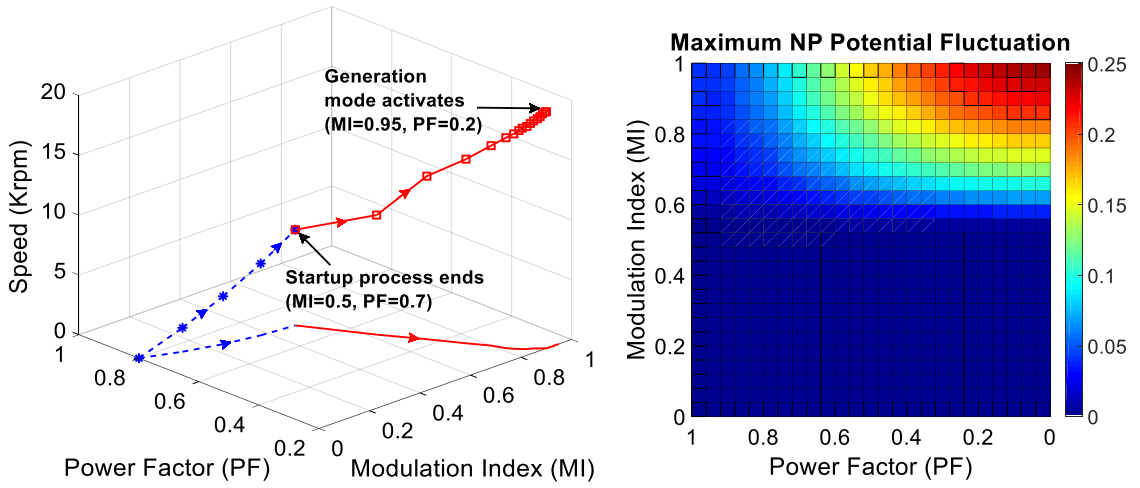
Chapter 6

Hybrid Modulation Algorithm for Three-Level NPC Converter

This Chapter presents a hybrid SVM (HBSVM) technique for the 3L-NPC converter according to the operating conditions of the ESG system. Aiming to attain a high-performance modulation strategy for both starter and generation mode, the proposed algorithm combines two types of SVM approaches together. The solution employs the NTV scheme in the low modulation index region, in which it corresponds to the startup process. In this case, switching loss would be expected to reduce in comparison with the conventional NTV^2 scheme. Moreover, an advanced NTV^2-based technique featuring reduced common-mode voltages is deployed in power generation mode. Additionally, in order to achieve the ability of active NP voltage balancing control, the phase duty cycle is regulated to compensate for extra electric charge in the NP. The fast calculation approach is adopted to simplify the complicated computational burden which the proposed study may cause.

6.1 Introduction

Since the studied 3L-NPC converter-fed S/G system exhibits a wide-speed range operation, each operating mode can be optimized from the hybrid modulation concept



(a) (b)

Figure 6.1: The characteristics for wide-speed range operation of the aircraft ESG system (a) correlation among modulation index, power factor and speed during a T_{ESG} (b) normalized amplitude of DC-link capacitor voltage fluctuation

viewpoint. The existing literature about the hybrid PWM technique for the three-level topology is discussed in the following. A hybrid CBPWM scheme has been developed in [154] to lower switching loss. A hybrid SVM solution proposed in [155] combines the NTV and NTV^2 scheme. Therefore, balanced capacitor voltages, lower switching frequency and better output harmonics are realized all the time. An adjustable proportional hybrid modulation scheme has been carried out for reducing power loss within an allowable NP voltage ripple range [156]. Nonetheless, a complicated implementation process might be a challenging task as the number of the total switching states of the method is extended from 27 to 39. In [157], with logical control blocks, a CBPWM scheme supplemented by SVM scheme is presented to improve modulation performance for traction drives. A method that selectively incorporates the NTV and NTV^2 schemes is discussed in [158] for a three-level photovoltaic (PV) inverter under imbalanced grid faults. However, the CMV issue is not considered to alleviate during the low-voltage-ride-through (LVRT) operation. In addition, based on the converter's operating points, a dual-mode modulation strategy [159] is investigated for grid-connected NPC converters feeding bipolar DC loads. More recently, a hybrid method [160] by synergizing the medium vector SVM and DPWM scheme is reported to eliminate leakage current and balance NP volt-

Table 6.1: Hybrid modulation concept-based PWM schemes

Exisiting methods	Characteristics
Hybrid CBPWM scheme [154]	Switching loss reduction
Hybrid SVM scheme [155]	Balance NP voltage for all loads
Proportional hybrid modulation scheme [156]	Large NP voltage fluctuation
CBPWM supplemented by SVM scheme [157]	Logical control blocks needed
Selective hybrid modulation scheme [158]	For imbalanced grid faults
Dual-mode modulation strategy [159]	For feeding bipolar DC loads
SVM and DPWM synergy scheme [160]	Leakage current elimination

age for a TNPC converter in the PV systems. Table 6.1 summarises the hybrid modulation strategies in the existing literature.

Since the conventional modulation strategies have their own advantages and disadvantages. Also, the studied ESG system is featured with wide-speed range operations, variable modulation indices and power factors, as depicted in Figure 6.1(a). It can be seen that the 3L-NPC converter spends 20% of T_{ESG} for running as an inverter until the starup process ends, and then it serves as a rectifier for the rest of the operational time, where a T_{ESG} (typically about 200 seconds) is defined as the time of the converter-fed PMSM drives starting from the standstill to the speed of 20krpm. On the other hand, from the analysis in Chapter 3, it is known that the voltage fluctuation in the NP varies with different modulation indices and power factors, as illustrated in Figure 6.1(b). Consequently, the globally optimized modulation strategy is beneficial for the target systems.

In this Chapter, a novel HBSVM algorithm is proposed for the 3L-NPC converter. According to the operating characteristics of the ESG system, the PWM modulator employs the NTV scheme in the low modulation index region, in which it corresponds to the starter mode. As a result, fewer switching actions can benefit lower switching losses in comparison with the NTV^2 scheme. Given that voltage stress of the motor

would be substantially increased when the CMV is imposed on machine terminals, and also its steep changes can induce damaging ground leakage, bearing currents and emission of common-mode noise. Moreover, irreversible damage of the winding insulation might be a threat to the applied high-speed electrical machine drives. Thus, an enhanced NTV^2-based modulation technique with suppressed CMVs is employed to improve the reliability of the ESG system in power generation mode. In order to correct the balanced capacitor voltages, the phase duty cycle is regulated to compensate for additional electric charge in the NP. The algebraic calculation is adopted to improve computational efficiency for digital control systems. The more detailed information will be given in the following Sections.

6.2 Principle of the Proposed Hybrid Modulation Technique

6.2.1 Definition and Dwell Time Calculation

Without loss of generality, the first sector is chosen as a representative example to explain. Through the establishment of the *g*-*h* plane, the space vector diagram (SVD) of the proposed HBSVM technique is shown in Figure 6.2. As can be observed, its subsector identification criteria is similar to that of the NTV^2 scheme. The corresponding half switching-sequence is: [ONN]→[OON]→[OOO]→[POO]. It can be seen that, when the reference voltage vector is located in subsector-1, redundant small vector pairs [POO] and [ONN] denoted as V_{S1}, small vector [OON] indicated as V_{S2}, and zero vector [OOO] manifested as V_0 are chosen to synthesize V_{ref}. Similarly, when the reference voltage vector falls into subsector 2, V_{ref} will be composed of redundant small vector pairs [PPO] and [OON] denoted as V_{S2}, small vector [POO] indicated as V_{S1}, and zero vector [OOO] manifested as V_0. In this case, the half switching-sequence is: [OON]→[OOO]→[POO]→[PPO].

Based on the volts-second principle in the *g*-*h* reference frame, as given in equation (4.7), the corresponding duty cycle of space vectors can be calculated as follows:

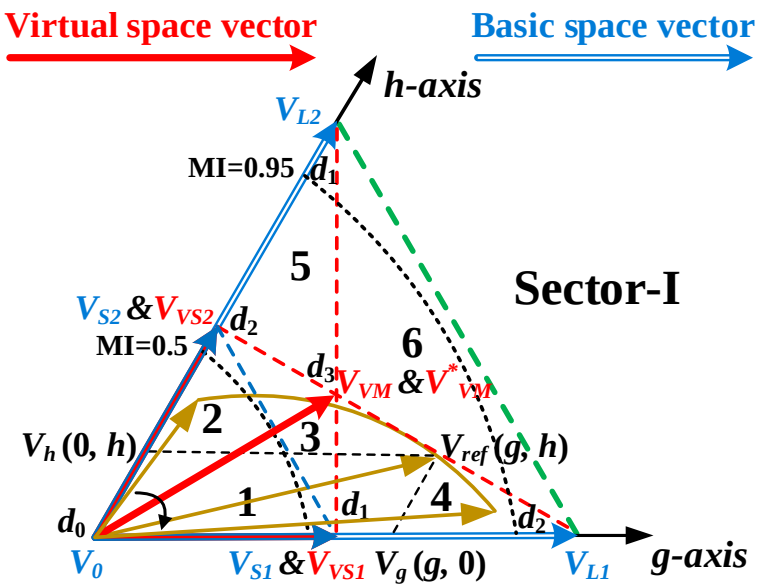


Figure 6.2: SVD of the proposed HBSVM strategy in the g-h plane

$$\begin{cases} d_1 = 2g \\ d_2 = 2h \\ d_0 = 1 - 2(g + h) \end{cases} \tag{6.1}$$

where d_1, d_2 and d_0 represent the duty cycle of V_{S1}, V_{S2} and V_0, respectively.

As seen from Figure 6.1(a), the conventional NTV scheme leads to a large NP voltage fluctuation when the modulation index exceeds 0.5. Hence, the VSVs are preferred to employ in subsectors 3-5 for their superiority of eliminated NP potential fluctuation and balanced DC-link capacitor voltages irrespective of output voltages and load angles.

Likewise, the duty cycles associated with the NTV^2 scheme can be derived:

(i) For subsector 3

$$\begin{cases} d_1 = 1 - g - h \\ d_2 = 1 - g - h \\ d_3 = 2(g + h) - 1 \end{cases} \tag{6.2}$$

(ii) For subsector 4

$$\begin{cases} d_1 = 2 - 2(g + 2h) \\ d_2 = 2g + h - 1 \\ d_3 = 3h \end{cases} \tag{6.3}$$

(iii) For subsector 5

$$\begin{cases} d_1 = 2h + g - 1 \\ d_2 = 2 - 2(h + 2g) \\ d_3 = 3g \end{cases} \tag{6.4}$$

where d_1, d_2 and d_3 refer to the duty cycles of the VSVs shown in Figure 6.2.

In order to avoid the risk of premature motor bearing failure rendered by shaft current, the basic vectors composing VSVs should be chosen based on their CMV magnitude. For our case, more attention needs to be given to subsector 6. This is because most output voltage vectors are near the hexagon side in the power generation mode of the ESG system.

As can be seen from Table 5.3, not only can medium vectors produce zero CMV, but also NP currents of the adjacent three medium vectors are three-phase stator currents, i_a, i_b and i_c. Considering that the target drive systems feature i_a+i_b+i_c=0, a new virtual medium vector presented in Chapter 5 can be therefore synthesized to obtain inherent NP voltage balance and CMV mitigation at the same time.

The dedicated space vectors and corresponding duty cycles for subsector 6 are given as follows:

$$\begin{cases} V_{L1} = V_{[\mathrm{PNN}]} \\ V_{L2} = V_{[\mathrm{PPN}]} \\ V_{VM}^{*} = (V_{[\mathrm{OPN}]} + V_{[\mathrm{PON}]} + V_{[\mathrm{PNO}]})/3 \end{cases} \tag{6.5}$$

$$\begin{cases} d_1 = 2h + g - 1 \\ d_2 = 2g + h - 1 \\ d_3 = 3(1 - g - h) \end{cases} \tag{6.6}$$

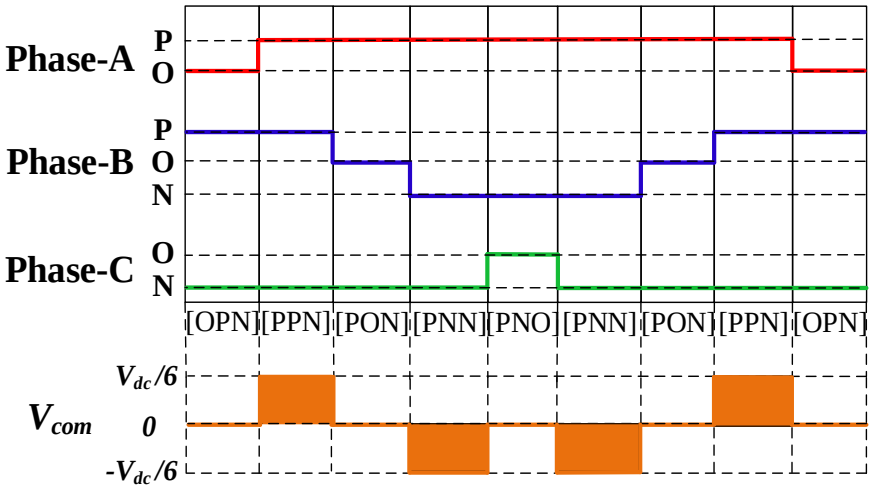


Figure 6.3: Pulse train of the proposed HBSVM for subsector-6 of Sector-I

Table 6.2: Half switching sequence of the proposed hybrid modulation strategy

Subsector	Half Switching Sequence
1	[POO]→[OOO]→[OON]→[ONN]
2	[PPO]→[POO]→[OOO]→[OON]
3	[PPO]→[POO]→[PON]→[OON]→[ONN]
4	[PPO]→[POO]→[PON]→[PNN]→[ONN]
5	[PPO]→[PPN]→[PON]→[OON]→[ONN]
6	[OPN]→[PPN]→[PON]→[PNN]

Figure 6.3 shows the pulse trains generated by the proposed HBSVM technique for subsector-6 of Sector-I. It can be clearly seen that the magnitude of CMV is confined within $\pm V_{dc}/6$. Despite the fact that the peak value of CMVs in subsectors 4-5 are still $\pm V_{dc}/3$, the synthesis period amongst these areas takes a short time as compared to that of subsector 6 over a fundamental cycle, particularly for near unity modulation index condition. Table 6.2 details the half-switching sequence of the proposed modulation algorithm.

6.2.2 Initial Capacitor Voltage Imbalance

Similar to the modified NTV^2 scheme presented in Chapter 5. Aiming to correct drifted NP voltage with the proposed HBSVM scheme, in this subsection, the ad-

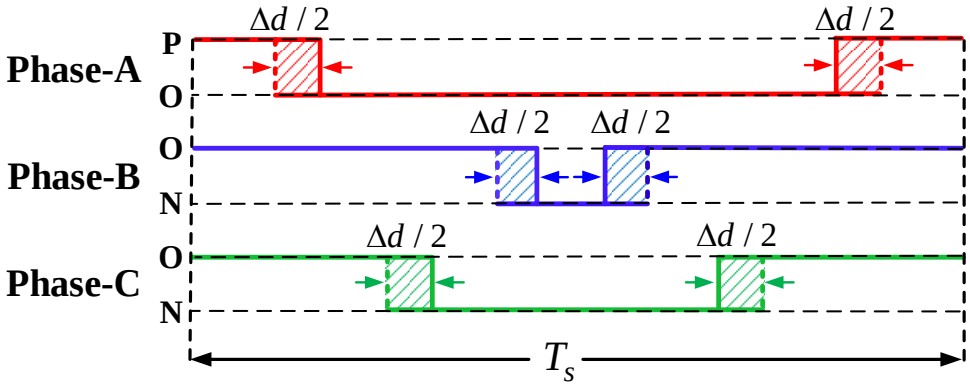


Figure 6.4: Pulse train with active capacitor voltage balancing control for subsector 1

justment of duty cycle for each small vector is investigated when an initial capacitor voltage imbalance exists in the DC-link.

The coefficient k defined by equation (5.1) is used to measure the voltage imbalance range ΔV_{dc}.

$$\Delta V_{dc} = (2k-1)(V_{dc1} + V_{dc2}) \tag{6.7}$$

where V_{dc1} and V_{dc2} represent the upper and lower-side capacitor voltage, respectively, and $k \in [0, 1]$.

From equation (6.7), it can be seen that NP voltage is in a balanced state if k is 0.5. Otherwise, active capacitor voltage balancing control must be activated to realize NP voltage convergence. By re-allocating the proportion of small vectors, the NP voltage imbalance problem can be effectively resolved, which is equivalent with injecting an offset value Δd in each phase duty cycle.

Due to the symmetry of subsectors 1-2, the control method for subsector 1 is taken as a case study in the following.

- If $k \in [0, 0.5)$, it means $V_{dc1} < V_{dc2}$. To maintain NP potential balance, the dwell time of [ONN] needs to be increased while the dwell time of [POO] should be dropped down.

  In Figure 6.4, phase-A is clamped between positive DC-rail and the NP, whereas phase-B and C are both clamped between the NP and negative DC-rail. Therefore, the compensated NP charge can be calculated by:

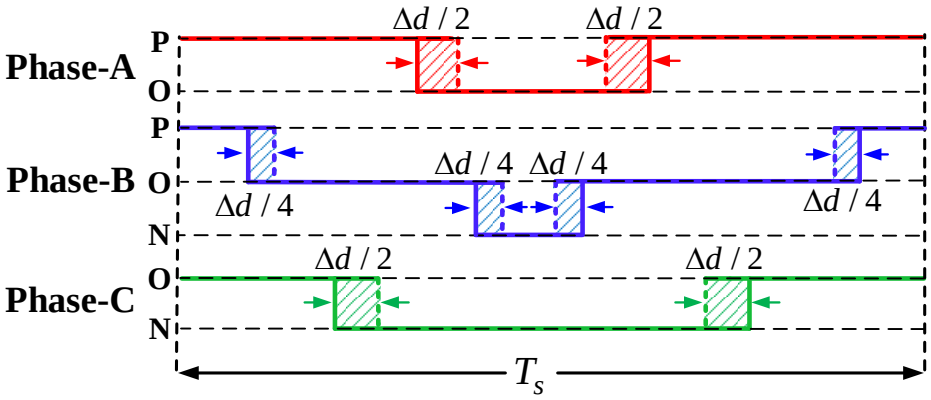


Figure 6.5: Pulse train with active capacitor voltage balancing control for subsector 3

$$\begin{aligned} C\Delta V_{dc} = -\,[&(1-g+\Delta d_I)i_a + (1-g-\Delta d_I)i_b \\ &+ (1-g-2h-\Delta d_I)i_c]T_s \end{aligned} \tag{6.8}$$

where Δd_I represents the duty cycle offset and T_s is a switching cycle.

And then, Δd_I can be derived as:

$$\Delta d_I = -(\frac{C\Delta V_{dc}}{2T_s i_a} + \frac{i_c}{i_a}h) \tag{6.9}$$

- If $k\in[0.5,\ 1]$, it means $V_{dc1}>V_{dc2}$. Hence, the dwell time of [ONN] needs to be decreased to balance the shifted NP potential, whereas the dwell time of [POO] should be increased, which is exactly opposite to the above situation of $k\in[0,\ 0.5)$. Thus, Δd_{II} can be expressed as:

$$\Delta d_{II} = -\Delta d_I \tag{6.10}$$

With the machine speed ramping up and modulation index deepening, generation mode is activated. Under this circumstance, subsectors 3-5 applying small vectors will be involved. Given that the symmetry of subsector 4 and 5, here, subsectors 4 is chosen as a representative example to analyse, together with subsector 3. The switching pulses associated with each subsector are shown in Figures 6.5 and 6.6, which indicates that both phase-A and C generate two consecutive voltage levels, whereas phase-B clamps to the NP and positive/negative rail of DC-link. The different cases are considered as follows:

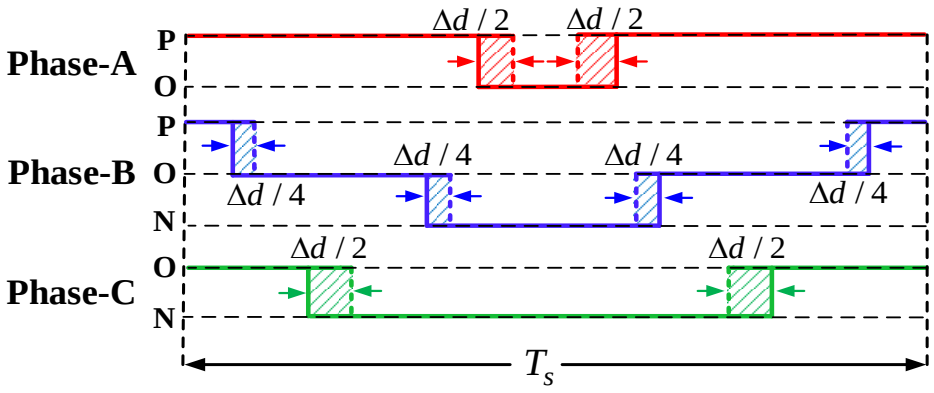


Figure 6.6: Pulse train with active capacitor voltage balancing control for subsector 4

For subsector 3:

- If $k\in[0,\ 0.5)$, it means $V_{dc1}<V_{dc2}$. Two pairs of small vectors are employed to handle the drift tendency of NP voltage. More specifically, the dwell time of [PPO] and [POO] are both longer than that of their counterparts.

  Then, the compensated NP electric charge over a switching period can be calculated as:

$$\begin{aligned} C\Delta V_{dc} = &-[(1-g-h-\Delta d_I)i_a + (1-g-h-\Delta d_I+\Delta d_I)i_b \\ &+ (1-g-h+\Delta d_I)i_c]T_s \end{aligned} \tag{6.11}$$

- If $k\in(0.5,\ 1]$, it means $V_{dc1}>V_{dc2}$. The dwell time of the P-type small vector should be dropped down, whereas that of the N-type small vector needs to be raised. Similar to equation (6.10), Δd_{II} can be expressed as:

$$\Delta d_{II} = -\Delta d_I \tag{6.12}$$

For subsector 4:

- If $k\in[0,\ 0.5)$, it means $V_{dc1}<V_{dc2}$. To keep the NP voltage balanced, the participation of small vector [POO] becomes predominant as compared to that of [ONN]. Therefore, the compensated NP charge is given by:

$$\begin{aligned} C\Delta V_{dc} = &-[(1-g-h-\Delta d_I)i_a + (1-g-h-\Delta d_I+\Delta d_I)i_b \\ &+ (1-g-h+\Delta d_I)i_c]T_s \end{aligned} \tag{6.13}$$

Further, Δd_I can be calculated as:

$$\Delta d_I = \frac{C\Delta V_{dc}}{2T_s(i_a - i_c)} \tag{6.14}$$

- If $k \in [0.5, 1]$, it means $V_{dc1} > V_{dc2}$. The dwell time of [POO] needs to be declined to raise the NP potential. At the same time, the interval of [ONN] becomes larger. Consequently, Δd_{II} can be obtained:

$$\Delta d_{II} = -\Delta d_I \tag{6.15}$$

  Because of the unavailability of small vectors in subsector 6, the provided method can hardly contribute to recovering the deviated capacitor voltage to a balanced state in that region, which therefore facilitates a trade-off for suppressing CMV magnitude. In spite of that, in the case of the ESG system operating at a modulation index of 0.95, the reference voltage vector can still pass through subsectors 4-5 to maintain NP voltage balanced.

6.2.3 Delay Compensation

The above-mentioned dwell time calculation is based on the assumption that the carrier-pulse ratio is high enough. Nevertheless, when the ESG system operates at a speed of 20krpm in power generating conditions, one sampling cycle delay caused by the digital control system should not be ignored as pulse numbers in that case is only 16 over a fundamental period. In order to avoid adverse effects, a simple compensation approach [105] is adopted for the measured phase current vector i_s:

$$i_s^* = i_s \cdot e^{-j \cdot 1.5 T_s \cdot 2\pi f_o} \tag{6.16}$$

where T_s represents the sampling frequency and f_0 denotes the fundamental frequency.

Equation (6.16) indicates that the phase current vector command needs to be advanced by $1.5T_s$ before calculating required duty cycle offset. Figure 6.7 shows a flowchart of the active NP voltage balancing control algorithm in Sector-I supplemented for the proposed HBSVM strategy.

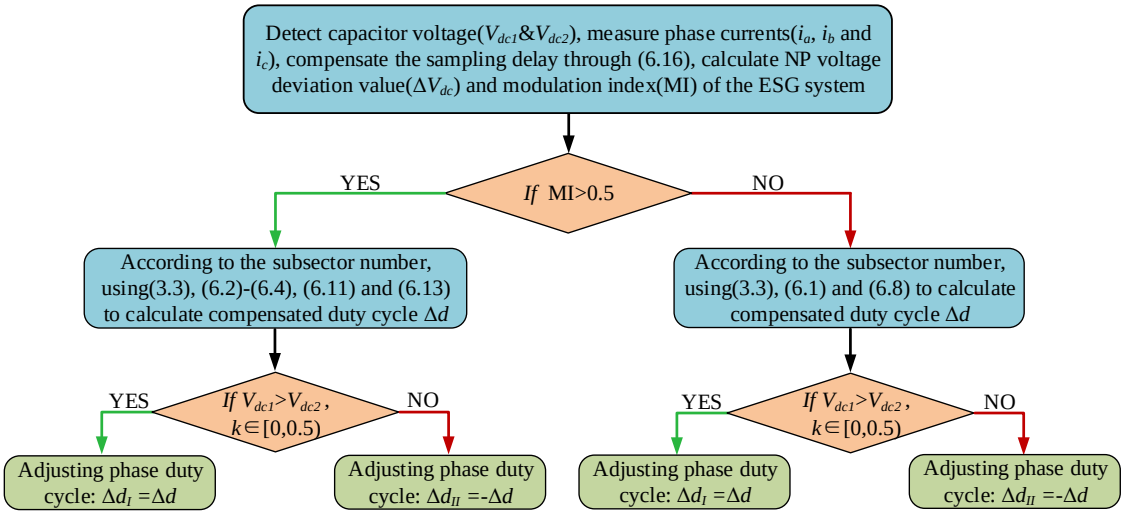


Figure 6.7: Flowchart of the NP voltage balancing control method for the proposed HBSVM strategy in Sector-I

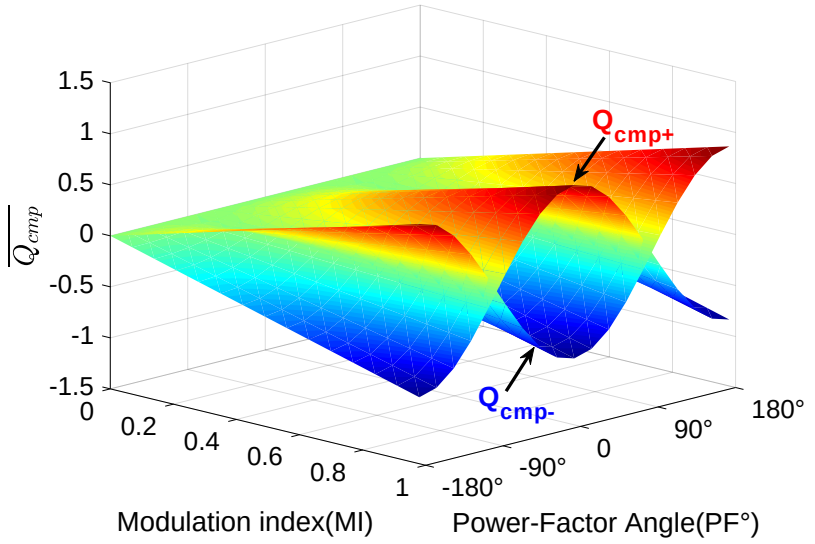


Figure 6.8: Normalized electric charge compensation under different modulation indices and power factors

6.2.4 Active NP Voltage Balancing Control Performance

From equations (6.8), (6.11) and (6.13), it can be seen that the compensation capability is determined by manipulated phase duty cycles and associated NP currents, which vary with different modulation indices and power factors. Here, the average compensated NP electric charge ($\overline{Q}_{cmp}$) over a fundamental cycle is adopted to

evaluate this performance, as expressed by:

$$\overline{Q_{cmp}} = \frac{1}{2\pi} \int_{t=0}^{t=2\pi} Q_{cmp}(\omega t) \cdot dt \tag{6.17}$$

With equation (6.17), the compensated electric charge is plotted in Figure 6.8. As shown, Q_{cmp+} and Q_{cmp-} can be generated to correct unbalanced NP voltage. Besides, the amount increases along with the deepening modulation index. Although the maximum compensation is achieved under the unity power factor condition, the state of NP potential can be effectively kept balanced during the entire operating points of the ESG system.

6.3 Simulation Results

The simulated ESG system is built in the Simulink/PLECS environment and selected parameters have been listed in Table 5.4. In order to demonstrate the modulation performance of the proposed HBSVM strategy, i.e., NP voltage balance, CMV and power loss, the conventional NTV and NTV^2 schemes are chosen as the benchmark method. The operating conditions with two modulation indices and power factors are carried out in the simulations, which correspond to the startup process and power generation mode, respectively.

6.3.1 Capacitor Voltage Balancing Capability

As shown in Figure 6.9, two capacitor voltages shifted from 135V can be effectively balanced with the presented modulation strategy in starter mode. Less distortion in line-to-line voltage further indicates good performance in the lower modulation index region.

The simulation results from Figure 6.10 show that the drifted NP voltage can be kept balanced again in generation mode. Furthermore, the undesirable low-frequency capacitor voltage oscillation has been greatly mitigated even under the operating condition of modulation index of 0.95 and power factor of 0.2.

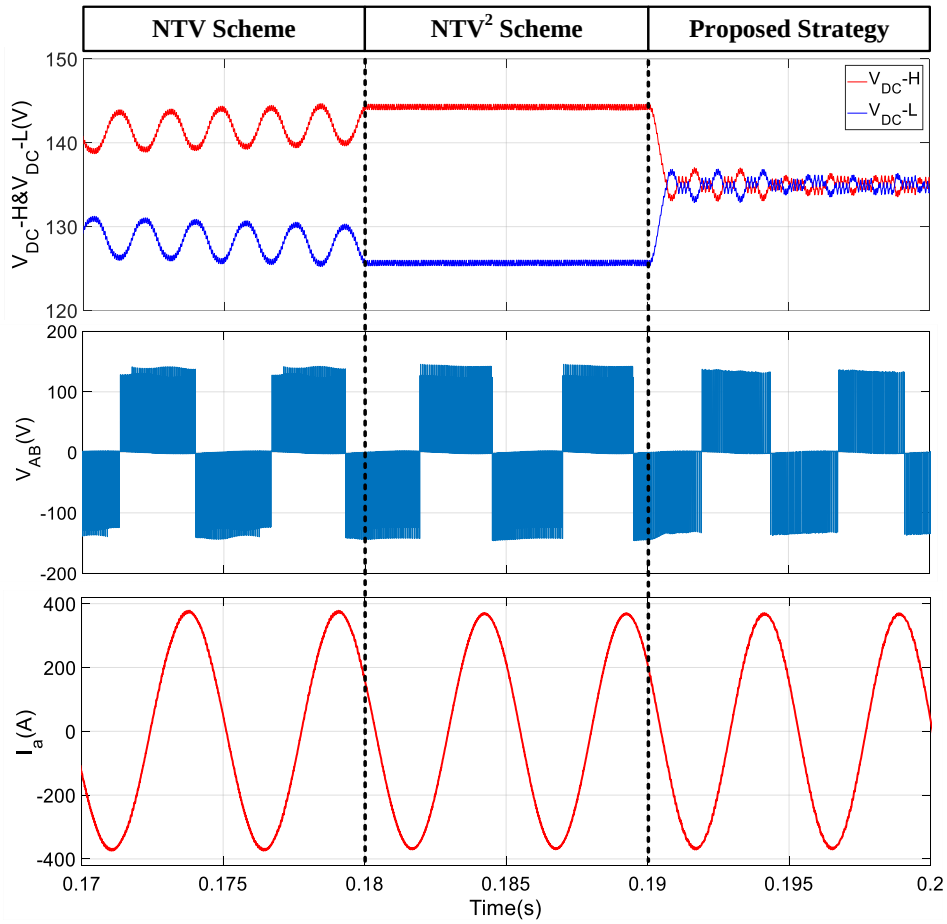


Figure 6.9: Simulation results in starter mode (MI=0.5 and PF=0.7)

6.3.2 CMV Suppression Performance

The CMV in the ESG system during the power generation mode is shown in Figure 6.11. It can be seen that the main components of the CMV produced by the NTV and NTV^2 schemes are $\pm V_{dc}/3$. In this regard, however, the proposed modulation strategy reduces that amount to $\pm V_{dc}/6$.

6.3.3 Power Losses Analysis

The conduction loss depends on the magnitude of phase current flowing through semiconductor devices. That value is normally the same for the aforesaid modulation strategies under the designed power rating. By contrast, the switching loss is related to switching actions during a switching period. It can be clearly seen that the

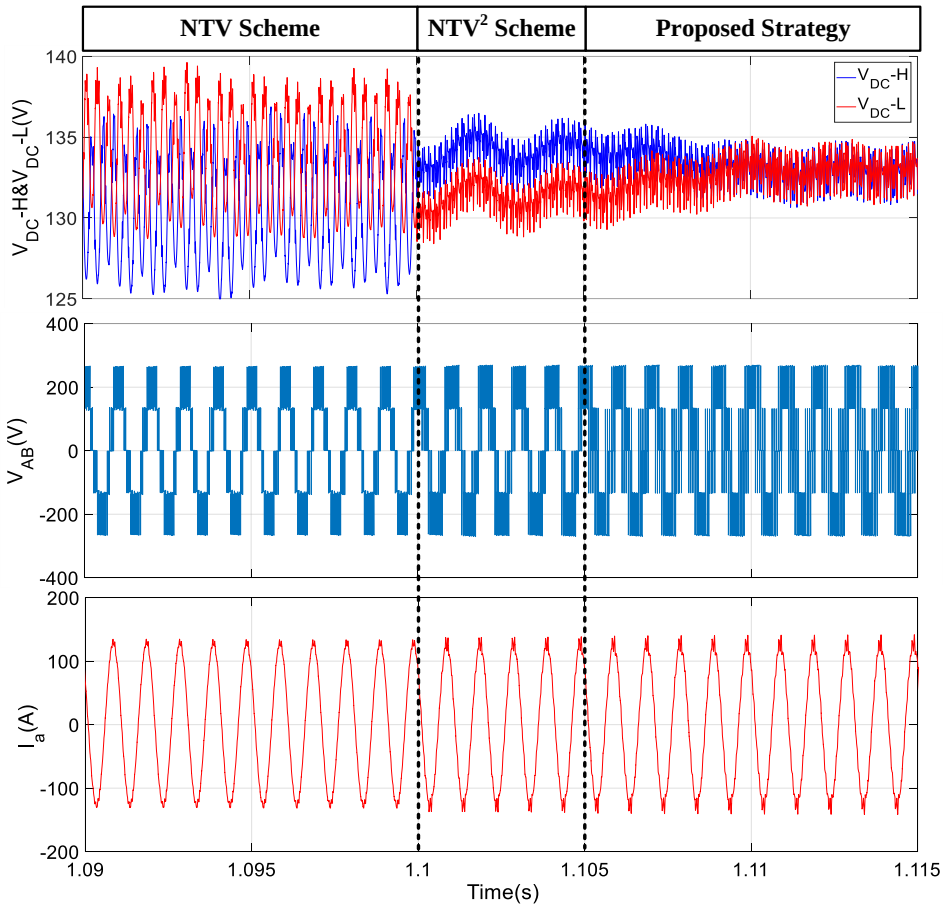


Figure 6.10: Simulation results in generation mode (MI=0.95 and PF=0.2)

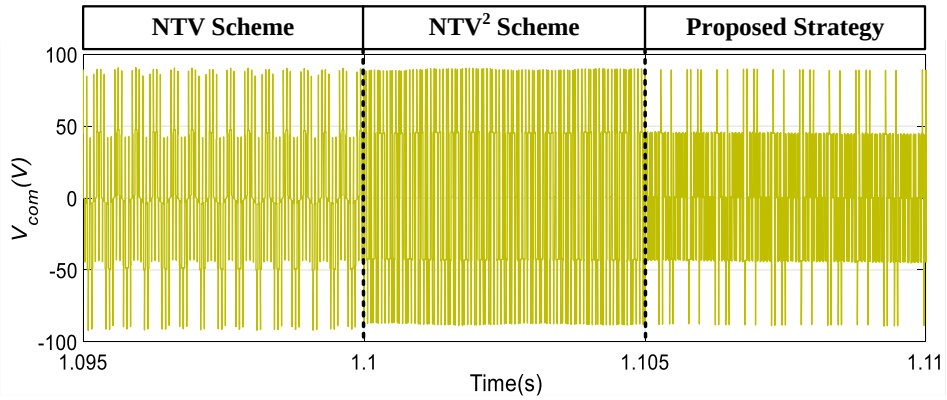


Figure 6.11: CMV generated by the NTV, NTV^2 scheme and the proposed HBSVM strategy in the ESG system

NTV scheme exhibits six switching actions, whereas both the NTV^2 scheme and the HBSVM strategy feature three-level switching intervals in a phase leg, which causes extra two switching actions. The switching frequency is set at 16kHz, DC-link volt-

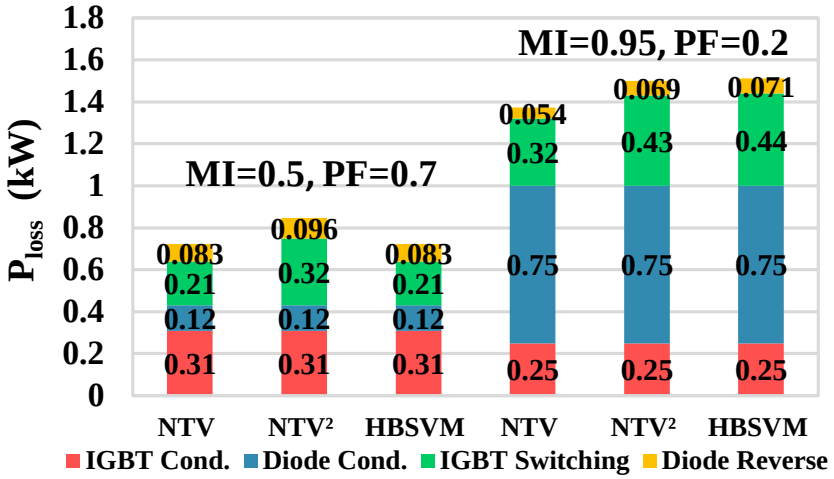


Figure 6.12: Comparison of power losses distribution under the conventional NTV, NTV^2 scheme and the proposed HBSVM strategy for two operating modes

age is 270VDC and power rating is 45kW. Using the data from the manufacturer's datasheet, power loss can be attained through the PLECS simulation tools.

Figure 6.12 shows the comparison of power loss breakdown based on the NTV, NTV^2 scheme, and the proposed HBSVM scheme at modulation indices of 0.5 and 0.95 under power factors of 0.7 and 0.2. As seen from Figure 6.12, the amount of losses by the presented technique are the same as that of the NTV scheme in the startup process. It is also notable that the proposed strategy features three-level output voltages in one phase leg. Hence, the results show a similar loss distribution with the NTV^2 scheme in the steady-state. Besides, it can conclude that total losses in generation mode are higher than the amount in motoring mode.

6.3.4 Comparison with Other Hybrid Modulation Strategies for Three-Level NPC Converters

Compared with other hybrid modulation strategies for 3L-NPC converters, the proposed technique brings the following attractive features:

1) Unlike [155] and [156], with the help of algebraic functions, the duty cycle determination process is simplified to avoid the heavy computational burden.

2) By adjusting duty cycle in each phase, capacitor voltage balancing control

under initial NP voltage imbalance, which is not discussed in [158], can be thus realized. Moreover, the NP voltage drift is easily resolved instead of calculating complex analytical solutions of NP currents [159].

3) Since the switching states are optimally selected, CMVs generated by the proposed scheme can be significantly suppressed in the steady-state. However, the main component of that value is at least doubled by the existing hybrid modulation schemes in [154–159].

4) Although the switching actions are increased as compared to that amount in [154], [157] and [160], the NP voltage ripple in generation mode can be validly eliminated by this work.

6.4 Experimental Validation

In this section, the proposed modulation technique is experimentally validated by our developed aircraft ESG system test rig, as shown in Figure 5.20. The experimentation also primarily focuses on the ESG system operating in a light-load condition. The experimental results by the NTV, NTV^2 schemes and the proposed HBSVM strategy are all performed in the period of motoring and generating mode. A shaft speed of 8krpm, a modulation index of 0.5 and a power factor of 0.7 are chosen as a representative operating point for the former case, whereas the latter operating point refers to a machine speed of 20krpm, a modulation index of 0.95 and a power factor of 0.2.

6.4.1 Steady-State Experiments

In the case of a shaft speed of 8krpm, two capacitor voltages (V_{DC-H}/V_{DC-L}), phase current and line-to-line voltage are shown in Figure 6.13(a). While experimental results in power generation mode are shown in Figure 6.13(b). As shown, capacitor bank voltages can be well balanced for the above operating conditions. Furthermore, it can be seen that switching pulses become fewer because of lower pulse ratios at

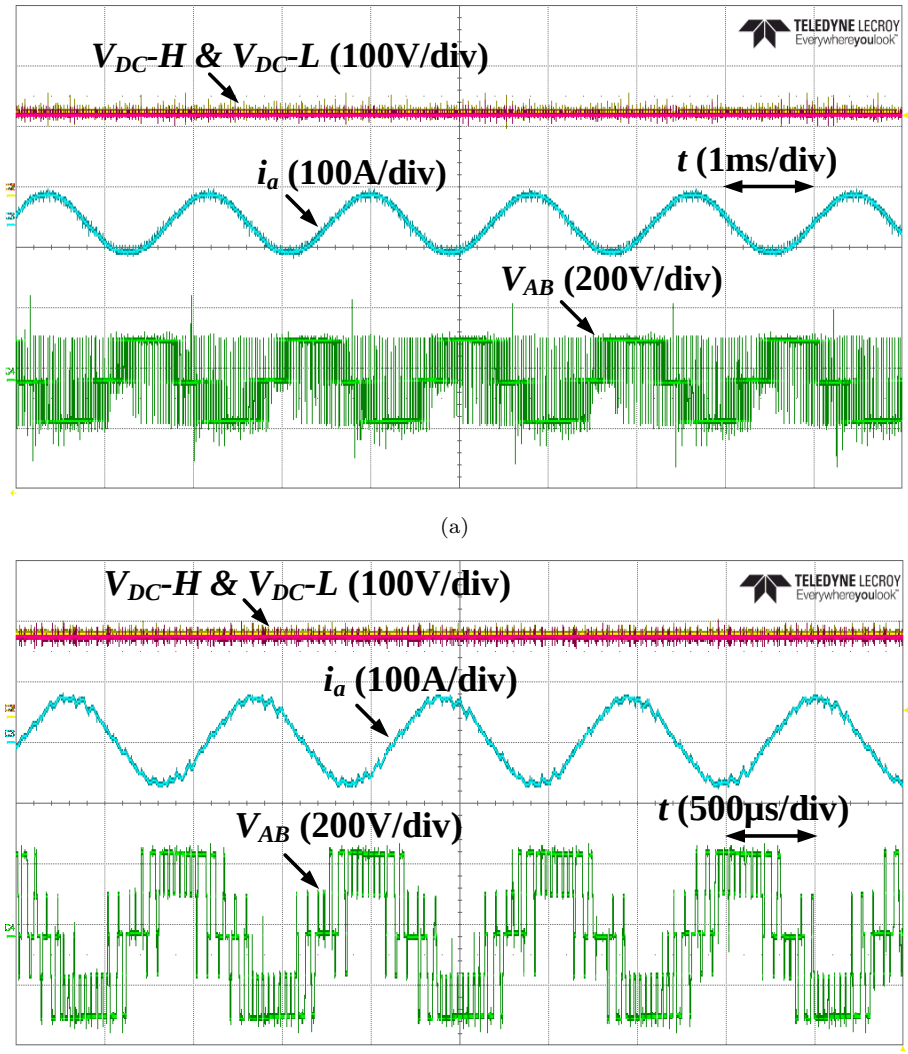


Figure 6.13: The experimental results under: (a) the startup process (MI=0.5, PF=0.7) and (b) the generation mode (MI=0.95, PF=0.2)

the high-speed operation.

6.4.2 Dynamic-State Experiments

In order to evaluate the dynamic-state performance of the proposed modulation strategy, the load and speed-change conditions are considered. Figure 6.14(a) shows the converter output variables when the i_q reference command increases from 5A to 25A, while Figure 6.14(b) shows the experimental results when the rotation speed ramps up from 18krpm to 20krpm. The above experimentation regarding NP voltage

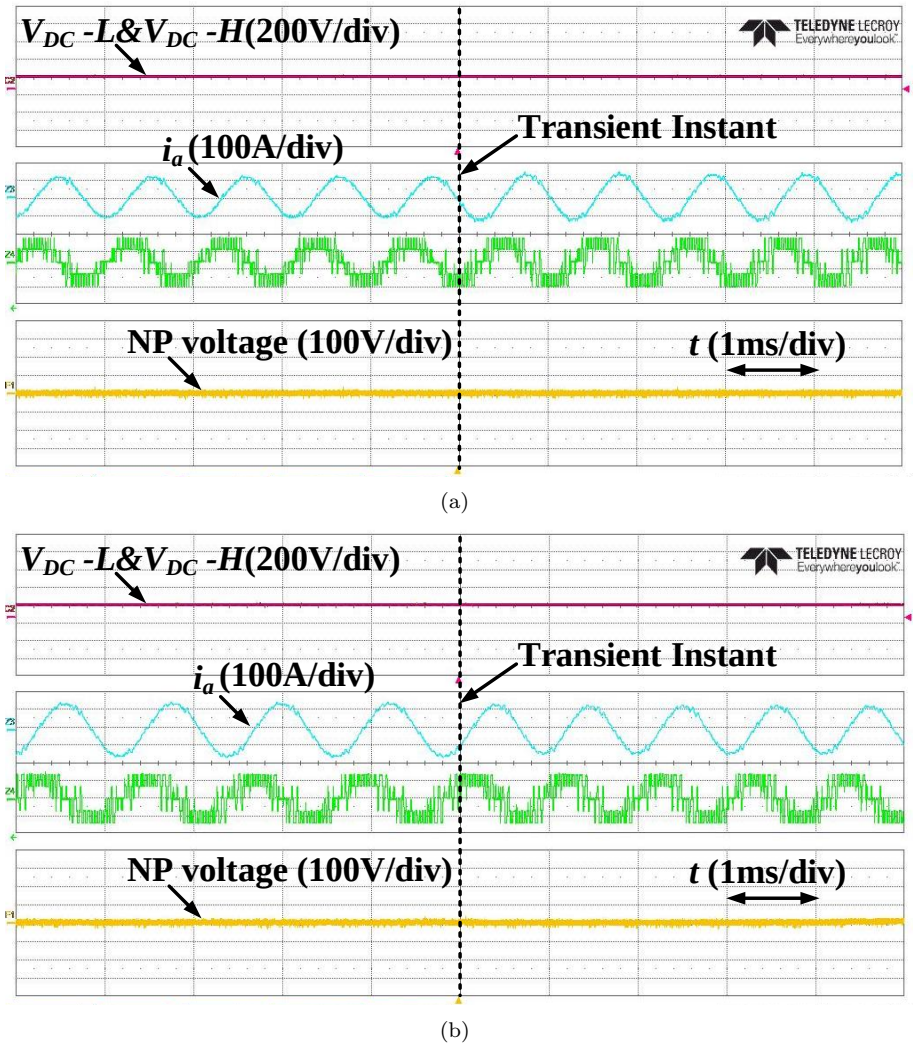


Figure 6.14: Dynamic-state performance under (a) loading condition and (b) speed-changing condition

balance and smooth transition period of phase current/voltage verify a superior dynamic performance of the proposed HBSVM technique.

6.4.3 CMV Reduction Performance

To validate the CMV suppression performance for the high-speed drive systems, the comparison experiments are carried out among the NTV, NTV^2 schemes and the proposed strategy during power generating conditions. As shown in Figure 6.15(a), the main component of CMVs produced by the proposed HBSVM technique is much lower than for the NTV scheme. Similarly, the CMV composed of a series of $\pm V_{dc}/3$

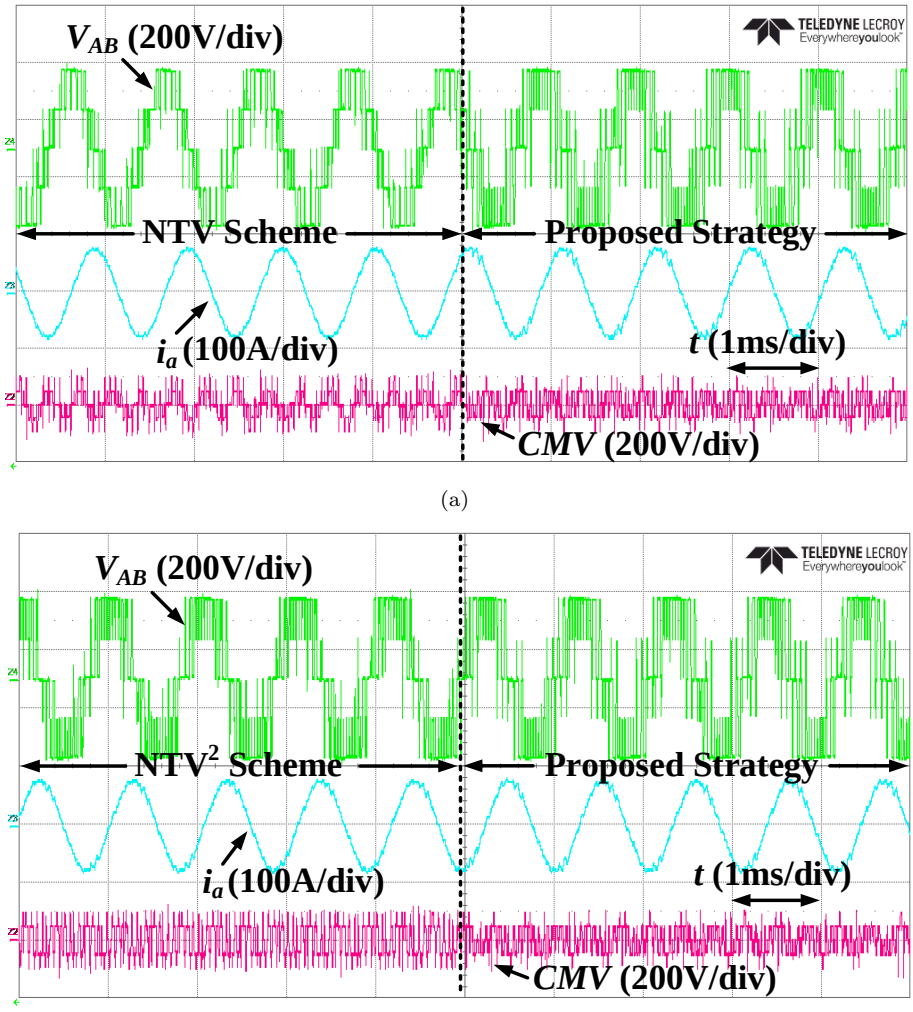


Figure 6.15: CMV comparison between the proposed HBSVM scheme and (a) the NTV scheme and (b) the NTV^2 scheme

is significantly reduced when the NTV^2 scheme is switched to the proposed HBSVM method, as shown in Figure 6.15(b).

6.4.4 Capacitor Voltage Balancing Performance

Considering that capacitor voltage is required to be actively balanced in full-speed range operation. Firstly, the proposed HBSVM is demonstrated in motoring mode, in which a shifted NP voltage of 70V initially exists under the conventional NTV scheme, as shown in Figure 6.16(a). It can be seen that the line-to-line voltage is distorted because of the capacitor voltage imbalance problem. Nevertheless, the

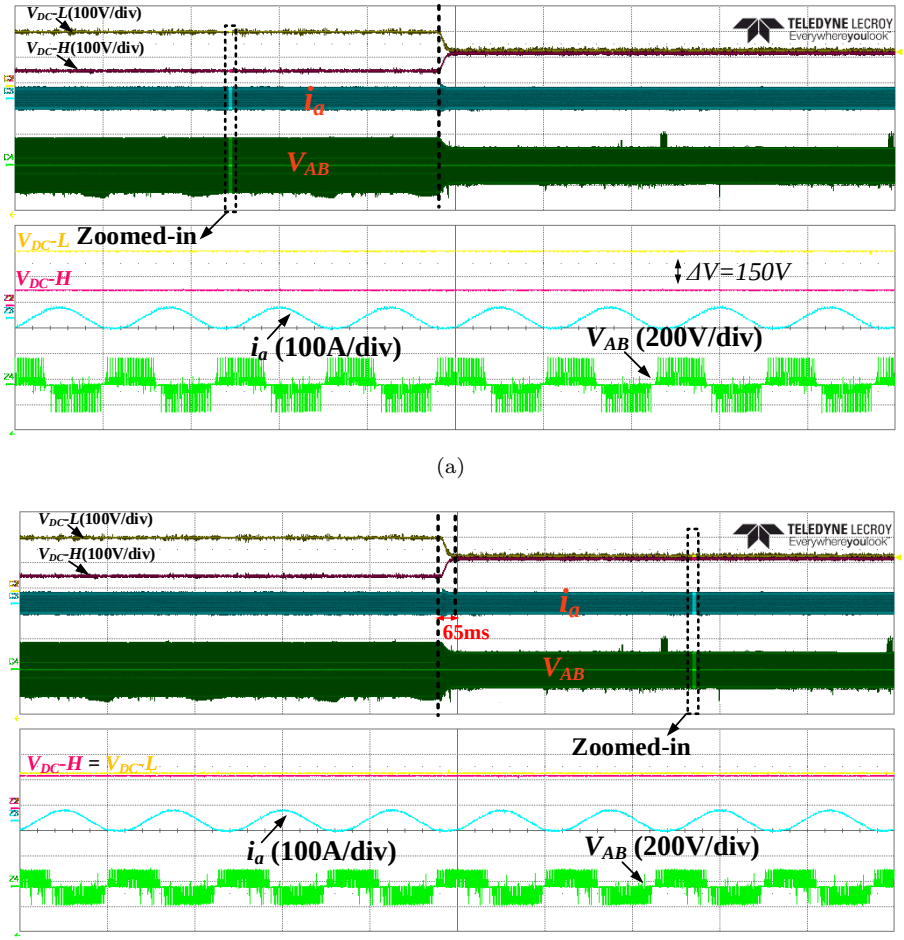
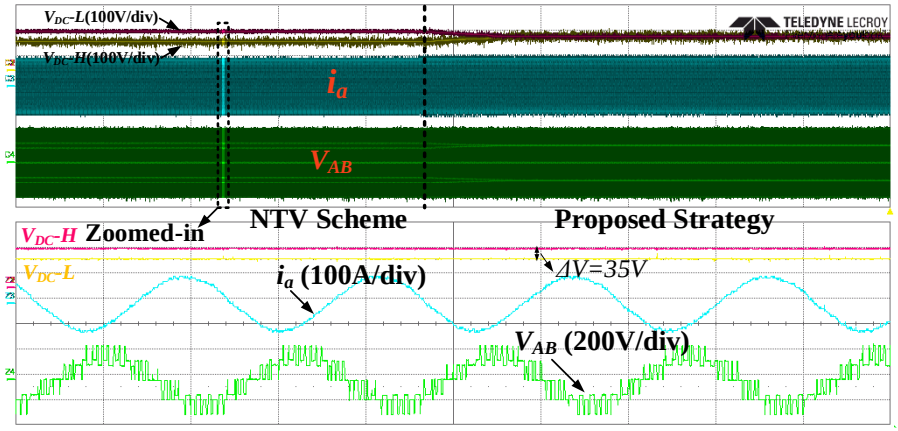


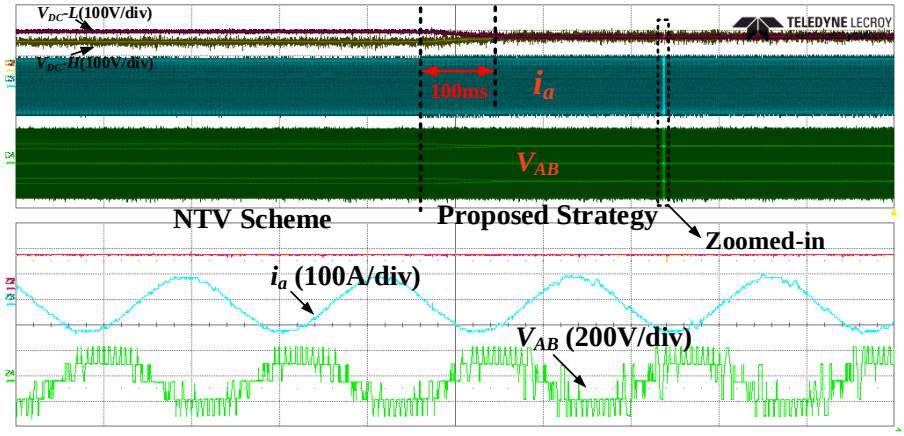
Figure 6.16: Capacitor voltage balancing performance during motoring mode (MI=0.5, PF=0.7) under (a) the NTV scheme and (b) the proposed HBSVM scheme

zoomed-in waveform shown in Figure 6.16(b) validates the NP capacitor voltage can be kept balanced again within $65ms$.When running the machine at a speed of 20krpm, two capacitor voltages are hard to be converged by the NTV scheme under the conditions of a modulation index of 0.95 and a power factor of 0.2, as shown in Figure 6.17(a). In order to evaluate the NP voltage recovery performance, the proposed approach is tested under that condition as well. As shown in Figure 6.17(b), a DC voltage bias of 35V between two capacitors can be quickly maintained balanced again within $100ms$ after deploying the proposed HBSVM strategy.

A similar experimentation with the NTV^2 scheme is conducted under an initial capacitor voltage imbalance. As seen from zoomed-in waveforms in Figure 6.18(a),



(a)



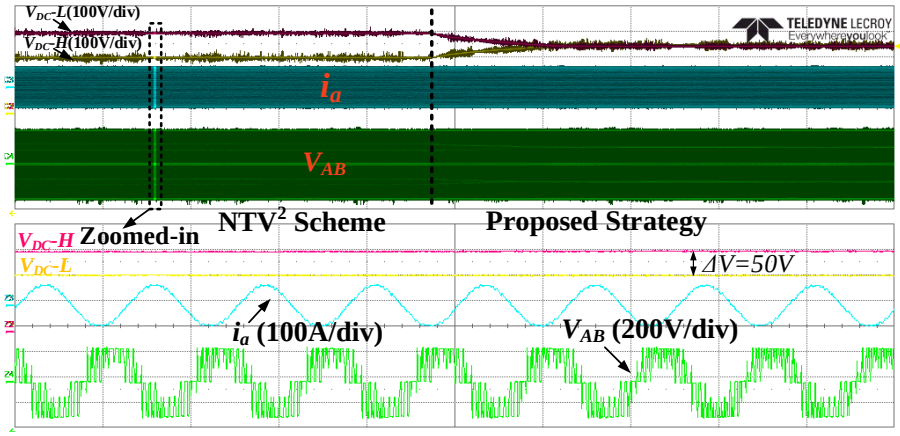
(b)

Figure 6.17: Capacitor voltage balancing performance during generation mode (MI=0.95, PF=0.2) under (a) the NTV scheme (b) the proposed HBSVM scheme

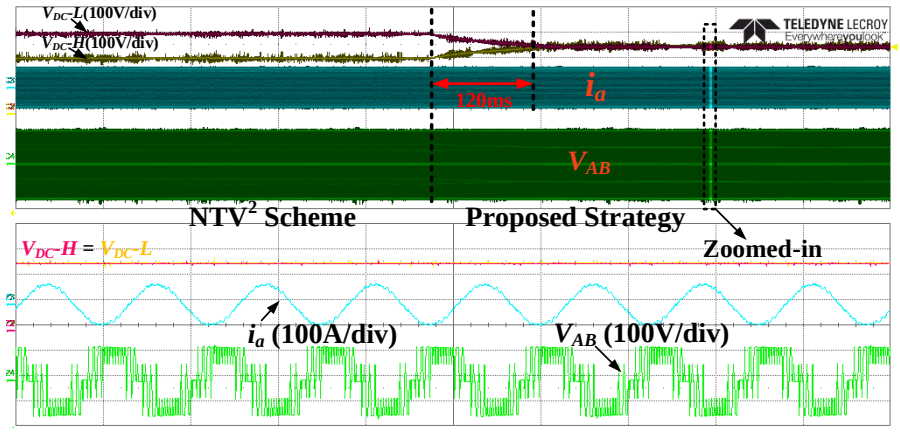
the original NTV^2 scheme is not capable of keeping capacitor voltage at a balanced state. As a result, an NP potential imbalance of 50V exists before switching to the proposed method. By contrast, output phase voltage can be constantly clamped at three levels, the drifted NP voltage can be corrected and distorted phase current problem can be addressed properly when the proposed hybrid modulation technique is applied within $120ms$, as shown in Figure 6.18(b).

6.4.5 Distortion Analysis

Figures 6.19-6.21 present the harmonic spectra of the line-to-line voltage when using the NTV, NTV^2 schemes and the proposed HBSVM approach under the aforemen-



(a)

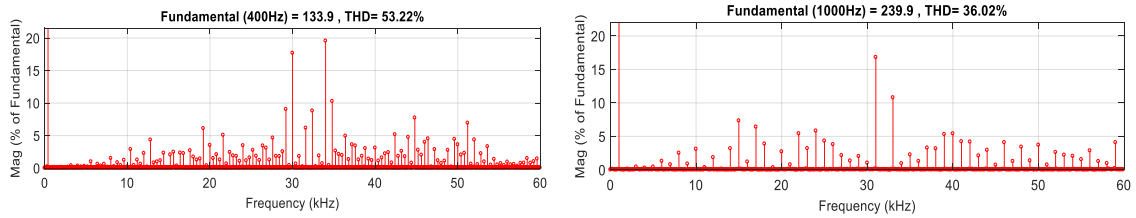


(b)

Figure 6.18: Capacitor voltage balancing performance during generation mode (MI=0.95, PF=0.2) under (a) the NTV^2 scheme and (b) the proposed HBSVM scheme

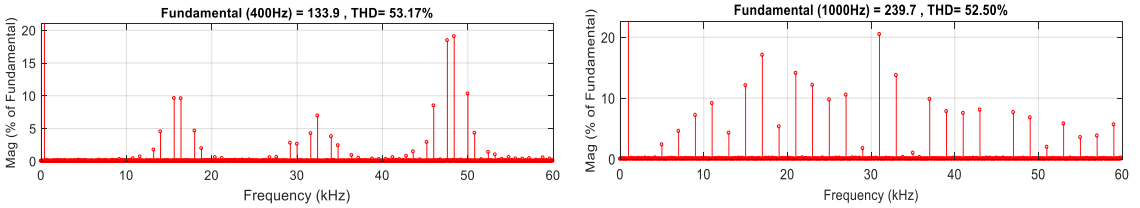
tioned operating conditions. It can be seen that, for the startup process, the THD by these three modulation methods is similar. The main difference is that the harmonic contents for the NTV scheme and the presented strategy are more wide presence than that for the NTV^2 scheme. In power generation mode, the THD by the HB-SVM strategy is higher than the other two counterparts. This is because the nearest space vectors are not applied by the proposed algorithm during the steady-state. In addition, the presence of harmonic contents for the NTV^2 and the proposed HBSVM schemes is wider than that amount for the NTV scheme which always exhibits the lowest THD in both operational modes.

Figure 6.22 presents the WTHD comparison of the line-to-line voltage under



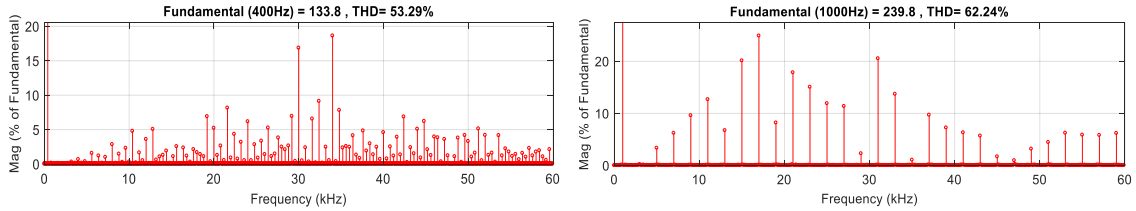
(a) (b)

Figure 6.19: Harmonic spectra of the line-to-line voltage by the NTV scheme at: (a) MI=0.5, PF=0.7 and (b) MI=0.95, PF=0.2



(a) (b)

Figure 6.20: Harmonic spectra of the line-to-line voltage by the NTV^2 scheme at: (a) MI=0.5, PF=0.7 and (b) MI=0.95, PF=0.2



(a) (b)

Figure 6.21: Harmonic spectra of the line-to-line voltage by the proposed HBSVM scheme at: (a) MI=0.5, PF=0.7 and (b) MI=0.95, PF=0.2

the NTV, NTV^2 and the proposed modulation techniques at different modulation indices. It can be seen that the WTHD by the proposed strategy is overlapped with that of the NTV scheme if the modulation index is lower than 0.5, whereas that value produced by the NTV^2 scheme is higher at this stage. After that, the distortion of the presented strategy increases due to more three-level intervals. Thus, it renders that the WTHD by the HBSVM method in the high output voltage region is higher than that by the conventional modulation counterparts.

Since near unity modulation index and power factor around zero aggravate NP voltage fluctuation, as plotted in Figure 6.1, the harmonic content of the resultant NP voltage in Figure 6.17 is analysed by the FFT when employing the traditional NTV method and the proposed HBSVM scheme in generation mode. It is evident

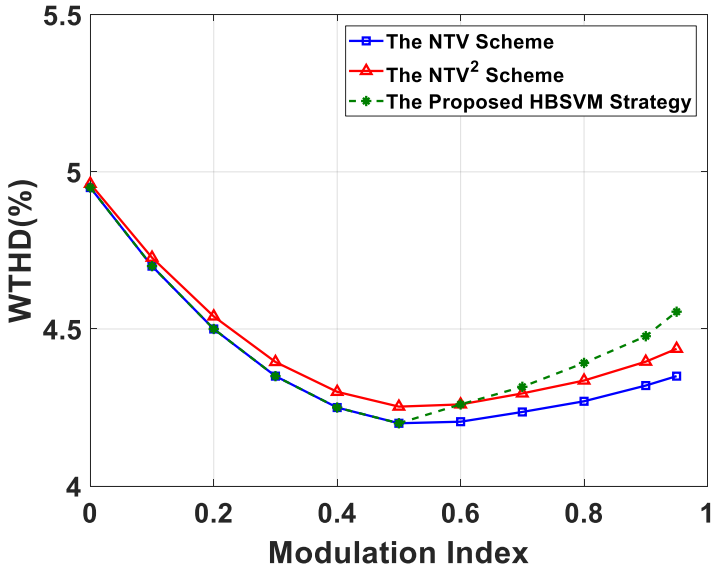
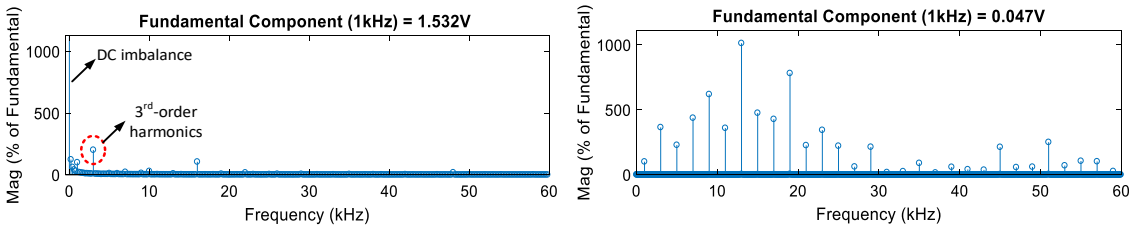


Figure 6.22: WTHD of the line-to-line voltage under the NTV, NTV^2 and the proposed HBSVM schemes at different modulation indices



(a) (b)

Figure 6.23: FFT analysis of NP voltage fluctuation under (a) the NTV scheme and (b) the proposed HBSVM scheme

from the results that not only can the imbalance issue be resolved by the proposed PWM strategy but also the low-frequency NP voltage ripple has been effectively eliminated, particularly for 3^{rd}-order harmonics, as shown in Figure 6.23.

6.4.6 Computational Performance

In order to evaluate the computational performance of the presented approach, the execution time is tested by the digital control platform. The results show that the execution time of the proposed algorithm costs about 56.8μs. Compared with the time taken by trignometric opertations in the α-β reference frame, i.e., 66.5μs, the computational burden has been approximately reduced by 17%.

6.5 Conclusions

In this Chapter, a new HBSVM technique has been proposed for the 3L-NPC converter, which aims to improve the modulation performance, especially for the wide-speed operation of the aircraft ESG system.

Considering the operating points of the target systems, the NTV scheme is initially employed in the startup process as the balanced NP voltage can be easily obtained, and switching actions are fewer as compared to the original NTV^2 scheme. If the power generation mode activates, an advanced NTV^2-based modulation strategy is deployed. Not only can this method be capable of mitigating low-frequency NP voltage ripple but also the high magnitude of CMVs in the converter-fed PMSM drives are suppressed significantly. Furthermore, with the help of the phase duty cycle offset, the provided technique enables to gain active DC-link capacitor voltage balancing control capability even though the NP voltage drifts away under high modulation index and low power factor conditions. The fast calculation approach is also established in this work to improve algorithmic efficiency for the used microcontroller. At last, the results obtained from the simulation and experimental prototype validated the correctness and effectiveness of the proposed hybrid modulation strategy.

Chapter 7

DC-Link Voltage Utilization Ratio Improvement Technique for Three-Level NPC Converter

This Chapter presents a PWM algorithm based on virtual-space-vectors (VSVs) for the 3L-NPC converter in our studied high-speed aerospace motor drives. The proposed technique aims to boost the DC-link voltage utilization ratio, which brings an opportunity for the operation of aircraft ESG systems easily extending from the linear modulation range into the overmodulation region. Moreover, the algorithm is capable of balancing initial DC-link capacitor voltage deviation. The fast PWM calculation approach is established in this work for the purpose of higher computational efficiency in the digital controller.

7.1 Introduction

In order to improve DC-link voltage utilization for AC/DC or DC/AC power converters, the overmodulation conditions have motivated researchers to develop dedicated PWM algorithms for two-level [161–168] and diode-clamped multilevel converters [121, 169–175]. For the basic two-level topology, according to the required

reference space vector track, a continuous PWM control scheme has been studied in [161]. This method consists of two modes until it transits to the six-step operation. A novel overmodulation strategy is reported in [162] by defining a holding angle and a reference voltage vector angle. Therefore, the desired modulation index can be precisely regulated based on the Fourier series expansion. The authors of [163] consider the accuracy and computational effort of a classification algorithm in the overmodulation region. For high-power motor drive applications, a DC-link clamping synchronized PWM strategy incorporated with an overmodulation scheme is presented in [164], which can raise the output voltage and reduce switching losses. In [165], an improved discontinuous SVM scheme incorporates overmodulation conditions with a pulse-dropping technique. In [166], an overmodulation scheme with the phase current reconstruction is presented for the PMSM drives. An optimized PWM strategy is explored in [167] for minimum harmonics under overmodulation conditions, particularly for two-level inverter fed high-speed motor drive systems with a low-carrier ratio. In [168], the output torque performance is analysed under the six-mode operation for induction motor (IM) drives.

The existing literature about the overmodulation strategy for the NPC topology is discussed in the following. In [121], the authors propose an overmodulation method by calculating three-phase modulation waves, which is beneficial for simple implementation in digital controllers. For the high-power applications with a low pulse-ratio, a synchronized SVM strategy [169] is proposed to operate IM drives in the overmodulation region. In order to avoid trigonometric operations, a duty cycle-based overmodulation strategy is presented in [170], together with a dedicated NP voltage balancing control method. In [171], a timing-correction based algorithm is investigated to gain the output voltage under overmodulation conditions. Also, the approach is implemented in a field-programmable-gate-array (FPGA)-based real-time control platform to attain the minimum computational resources. With the help of the neural-network, a classification SVM technique [172] for the overmodulation region has been studied for 3L-NPC converters, which ensures a smooth linear transition and lower complexity. It is noted that the authors employ

the NTV scheme and predefine a series of switching sequences to maintain two capacitor voltages balanced. With respect to low power factor loads, however, the aforementioned methods pose a challenge for capacitor voltage balance, as well as eliminating low-frequency NP potential oscillation. To address these deficiencies, a hybrid SVM strategy is introduced in [173] to operate a 3L-NPC inverter in the overmodulation region. This approach abandons medium vectors to mitigate voltage fluctuation in the NP, but non-nearest-three-vectors may result in phase current distortion within the higher output voltage range. In [174], a CBPWM scheme for the 3L-NPC inverter-fed IM drives with dynamic loads has been discussed to extend the operating point into the overmodulation region. Besides, the technique is capable of keeping two capacitor voltage in a balanced state when NP potential deviation occurs. It is worth noting that calculating appropriate zero-sequence voltage components are required. The work reported in [175] discusses a novel overmodulation scheme that achieves balanced capacitor voltages and alleviated low-frequency NP potential oscillation over the entire range of modulation indices and power factors, even for n-level NPC topologies. Although the performance is desirable by applying VSVs, keeping capacitor voltage balanced is not discussed if NP voltage shifts. In addition, the presented hexagonal compression limit may impair overmodulation capability to some extent. Table 7.1 summarises the existing overmodulation techniques for the 3L-NPC converter.

In this Chapter, a new variant of the VSV-based PWM algorithm is investigated for the operation of aircraft ESG system extending into the overmodulation region. Besides, active capacitor voltage balancing control is involved in this work. Compared with the prior method presented in [175], the proposed trajectory of the reference voltage vector provides a better overmodulation capability. With the presented NP voltage balancing control strategy, the diverged capacitor voltages can be effectively controlled at a balanced condition if NP potential drifts away unexpectedly. More importantly, the g-h coordinate introduced in Chapter 4 offers a degree of freedom to connect the reference voltage vector's position with the dwell time of switching state. Therefore, the proposed overmodulation technique can be

Table 7.1: Overmodulation techniques for 3L-NPC converters

Exisiting methods	Characteristics
Calculating modulation waves [121]	Simple implementation
Synchronization based scheme [169]	For low pulse-ratio applications
Duty-cycle based scheme [170]	No trigonometric operations
Time-correction based scheme [171]	For FPGA-based control platform
Neural-network based scheme [172]	Smooth linear transition and lower complexity
Hybrid SVM based scheme [173]	NP voltage ripple mitigation
CBPWM based scheme [174]	Appropriate zero-sequence needed
Virtual-space-vector based scheme [175]	Balanced NP voltage for all loads

implemented with high computational efficiency for the applied microcontrollers.

7.2 Overmodulation Principle

The modulation index is evaluated by the magnitude of converter's fundamental output voltage and DC-link voltage. The definition is given by:

$$m = \frac{|V_{ref}|}{V_{dc}/\sqrt{3}} \tag{7.1}$$

According to the range of equation (7.1), the operating regions of a given converter can be divided into three parts:

1. Linear modulation (LM)
2. Overmodulation mode-I (OM-I)
3. Overmodulation mode-II (OM-II)

In the LM region, the reference voltage vector traces a circular trajectory inside the hexagon. Accordingly, the modulation index ($0 \leq m \leq 1$) arises with increasing magnitude of output voltage until the trajectory is inscribed in the hexagon side.

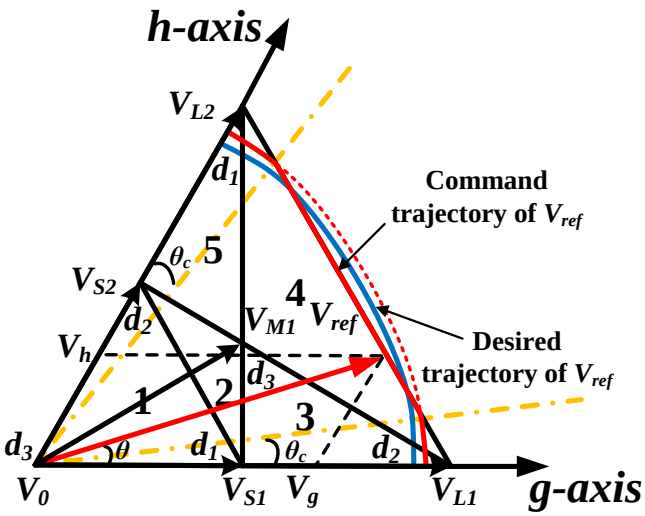


Figure 7.1: VSV-based PWM scheme for operating OM-I in Sector-I

Within linear range, the duty cycle for each space vector can be calculated by equations (4.4) and (4.5). The OM-I denotes the radius of desired reference voltage vector is between the inscribed circle and circumscribed circle of the hexagon, which indicates a higher achievable modulation index ($1 < m \leq 1.05$). In this mode, the trace of modified reference space vector transits from a circular trajectory and moves along the hexagon side when it exceeds the boundary of hexagon. As a result, a crossover angle (θ_c) that keeps the trajectory inside half of sextant needs to be controlled for obtaining adequate modulation depth, as shown in Figure 7.1. In order to further increase modulation index, the reference voltage vector is fixed at the vertex for a period of time, and then jumps to straight line of the hexagon by a holding angle (θ_h). When θ_h equals 30°, the discrete six-step mode operates, which constrains the maximum modulation index (m_{max}) of the OM-II at 1.1 [161].

Since the output variables of a converter steeply deteriorate in the OM-II [162, 168, 176], the acoustic noise and torque ripple issues are much severe, which is not suitable for the applications of high-speed aerospace motor drives. For this consideration, the scope of this study primarily focuses on the operation of OM-I, which provides a chance to achieve higher DC-link voltage utilization, enhance output torque capability, and reduce large-required flux-weakening current for the

target system. For the purpose of simplifying calculation process, the proposed VSV-based overmodulation algorithm is carried out in a transformed reference frame. The detailed descriptions of each subsection are given in the following.

7.3 The Inscribed Polygonal-Boundary Compression Technique

As mentioned above, before tracking circular trajectory in linear range again, the reference voltage vector command is programmed to coincide with the hexagon side for the purpose of a higher fundamental component in output voltage. As seen from Figure 7.1, with the geometric relationships of VSV-based SVM scheme, the following equations are given:

$$\begin{cases} \dfrac{|V_{ref}|_{p.u}}{\sin 120^\circ} = \dfrac{g}{\sin(60^\circ - \theta)} = \dfrac{h}{\sin\theta} \\ \dfrac{1}{\sin(120^\circ - \theta)} = \dfrac{|V_{ref}|_{p.u}}{\sin 60^\circ} \end{cases} \tag{7.2}$$

To approximate the red straight-line in Figure 7.1, the duty cycle of each VSV can be easily calculated using Table 4.7 and equation (7.2):

$$\begin{cases} d_1 = \dfrac{2\sin\theta}{\sin(2\pi/3 - \theta)} + \dfrac{\sin(\pi/3 - \theta)}{\sin(2\pi/3 - \theta)} - 1 \\ d_2 = \dfrac{2\sin(\pi/3 - \theta)}{\sin(2\pi/3 - \theta)} + \dfrac{\sin\theta}{\sin(2\pi/3 - \theta)} - 1 \\ d_3 = [3(1 - \dfrac{\sin(\pi/3 - \theta)}{\sin(2\pi/3 - \theta)} - \dfrac{\sin\theta}{\sin(2\pi/3 - \theta)})] = 0 \end{cases} \tag{7.3}$$

As seen from above equation, however, the dwell time of virtual medium vector ($d_3 T_s$) constantly equals zero. It means that only large vectors are used, which therefore violates the three-level operation of the converter. This phenomenon not only lowers the performance of the ESG system but also incurs a steady-state capacitor voltage error if an initial NP potential imbalance has already existed.

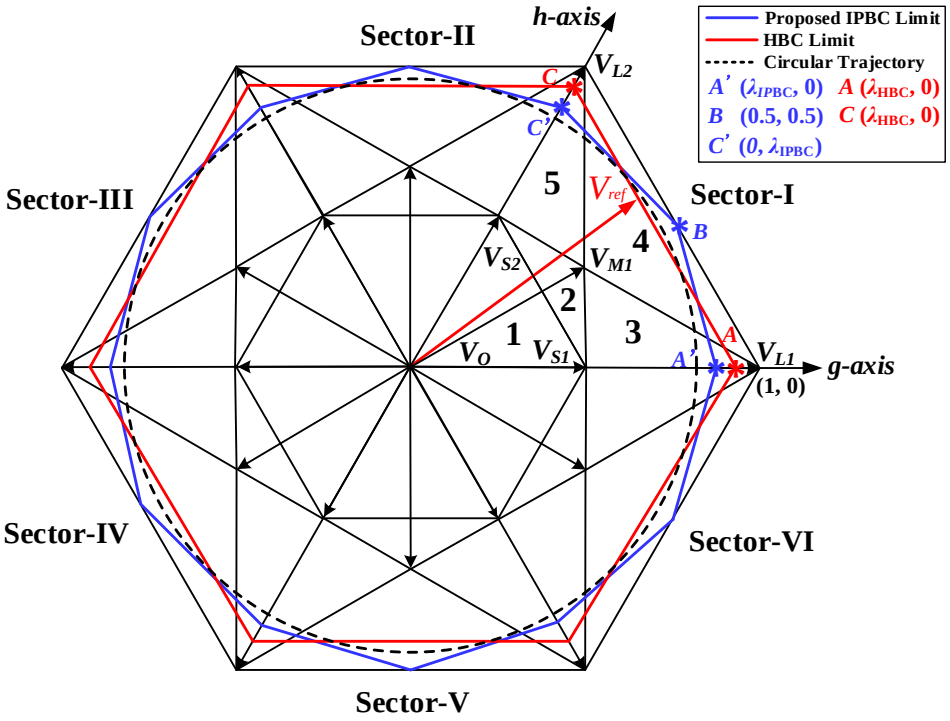


Figure 7.2: Space vector diagram of polygonal-boundary limits for the VSV-based PWM scheme

7.3.1 Hexagonal-Boundary Compression Limit

In order to tackle the above unfavourable problem, the hexagon side was scaled down by a compression coefficient λ [174]. The space vector diagram (SVD) of the polygonal-boundary limit is shown in Figure 7.2, in which the red line displays the prior hexagonal-boundary compression (HBC) limit [174]. For the first sextant, it is defined as a straight-line passing through A(λ_{HBC},0) and C(0,λ_{HBC}).

Consequently, the method can make full use of the virtual medium vector and take its dwell time to $3(1-\lambda)$, which is derived as:

$$\begin{cases} d_1 = \dfrac{2\lambda \sin\theta}{\sin(2\pi/3-\theta)} + \dfrac{\lambda \sin(\pi/3-\theta)}{\sin(2\pi/3-\theta)} - 1 \\ d_2 = \dfrac{2\lambda \sin(\pi/3-\theta)}{\sin(2\pi/3-\theta)} + \dfrac{\lambda \sin\theta}{\sin(2\pi/3-\theta)} - 1 \\ d_3 = [3(1 - \dfrac{\lambda \sin(\pi/3-\theta)}{\sin(2\pi/3-\theta)} - \dfrac{\lambda \sin\theta}{\sin(2\pi/3-\theta)})] \\ \quad = 3(1-\lambda) \end{cases} \tag{7.4}$$

where d_1, d_2 and d_3 represent the duty cycle of V_{L2}, V_{L1} and V_{M2}, respectively. θ is the rotating angle. λ indicates the compression coefficient.

7.3.2 Proposed Inscribed Polygonal-Boundary Compression Limit

In order to fully utilize the margin of the hexagon, not only the tip of V_{ref} passes through A$'$(λ_{IPBC},0) and C$'$(0,λ_{IPBC}), but also the middle point of hexagon side is involved, as shown in Figure 7.2, which is an inscribed polygonal-boundary compression (IPBC) limit represented by a blue dodecagon and forms the basis of the proposed approach. For example, B(0.5,0.5) is a turning point for Sector-I. It is worth noting that both two boundaries gradually coincide with the hexagon side when the compression coefficient converges to 1, and output voltage eventually reaches the upper limit of the OM-I.

For a given λ, the proposed trajectory of normalized $|V_{ref}|$ over a quarter cycle is given by:

$$|V_{ref}|(\theta) = \begin{cases} \dfrac{\sigma}{\sin[\theta + \arcsin\sigma]} & 0 \le \theta < 30^\circ \\ \dfrac{\sigma}{\sin[60^\circ - \theta + \arcsin\sigma]} & 30^\circ \le \theta < 60^\circ \\ \dfrac{\sigma}{\sin[\theta - 60^\circ + \arcsin\sigma]} & 60^\circ \le \theta < 90^\circ \end{cases} \tag{7.5}$$

where $\sigma = \dfrac{\frac{\sqrt{3}}{4} \times \lambda}{\sqrt{\lambda^2 - \frac{3}{2}\lambda + \frac{3}{4}}}$ and $\theta = \omega t$ (ω is the angular fundamental frequency).

Given that the selected compression coefficient equals 0.9 (i.e., λ=0.9), the $\alpha\beta$-axis components of the proposed technique and the HBC method under different θ_c is shown in Figure 7.3, in which red and blue waveforms refer to V_α and V_β generated by the HBC and IPBC scheme. As shown, the proposed solution makes these two components more sinusoidal. Therefore, it would be expected to attain less distortion in output voltage and current.

The proposed trajectory of the reference voltage vector and its output phase

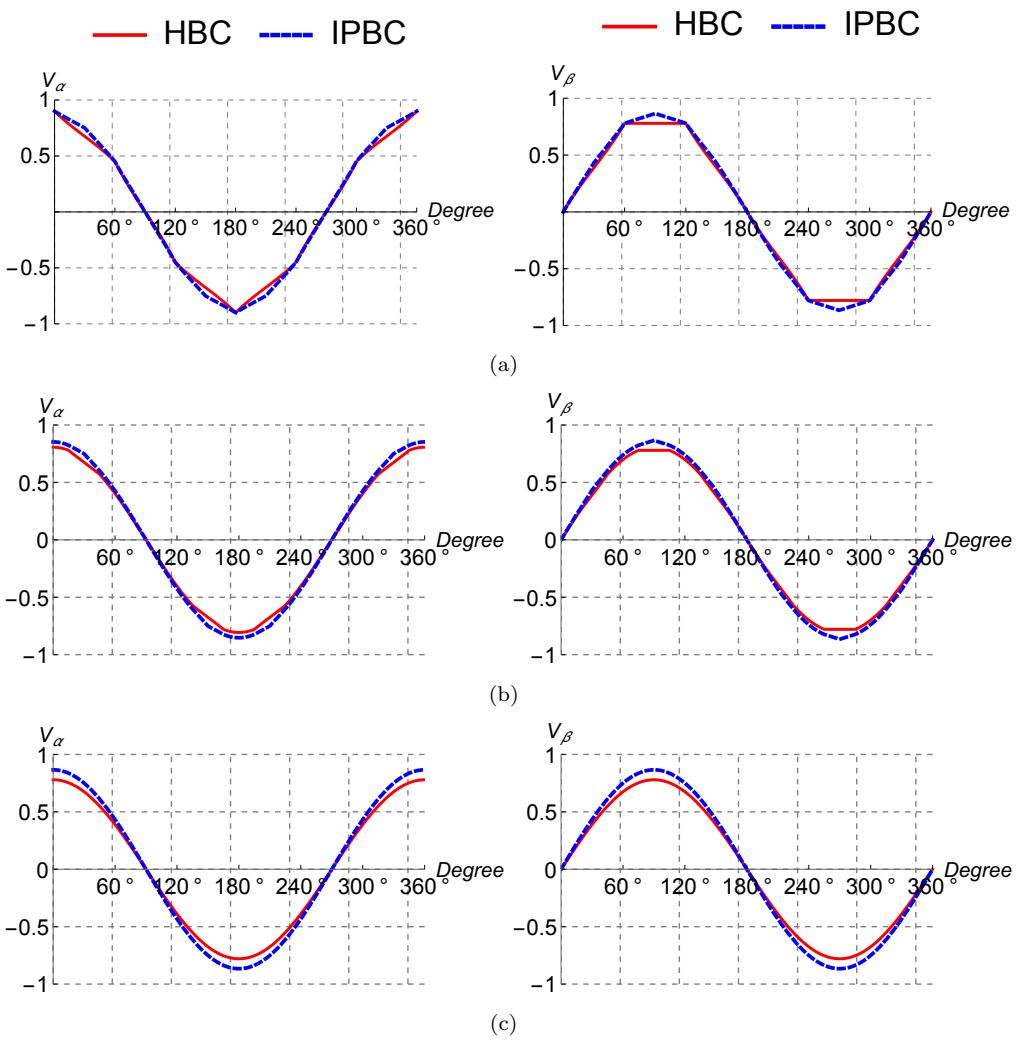


Figure 7.3: V_α and V_β ($\lambda = 0.9$) with (a) $\theta_c = 0°$ (b) $\theta_c = 15°$ (c) $\theta_c = 30°$

voltage in β-axis is given in Figure 7.4. The amplitude of its fundamental component can be thus calculated by the Fourier series expansion:

$$F(\theta) = \frac{\pi}{4} \int_{0°}^{90°} |V_{ref}|(\theta) \cdot \sin\theta \cdot d\theta \tag{7.6}$$

With equation (7.6), the desired modulation indices with different compression coefficients and crossover angles can be attained and described by Figures 7.5 and 7.6. As shown, the DC-link voltage utilization of the IPBC scheme is higher than that of the HBC scheme under the same conditions. In other words, λ and θ_c of the proposed technique are allowed to be set at a smaller value to achieve the same

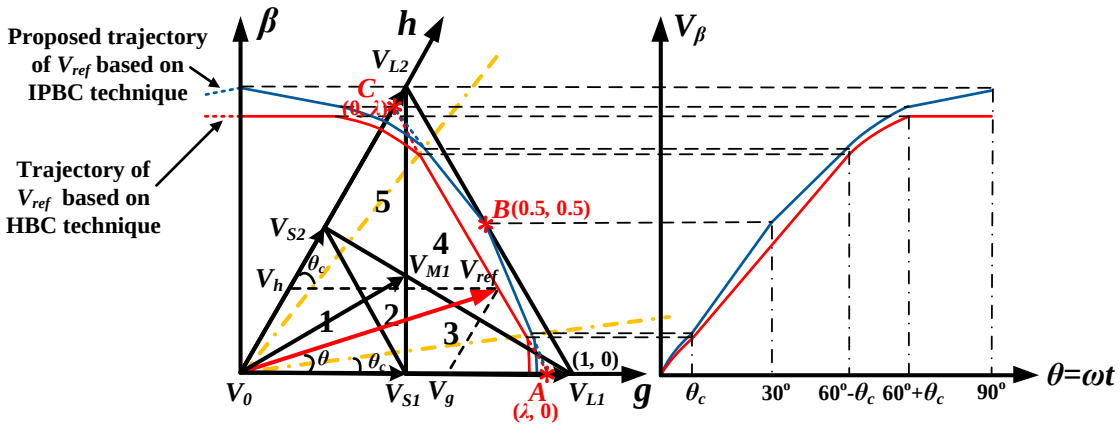


Figure 7.4: The trajectory of modified V_{ref} and corresponding V_β waveforms

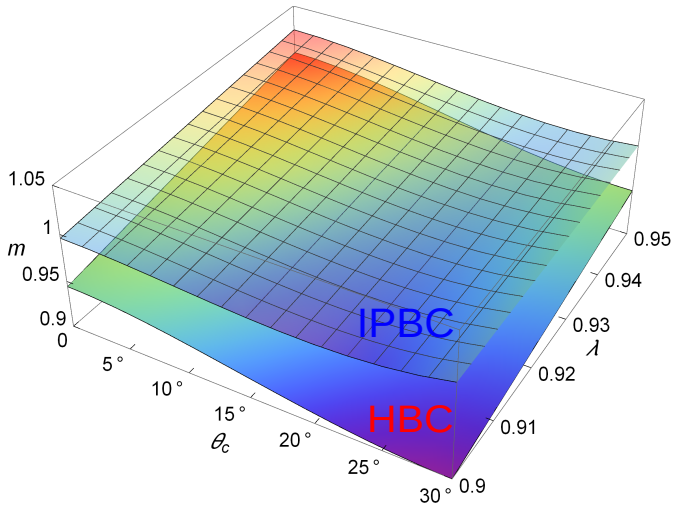


Figure 7.5: The 3D plot of $m(\theta_c, \lambda)$ with the HBC and IPBC technique

overmodulation capability as the prior method. Besides, it can be seen that m_{max} of the proposed approach is the same as that of the counterpart.

7.4 Initial Capacitor Voltage Imbalance

Although the employed VSVs can maintain NP voltage naturally balanced irrespective of modulation index and power factor angle, the voltage balance between two capacitors cannot be facilitated by itself if the initial NP potential imbalance exists under overmodulation conditions. As a result, the active capacitor voltage balancing control must be involved to handle the divergence.

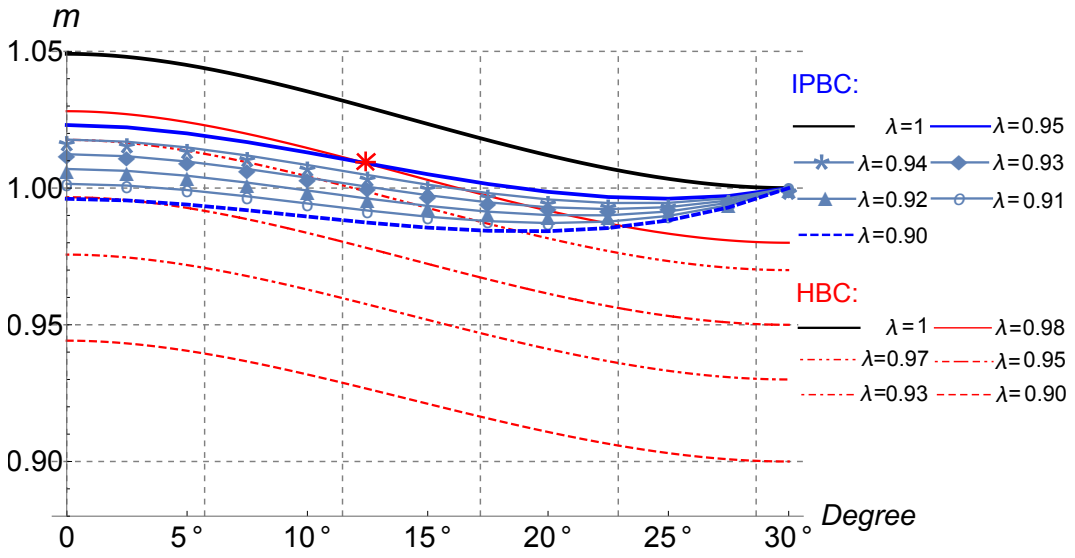


Figure 7.6: The relationship between m and θ_c at different λ

When an extra electric charge is accumulated in the last control period, the NP capacitor voltage shifts in the overmodulation region. Similar to the method presented in Chapter 5, in accordance with the operation mode of the ESG system, a straightforward approach is to manipulate the dwell time of space vectors that are able to provide NP current with appropriate polarity. By equation (5.1), here, the factor k defined by a ratio of upper and lower-side capacitor voltages is also chosen to allocate redundant small vector pairs. Figure 7.7 gives the modified switching instants under overmodulation conditions when V_{ref} is located in subsector 4 of Sector-I, where (g,h) is the real-time coordinate of the blue line shown in Figure 7.2.

To evaluate the ability of capacitor voltage balancing control, the fundamental component of output voltage should be set at the same value. For example, the compression coefficient of the HBC and IPBC limit are 0.98 and 0.95, respectively, and the crossover angle is set to be 12.5°. By doing so, the desired modulation indices are both 1.01 and the reference voltage vector is synthesized in subsectors 3-5. For simplicity, Sector-I is chosen as a representative example to investigate. The dwell time of active VSVs and the compensated charge ΔQ based on equations (3.3) and (5.2) are illustrated in Figure 7.8(a) and Figure 7.8(b), respectively, in which

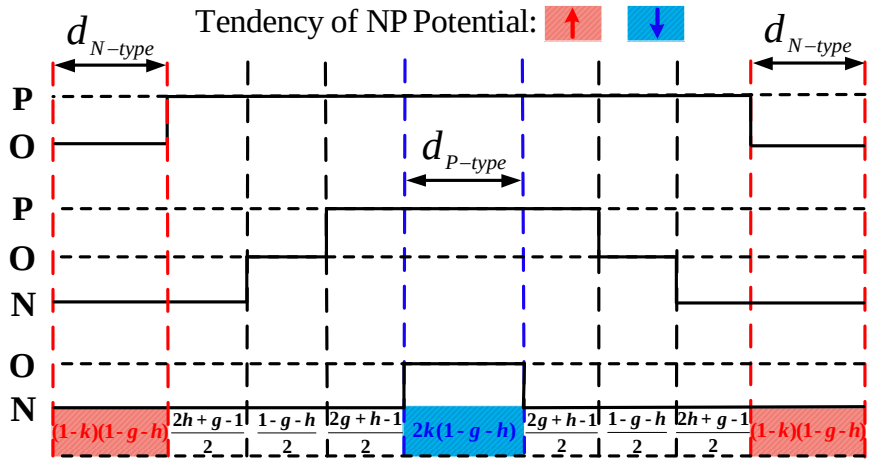
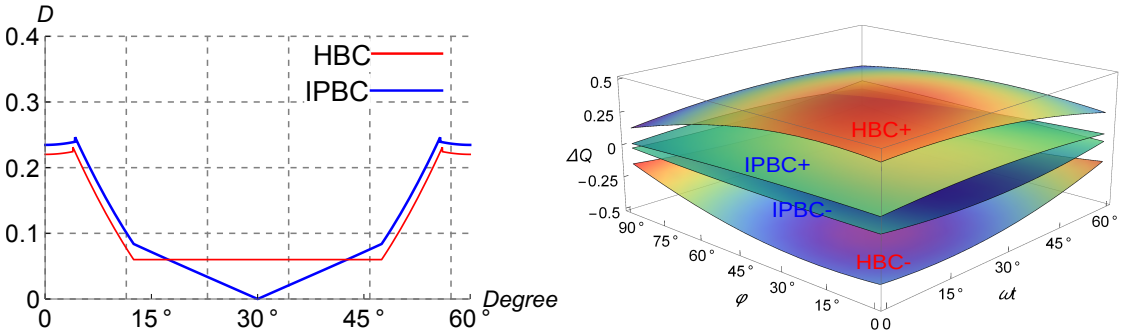


Figure 7.7: The modified switching instant for balancing NP voltage in subsector 4 of Sector-I



(a) (b)

Figure 7.8: The comparison of NP voltage balancing capability (a) active duty cycle of VSVs (b) ΔQ as a function of power factor ϕ and ωt

'+' and '−' represent the maximum and minimum value by corresponding solutions. As can be seen, though the compensation capability of the IPBC technique is a bit weak as compared to that of the HBC method, it can still resolve the NP voltage imbalance issue for all loads.

7.5 Simulation Results

In this section, the effectiveness and feasibility of the proposed overmodulation algorithm are validated by simulation results that are obtained from a Simulink/PLECS model. First of all, the ESG system works in the startup process. The flux-weakening control is triggered at 0.5s. Generation mode starts by connecting a

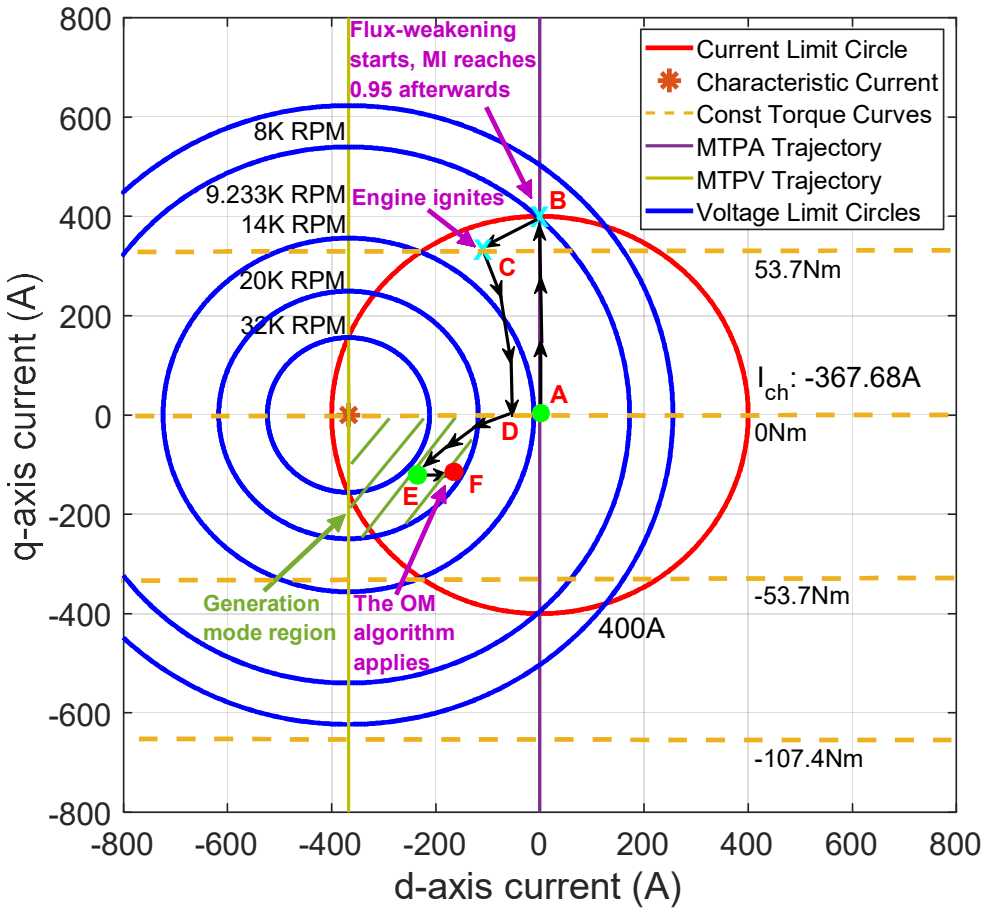


Figure 7.9: Operating trajectory of the studied ESG system

10kW resistive load to the DC-link at 1s. The presented strategy is activated at 1.1s. The main parameters can be found in Table 5.3.

7.5.1 The Operation of High-Speed Machine

The whole operating trajectory and relevant limits given by equations (2.4) and (2.5) are shown in Figure 7.9. In the startup process, denoted as the constant torque region, the maximum torque per amp (MTPA) line is followed by point A. The deep flux-weakening current is injected at point B in the constant power region. Then, the trajectory tracks the voltage limits based on the machine speed and current limits set by the converter. The ESG system is in standby mode after engine ignition at 10krpm, which is denoted by point C. The q-axis current maintains at zero and

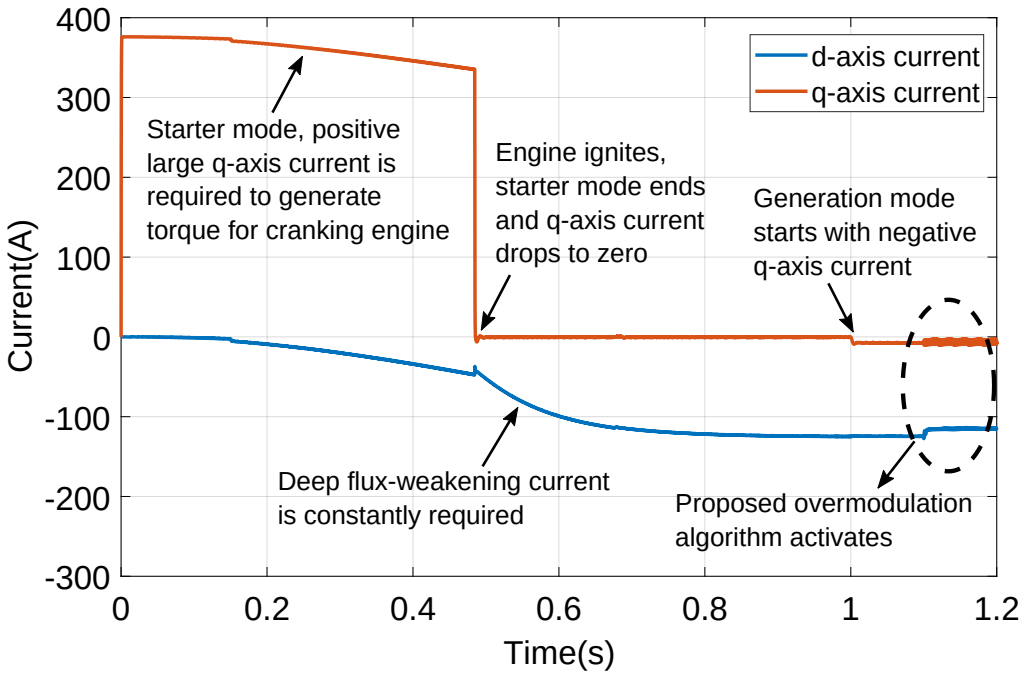
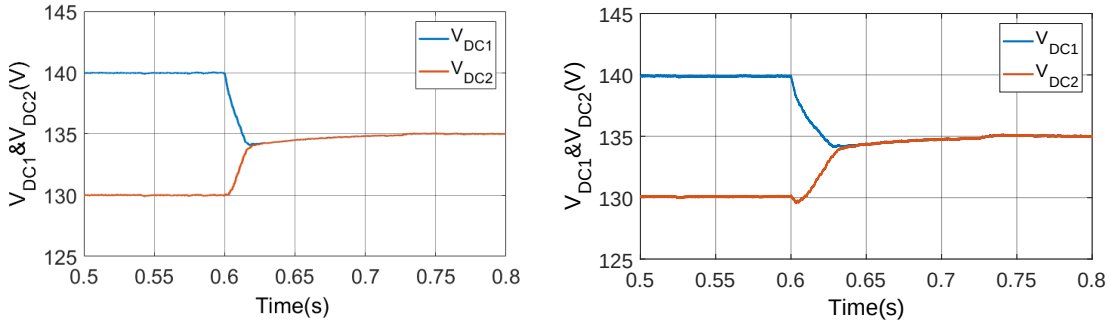


Figure 7.10: Simulated dq-axis current of the ESG system

operation status is at point D until the generation mode starts. At that time, the S/G systems work in the power generating region, and the modulation index ramps up to 0.95. As the required flux-weakening current is dropped due to a boosted DC-link voltage utilization, the operating point subsequently moves from point E to F.

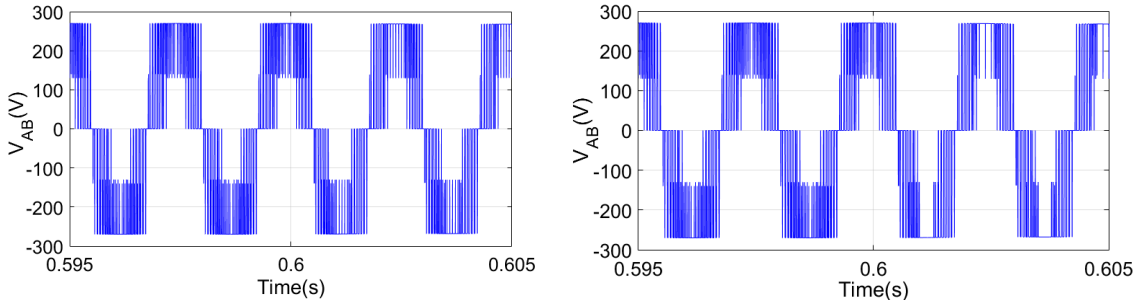
7.5.2 Improvement of DC-link Voltage Utilization

Without loss of generality, for the proposed algorithm, the crossover angle θ_c is set to be 12.5° and the compression coefficient λ is 0.95. The results of simulated dq-axis current shown in Figure 7.10 describe the required torque and flux-weakening currents for the motor drives in the entire-speed range operation. As can be seen, d-axis current is significantly reduced after 1.1s. This indicates that the IPBC scheme offers a higher DC-link voltage utilization, thereby extending the operation of the ESG system into the overmodulation region. While the ripple in i_q is unavoidably increased, which trades an enlarged converter output voltage range against output harmonics.



(a) (b)

Figure 7.11: DC-link capacitor voltage balancing process with (a) the HBC method (b) the proposed IPBC method



(a) (b)

Figure 7.12: The line-to-line voltage when transiting modulation scheme at 0.6s with (a) the HBC method (b) the proposed IPBC method

7.5.3 Capacitor Voltage Balancing and Three-Level Switching Performance

In order to verify the capacitor voltage balancing performance of the HBC scheme and the proposed overmodulation technique, the condition of λ and θ_c are both set to be 0.95 and 12.5°. Additionally, the initial voltage of upper and lower-side capacitors are 140V and 130V, respectively.

Before gaining the overmodulation conditions at 0.6s, the operating point is in the LM region with a modulation index of 0.95 and the conventional NTV^2 scheme is used to generate firing pulses. After that, the HBC and IPBC schemes are performed, respectively. As shown in Figure 7.11, the NP voltage can be kept at a balanced state by using these two methods. It can be also observed that the recovery time for the IPBC scheme is a bit longer than the HBC counterpart, which is

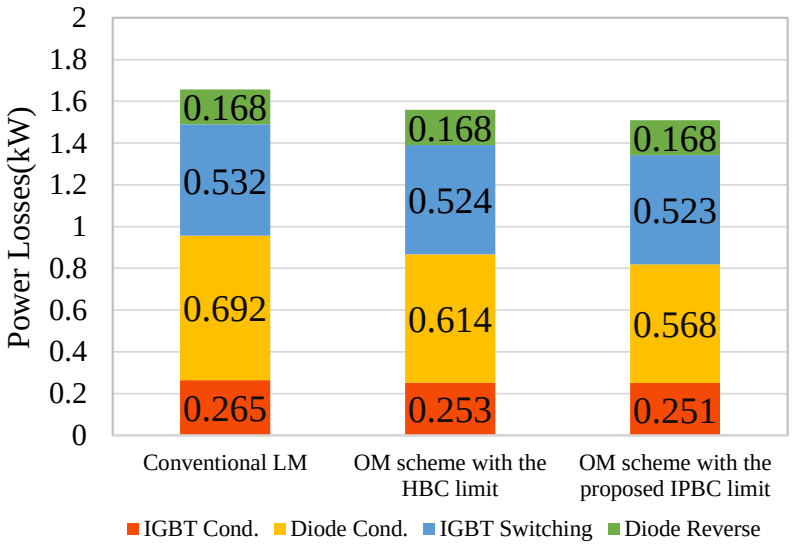


Figure 7.13: The converter losses comparison under different PWM schemes at 20krpm in the generation mode

consistent with the theoretical analysis in the last Section.

Furthermore, the line-to-line voltage shown in Figure 7.12 validates that both the HBC and IPBC schemes can ensure three-level switching using their dedicated reference voltage vector trajectories.

7.5.4 Power Losses Analysis

According to the data from manufacturer's manual, the loss can be obtained through the PLECS tools. For example, θ_c is set at 10° while λ for the HBC and IPBC limit are selected at 0.97 and 0.94, respectively. The modulation index in the LM region is 0.95. Under these circumstances, with converter's switching frequency of 16kHz and 35kW of active power generation at a speed of 20krpm, the semiconductor losses distribution in the LM and the OM-I are shown in Figure 7.13. As shown, the two overmodulation algorithms can both lower conduction losses compared with the normal LM operation. Moreover, due to the increased DC-bus terminal clamping instants, the switching losses are reduced as compared to that by the LM.

By importing the data of stator currents into the finite element analysis (FEA) model of the applied PMSM, the machine copper loss can be calculated in the steady

state. Compared with typical operation in the LM, the results show that the value is significantly decreased from 189.96W to 160.18W with the upper limit of the OM-I, which means a nearly 15.7% reduction.

The harmonic loss on a machine depends on stator harmonic copper losses, rotor harmonic copper losses, harmonics core losses and stray-load losses, also this value is highly related to the selected loss coefficient [177]. Such a complicated loss investigation by the PWM effects will be carried out in our future study.

7.6 Experimental Validation

The experimental validation in this section primarily focuses on the ESG system operating in the OM-I, particularly for a light-load condition.

7.6.1 Overmodulation Performance

The experimental comparison between the HBC scheme and the presented IPBC scheme with the same θ_c of 12.5° is performed at a machine speed of 20krpm, whereas λ of these two methods refer to 0.97 and 0.95, respectively. As shown in Figure 7.14, both the HBC scheme and the proposed solution can lower i_d. Because of the ability to further deepen 1.5% of modulation index, i.e., m^* of 1.020 and 1.015 correspond to the HBC and IPBC scheme, respectively, the presented overmodulation technique therefore brings that value from -115A to -107.5A, as opposed to i_d of -110A with the HBC scheme at the same operating conditions. Moreover, it can be observed that the ripple of i_q by the IPBC scheme is smaller than the HBC counterpart.

The maximum torque by the HBC (λ=0.97) and IPBC (λ=0.95) scheme is measured at the different machine speeds, as shown in Figure 7.15. It can be seen that the proposed strategy gains T_{em}=14.3Nm at a shaft speed of 20krpm, which means the output torque capability is roughly increased by 3.6% as compared to the HBC limit. Besides, in comparison with the LM operation, the proposed modulation algorithm enhances 10% output torque capability for the studied drives. On the other hand, it is known from the above torque-speed characteristic that the base speed

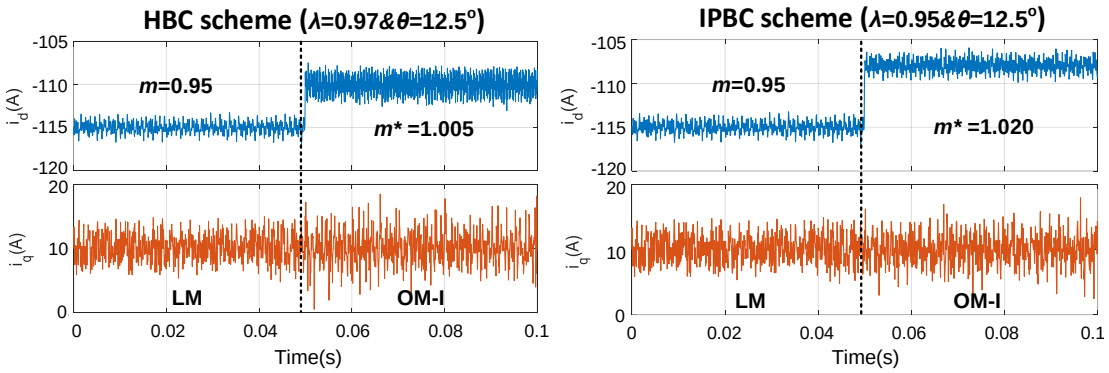


Figure 7.14: Experimental results of dq-axis current

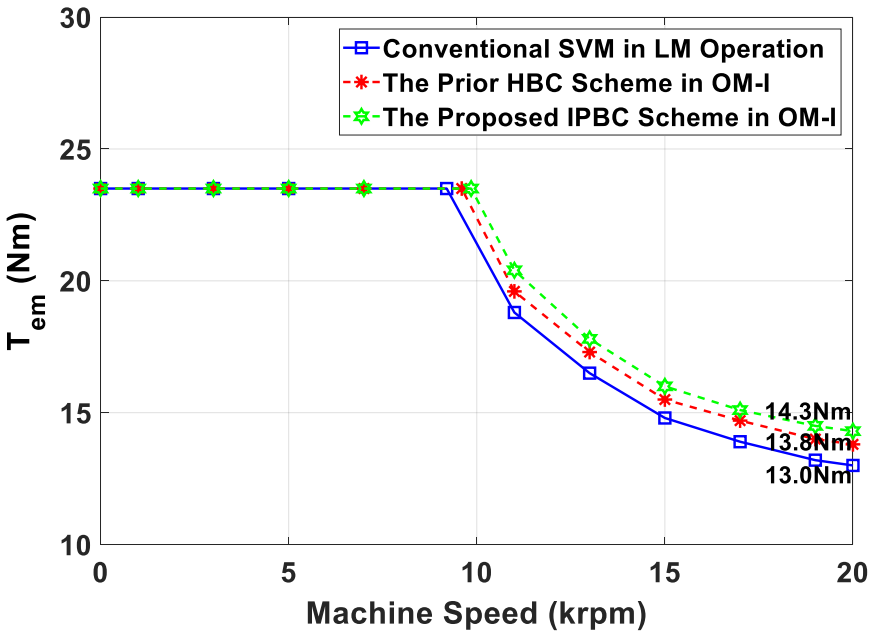


Figure 7.15: Output torque capability curves of the 3L-NPC power converter-fed PMSM drives

of the target motor drives has arisen from 9233rpm to 9850rpm with the proposed IPBC scheme.

7.6.2 Steady-State Performance

When the PMSM operates at a speed of 20krpm, the steady-state performance under the LM (m=0.95) and the OM-I with the proposed IPBC limit (λ=0.95 and θ_c=12.5°) are tested. The results from Figure 7.16 show that the line-to-line voltage by the proposed overmodulation algorithm features five levels and constant clamping

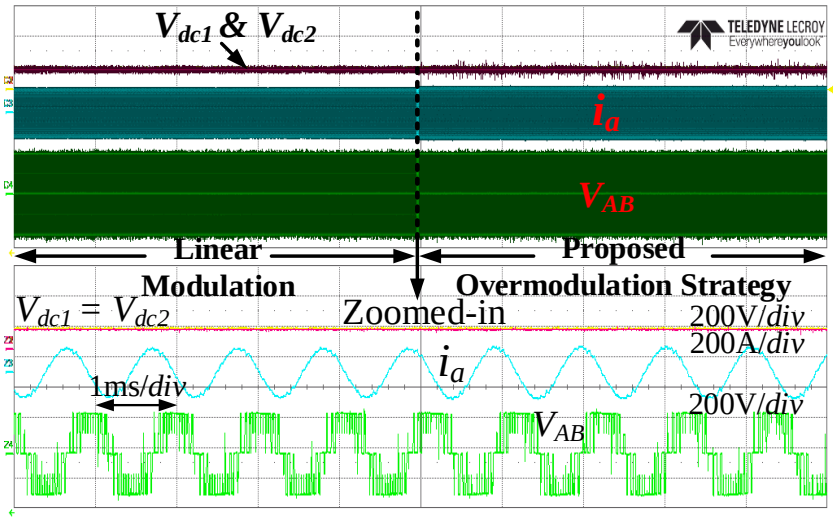


Figure 7.16: Steady-state performance

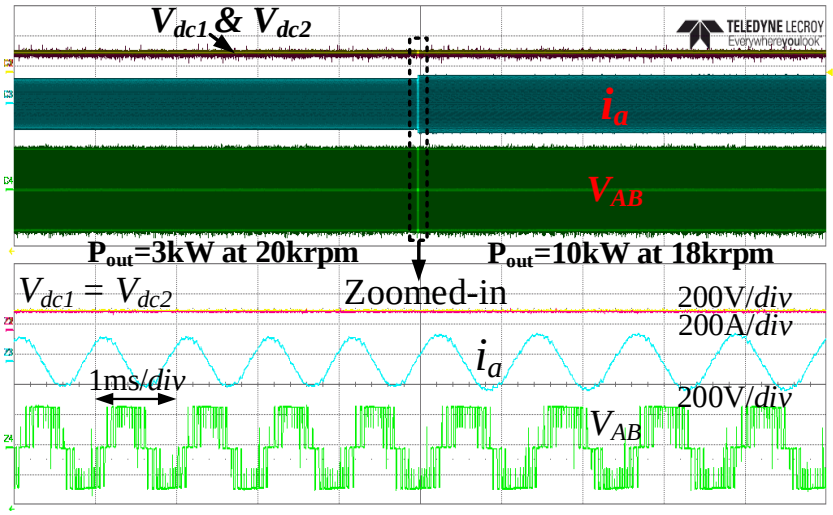
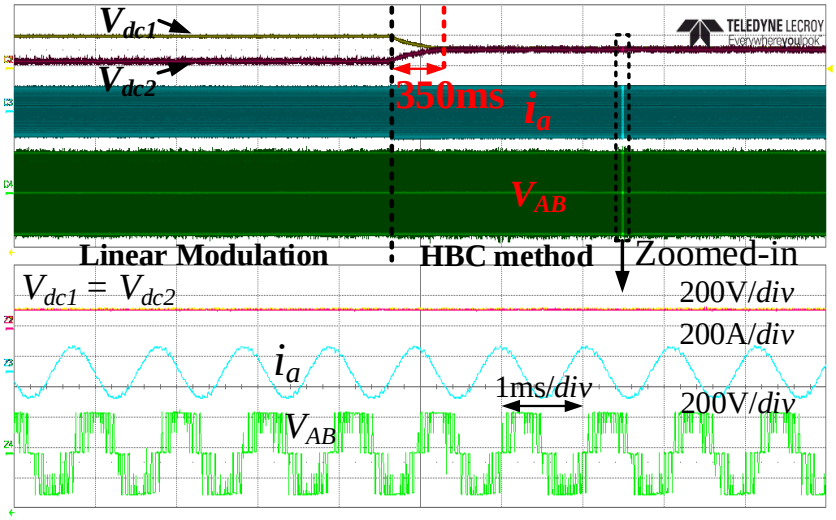


Figure 7.17: Transient-State performance

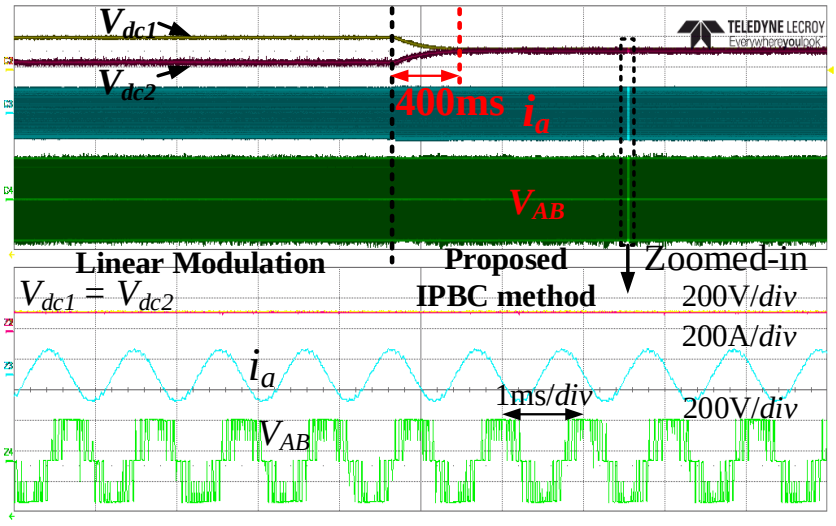
instants in some periods. Apart from that, two capacitor voltages are well balanced.

7.6.3 Transient-State Performance

To verify the transient-state performance of the proposed algorithm, machine speed and load are both changed instantly, in which λ and θ_c are set to be 0.95 and 12.5°, respectively. Initially, the output active power delivered by the ESG system is 3kW when the machine speed is 20krpm, in which the q-axis reference current command is -6A. After that, the motor speed descends to 18krpm while the load is increased



(a)



(b)

Figure 7.18: NP voltage balancing process with (a) the HBC method and (b) the proposed IPBC method

to 10kW, where the q-axis reference current command is -25A. The results from Figure 7.17 present a smooth dynamic performance in terms of NP voltage, phase current and line-to-line voltage.

7.6.4 Capacitor Voltage Balancing Performance

This key performance is demonstrated under a DC-link voltage utilization ratio of 1.02. That is, λ for the HBC and IPBC scheme is 0.98 and 0.95, while θ_c equals

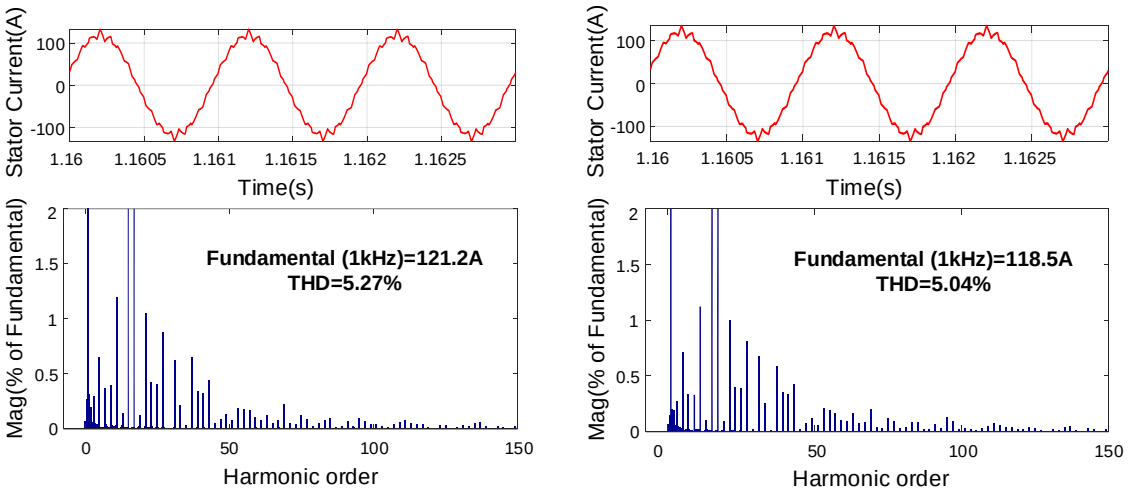


Figure 7.19: FFT analysis of the stator currents under λ=0.95 and θ_c=12.5° with (a) the HBC scheme (b) the proposed IPBC scheme

12.5°. As seen from Figure 7.18, the initial NP voltage deviation is 200V in the LM region, in which the average modulation index and power factor are around 0.95 and 0.12, respectively. When switching to the proposed overmodulation strategy, two capacitor voltages can be maintained at a balanced state again. Compared with the HBC scheme, an additional recovery time of 50ms is required to correct the unbalanced NP voltage.

7.6.5 Phase Current Distortion Analysis

Figure 7.19 presents the FFT analysis of the stator currents when the compression coefficient is set at 0.95 and the crossover angle is controlled at 12.5°. It can be seen that the THD by the proposed scheme is less than that by the HBC scheme, which is consistent with the theoretical analysis given in Section 7.3.

7.6.6 Output Voltage Distortion Analysis

The weighted THD (WTHD) comparison of the line-to-line voltage under different λ and desired m is illustrated in Figure 7.20. From the results, it can conclude that the presented inscribed polygonal-boundary limit obtains a lower WTHD as compared to the hexagonal compression limit.

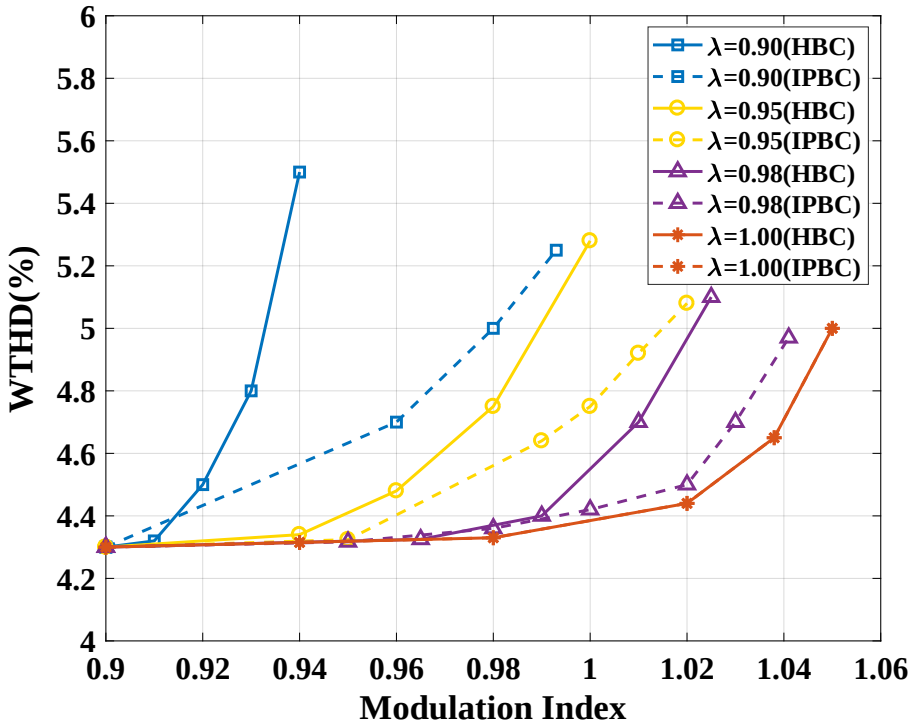


Figure 7.20: WTHD comparison of the line-to-line voltage at different λ and m

7.6.7 Power Converter's Losses

In order to experimentally test the 3L-NPC converter's total losses under the above overmodulation conditions, a power analyzer PPA5330 is used to monitor the input and output parameters when the target system delivers an active power of 25kW at a rotation speed of 20krpm. A resultant of 1.24kW power loss is measured under the presented approach, while that value in the case of the benchmark method is about 1.30kW.

7.6.8 Computational Time Performance

The simplified computation is one of the benefits of the proposed overmodulation strategy. Its execution time is tested through the applied control platform. The results show that it uses 57.2μs to implement the algorithm in the g-h reference frame, while 73.8μs to implement in the conventional α-β reference frame. As a result, the computational effort is approximately reduced by 22.49%.

7.6.9 Comparison with Other NP Control-Based Overmodulation Strategies

Compared with existing NP control-based overmodulation strategies [121, 169–174] for 3L-NPC converters, the proposed strategy embraces the following advantages:

1) Since the configured switching patterns generate extra electric charge to realize net-zero NP current, the proposed capacitor voltage balancing control is effective for high modulation index and low power factor operating conditions. However, the methods presented in [169–173] can hardly achieve this target.

2) Due to the adopted nearest-three VSVs, less output distortion would be expected as compared to the work of [121] that omits space vector numbers in the high output voltage region.

3) The complexity caused by massive trigonometric functions is reduced by algebraic operations in the g-h plane. While the CBPWM scheme reported in [174] gains overmodulation conditions, the appropriate ZSVs need to be calculated.

4) With the proposed IPBC technique, the maximum output voltage converges to the upper limit of LM, which is beneficial for smooth transition among various compression coefficients, particularly for traction and servo drives, where loading conditions and speed change frequently [174]. On the other hand, due to the non-monotonous relationship between θ_c and m shown in Figure 7.6, the continuity of boosted DC-link voltage utilization would be affected to some extent in comparison with the HBC scheme. However, the minimum modulation depth by the provided strategy gaining near unity might make this issue marginal.

7.7 Conclusions

In order to further improve DC bus voltage utilization with a definite unipolar structure for the aircraft's electrical power system, i.e., 270VDC, a VSV-based PWM algorithm has been proposed in this Chapter for the 3L-NPC power converter, which aims at the operation of studied ESG systems extending into the overmodulation

region.

With the proposed reference voltage vector trajectory, this study embraces the following advantages. First of all, DC-link voltage utilization is boosted under a lower crossover angle and compression coefficient, which brings benefits regarding flux-weakening current reduction, lower machine copper loss and higher output torque of the PMSM. Secondly, in order to remain a balanced NP voltage under stringent operating conditions, an active capacitor voltage control method is developed to supplement the algorithm. What's more, a fast-executed approach is adopted as an alternative to overcome the computational burden.

Although the OM-II is out of the scope of this work, a higher DC-link voltage utilization achieved by the proposed IPBC technique is also applicable to other industrial fields and will be discussed in the future study.

Chapter 8

Conclusions and Future Works

8.1 Summary

In our developed aircraft ESG system for the MEA, a high-speed PMSM is mechanically coupled to an engine shaft via a gearbox, and electrically connected with a 3L-NPC power converter that interfaces the S/G systems to the onboard EPS. In the startup process, the converter serves as an inverter that drives the machine to crank and accelerate the engine shaft. Once the machine is driven up to a self-sustained speed, the engine ignites immediately. After that, the target system goes into the standby mode. When the motor's shaft speed approaches 20krpm, generation mode starts. In this mode, the engine drives the PMSM to generate electrical power, and the converter works as a rectifier to convert this variable frequency AC into DC which supplies aircraft onboard loads.

Considering that the employed three-level topology has the inherent NP voltage imbalance problem due to the split DC-link capacitor bank, CMV in the drive systems highly depends on the adopted PWM strategy, and the converter interfaced by a definite DC-link voltage of 270VDC might be subjected to large back EMF during the PMSM's high-speed operation. These crucial characteristics indicate optimization objectives for the ESG system, which are elaborated in the following:

- The voltage drift in the NP causes extra over-stress on semiconductor devices.

Besides, it produces low-order harmonics on the motor side. More seriously, the power quality of onboard EPS might be degraded.

- The reliability issue should be drawn more attention for the developed high-speed aerospace drives fed by three-phase PWM converters. This is because the high component of CMVs in the S/G systems much easily results in premature failure of the motor bearings because of motor shaft voltage and leads to radiated EMI issues due to high-frequency leakage current flowing into the ground through motor stray capacitors.
- The flux-weakening control is required to ensure that the back EMF is within the converter limits. Consequently, a large flux-weakening current causes additional machine copper losses and reactive power. In addition, the output electromagnetic torque capability in the constant power region is weakened as the speed of machine increases and is constrained by stator voltage.

8.2 Conclusions

The thesis provides insight into the PWM technique for the performance improvement of the ESG system in the MEA.

1. In order to implement active capacitor voltage balancing control, the conventional NTV^2 scheme is modified by adjusting the dwell time of redundant small vectors dynamically. For the pursuit of lower CMV magnitude and perfectly balanced NP voltage, a series of new virtual space vectors are synthesized.
2. The hybrid modulation strategy is proposed since there is an operational time for the startup process until the ESG system runs under the power generating conditions. With the presented modulation strategy, switching losses are reduced in starter mode. In generation mode, the magnitude of CMV is suppressed. Furthermore, the capacitor voltage balance is satisfied during the whole operating period.

3. The overmodulation conditions by the proposed reference voltage vector trajectory are investigated. This aims to achieve a higher DC-link voltage utilization, thereby reducing the large required flux-weakening current.

In Chapter 3, the NP voltage imbalance and oscillation problem for 3L-NPC converters have been studied based on the conventional SVM and CBPWM schemes.

The findings show that phase current flowing into and out the midpoint of DC-link has a negative impact on two capacitor voltages. Besides, the average non-zero NP currents render the NP voltage variation in every switching period. Since the participation of small vectors of the NTV method becomes less for high modulation index and low power factor conditions, the NP drift becomes severe, particularly for the unfavourable operating conditions of the aircraft ESG system. The 3^{rd}-order harmonic injection-based SPWM scheme shows that the existence of low-frequency NP voltage ripple is characterized by three times of the fundamental frequency.

The analysis and discussion in this Chapter reveal the shortcomings of conventional methods. It is notable that the average NP current generated by the NTV^2 scheme is constantly zero, which is free from the limitation of modulation index and power factor. Based on these reasons, the VSV-based modulation strategy is chosen as the candidate for our application in the subsequent Chapters.

In Chapter 4, considering that the modulation process of the NTV^2 scheme is more complicated than that of the NTV scheme, especially for the complexity of subsector identification, the fast calculation approach based on the g-h reference frame has been introduced, which aims to simplify the sector/subsector identification and dwell time calculation.

Even though the method based on the conventional α-β reference frame can use two auxiliary angles to identify the subsector numbers, cumbersome implementation unavoidably results in computational burden. To address this disadvantage, the fast calculation approach is adopted to simplify the identification and dwell time calculation process for the digital control systems. The results show that sinusoidal operations have been avoided, which is helpful for improving algorithmic-efficiency of the enhanced SVM strategies proposed in the following Chapters.

In Chapter 5, the conventional NTV^2 modulation strategy has been modified to report two new SVM techniques.

With the duty cycle offset over a switching sequence, the first modulation strategy is characterized by active capacitor voltage balancing control capability. The method is able to resolve the NP deviation issue even under initial capacitor voltage imbalance conditions.

By composing basic space vectors with a lower CMV magnitude, a series of new virtual space vectors are hence generated. In comparison with the original NTV^2 scheme, switching actions are increased, particularly for the lower modulation index region. Through the flux-vector error analysis, it is known that the torque ripple of the proposed scheme is a bit larger than that of the conventional counterpart. Nevertheless, the proposed scheme facilitates a trade-off for NP voltage balance and CMV reduction.

In Chapter 6, a hybrid SVM technique has been proposed for the 3L-NPC converter in the developed motor drive systems, which improves the modulation performance for the wide-speed range operation of the ESG system.

In the beginning, the NTV scheme is used in the startup process as NP voltage balance can be effectively controlled in low modulation index and high power factor region. In addition, switching actions are lower than that of the conventional NTV^2 scheme. When the ESG system enters into power generation mode, an enhanced NTV^2-based modulation scheme is employed. Consequently, not only can low-frequency NP voltage ripple be eliminated, but also CMVs in the converter-fed motor drives are significantly suppressed. Additionally, with the proposed phase duty cycle offset approach, the modulation algorithm achieves DC-link capacitor voltage balancing control capability even though the NP voltage shifts under operating conditions of high modulation index and low power factor.

In Chapter 7, a VSV-based PWM algorithm has been proposed for the operation of the 3L-NPC converter in the overmodulation region. The reason is that the current DC-link voltage of 270VDC constraints the output capability of the converter-fed high-speed PMSM drives, such as electromagnetic toque and maxi-

mum machine speed range. Although a large injected flux-weakening current can handle these deficiencies, it induces extra copper losses on the motor.

With the help of the proposed reference voltage vector's trajectory, firstly, DC bus voltage utilization ratio is improved under a lower crossover angle and compression coefficient, which brings further benefits of flux-weakening current and machine copper loss reduction, together with the enhanced maximum output torque of the applied PMSM. Secondly, the capacitor voltage control method is developed to supplement the algorithm so as to maintain NP voltage balanced if a voltage error across the capacitors initially exists.

The simulation and experimental results have been carried out to validate the correctness and effectiveness of the proposed strategy of the thesis and have been shown in each Chapter.

8.3 Future Works

Although the works in this thesis have addressed several technical problems in the field of the pulse-width-modulation for the 3L-NPC converter used in the aircraft ESG system, there are still potential research topics that could be explored further in the future.

8.3.1 Unbalanced DC-Link Capacitor Voltage Control

In order to reduce the cable weight of the current electrical system, high-voltage electrical systems are considered. The emerging standards of 540VDC (±270VDC) are incorporated for the bipolar structure of future aircraft. Based on the MIL-STD-704 [15], onboard loads connected to positive or negative DC-rail have a margin voltage in accordance with their power demands. Hence, upper and lower-side voltages are allowed to be unevenly manipulated in that scenario. Through the study of this thesis, small space vectors play a crucial role in the NP voltage regulation. This provides a good starting point to achieve that goal.

8.3.2 Modulated Model Predictive Control

A number of VSV-based modulation schemes have been discussed in the thesis. However, in terms of the dynamic performance of the system, the conventional PI+SVM method can be greatly improved if the VSV-based modulated model predictive control (M^2PC) is applied. Future works will incorporate the superiorities of the traditional NTV^2 scheme and the finite-set MPC algorithm.

8.3.3 Discontinuous Pulse-Width-Modulation Scheme

As one of the main drawbacks of the NTV^2 scheme is the extra switching actions, thermal loss reduction is an objective of optimization. It is known that the DPWM scheme maintains none-commutation in some phase legs. However, in order to control NP voltage, the relationship between ZSV and NP current should be investigated, and then appropriate ZSVs are injected into three-phase modulation signals.

8.3.4 Synchronized Pulse-Width-Modulation Technique

Due to the high fundamental frequency of the ESG system (up to 1kHz in the case of 16kHz and rotation speed of 20krpm), the carrier-ratio is as low as 16 over a line period. As a result, the sub-order harmonic issue that is harmful to the machine may occur. When the motor speed approaches 32krpm in future tests, that value will decrease further. i.e., carrier-ratio equals 10. In order to solve this tricky problem, the synchronized PWM technique will be explored, which aims to keep carrier-ratio at a constant value even though the drives operate at a high speed in the power generation mode.

8.3.5 Artificial-Neural-Network Aided Modulation Scheme

It can be seen that a modulation strategy is performed through three input variables, i.e., V_g, V_h and V_{dc}, and a series of output variables that are normally dedicated duty cycles and switching sequences. As a result, a PWM modulator can be treated

as a black box. With the help of the highly-developed artificial intelligence (AI) algorithms, such as the artificial neural network (ANN), the correlation between the input and output variables could be trained after data collection. Therefore, the approaches presented in this thesis would be substantially simplified based on ANN-aided technique, which will be investigated in our future works.

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Appendix A

A Reference Frame Transformation

There are three conventional reference frames: natural (abc), stationary ($\alpha\beta$), synchronous rotating (dq). Clarke's and Park's transformations are widely used to simplify the analysis of three-phase circuits. The aim of Clarke's transformation is to project the three-phase variables into a stationary two-axis reference frame, i.e., transform the variables from the natural reference frame to the stationary frame. However, the Park's transformation transforms the variables from the stationary reference frame into a rotating two-axis reference frame.

A.1 Clarke Transformation

The Clarke transformation converts three-phase balanced variables into balanced two-phase quadrature variables. In order to make the transformation invertible, the zero sequence component is normally added. Hence, Clarke's transformation matrix can be expressed by:

$$x_{\alpha\beta 0} = T_c \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} x_{abc} \tag{A.1}$$

where where $x_{\alpha\beta 0}$ is the quantity in the stationary reference frame and x_{abc} is the quantity in the natural reference frame. T_c is a constant coefficient depending on

the principle of the transformation. There are different T_c corresponding to the following situation:

$$\begin{aligned} T_c &= 2/3, \text{ amplitude invariant} \\ T_c &= \sqrt{2/3}, \text{ power invariant} \end{aligned} \tag{A.2}$$

In this thesis, the amplitude invariant principle is applied. That is, T_c equals 2/3.

A.2 Park Transformation

The Park transformation converts a vector in two-phase balanced orthogonal stationary system into an orthogonal rotating reference frame. The dq transform is often used in order to simplify the analysis of three-phase synchronous machines or to simplify calculations for the control of three-phase inverters. In the analysis of three-phase synchronous machines, the transformation transfers three-phase stator and rotor quantities into a single rotating reference frame to eliminate the effect of time-varying inductances. The primary value of the Park transform is to rotate the reference frame of a vector at an arbitrary frequency. The Park transformation matrix is defined as:

$$x_{dq} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} x_{\alpha\beta} \tag{A.3}$$

On the other hand, in order to convert back from a dq-based reference vector to the $x_{\alpha\beta}$ reference frame, the column vector signal must be pre-multiplied by the inverse Park transformation matrix:

$$x_{\alpha\beta} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} x_{dq} \tag{A.4}$$

By utilizing the Clarke and Park transformation, three time-varying quantities are therefore transformed into two non-time-varying quantities. Linear control methods, such as PI control, can be easily used in a synchronously rotating dq reference frame.

As a result, these two transformation procedures are beneficial for the analysis of the electrical power system and the development of control layout.

Appendix B

Power Electronic Devices Losses

B.1 Calculation of Power Module Loss

The power module of our designed 3L-NPC prototype is composed of an IGBT and an antiparallel freewheeling diode. In the following, the theoretical calculations are derived.

First of all, the total loss of IGBT includes conduction loss and switching loss, where conduction loss can be expressed as:

$$P_{cond,T} = v_{0,T} I_T + r_T I_T^2 \tag{B.1}$$

where I_T is the current flowing through IGBT, $v_{0,T}$ and r_T are the initial saturation voltage drop and on-resistance of IGBT at ambient temperature T, respectively. Its switching loss can be expressed as:

$$E_{sw,T} = (A_{sw,T} I_T^2 + B_{sw,T} I_T^2 + C_{sw,T}) \times (\frac{U_{ce}}{U_{base}})^{D_{sw,T}} (\frac{T}{T_{base}})^{k_{sw,T}} \tag{B.2}$$

where $A_{sw,T}$, $B_{sw,T}$, and $C_{sw,T}$ are the parameters obtained by the quadratic fitting of the switching loss to the current. U_{ce} is the real voltage across the switching devices, T is ambient temperature of IGBT. U_{base} and T_{base} are the reference voltage and temperature, respectively. $D_{sw,T}$ and $k_{sw,T}$ are the voltage and temperature

correction coefficients, respectively. As a result, the total losses of IGBT is given by:

$$P_T = E_{sw,T} + P_{cond,T} \tag{B.3}$$

Secondly, the total losses of freewheeling diode include conduction loss and reverse recovery loss. Its conduction loss can be expressed as:

$$P_{cond,D} = v_{0,D} I_D + r_D I_D^2 \tag{B.4}$$

where I_D is the current flowing through the freewheeling diode, $v_{0,D}$ and r_D are the initial saturation voltage drop and on-state resistance of freewheeling diode at ambient temperature, respectively.

The conduction loss of freewheeling diode is very small, its main switching loss is the reverse recovery loss $E_{rec,D}$ which can be calculated by:

$$E_{rec,D} = (A_{rec,D} I_D^2 + B_{rec,D} I_D^2 + C_{rec,D}) \times (\frac{U_{ce}}{U_{base}})^{D_{rec,D}} (\frac{T}{T_{base}})^{k_{rec,D}} \tag{B.5}$$

where $A_{rec,D}$, $B_{rec,D}$, and $C_{rec,D}$ are the parameters of freewheeling diode obtained by the quadratic fitting of the switching loss to the current. $D_{rec,D}$ and $k_{rec,D}$ are the voltage and temperature correction coefficients of the diode, respectively. Hence, the total loss of freewheeling diode can be expressed as:

$$P_D = E_{rec,D} + P_{cond,D} \tag{B.6}$$

Consequently, the total losses of power module including IGBT and freewheeling diode can be yielded as:

$$P_S = P_T + P_D \tag{B.7}$$

B.2 Simulation of Power Module Loss

In Chapter 5-7, the power converter's efficiency is taken into account for the purpose of modulation comparison. The tool used to obtain those results was Matlab/Simulink with the *Plexim* PLECS toolbox. PLECS (Piece-Wise Linear Electrical Circuit Simulation) is a toolbox for the fast simulation of electrical circuits within the Simulink environment. Also, it enables to evaluate switch device conduction and switching losses by using the specifications that can be found from the manufacturer's datasheet. For our case, the manual of F3L400R07ME4_B22/B23 [72] is considered in the following.

B.2.1 Conduction Losses

The PLECS toolbox allows to specify the on-state voltage used for the loss calculation as a function of the device current and the device temperature: $v{=}f(i,T)$. This function is defined in the 'Conduction loss' tab of the 'Thermal Description' as a 2D look-up table, as shown in Figure B.1. Then, the conduction loss can be simply evaluated starting from the instantaneous current, moving along the 2D look-up table and multiplying the actual current by the correspondent voltage.

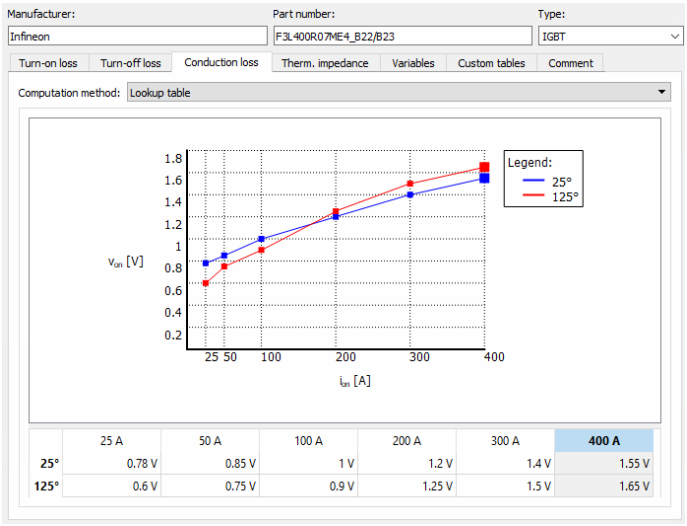
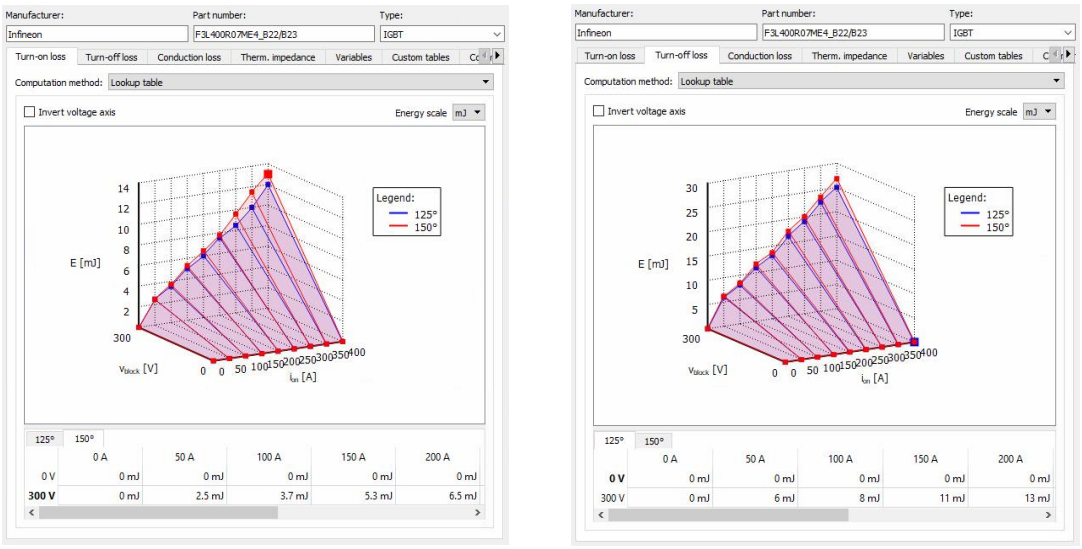


Figure B.1: Conduction loss with 2D look-up table in the Thermal Description



(a) (b)

Figure B.2: 3D look-up table in the Thermal Description for (a) turn-on loss (b) turn-off loss

B.2.2 Switching Losses

Switching losses are produced in the power module because the device's transitions from on-state to off-state do not occur instantaneously, and vice versa. During the transition, there is an interval where both current through and the voltage across the device are different from zero at the same time. This effect will cause large instantaneous switching energy.

PLECS calculates this loss by a function containing pre-, post-switching conditions and device temperature, i.e., E_{on}=f(v_{block},i_{on},T) and E_{off}=f(v_{block},i_{off},T). These two functions are defined in the tabs 'Turn-on loss' and 'Turn-off loss' of the 'Thermal Description" as 3D look-up tables. E_{on} and E_{off} curves of the power module can be seen from Figure B.2(a) and Figure B.2(b).

Appendix C

Simulation Models

Simulation analysis was primarily done with MATLAB/SIMULINK and PLECS. The following were the models created in the Simulink/PLECS environment to support the research work of this thesis.

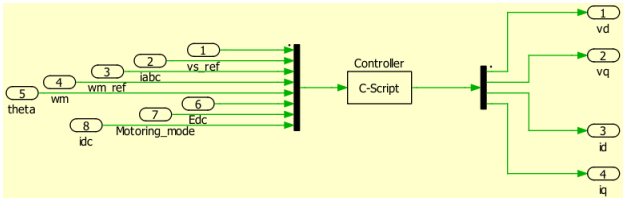


Figure C.1: Control model of the ESG system

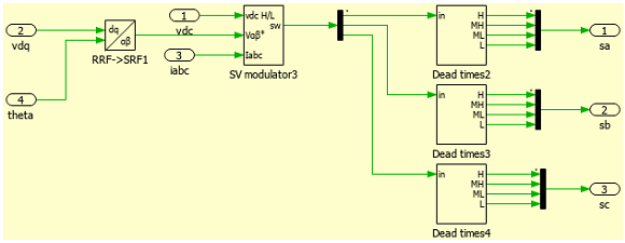


Figure C.2: Modulation model of the 3L-NPC converter

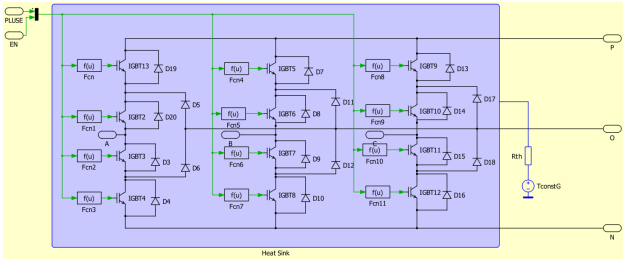


Figure C.3: Thermal model of the 3L-NPC converter

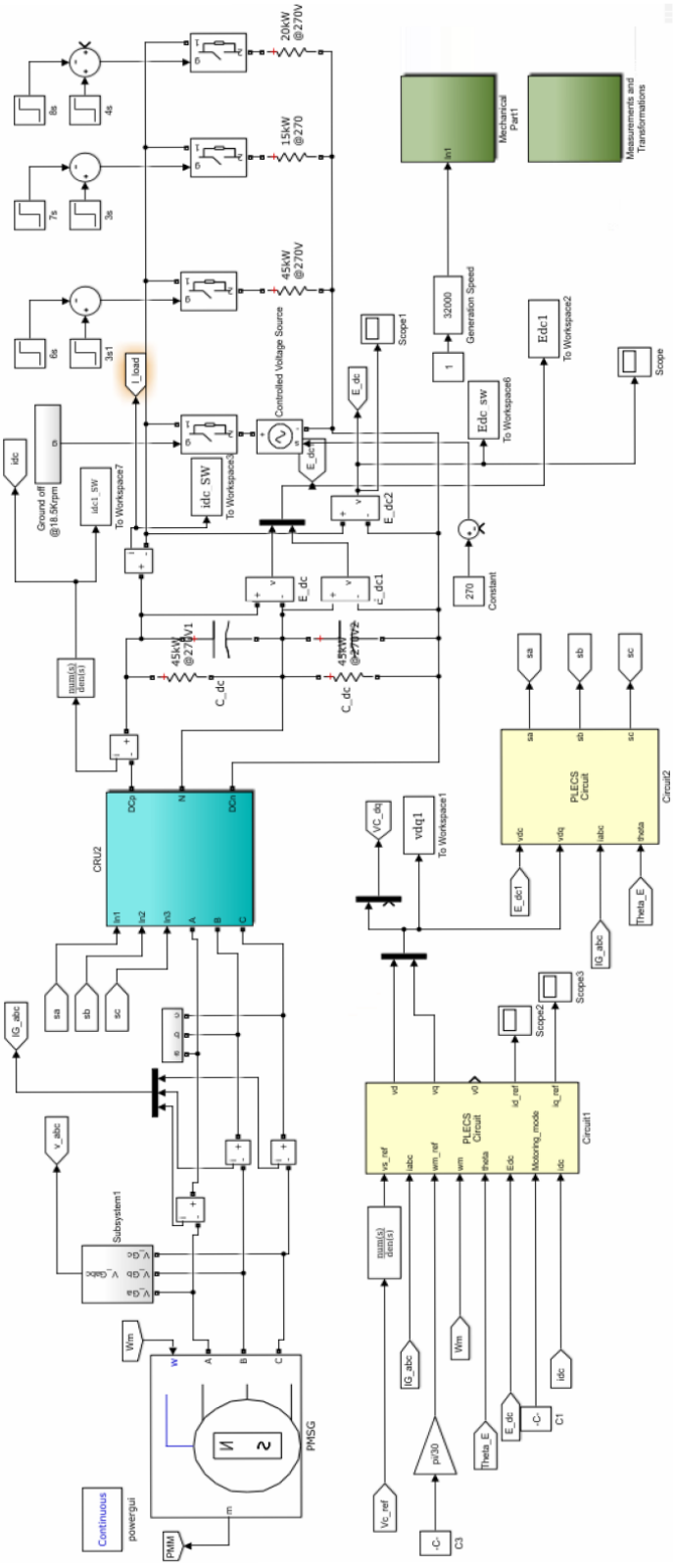


Figure C.4: Simulation model of the aircraft ESG system