

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Modelling, Fabrication, and Characterization of Memristor for Mitigating the Sneak Path Current in a Nano-Crossbar Memory Array

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List of Abbreviations

Abbreviation	Description
NVM	Non-Volatile Memory
MIM	Metal-Insulator-Metal
RRAM	Resistive Random-Access Memory
VCM	Valance Change Memory
ECM	Electrochemical Metallization Memory
RS	Resistive Switching
BRS	Bipolar Resistive Switching
HRS	High Resistance State
LRS	Low Resistance State
CRS	Complementary Switching Memory
1S1R	One Selector- One Resistor
SMU	Source Measurement Unit
SCLC	Space Charge Limited Conduction
CF	Conductive Filament
OCF	Outside Conduction Filament
ALD	Atomic Layer Deposition
FNT	Fowler Nordheim Tunneling
FESEM	Field emission scanning electron microscopy
EDX	Energy-dispersive X-ray technology
VCCS	Voltage-Controlled Current Source
VCVS	Voltage-Controlled Voltage Source
SMU	Source measurement Unit
SEM	Scanning electron microscope
EDX	Energy dispersive X-ray spectroscopy

List of Publications

Book Chapter:

1. Electrical modeling of one selector- one resistor (1S1R) for Mitigating the Sneak Path Current in a Nano-Crossbar Memory Array –for the book titled "Nanoelectronics for Next-generation Integrated Circuits" to be published by CRC Press (In press)

Peer reviewed Journals:

2. Jagath, A.L., Leong, C.H., Kumar, T.N., et al.: 'Insight into physics-based RRAM models – Review', **IET Journal of Eng.**, 2019, 2019, (7), pp. 4644–4652.
3. Arya Lekshmi Jagath, T. Nandha Kumar, Haider A.F. Almurib, K.B. Jinesh "Analytical modeling of tantalum/titanium oxide-based multi-layer selector to eliminate sneak path current in RRAM arrays," **IET Circuits, Devices & Systems**, ISSN 1751-858X, doi: 10.1049/iet-cds.2019.0480
4. Jagath Arya Lekshmi, T. Nandha Kumar, K.B. Jinesh," Multilevel non-volatile memory based on Al_2O_3/ZnO bilayer device," **IET Micro & Nano Letters**, pp. 1–5 doi: 10.1049/mnl.2020.0335.
5. Arya Lekshmi, T. N. Kumar, K.B Jinesh," Self-limited Bipolar Au/ Al_2O_3/ZnO/FTO RRAM and its comparison with Ag/ Al_2O_3/ZnO/FTO devices", **Elsevier's Microelectronic Engineering,** Volume 250,2021,111637,ISSN 0167-9317,https://doi.org/10.1016/j.mee.2021.111637.

Conferences:

6. A. L. Jagath, T. N. Kumar and H. A. F. Almurib, "Electrical model of Ta_2O_5/TaOx RRAM device with current conduction beyond RESET phase," 2019 **IEEE** 9th International Nanoelectronics Conferences (INEC), Kuching, Malaysia, 2019, pp. 1-5, doi: 10.1109/INEC.2019.8853845.
7. A. L. Jagath, T. Nandha Kumar and H. A. F. Almurib, "Modeling of Current Conduction during RESET Phase of Pt/ Ta_2O_5/TaOx/Pt Bipolar Resistive RAM Devices," 2018 **IEEE** 7th Non-Volatile Memory Systems and Applications Symposium (NVMSA), Hakodate, 2018, pp. 55-60, doi: 10.1109/NVMSA.2018.00014.
8. A. L. Jagath and T. N. Kumar, "A comparative study on the performance of 1S1R and Complementary resistive switching models," 2020 IEEE International Conference on Semiconductor Electronics (ICSE), Kuala Lumpur, Malaysia, 2020, pp. 9-12, doi: 10.1109/ICSE49846.2020.9166874.(**IEEE Best paper award ICSE 2020**)
9. Arya Lekshmi., T. N. Kumar, A. F. Haider, and K. B. Jinesh, "Implementation of sub-filamentary network-based variability model for Ta2O5/TaOx RRAM," 2021 IEEE 21st International Conference on Nanotechnology (NANO), 2021, pp. 366-369, doi: 10.1109/NANO51122.2021.9514298.
10. Arya Lekshmi, T. Nandha Kumar, A. F. Haider, and K. B. Jinesh, "Self-rectifying self-limited Resistive switching in Au/Al2O3/FTO Devices," 2021 IEEE 21st International Conference on Nanotechnology (NANO), 2021, pp. 17-20, doi: 10.1109/NANO51122.2021.9514299.

11. Amr Nabil, Arya Lekshmi, T. Nandha Kumar and A. F. Haider, ”Effect of Sneak Path Current in TiO_x/HfO_x Based 1S1R RRAM Crossbar Memory Arrays”, IEEE Student Conference on Research and Development (accepted in SCOReD 2021).

Manuscripts Submitted and in review:

12. Complementary Resistive Switching in ZnO/ Al_2O_3 bi-layer devices, IEEE Transaction on Nanotechnology.

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ABSTRACT

The semiconductor industry looks ahead to Resistive random-access memory (RRAM), (alternatively known as memristor), a promising emerging non-volatile memory technology that can be developed to become a solution for high-density data storage problems. However, the formation of crossbar arrays with RRAM devices results in the origin of leakage current from the unselected cells known as sneak path current, which is identified as the major hindrance to the development of RRAM as it adversely affects data integrity. Among various prevailing solutions to mitigate sneak path current, the effective methods are incorporating a selector switch in association with the memory device to form one selector-one resistor (1S1R) configuration and complementary switching (CRS) devices formed by back-to-back connected RRAMs.

Even though the experimental results of several one selector -one resistor (1S1R) are reported, physical/electrical mechanisms explaining the working of such device integrations are missing; hence the first part of this research work focuses on the analytical/electrical model of a selector device and selector -RRAM integrated device (1S1R) architecture to demonstrate the working of devices and to illustrate how effective is a selector switch in mitigating the sneak path current. The selector device chosen to model is a tri-layer Pt/Ta_2O_5/TaO_x/TiO_2/Pt stack with nonlinear characteristics. The model is developed with the concept of electron tunneling across the nanoscale multilayer stack, derived using energy band theory. The current conduction in the proposed selector model is devised with the electric field-driven tunneling mechanisms that co-exist in thin multi-layer devices such as Fowler Northeim tunneling and direct tunneling/hopping. From the simulated selector characteristics, it has been noticed that below the threshold voltage (~0.7 V), the model shows low leakage current attributing to the open switch, while at an input voltage >1.2 V, the current profile exponentially increases attributes to closed switch behavior. The resulting I-V characteristics of the selector model can reproduce desired selector properties such as high non-linearity (~1600), high selectivity (~10^4), high current density (~10^7 A/cm^2), and low OFF-current (~46 nA) in agreement with the measured device characteristics.

In addition, the proposed selector model is integrated with established RRAM models such as HP memristor, Pt/Ta_2O_5/TaO_x/Pt RRAM (SAMSUNG), TiN/TiO_x/ HfO_2/Pt (Stanford-PKU) model, and generalized RRAM device models proposed by Yakopcic to demonstrate the reduction in sneak path current achieved. Among these models, the proposed selector with

$TiN/TiO_x/HfO_2/TiN$ model reduced 99.8 % of the sneak current at low dimensional arrays, whereas the reduction in sneak current with HP memristor and $Pt/Ta_2O_5/TaO_x/Pt$ model are 96% and 98% respectively. Moreover, it is noticed that V/3 based scheme is more suitable for performing read/write in a nano-crossbar array among various writing schemes.

Several RRAM and selector model parameters are inherited to the 1S1R model, thus enabling it to reduce sneak path current. For instance, the nonlinear selector characteristics are directly reflected on the 1S1R curves, ensuring the reduction in sneak path current. The nonlinearity of Ta_2O_5/TaO_x, TiO_x/HfO_x, TiO_x/TiO_{x-2} are ~2, ~5, and ~5, respectively, while their corresponding 1S1R models exhibited 50, 20, and 55, respectively. Similarly, the Roff/ Ron ratio of RRAM is directly absorbed to 1S1R. Further, the Roff/Ron ratios obtained with 1S1R configuration of Ta_2O_5/TaO_x, TiO_x/HfO_x, TiO_x/TiO_{x-2} are ~400,~100, and 15, respectively. Likewise, another parameter that determines the sneak current reduction is off-current in 1S1R. Low OFF-current is another desirable factor to eliminate the sneak current. The selector- $Ta_2O_5/TaOx$ combination provided off-current as low as 0.04 μA whereas 1S1R with Stanford PKU model is 8 nA and 1S-HP memristor combination is 0.01 μA. In addition, the optimum input voltage required to assert on selected/ unselected crossbar array lines to attain SET and RESET voltages are predicted. In $Pt/Ta_2O_5/TaO_x/TiO_2/Pt$ selector- $Pt/Ta_2O_5/TaOx/Pt$ RRAM integrated circuit, SET/RESET voltage is falling within ~2.7-3.6 V/>=~4.4 V whereas in HP and Stanford model these readings are approximately 3.5/-3.7 V and 2.5/-3.0 V respectively.

While in $Pt/Ta_2O_5/TaO_x/Pt$ device model, it has been observed that its experimental I-V characteristics show an increase in current level beyond RESET voltage. However, it has not been addressed in the existing analytical/ electrical models. Hence, an analytical and electrical model has been proposed to incorporate the increased current conduction by considering an additional state-independent current component that flows through the area outside the conduction filament(OCF). The current component is modeled by the trap assisted tunneling (TAT) mechanism, where the oxygen vacancy traps present at OCF enable the electrons to tunnel through that area. Moreover, the variability in the $Pt/Ta_2O_5/TaOx/Pt$ device characteristics over multiple cycles of input is also explained and simulated by considering three possible factors such as multifilament formation in the device, variation in the radius of the conduction filament(CF), and variations in tunneling barrier height.

Next, a comparison of the sneak path current reduction in the 1S1R array and CRS array is carried out, where CRS reduced 93% of the total sneak path current compared to 1S1R. Analysis shows that 1S1R outperforms the CRS model (back-to-back connected RRAM) configuration. The major challenges noticed with the configuration of 1S1R are the shared electrode, compatibility of current /voltages of the chosen selector, and RRAM device. Similarly, the drawbacks identified with CRS devices formed with back-to-back connected RRAM devices are; the presence of the shared electrode at the middle of switching layers, related complicated process flow, and interface issues due to multiple metal-semiconductor junctions.

Therefore, a novel bilayer stack fabrication with CRS functionality is proposed in the second part of the research. The proposed CRS stack is implemented with two switching layers (bilayer) thus, eliminating the need for a shared electrode. In the CRS design, atomic layer deposition (ALD) and thermal evaporation methods are exploited to deposit the switching and electrode layers, respectively. The proposed CRS stack has Au/ZnO/Al_2O_3/FTO structure, and its characteristics are analyzed to validate the complementary switching. The stable CRS state of the device exhibits a high current of ~500 µA during the ON-state and a low current of 300 nA during OFF-state at low input voltages ranging from -0.5 V to 0.5 V, which enables the proposed device to use in crossbar array to mitigate the sneak path current. The device performance to write and read processes is evaluated with pulses of magnitudes ~|2.5| V and 1.3 V, respectively, and a ~ 60µA difference in read-out current between data bits 0 and 1 is noticed. Also, the power dissipation was in the range of microwatts enabling the device to use in medium power applications. The CRS switching in the proposed device is reported to be due to redistribution of oxygen vacancies spanning in both ZnO and Al_2O_3 layers based on the electric field distribution. In addition to this, the major current transport mechanism in the proposed device is identified as the space charge limited conduction (SCLC).

Analysis shows that self-rectifying memristor with Au/Al_2O_3/FTO (MIM) structure is the most promising device used in crossbar array to mitigate the sneak path current. In addition, a recently trending self-rectifying RRAM device is fabricated with Au/Al_2O_3/FTO, metal-insulator-metal (MIM) structure which gives a 1D1R kind of characteristics with the rectification ratio of 200, is a promising value for reducing sneak current. Moreover, the device has shown a specific characteristic of non-zero cross-over phenomenon reported due to the asymmetric MIM structure's capacitive nature. Also, it is reported that the device can be biased appropriately to obtain analog or digital characteristics.

Furthermore, a conductive bridge RRAM (CBRAM) and a resistive random-access memory (RRAM) device are developed to study their performance with a selector device(1S1R). The CBRAM is created from Al_2O_3/ZnO/FTO stacking with Ag top electrode, which shows the multilevel capability enabling the device to be used in high-density memory applications. The novel multilevel device has shown five distinct states achieved with voltage levels that differ at least ~0.7 V between them. Among five distinct memory states, three resistive states are attained with RESET voltages, and two are attained with SET voltages. The distinguishable resistive levels obtained with RESET voltages 2.3, 3.0, and 3.8 V are 1300, 2700, and 4320 Ω, respectively, whereas two stable resistive levels attained with SET voltages 0.8 and 1.70 V are 3000 and 100 Ω, respectively.

Moreover, the proposed device excels in its Roff/Ron ratio of 354 obtained with HRS/LRS and the ratio of intermediate states IRS1, IRS2, IRS3 to HRS becomes 15, 04 and 27, respectively. The multilevel property of the device is explained after the formation and rupture of multiple metallic filaments. Finally, the cycle-to-cycle and device-to-device variability in device characteristics and statistical distribution of their resistance levels are also analyzed. Then the device is hypothetically connected with Pt/Ta_2O_5/TaO_x/TiO_2/Pt selector to obtain 1S1R architecture with multilevel functionality, which gives a Roff/Ron ratio of 10^2 and the non-linearity of ~25, as well as off-current in the order of nano Amperes enable it to use in crossbar array along with selector.

For conducting a theoretical study with the selector device (1S1R), a RRAM device is also fabricated with Au/Al_2O_3/ZnO/FTO stack, which shows bipolar resistive switching behavior with excellent retention and endurance(>10^3)and has offered Roff/Ron ratio of ~200. In contrast, the hypothetical 1S1R configuration of the RRAM device gives a Roff/Ron ratio of 10^4. Similarly, the non-linearity obtained from combined architecture (hypothetical) is ~100. Moreover, the off-currents observed in both multilevel-CBRAM and RRAM are negligibly low in the range of nano Amperes. All these values indicate the efficiency of the devices to be used in crossbar arrays to mitigate sneak path current.

Chapter 1

Introduction

In the digital era, data explosion due to the latest trends such as big data analytics, cloud computing, artificial intelligence, and neuromorphic computing demands efficient memory technology. To cater to such a high data processing demand, prevailing memory technologies like DRAM, SRAM, and NAND have been continuously superseded with better technologies such as SDRAM, 3D NAND, and currently emerging non-volatile memories[1]–[5]. Generally, as shown in Fig. 1.1, semiconductor memory technologies can be broadly classified as volatile and non-volatile. Among the non-volatile memory technology, the emerging memory technologies such as Phase-change memory (PCM), Resistive Random-Access Memory (RRAM or Memristor), Spin transfer torque magnetic random-access memory (STT RAM), Racetrack memory, Ferroelectric random-access memory (FeRAM), and Magnetoresistive random-access memory (MRAM) exhibit best features such as CMOS compatibility, scalability beyond the present limits of SRAM and FLASH memories, also expected to have features like non-volatility, high speed, high density, low cost, and low power.

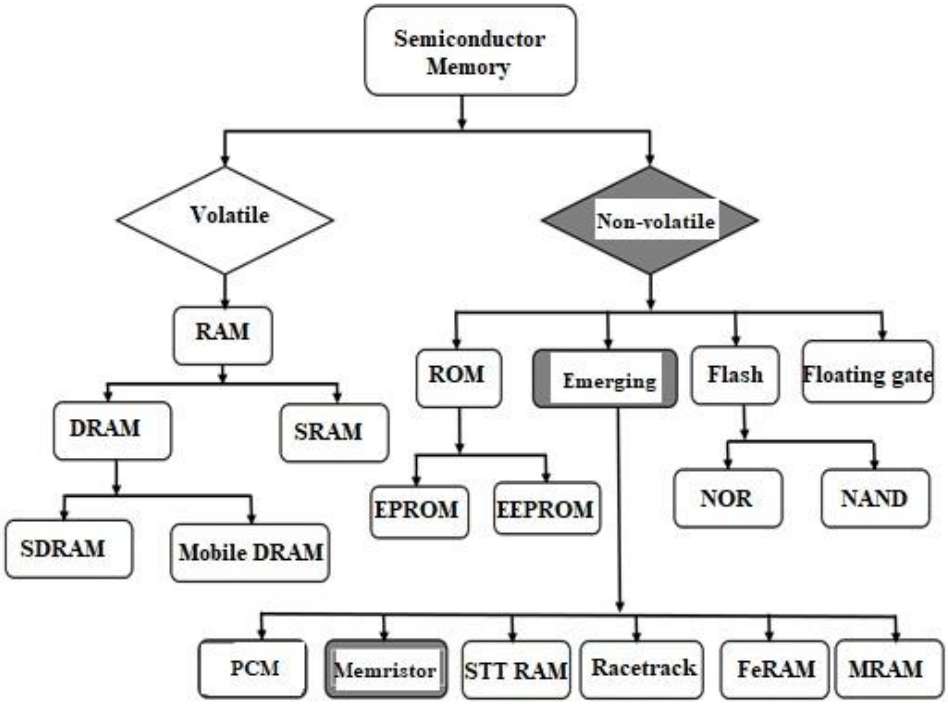


Fig. 1.1 Classification of semiconductor memory technologies

Among the emerging non-volatile memory technologies, as illustrated in Table 1.1, RRAM outperforms other emerging non-volatile devices due to its high memory density, low energy density per bit, fast READ/WRITE time, low operating voltages, nanoscale dimension, high endurance and high Roff/Ron ratio. In addition, RRAM provides promising reliability measures such as endurance and retention compared to its counterparts. Compatibility with the CMOS is another feature that makes it distinguishable among other emerging memory technologies such as PCM, MTT-RAM, etc. [6][7]. Therefore, RRAM is considered as the potential successor to the 3D NAND [8]. In the following section, the basics of the RRAM technology and its recent research development have been presented.

Table 1.1. Comparison of various parameters across different emerging non-volatile memory devices[9].

	Memristor	PCM	STTRAM	DRAM	Flash	HDD
Density(F^2)	4	8-16	14-64	6-10	4-6	2/3
Energy per bit (pJ)	0.1-3	2-27	0.1	2	10000	$1\text{-}10\text{x}10^9$
Read time(ns)	<10	20-70	10-30	10-50	25000	$5\text{-}8\text{x}10^6$
Write time(ns)	~20	50-500	13-95	10-50	200000	$5\text{-}8\text{x}10^6$
Retention	years	years	Weeks	<<second	years	years
Endurance (cycles)	$>10^{12}$	10^7	10^{15}	10^{16}	$10^3\text{-}10^6$	10^{15}

2.1 Resistive Random-Access Memory (RRAM) technology- background and current research development

Resistive random-access memory (RRAM) had been first postulated by Prof. Leon Chua in 1971 [10][11][12], and the first prototype was developed in HP labs[13]. RRAM is a two-terminal device with its functionality based on resistance switching (RS) mechanism, where the device exhibits two different resistance levels controlled with current or voltage. The current-voltage characteristics of the memristor show a closed hysteresis behavior that retains the memory. The hysteresis loop exhibited by the HP memristor device with $Pt/TiO_2/Pt$ structure is shown in Fig. 1.2.

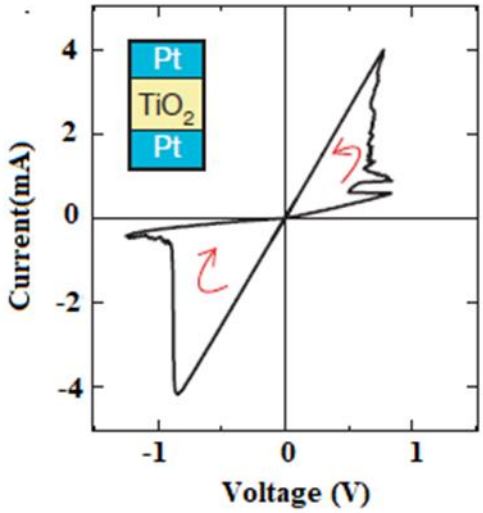


Fig. 1.2. I-V characteristics obtained from Pt/TiO_2/Pt HP memristor device.[14]

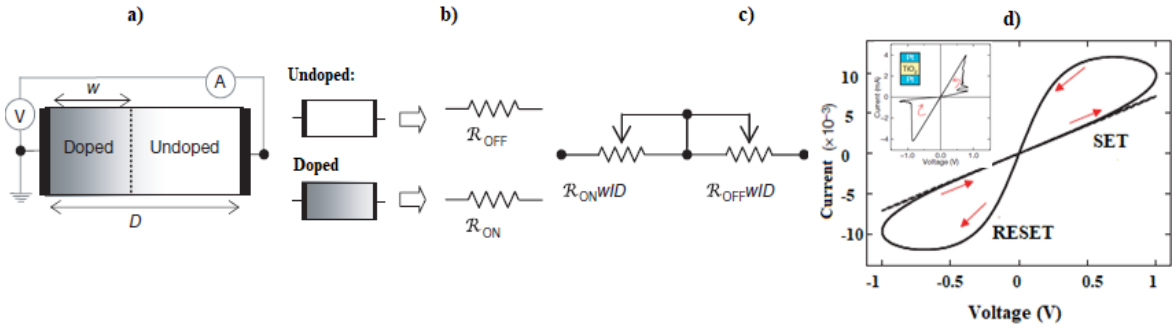


Fig. 1.3 Basic working of HP memristor model a) model showing with doped and undoped region b) equivalent resistance of doping regions c) moving boundary between doped and undoped region d) I-V characteristics obtained from the model(inset showing corresponding actual characteristics obtained from the device)[15]

A variable resistor model of the memristor device proposed by HP labs is illustrated in Fig. 1.3, where the device structure consists of a thin oxide film of thickness D sandwiched between two metal contacts to form a metal-insulator-metal (MIM) structure as shown in Fig. 1.3 (a). The device structure is divided into two regions: high dopant concentration (marked as doped in the figure) and low dopant concentration (marked as undoped in the figure). The concentration of dopants in the film affects the resistance of that region. That is, the highly doped regions show low resistivity, and less doped region shows high resistivity; hence the total resistance of the device is contributed by two variable resistors connected in series. The resistance values of the variable resistors Ron and Roff are shown in Fig. 1.3(b). The application of an external bias v(t) across the device moves the boundary between the two resistance regions due to the charged dopants drift as depicted in Fig. 1.3(c); thus, the model

showed a hysteresis curve for current-voltage characteristics as given in Fig. 1.3(d), (the inset shows the I-V characteristics obtained from the actual device).

However, to attain the hysteresis behavior, the device requires some atomic rearrangement that modulates the electronic current. Here the atomic arrangement refers to the movement of oxygen vacancies across the semiconducting film. In the given device, the device switch to ON-state with the application of a positive voltage and the state of the device is referred to as low resistance state (LRS), and switches back to OFF-state with the application of a negative voltage. The OFF state of the device is referred to as a high resistance state (HRS). The device remains in the ON-state as long as a positive voltage is applied, and with a negative bias, it will switch back to the OFF-state[16] .

Later, the evolution of the RRAM device continued with different materials such as transitional metal oxides and organic metal oxides such as Ta_2O_5, Al_2O_3, HfO_2, NbO_2, and graphene. In addition to the development of simple metal-insulator-metal (MIM) structure as shown in Fig. 1.4(a)[14], [15], memristor devices are developed with bilayer (Fig. 1.4 (b)) as well as multilayer stacking morphology (Fig. 1.4(c)). The bilayer device structure is created with the metal-insulator-semiconductor-metal (MISM) stacking, where two layers can be made of the same metal oxide with its stoichiometric and sub-stoichiometric phases [17]or bilayers can be made from hetero oxides[18], [19]. If a RRAM device is designed with more than two resistive switching layers, it is called a multilayer device[20].

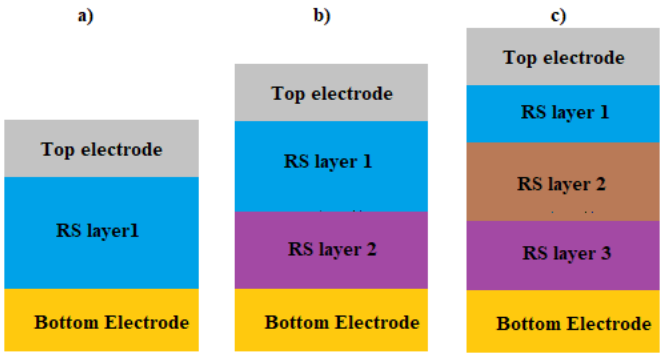


Fig. 1.4 Structure of RRAM devices a) single layer MIM structure b) bilayer structure with two resistance switching layers c) Multilayer structure with multiple resistive switching layers.

Yet another classification of RRAM memory is based on the type of the switching element; it can be valance change mechanism (VCM) based oxide-RRAM (ox-RRAM) and metallic cations-based conduction bridge RRAM (CBRAM) memories. In addition, based on

the nature of the current profile variation with the input voltage, RRAM devices can be of two types, analog or digital. The analog devices show analog I-V characteristics where the switching (transition) between states is gradual. On the other hand, devices exhibiting digital characteristics show abrupt switching process. According to the nature of device characteristics, the memristive devices can be used in various applications[21], [22]. For instance, the analog memristor is suitable for neuromorphic applications. It emulates the step-by-step spiking of neurons, whereas for digital applications, abruptly switching digital memristive devices is beneficial. In addition, RRAM is gaining momentum in the field of emerging non-volatile memory industry owing to its versatility in applications such as its ability to be used in in-memory computing technologies, storage systems, realizing Boolean logic functions such as NAND, NOR, etc., look-up table (LUT) for FPGA and sequential circuit implementations such as D-latch, implementation of reconfigurable logic operations, crossbar adders, etc. [23], [24], [25]. All these applications use high-density RRAM memory structures where RRAMs should be connected in nano-cross bars.

Even though the technology is in its research and development stage, progressions achieved in the last few years are remarkable. SanDisk Corporation has demonstrated a 32Gb RRAM test chip with a 24 nm CMOS process in 2013. In 2014, researchers at IMEC and Panasonic had created a 2-Mbit chip made of 40nm node with $Ir/Ta_2O_5/TaO_x/TaN$ structure. Further, a 16Mb array of HfO_x/TaO_x bi-layer RRAM stack was reported in 2015. In addition, 'Crossbar' has been reported a 4-Mbit 1S1R chip and 1T1R IP cores. The proposed built-in selectors targeted for high-density memories are useful in data centers, and their applications include machine learning neural networks [4]. Another milestone is laid by IBM is the proposal of a Resistive processing unit (RPU) for the storage and processing of data to improve deep neural network training (DNN) [26]. Further in 2018, The Intel corporation introduced the non-volatile Optane DIMM with 3DXpoint technology (shown in Fig. 1.5), which is considered another milestone for the non-volatile technology[4]. Moreover, it recently reported that RRAM devices are used in the internet of things (IoT), artificial intelligence (AI), and data center storage. However, all these devices are in the research phase, and none of them reached the consumer market yet.

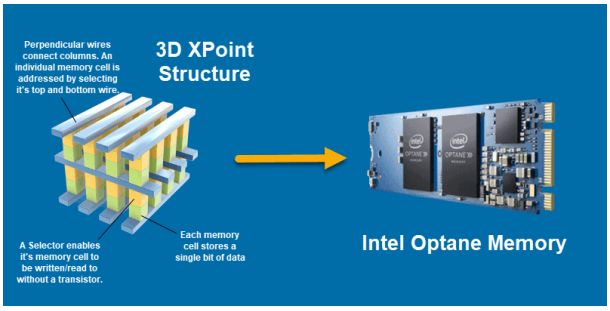


Fig. 1.5 Intel Optane Memory developed with 3DX structure [4]

Fig. 1.6 gives an insight into the current state of research and milestones to reach over the foreseeable future. Since the technology is still in its infant stage and as time progresses, the potential memristive device will replace Flash technology and DRAM to use it as a universal memory to use in storage and high-end applications like neuromorphic computing [8]. As such, the current development of RRAM technology opens up potential research opportunities resulting in the research motivation of the presented thesis, and those are discussed in the next section.

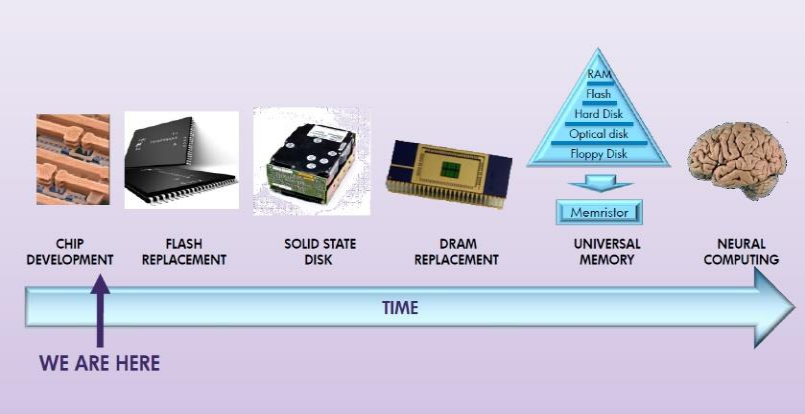


Fig. 1.6 The current state of memristor research and milestones to reach over the foreseeable future [8]

Note: Throughout this thesis, the term ‘memristor’ will be replaced with the more specific term ‘Resistive random-access memory (RRAM).

2.2 Research Problem and Motivation

Dense RRAM memory is attained by configuring devices 2D or 3D nano crossbar arrays (CBA). A nano crossbar array consists of horizontal word lines and

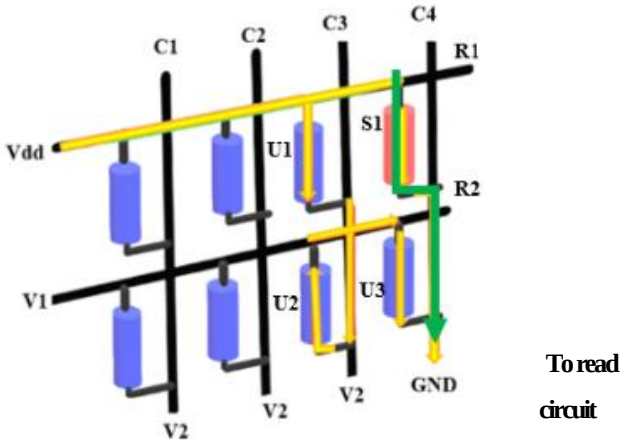


Fig. 1.7. A simple crossbar array of RRAMs showing the traces of sneak path current (solid yellow line), actual expected current (solid green line)

vertical bit lines where the bidirectional memory element sits between their cross points [27]–[29]. The major challenge with RRAM devices while forming array is the leakage current; this unforeseen current component is known as sneak path current, which originates due to the low resistance path offered by the unselected cells remain in its low resistance state (LRS) in the crossbar array. An example of a crossbar array is shown in Fig. 1.7 where the vertical bit lines are C1, C2, C3, and C4, and horizontal word lines are denoted with R1 and R2. Note that in Fig. 1.7, Vdd is applied to the selected word line, and the selected bit line is connected to ground potential. In the figure, V1 and V2 are arbitrary voltage biases, and their magnitude depends on the adopted writing scheme.

In Fig. 1.7, the red-colored cell denotes the selected RRAM (S1), and all blue cylinders denote the unselected RRAM cells where U1, U2, U3 are the neighboring cells which are also known as half selected cells because they share either the bit or word line of the selected cell. In this case, the worst-case scenario is discussed where all unselected cells are in a low resistance state and the selected cell is in a high resistance state. In this circuit, the sneak path current path emerges from R1 to U1; then the current flows to the C3 bit line. Subsequently, the current takes a path towards the R2 row through the unselected cell U2. Finally, it flows to the C4 column through unselected cell U3 and then flows to the read circuit. Thus, the sneak current path is Vdd-U1-U2-U3 to read the circuit, whereas the actual expected current through the selected cell (S1) is shown with solid green lines. In this case, the current flows from the

R1 row to the C4 column through the selected cell and finally reaches the read circuit or sensing circuit. Thus, resulting in an erroneous read current of the selected RRAM cell. Also, the sneak path current, when flowing through the unselected RRAM cells (U1, U2, U3), changes the memristance (or state) of the respective RRAM cell, thereby corrupting the data stored in the unselected RRAM cells.

Various techniques are employed to circumvent the problem of sneak path current, such as complementary resistive switching (CRS) devices [8, 9] and selector devices [10, 11]. To date, many selector devices such as diodes [21], transistors [22], [23], and volatile bi-layer devices are reported to use in association with RRAM. Nevertheless, the unipolar behavior of diodes and scaling concerns of transistor switches impede their use in CBA. These shortcomings of the available selector switches are overcome by proposing several non-linear selectors [24], [25], which are fabricated either as single-layer or as a multi-layer material stack with advanced engineered designs [26], [27]. Moreover, recent studies show that the selector device with a tri-layer structure provides more stable selector characteristics [20] with significant nonlinearity. Similarly, various CRS devices are also available where the most common configuration is the anti-serially connected RRAMs.

However, to test the contributions of fabricated RRAM devices, selector devices, CRS devices, on mitigating sneak path current in a nano cross bar array (either as 1S1R or CRS), physics and electrical models of those devices are required. In addition, the accuracy of the physics-based/ electrical models of the RRAM with respect to the measured RRAM characteristics is vital to analyze the functionality of such devices when connected with other devices. Because of this, last few years, several analytical models have been developed to simulate the characteristics of filamentary type RRAM devices [30], [31], [32] (where the current conduction and corresponding switching process is explained after the formation of a conduction filament (CF)). The physics-based model of the most common RRAM device $Pt/Ta_2O_5/TaO_x/Pt$ presented in [31], [32], demonstrates the Schottky current conduction through the conduction filament of the RRAM device. But such models consider only the current conduction through the conduction filament of the Ta_2O_5 RRAM device and completely ignores the current conduction outside the conduction filament (OCF) [33]. The current conduction outside the filament has significant implications in the device's characteristics, particularly when the voltage is increased beyond the reset voltage at which the RRAM device turns to a low resistance state even though it is expected to be at a high resistance state. Thus, providing an opportunity to explore the reasons for the additional current component and the

influence of OCF on this additional current, which lights to the development of a robust analytical and corresponding electrical model of the $Pt/Ta_2O_5/TaO_x/Pt$ RRAM cell. In addition to this, the variability of the RRAM device with respect to the radius of the conduction filament is an open area for research that requires to be incorporated in the device model for the model to behave close to the RRAM device characteristics.

Next, to analyze the contribution of a selector switch on the RRAM device, a few fitting models of multi-layer selectors are prevailing[34], [35], though a proper physics-based model and electrical-based model are not available, providing another open area of research. Besides, selecting and modeling a selector device and a compatible RRAM device to use it in the nano-cross bar to mitigate the sneak path current is also another challenge. Hence the detailed study of one selector-one resistor (1S1R) duo is highly required in this context.

As mentioned above, in addition to 1S1R, an alternative technology to mitigate the sneak path current is available, known as the complementary resistive switching (CRS) devices where an individual device is configured with two RRAM devices connected in a back-to-back manner, though major challenge found with such a device configuration is its poor design due to deposition of the metallic electrode between the switching layers and formation of multiple metal-semiconductor junctions. Therefore, it is thought-provoking to investigate alternate CRS fabrication technologies by stacking of multiple switching layers or by depositing a single switching layer with a focus to obtain the CRS characteristics.

Furthermore, it is interesting to contemplate how the device characteristics change with stack ordering and the effect of different electrode material with similar switching layer stacks, what are different strategies to optimize a RRAM device, etc. Therefore, further advancement of RRAM technology needs the optimizations and profound study on bilayer and multilayer structures, 1S1R integration technology, and CRS configurations.

2.3 Aim and objectives of the research

1.1.1. Aim

The research aims to develop accurate physics and electrical-based models of the potential Ta_2O_5/TaO_x RRAM device and selector devices and integrate them to develop an appropriate 1S1R model to effectively mitigate the sneak path current in a nano-cross bar memory array. In addition to this, as an alternate method to 1S1R, the CRS configuration to be developed utilizing accurate physics and electrical models of

RRAM devices. Further, the CRS configuration device to be fabricated and its characteristics with stack ordering and the effect of different electrode material with similar switching layer stacks and optimization of the device to be analyzed.

1.1.2. Objectives

1. To develop an insight on the resistive switching and current conduction behavior of various RRAM devices and analyze the parameters required to realize the analytical as well as electrical RRAM and selector models. Then, to develop accurate physics and circuit models of Pt/Ta_2O_5/TaO_x/Pt RRAM device by incorporating the current conducting through outside of the conduction filament (OCF) during RESET phase. To analyze the influence of the parameters such as barrier height, the radius of filament, geometry of the filament on the variability of Pt/Ta_2O_5/TaO_x/Pt RRAM device characteristics by analytically modeling its cycle-to-cycle variability.
2. To develop an accurate analytical and electrical model of the tri-layer Pt/Ta_2O_5/TaO_x/TiO_2/ Pt selector device in order to realize an integrated model of 1S1R.
3. Develop an electrical as well as an analytical model of single and crossbar array of 1S1R cells by integrating the proposed selector model with RRAM models and study the acquired features of the 1S1R model to ensure its potential to reduce the sneak path current, derive necessary electrical parameters, and evaluate its performance in reducing the sneak path current. Also, analyse the versatility of the developed selector model to adapt with various RRAM models by integrating it with other existing electrical RRAM models such as HP, Yakopcic, and Stanford.
4. To compare the performance of 1S1R with the CRS model, realize the electrical model of the 2x2 array of CRS devices and compare with the 2x2 array of 1S1R devices to analyze how effective both circuits are in reducing the sneak path currents.
5. Fabricate and characterize RRAM device with a single switching layer and an inactive top electrode to obtain the memory characteristics. Further, design for a CRS device by stacking the proposed device with two active switching layers and performing its characterization. Also, optimize the proposed CRS device structure by varying the thickness of active switching layers. Moreover, study the effect of changing the order of switching layer stack and electrode material (use active

electrode) on device characteristics. Further, study the effect of sneak path current in multilevel memory.

2.4 Research Outcomes

a) Accurate physics and electrical model of $Pt/Ta_2O_5/TaO_x/Pt$ device by incorporating the current conduction in OCF and cycle-to-cycle variability analysis involving parameters such as barrier height, the radius of filament, the geometry of the filament.
b) Accurate analytical model and electrical model of the tri-layer $Pt/Ta_2O_5/TaO_x/TiO_2/$ Pt selector device.
c) Electrical model of 1S1R memory cell and its influence in mitigating the sneak path current in a low dimension crossbar array.
d) Electrical model of CRS memory cell and its influence in mitigating the sneak path current.
e) Evaluation of 1S1R and CRS cells' contributions on reducing the sneak path current.
f) Fabrication and characterization of the counter parts of RRAM and CRS models using available materials(Al_2O_3 and ZnO) and evaluate their effectiveness in reducing the sneak path current.
g) Design/fabricate the counter parts of $Pt/Ta_2O_5/Pt$ and $Pt/Ta_2O_5/TaO_x/Pt$ RRAM models such as $Au/Al_2O_3/FTO$ and $Au/Al_2O_3/ZnO/FTO$ to integrate with selector (considering that each layer has similar functionality).
h) Then, to avoid poor design of conventional CRS devices; propose, fabricate, and characterize a novel bilayer CRS device with $Au/ZnO/Al_2O_3/FTO$ stack to use in crossbar array to reduce sneak path current. Moreover, develop multilevel RRAM device based on $Ag/Al_2O_3/ZnO/FTO$ to combine with selector to utilize in high-density memory applications.

2.5 Thesis Outline

Chapter 1: It is an introductory chapter explaining the basics of RRAM devices, their advantages, and recent advancements in the field. Also, the Aim and objective of the research, to develop the models and devices, and finally, the research outcomes are also summarized.

Chapter 2: This chapter deals with preliminary concepts associated with RRAM devices such as electroforming, resistive switching, and various conduction mechanisms are discussed.

Further, various physics-based RRAM models are also reviewed. Then, RRAM memory devices' classification is described and introduces the basic terminologies associated with RRAM technology. After that, the existing examples of selector-RRAM as well as CRS devices are discussed; last part of the chapter includes the research gaps identified in the field.

Chapter 3: This chapter discusses the methodologies followed to develop selector, RRAM,1S1R analytical models, methodologies adopted to develop electrical models, and then described the steps and procedures to follow the fabrication of RRAM

Chapter 4: This chapter deals with the analytical and an electrical model of Pt/ Ta_2O_5/TaO_x/Pt RRAM device incorporating the effect of current conduction present at outside of the conduction filament area. Further, the simulated characteristics are validated with experimental results.

Chapter 5: In this chapter, the details of analytical and electrical models of $Pt/Ta_2O_5/TaO_x/TiO_2$/Pt selector device, its characteristics, parameters derived, and its comparison with existing selector models are included.

Chapter 6: This chapter outlines the integration of analytical and an electrical model of selector device with RRAM models, formation of 2x2 crossbar arrays, and sneak current measurements. The last part of the chapter discusses the implementation of an electrical model of CRS and its comparison with different 1S1R models and compares the performance of both configurations.

Chapter 7: This chapter explores the electrical characterization, structural characterization, and performance measures of the fabricated Au/Al_2O_3/ FTO RRAM device and $Au/ZnO/Al_2O_3$/ FTO CRS device. Then, various parameters are measured and evaluated from the device characteristics. Also, a theoretical study on device conduction and switching mechanism are conducted.

Chapter 8: This chapter illustrates the fabrication and characterization of CBRAM and an RRAM device ($Ag/Al_2O_3/ZnO$ /FTO and $Au/Al_2O_3/ZnO$/FTO) to integrate with selector hypothetically. Also, the parameters and qualities achieved by both devices as the individual cell is studied. The device's switching dynamics, as well as reliability analysis, are discussed. Then, a comparison of the aforementioned devices is also included in the chapter.

Chapter 9: The chapter summarizes all the studies/works and studies conducted in the research work. Also, it explains all contributions of the research.

Chapter 2

Research preliminaries & Literature review

Chapter summary

The first part of the chapter discusses resistive random-access memory (RRAM) basics, elementary terminologies to specify RRAMs, and various parameters associated with nonvolatile memory. Further, the classification of RRAM devices based on the switching mechanism includes valance change mechanism, electrochemical metallization, and thermochemical mechanism are discussed. Furthermore, the modeling of RRAM devices is described, where each model comprises three major mechanisms: switching mechanism, current mechanism. The switching mechanism explains the ionic movement associated with the device responsible for memory features, whereas the conduction mechanism deals with the electronic conduction through the device. In the second part of the chapter, background study and literature review of the research problem and the study of prevailing methods to reduce sneak path current are discussed. These methods include 1D1R,1T1R,1S1R, CRS, and self-rectifying devices. Also, various comparisons among these methods are listed down. Towards the end of the chapter, the main research gaps existing with RRAM technology are investigated.

Related Publications

1. A. L. Jagath, C. H. Leong, T. N. Kumar, and H. F. Almurib, "Insight into physics-based RRAM models – review," *J. Eng.*, vol. 2019, no. 7, pp. 4644–4652, 2019, doi: 10.1049/joe.2018.5234.

The first section of the chapter discusses the research preliminaries, including the overview of RRAM devices, basic terminologies, models, and the second section describes the literature review on major technological advancements existing to mitigate the sneak path current.

2.6 Resistive random-access memory: Electroforming, basic terminologies, classification, switching mechanisms, conductive mechanisms

RRAMs are two-terminal devices made of metal oxides sandwiched between electrodes. The most frequently used electrode materials are Al, Au, Ag, Pt, TiN, FTO, etc., and metallic oxides consist of transition metal oxides (TMO) such as Ta2O5, HfO2, and semiconducting oxides as Al_2O_3, ZnO, and organic metal oxides such as graphene. Compared to conventional memory devices, a paradigm shift can be seen in the data storage of emerging RRAM, where the data/information is stored within the metallic oxides, as distinguishable resistive states governed by the resistive switching (RS) process. However, before entering to a resistive switching state, some devices require an electroforming (EF) step. Electroforming is an irreversible process that occurs in the oxide layer at a higher electric field [36] due to the electro-reduction and vacancy creation attained by applying a high voltage or high current. Generally, during EF, a high electric field set up across the dielectric results in soft dielectric breakdown so that the highly insulating material becomes conductive with the abundance of defects or oxygen vacancies. Fig. 2.1(a) shows the electroforming in Pt/HfO_x/TiN device by the application of a high electric field limited by 1 mA compliance current; it can be observed that the pristine device is highly resistive as its resistance is in $10^8\Omega$ range, whereas as after EF, the device resistance reduced to10^6 Ω [20].

However, some devices can exhibit a resistive switching process without performing the initial electroforming process. In such devices, it is observed that the initial resistance is comparable to the high resistance state (off-state) obtained with initial reset switching; likewise, the forming voltage is comparable to the SET voltage of the device. Fig. 2.1(b) shows the forming free characteristics of multilayer Pt/HfO_x/TiO_x/TiN device [20] where the high resistance before forming and after resetting is the same, i.e., 10^7 Ω. Similarly, the SET voltage obtained while performing EF and Set switching during switching is the same (1.5 V); hence the device is termed as forming free.

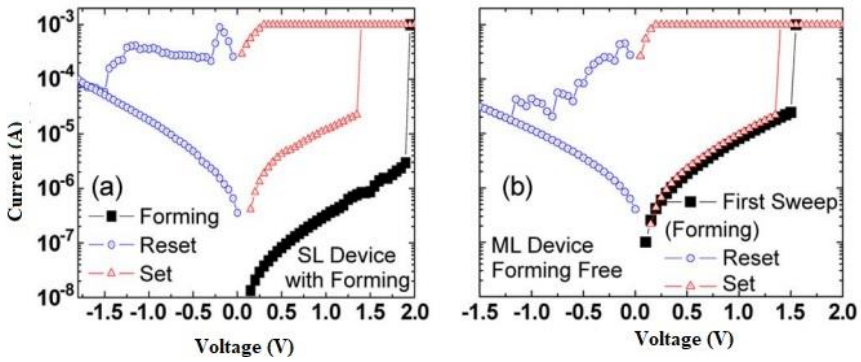


Fig. 2.1(a) Electroforming in Pt/HfO_x/TiN device (b) forming free device characteristics of Pt/HfO_x/TiO_x/TiN [20]

Initial switching in the device results in the formation of a percolating path known as conduction filament (CF), through which the oxygen vacancy drift occurs. Widely accepted theory to fit with the RS of resistive memories is the formation and rupture of conduction filament (CF). CF can establish either with oxygen vacancies or metallic ions spanning from top electrode to bottom electrode or vice versa. The filament formation results in a decrease in resistance of the device, and the corresponding resistance level is known as low resistance state (LRS), whereas the rupture of the filament occurs at an opposite polarity of input voltage so that the resistance of the device increases to enter into a high resistance state (HRS). Thus, switching the device back and forth from LRS to HRS and vice versa is referred to as resistive switching (RS).

Resistive switching can occur either with a single polarity of input voltage or with two different polarities of input. The former class of devices is known as unipolar resistance switching (URS) devices [37], [38], where both SET and RESET switching can occur with the same polarity of the input voltage (positive or negative). Fig. 2.2(a) shows the characteristics of URS [39], where the red color solid line represents the LRS and blue represents HRS. On the contrary, in the second class of devices, two different polarities of biasing voltage are required to switch the device from one state to another, known as bipolar resistive switching (BRS).In Fig. 2.2(b), the HRS and LRS of the device are shown with blue and red solid lines, respectively. Also, the voltage at which the LRS to HRS transition occurs is marked as RESET (negative polarity), and HRS to LRS transition is marked with SET (positive polarity). However, both URS and BRS devices exhibit two stable resistance states namely; HRS and LRS which enables the memory unit to store a bit of data, whereas several other devices exhibit stable intermediate resistance states (IRS) in addition to LRS and HRS, capable of storing

multiple bits known as multilevel-cell (MLC), which is the widely recognized solution to attain ultra-high-density memories [40], [41] by storing multiple bits in one memory unit.

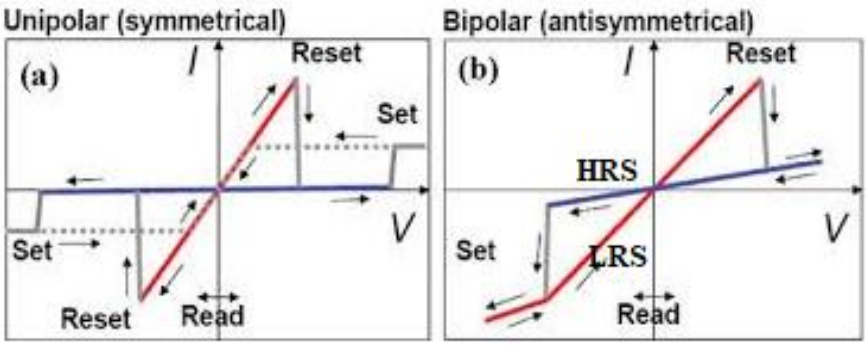


Fig. 2.2 (a) Unipolar switching (b) bipolar resistive switching characteristics [39]

Based on the mechanism of conduction filament formation, RRAM devices can be classified as Oxide-RRAM, conduction bridge resistive RAM (CBRAM), and thermochemical memory(TCM). In Oxide-RRAM, the switching process can be defined with valance change mechanism (VCM), whereas in CBRAM, the switching is governed by a process known as Electrochemical metallization (ECM) [6], [27], [42]–[46]. In TCM, the switching occurs due to the thermochemical mechanism (TCM) [47]. The following subsection explains these three switching mechanisms in detail.

2.1.1. Classification of RRAM memory devices

The memory devices can be classified as valance change memory-based ox-RRAM, Electrochemical metallization-based CBRAM, and TCM based on the mechanism of switching.

2.1.1.1. **Valance change memory (VCM)**

The valance change mechanism (VCM) is the switching mechanism seen in oxide-based RRAM (Ox-RRAM), where the oxygen vacancies contribute to the switching process. Oxygen vacancies (Vo) are either positively charged or neutral based on their chemical composition. During the decomposition of oxygen, electrons are released in addition to oxygen vacancies. Therefore, it is considered as the n-type donor. Based on applied input, the oxygen vacancies present within a material can create additional energy states within its bandgap, thereby contribute to the switching process [48]. The transition metal oxides that exist with multiple valency states are the ideal materials that exhibit VCM. Besides, the density of V_o is

a factor that determines the conduction character of the device. If the density of Oxygen vacancy is low, the transition metal oxide becomes semiconductive in nature due to the presence of localized states. Conversely, as the density of Oxygen vacancy is high, the CF may show metallic nature due to the formation of subbands with the presence of extended states within the bandgap.

The initial electroforming mechanism in VCM is attributed to the generation and drift-diffusion of oxygen vacancies [49] within the transition metal oxides. After the electroforming process, the resistive switching occurs due to reduction reaction and oxygen vacancy migration (or ion migration), resulting in a change in the stoichiometry of the transition metal oxide, thereby the insulating oxide temporarily changes to a more conductive sub-stoichiometric phase, and the oxygen vacancies drift towards the anode to form a conductive filament (CF) which in turn results in a significant reduction in barrier heights [48]. Thus, the device switch to ON-state. When applying an opposite polarity of input voltage, the Oxygen vacancies drift back to their position, causing the rupture of filament leading to RESET process. Examples of VCM based memories are Pt/Ta_2O_5/TaOx/Pt, Au/Al_2O_3/FTO [50] [51]. Microscopic view of VCM is reported in Pt/ZrO_x/Zr VCM cell on response to a triangular voltage sweep as shown in Fig. 2. 3, where Pt represents the active electrode (AE), Zr the ohmic electrode (OE), and ZrOx is the insulator [52].

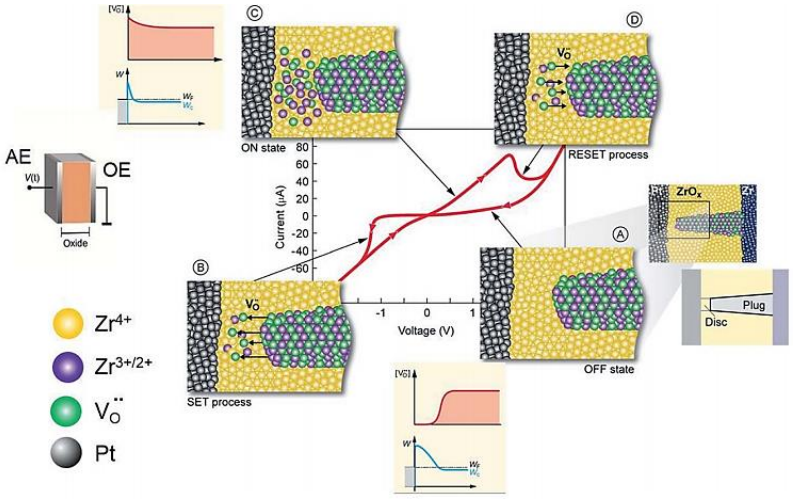


Fig. 2.3 Valance change memory switching mechanism in Pt/ZrO_x/Zr VCM cell where A denotes the off-state, B denotes the SET process C is ON-state and D is the reset process [52]

2.1.1.2. **Thermo chemical mechanism (TCM)**

The thermo-chemical mechanism or TCM occurs in RRAM devices in which thermo chemical reactions affect the thermal decomposition of oxides to form the filament during forming and SET switching process, whereas the rupture of filament causes RESET due to the joule heating effect. It is reported that unipolar devices like e Pt/NiO/Pt shows TCM kind of switching [50], [53].

2.1.1.3. **Electrochemical metallization (ECM)**

Electrochemical metallization (ECM) is the switching mechanism exhibited by the RRAM devices attributed with an electro-chemically active electrode such as Ag, Cu, or Ni [19], [54]–[56], and an electrochemically inactive counter electrode made of Pt, Au, FTO, etc. The devices that exhibit ECM-based switching mechanisms are known as conductive bridge resistive random-access Memory (CBRAM). The schematic of processes associated with ECM is depicted in Fig. 2.4, where Fig. 2.4(a) illustrates the oxidation of active metal atoms to ions at the anode and its migration towards the cathode and the subsequent reduction process. Reduction of metal cations to metal takes place at an electrochemically inert electrode and the onset of formation of a highly conductive filament connecting the bottom electrode (BE) to the top electrode (TE) is shown in Fig. 2.4(b). Fig. 2.4(c) illustrates the electrochemical dissolution of the filament while reversing the polarity of the applied voltage and subsequent resetting of the cell to HRS [57]. Examples of devices falling under this category are Ag/ZnO:Mn/Pt, Ag/TiO_x/Pt [40], [58], [59].

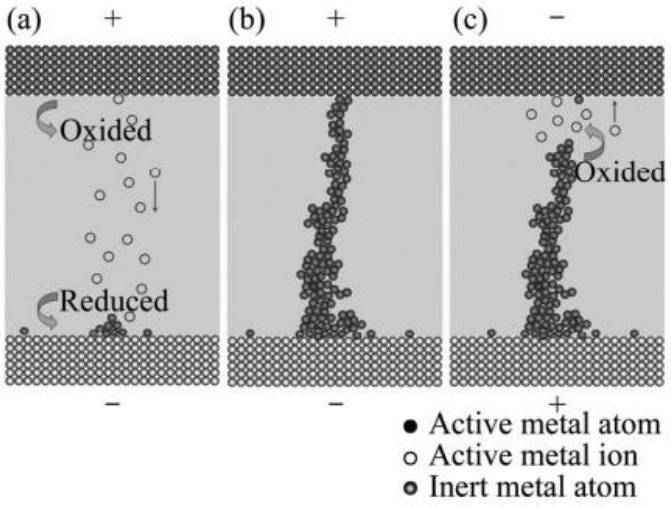


Fig. 2.4 Electro-chemical metallization process [57](a) oxidation of active metal atoms and its migration (b) formation of CF connecting the BE to TE (c) dissolution of filament

Various reliability testing parameters and other terminologies related to resistance switching devices are given below, where the endurance and retention are related to the reliability of a device.

2.1.2. Basic terminologies

Even though the devices exhibiting VCM or ECM are made from the same or different memory medium (switching layer), the electrodes have a major role in determining the switching mechanism. The electrodes seldom participate in the switching process of VCM, whereas in ECM, at least one of the electrodes would be reactive to facilitate the cations to participate in resistive switching. As the electrodes play an important role in switching, there are differences in the selection of electrode material for ECM and VCM.

Another classification of RRAM memory is based on the presence or absence of a conduction filament. If resistive switching is contributed by the switching elements within the nano scale conduction filament, such switching is known as filamentary switching [48], [60], whereas the switching occurs at the interface of semiconductor/dielectric material and the metal electrode is known as interface switching (uniform switching). In filamentary switching devices, the presence of a filament can be viewed using transmission electron microscopy [61]. Nevertheless, various arguments are existing to identify both categories. One method of identification is by analysing the I-V characteristics of the device, next is by investigating the area scaling where it is believed that the filamentary devices show area independent switching where the uniform switching devices do not. Next idea is to conduct a fraction test; means — physically breaking the device into two and analyze their resistance, in this method, the uniformly switching device will show similar resistance for both parts. In contrast, the filamentary switching device parts show different resistance values [60].

2.1.2.1. **Read margin:**

The readout margin is defined as the voltage difference between the output voltages produced by a cell in its low resistance (LRS) and high resistance (HRS) during the read operation. Read-out margin affects the access latency and power dissipation [62]. This factor is also considered as a measure of performance and reliability. It has also been reported that the readout margin has a dependency on temperature [62], when the temperature increases, the readout margin drops sharply.

2.1.2.2. **Roff/Ron ratio**

Roff/Ron ratio is a measure of the quality of the device to be used in an application, which can be calculated by measuring the ratio of HRS resistance and LRS resistance at a constant voltage.

2.1.2.3. **Variability:**

The inconsistency in device characteristics is known as variability, which can be of two types: cycle to cycle(c2c) variability and device to device (d2d) variability. If an inconsistency is present in the characteristics of a single device when subjected to multiple cycles of the input signal is known as c2c variability. On the other hand, if the inconsistency present in the characteristics of multiple devices, then it is termed as d2d variability. Variability is considered as one of the major challenges in the evolution of the RRAM device which is originating from the random nature of the ionic/vacancies movement [63]–[66].

2.1.2.4. **Endurance:**

Endurance can be defined as the number of cycles of write 0 and write1 processes a device can perform before failing its operation. This parameter is considered as a reliability measure which is evaluated by subjecting the device to multiple write pulses under controlled current compliance and is represented with measured resistance levels Vs time plots [67]–[70]. In a few devices, endurance failure is reported where both HRS and LRS levels became difficult to distinguish. The plot given in Fig. 2.5 demonstrates the endurance cycle plotted against resistance. Recently, 'Crossbar. inc' has developed a memory with 1 million input write cycles.

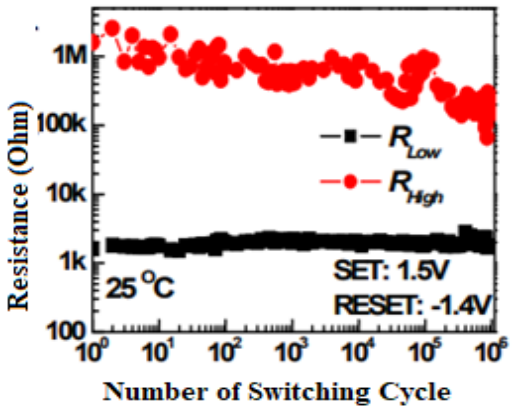


Fig. 2.5 Example for an endurance plot [71], with LRS and HRS, can be distinguished.

2.1.2.5. **Retention:**

The ability of a memory device to remember its previous state after multiple read cycles. In order to measure retention, the device must be driven to a particular memory state (LRS or HRS) and apply read pulses for a long time. This feature is also considered as a reliability measure and is represented with a resistance Vs time plot [72]–[75]. It is reported that the retention of data in several devices has reached a limit of 10 years at 85^0C. The graph plotting the resistance vs time is given in Fig. 2.6.

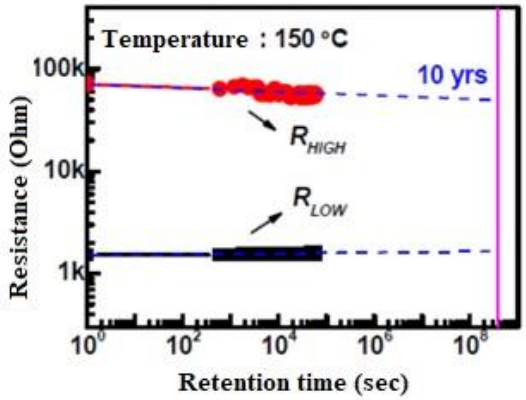


Fig. 2.6 Retention plot showing the retention of data during the reading process [76]

2.1.2.6. **Nonlinearity**

Nonlinearity is an essential parameter in the I-V characteristics of a RRAM device that conforms the potential range of biasing voltages available for selected and unselected cells while using them in crossbar array. In a CBA, the rails of unselected RRAM device will be supplied with a low voltage to prevent the sneak path current and high voltage supplied to selected device ensures the high current to perform read/write to the selected RRAM. Low nonlinearity adversely affects the data integrity by changing the state of the unselected device and causing the sneak path current. Nonlinearity can be measured with respect to the read voltage and SET voltage. High nonlinearity is the desired factor for RRAM devices. Non-linearity in device characteristics with respect to SET is defined as the ratio of magnitude of the current attained at SET voltage and the magnitude of current attained at half of SET voltage, which in turn means the writing process would be stable. Likewise, the non-linearity measured at read voltage is the ratio of the magnitude of the current attained at read voltage and at half of read voltage, which ensures the optimum voltage range available for the read operation.

To understand the basic working of the RRAM devices, several Physics-based models are evolved to study its memory property, in which the ionic and electronic interactions are governed by three major attributes such as switching mechanisms, conduction mechanisms, and temperature modeling.

2.1.3. Switching mechanisms adopted in RRAM models

Several models are given explanations for the switching mechanism. In a few models, the switching mechanism is defined as the movement/reduction of oxygen vacancies (oxygen ions) or metallic cations by drift-diffusion or REDOX reactions [44]. In the drift-diffusion model, the defect migration is induced by an electric field and localized temperature during SET and RESET switching respectively. In this approach, the migration depends on the electric field strength, direction of the electric field, and charge of ionic species. In the drift-diffusion model, Fick's diffusion and ionic drift are the two fluxes that determine the ionic movement [77] which is given in (2.1).

$$\frac{\partial n_D}{\partial t} = \nabla \cdot (D\nabla n_D - \mu F n_D) \qquad 2.1$$

where $D\nabla n_D$ and $\mu F n_D$ are the Fick's diffusion and ionic drift terms, respectively. n_D is the doping concentration, D is ion diffusivity, μ is the ion mobility, and F=-∇ψ where ψ is the local electrostatic potential demonstrating the relationship between drift and electric field. D and μ are based on the Mott-Gurney ion hopping law.

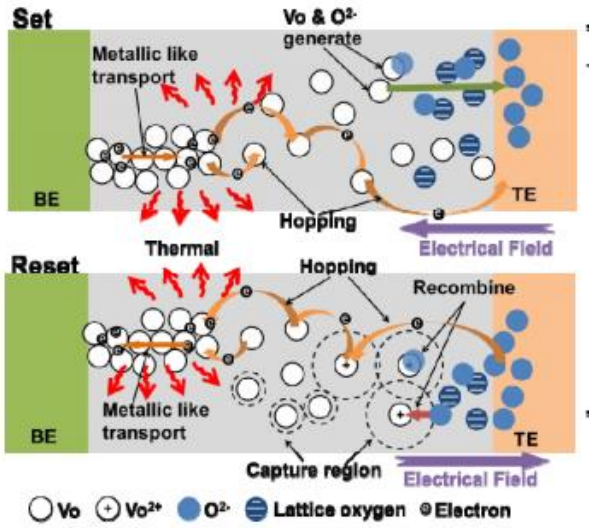


Fig. 2.7 The physical process of modeling the oxygen vacancy switching and electron-based conduction mechanism [78]

Another approach adopted to model resistive switching is the REDOX mechanism, where generation and recombination (G-R) of oxygen vacancies (V_O) with oxygen ions, oxide phase transition (P-T), as well as the hopping and migration of generated defects are considered as the basis of switching. These mechanisms are illustrated in Fig. 2.7. In such modeling approach, the SET process comprises the P-T from semiconductor to metallic phase and the generation of oxygen vacancies [79], [80], while the RESET process involves the reverse P-T from metal to semiconductor phase, where oxygen ions are released and hopped into the switching layer to recombine with oxygen vacancies [64], [81] to create a gap at the interface. The variation of the filament gap is given as:

$$\frac{dg}{dt} = a.f.\left(\exp\frac{-E_A}{KT}\right) \qquad 2.2$$

where g is the gap length, a is the field enhancement factor, and f is the attempt-to-escape frequency. The activation energy E_A is lowered due to the Poole-Frenkel effect by the electric field in the gap generated during RESET is given as:

$$E_A = E_{A0} - \alpha_0 q V_{gap} \qquad 2.3$$

where α0 is the activation energy barrier lowering factor, E_{A0} is the barrier at zero fields, and Vgap is the voltage across the gap.

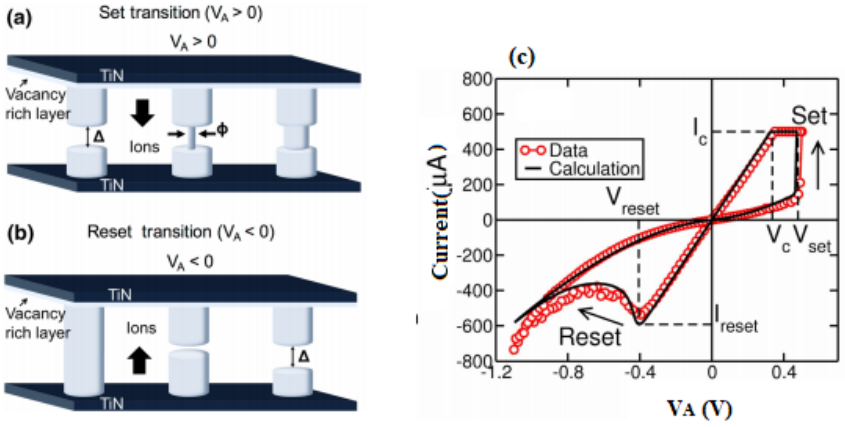


Fig. 2.8 (a)Schematic of set model showing the filament growth and (b) showing the reset model demonstrating the RESET model (c) I-V characteristics obtained from model plotted against experiment curve[30]

An analytical model of conduction filament evolution in filamentary-type RRAM is demonstrated in [30] is described in Fig. 2.8. In which Fig. 2.8(a) demonstrates the growth of oxygen vacancy-rich filament. In response to a high electric field developed between the

broken filaments, the oxygen vacancies migrate towards the top electrode, which in turn reduce the gap Δ between broken filaments, and at the meantime, the diameter of the filament represented with ϕ also increases, and its growth is limited by an external compliance current (Ic), whereas the Fig 2.8(b) shows the reset transition by illustrating the replenishment of the filament showing an increase in the gap between filament segments due to the effect of local electric field and temperature. Further, the resulting model characteristics are plotted against the experiment result as shown in Fig 2.8(c), where external compliance current is marked with Ic.

Similarly, other analytical models explaining the device physics of Pt/Ta_2O_5/TaO_x/Pt are presented in [31], [32], where both models demonstrate the Schottky current conduction through the conduction filament as shown in Fig. 2.9(a).

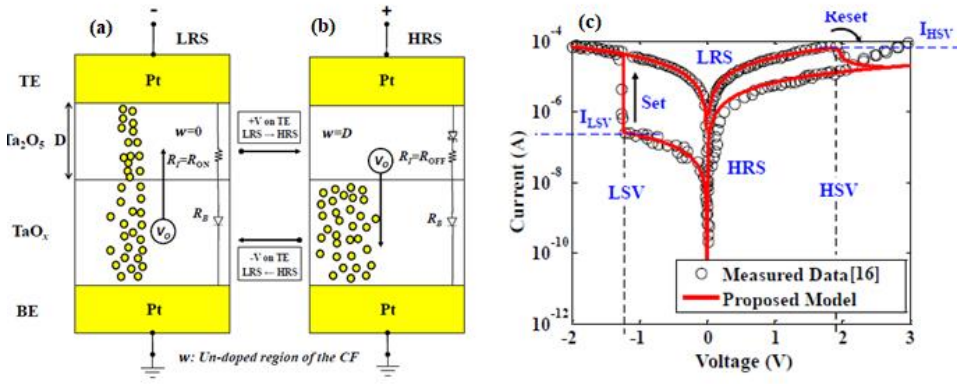


Fig. 2.9 a) Demonstration of state independent current conduction during LRS b) The reset switching occurs with positive voltage c) Results of model results plotted against experiment data [31]

When a negative voltage is applied to the top electrode, the positively charged Oxygen vacancies migrate towards the top electrode to form a conduction filament spanning in the Ta_2O_5 layer therefore the resistance of the device decreases, and it switches to a low resistance state (LRS). While on applying a positive voltage on the top electrode causes the positively charged oxygen vacancies to migrate towards the bottom electrode leaving the gap, hence the device switches to a high resistance state (HRS) as demonstrated in Fig. 2.9(b). Experiment data as well as resulting simulated characteristics are shown in Fig. 2.9(c).

2.1.4. Conduction mechanisms in RRAM devices

A wide range of conduction mechanisms are used to describe the current conduction in RRAM devices, such as Schottky barrier conduction [82] tunneling, Space Charge Limited

Current (SCLC), ohmic conduction, hopping conduction etc. The conduction mechanism present in a device is determined by the nature of bulk material and its corresponding interfaces with metal and oxides. For specific models, the conduction mechanisms are derived by fitting the experimental results with existing models defined with mathematical expressions.

The factors used to model conduction mechanisms are barrier height, activation energy, hopping distance, tunneling barrier height, barrier thickness, electric field, image force as well as temperature. The most critical parameter required to model thermionic conduction in Schottky contact(metal-oxide interface) is the barrier height [34], which is determined by the physical properties of the oxide layer, structure of RRAM devices, image force lowering effect, and electric field. Image Force lowering effect at the depletion layer interface influences the current conduction in semiconducting devices. Image force lowering is the reduction in activation energy required for the carriers to overcome the Schottky barrier by the accumulation of charges at the interface of the metal-dielectric layer due to the presence of a high electric field. Various approaches are adopted to include the effect of image force in conduction mechanism [84], [85], [45], [86]. Physical parameters like channel length, filament thickness, formation of Schottky junction with different materials. Moreover, Oxygen vacancy doping concentration has a significant impact on modulating the Schottky barrier where the length of the doped (concentrated) or un-doped section of the filament is spotted as a variable to control the Schottky barrier height in Schottky conduction models. Alternatively, the current through the device is implemented with hopping conduction in some of the [64], [81] models, where gap length g and applied input voltage V are the control variables.

$$I(d, V) = I_0 * e^{\left(\frac{-g}{g_0}\right)} \sinh\left(\frac{V}{V_0}\right) \qquad 2.4$$

However, in filamentary models, the total current in the device is associated with the shape of CF. In [87], a conical shape is approximated to the CF where the magnitude of the current is not only contributed by the radius of the top face of CF but the lateral sides as well.

In addition to Schottky and hopping models, derive current characteristics have been derived by considering the electron tunneling through nano meter scaled dielectric layers [88], [89].

2.1.5. Temperature modeling:

Temperature is another factor that is used to model switching and current conduction in several physics-based models. Joule heating is responsible for the temperature variations in the

CF. For example, the models in [85], [64] use a simple Joule heating temperature model controlled by the electronic current that flows through the filament [80]:

$$T = V_{el} I_{el} R_{th} + T_0 \quad (2.5)$$

$$T = RI^2 R_{th} + T_0 \quad (2.6)$$

Physical models based on generalized hopping do not consider temperature variations while modeling the current. However, many Schottky-based models approximate room temperature for current conduction (300K) [20], [45], [86].

2.7 Crossbar array formation of RRAM devices, sneak path current, and technologies to mitigate sneak path current

A Cross bar array is an array of horizontal word lines and vertical bit line trails where the bidirectional memory element sits between their cross points [27]–[29]. To use the RRAM devices in-memory applications, the devices should be configured in 2D or 3D arrays, though the major challenge encounter with RRAM device in array formation is the sneak path current originating from the low resistance path offered by the unselected cells in the crossbar array, which is demonstrated in the previous chapter.

To circumvent the problem of sneak path current, various techniques are employed, such as writing/reading schemes, variations with nano crossbar architecture, and associating the memory device with switches; where the main idea of the approach is to associate selector switches/devices such as diodes [90], transistors [76], [91], volatile bi-layer devices and multilayer selector devices with RRAM device. The following section demonstrates each of the implementation techniques.

2.1.6. Multistage reading/writing schemes adopted to reduce sneak path current

The adverse effects of sneak path current in nano crossbar array are the degradation/misread of the data available in the selected memory device and affecting the data stored in unselected cells, thereby affecting data integrity. At the initial stage, various single write/read schemes are defined to reduce sneak path currents. Recently, multiple-read/write are proposed, which uses analog to digital converter (ADC) and comparators in the design [92], [93] In another approach, the adaptive threshold read-out technique is used to reduce the sneaking current by using predefined dummy cells in the array to assist in reading the data [94].

Yet another method to minimize sneak current crossbar array is the implementation of a data-encoding circuit that guarantees that at least half of the memory cells in the CBA should be in a high-resistance state [95].

2.1.7. Architectural variations of the crossbar array

The scheme proposed to reduce sneak path current in [96] is the modification in nano cross bar array configuration, where instead of the crossed row and columns, isolated rows and connected columns are proposed (Fig. 2.10(a)) along with that the modified read scheme to reduce the power dissipation [97] is used. In this scheme, the data write performed across all memristors sharing the same column (bit line) while the read is performed in individual cells, thus avoiding the need for Vdd/2 bias.

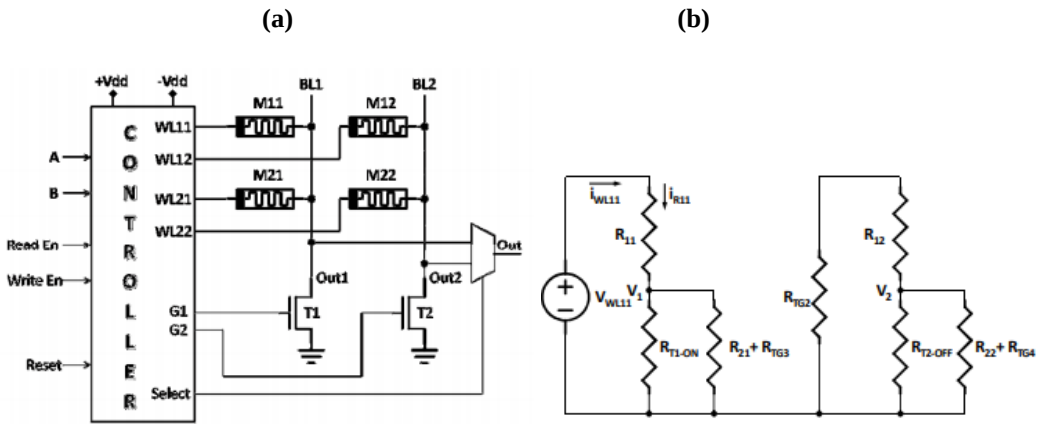


Fig. 2.10 The scheme of isolated rows and connected columns (b) Demonstration of reading process unaffecting the unselected cell [96]

The equivalent circuit demonstrating the read is shown in Fig. 2.10(b) where R11 is the selected cell and R21 is the unselected cell sharing the bit line with R11. In this case, the current iwL1 passes through the selected cell, and then it divides into two branches where one branch consists of R21 however, the magnitude of current flow through R21 is infinitesimally small to change the state of R21 thus reducing the effect of sneak path current. The scheme is particularly designed to use in look-up tables (LUT) of FPGA where multiple reads occur.

Similarly, to attain the least sneak path current with the best noise margin (NM), another architecture is proposed in [98] with unfolded crossbar architecture where instead of providing separate rows, separate columns are provided to individual memristor through CMOS based multiplexer circuit. The unfolded cross bar array architecture is shown in Fig. 2.11.

Nevertheless, the proposed scheme is not a good idea due to the necessity of multiple trails at column.

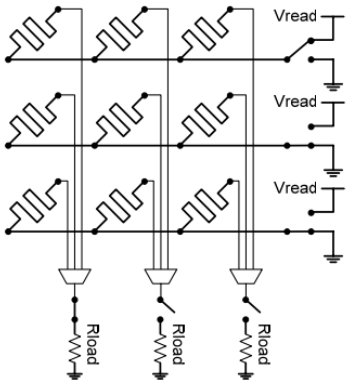


Fig. 2.11 unfolded crossbar array architecture to reduce sneak path current [98].

2.1.8. Associating a diode with a memory unit (1D1R)

Diodes are semiconductor devices, mostly unidirectional. These devices can be used as switches to prevent sneak path current by associating each memory unit in a crossbar array. Different diodes are used to obtain the 1D1R structure, such as PN diode, Schottky diode, Zener diode, etc.

For instance, to reduce sneak current, Ni/AlO_y/n+-Si diode cell is connected to bipolar RRAM with TiN/HfO_x/Ni stack and 1D1R characteristics are obtained with a self-compliance current of 10 µA [99]. The bipolar resistive switching curve of RRAM is shown in Fig. 2.12(a), diode characteristics are depicted in Fig. 2.12(b) and the combined characteristics are displayed in Fig. 2.12(c).

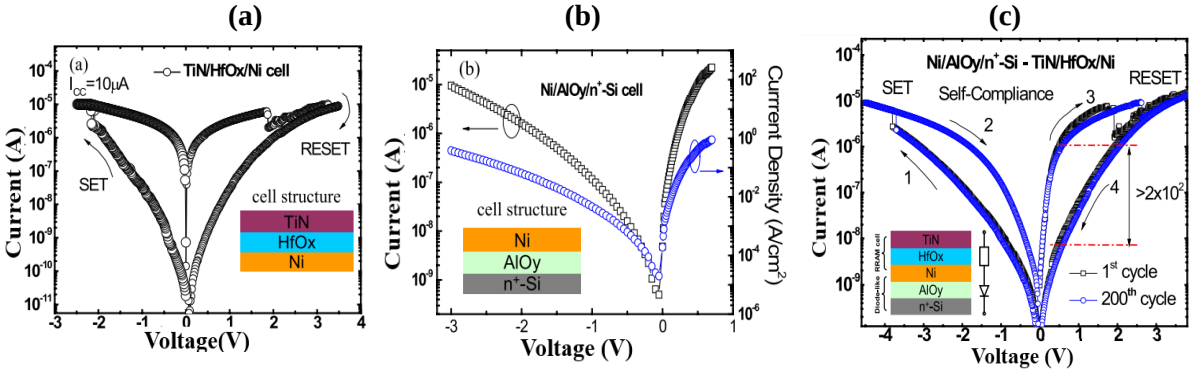


Fig. 2.12(a) Bipolar resistive switching behavior of TiN/HfOx/Ni RRAM device (b) Diode characteristics of Ni/AlOy/n+-Si (c) Integrated 1D1R characteristics [99]

In the combined characteristics, the non-linearity is found to be >200 while the Roff/Ron ratio got reduced compared to the RRAM device. Similarly, the 1D1R implementation based on the W/TiO_x/Ni Schottky diode and Cu/HfO_2/Pt RRAM demonstrated the self-compliance feature achieved due to the reverse current attained during the SET switching [100]. However, the non-linearity of the 1D1R architecture remains the same as that of the 1R, also the SET switching occurs at a low voltage made it insignificant to use in a crossbar array. The corresponding diode and RRAM characteristics are represented in Fig. 2.13(a) with red and blue lines respectively. Fig. 2.13(b) portrays the result of current offered by the integrated architecture.

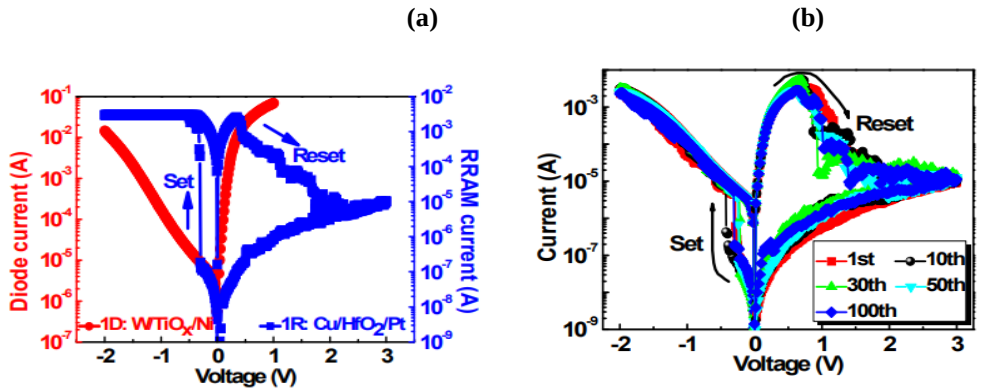


Fig. 2.13 (a) I-V characteristics of 1diode and one RRAM b) multiple cycles of I-V characteristics obtained with 1D1R [100]

The sneak path current measured from a 2x2 cross bar array of Pt/ZnO/Pt device exhibiting BRS characteristics is reported in Fig. 2.14(a), where the sneak path current reaches an amplitude of approximately 5 mA at an input voltage of 1.5 V. Therefore, two designs are employed to reduce sneak current where in the first design NiO/ZnO pn junction diode is associated with RRAM while in the second design, WO_3/ZnO based tunnel diode relates to RRAM. The resulting characteristics of the combined 1D1R with NiO/ZnO and WO_3/ZnO are presented in Fig. 2.14(b) and Fig. 2.14(c), respectively. After associating the device with diodes, the sneak current is eliminated to a certain extent. This experiment proves that the association of tunnel barrier diode is promising compared to PN junction diode as it retains the SET switching characteristics and shows a low potential subthreshold slope [101]. The approach of using the tunnel barrier-based diode provides low voltage operation of cross-bar array memory devices which is an added advantage [102]. Yet another architecture demonstrating a reverse biased diode with RRAM in crossbar array limits the sneak current presented in [103].

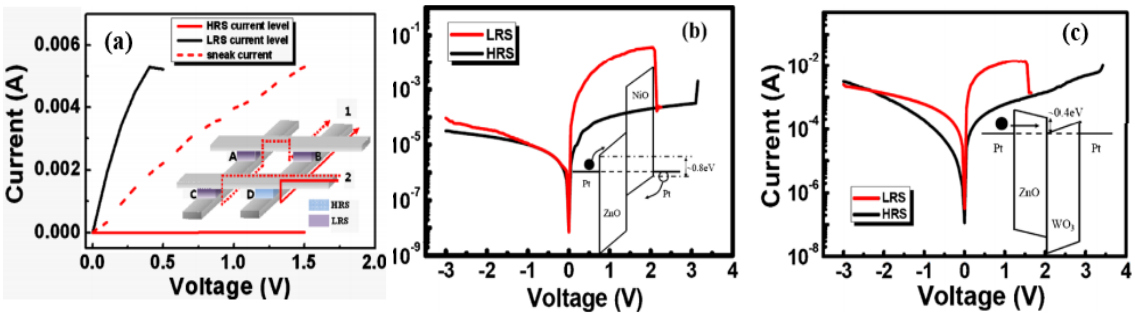


Fig. 2.14 The sneak path current measured from2x2 cross bar array (b)1D1R structure with ZnO/NiO diode(c)1D1R with ZnO/WO_3 tunnel diode [102]

Zener diodes are also can be used in association with RRAM to reduce the sneak path currents [104]. Connecting Zener diode and a Cu/HfO_2/Pt RRAM in series as shown in Fig. 2.15(a) results in the BRS characteristics with rectifying behavior as given in Fig. 2.15(b).

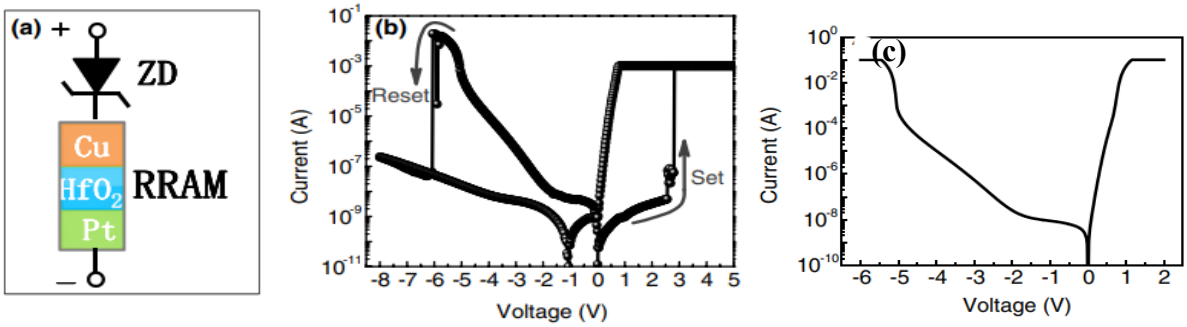


Fig. 2.15 (a) Schematic of Zener and CBRAM memory (b)Resulting curve showing the result of combination(c) Zener characteristics [104]

Zener diode can be a conventional diode at forward bias with a high current density that is achieved beyond a threshold voltage. Meantime, the reverse current holds at low value until it reaches its Zener breakdown region, and beyond that, it conducts and can enable the RRAM to drive in to SET/RESET switching process. In the Zener- Cu/HfO_2/Pt combination, it is noticed that the Zener breakdown occurs at a large voltage (2.5V). The readout margin is also sufficiently improved compared to the results obtained without the selection device. Hence, it can be useful in a write-once-read-many-times (WORM) crossbar array.

The major advantage noted with 1D1R architecture is the reflection of the rectification feature of the diode in the I-V characteristics of integrated design which possibly eliminates

the sneak current. Also, when connecting Ox-RRAM devices with low SET switching voltage to the diode can add the self-current compliance feature to the 1D1R, determined by the large reverse bias current of the diode [100].

Several drawbacks are noted down while delving into the diode-based design, they are; diodes with low reverse current cannot ensure BRS switching in 1D1R architecture, also the leakage current cannot be eliminated significantly in 1D1R as the devices can show some magnitudes of current flow at very low voltage ranges, which may cause the sneak path to emerge. Next, the maximum achievable crossbar memory capacity is limited by the reverse saturation current of the diode [105]. Similarly, the low reverse saturation current of the diode is the limiting factor for read failure in multi-level-cell (MLC) operation [105]. Among others, Zener diodes are not found to be a better candidate to act as a selector as its high Zener breakdown voltage causes the 1D1R to extend its reverse bias voltage to a higher value.

The implication from the study is that the selected diode should have a high forward current density and reasonably large reverse current density to ensure that proper switching can happen with 1D1R. As the forward current should be high enough to switch the memristor, a higher forward current density allows a smaller cell area of the diode and a higher integration density. Also, the properties such as endurance, low-temperature fabrication process, and compatibility with CMOS technology are considered when approaching their commercial application [106]. A table listing most of the 1D1R structures prevailing under this research field is shown in Table 2.1. In the given table, the ratio refers to the rectification ratio, which means the ratio of HRS current measured at forward bias as well as reverse bias. From the table, it is inferred that the most suitable diode to combine with RRAM is Schottky or PN type. Some Schottky diodes are bipolar, which is more suitable for achieving resistive switching and offers a rectification ratio of ~10^3. Moreover, it is noticed that the 1D1R devices can provide current density in the range of 10^2 to 10^6 A c.m^{-2}. Also, the average retention of the 1D1R device is found to be 10^4.

Table 2.1 1D1R architectures available in the literature [106]

D	M	Current density[a]	Fabrication temperature	Ratio[b]	Endurance	Retention	Current array size
Pt/TiO_2/Ti Schottky	Ti/SiO_x/Pt unipolar	10^2 A cm^{-2} (2 V)	≤200 °C	10^5 (±2 V)	300 (1D1M)	>10^5 s	8 × 8
Pt/TiO_2/Ti Schottky	Pt/TiO_2/Pt unipolar	>10^4 A cm^{-2} (2 V)	Near room temperature	10^9 (±2 V)	10^8 (D), 500 (1D1M)	10^4 s	4 × 4 × 2 (integrated 2 layer)
Pt/$InZnO_x$/CuO_x/Pt p–n junction	Pt/Ti-doped NiO/Pt unipolar	10^4 A cm^{-2} (2 V)	Room temperature	10^2 (±1 V)	100 (1D1M)	—	8 × 8
Pt/n-type Si Schottky	Pt/Ta_2O_5/Pt unipolar	>10^6 A cm^{-2} (1 V)	—	10^2 (±1 V)	10^3 (1D1M)	10^4 s	—
Pt/a-IGZO/Cu Schottky	Pt/HfO_2/Cu bipolar	10^2 A cm^{-2} (1 V)	Room temperature	10^3 (±0.5 V)	10^8 (D)	—	—
Ni/TiO_2/Ti Schottky	Al/STN/Pt bipolar	10^4 A cm^{-2} (1 V)	100 °C	10^3 (±0.5 V)	—	>10^5 s	—

[a] The forward current density of the series diode. [b] The ratio is defined as the ratio between forward and reverse currents of the lowest resistance state of the 1D1M unit.

2.1.9. Associating a transistor with a memory unit (1T1R)

Transistor-memristor combination is another solution to tackle the sneak current in the cross-bar array. In a 1T1R CBA, current flows only through the desired path and restricts through all other paths by keeping all transistors in the unselected rows remain in OFF-state. A typical 1T1R crossbar array is shown in Fig. 2.16 where the first row represents the selected cell in the array in which the transistor remains in ON-state. In contrast, the remaining rows are turned to OFF-state to unselect by keeping the transistor in the OFF position.

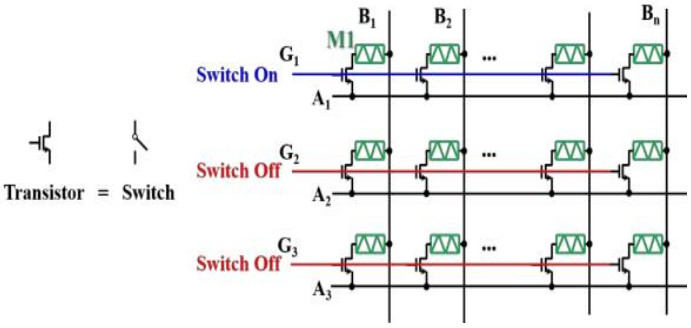


Fig. 2.16 Crossbar array formed of one transistor-one memristor (1T1R) structure [106]

Connecting/etching a ZnO-based thin-film transistor (TFT) in series with TiO_2-based resistive switching (RS) device resulted in 1T1R architecture.

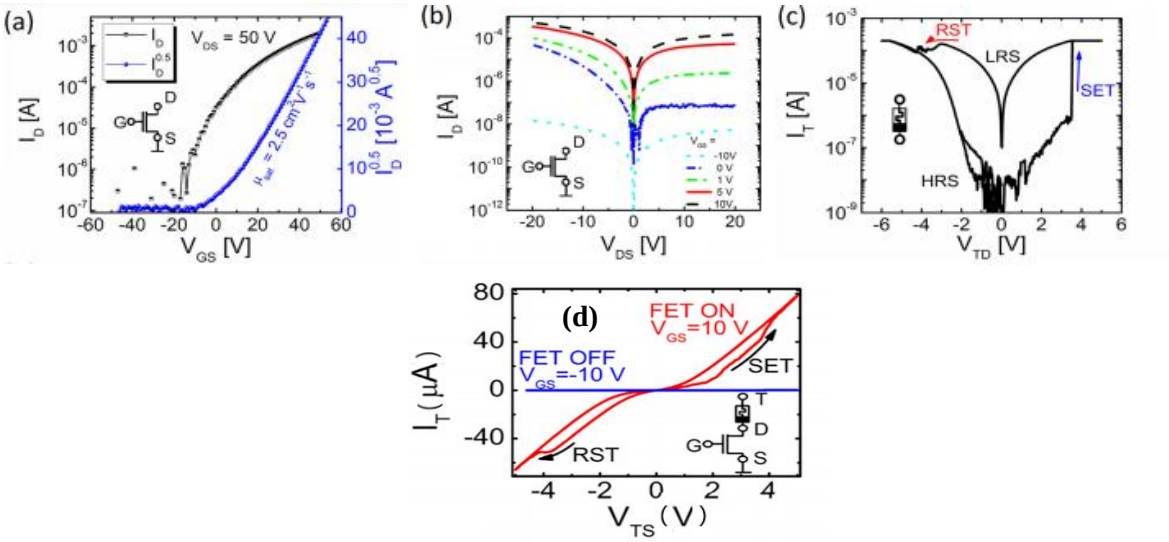


Fig. 2.17(a) Characteristics of Vgs (b) Current on response to Vds (c) Characteristics of resistive switching device [107] (d) 1T-1R characteristics [107]

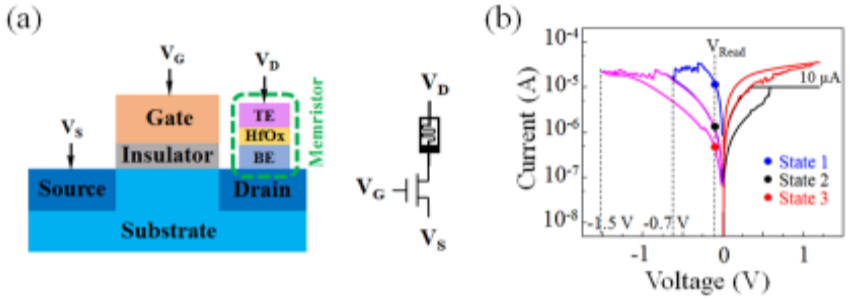


Fig. 2.18(a) Transistor -Resistor layout (b) I-V Characteristics of 1T1R [108]

The characteristics of 1T on response to the gate to source voltage (Vgs), drain to source voltage(Vds), and 1R are shown in Fig. 2.17(a), (b), and (c), respectively [107], where TFT conducts in both directions and controls the current through the memristor. The analysis found that at low Vgs, the device shows asymmetry in its characteristics, but at high Vgs the rectification factor reduces. Fig. 2.17(d) shows the integrated device characteristics which is obtained by providing Vgs=10 V and Vts sweep from -4 V to 4V. However, the device characteristics is not promising one due to low Roff/ Ron window.

In addition to binary states, 1T1R can offer multilevel memory states which is useful for application like digital comparators. In [108], multilevel is exhibited by TE/HfO_x/BE RRAM incorporated with NMOS transistor with 40 nm CMOS process. The layout of the device is shown in Fig. 2.18(a) and the combined characteristics illustrating the multiple states are shown in Fig. 2.18(b).

Another 1T1R realization where an NMOS transistor fabricated with 40 nm process is incorporated with RRAM [109] with the gate voltage VG applied during the complete operation is 1.7 V. The I-V curves of the transistor on response to different gate voltage is shown in Fig. 2.19(a). The gate voltage is fixed at 1.7 V based on the RRAM device's current values. The SET process in 1T1R is obtained in response to positive voltage (0 to 1 V) applied on the top electrode of RRAM, and RESET is obtained by grounding the top electrode of RRAM, further sweeping the input applied to source from 0 to 1.5 V.

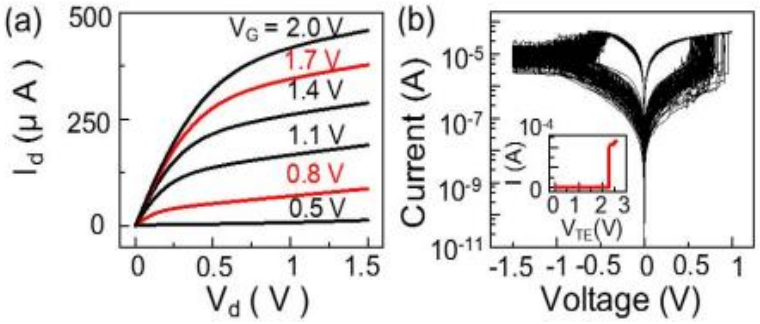


Fig. 2.19 (a) IV curves of NMOS transistor made with 40 nm process (b) Combined characteristics [109]

The implementation of 1T1R architecture with PNP transistor with vertical layout is present in [110]. The RRAM device is formed within the same substrate sharing the common bottom electrode as given in Fig. 2.20(a). The obtained NiO-GZO-NiO (PNP)transistor characteristics with conductivity in both positive and negative directions mimic the selector switch as shown in Fig. 2.20(b). Similarly, the RRAM switching characteristics of TiN/Al_2O_3/TiN RRAM is demonstrated in Fig. 2.20(c). However, the switching characteristics of the combined structure have shown to be a selector kind, with SET switching at -2 V and RESET switching at -2.5 V as shown in Fig. 2.20(d). Even if the memory window is small, it is claimed that the device has shown better

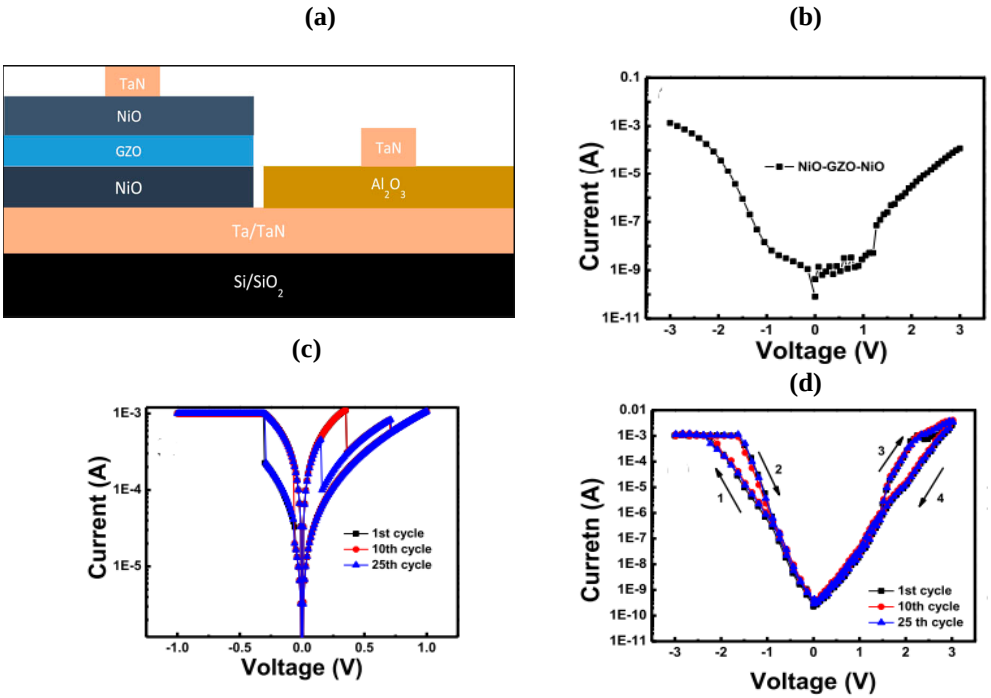


Fig. 2.20(a) Schematic of one transistor (pnp vertical structure) and RRAM device sharing common electrode TiN (b) Transistor I-V characteristics c)RRAM characteristics obtained with multiple cycles d) Combined characteristics obtained from the 1T1R architecture [110]

endurance and retention behavior. Moreover, the non-linearity offered by the 1T1R structure is reported to be in the order of 2, though which is not favorable for the crossbar array. Nonetheless, the transistor is reported to be a PNP; the structure is comparable with the crested barrier sector device.

The major disadvantage with a transistor in 1T1R design is the implementation of circuits spanning large areas. Hence, they are not suggested to use in large neuromorphic circuits or high-density memories. In particular, the performance of thin-film transistors is less compared to silicon transistors though their high forward current density has added advantage in the combined circuit. Also, in many 1T1R devices, the nonlinearity is not up to the mark.

Nevertheless, the unipolar behavior of diodes and scaling concerns of transistor switches impede their use in CBA. To overcome these shortcomings of the available selector switches, several non-linear selectors have been realized [111], [112], which are fabricated either as single-layer or multi-layer material stacks with advanced engineered designs [101], [113] while the recent studies show that the selector device with tri-layer structure provides more stable selector characteristics [112] with significant nonlinearity. Similarly, various CRS devices are also available where the most common configuration is the anti-serially connected RRAMs. The following section discusses different methods adopted to reduce sneak path current.

2.1.10. Associating a selector device with a memory unit (1S1R)

The recent progress in the emerging non-volatile technology is the implementation of selector devices in co-operation with the RRAM or CBRAM devices to alleviate the sneak path current. Selectors are volatile devices, work with the electron population, and do not show any kind of switching characteristics. The desired characteristics expected from a good selector are high non-linearity in I-V characteristics, low OFF-current, high selectivity, high current density, and voltage compatibility with the associated memory device. In 1Selector-1Resistor (1S1R) crossbar array, highly nonlinear selector connects in series with RRAM memory at each cross point as shown in Fig. 2.21, where the selector act as a switch to control the current flowing through the memristors while reading and writing, thereby the selector enables to select required memory unit among other unselected cells. At low voltage levels, the selector provides a high impedance to act as an open switch, and at high input voltages, due to inherent high conductivity, the selector acts as a closed switch or fully conducting device, thus controlling the selection of memory cells whilst blocking the sneak path current [114], [23], [115]. Based

on the type of applications two variants of selectors are present; selectors with analog I-V characteristics or digital I-V characteristics, where the first category finds applications in selector- RRAM neuromorphic computing platforms whereas, the second can be used in digital applications with discrete resistance levels in which the abrupt transition of resistance occurs at a specific threshold voltage. Ta_2O_5/TaO_x /TiO_2 [116] tri-layer stack, $TiN_{1+x}/Ta_2O_5/ Ti_{N1+x}$ [117] are examples of analog selectors while field-assisted superliner threshold selector is an example for selector with digital characteristics [118].

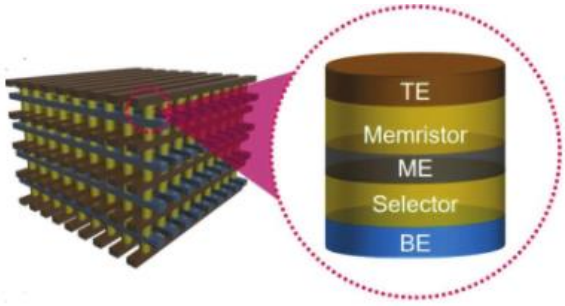


Fig. 2.21 Crossbar structure with selector -RRAM device [119]

In 1S1R approach, various factors are to be considered before connecting the selector with RRAM such as compatibility of electrodes, i.e., the top electrode of RRAM and bottom electrode of the selector should be compatible. Then, the operating voltage and current of both devices should be in a comparable range. There are several 1S1R combinations available with VCM memories and CBRAM devices. The following sections review some of the selector devices and their combined characteristics with memory.

Various fabrication strategies are adopted in selector design to attain the desired characteristics such as the crusted barrier formation or tunneling barrier formation, with oxides of nano meter thickness. The concept of crusted oxide barrier has been utilized in the high-performance $TaO_x/TiO_2/TaO_x$ based sector device, that satisfies all the desired features of selector such as high non-linearity, endurance, Roff/Ron ratio, current density ($1.6*10^7$ A/c.m), also the voltage compatibility with RRAM devices [120]. To demonstrate sneak path current reduction, the selector device has been fabricated in Pt/Cu doped HfO_2/Pt RRAM stack and been tested in cross bar array. Until a bias potential of -0.9 V to 0.7 V, the selector device shows high impedance to current, and beyond that, the selector shows increased conduction. At the same time, the RRAM starts to SET or RESET according to the polarity. In that work, it is reported that the sneak path current is suppressed by more than 4 orders of magnitude compared to RRAM. The corresponding selector characteristics and integrated selector-RRAM

characteristics are given in Fig. 2.22 (a) and (b) respectively [121] where Fig. 2. 22(a) shows asymmetric selector characteristics with non-linearity factor 10^4 and Fig. 2. 22 (b) shows the integrated characteristics showing the memory window with very low leakage current at low voltages (37 nA).

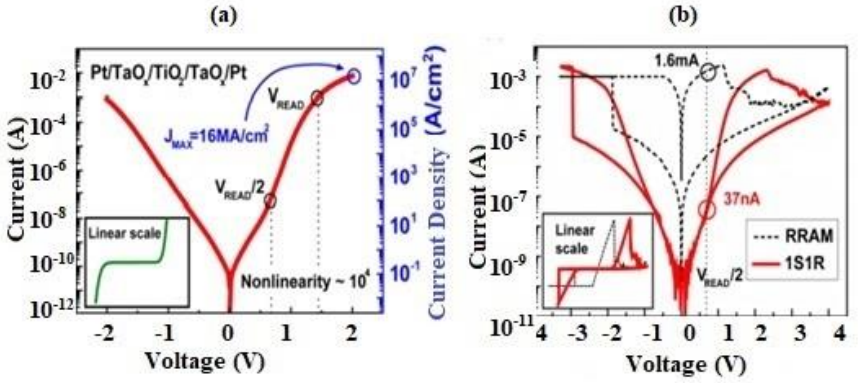


Fig. 2.22 (a) Typical I-V characteristics of $TaO_x/TiO_2/TaO_x$ selector (b) Characteristics of selector with Pt/Cu-HfO_2/Pt device [80]

Another implementation based on the vertical stacking of 1S1R with $Ta_2O_5/TaO_x/TiO_2$ selector device and Cu/TiO_2/Pt conductive bridge RRAM has been reported in [122], in which the integrated device reproduced robust bipolar switching behavior with abrupt transition between states, and the effect of the selector in the 1S1R circuit is the suppression of leakage current by a factor of 10^3. It has been reported that the presence of parasitic resistance affects device characteristics.

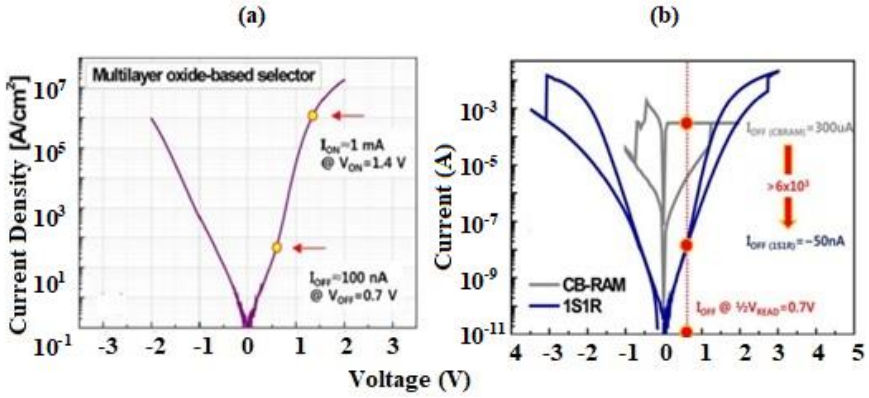


Fig. 2.23 Selector characteristics for (a) $Ta_2O_5/TaO_x/TiO_2$ device and (b) integrated device characteristics [122]

In the combined circuit, the sensing margin is improved compared to the CBRAM device. Moreover, stable endurance is observed for the integrated devices while maintaining the on/off ratio (>10). The selector I-V curve and the combined characteristics of the device and selector are shown in Fig. 2.23(a) and Fig. 2.23(b), respectively.

A high-performance Ni/TiO_2/Ni bipolar selector with Ni/HfO_2/Pt memory element is integrated and its characteristics are reported in [123], where the device structure of Ni/TiO_2/Ni/HfO_2/Pt with a crossbar array of dimension 8×8 is fabricated to demonstrate the reduction in sneaking current and reported that its V_{SET} / V_{RESET} is below ±4 V and, I_{RESET} is less than 150 μA. Another example for the 1S1R with an analog selector is the integration of TiN_{1+x}/Ta_2O_5/TiN_{1+x} material stack with Ta/TaO_x/Pt RRAM to achieve high non-linearity, high endurance, low variability, and low dependence on temperature [124].

There are several 1S1R devices formed by the connecting selector and ox-RRAM/CBRAM externally (means not etched in the same substrate). In [125], Ru/TaO_x/W selector is externally connected with Cu/HfO_2/Pt RRAM to form the 1S1R circuit. The selector is created by tuning defects and having a trapezoidal band structure that exhibits certain features such as selectivity (5×10^4), low off-state current (~10 pA), robust endurance (>10^{10}), high current density (1MA/cm^2). Besides, the combined circuit shows self-compliance and excellent uniformity. When connecting 1S and 1R serially, the circuit shows a set voltage under 4 V, and the reset voltage under -5 V suggested to use in practical applications. The selector and the externally connected device's characteristics are shown in Fig 2.24(a) and (b), respectively.

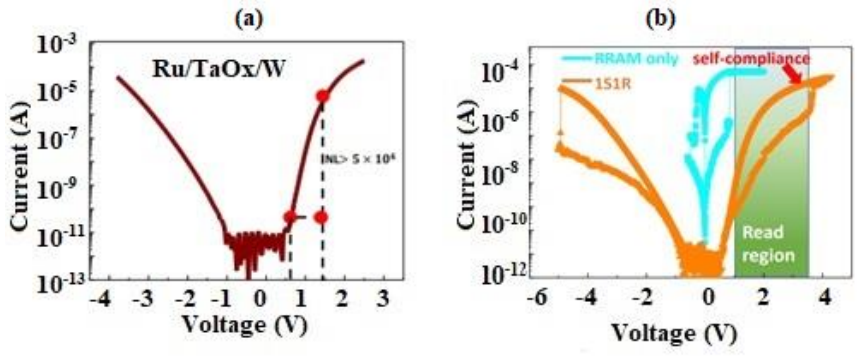


Fig. 2.24 a) Selector characteristics b) Integrated characteristics [125]

Another selector -RRAM combination connected externally to obtain the combined characteristics can be seen in [124], where TaN1+x /Ta2O5/TaN1+x stack is

used as the selector device I-V curve is given in Fig. 2.25(a). In the experiment, single layer Ta/ TaN 1+x/Pt is used as RRAM device. And the resulting characteristics plotted in Fig. 2.25 (b) shows the memory window though it is not very significant.

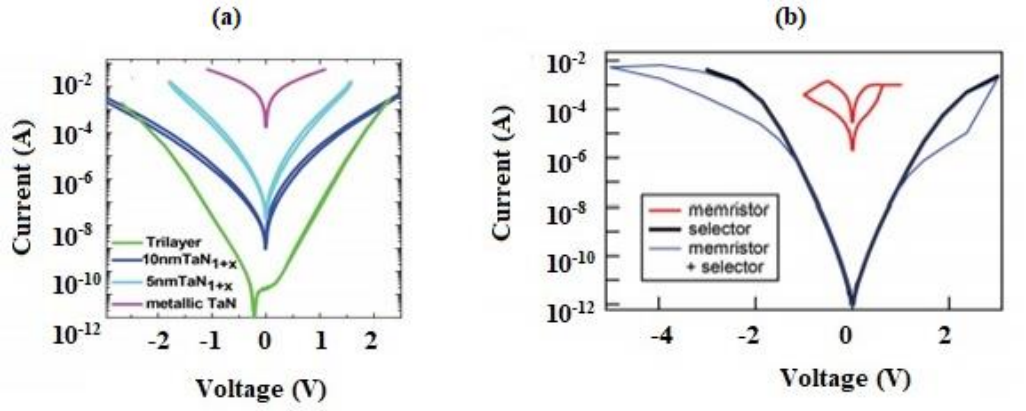


Fig. 2.25 (a) Selector characteristics (b) combined characteristics with RRAM [124]

A field-assisted superliner selector exhibiting digital characteristics (Fig. 2.26(a)) has been introduced in [126] claims the highest selectivity for the selector device as > $10^{10,}$ with the threshold can be modulated with controlling the insulator thickness. Moreover, this device provides a faster switching transition between ON and OFF, as shown in Fig. 2.26(b).

From the analysis of selectors and integrations with various RRAMs, it can be concluded that the tri-layer/ or multilayer structures of the tunnel or crusted barriers offer better selector functionality with significant non-linearity.

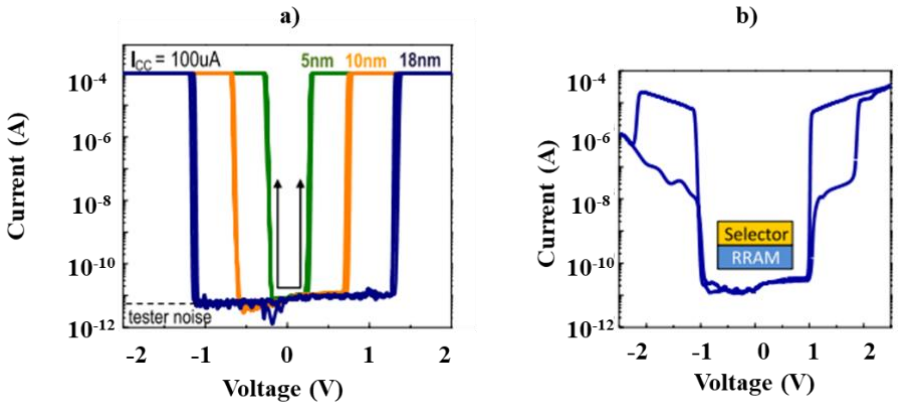


Fig. 2.26 (a) FAST selector characteristics (b) integrated characteristics of selector and RRAM [126]

In addition, the resistance of the device increases with an increase in the thickness of the layers in the multilayer structure, and the bidirectional functionality of these selector devices provides better performance to attain the memory feature. Experimental evidence shows that both externally connected selector with RRAM and those fabricated in single substrate offers high non-linearity. Furthermore, it is observed that the minimum SET and RESET voltage required to program the combined circuits is |>3V|. Also, the readout margin is significantly decreased as the array size increases [127]. Various 1S1R device stacks are listed out in Table 2.2 where various design with a current density variation of 10^{-1} to 10^{8} is available. Also, 1S1R provides better nonlinearity, which has a span of 10^{2} to 10^{10} available with different designs. Another metric to evaluate the combined device efficiency is endurance. Interestingly, all device combinations offer an endurance of $>10^{4}$, showing that the selector is a better switching device to eradicate the sneak path current problem.

Table 2.2 1S1R devices and its related parameters [106]

S	M	Current density	Fabrication temperature	Nonlinearity	Endurance of S	Dynamics
$Pt/TaN_{1+x}/Ta_2O_5/TaN_{1+x}/Pt$, tunneling barrier	$Pt/TaN_{1+x}/Pt$	10^3 A cm^{-2}	400 °C	10^4	10^8	—
$TaN/ITO/Co_3O_4/ITO/TaN$, n–p–n	$TaN/Al_2O_3/ZrO_2/Al_2O_3/TaN$	6.5 A cm^{-2}	Room temperature	10^3	10^7	—
$Pt/CoO_x/IGZO/CoO_x/Pt$, p–n–p	$Pt/TaO_x/TiN$	0.1 A cm^{-2}	—	10^4	10^4	—
$Ag/HfO_x/Ag$, OTS	$Pd/Ta_2O_5/TaO_x/Pd$	$>10^4$ A cm^{-2}	200 °C	10^{10}	10^8	75 ns, 300 ns
$TiN/Nb_{1-x}O_2/Pt$, OTS	$Cu/HfO_2/Pt$	$>10^6$ A cm^{-2}	—	10^2	10^{12}	<10 ns, <10 ns
W/SiTe/W, OTS	—	10^7 A cm^{-2}	Room temperature	10^5	10^8	2 ns, 7 ns
TiN/SiTe/Ag, OTS	—	$>10^2$ A cm^{-2}	300 °C	10^4	10^5	30 ns, 5.1 µs
TiN/GeSe/TiN, OTS	—	10^3 A cm^{-2}	300 °C	10^7	10^5	100 ns, 300 ns
Ti/CuO-NW/Ti, OTS	—	—	—	10^4	10^5	—

2.1.11. Array formation with Complementary resistive switching devices

An alternative approach to mitigate sneak path current in crossbar array is the implementation of complementary resistive switches (CRS). In addition, to sneak current mitigation, large power consumption problems of the RRAM devices can be bypassed by using complementary resistive switching (CRS**)** [128] devices. The CRS device implementation is generally done by connecting two similar RRAM devices in a back-to-back configuration with a shared electrode, as depicted in Fig. 2.27(a). Realization of anti-serial bipolar memristive elements is to address sneak current is first proposed in [129], where the memristive element used was $Pt/SiO_2/GeSe/Cu$, and the CRS characteristics result in a superimposed I–V

characteristics of RRAM elements (Fig. 2.27 (b)). In this case, the CRS circuit acts as a voltage divider so that at any time, any one of the RRAM in the LRS state and others would be in the HRS state, providing high resistance.

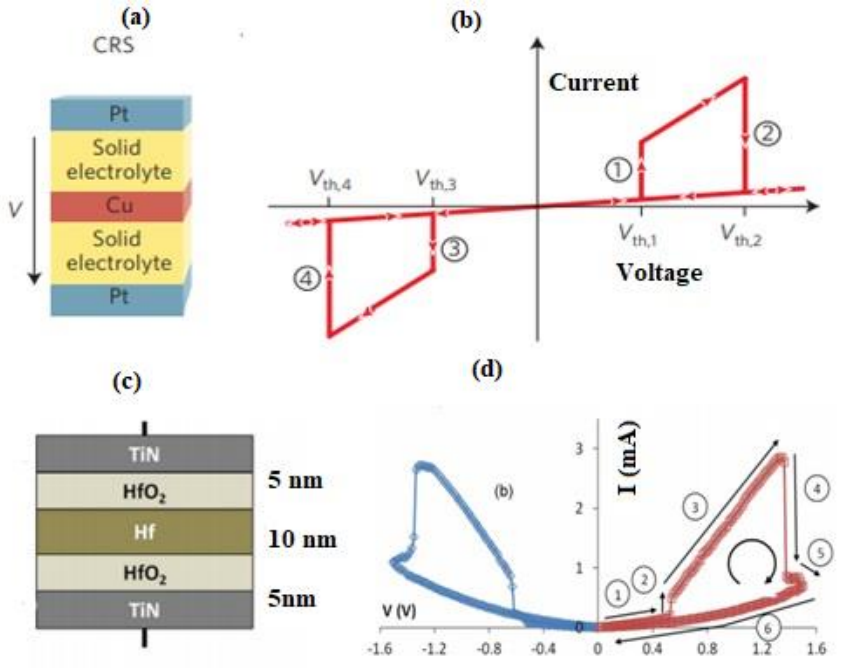


Fig. 2.27 (a) CRS cell made of $Pt/SiO_2/GeSe/Cu$ RRAM device with anti-serial connection [129] (b) CRS characteristics obtained from (a) (c) CRS device made of $TiN/HfO_2/Hf/HfO_2/TiN$ structure [130] d) I-V characteristics of the device given in (c)

The state of the cell is determined by the state of both RRAMs connected in CRS. Generally, CRS devices offer three distinct states: HRS‘ 0’, HRS’1’ and ON-state, in which the data can be stored in either HRS ’1’ or ’0’ state. This device performs the write ‘0’/ write’1’ with 5 V pulse and −7 V pulses, respectively. Similarly, another anti-serial configuration of RRAM device with $TiN/HfO_2/Hf/HfO_2/TiN$ structure [130] exhibits CRS characteristics as given in Fig. 2.27(c) and (d). Yet another example for such anti serial formation of CRS cell is with $Pt/Ta_2O_5/Ta/Ta_2O_5/Pt$ device presented in [131].

From the above devices, it is interpreted that the sneak path current is suppressed at a low voltage regime by the serial resistance of RRAM devices. Nevertheless, the shared electrode at the middle of active layers increases the process complexity in 3D architecture, and the degradation probability of the common electrode is also high [132]. Moreover, the presence of an electrode at the middle of active layers form additional interfaces and may

introduce ambiguities in device operation. Therefore, several single layers and bilayer RRAM devices are engineered to obtain the CRS functionality.

Several CRS devices developed from a single sandwich structure; for example, Pt/Cu_2O/FTO is a device that exhibits a high resistance ratio and good retention characteristics, in this case, the CRS is obtained without the forming process. Likewise, the TiN/HfO_2/Pt device also displayed CRS behavior, which can be explained due to the change in the conduction filament properties such as shape and size due to redistribution of oxygen vacancies [133]**.** Similarly, several bilayer devices also exhibit CRS characteristics. For instance, TiO_x/Al_2O_3 device initially shows resistive switching behavior, while after multiple cycles, the device has undergone RESET failure and thereby transit to a CRS behavior as shown in Fig. 2.28. However, the read window associated with the device seems to be very small <1 V [134].

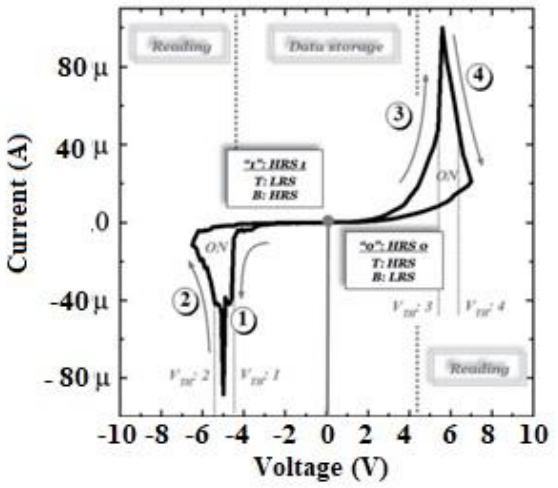


Fig. 2.28 CRS behavior shown by HfO_2/Al_2O_3/TiO_x device[128]

Al/Ni/$NiAlO_x$/Al_2O_{3-x}/ITO is another bilayer structure capable of producing the CRS behavior achieved with the redistribution of oxygen vacancies in $NiAlO_x$/Al_2O_{3-x} layers [135]. Recently, a tri-layer device is also reported to be used as the CRS device made of HfO2/TiOx/Al2O3 layers [136], where the CRS switching originated in TiO_x layer, and Al_2O_3 is acting as a tunneling layer due to its small thickness around 2 nm.

Table 2.3 Comparison across various solutions to mitigate sneak path current

Parameters	1D1R	1T1R	1S1R	CRS
Conduction phenomenon of switch	Unidirectional tunneling	Zener tunneling/electronic conduction	Bidirectional Tunneling	No switch
Disadvantages	Low nonlinearity Unipolar, Low reverse bias current may lead to loss of switching character at negative polarity	Low nonlinearity Large area, scaling problem, complex fabrication process	Non-compatible selector and RRAM leads to unexpected results; electrode materials of 1S and 1R should be the same	Destructive read, Shared electrode in back-to-back RRAM leads to poor design
Advantages and Applications	Application where self-rectification required, write-once-read-many memories	Neuromorphic Network, Boolean logic [109] NOR flash-like and embedded nonvolatile memory applications [136]	Neuromorphic computing, Boolean logic implementation, high-density flexible memory arrays [123], combinational circuits such as adders [137]	Neuromorphic High density, logics , Moore and mealy logic implementation ,Flexible RRAM devices [135]
Variations in design	Zener diode[104] PN junction diode[102] Tunnel diode[102] Schottky diode[100]	TFT [107] PNP [110] MOSFET [108][109]	Tunnel [122]/ Crested barrier based [80] Analog [122]s,[123]/Digital [126]	Back to back connected RRAM [130] Single layer [133] bilayer [134]

2.1.12. Self-rectifying single memory devices

Use of RRAM devices with self-limited, self-rectifying characteristics are recent trend in the field to eliminate sneak path current. Most of the self-rectifying memristors are made of single stack structure with low reverse current, and their I-V characteristics emulate the

characteristics of a 1D1R structure. The self-rectifying feature of such devices arises from its asymmetric structure/barrier due to Schottky contact or asymmetric potential in the device [106].

While comparing various aspects of 1D1R, 1T1R, 1S1R, and CRS devices as in Table 2.3, it can be understood that 1S1R and CRS designs outweigh the other two in many ways, such as the implementation of high-density applications, low sneak path current, and high nonlinearity.

Even though many devices with 1S1R and CRS behavior are reported, researchers are experimenting with different materials to attain better features. Therefore, the fabrication and modeling of integrated 1S1R devices and CRS are of prime importance. Moreover, additional studies are required to understand the scope of self-rectifying devices to contribute to the field.

2.8 Research Gaps in the Field of RRAM technology

While performing the literature review of RRAM models and devices, a few research gaps are identified in the field, which are given as follows.

1. In order to eliminate the unwanted leakage current (sneak path current) present in a crossbar array, 1S1R is found to be a better solution, though, to understand the performance of selector in 1S1R circuit, a comprehensive analytical model of selector based on the physical concept is required. Moreover, to study the behaviors of the selector with other electronic components, it is essential to have a circuit model of the selector device. Therefore, proposing an analytical and electrical model of selector device/ complementary resistive switching (CRS) device can helps further progress of RRAM technology.
2. Further, it has been observed that an analytical or electrical model of 1selector with Ox-RRAM (integrated models) is also missing in the literature, which is a highly needed circuit to understand the working of 1S1R in a crossbar array.
3. As mentioned in the previous section, CRS devices are developed based on back-to-back configuration of RRAMs, but it is evident that the middle metal electrode sandwiching between the active layers is instead a poor design, and it may lead to the formation of multiple interfaces, which may also make the device operation uncertain and increases the complexity of process flow. Therefore, a more sophisticated design without an intermediate metal layer would be a better solution.

4. The devices with multilevel characteristics and high nonlinearity have the potential to reduce sneak path current whilst offering high-density memory design; hence such a device implementation can be helpful in progressing the memory technology.
5. Recent studies are focusing on simple RRAM devices that can contribute to the sneak current problem while still in its infant stage. Hence developing such RRAM devices would open up another broad area for research.
6. The I-V characteristics of several RRAM devices ($Pt/Ta_2O_5/TaO_x/Pt$ in particular) exhibit current conduction while extending the input voltage beyond its RESET voltage. However, the exact reason behind this phenomenon has not been explained or proved with the analytical or electrical modeling approach. Besides, the prevailing models are developed by modeling the current transport through the conduction filament, ignoring the contribution of the large area present outside of the nanoscale conduction filament (OCF), which gives an opportunity to study the influence of the current conduction through OCF on the current present in the device after the RESET voltage.
7. Similarly, the study of $Pt/Ta_2O_5/TaO_x/Pt$ RRAM device lacks its variability analysis and is unable to explain the effect of oxide charges present at the interface, significance of radius of the filament formed during each cycle on switching characteristics. Therefore, several possible aspects leading to the variations in current is an interesting area to contribute.

Chapter 3

Research Methodology

Chapter summary

The chapter discusses the methodology adopted in the presented research comprising analytical modeling, electrical modeling, and RRAM device fabrication. The analytical modeling strategy is adopted to develop the RRAM, Selector, and 1S1R cell models, whereas electrical modeling methodology is adopted to create selector, RRAM,1S1R, CRS, and the crossbar arrays. Besides, the fabrication and electrical/structural characterization methods are also included. Moreover, the instruments involved in RRAM, CRS cell fabrication are precise atomic layer deposition (ALD), thermal evaporation and FESEM analysis, etc. In addition, each section explored standard tools and analyzers used for developing the models such as LTSPICE, MATLAB, CADENCE, etc.

The research methodology discusses in this chapter involves the systematic procedures followed to find the solution to the research problem stated in chapter 1. The methodology is classified based on the developmental stages and tools involved in the analytical and electrical modeling and the fabrication methods and tools utilized to realize RRAM devices.

2.9 Methodology to develop analytical models of selector and RRAM devices

A flow chart demonstrating the methodology to develop analytical models is shown in Fig. 3.1. It explains the steps followed while developing the analytical models of a selector, RRAM, and 1S1R combination.

Initially, the analytical model of the selector device was developed in MATLAB tool built on the physical concepts of tunneling of electrons across the multilayer selector device structure with the help of energy band diagrams. After that, the model parameters are selected based on the type of materials used in the device structure. These parameters include electric field, dielectric constants, the thickness of oxide, electron mass, etc. Then the model has been plotted using graphing software. Meanwhile, the experimental characteristics of the real device presented in [121] is calibrated with standard tools. In the next step, the model has been validated against the experimental data to find if there is any discrepancy, then the parameter values are to be revised to ensure the precision of the model. Finally, the optimized model is generated.

Next, the same procedures are followed for developing the analytical model of RRAM, where an additional current component ‘trap assisted tunneling conduction’ is included in addition to conduction filament limited Schottky barrier modulation and the tunneling, which influences the current conduct through the device after its RESET voltage. The additional parameters included in the model are the electric field external to the CF, diffusion of vacancies across the CF boundary, number of oxygen vacancy traps, effective barrier across the Schottky junction, the concentration gradient of oxygen vacancies, etc. Then, as illustrated in the flow chart, the validation of the current value is done against those data calibrated from the experimental [32] values, and the final model is generated.

Further, the 1S1R is developed by following the same methodology as discussed above, where the parameters accessed in the design are the electric fields across RRAM and selector, minimum of the current flow through device etc. From the combined characteristics, the model’s non-linearity, the magnitude of OFF-current, and memory window are evaluated to

verify the potential of 1S1R model to reduce the sneak path current. Moreover, to use in crossbar array, the read/write voltage biases to be applied on both selected and unselected bit/word lines are also predicted. But the design lacks the validation step as there is no experimental results available for the proposed RRAM-selector combination.

3.1.1. Flow chart

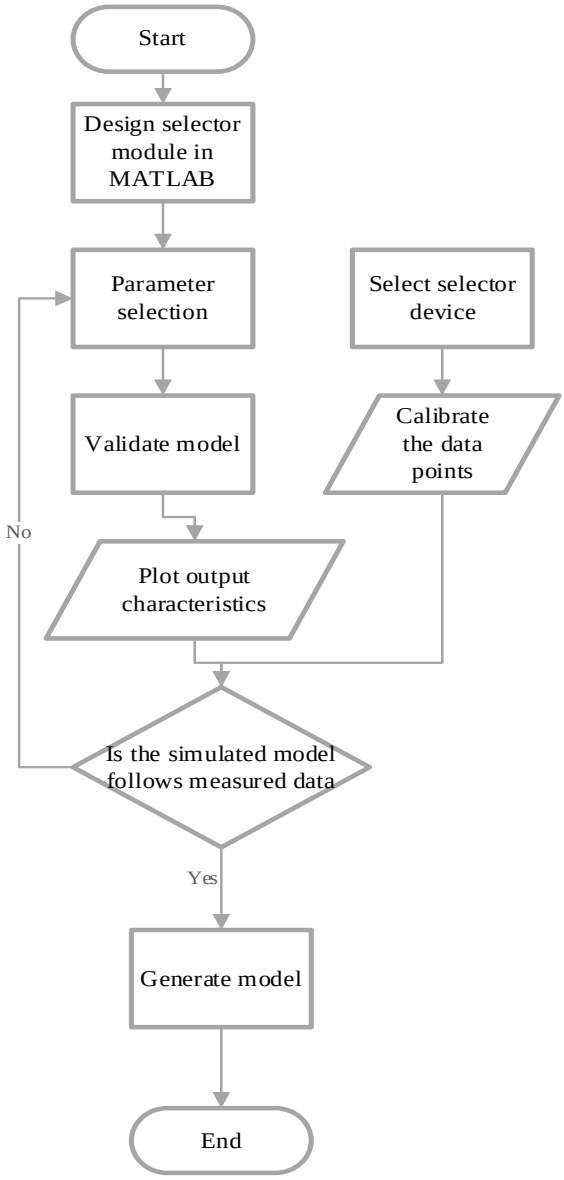


Fig. 3.1 Methodology adopted to model aanalytical model of the selector, RRAM and 1S1R devices

3.1.2. Tools utilized to develop analytical model

1. MATLAB R2020a is the tool used for developing the analytical model of the selector, 1S1R and the model of Pt/Ta_2O_5/TaO_x/Pt.
2. Band energy program software is used to analyze the band energy diagram in multilayer devices.
3. Calibration tools and graph analyzers utilized in the analytical modeling are Digitize it, Origin Lab and Graphpad Prism

2.10 Methodology to develop electrical models of selector, RRAM, 1S1R and CRS devices

To study the response of 1S1R devices in circuit simulations, an electrical model of selector device is developed using LTSPICE simulation environment and the resulting characteristics have been validated with the experimental I-V characteristics of the selector device given in [121]. The dynamic parameters derived using the model library are electric field, effective barrier of tunneling and the static parameters such as switching layer thickness, dielectric constant, effective mass of an electron etc. These parameters are selected based on the material property of the dielectric layers, which govern the magnitude of current provided by the current source. The range of input voltages required to operate the device and the parameters required for the quantitative and reliability analysis of the model such as on-current density, Roff/Ron ratio, magnitude of off-current as well as the memory window are also extracted from the model.

In order to demonstrate the methodology followed to develop electrical models, a flow chart is drawn which is shown in Fig. 3.2 in which the first step is to define the device specifications, then develop the model design using the model library. On subsequent step, select the parameters and assign values. At the same time collect the measured data of selector as well as RRAM, subsequently validate it with the model. At this point, if data does not match with model, refine the parameter values and fitting parameters, and simulate again. On the other hand, if data matches with model, generate the subcircuit and which can be included in the library as a third-party model to use as an instance/ component for further use. However, the 1S1R model subcircuit can be established at this step as no experimental data is prevailing to validate.

3.1.3. Flowchart

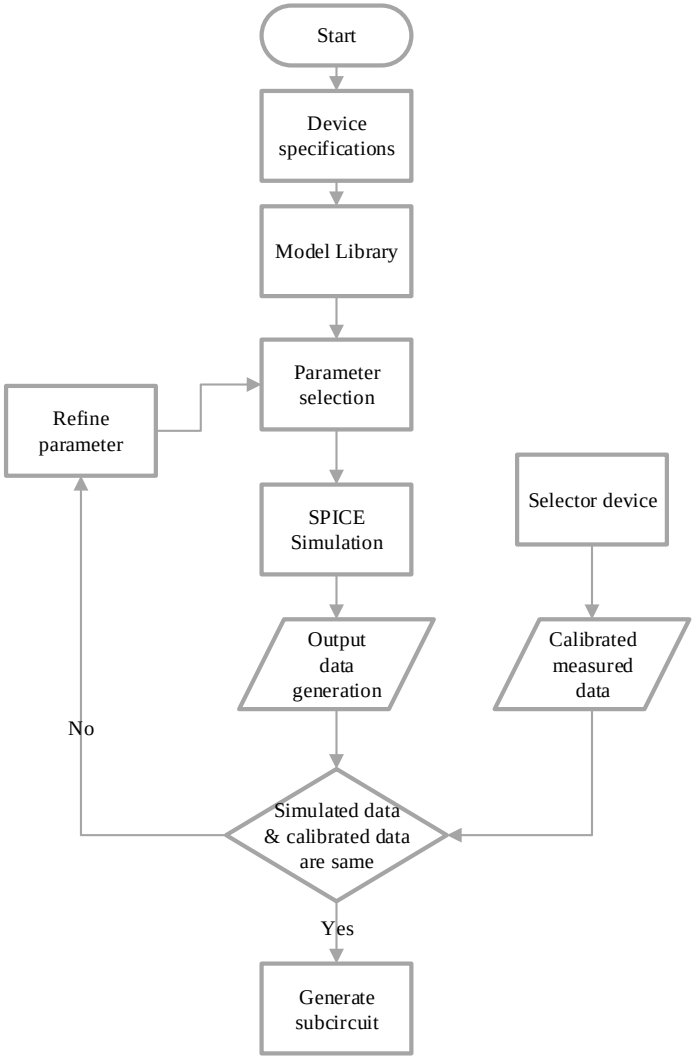


Fig. 3.2 Methodology adopted to model Electrical/ circuit model of the selector RRAM devices

The additional voltage/ current sources are included in the existing $Pt/Ta_2O_5/TaO_x/Pt$ RRAM model to implement the current through OCF. In the final step, the model data and calibrated data are validated. Finally, the accurate sub-circuit is developed.

The proposed RRAM model is integrated with the proposed electrical model of selector to form 1S1R circuit. The subsequent I-V characteristics of the model are extracted to analyse the acquired features of the combined circuit conducive to the sneak current reduction. The parameters predicted are, the SET voltage, RESET voltage, read voltage, read margin etc.

Lastly, different 2x2 CBAs are created by combining the proposed electrical model of the selector with HP memristor, Yakopcic model, Stanford-PKU model, and $Pt/Ta_2O_5/TaO_x/Pt$ RRAM model in circuit level and read/write voltage and reduction in sneak path current is

calculated. In addition, the CRS array of HP memristor has also been modeled using LTSPICE tool. The following section explains the tools used to develop the model.

3.1.4. Tools utilized to develop the electrical model

LT SPICE XVII is the tool used for developing the electrical model/circuit model of 1S, 1S1R, RRAM, CRS. Calibration and graph analyzers: Digitize it, Origin Lab, GraphPad Prism.

2.11 Methodology to fabricate the RRAM device, CRS device, and multilevel device

a) Identify the materials with switching properties and deposition methods to be used to obtain the RRAM device and CRS device.

b) Realize a RRAM device with a single active switching layer and inert electrodes.

c) Perform data analysis on the results of electrical and structural characterization of the device

d) Develop a novel CRS device by stacking two active switching layers, thereby eliminate the use of middle electrode as in the design of conventional CRS fabrication.

e) Further, the structural characterization of the device is performed using the ellipsometer and FESEM with EDX analysis.

f) Electrical characterization is conducted to analyze the I-V characteristics of the device and various studies have been performed to analyze the device performance on read and write operations.

g) Further, the reliability measures of RRAM devices such as endurance and retention are measured using the source measurement Unit (SMU).

h) Moreover, the device has been optimized by fabricating different devices with varying active layer thickness and with another top electrode.

i) From the calibrated data, the analysis has been conducted with the help of graphing tools. Thus, the underlaying conduction mechanism and switching mechanism of the device are derived to investigate the device's working.

The tools used for the fabrication, characterization, and analysis of devices are given in sections 3.3.1 and Fig. 3.3.2 show the methodology followed to develop RRAM and CRS devices

3.1.5. Calibration and data analysis tools

1. Origin Labs and Graph pad Prism
2. Microsoft VISIO, Band diagram Program, and FEI Quanta 400F FESEM with EDX

3.1.6. Flow chart

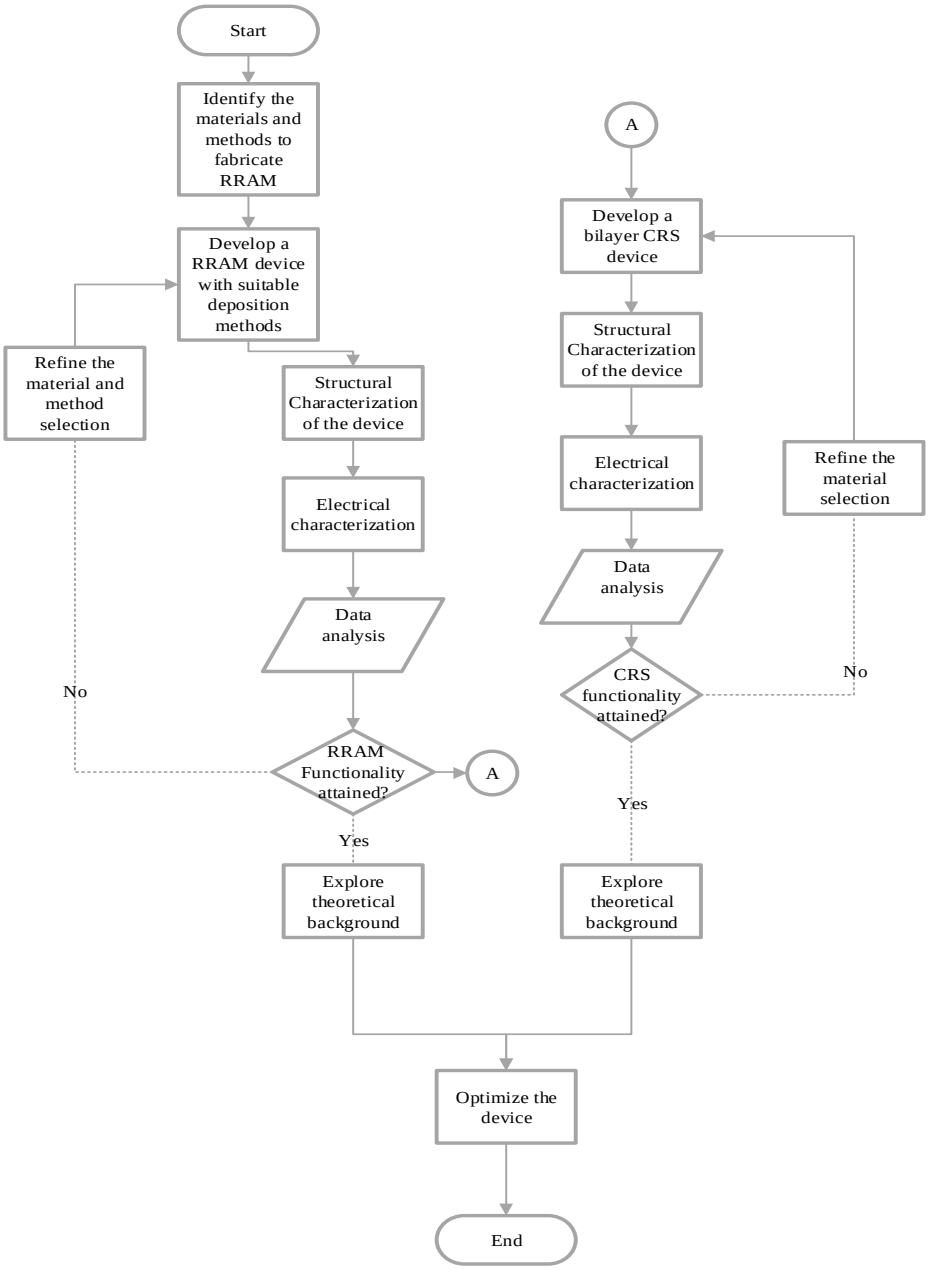


Fig. 3.3 Methodology followed to develop RRAM and CRS devices

3.1.7. Approaches/ instruments used for the Fabrication of RRAM/CRS device

3.1.7.1. Material selection

Various materials exhibiting resistive switching behavior are identified at the initial stage, such as Al_2O_3, HfO_2, ZnO in order to achieve the CRS/1S1R/1D1R structure. Even though the modeling is performed on various transition metal oxides such as Ta_2O_5, HfO_2, and, TiO_2, different metal oxides are opted for the experiment procedure such as Al_2O_3 and ZnO because of the cost/availability of the materials and accessibility of the instrument to process/deposit those specific materials. Sample preparation stage. Various active/inactive electrode materials such as FTO, Au, and Ag have been selected based on the availability of materials, precursors, and deposition method. Most importantly, it is ensured that the device stacks developed in the study are novel.

It is the first stage in the fabrication of the device. Initially, the FTO coated glass substrate has been cut and cleaned with acetone in a sonicator. Subsequently, the sample has been cleaned with IPA and distilled water. At the final stage, the surface is cleaned with N2 gas.

3.1.7.2. Active layer deposition Process

The active switching layer is deposited using HHV's high-quality atomic layer deposition (ALD) technology. The atomic layer deposition (ALD) system is configured to deposition material on a substrate in a controlled manner while maintaining the vacuum conditions throughout the process. The vacuum condition is achieved through the vacuum pump, which ensure a low pressure in the chamber. In our experiments, the vacuum level achieved is approximately $3X10^{-1}$ m bars. Similarly, the temperature inside the chamber is controlled by using a thermocouple associated with the reaction chamber and the computer program associated with the heaters. The process chamber is equipped with dual-stage rotary pump, and the substrate holder in the chamber is static, which is designed to accommodate a maximum of 100 mm diameter wafer. The chemicals used for the deposition are known as precursors. To deposit the required material, its precursors (materials) in the gaseous state should be loaded through the valve to enter the chamber. The deposition occurs sequentially, that means one after another based on the pulses applied. During deposition, the precursor along with oxidizer let into the chamber for a specified time to react with the substrate and a thin layer deposition takes place due to chemical reactions. After one precursor's deposition (Al_2O_3), during the next cycle high purity N2/Ar pulses are provided to purge out the unreacted

gases and byproducts. On subsequent cycle another precursor valve allows the gas to enter the reaction chamber to form another deposition (Eg. ZnO) followed by the influx of N2 gas. Further, the thickness of the film deposited in ALD is measured based on the GPC (growth per cycle), where the thickness of deposition layers grows incrementally per cycle of deposition, where the thickness can be controlled by limiting the number of ALD cycles. Fig. 3.4 shows one ALD cycle associated with a specific material deposition. Also, Fig. 3.5(a) shows the ALD instrument used in the experiment, Fig. 3.5(b) depicts the software interface to set up the recipe.

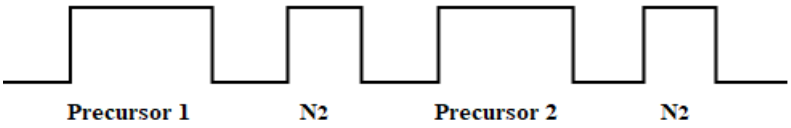


Fig. 3.4 One ALD cycle consisting of pulses of precursors with purged gas



Fig. 3.5 (a) ALD system set up (b) ALD software for the setting the program

3.1.7.3. **Thermal Evaporation system**

A thermal evaporation system is used for evaporating low melting point materials for creating multilayer thin-film structures. In this experiment, the instrument used for the thermal evaporation is the Fillunger high vacuum thermal coating system, as shown in Fig. 3.6 (a). Using the instrument, the top electrodes such as Ag and Au are deposited. The instrument consists of a reaction chamber comprising a resistive heating source, wafer holder, opening of vacuum pump, a piezo electric crystal oscillator, etc. The resistive heating source is in the form of a boat which holds the material to be evaporated/deposited on the substrate. The wafer would be placed in the wafer holder, which rotates above the metal boat, and subsequently, the high vacuum-based ($7x10^{-5}$ Torr) evaporation occurs. Further, the thickness measurement is carried

out using a piezoelectric crystal oscillator connected with the deposition setup. As the material deposits on the crystal surface, its frequency of oscillation changes, and by measuring it, the thickness can be measured.



Fig. 3.6 Thermal evaporation system complete setup

3.1.7.4. **Characterization tools**

Agilent technologies B2912A Precision Source/Measure Unit (SMU) and the probe station are used for conducting electrical characterization. The characterization is performed after keeping the samples at room temperature and in dark conditions. The probe base is shown in Fig. 3.7(a), and the probe station chamber is shown in Fig. 3.7(b)

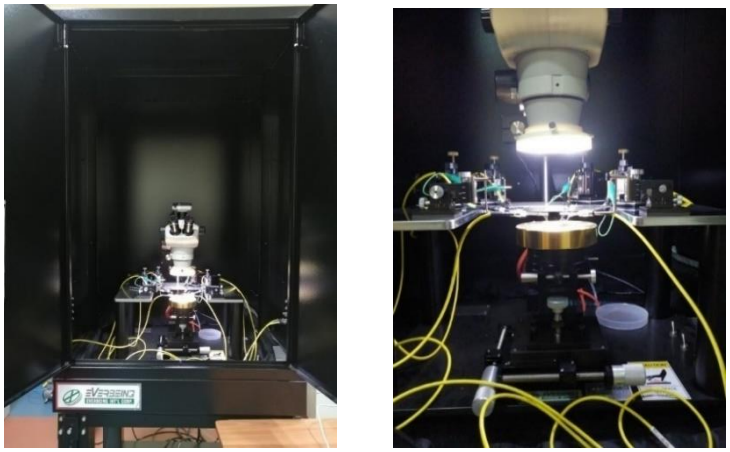


Fig. 3.7 Characterization tool (a) Probe station base (b) Probe station chamber

3.1.7.5. **Tools used for structural analysis**

a) Ellipsometer: Ellipsometer is used for the thickness optimization of ZnO coating. The model used for fitting ZnO coating is Cauchy-Urbach.

b) Field Emission Scanning Electron Microscopy with Energy Dispersive X-ray Spectroscopy (FESEM with EDX): The surface morphology, cross-sectional analysis, and the EDX analysis have been carried out using the FEI Quanta 400F FESEM.



Fig. 3.8 FEI Quanta 400F FESEM device used for the structural analysis of the device surface and cross section

3.1.7.6. **Prepared samples**

The substrate used to fabricate the sample is FTO coated glass with 7 Ohm/mm resistivity and the FTO (Fluorine doped Tin oxide) conductive material itself is used as the bottom electrode.

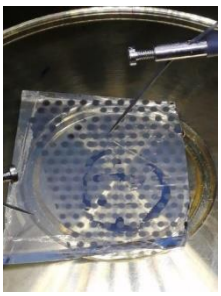


Fig. 3.9 Prepared sample

All measurements in the experiment are taken with respect to the Au top electrode, and the bottom electrode kept at the ground. Several devices are fabricated on each sample, as shown in Fig. 3.9, where each dot represents a device. Multiple devices are defined with the help of a shadow mask of area ~1mm^2 .

Chapter 4

Resistive random-access memory (RRAM): Analytical and electrical modeling approach

Chapter Summary

An analytical, and electrical model of Pt/Ta_2O_5/TaO_x/Pt RRAM device incorporating the phenomenon of increased current conduction beyond the RESET phase, has been modelled by introducing a state independent current conduction mechanism known as trap assisted tunneling (TAT), where additional current is contributed by the oxygen vacancy traps present at outside of the conduction filament (OCF). Also, the variability present in the Ta_2O_5/TaO_x device is modelled where the possible reasons of variability are the formation of unstable sub filaments, varying radius of the conduction filament, barrier height modulations due to change in number of oxygen vacancies at interface as well as at bulk. Further the simulation results revealed that multiple resistive levels are due to the formation of multiple filaments, the radius of the filament affect RESET voltage, and slight modulations in tunneling barrier causes randomness in high resistance state of the device. Meanwhile, the electrical model is developed by implementing the dependent current sources representing the bulk transport of electrons across the Ta_2O_5 layer outside of the conduction filament. Moreover, the model takes account of the variable number of oxygen vacancy traps at the bulk by incorporating the Fick's diffusion. Further the proposed model has been tested under various standard signals and its results are verified.

Related Publications

1. A. L. Jagath, T. Nandha Kumar and H. A. F. Almurib, "Electrical model of Ta_2O_5/TaO_x RRAM device with current conduction beyond RESET phase," 2019 IEEE 9th International Nanoelectronics Conferences (INEC), Kuching, Malaysia, 2019, pp. 1-5,

2. A. L. Jagath, T. Nandha Kumar and H. A. F. Almurib, "Modeling of Current Conduction during RESET Phase of Pt/Ta_2O_5/TaO_x/Pt Bipolar Resistive RAM Devices," 2018 IEEE 7th Non-Volatile Memory Systems and Applications Symposium (NVMSA), Hakodate, Japan 2018, pp. 55-60, doi: 10.1109/NVMSA.2018.00014.

This chapter discusses the Resistive random-access memories (RRAMs) suitable to combine with the proposed selector to study the effect of the selector to reduce sneak path current in a crossbar. Several RRAM devices are made of transition metal oxides (TMO) such as HfO_2, Ta_2O_5, NbO_2, and TiO_2. Among these TMOs, Tantalum devices with bilayer structures show better memory properties. In Tantalum based RRAM devices, $Pt/Ta_2O_5/TaO_x/Pt$ [138], is found to be a potential candidate to configure with the proposed selector due to its device structure with Pt top electrode enables it to serially connect with $Pt/Ta_2O_5/TaO_x/TiO_2/Pt$ selector as both can share the same electrode (Pt). Likewise, the voltage and current levels of the RRAM is also comparable to the selector device.

However, in the I-V characteristics of $Pt/Ta_2O_5/TaO_x/Pt$ RRAM device, the current flow occurs through the device beyond its RESET voltage, which is not captured in the existing models. Hence this chapter includes further studies conducted to obtain the exact device characteristics of Pt/ $Pt/Ta_2O_5/TaO_x/Pt$ by considering the current conduction through outside of the conduction filament (OCF), responsible for the additional current component present beyond the RESET voltage. Moreover, the factors affecting the variability of $Pt/Ta_2O_5/TaO_x/Pt$ device is also not yet known, therefore a model proposing the possible reasons behind the variability is also developed analytically. In addition to $Pt/Ta_2O_5/TaO_x/Pt$ device, a few more existing RRAM models are also adopted to use in this chapter, such as the Yakopcic model, HP model, Stanford model, etc.

In RRAM devices, the stop voltage is responsible for the device to undergo RESET to reach HRS. The applied stop voltage can be greater than or equal to the RESET voltage of a device. However, in some devices, on response to a stop voltage, the device RESETs initially and on further increase in voltage causes the current to increase so that to reach LRS level. The reason for such phenomenon is important because the high stop voltage or noise spikes may cause the device to reach at LRS, which affects the device's reliability. Hence the response of the device beyond its RESET voltage has a major role in the field. Next section discusses the analytical as well as electrical model of the $Pt/Ta_2O_5/TaO_x/Pt$ device incorporating the additional current component present beyond the increased RESET voltage followed by the proposed variability model.

2.12 Analytical Modeling of $Pt/Ta_2O_5/TaO_x/Pt$ RRAM device

The I-V characteristics of Pt/ $Ta_2O_5/TaO_x/Pt$ device and its existing model are given in Fig. 4.1, where the device exhibits an abrupt SET switching at a voltage ~ -1.2 V and a gradual

RESET switching at a voltage of ~2 V. Besides, it is observed that when the applied voltage increases beyond the RESET voltage, an interesting phenomenon of a substantial reduction in the resistance of the device is observed [78], [139], [140] resulting in the device current to reach approximately close to LRS level as shown in Fig.4.1 [86]. Several models are existing to study the device characteristics, though their characteristics do not follow the device characteristics beyond its RESET voltage. For instance, the characteristics obtained from an existing model is plotted in Fig. 4.1, where it does not follow the experiment data after the RESET voltage (~2V). This is mainly important as further increase in the reset voltage increases the conduction causing more current to flow. Therefore, in this chapter, an analytical model is proposed that incorporates the increase in current beyond the RESET voltage.

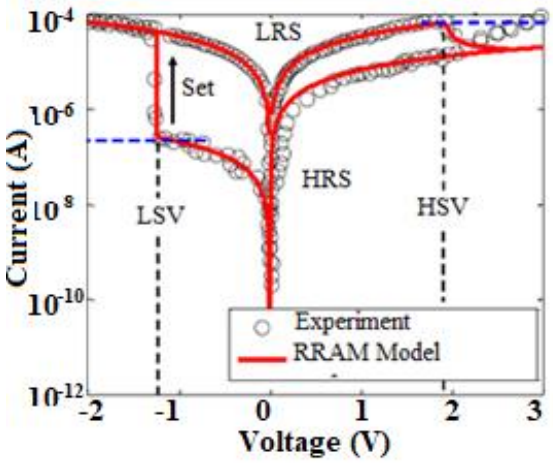


Fig. 4.1 Experimental characteristics of RRAM device [32] and its corresponding analytical model [31]

The current conduction through CF and resistive switching concepts of the presented model is adopted from [31] , where the electronic current conduction is modelled with Schottky emission concept which incorporates tunneling probability to include the effect of tunneling through the CF, thus the thermionic emission of electrons and its magnitude is expressed in [31] as

$$\mathrm{I} = AA^{*}T^{2}exp\left(\frac{-\emptyset_{Bno}}{V_T}\right)exp\left(\frac{V-IR_{series}}{\eta V_T}-1\right)exp\left(-\sqrt{\xi}w\right) \qquad 4.1$$

The first two exponential terms with pre-exponential factor denote the Schottky emission with applied voltage V, barrier potential $\emptyset_{Bno}$ and η is the deviation from the ideal metal-semiconductor junction due to the presence of traps at the depletion region. R_{series} is the

total resistance of the device. The third exponential shows the contribution of tunneling current through CF on Schottky emission where ξ is the effective barrier height and w is the thickness of insulator volume [31] ,V_T, is the thermal voltage. The resistive switching mechanism of the proposed model is realized with the Mott-Gurney ionic/vacancy hopping mechanism, which is adopted from [31]. In that model, the average ionic drift velocity under applied electric field (E) across the gap region is given in [31] as :

$$\frac{dw}{dt} = a.c.exp\left(\frac{-U}{KT}\right) sinh\left(\frac{qaE}{2KT}\right) \quad 4.2$$

Where, U is the intrinsic barrier for ion hopping, c is the attempt-to-escape frequency, a is the effective hopping distance, K is the Boltzmann constant, E is the electric field at CF region which is estimated with varying gap length (w) across the top electrode and conduction filament (3) which is obtained from [31] as given below:

$$E = \frac{V}{w+\frac{R_{on}}{R_{off}}(D-w)} \quad 4.3$$

Here, E is electric field across the CF region, R_{on} and R_{off} are the on-resistance and off resistance of the device respectively. D is the thickness of the device in nm and w is the gap length between the top electrode and CF tip.

In the device characteristics, the current through outside of conduction filament (OCF) emerges while the device is in HRS, therefore the additional current component is considered as the leakage current. Even though several conduction mechanisms such as Poole-Frenkel, variable hopping, or F-N tunneling can be used to model the leakage current, trap assisted tunneling suits well with the measured current characteristics. Hence in the proposed model, the conduction behavior of leakage current at OCF is modelled with Trap assisted tunneling (TAT) conduction mechanism.

In TAT, the electrons tunnel through oxygen vacancy traps existing in the dielectric material at OCF (in this case, Ta_2O_5). These vacancies in bulk are originated from the electroforming and diffusion process [141]. During the electroforming process, oxygen vacancies are created in the entire volume of the material, though the concentration of vacancies form a percolating path to form CF [141]. However, the isolated oxygen vacancies created in the OCF area act as intermediate jumping sites for the electron to tunnel. Another source of Oxygen vacancy at OCF is the diffusion that occurs at LRS. In this work, it is assumed that the SET process creates a concentration gradient across the device's width, which causes

diffusion of oxygen vacancies from CF to OCF; thus this lateral diffusion contributes to leakage current [141]. The distribution of traps across the device's width is modeled with Fick's second law [46], which defines an error function to calculate the concentration of vacancies at a distance from the CF region.

Tunneling of electrons through the traps at OCF occurs at forward bias, whereas at reverse bias conditions, the highly conducting CF provides a lower resistance path. At low positive voltage, the current through OCF is negligible due to the highly insulating nature of the dielectric [46], but at a high positive voltage, the filament ruptures, and it forces the current to follow the OCF path. Although the thickness of the insulator at OCF remains constant, the electric field across the non-filament area increases with an increase in applied potential. The electric field across the outside conduction filament for the device Pt/Ta_2O_5/TaO_x/Pt is low as ~ 3V/nm; hence trap assisted tunneling (TAT) becomes the suitable mechanism to model the current conduction [142].

In TAT, the potential barrier for the electrons to tunnel is lowered by the doping effect of oxygen vacancies at the insulator layer. In this barrier lowering process, oxygen vacancies at OCF are facilitated as an intermediate jumping site for electrons. This trapping and de-trapping of electrons can be explained with the concept of energy bands. Since the insulator material (Ta_2O_5) has a large bandwidth of ~4.4 eV [143], electrons cannot pass to the conduction band directly. However, energy bands/states created within the bandgap of the insulator material due to the presence of traps provide a conductive path for the electrons to excite and move to the conduction band [144] by lowering the effective barrier.

The potential barrier form in oxide material can be explained with energy band theory. When an oxide is in contact with the metal, the fermi-levels align, resulting in band bending; thereby, the potential barrier seen by the electrons can be either a triangular shaped barrier or a trapezoidal-shaped barrier. In conventional TAT, the current is contributed by electrons that overcome the triangular barrier only. In contrast, in GTAT, electrons that overcome triangular and trapezoidal energy barriers are considered for modeling the TAT conduction [46]. The following sections discuss conventional TAT with the modified barrier, followed by the two-step GTAT process with variable trap density (N_{t1}).

4.1.1. Modeling of OCF conduction using Conventional Trap Assisted Tunneling

The device's Pt/Ta2O5/TaOx layers are considered a Metal-Insulator-Semiconductor (MIS) structure with oxygen vacancies present at the insulator layer. Since the thickness of the insulating layer is small (4 nm) enough for the electrons to tunnel through, as discussed in the previous section, the current through OCF is modeled as TAT conduction. In conventional TAT, an exponential relation is held between the current and trap energy level [142], while this section introduces a modified barrier term by considering the effective barrier that is determined by both Schottky barriers and trap energy level, where the effective Schottky barrier is evaluated by considering the effect of barrier lowering term. To contribute to TAT, the electrons need to overcome a potential barrier of effective height $\phi_x^{3/2}$-$\varphi_t^{3/2,}$ and the shape of the barrier is assumed to be triangular [145]. An effective barrier across Pt/ Ta_2O_5

Schottky junction is given in [31], which is expressed as:

$$\varphi_x = \varphi_{actual} - \Delta\varphi \qquad 4.5$$

In equation 4.5, φ_x is the effective potential barrier across Pt- Ta_2O_5 Schottky junction, $\Delta\varphi$ is the barrier lowering term which is due to the effect of electric field and image force. It is observed that at the RESET phase, an average rate of change of electric field at the outside of the filament region is high compared to the change in the field across CF. The current flows at OCF is modelled with TAT as given in (4.6), where E1 is the electric field (4.7) across OCF, which changes linearly with applied potential across the dielectric layer:

$$I_{TAT} \ \alpha \ A * \exp\left(\frac{-4*\sqrt{(2*e*m_{ox})}\left|(\varphi_x)^{3/2}-(\varphi_t)^{3/2}\right|}{3*h*|E1|}\right) \qquad 4.6$$

$$E1(t) = \frac{V_{Ta2O5}(t)}{D} \qquad 4.7$$

where A is the electrode area, m_{ox} is the effective mass of electron in the oxide layer, e is the electronic charge, φ_x is effective barrier height seen by electrons in the metal. φ_t is the trap energy level below the conduction band edge. The magnitude of the electric field (E1) is considered in (4.6) since current flow occurs through the OCF at forward bias.

The next sub-section describes the implementation details of the Generalized TAT (GTAT) conduction mechanism, an improved model of TAT put forward by Houng et.al [142].

4.1.2. Modeling of Conduction through OCF with Generalized Trap Assisted Tunneling (GTAT)

GTAT is a two-step tunneling process where the electrons tunnel from metal to the trap state in the metal oxide (Ta_2O_5) with a probability of P_1. Subsequently, electrons de-trap to the conduction band of semiconductor (TaO_x) with a probability of P_2.

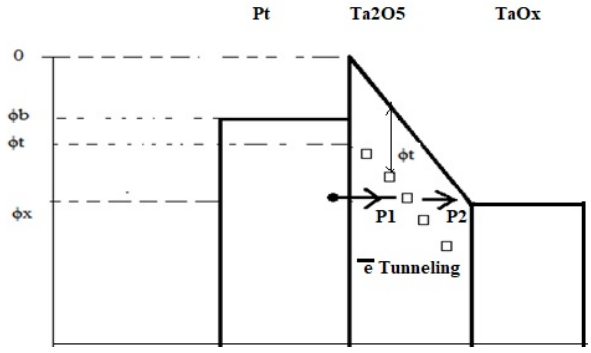


Fig. 4.2 Schematic energy diagram of metal-insulator semiconductor structure

For a given voltage, electrons that tunnel from metal to oxide can see either triangular or trapezoid potential barrier [142]. The schematic of the energy band diagram showing the barrier formation is shown in Fig. 4.2 in that the probabilities P1, P2, and the trap energy level are marked.

The tunneling current in GTAT is contributed by the electrons that tunnel through both barriers. However, the trapezoidal barrier dominates at low voltages, and it contributes additional tunneling paths, while tunneling through the triangular barrier dominates at high voltages [142]. It can be explained as; at the low applied voltage, the conduction band of the oxide bends at a lesser extent which indeed forms a trapezoidal barrier and tunneling of electrons through this barrier contributes major component of leakage current. In contrast, at high voltages, the band bends more to form a triangular barrier. Consequently, the triangular barrier contributes more leakage current at high voltages. Even though the total current in the device after the RESET phase is contributed by electrons from both barriers, tunneling through a triangular barrier dominates. The current obtained from the GTAT model is given in [142], which can be quantified as:

$$I_{GTAT}\ \alpha\ \mathrm{A} * \int \mathrm{e} * \mathrm{C_t} * \mathrm{N_{t1}} * \left(\frac{1}{\mathrm{P1}} + \frac{1}{\mathrm{P2}}\right)^{-1} \mathrm{dx} \qquad 4.8$$

Where A is the area of OCF, the electroformed CF area is small as compared to the area of OCF [9]. However, the area of the device has a significant role in the current conduction

through outside filament [146]. The electronic charge is represented as 'e', P_1 is the probability of trapping an electron from metal to oxide and P_2 be the probability of moving an electron from a trap to semiconductor, C_t is the function of trap energy (φ_t) and the total energy of electron (E_0) as given in (4.9) which is constant for a given trap energy level [147].

$$C_t = \left(\frac{m_{no}}{m_{ox}}\right)^{5/2} \left(\frac{8{E_0}^{3/2}}{3h\sqrt{(\varphi_t)-E_0}}\right) \qquad 4.9$$

Where m_{no} and m_{ox} are an effective mass of electrons in metal and metal oxide respectively. The solution for the current expression given in (4.8) is derived in [142] with each probability term has a dependency on φ_t. To assist tunneling, traps would be at shallow levels or near to the conduction band edge with the assumption that $\varphi_t > \varphi_b$, φ_b be the barrier height for Fowler-Nordheim tunneling [142]. These trap levels depend on vacancies in the lattice of the Ta_2O_5 unit cell, which comprises TaO_6 and TaO_7 polyhedra. Two types of vacancies are reported in Ta_2O_5 based on the vacancy in polyhedral namely, in-plane and cap vacancies; those are created from the base plane and the basal plane of polyhedral, respectively [159] can be obtained with density function theory (DFT). The trap energy levels created within the bandgap due to oxygen vacancies are displayed in [145], which clearly shows trap energy level around 2.1eV [145]. In this work, both tunneling approaches are implemented by considering φ_t and m_{ox} as fitting parameters. The trap energy required for TAT to fit the experimental data is ~ 2.2eV, $m_{no}$is assumed as $0.1m_0$ [147] and m_{ox} can have values from $0.3\ m_0$ to $0.5\ m_0$ [148], [149], [147], where m_0 is the mass of free electron while in the proposed model, m_{ox} taken as a constant ($0.3m_0$).

Another prominent factor to be considered while calculating the current at OCF is the trap density (N_{t1}). In RRAM devices, this parameter is no longer considered as a constant because the trap density at conduction filament and outside of the filament changes with diffusion owing to the concentration gradient of oxygen vacancies across the width of the device, which in turn causes an increase in the leakage current level at OCF. Hence in the GTAT model, rather than assuming the concentration of traps as a constant, variable density of traps $N_{t1}(x)$ at OCF is established. Here, the diffusion process responsible for variable $N_{t1}(x)$ is modeled with the assumption that the SET process set up a concentration gradient across the device's width, causing lateral diffusion of vacancies from CF to OCF [141]. These diffused oxygen vacancy traps enhance tunneling by reducing the resistance of the insulating layer. This lateral diffusion is modelled with Fick's second law, and the variable trap density is given in as in (eq. 4.10) [150]

$$N_{t1}(x) = N_t * \left(1 - \text{erf}\left(\frac{x}{2\sqrt{D_c * t}}\right)\right) \quad 4.10$$

Where N_t is the concentration of oxygen vacancies in the CF area with the assumption that CF filled with oxygen vacancy acts as a source of diffusion (Thin plane of maximum fixed concentration). x is the horizontal distance from CF, D_c is the diffusion coefficient which determines the rate of diffusion, t is the time parameter. Two parameters that affect the diffusion characteristics are the variation in the gradient of vacancies with distance from the surface of CF to OCF and the diffusion constant, which is calculated using (4.11) [141].

$$D_c = D_0 \exp\left(-\frac{Ea}{KT}\right) \quad 4.11$$

Where D_0 is the maximal diffusion. Ea is the activation energy that can take values from 1eV to 1.3eV, where T is the temperature [31], K is the Boltzmann constant. TABLE 1 shows the parameters used in the simulation of conventional TAT and GTAT in the proposed model.

Table 4.1 Parameters used in the simulation of proposed RRAM model

Parameters used in Proposed Model	**Symbols and Parameter values**	
	Symbol	***Value (TAT/GTAT)***
Trap Energy	φ_t	$2.3eV^{*}/2.2eV^{\#}$ [145]
The effective mass of electron in metal oxide	m_{ox}	$0.3m_0$ [148]
The effective mass of electrons in a metal	m_{no}	$0.1\ m_0^{\#}$ [147]
Mass of free electron	m_0	$9.1x10^{-31}$ Kg
Area	A	$9x10^{-9}m^{-2}$
Trap density at CF	N_t	$1x10^{20\#}m^{-3}$
Maximal diffusion constant	D_0	$2.6x10^{-3}nm^2s^{-1\#}$ [150]
Metal Oxide thickness	D	4 nm
Activation Energy	Ea	1.3 eV
The total energy of an electron	E_0	0.2 eV [147]

*Denotes parameter value used for TAT and # denotes parameter values used for GTAT tunneling. Parameter value with no symbols applies to both mechanisms.

4.1.3. Results and Observations

A MATLAB simulator is developed to implement the proposed RRAM model incorporating the current conduction beyond RESET, where leakage current through OCF is validated with conventional TAT and GTAT. The following sections discuss the simulation results. The I-V characteristics obtained from the conventional TAT with the modified barrier is shown in Fig. 4.3 (a), where the effective mass of electron in metal and oxide are taken as 0.1 m_0 and 0.3 m_0 respectively [147], [148], [149], $\varphi_t$is taken as ~2.15 eV and φ_x is obtained from expression 4.5. The observation from Fig. 4.3(a) and (b) are; The RESET process starts at 1.9 V shows a drip of current to 0.4 µA due to rupture of CF. Beyond RESET voltage (≥2V), the CF no longer exists, consequently, the electrons which overcome the triangular potential barrier contribute to the leakage current which is transpired by the tunneling of electrons through the traps at OCF. This leakage current rises and reaches ~ 0.8 µA at a forward bias voltage (FBV) of 3 V. Next, the simulation results of two step generalized trap assisted tunneling (GTAT) process is given. Leakage current due to GTAT is obtained by taking the sum of currents contributed by electrons that crossed triangular as well as a trapezoidal barrier.

In GTAT, at low electric fields, current from trapezoidal barrier dominates, while at high potential, the effect of triangular barrier governs the total leakage current depicted in Fig. 4.3(a). Observing the current density variations with the electric field across OCF shows that the main component of leakage current at low electric fields is contributed by the electrons that cross the trapezoidal barrier. At an electric field of ~ 2V/nm, the current through the triangular barrier contributes more to the leakage current. The density of oxygen vacancies at OCF has a major role in determining the leakage current in the GTAT approach. The number of oxygen vacancy traps present at OCF changes with the diffusion of traps to OCF and is approximated as $0.1x10^{20}$ $m^{-3,}$ and the diffusion constant is taken as $2.6x10^{-3}nm^2s^{-1}$. Trap level of Ta_2O_5 is taken as ~ 2.3 eV [145]. Fig. 4.3(b) shows the I-V characteristic curve of the GTAT model of the device on a logarithmic scale.

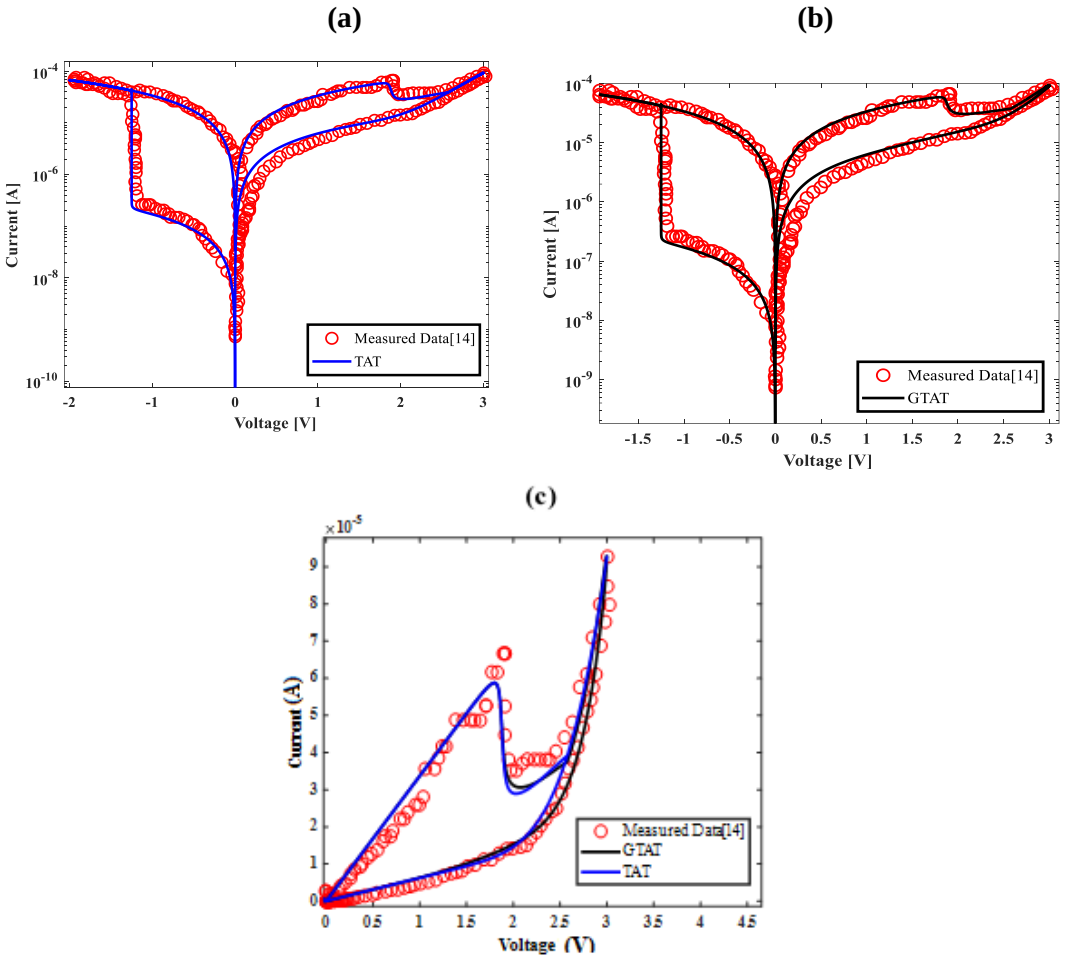


Fig. 4.3 (a) Simulated I-V characteristics of TAT model in logarithmic scale (b) Simulated I-V characteristics of proposed GTAT model in logarithmic scale (c) Simulation results of TAT and GTAT in linear scale

Simulation results of both tunneling approaches show a good fit for the experimental data; nevertheless, GTAT provides a better fit than TAT. In logarithmic curves, the difference between both approaches is not clearly visible; hence the simulation results plotted in linear scale is depicted in Fig. 4.3(c), where the slope of current obtained for GTAT has a good correlation with measured data whereas, in TAT, the slope of the curve does not follow the slope of experimental data at certain points. At FBV of 2 V to 3 V, the rising and falling current in conventional TAT follows the same path. In GTAT, the rising and falling current values showed a slight deviation in the current level due to diffusion of oxygen vacancies. On compared to TAT, GTAT is a comprehensive model which considers deposition conditions and other significant parameters such as the number of vacancy traps/carriers contributing to the current which is useful in the current work as the number of oxygen vacancy traps at outside of the filament is considered as a variable parameter that changes with the magnitude

of applied voltage and the carrier diffusion occurring within the device due to concentration gradient.

Next, an analytical model is developed to understand the variability present during multiple cycles (cycle to cycle variability) of Pt/Ta_2O_5/TaO_x/Pt device characteristics. The following section discusses the variability model.

2.13 Variability model for Ta_2O_5/TaO_x RRAM

Even though the Pt/Ta_2O_5/TaO_x/Pt device is a better memory candidate, like other memories, these memories are also vulnerable to variability [86], [151]. Variability can be defined as an undesired process that causes inconsistency in the device characteristics due to intrinsic and external perturbations. If variations occur in I-V curves of individual cells over many input cycles, it is known as cycle-to-cycle variability (c2c). The variability shown by the tantalum bilayer (Ta_2O_5/TaO_x) devices is reported in [152], where variations are noticeable during SET/RESET switching voltages and at high resistance state (HRS). It is noticed that the characteristics show uniformity in its LRS. However, the reasons for c2c variability is unknown; therefore, this section focus on the reasons behind variability in I-V characteristics and presents an analytical model demonstrating the c2c variations in the I-V curve of Ta_2O_5/TaO_x device by considering parameters influencing the device behavior, such as multifilament formation, modulations in the radius of conduction filaments (CF), barrier height and number of oxygen vacancies (Nv0) at the interface between the top electrode (TE) and active switching layer (Ta_2O_5).

4.1.4. Impact of multiple filament formation on the device characteristics

In the proposed variability model, Oxygen vacancies are the switching elements that form random percolating paths (CF). While sweeping the input, the dimension, including the length and area of CF, changes and reflects the I-V curves. As these filaments grow, they provide additional low resistance paths to change actual current flow from one filament to another. Only one filament is assumed to be stable in the present scenario, and all others are unstable. Only one filament, among others, ultimately grows to connect the TE and BE, while the remaining unstable sub-filaments define the current path before forming a completely developed filament. Fig. 4.4 (a) depicts the multifilament concept, where F1, F2, F3, and F4 are arbitrary filaments, in which F4 is considered a stable filament that can grow up to 4 nm. At threshold voltage (0.8 V), F1 emerges and grows towards the TE up to 3.4 nm as shown in Fig. 4.4(a); thus, it directs the device current.

Further increase in voltage brings F2 to grow up to 3.6 nm which offers a new low resistance path; therefore, the current flows through F2. After that, F3 with a length of 3.8 nm emerges, whereby the current takes a new path. Finally, a complete filament F4 (4 nm) connects TE and BE; thus current ultimately follow that least resistance path and offers the maximum possible current (I_{max}) that can flow through the device.

The above concept is demonstrated with the simulated result given in Fig. 4.4(b) where the inset shows the zoomed view of the current path shown with a grey circle.

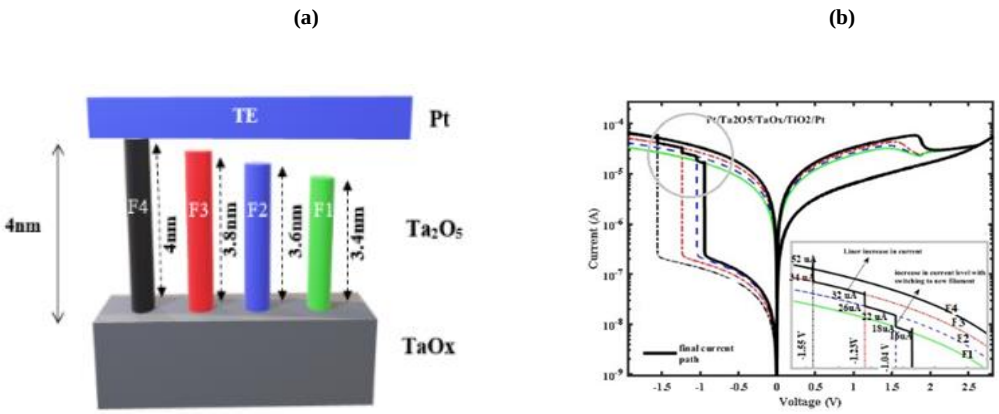


Fig. 4.4 (a)Formation of multiple filaments(b)Simulated I-v showing variability due to sub filamentary network(inset: zoomed view of the circled part

Fig. 4.4 (b) shows that an upsurge in current occurs only when forming a new filament. Otherwise, the current linearly increases through the existing filament. Initially, the filament formation starts at a threshold of~- 0.8 V, where the first filament forms and the current flows through F1 (represented with dashed green line), which linearly increases from 16 µA to 18 µA. As the filament F2 (blue) emerges at ~1V, the current switches to 22 µA, and the current then linearly increase from 22 µA to 26 µA (-1V to -1.23 V). Then, an uprise in current from 26 µA to 32 µA occurs due to the formation of F3 (red). The increase in voltage caused a linear increase in the current until F4 (red color) emerges to provide a low resistance path. When F4 emerges, an upsurge in current from 32 µA to 52 µA occurs at -1.5 V, and finally, the maximum current (Imax) passes through F4. The actual/equivalent current path obtained during one cycle is shown with a thick black line connecting all least resistance paths. The simulation result also matches with the current paths as given in [151].

4.1.5. Impact of filament radius on I-V curves

In each input cycle, the switching process in RRAM is governed by newly formed CF(s). Therefore, variability occurs with randomness in radius due to change in the number of

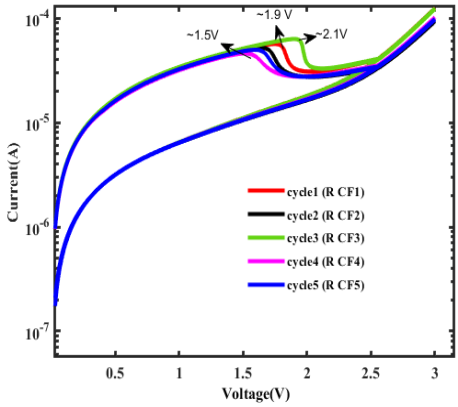


Fig. 4.5 simulated I-V showing variation in RESET voltage with different radius

oxygen vacancies (N_{v0},) in new filament, which in turn causes conductivity variations. Hence, the filaments' conductivity is modeled with the filament and N_{v0}, where N_{v0} is varying with applied voltage. It is modeled with the error function of voltage. The random variables are included in the model to assimilate the variability concept, where the random changes are added with filament diameter [153], [154]. In addition to this, the filament shape is also considered to contribute to the variability. Hence in the proposed model, filaments are assumed to have a conical shape with a maximum area limited to 0.5 nm^2. Thus, the change in conductivity of the CF itself changes the ON resistance. Hence this change directly affects the current conduction. However, the change in the radius of the filament shows reflections on the RESET switching voltage. Larger the radius of the filament more will be the required voltage to rupture (RESET) the filament, which is shown in Fig. 4.5 by demonstrating with five input cycles, where CF1 is the conduction filament formed during cycle 1, CF2 is formed during cycle two and so on. Then, it is inferred that the filament radius is in the following order $R_{CF3}>R_{CF1}>R_{CF2}>R_{CF5}>R_{CF4,}$ where R_{CFn} represents the radius of the CF formed at n^{th} cycle, therefore RESET voltage becomes V_{RESET3}(~2.1V) > V_{RESET1}(1.9V)> V_{RESET2}(~1.8)> V_{RESET5}(~1.7) >V_{RESET4}(1.5V) where the filament with the largest radius (CF3) rupture only at ~2.1 V.

4.1.6. Impact of variations in tunneling barrier height on I-V curves

In addition to the randomness in the length and width, constituent oxygen vacancies within the conduction filaments and the number of trapped oxygen vacancies at the interface

of TE also result in variations in device characteristics. Generally, the oxygen vacancy traps create at the bulk and metal-semiconductor interfaces. These positional difference of oxygen vacancies affects the conductance characteristics by forming different energy levels within the forbidden band. In this study, even though the effect of oxygen vacancy traps formed at the bulk is not directly considered, the dimensional parameters such as length and width of CF are indirectly affected by the N_{v0} traps created within the bulk oxide. In the proposed model, the thickness of Ta_2O_5 is limited to a few nanometers, which facilitate electron tunneling with its magnitude proportional to the probability factor [155], which in turn is dependent on tunneling barrier height and thickness of oxide (D).

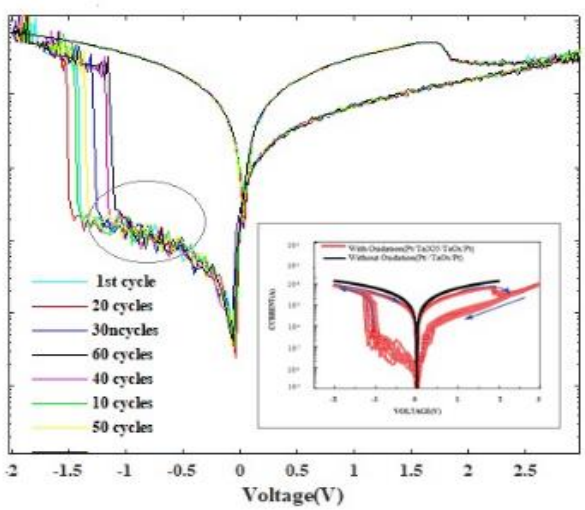


Fig. 4.6 variability model obtained due to variation in tunnel barrier modulation(inset shows variability reported in actual device

From the proposed model, it has been observed that even the trivial changes in the barrier height significantly affect the conduction process, and it reflects on the variations in HRS current levels (circled in Fig. 4.6) and SET switching voltages. The variation in N_{v0} at the interface is modelled with the image force lowering factor, affecting the Schottky barrier height. In the case of multiple filament formation, each filament-metal interface has a different N_{v0} to differentiate the barrier lowering. Hence, the model shows congruence with the experiment result depicted in the inset of Fig. 4.6. The following section discusses the SPICE model of $Pt/Ta_2O_5/TaO_x/Pt$ device used in circuits to analyze the electrical behavior.

2.14 SPICE Model Implementation of $Pt/Ta_2O_5/TaO_x/Pt$ device

Two terminal SPICE circuit models with TAT and GTAT are realized at the circuit level by implementing additional voltage-dependent current sources in the existing two-

terminal circuit model of the device [84], [155]. In the existing device model, the current conduction is modeled with Schottky barrier tunneling. In contrast, the state dynamics of resistive switching is modeled with the existence of oxygen vacancies present at the conduction filament as depicted in Fig. 4.7, where the capacitor Cw and resistor R take values as given in [84]. Gon and Goff are the current sources representing the ionic current (I_w) during reverse and forward bias, respectively. Finally, the integration of I_w provides the state evolution of the RRAM model. The details of the realization of the current path subcircuit using TAT and GTAT models are explained in the following sub-sections.

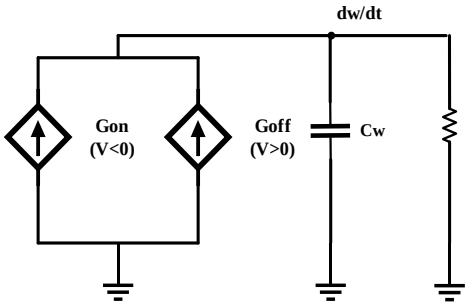


Fig. 4.7 . Subcircuit implementing the evolution of state dynamics of Pt/ Ta_2O_5/TaO_x /Pt taken from [84]

4.1.7. Realization of TAT

In the proposed model, the increase in current conduction at the RESET phase of $Pt/Ta_2O_5/TaO_x/Pt$ device is attained by incorporating TAT, which is realized in the circuit model by integrating an additional voltage-dependent current-source in the port equation given in [84].

In Fig. 4.8, a single current source associated with TAT (GTri) has been connected parallel to the current sources representing Schottky conduction during forward (GItunOFF) and reverse bias (GItunON), respectively. In addition to the current source, two voltage sources are also implemented to indicate the triangular barrier's contribution at high electric fields [45]. These voltage-dependent voltage sources are Etri and Eu1, which are added to the existing SPICE model port equation to obtain the RESET characteristics controlled by the voltage drop across the switching layer (VD).

4.1.8. Realization of GTAT with variable Oxygen vacancies

In the proposed model, GTAT conduction is defined with voltage-controlled current sources (VCCS) representing the tunneling of electrons across the Ta_2O_5 layer at OCF in addition to the Schottky barrier tunneling currents through the CF denoted by GItunON and GItunOFF. The circuit diagram in Fig. 4.8(a) depicts that the current source GItunON delivers charge to the internal node (PVs) between the VCCSs and voltage source EVRS representing the contribution of Schottky barrier tunneling current through CF activated at an applied voltage of V<0, while another current source GItunOFF representing the activated current through CF for applied voltage V>0. In addition to this, a current source G_GTAT is included in the circuit to represent the current emerging due to trap assisted tunneling mechanism occurs at OCF region of Ta_2O_5 layer. The current source G_GTAT delivers charges to the internal node PVs that are evolved from the triangular (GTri) and trapezoidal barriers (GTra). Hence, these two current sources can be connected parallel to indicate the sum of electronic current overcome by the barriers activating at high and low electric fields. However, the inclusion of the GTAT current component does not influence the state equation deriving the ion dynamics; hence this current component is state-independent.

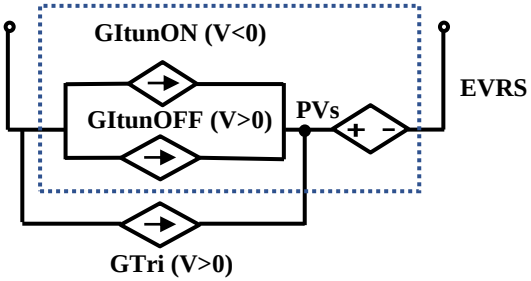
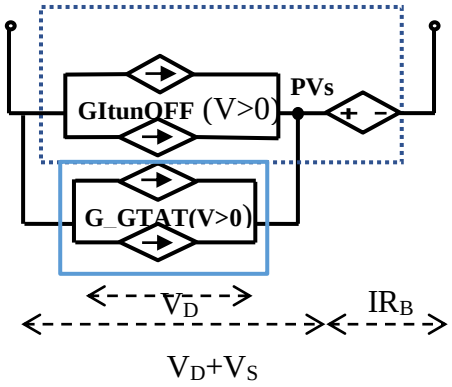


Fig. 4.8 LTSPICE implementation of the proposed SPICE model for TAT. The Two terminal (current path) SPICE implementation of the single Pt/Ta_2O_5/TaO_x/Pt device with three current components. Dotted lines show the port representation from the existing model [84] where PVs denote the internal node. GTri is the state-independent TAT current.

Lastly, in Fig. 4.9(a), the voltage-controlled voltage source (EVRS) is connected in series with the overall circuitry representing the total voltage drop on the bulk TaOx layer (IR_B) [84]. The remaining voltage drop across the VCCS represents the sum of the potential drop across the Schottky interface (Vs) as well as the bulk Ta_2O_5 layer (V_D). Here, Vs is the voltage drop across GItunON and GItunOFF, are the parallel current sources, and V_D is the voltage drop across the parallelly connected GTra and GTri current sources. Thus, the complete picture of the model is described as the total current through the device is the sum of Schottky barrier

tunneling and GTAT current components contributing charge to the node PVs connected in series with the EVRS, with both current sources and voltage sources controlled by voltage-dependent voltage sources (VCVS) present at the circuit.

(a)



(b)

E_{E1}=f (E_{VD}), **E_{DC}=f (E_T)** E_{Nt}=f(E_{DC},time) Ejtri=f (E_1, E_{Nt}) Etra=f (E_1, E_{Nt})

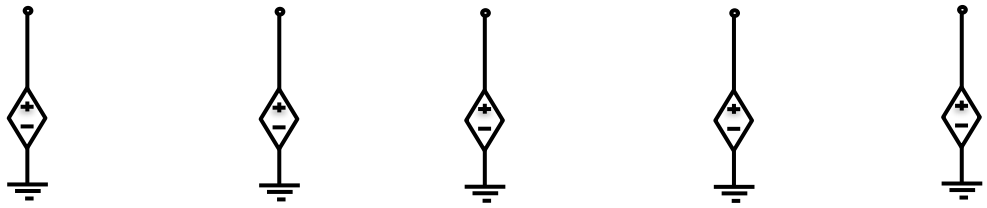


Fig. 4.9 LTSPICE implementation of the proposed SPICE model. (a) The two-terminal (current path) SPICE implementation of the single Pt/Ta_2O_5/TaO_x/Pt device with Schottky tunneling and GTAT current sources and voltage source EVRs. The sub-circuit shown with dotted box (blue) is taken from [84] (b) Represents the voltage-dependent voltage sources controlling the current sources.

The voltage sources used to derive the voltage-controlled current sources GItunON and GItunOFF are presented in [84]. Likewise, several voltage sources are used in the proposed RRAM model to realize G_GTAT current source (as given in figure) such as; the sources to implement Fick's law of diffusion and field controlled tunneling current such as E_{E1}(E_{VD}), E_{DC}(E_T), E_{Nt} (E_{DC}, time), Etri (E_1, E_{Nt}), Etra (E_1, E_{Nt}) (Fig. 4.9(b)). E1 is the electric field across the switching layer as a function of voltage drop (VD) across the Ta_2O_5 layer. Etri and Etra are the voltage sources controlled by the electric field and the concentration of oxygen vacancies (E_{Nt}). The oxygen vacancy concentration is a function of diffusion constant (E_{DC}) and varying temperature (E_T).

The voltage-controlled voltage sources E_{DC} and E_{Nt} are implemented to represent the diffusion of oxygen vacancies across the device and the stepping parameter 'time' is utilized in the SPICE model to indicate the diffusion of oxygen vacancies overtime where the '.Step' function triggers the analysis of diffusion process which repeatedly performed while stepping the time parameter from 0 to 10 ms in steps of 5 µs.

4.1.9. Results and Discussions

The proposed device model is simulated with sinusoidal input of an amplitude 3V and frequency 100 Hz; then, the characteristics are analyzed for a transient of 0.01 seconds. The simulation results obtained from the transient analysis are illustrated in Fig. 4.10, it can be demonstrated as the increase in the current profile beyond 2 V is due to the reduction in entire resistance of the device owing to the additional current path outside of the filament, the results show that the model correlated with the experimental result. Likewise, the model with the TAT approach (Fig. 4.10(a)) also follows the experimental result [151] while tunneling current follows the same path for both increase and decrease in applied voltage beyond 2 V because of the assumption that the oxygen vacancies across the device is a constant. The maximum current attained for both TAT and GTAT at 3 V is ~80 µA, matching the experimental results [32]. Because of the improvisation and inclusion of the diffusion process in GTAT, its characteristics replicate the experimental result than that obtained from TAT.

For a closer analysis, the I-V characteristics obtained from GTAT are plotted in linear scale as in Fig. 4.10 (b), which shows that a change in the device's resistance occurs at 2 V-3 V, owing to the diffusion of oxygen vacancies outside of the filament area. An average of ~ 20 KOhm resistance change is noticed in the characteristics during the above voltage range. Further, the model is tested with triangular and rectangular pulses to study the response of the device model to various inputs. The following sections discuss the response of the proposed device model to both inputs.

Table 4.2 Parameters used in SPICE Model of Ta_2O_5/TaO_x RRAM

Symbol	Value	Unit	Description
φ_t	2.3*/2.35 # [145]	eV	Trap Energy
m_{ox}	$0.3m_0$ [148]	Kg	The effective mass of electron in metal oxide
m_{no}	0.1 m_0# [147]	Kg	The effective mass of electron in the metal
m_0	$9.1x10^{-31}$	Kg	Mass of free electron
A	$9x10^{-9}$	m^{-2}	Area
N_t	$1x10^{20}$#	m^{-3}	Trap density at CF
D_0	$2.8x10^{-3}$# [150]	nm^2s^{-1}	Maximal diffusion constant
D	4	nm	Metal Oxide thickness
Ea	1.3	eV	Activation Energy
E_0	0.2 [147]	eV	Total energy of an electron

*Denotes parameter value used for TAT and # denotes parameter values used for GTAT tunneling. Parameter value with no symbols applies to both mechanisms.

(a) (b)

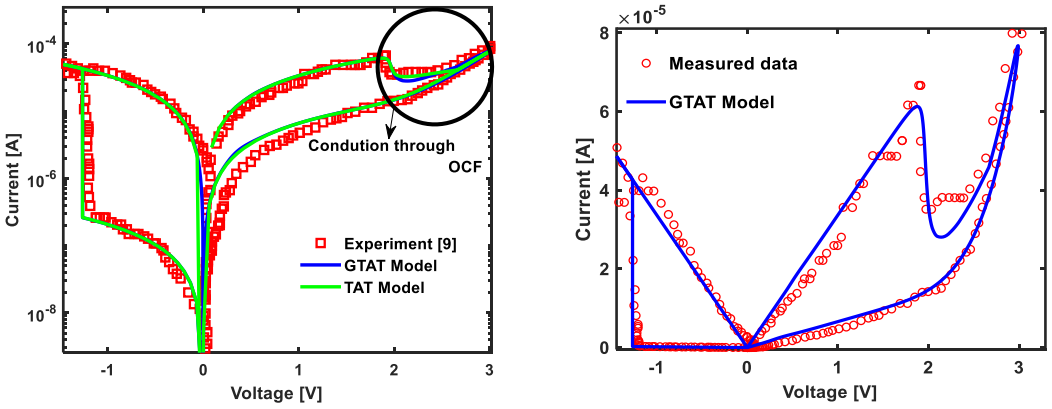


Fig. 4.10 (a)The characteristics obtained from the proposed model with TAT and GTAT approach; the region highlighted in a black circle denotes the increased current conduction beyond RESET due to the current conduction path through OCF. The plotted experiment value is taken from [32](b) The linear I-V characteristics obtained from the proposed model with GTAT approach with measured data.

4.1.10. The response of the model to triangular pulse and step input

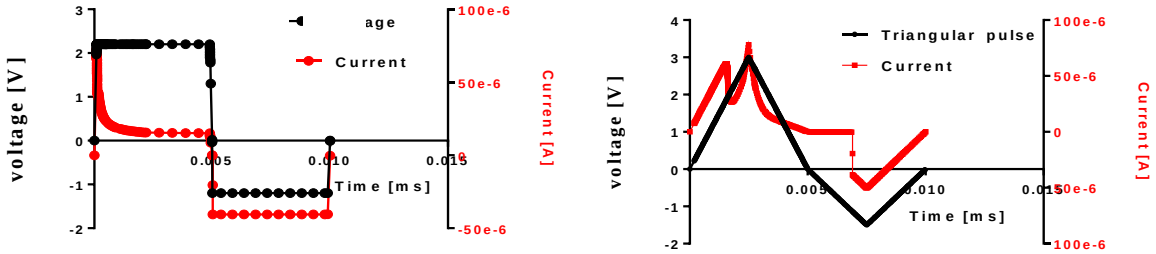


Fig. 4.11 (a) The model response to step input with 2V amplitude and 100Hz frequency (b) The model response to triangular input with 2V and -1.5V voltage swings and frequency of 100Hz.

To use RRAM devices in various applciations, it is necessary to test it with different conventional input signals such as square waves, sinewaves, and triangular pulses. Hence, this section discusses the response of the model to conventional inputs. Moreover, it has been reported that the use of triangular pulse in RRAM helps it to improve endurance by suppressing the current overshoot [156]. Response to step input is tested with an input pulse signal with 2 V amplitude, and 100Hz is, and its output shows ~80 µA current beyond the RESET voltage at 3 V as in Fig. 4.11(a). Similarly, the response of the model to the triangular input is tested with a pulse of 3 V and -1.5 V input swings, 100Hz frequency corresponding result is plotted in Fig. 4.11(b) shows that the current at RESET phase of the device increases up to a level of ~80 µA.

In conclusion, an analytical and electrical model of Pt/Ta_2O_5/TaOx/Pt is developed by implementing an additional state-independent current conduction mechanism of trap-assisted tunneling (TAT) that occurs at the outside of the conduction filament at high positive voltages. In this mechanism, the leakage current is contributed by the traps or the oxygen vacancies present outside the filament (OCF). These traps present at shallow energy levels introduce additional energy states at the bandgap to enhance the leakage current. The model is implemented with TAT and GTAT, where GTAT provides reliable results as the model considers the variable oxygen concentration present at OCF. The simulation results of the analytical and electrical model of the Ta_2O_5/TaOx RRAM exhibit ~80 µA current beyond the RESET voltage.

Chapter 5

Selector model: Analytical and Electrical modeling of $Pt/Ta_2O_5/TaO_x/TiO_2/Pt$ selector device

Chapter Summary

The chapter consists of analytical and electrical modeling details of Pt/Ta_2O_5 /TaO_x /TiO_2 / Pt selector device. The first part of the chapter discusses the implementation details of the Physics-based analytical model of the selector, which is developed with the concept of tunneling such as Fowler Northeim tunneling and direct tunneling. Besides, the simulated model has been validated with the experiment result. The model optimization is done by varying the dielectric layer thickness and modifying the material properties of the top electrode. Further, to use the model in electrical circuitry, an electrical model has also been realized using the voltage-controlled voltage and current sources, resulting in I-V characteristics that best match the experiment result. From the simulated curve, it has been noticed that below the threshold voltage (~0.7 V), the model shows a low leakage current (sneak current) attributing to the open switch, while at an input voltage >1.2 V, the model characteristics exponentially increase attributed to closed switch behavior. The key observations from the proposed selector model are; the model exhibits high selectivity of ~10^4 with a highly nonlinear current profile with a high current density of ~$10^7 A/cm^2$. Further, the reasons behind the asymmetric, nonlinear characteristics are also explained with the help of the energy band diagram.

Related Publications

1.Arya Lekshmi Jagath, T. Nandha Kumar, Haider A.F. Almurib, K.B. Jinesh "Analytical modeling of tantalum/titanium oxide-based multi-layer selector to eliminate sneak path current in RRAM arrays," IET Circuits, Devices & Systems, ISSN 1751-858X, doi: 10.1049/iet-cds.2019.0480

The major challenge with Resistive random-access memory (RRAM) technology is the presence of a sneak path current that arises while integrating the memory units in a crossbar array (CBA). This leakage current (or sneak path current) originates from the low resistive paths emerging through unselected memory cells in the array [114]. Various existing solutions to mitigate sneak path current are discussed in the previous chapter. Among them, associating a selector with RRAM is a potential solution for mitigating the sneak path current. Moreover, a selector can be associated with either a conductive bridge random-access memory (CBRAM) [136], [123], or an oxide- RRAM device to reduce the sneak path current whereby the combination inherits the features of both the selector and memory unit. The desirable features of a selector are scalability, high selectivity, high current density, low OFF-current, and compatibility with memory cells [157]. Also, it has been proven experimentally that selector device exhibits good compatibility with the RRAM devices [122] when the devices are connected in a one-selector-one-resistor (1S1R) configuration, as described in chapter 2. Apart from the experimental investigations [117], [121], [158], modeling of 1S1R is a timely requirement that enables to verify devices compatibility in a crossbar array (CBA) for reducing the sneak path current. However, to understand the 1S1R model functionality, a selector model is necessary. Among the available selectors, Ta_2O_5 /TaO_x /TiO_2 -based selector has exceptionally good selectivity ($\sim 10^4$) and high current density [122]; hence this chapter describes the analytical and electrical modeling of tri-layer Ta_2O_5 /TaO_x /TiO_2 selector device by considering the electric field-driven electron tunneling mechanisms co-exist in thin multi-layer devices. The following sections explain the analytical and electrical model of the Ta_2O_5 /TaO_x /TiO_2 selector device.

5.1 An analytical model of Pt/Ta_2O_5/TaO_x/TiO_2/Pt selector

The proposed analytical model of Ta_2O_5 /TaO_x /TiO_2 helps to understand the semiconductor physics behind the device's working, hereafter Pt/ Ta_2O_5 /TaO_x /TiO_2 /Pt selector device would be referred to as selector throughout this chapter. The selected multilayer stack consists of different dielectric layers [157], [159], [160] made of Ta_2O_5 and TiO_2, respectively, as shown in Fig. 5.1, where TaO_x is the middle layer that is considered as the suboxide phase of Ta_2O_5 material regarding the XPS depth profile [10]. Properties of this layer are slightly different from Ta_2O_5 and have a significant role in transferring electrons between the top and bottom electrodes (TE and BE).

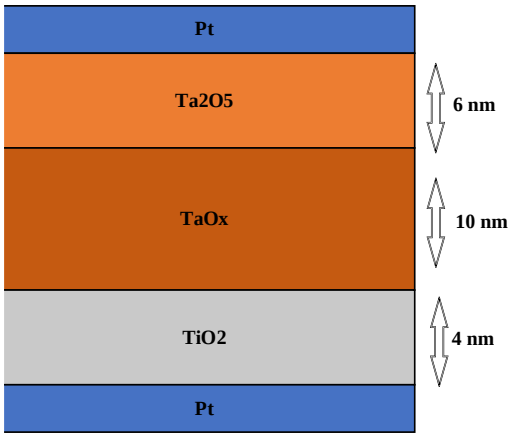


Fig. 5.1 Multilayer stack of selector device

When the input voltage is applied on the multi-layered device, the total electric field distributes across the resistive dielectric layers depending on their dielectric constants and layer thickness. The relation between electric field, dielectric constant and layer thickness is derived using Gausses' law as specified in equation 5.1 where, E_{Ta2O5} is the electric field across Ta_2O_5/TaO_x layer, D_{Ta2O5} is the thickness of the top insulator and D_{TiO2} is the thickness of the bottom insulator [162], $\varepsilon_{Ta2O5,}\varepsilon_{TiO2,}$ denotes the permittivity of the dielectric materials Ta_2O_5 and TiO_2 respectively. From the simulation, it has been noticed that most of the electric field appears across Ta_2O_5/TaO_x layer [163]. Further, the distribution of electric potential across the insulating layers is given by Kirchhoff's voltage law as given in equation 5.2, where $E_{TiO2}$is the electric field across the bottom oxide.

$$E_{Ta2O5} = V/(D_{Ta2O5/TaOx} + D_{TiO2}\left(\frac{\varepsilon_{Ta2O5}}{\varepsilon_{TiO_2}}\right)) \qquad 5.1$$

$$V = E_{Ta2O5}D_{Ta2O5} + E_{TiO2}D_{TiO2} \qquad 5.2$$

In the device structure, the thicknesses of dielectric layers are small enough for (in nanometers) the electrons to tunnel. Therefore, the current conduction in the device is modeled using the tunneling mechanism that occurs with respect to the applied electric field. Based on the potential barrier formation across the stack, the model employs two types of tunneling mechanisms: Fowler Nordheim (FN) tunneling and direct tunneling (DT) to capture the selector characteristics, where the asymmetry and non-linearity of the device characteristics are explained with various parameters such as electric field, electric potential, and effective tunneling distances (ΔD) obtained with energy band diagram of the multilayer stack. Here, ΔD is the effective tunneling distance, a virtual parameter that reflects the effect of the electric field

on the tunneling process. At equilibrium condition, the Fermi levels of the dielectric layer align to form a trapezoidal barrier with effective tunneling distance the same as the total thickness of insulating layers [20], resulting in negligible tunneling current.

Apparently, when a small positive voltage (<1V) is applied on the top electrode, the energy bands of the underlying layers tilts while maintaining the trapezoidal barriers, which results in electron flow from BE to TE. Thereby, the current flows in a direction from TE to BE, and this electronic current through the trapezoidal barrier can be modeled with direct tunneling current as given in equation 5.3, where $B1$, $B2$ are correction factors [166] represented in expressions 5.4, 5.5 respectively and A is the active area ~$6e^{-12}cm^2$. Thus, in the proposed model, direct tunneling of electrons through the bulk is limited by the total thickness of the device layers, which in turn provides high resistance at low biases to ensure the low off-current density of the selector.

$$IDT=A*\frac{q^3 m_{eff} E^2}{8\pi m_{diel} hq\varphi B1} e^{\frac{-4\sqrt{2m}\varphi_B^{\frac{3}{2}} B2}{3hqE}} \quad 5.3$$

$$B_1=\left(1-\left(1-\frac{qE_{diel}t_{diel}}{q\varphi_b}\right)^{1/2}\right)^2 \quad 5.4$$

$$B_2=\left(1-\left(1-\frac{qE_{diel}t_{diel}}{q\varphi_b}\right)^{3/2}\right) \quad 5.5$$

The presence of a high electric field at high amplitudes of positive and negative voltage causes bending of energy bands to form a triangular barrier, as shown in Fig. 5.2 (a) and (b), facilitating field-dependent FN tunneling of electrons across the metal-insulator barrier [167].

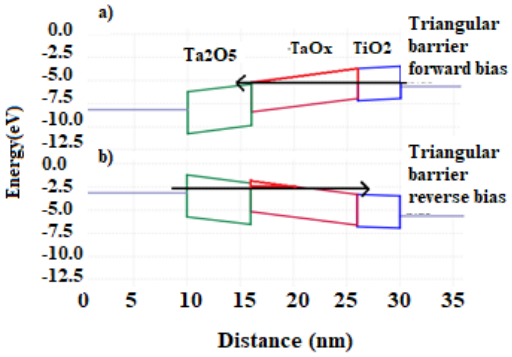


Fig. 5.2 The energy band corresponding to each layer is shown where x-axis shows distance from switching layer on the top in nm and Y-axis shows energy levels [168]. (a) Formation of the triangular barrier at forward bias (b) Formation of a triangular barrier at reverse bias

As given in Fig. 5.2 (a), the energy of electrons in the top Pt/Ta_2O_5 interface is higher at high voltages; hence the electrons flow from BE to the TE. However, due to the formation of a triangular barrier, the effective tunneling distance from the bottom electrode to the Ta2O5 layer significantly decreased. The tunneling current starts to rise exponentially. Likewise, the triangular barrier is shown in Fig. 5.2(b) demonstrates the effect of high negative input voltages on the energy band diagram. From the simulations, it is noticed that at -2.5V, the effective tunneling distance (ΔD) from bottom metal to top metal layer becomes ~16 nm to support the field-dependent tunneling of electrons (obtained from the energy band diagram).

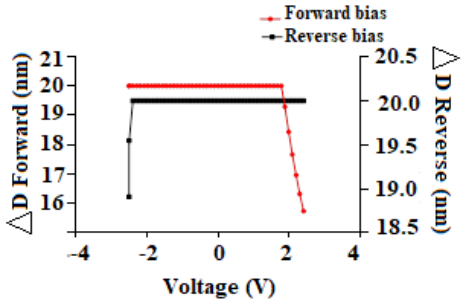


Fig. 5.3 Effective tunneling distance(ΔD) during forward (denoted with red line) and reverse bias (black line) due to the formation of triangular barrier [168].

Hence, at high voltages, FN tunneling (IFN) becomes the dominant conduction mechanism in which the exponential rise in current with high electric field introduces non-linearity in the device behavior. The expression for FN current is given in 5.6 [113]:

$$IFN = A^* \frac{q^3 m_{eff} E^2}{8\pi m_{diel} hq\varphi} e^{\frac{-4\sqrt{2m}\varphi^{3/2}}{3hqE}} \qquad 5.6$$

where m_{eff} is the effective mass of an electron, h is Planks constant, m_{diel} is the mass of electrons at the dielectric layer, E is the electric field across the insulator layer as given in 5.1 [162]. Table 5.1 shows the model parameter values used in equations 5.3, 5.4, 5.5, and 5.6.

Next, the effect of negative polarity of input voltage (reverse bias) on the model is studied. The conduction follows a similar pattern as that in the low voltage regime and can be modelled with direct tunneling (DT). Similarly, at higher amplitudes of negative input voltage, tunneling current conduct through the triangular barrier follows FN tunneling as in Fig. 5.2(b) and ΔD becomes ~19 nm at a potential of -2.5 V [163], [168]. Fig. 5.3 shows the effective tunneling distance with applied input voltage at both forward as well as reverse biases [163], [168]. When comparing the effective tunneling distance across the stack in both biases; ΔD reduced to ~16 nm in forward bias, while at reverse bias, it is ~19 nm as shown in Fig. 5.3.

This difference in the tunneling distance is inversely related to the magnitude of current at both biases. Therefore, the magnitude of FN tunneling current at positive bias becomes high compared to that of the current during reverse bias. This is due to the influence of ΔD [162] on tunneling current, which in turn reflects the difference in barrier height and the high electric fields. In the proposed model, the tunneling processes are field-driven and seldom depend on the variations in temperature [162].

Table 5.1 Parameters used in the analytical model of a selector device

Quantity		**FB**	**RB**
Tunnel barrier height(ϕ_0)		2.5eV	2eV
Effective mass of e^- in metal		$0.1m_0$	$0.1m_0$
Effective mass of e^- in dielectric		$0.5m_0$	$0.5m_0$
Active area of the device(cm^2)		$6e^{-12}$	
Dielectrics:	**Ta_2O_5**	**TiO_2**	**TaO_x**
Electron affinity(eV)	3.7	3.2	3.3
Dielectric constant	26	80	~25
Band gap(eV)	4.4	3.5	~4.0
Metals(M)	**Pt**	**W**	**Ni**
Work function(eV)	5.65	4.55	5.15
Barrier height(eV)	2.5	1.32	1.5

5.1.1. Simulated I-V Characteristics of the Proposed Analytic selector device model

Semilogarithmic I-V characteristics of the proposed selector model is plotted in Fig. 5.4 along with the experimental results [121]. As reported in published data [121], the model also shows better non-linearity with a high current density of ~10^7A/cm^2, high selectivity of ~10^4, and a low magnitude of OFF-current (46 nA). High selectivity(n on-linearity) is the desired parameter that makes the selector model to ensemble with the adopted RRAM model. At low voltages below the threshold voltage (~±0.7V), the model shows high resistance and this feature helps to reduce the sneak path current while using it in crossbar array, whereas beyond the threshold voltage, the model exhibits low resistance so that RRAM can perform read/write function. Even though Fig. 5.4. seems to be symmetrical, the device shows asymmetry in its I-V characteristics beyond 0.7V at both polarities as shown in Fig. 5.5(a), where the magnitude of current at +1V and -1V is $1e^{-5}$ A and $1e^{-7}$ A respectively. This

asymmetry in the device characteristics with different polarities is originated from the asymmetrical structure of the dielectric layers. Alternatively, it has been demonstrated that the magnitude of current at negative bias is less compared to the positive bias and this difference in the current depends on the effective barrier ($\Delta\phi$) across the stack, which can be calculated as, $\Delta\phi = \phi_1 - \phi_2$, where ϕ_1 (2.65 eV) and ϕ_2(1.95 eV), are the barrier heights (obtained from simulation)as shown in Fig. 5.5(b), and the parameter $\Delta\phi$ is observed as~ 0.7 V, which indicates that the current becomes polarity dependent beyond a potential of $V > \Delta\phi$. In addition to this, in Fig. 5.4, the slope of the I-V characteristics changes at an input voltage of ~1 V, which can be explained as the switching of the current conduction mechanism from DT to FN tunneling owing to the effect of the electric field. Thus, it results in the high nonlinearity in device characteristics.

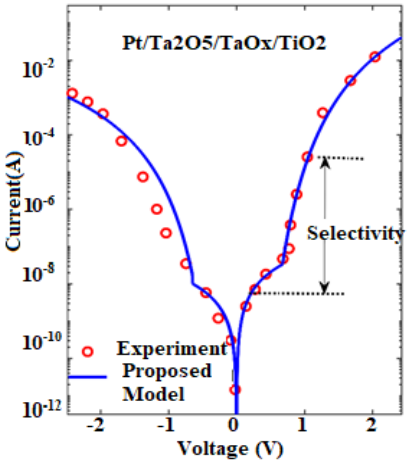


Fig. 5.4 I-V characteristics of the selector obtained from the proposed model and corresponding experimental result [121] marking the selectivity

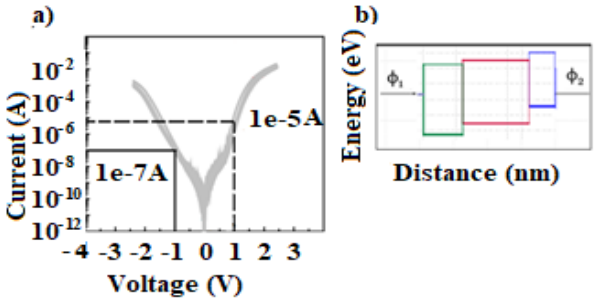


Fig. 5.5 Measured I-V characteristics [17] (a) Figure showing the asymmetry [17] beyond $\Delta\phi/e$, the dotted lines represent the forward bias current at 1V and solid lines indicate the reverse bias current at -1V (b) Asymmetry in barrier heights resulting in asymmetric I-V

5.1.2. Optimization of selector stack with tunnel layer thickness and material properties

A study has been conducted to optimize the selector stack by considering variable tunneling layer thickness and material properties. Fig. 5.6(a) is shown to demonstrate the drastic reduction in tunneling current with an increase in the thickness of the tunneling layer. For instance, the tunneling current decreased from ~15 mA to ~4 mA for a thickness variation from 2 nm to 5 nm of the dielectric layer (TiO_2).

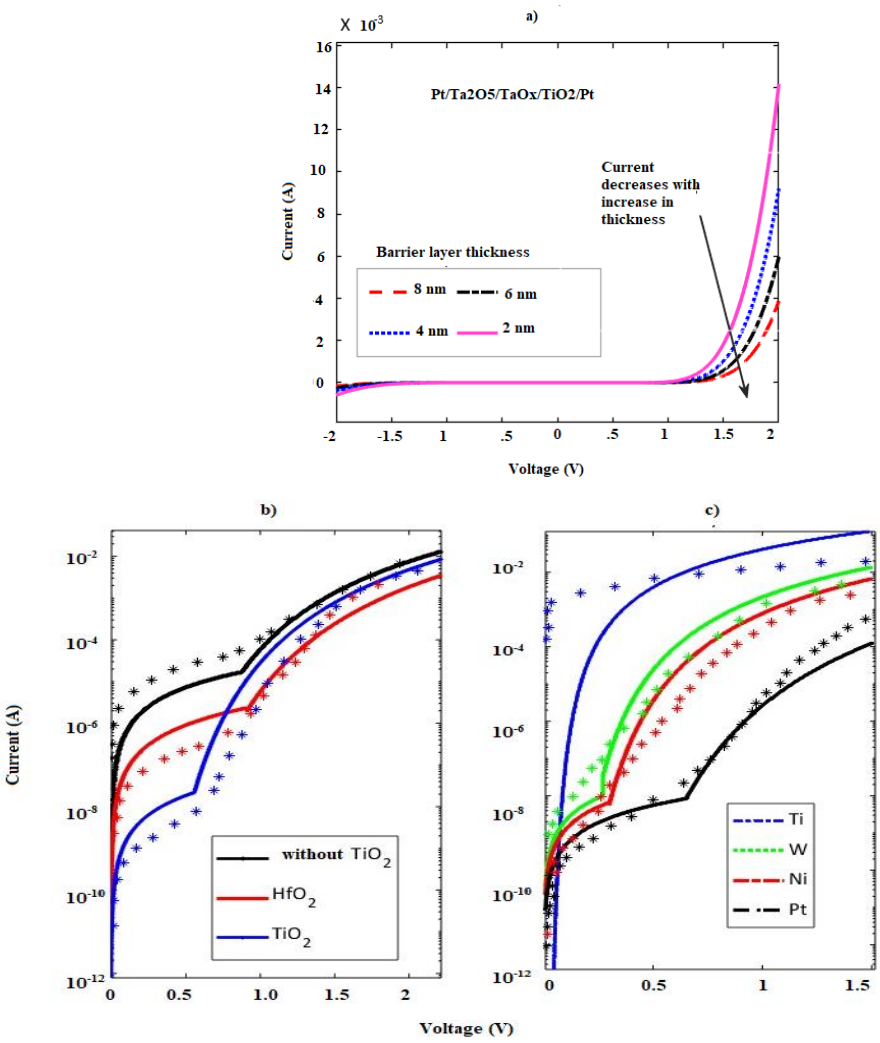


Fig. 5.6 Demonstration of various parameters to obtain the optimal selector stack (a) Current through the device with varying barrier layer thickness, arrow denotes the decrease in tunneling current with increase in tunneling layer thickness, plotted in linear scale, (b) Tunneling current obtained with different dielectric materials and absence of TiO_2 layer, (c) Dependence of electrode material on tunneling current. In (b) and (c), the scale is semilogarithmic with symbols that represents the experiment result [121], and solid lines represent the simulated results (semi-logarithmic)

Here, the analysis of thickness variation of the tunneling layer is useful in optimizing the magnitude of selector current for the desired application. Further, the influence of various dielectric materials on the selector stack is demonstrated in Fig. 5.6(b). It is found that the material properties such as the effective mass as well as the dielectric constant affect the magnitude of leakage current at a low voltage regime.

In the simulation, the effective mass of electrons in HfO_2, TiO_2, and Ta_2O_5 are taken as $0.1m_0$, $0.5m_{0,}$ and $0.5m_{0,}$ respectively, where m_0 is the mass of a free electron remaining parameters used for the simulation are shown in Table 5.1. Referred to Fig. 5.6(b), the estimate of leakage current through HfO_2 at the low voltage range is found to be higher than the leakage current obtained with $TiO_{2.}$ Therefore, TiO_2 is a better candidate to use in selector devices as it offers high resistance. Further, the effect of removing the thin insulating layer is also considered in the study. As anticipated, Fig. 5.6(b) shows that the absence of the layer significantly improves the magnitude of current, which is visible during low bias voltages. Fig. 5.6(c) demonstrates the variation in tunneling current with different top electrodes such as Ti, W, Ni, and Pt. From the results, it is inferred that the top electrode metal with high work function and high barrier height such as Platinum and Nickel provides the least leakage current, therefore these materials are effective to use as top electrode to reduce the sneak path current. For this simulation, the effective mass of electrons in metals is taken as $0.1m_0$ and the mass of electrons in dielectric m_{diel} as $0.5m_{0,}$ respectively.

5.2 Proposed Electrical Model of multilayer selector device

An electrical model has been proposed to study the electrical characteristics of a non-linear multilayer $Ta_2O_5/TaO_x/TiO_2$ selector stack. As explained in the previous section, tunneling of electrons through the device depends on the formation of barriers across the insulating layers due to the applied electric field. As mentioned in the analytical model, at high electric fields, tunneling occurs across the triangular barrier. It can be modelled with Fowler Nordheim tunneling [113]. In contrast, the current conduction occurs across a trapezoidal barrier at low electric fields and follows direct tunneling or hopping across the bulk, showing the exponential relation with the tunneling distance [151]. However, the hopping mechanism is adopted in the electrical model as it fits well with the proposed selector. Subsequently, these current conduction mechanisms are mapped to their equivalent current and voltage sources in the electrical model. The current components in the proposed electrical model are represented with parallelly connected dependent sources; those, in turn, depend on their corresponding

voltage sources; therefore, the current sources are considered as voltage-dependent sources. Since the current through the device is controlled by input voltage (electric field) developed across the layers, voltage-controlled voltage sources (VCVS) and voltage-controlled current sources (VCCS) available in the SPICE tool are utilized in the proposed electrical model.

In the simulation environment, E-type voltage sources and G-type current sources available in the SPICE library are utilized to implement dependent voltage sources and current sources, respectively. The transconductance of the current source is defined with the magnitude of the current obtained from the tunneling/hopping models. Fig. 5.7 (a) shows the equivalent circuit model of the selector with two dependent current sources representing different current conduction mechanisms, and Fig. 5.7(b) shows corresponding voltage-controlled voltage sources (VCVC). For simplicity, the current sources representing the forward and reverse bias are not shown separately.

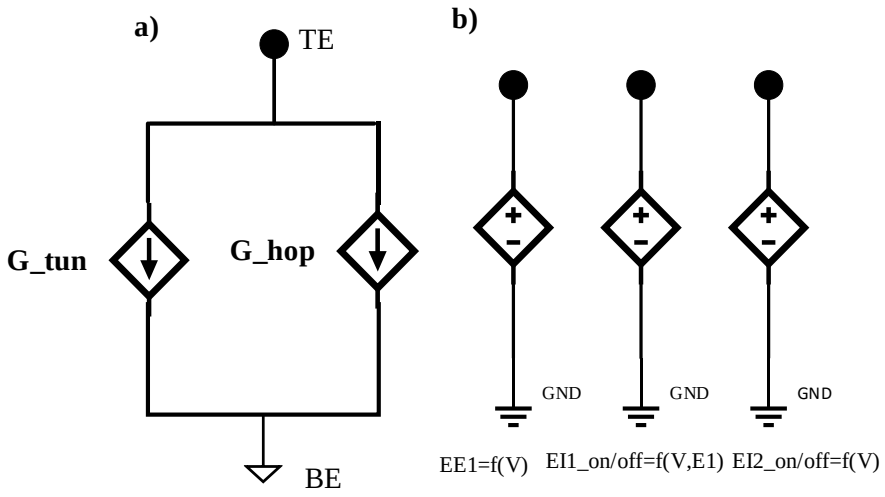


Fig. 5.7 Electrical model of selector (a) Voltage controlled current sources

(b) Voltage controlled voltage sources

The current sources representing the tunneling and hopping conduction mechanisms are connected across the top and bottom electrodes marked with G_tun and G_hop, respectively. As a result, these current sources provide the sum of current to describe the total current, and the magnitude of the current provided by the current sources varies with corresponding dependent voltage sources. The voltage-controlled voltage sources shown in Fig. 5.7(b) are the voltage sources to derive the current components such as EE1, EI1_on/off, and EI2_on/off in the SPICE model, where EE1 is the voltage source that depends on the

electric field across the device, which is a function of applied input voltage V(V), EI1_on/off represents the voltage source that depends on the electric field across the device and EI2_on/off is the voltage source governing the hopping conduction that in turn depends on the input voltage source.

A pseudo-code has been developed for the circuit model, which is shown in Fig. 5.8, and the code is based on the current port equations given in 5.6 and 5.7, in which dependent source functions are defined for the derivation of current components.

```
******* Parameters

.SUBCKT sel plus minus PARAMS:
+k1=1.54e-7 k2=4.31e8  Io=3.9n Io'=2.5n
+c1=2.1 c2=9e-2 v0=0.2 A=1e-9 d0=0.3e-9
+D2=10e-9 ε_Ta2O5=80 ε_TiO2=26 D1=6e-9 D3=4e-9
*******Current Path SPICE Subcircuit
EV V 0 value={V(plus)-V(minus)}
EE1 E1 0 value={V(V)/(D1+D3*(ε_Ta2O5/ε_TiO2))}
EE2 E2 0 value={-V(V)/(D1+D3*(ε_Ta2O5/ε_TiO2))}
EI1_on I1_on 0 value={c1* ((   k1*V(E1)**2))
                    *exp(((-k2)/abs(V(E1))))*A}
EI1_off  I1_off 0 value={-c2*((  k1*V(E2)**2))
                    *exp(((-k2)/abs(V(E2))))*A}
EI2_on  I2_on 0 value={Io*exp(-(10n)/d0)
                    *sinh(V(V)/v0)}
EI2_off  I2_off 0 value={Io'*exp(-(10n)/d0)
                    *sinh(V(V)/v0)}
********Device current
G_tun plus minus value={(V(V) >= 0)  ? {V( I1_on)} : {V(I1_off)} }
G_hop plus minus value={(V(V) >= 0)  ? {V(I2_on)} : {V(I2_off )} }
```

Fig. 5.8 Pseudocode for the electrical model of a selector

$$I(d, V)=\mathrm{I0}*e^{\left(\frac{-d}{d0}\right)}\sinh\left(\frac{V}{V0}\right) \qquad 5.7$$

In 5.7, d_0, v_0 are also fitting parameters, and d, V are the thickness of the dielectric layer and voltage. In the pseudocode, c1 and c2 are the fitting parameters, D1, D2, D3 are the thicknesses of dielectric layers where k1= $\frac{q^3 m_{eff}}{8\pi m_{diel} hq\varphi}$ and k2=$\frac{-4\sqrt{2m}\varphi^{3/2}}{3hq}$

5.3 Results and Discussions

To simulate the sub circuit of the proposed electrical model, a sinusoidal input of amplitude 3 V, frequency 100 Hz is asserted and analyzed for a transient of 0.01 seconds; the resulting simulated characteristics are depicted in Fig. 5.9(a). showing congruence with the measured data as reported in [116]. From the simulated curve, it has been noticed that below the threshold voltage (~0.7 V), the model shows a low leakage current attributing to the open switch, while at an input voltage >1.2 V, the model characteristics exponentially increase attributed to a closed switch behavior. Moreover, the device current is asymmetric at both polarities, with ~0.01 A appearing at 3 V and 2 mA appearing at -3 V.

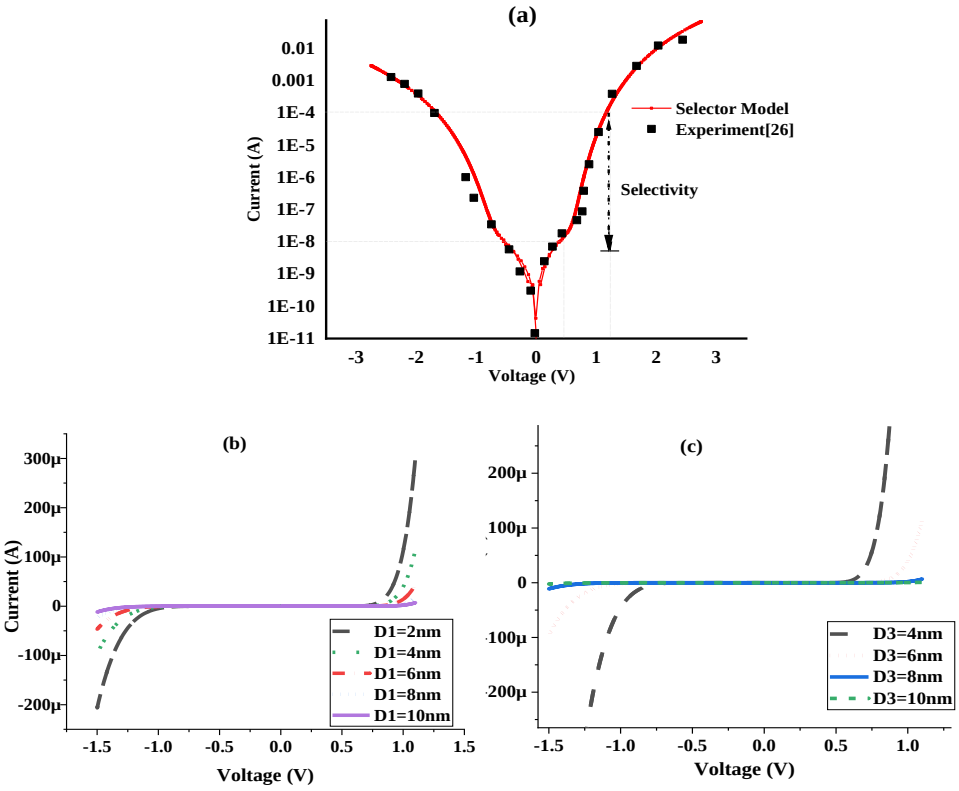


Fig. 5.9 (a) Semi logarithmic I-V characteristics of the selector device and proposed model where model is represented with red colour solid line and black symbols denotes the measured data [121] (b) Variations in current value with variations in thickness of Ta_2O_5 plotted in linear scale (c) Drastic change in the current level with variations in TiO_2 thickness

Further observations from the proposed selector model exhibit high selectivity of ~104 with a nonlinear variation of current at low (Vread/2), high voltages (Vread), and a high current density of ~10^7A/cm^2. Moreover, variations in current value for various thickness of tunneling

oxides are analyzed (given in Fig. 5.9(b)) and found that when the thickness of Ta_2O_5 increases, the current across the device decreases in a linear relation. In contrast, an increase in the thickness of TiO_2 shows a drastic reduction in current (as shown in Fig. 5.9 (c)), and it is observed that beyond 8 nm, the current variations are negligible.

To conclude, an analytical and electrical model of a tri layer selector is implemented with coexisting tunneling/hopping mechanisms such as direct tunneling/hopping and Fowler Nordheim tunneling. Direct tunneling dominates at a voltage level less than 0.7 V, and beyond that it follows Fowler Nordheim tunneling. The asymmetry in the device characteristics is reported to be due to the influence of electric field on tunneling distance (ΔD), which in turn directly reflects on the tunneling current. Also, it has been demonstrated that the magnitude of current at negative bias is less compared to the positive bias and this difference in the current depends on the effective barrier ($\Delta\phi$) across the stack. Moreover, the dependence of material properties and thickness of layers on device characteristics is demonstrated. It is found that the material properties such as the effective mass as well as the dielectric constant affect the magnitude of leakage current at a low voltage regime. Among other oxides, TiO_2 is a better candidate to use in selector devices as it offers high resistance at low voltage levels. Also, from the results, it is inferred that the top electrode metal with high work function and high barrier height (Platinum and Nickel) provides the least leakage current, hence they are better candidate to use as top electrodes.

Chapter 6

Integrated modeling of the proposed selector model with RRAM models (1S1R) and Complementary resistive switching (CRS)

Chapter Summary

This chapter discusses the integration of the selector model with various RRAM models to form 1S1R to eliminate the sneak path current in the crossbar array. An analytical model of 1S1R circuit is developed, and necessary parameters are derived from the closest models. Further, the electrical model of 1S1R is developed, and essential constraints required to create the crossbar array is predicted, such as read voltage, write voltage etc. Also, the response of the model to pulse input is studied. The effect of different pulse amplitudes, pulse width, and rise/fall delay time on switching characteristics are also analyzed. In addition, the 1S1R characteristics of Pt/Ta_2O_5/TaO_x/Pt, TiN/HfO_x/TiO_x/Pt, and Pt/TiO_2/TiO_{2-x}/Pt RRAM models with the proposed selector are studied. Furthermore, a CRS model is developed using the HP memristor model, and its state evolution is estimated. Finally, a comparison of various 1S1R models and CRS are reported.

Related Publications

1. A. L. Jagath and T. N. Kumar, "A comparative study on the performance of 1S1R and Complementary resistive switching models," 2020 IEEE International Conference on Semiconductor Electronics (ICSE), Kuala Lumpur, Malaysia, 2020, pp. 9-12, doi: 10.1109/ICSE49846.2020.9166874.
2. Effect of Sneak Path Current in TiOx/HfOx Based 1S1R RRAM Crossbar Memory Arrays, International Journal of Electronics and Communications (under review)

Integration of RRAM device with selector device (1S1R) is an experimentally proven solution for mitigating the sneak path current. However, the circuit level study of the integrated RRAM and selector model (1S1R) is required to understand the contribution of individual circuits as well as the compatibility of the circuits to use in the crossbar development. Although the authors of [169], [170] reported the simulation results of a hypothetical fitting model of Ta_2O_5 /TaO_x /TiO_2 selector device with V0 /Ta metal ion diffusion-based CBRAM model [170]. However, an integrated approach of modeling 1S1R comprising Pt/ Ta_2O_5 /TaO_x /TiO_2 /Pt selector model with Ta_2O_5/TaO_x RRAM, Pt/TiOx/Pt (HP Memristor), and TiN/TiOx/HfOx/Pt (Stanford-PKU model) are not yet established to demonstrate their compatibility to reduce the sneak path current. Therefore, the following section of the chapter discusses the analytical / electrical model of the 1S1R circuit and its contribution in reducing the sneak path current. Towards the end of the chapter, the implementation details of the HP memristor based complementary resistive switching model (CRS) are also given.

6.1 Analytical model 1S1R with Proposed Ta_2O_5 /TaO_x /TiO_2 selector model with Ta_2O_5 /TaO_x RRAM

A simplified analytical model of one selector- one resistor (1S1R) is developed by connecting the analytical model of the selector proposed in chapter 4 with an existing model of Ta_2O_5 /TaOx based RRAM device [155], [162] in series. As mentioned in the previous chapter (chapter 5), the Ta_2O_5 /TaO_x RRAM model [155], [171] is generated with two conduction mechanisms such as Schottky barrier conduction and trap assisted tunneling. The resistive switching mechanism of the model is demonstrated as the forming and replenishing of conduction filament (CF) due to the migration of oxygen vacancies with the applied input voltage, which is modeled with the Mott and Gurney rigid point-ion model [155],[46], [172]. Thus, the ion dynamics and electronic conduction modeling provided the exact I-V characteristics of the device.

When connecting proposed RRAM with selector model/circuits, by Kirchhoff's voltage law, the total potential applied across the set-up, is distributed between both circuits. Most of the applied voltage drops across the selector at low voltages, while the rest appears across the RRAM, though this voltage is low enough to switch the RRAM cell. But at high input voltages, the selector becomes more conductive so that most of the input voltage appears across RRAM to enables it to transit its states. While integrating both models, certain selector and RRAM model parameters are absorbed to 1S1R configuration, such as the Roff/Ron ratio, switching

voltages, non-linearity, and current levels. Since the models are connected in series, the overall current flow through the setup should be the same. At any instance, the prevailing current is limited by one of the device models (either selector or RRAM), i.e., one with the least electric field distribution controls the current through the series-connected models. Hence, the current in the analytical model is governed by the minimum current that flows through the serially connected devices for simplicity. Accordingly, a MATLAB simulator is developed based on this concept. In 1S1R configuration, total input voltage (V_{Total}) swings between -3 to 4V, and the voltage drop across RRAM is found to be -2 to 2 V, with the remaining voltage (V_{sel}) drops across the selector as given in (6.1).

$$V_{Total}=V_{sel}+V_{RRAM} \tag{6.1}$$

6.2 Results and Discussions

The I-V characteristics obtained from the proposed analytical models of a selector, RRAM, and 1S1R configuration are shown in Fig. 6.1, showing that Ta_2O_5/TaO_x RRAM is compatible with CBA with the proposed selector. Also, the 1S1R characteristics support well for the reduction of sneak path current; the parameter values derived from the proposed models are reported in Table 6.1. Moreover, a comparison of the proposed model with other 1S1R models are given in Table 6.2

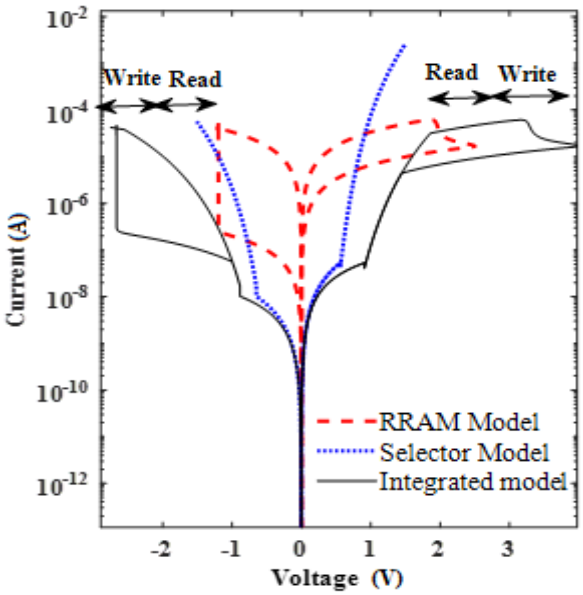


Fig. 6.1 I-V characteristics obtained from the proposed selector, RRAM model, and 1S1R plotted in semilogarithmic scale demonstrating the compatibility of the selector and RRAM.

From 1S1R I-V characteristics, it has been understood that the device current at low input voltage is limited by high resistance (~100 MΩ) of the selector, while at high voltages, the 1S1R characteristics follow RRAM current characteristics. Moreover, the read/write voltages of the integrated device can also be predicted from the obtained simulation results of the models. Table 6.1. shows various parameters derived from the proposed model, where SET and RESET voltages of RRAM are found to be -1.2 V and 2.0 V respectively, whereas SET and RESET voltages of the 1S1R model shows a shift in the x-axis, that is SET and RESET voltage are shifted to –2.8 V and 3.6 V respectively. The on-state and off-state current are measured for all three models demonstrate that the off-current of selector device, 1R model, and 1S1R model measured at 0.5 V are 46 nA, 3.5 µA, and 10 nA respectively. These results reveal that the low off-state current (10 nA) of 1S1R is inherited from the high resistance of the series-connected selector. Similarly, an analysis of on-state current is performed at 1.5 V shows that magnitude of on-current in the integrated model (46 µA) follows the characteristics of the RRAM model (50 µA). Next, the non-linearity (NL) factor of 1S1R at 2.8 V is calculated and it is approximately ~1000, whereas the RRAM model provides negligible non-linearity when measured at a read voltage of 1.4 V. Therefore, NL of 1S1R attained from the selector model (1600) makes it desirable to use in CBA to mitigate sneak path current. Next, the Roff/Ron ratio of 1S1R model is approximately ~50 while the RRAM model is at 170. However, the Roff/Ron ratio of 1S1R model is well above (~50) the desirable range for memory operations. In the table, the read-window is defined as the ratio of on current to off current at read voltage. In the given analysis, a better-read window is displayed by W/Ta(10nm)/TaOx/Pt device.

When implementing the presented 1S1R as a memory cell in a crossbar array, read voltage can be predicted to be in the range of 1.8 to 2.6 V during positive polarity or -1.7 to -2.3V during negative polarity. Meantime, the read bias asserted to unselected cells should be in the range of -1.0 V to 1.0 V. Similarly, the write voltage (Vwrite) can be in the range of –2.4 to -2.9 V to write logic ’1’ and 2.6V to 4V for writing logic ‘0’. While writing the data, the trails connected to unselected cells can be asserted with a potential of Vwrite/2.

Even though there are various 1S1R models [35] [173]available in the literature, many of them are implemented with threshold switching based selectors [35] [173][174]. To compare with the features of the proposed 1S1R configuration, a model with a similar selector and oxygen vacancy-based RRAM configuration is not available. However, a comparison of the proposed model with the results of the closest models [170], [35] is shown in Table 6.2. From

Table 6.1 Comparison of parameters derived from the various 1S1R models and proposed model

Models and parameters	[170] **model**	**[35] model**	**[170] model**	**1S1R (proposed model)**
Resistive switching element (RSE)	W/Ta(10nm)/TaO_x/Pt	TiN\HfO_2\Hf\TiN	TiN/Hf/HfO_2/TiN	Pt/ Ta_2O_5(4nm)/ TaO_x/Pt
Selector model	Exponential function-based conduction	Independent of conduction mechanism	Independent of conduction mechanism	Depends on current (DT& FNT)
SET Voltage (V)	2.75V	~+0.8V	~+1.5 V	-2.8V
RESET Voltage (V)	-2.6V	-2.47V	~-1.7 V	3.6V
ΔVread (range of read voltages)	0.65V	~0.35V	~0.5V	~ 0.8V
I at ½ V_{read}	~60nA	~100 µA	~1.2nA	~40nA
Read window (RW)	~80	~7	10	~65
Non-linearity (NL) at read ($V_{read/2}$, V_{read})	~1300	813	~6561	~1000
Non-linearity (NL) at SET ($V_{reset/set/2}$ & $V_{reset/set}$)	100	<10	~1	~1000

Table 6.2, the resistive switching element used to integrate with the selector in [35] and [45] is TiN/Hf/HfO_2/TiN, whereas the resistive switching element (RSE) in[170] and proposed model are W/Ta(10nm)/TaO_x(7nm)/Pt and Pt/Ta_2O_5(4nm)/TaO_x/Pt respectively. However, the switching mechanism of these two RSE is different such that oxygen vacancy (V_0) migration based switching is present in the proposed model and metal ion/V_0 based switching is found in [170]. Consequently, the SET and RESET switching voltages of both models are of opposite polarities, the presented models are independent of the conduction mechanism while in [170] the model is developed with a simple exponential fitting function. But the selector in the proposed model is developed with electric field-driven direct tunneling as well as FN tunneling conduction derived with different material properties.

Next, a comparison on read-window (RW) [35] is presented where RW exhibited by [170] is ~80, and the proposed 1S1R is ~65, which is also suitable for memory application to

distinguish the logic states clearly. The nonlinearity of the proposed model (~1000) is less than that of the models [170] and [173], but it is still with the recommended order of 10^3.

Table 6.2 Comparison of parameters derived from RRAM and proposed 1S1R model

Parameters	**1R**	**1S1R (proposed analytical model)**
Roff/Ron ratio	~150 (at 1.0 V)	~160 at -2 V
Nonlinearity ($V_{read/2}$, V_{read})	~2 (at 0.5&1 V)0	~1000 (at 1 & 2 V)
OFF-current(A) (at 0.5V)	3 µA	0.04 µA
ON-state current(A)	60 µA	60 µA
RESET Voltage	~2.0 V	>=4.4 V
SET Voltage	~-1.2 V	-2.7 to -3.6 V

Further, the OFF-current or leakage current during $V_{read/2}$ (~1 V) is measured, the proposed model shows an improvement (~40 nA) compared to [170] and [35], demonstrating the advantage of the proposed 1S1R to use in CBA to reduce the sneak path current. Similarly, the proposed model exhibits better non-linearity when measured at Vreset/set. Further, the available range of voltages used to perform the read process (ΔV_{read}) is calculated, which shows that the proposed model has better ΔV_{read} (0.8 V)compared to other models [35], [170], [173], [173]. Thus, the results reveal that the presented 1S1R model is a better candidate for CBA to reduce sneak path current, and the selector is versatile to use with CBRAM [171].

In Oxygen vacancy migration-based RRAM (Ox-RRAM) models, the analysis shows that the analytical model of the 1S1R circuit is beneficial to use in RRAM crossbar arrays to reduce sneak path current.

6.3 Circuit model of 1S1R with $Ta_2O_5/TaO_x/TiO_2$ selector and Ta_2O_5 /TaO_x RRAM

The Ta_2O_5 /TaO_x is RRAM and Ta_2O_5 /TaO_x/TiO_2 selector model are concatenated to obtain the 1S1R model as given in Fig. 6.2, with Pt as the electrodes. The complete circuit diagram representing the 1S1R configuration (Pt/ Ta_2O_5 /TaO_x /TiO_2 /Pt selector model with Ta_2O_5 /TaOx RRAM model) is shown in Fig. 6.3 where the first part of the circuit model represents the selector, and the second part represents the RRAM model. The selector model is developed with two current components representing the G_tun and G_hop voltage-controlled voltage source (VCCS). However, the magnitude of the current changes with the polarity due to asymmetry in the device structure, hence both forward as well as the reverse

bias current components are depicted in Fig. 6.3, that is G_tun _On and G_hop _On to represent the forward current and G_tun _Off and G_hop _Off represent reverse current.

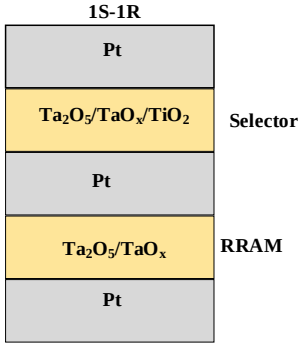


Fig. 6.2 Schematic representation of 1S1R consisting of RRAM and selector

In the second part of the combined circuit, three voltage-controlled current sources (VCCS) used to develop the current path sub-circuit of the memory are shown, where the first element GTAT is the VCCS that represents the electron tunneling current driven by the electric field across the dielectric layer at a positive bias of the input voltage [74], [78], [139] therefore, the forward component of GTAT is shown in Fig. 6.3. Similarly, the sources GItunON and GItunOFF in Fig. 6.3 represent Schottky barrier tunneling current through the conduction filament (CF) activated at an applied voltage of V<0 and V>0, respectively.

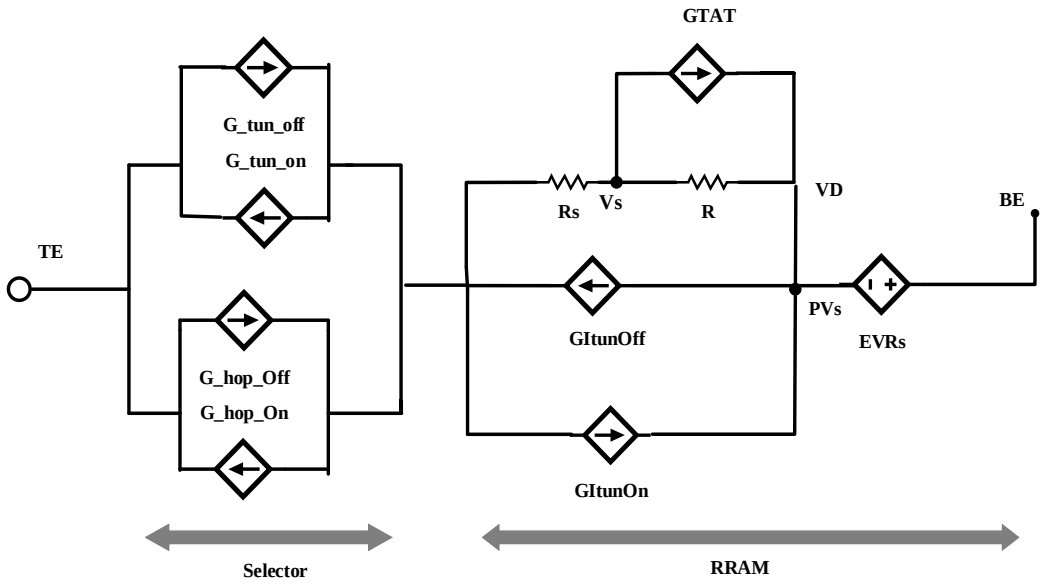


Fig. 6.3 Electrical model of 1S1R configuration marking all the associated current sources

These current sources deliver charge to the internal node (PVs) between the VCCSs and voltage source EVRs as shown in Fig. 6.3. The voltage-controlled voltage source (EVRs) is connected in series with the current sources represents the voltage drop at the bulk TaO_x layer (IRB) [84]. The remaining voltage (V-Vsel-IRB) drop across the VCCS, representing the sum of the potential drop across the Schottky interface (Vs) as well as the Ta_2O_5 layer (VD) that appears across the current sources GItunOFF and GItunON. Thus, the 1S1R model is described as; the total current through the device is the sum of Schottky barrier tunneling and TAT current contributing charge to the node PVs connected in series with EVRs with both current sources and voltage sources are controlled by the dependent voltage sources (VCVS).

6.4 Analysis and results

The proposed 1S1R circuit model is invoked with a Piecewise Linear (PWL) input sweep of amplitude 4.5 V and -2.7 V at a transient of 20 ms, results in the distribution of total voltage between the selector and RRAM memory. Let Vtot be the total voltage across the setup, Vsel is the drop across the selector and the remaining voltage appears across the RRAM cell. Based on Kirchoff's voltage law, the total input voltage applied is distributed across the selector and RRAM circuit models as given in Fig. 6.4(a) shows that from ~-1.0 V to 1.5 V, most of the applied voltage (Vtot) appears across the selector. Therefore, the voltage developed across the RRAM is negligible to change its current memory state; thereby, the leakage current can be eliminated to an extent. At Vtot >-0.85 V, the voltage across RRAM starts to build up due to the formation of conduction filament, when it reaches -1.3 V, the device switches to low resistance state (LRS); therefore, the voltage drops across it reduces abruptly back to -0.7 V as given in inset of Fig. 6.4(a). After that, further increase in voltage leads to an increase in potential across both models with more voltage drop at the selector. Fig. 6.4(b) has been shown to illustrate the comparison of the resistance across 1S, 1R, and 1S1R combinations. The circuit of the 1S1R model shows comparatively higher resistance than 1S and 1R for the entire cycle of testing owing to the effect of series resistance. However, during ON-state (LRS), the resistance of the combined circuit is in the same order as the resistance that appears in the RRAM model, whereas at low voltage regions, the total resistance of 1S1R becomes ~10 GΩ which is high enough to prevent sneak path current, inheriting the high resistance of selector. Fig. 6.4(c) shows the I-V characteristics plotted on a linear scale showing the proposed selector, RRAM response, and both models together. As expected, the simulated model of 1S1R has demonstrated the characteristics with memory window, but there is a variation in SET and RESET voltage of both RRAM and 1S1R are observed and are marked in the figure.

Similarly, the combination of the proposed selector model with the RRAM model [46] incorporating the current conduction beyond the RESET phase is also found compatible with the selector model as shown in Fig. 6.4(d).

The main interpretations from the combined characteristics are; at low voltages, the combined characteristics followed the selector behavior, and at high voltages it followed the RRAM switching behavior showing the voltage and current compatibility of the RRAM with the selector, the preferable range of read/write voltages required for both selected and unselected bit/word lines to avoid the excess of sneak path current can be predicted. Moreover, the optimum input voltage asserted to attain SET and RESET voltage in the 1S1R cell can also be predicted in advance. For instance, the input voltage required for SET switching in RRAM is ~-1.2 V whereas, in an integrated circuit, this parameter becomes ~2.7-3.6 V. Likewise, the voltage required for RRAM and 1S1R to drive in to RESET state is found to be ~1.9 V and ~4.5 V respectively. Even though the non-linearity of RRAM is ~2, the combined circuit acquired a non-linearity factor of ~45, which is inherited from the selector model.

Similarly, the off-current in 1S1R is as low as 0.04 µA to facilitate the reduction in sneak path current. From the analysis, the low OFF-current present in the selector is directly reflecting on the 1S1R setup. However, the Roff/Ron ratio of the combined circuit is ~160, which is inherited from RRAM, calculated at the read voltage of each circuit.

The on-current in both circuits reached a maximum of 60 µA. Moreover, the 1S1R circuit provides the least OFF-current of 0.04 µA which enables the circuit to reduce sneak current. The extracted parameters are listed in table 6.3 which compares the simulated curves of RRAM and 1S1R models. Next, the response of the integrated (1S1R) model to pulse input is tested and is given in, where (a) and 6.5(b) are showing the amplitude and width of the negative and positive input pulses applied, 6.5 (c) is showing corresponding hysteresis characteristics. When simulating with pulse input, the SET current increased up to 36 µA in response to the negative input pulse of amplitude -2.7 V, a pulse width of 180 µs with a fall delay time of 80 µs.

Similarly, to achieve RESET switching, a positive pulse with an amplitude of 4.5 V and a pulse width of 180 µs and a transition delay of 80 µs (T_rise) has been applied. The result showed the hysteresis curve with negligible OFF-current (10 nA) at an input of -1 V to 1 V and followed the RRAM current characteristics beyond an input voltage of ~-1.5 to -3.5 V and ~1.5 to 4.5 V. The necessary parameters obtained from the model are listed out in Table 6.3.

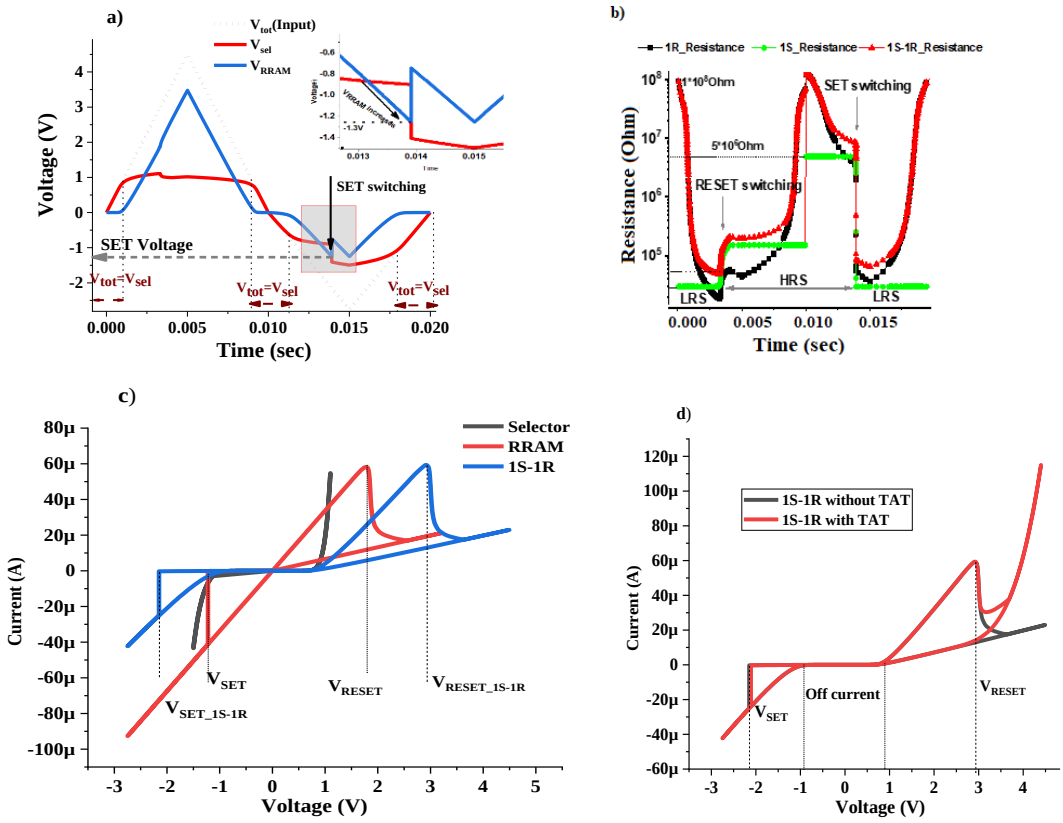


Fig. 6.4 Comparison of related parameters in 1S1R ,1S and 1R. (a) Voltage distribution across the 1S1R model (black dotted line), blue solid line showing the voltage developed across RRAM and red solid line represents the voltage drop across selector model. (b) Comparison of resistance offered by 1S1R combination (Red), 1S(black), 1R(green). (c) I-V characteristics obtained from the proposed 1S1R model(blue), RRAM model(red), proposed selector model(green) plotted on linear scale (d) Comparison of the I-V characteristics of 1S1R obtained with RRAM model presented in [84] without considering the current through OCF (black) and the model presented in [175], incorporating the current conduction beyond RESET phase by considering TAT current component (red line)

The read voltage required to supply for the selected RRAM device can be predicted from the above analysis. In general, the read voltage for 1S1R can be assigned in the range of |Vthr|< |Vsel_read|< |Vwrite/2|, where Vsel_read is the read voltage to be applied to the selected cell, Vthr is the threshold voltage measured from the selector, Vwrite/2 is half of the write voltage applied to the bit line of the selected RRAM cell. The read bias of unselected cells can be allotted below the threshold voltage of the selector so that the selector drives to a high resistance state and effectively blocks sneak path current from unselected cells whereas, beyond the threshold, the selector model enables the RRAM to function write or read.

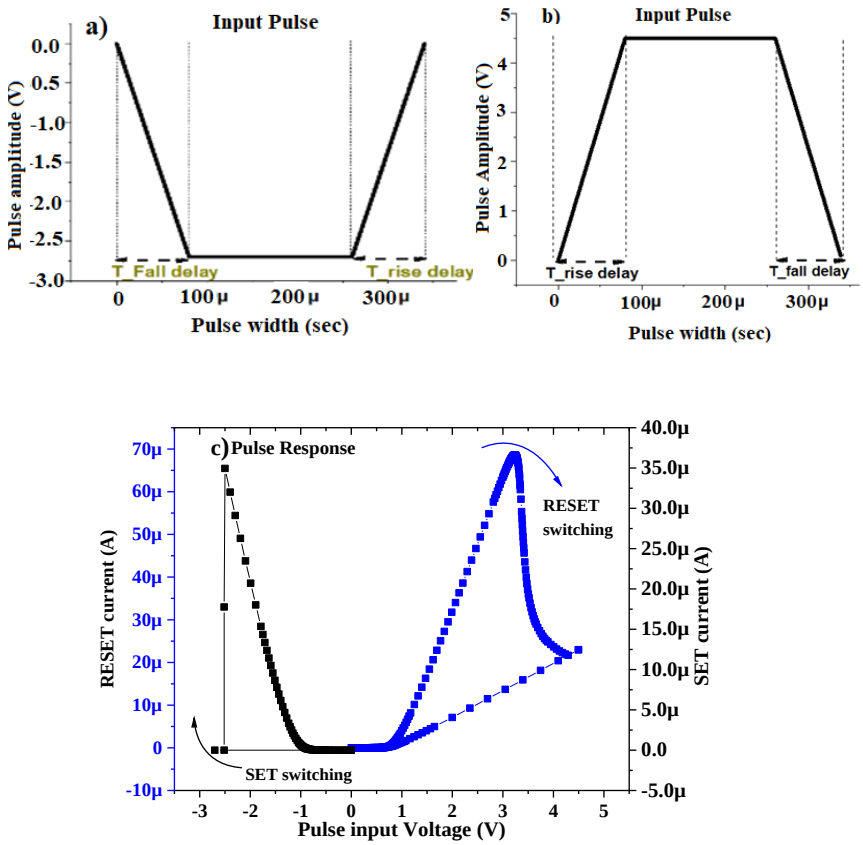


Fig. 6.5 Response of 1S1R model to pulse input (a) Negative pulse input and (b) Positive pulse input (c) 1S1R I-V characteristics with applied above-mentioned input pulses

Table 6.3 The parameters derived from the 1S1R model invoked with pulse input as given in Fig. 6.

Parameters	**1S1R (proposed electrical model)**
Roff/Ron ratio	~500
Nonlinearity ($V_{read/2}$, V_{read})	~1000
OFF-current(A) (at 0.5V)	70 nA
On-state current(A)	~70 µA
RESET Voltage	>=4.4 V
SET Voltage	~ -2.7

While analyzing, we have noticed that the pulse transition time (rise/fall) and the amplitudes of positive and negative pulses affect the switching characteristics. A study conducted on the dependence of rising delay of the input pulse on the RESET current is given in Fig. 6.6(a), in which three positive input pulses are applied to the model with rising transition delays of 0.5 ms, 1.0 ms, and 1.5 ms. Its corresponding characteristics illustrate that increase

in transition delay affects the slew rate at which the RESET current changes. Besides, this increase in the rising delay of the signal causes a trivial reduction in RESET voltage as well. Fig. 6.6(a) marks the increase in delay and the reduction in RESET voltage (top). Similarly, a decrease in pulse amplitude (Vp) also affects RESET voltage, illustrated in Fig. 6.6(b) where the current settles at 10 µA.

Alternatively, the influence of pulse amplitude on RESET is investigated, which is also depicted in Fig. 6.6(c). When the model is simulated with a pulse amplitude of 3 V, the device RESETs, while the characteristics do not follow the RESET characteristics of the RRAM. That means the rupture of filament is not complete. The same was the case with pulse amplitude 3.3 V, but when simulated with a pulse of amplitude 4.4 V, the device RESET followed the RRAM characteristics. Therefore, it can be concluded that the 1S1R model requires at least 4.4 V to attain a complete RESET.

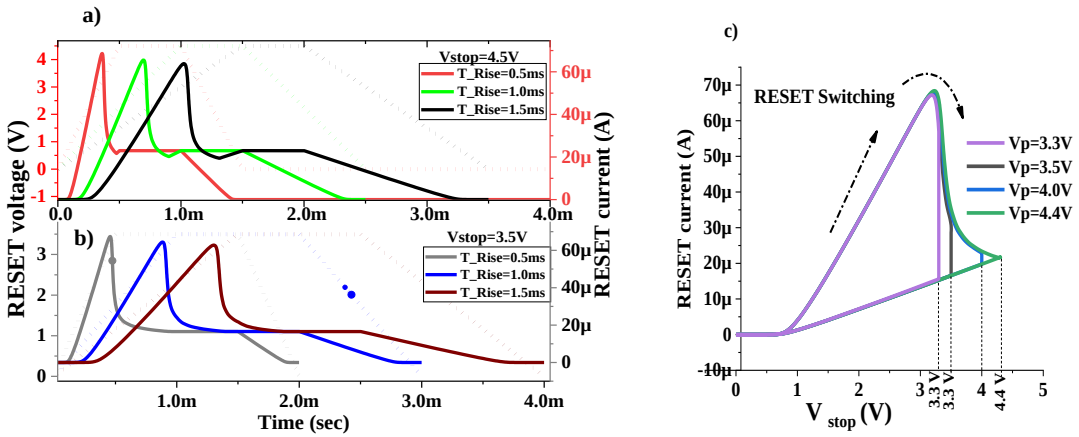


Fig. 6.6 Dependence of pulse rise delay time on 1S1R model behavior (dotted lines indicate input pulse and solid lines indicate simulated results) (a) Slew rate of the RESET current on the response of a positive pulse with 4.5 V pulse height,0.5 ms pulse width, and three different T_rise delays (0.5ms,1.0ms,1.5ms) (b)Response of a positive pulse with 3.5 V pulse height,1.0 ms pulse width and three different T_rise delays (0.5 ms,1.0 ms,1.5 ms) showing incomplete RESET with a shift in switching voltage (bottom) (c) Illustrating the possible range of pulse amplitudes to attain complete RESET by showing the influence of pulse amplitude variation on 1S1R characteristics.

Likewise, in Fig. 6.7, the dependence of pulse fall time delay (T_fall) and the amplitude on SET switching have been tested for the 1S1R model. As shown in Fig. 6.7(a), the simulation has been performed with negative pulse of different pulse fall time (T_fall) delay such as 0.08, 0.14 and 0.17 ms with a pulse amplitude of -2.7 V are applied to the integrated model. It has been investigated that increase in T_fall delay results in a decrease in SET voltage of the setup.

That is, when T_fall is 0.08 ms, the device transit from high resistance state (HRS) to low resistance state (LRS) at a potential of -2.7 V. In contrast, for a T_fall delay of 0.17 ms, the model exhibits SET switching at a potential of -2.4 V. Thus, during SET switching, T_fall delay of input voltage causes variation in SET voltage. We observed that the SET switching voltage shows a tendency to shift right with an increase in T_fall delay.

Next in sequence, to test the behavior of 1S1R model on response to different pulse amplitudes, several simulations are conducted as shown in Fig. 6.7(b), it is found that the SET state is attained only over a range of -2.6 V to -3.6 V. Fig. 6.7(c) shows that below -2.6 V, the device does not exhibit SET switching due to the voltage distributed across the RRAM is not enough to drive the device to LRS state, whereas when the model is executed with a voltage greater than -3.6 V, it exhibits an overset phenomenon which is likely due to the diffusion of oxygen vacancies out of the conduction filament or due to depletion of vacancies near the bottom interface leading to conduction filament rupture near the bottom electrode thus creating a strong electric field in the direction towards the bottom electrode so that the electrons flow in the opposite direction leading to the occurrence of a current in the opposite direction, hence a current of magnitude +800 nA to +10 µA flows through the device for some time, and then-current settles at a negligible value. This effect seems to be due to the formation of an equivalent capacitor with a bottom electrode acting as one plate and conductive filament act as another plate with dielectric sandwiched between them. Hence, it acts as a short circuit to the sudden dc pulse, conducts current, and subsequently settles down to zero.

When considering the 1S1R circuit in the perspective of sneak current, it is obvious that the proposed 1S1R circuit is beneficial to use in crossbar array as its OFF-current is within -1 to 1 V settles at nano amperes and the low/ high resistance are distinguishable with enough memory window to store binary data states. Moreover, the non-linearity exhibited by the 1S1R model enables to choose a distinguishable voltage range to bias both selected and unselected cells. In this study, the read voltage and write voltage required to supply with trails at cross points of selected and unselected cells are predicted.

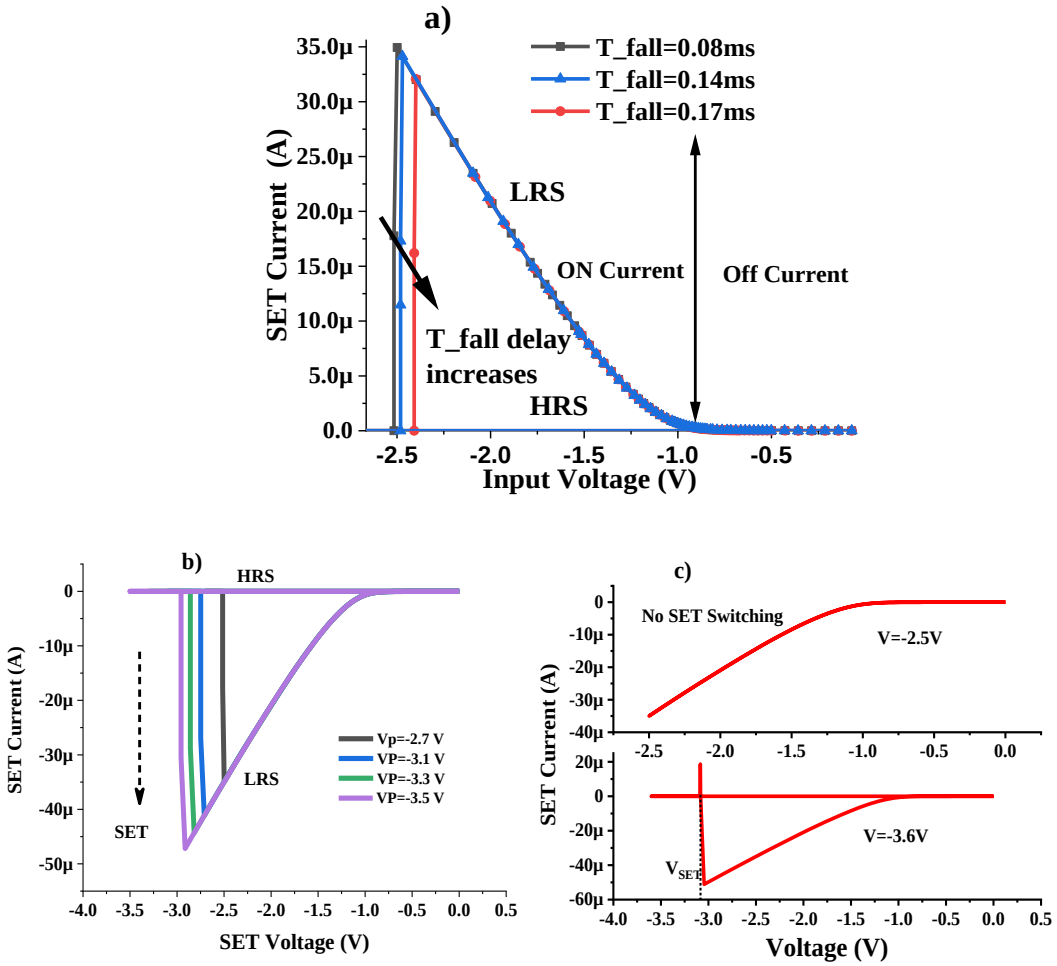


Fig. 6.7 Demonstration of pulse transition delay and pulse amplitude on 1S1R characteristics (a) Shift in SET switching voltage with transition delays (T_fall) (b) Dependence of various pulse amplitudes on SET switching characteristics (c) Demonstration of no switching condition (top) and over set(bottom) with pulse amplitudes -2.5V and -3.6 V respectively to define the range of pulse height for programming

The write operation is performed with an input voltage ranging from -2.6 V to -3.6 V, which drive the device to on-state, and at least 4.4 V is required to drive the device to off- state, whereas to perform read operation with selected cell, the range of voltages from 1.3 to 1.8 V is preferred.

6.5 Formation and sneak current measurement of 2x2 CBA of 1S1R with $Ta_2O_5/TaO_x/TiO_2$ and Ta_2O_5/TaO_x

Crossbar arrays (CBAs) of dimension 2x2 are created with the $Pt/Ta_2O_5/TaO_x/Pt$ RRAM model (1R) and $Pt/Ta_2O_5/TaO_x/TiO_2/Pt$ selector model to investigate the performance of 1S1R in reducing the sneak path current. The sneak path current problem in CBA becomes

crucial while performing the read operation; therefore, in this study, the read is performed in both 1R and 1S1R array at worst-case conditions. In the worst-case scenario, the selected cell should be in HRS, and all neighboring unselected cells should be in LRS to make the circuit prone to sneak path current.

Initially, RRAM CBA is developed with the selected RRAM model after keeping it in HRS and all other neighboring cells at LRS, and the sneak path current is analyzed while performing the read process. In CBAs, read/ write can be achieved by adopting various schemes such as floating schemes, V/2, and V/3. The word and bit line associated with the selected device will be connected with Vdd and GND in all three schemes, respectively. In the floating scheme, word and bit line trails of the unselected cell kept open, whereas in V/2 scheme, the word and bit lines of unselected cells connect to Vdd/2. Likewise, in V.3 scheme, the word lines of all unselected cells biased with a potential of V/3, and their bit lines biased with 2V/3 bias. Among these three schemes, the V/3 scheme is used in the proposed crossbar arrays to perform read/write.

In 1R crossbar array (Fig. 6.8(a)), the read is performed with a positive pulse of amplitude ~1 V as given in Fig. 6.8(b), whereas in 1S1R CBA read process requires 1.8 V, considering the drop across the selector. To read the data from 2x2 RRAM array (without selector), an input pulse of 1 V with 300 ns pulse width is applied and the measured sneak path current is 10 µA whereas, in the 1S1R array, the worst-case read process is invoked with 1.8 V, 300 ns pulse with rise/ fall time delay of 200 ns each and the corresponding sneak path current calculated as 56 nA. Hence, the observation is that 98% of the sneak current is reduced in the 1S1R array compared to the 1R array. Moreover, it has been noticed that the voltage drop across the unselected 1S1R cell is ~0.6V, whereas the drop across the selected 1S1R is ~1.9 V.

Also, the voltage distribution across the selector in the selected 1S1R cell during read is 0.98 V and at RRAM cell is ~1 V. Fig. 6.8 (c) shows the layout of the 1S1R array. Also, Fig. 6.8(d) and (e) show the voltage drop and the current across /through the selectors in the array, respectively. Here S2 is the selector at the selected 1S1R cell and the remaining selectors such as S1, S3 and S4 are unselected ones. As the voltage drop across the selector in the selected cell is ~1V, the current across the model increases in a non-linear manner, facilitating more voltage to drop across the RRAM cell.

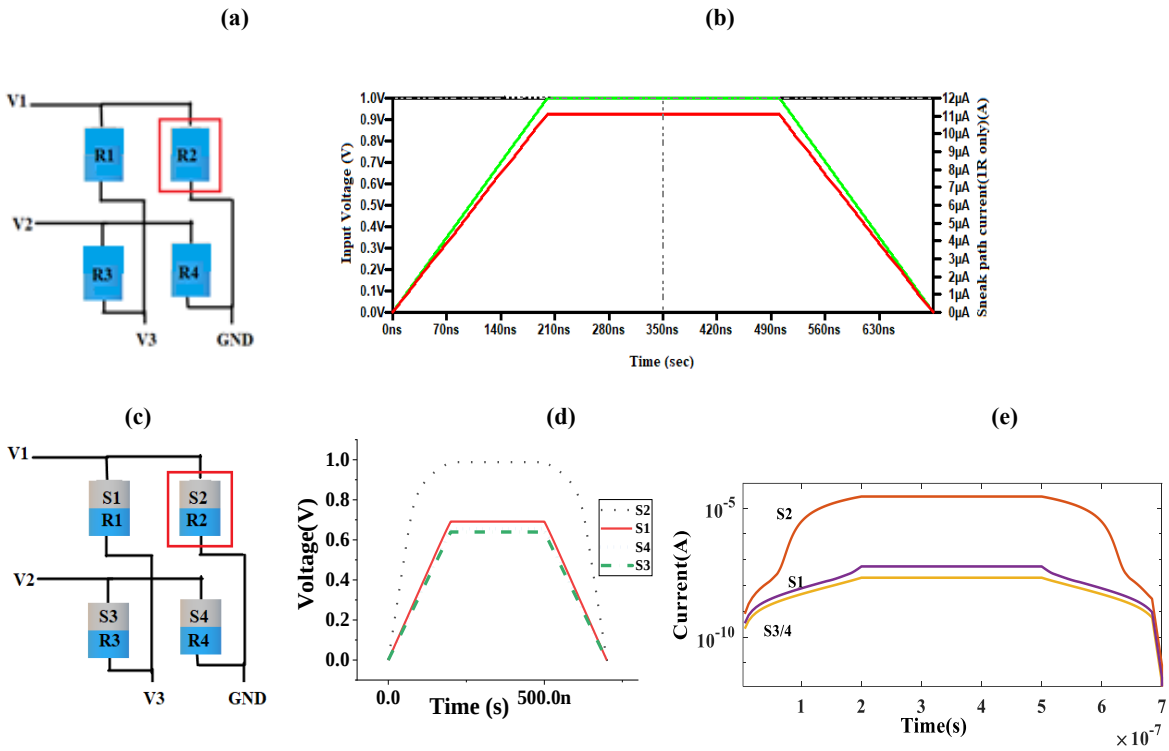


Fig. 6.8 (a) The layout of 2x2 crossbar array of RRAM only, (b) input pulse and sneak current measure from 1R array (c) Crossbar array of 1S1R where S2-R2 is the selected cell marked with a red square(d) The voltage distribution across the selectors S1, S2, S3, and S4. (e) current distribution across the selectors

The voltage across the unselected selectors is in the range of 0.6-0.7 V, which provides a comparatively lower current to drive the RRAM device; hence the unselected memory device remains switched off to prevent the sneaking current during the read process.

6.6 1S1R design with Proposed selector and Stanford/Beijing model of TiN/HfO$_x$/TiO$_x$/Pt RRAM

This section presents the details of the 1S1R cell composed of a proposed selector device and Stanford/Beijing resistive RAM connected in series (Fig. 6.9). The Stanford/Beijing RRAM model is a TiN/HfOx/TiOx/Pt oxide-based RRAM fitted with its parameters. The simulation of this model is carried out in CADENCE Virtuoso tool. The I-V characteristics obtained from the TiN/HfOx/TiOx/Pt model are displayed in Fig. 6.10 (a) and the integrated I-V characteristics are shown in Fig. 6.10 (b). In Fig. 6.10 (b), it is understood that from -1.5 V to 1 V the current is pinched off. The characteristics of the selector model dominate the characteristics of the cell.

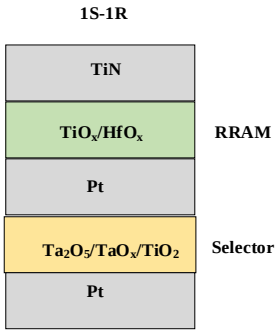


Fig. 6.9 The device layout of 1S1R showing TiOx/HfOx and proposed selector

In comparison, from -1.5 V to -5 V and from 1 V to 5 V, the characteristics is dominated by the RRAM device characteristics as shown in Fig. 6.10 (a). Also, we can see from Fig. 6.10 (b) that the switching voltage of the 1S1R cell becomes higher as compared to the RRAM characteristics. The required voltage to drive the cell to LRS is now 2.5 V; while driving the cell to HRS the required minimum voltage is -3.0 V. Various parameters related to TiN/HfOx/TiOx/Pt selector combination is given in Table 6.4.

Table 6.4 Parameters derived from 1S1R device

	1S1R (proposed electrical model)
Roff/Ron ratio	~100
Nonlinearity ($V_{read/2}$, V_{read})	~20
OFF-current(A) (at 0.5V)	8 nA
On-state current(A)	0.4 mA
RESET Voltage	>-3.0 V
SET Voltage	~ 2.5V

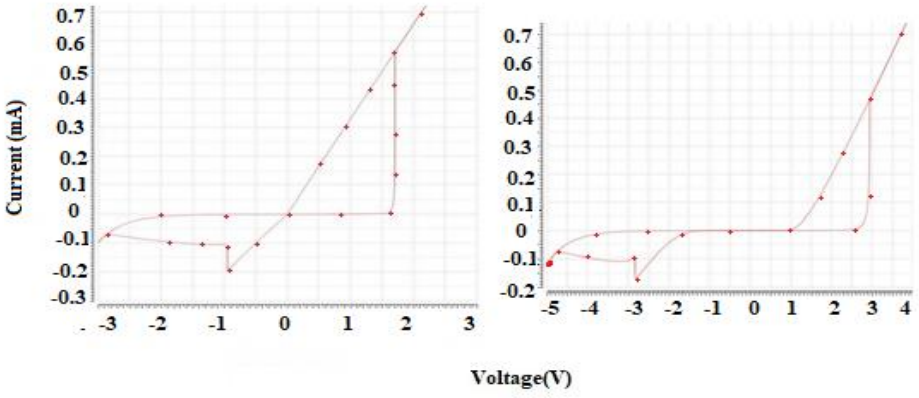


Fig. 6.10(a) TiN/HfO_x/TiO_x/Pt RRAM(b) The 1S1R model of RRAM with Pt/Ta_2O_5/TaO_x/TiO_2/Pt selector

1S1R and One Resistor (1R) crossbar arrays are formed with parasitic resistances (2.5 ohms per wire segment) of sizes. The state of all unselected devices remains unchanged. Read I_{on}/I_{off} ratio of 1S1R becomes 23 while for 1R array it is 5. Similarly, the total current seen in 1S1R is 0.4 mA, while in 1R, it is 1mA. Similarly, the sneak current measures in 1S1R are 6 nA, and for 1R, it is 2.5 μA. From analysis, it is found that the sneak path current increases with array size.

6.7 Implementation of 1S1R with Proposed selector model and HP memristor model

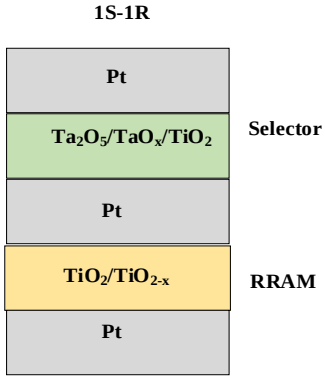


Fig. 6.11 The schematic of the 1S1R configuration

The schematic of the 1S1R configuration is shown in Fig. 6.11, in which both devices serially connected. Here, the selector device is Pt/Ta_2O_5/TaOx/TiO_2/Pt, and the HP memristor model is Pt/TiO_2/TiO_{2-x}/Pt. In this circuit, the middle electrode in both devices is the same; platinum is the shared metal electrode. The simulation results of the 1R and 1S1R are given in Fig. 6.12 (a) and (b), respectively. The device SET to LRS state at ~2V in 1R whereas in the 1S1R the SET voltage shifted to ~3.5 V. Likewise, the RESET voltage is also shifted from -1.5 V to -3.7 V.

The state transition diagram of the 1S1R is given in Fig. 6.13, where the device's state is initially at ‘0’ and at 0.05 sec. Further, the state of the model evolved to ‘1’ and later at ~0.15, the state transit back to ‘0’ so that the device model turned to off-state

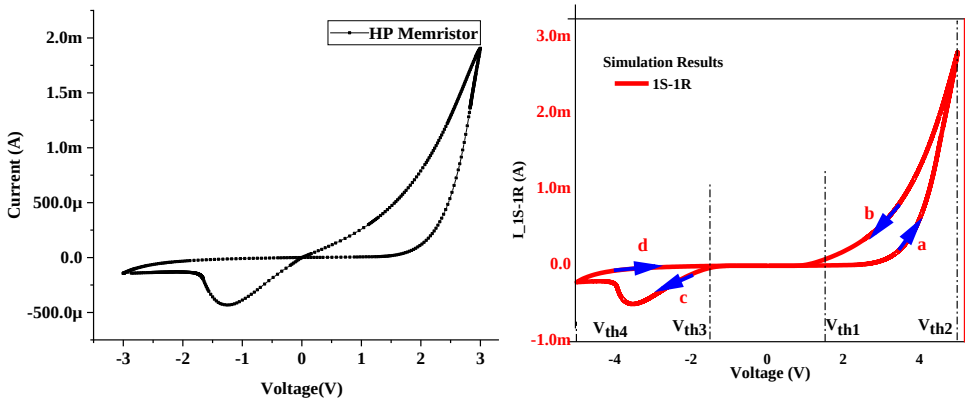


Fig. 6.12 a) The HP memristor RRAM model showing the hysteresis loop b) integrated electrical model of HP memristor and proposed 1S1R model

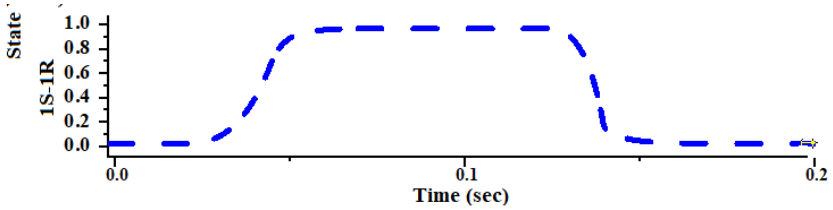


Fig. 6.13 State evolution diagram of the 1S1R model of HP memristor and proposed selector model

After that, the performance of the model to read write pulses is evaluated and see that on response to write '1', the model shows a current level of ~-800 µA, and for the write 0 pulse the device current reached 400 µA whereas, during read 0 the model has shown a difference of readout current of 38 µA is noticed in the model. The programming pulses and their corresponding output current is shown in Fig. 6.14(a). Further, the sneak current is measured after subjecting the mode to different write schemes such as floating, V/2, and V/3 as given in Fig. 6.14(b), where the V/3 scheme is found efficient over others. From this model, the measured sneak path current is in the order of several µA. Also, the comparison of sneak path current of 1S1R and CRS during read operation is compared and results are given in Fig. 6.14(c). Sneak current present while reading the data from 1S1R is less compared to CRS in all three schemes.

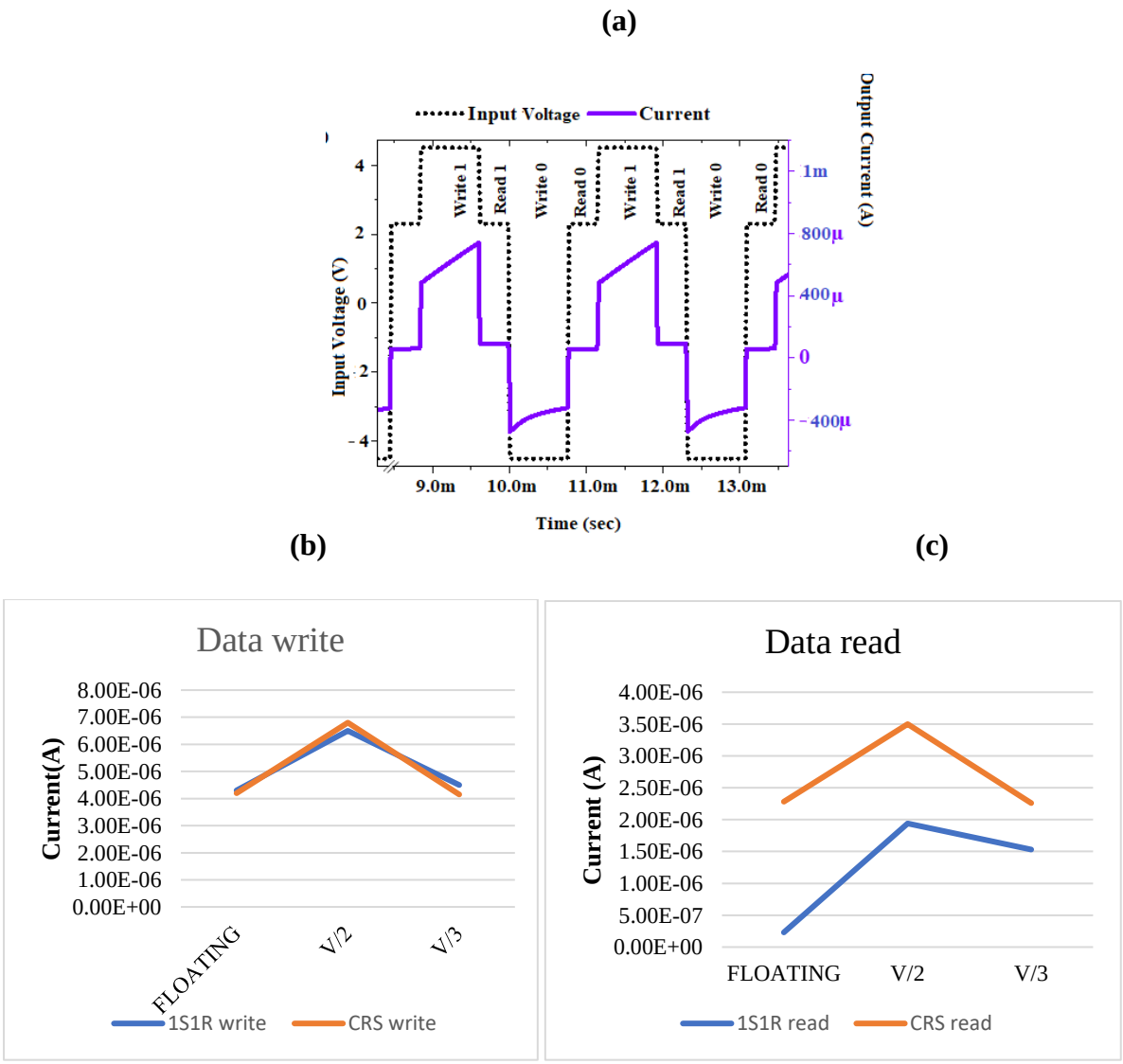


Fig. 6.14 (a) Read/write performed in IS1R array (b) comparison of sneak path current while writing data to 1S1R and CRS array (c) Sneak path current measured during read operation in three different schemes

6.8 CRS model of HP memristor

As an alternative method, the CRS model of HP memristor is also developed using the LTSPICE tool. The conventional CRS devices are formed by connecting RRAM devices in an anti-serial configuration. In this work, the basic memory element used to develop CRS is Pt/TiO_2/TiO_{2-x}/Pt RRAM model [13], otherwise known as HP memristor. Following the conventional method, back-to-back connected CRS cell is developed using an existing model of HP memristor.

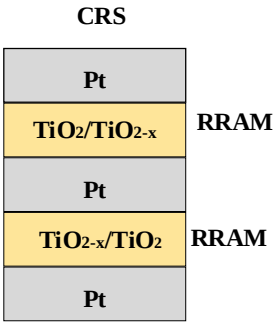


Fig. 6.15 Structure of Complementary switching device developed with back to back connected RRAMs

The adopted model is a generalized SPICE design developed by Yakopcic et.al [176]. In which various model parameters are modified to obtain the HP memristor characteristics [176]. The Pt/TiO_2/TiO_{2-x}/Pt/TiO_{2-x}/TiO_2/Pt structure of the CRS model is shown below in Fig. 6.15.

6.8.1 Simulation result

The I-V characteristics obtained from the simulation of the CRS model is given in Fig. 6.16 where Vth1, Vth2, Vth3, and Vth4 marks the threshold voltages of the complementary resistive switching model. Here, it can be noticed that the curve is symmetric with high resistance is shown at a region defined by Vth3 and Vth1. The characteristics have shown SET and RESET transitions both during positive and negative polarity of input voltage.

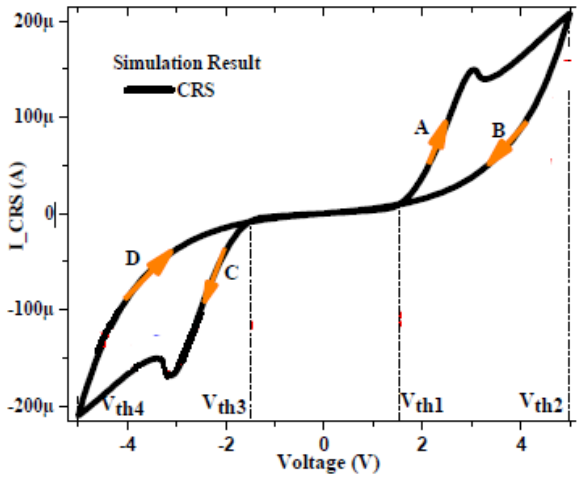


Fig. 6.16 The simulated I-V characteristics of CRS HP memristor

Next, the state variable analysis of CRS model in response to the input given in Fig. 6.17(a) is illustrated in Fig. 6.17(b). The state variables of RRAMs in CRS are represented with

a green dotted line and solid red lines in Fig. 6.17(b), where the legend RRAM1 denotes the RRAM connected on the top of the RRAM2 refers to the RRAM linked at bottom of CRS stack. Since two RRAMs are present at the device, the states can be represented with a pair of state variables describing the state variable of RRAM1 and state variable of RRAM2. Initially, the RRAM1 is in HRS, and RRAM2 is in LRS. Therefore, the state variable represents logic state 0. Then, the application of high voltages causes both RRAMs to partially on to switch in to LRS/LRS (ON- state). This happens during the transition of input threshold voltages Vth1 to Vth2 (marked in Fig. 6.17(b)), i.e., at time interval of 16 to 51 ms. Further increase in input to Vth2 turns RRAM2 to become in HRS with state variable indicated as state 1. Subsequently, when the negative input pulse is applied to the CRS cell, a transition of the state-1 to state-0 occurs after transiting through the completely ON-state (marked in Fig. 6.17(b) within the time interval 114 to 153 ms). However, in the model, the state variables switch between 0 and 0.4 and are weak signals that may introduce degradation in data storage after multiple cycles. In CRS array, the pulse train is not initialized, and it has been considered that the initial state of the RRAMs of CRS cell would be in LRS/HRS or HRS/LRS state.

Nonetheless, an additional write back signal (write 0) has been applied in the subsequent cycle after performing the read 0 process as the read 0 is a destructive process [21] as given in Fig. 6.13. The pulse signals used for SET and RESET in CRS are 4 V and -4 V, respectively, to write 0 and 1 logics. There are three schemes to write data to an array, they are floating, V/2 method and V/3 scheme.

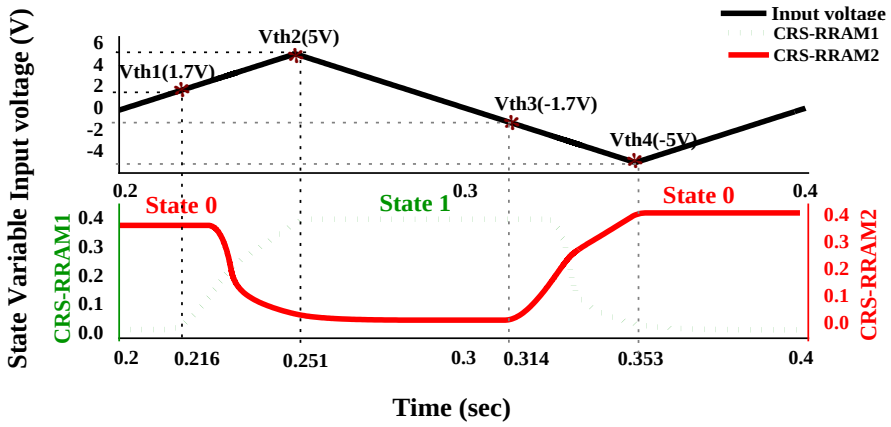


Fig. 6.17 a) Input voltage sweeps between -5 V to 5 V with period 200 ms. b) State variables of CRS where RRAM1 is the RRAM on the top and RRAM2 is the back connected memory cell

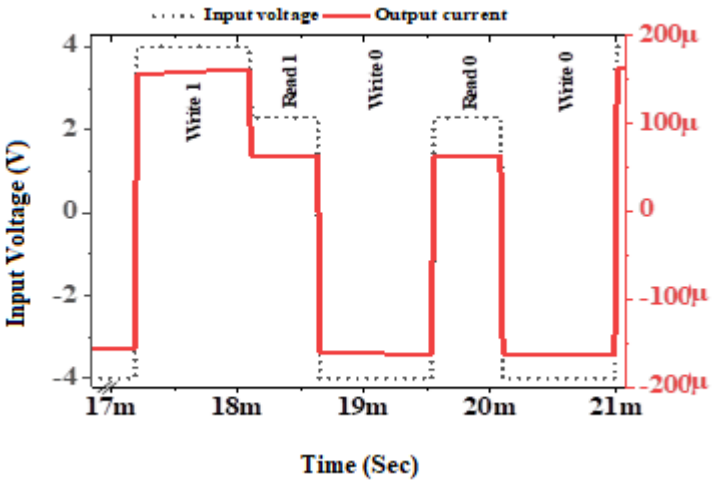


Fig. 6.18 Input voltage and current in CRS array with V/3 scheme

Among these three write schemes, floating schemes and V/3 schemes are found to be suitable for CRS arrays. Comparison of different RRAM models with Pt/Ta_2O_5/TaO_x/TiO_2 Selector model and CRS model of HP memristor is discussed below in Table 6.5. From the table it is interpreted that the non-linearity and off current of the selector is reflected on the 1S1R models. Also, it is found that 1S1R is effective in reducing sneak path current (>95%) while comparing with the CRS device model(93%). Moreover, it is conspicuous that the V/3 scheme is better to be adopted to perform read/write in 1S1R and CRS crossbar arrays. In the give table, the readout current is the difference in current measured at read voltage after driving the device to ON state and off-state (40 nA for Ta_2O_5 based RRAM with proposed selector) whereas, the sneak path current is a parameter related to the crossbar array.

Table 6.5 Comparison of different RRAM models with $Pt/Ta_2O_5/TaO_x/TiO_2$ Selector model, CRS model and CRS model developed with HP memristor(All parameters are calculated from simulated models)

Parameters	**1S Proposed $Ta_2O_5/TaOx/TiO_2$ Selector model**	**1S1R (Proposed selector with TiO_2/TiO_{2-x} HP model)**	**1S1R (Proposed selector with Stanford model)**	**1S1R (Proposed selector with $Ta_2O_5/TaOx$ model)**	**CRS Back-to-back connected HP memristor model**
Read	-	Nondestructive	Non destructive	Non destructive	Destructive
sneak path current (V/3 schemes) reduction (in %)	-	96%	99.8%	98%	93%
Roff/Ron	1	~15 at 2.3 V	~100	400	~8
Nonlinearity (Measured at Vread, Vread/2)	1600	~55	~20	~1000	~40
Readout current	-	38.6 µA	-	40 nA	6 µA
Off-current	46 nA	0.01 µA	8 nA	0.04µA	~1-7 µA
Sneak path current(read) (1S1R CBA)	-	1.5 µA	6 nA	56 nA	2 µA
Input signal	-	Initialization pulse is required	Initialization pulse is required	Initialization pulse is required	No initialization pulse
	-	No write back signal	No write back signal	No write back signal	Write back signal is needed
Suitable write scheme	-	V/3	V/3	V/3	V/3

In this chapter, the proposed trilayer selector model is connected with different RRAM models to check the compatibility of producing nonlinear memory characteristics in CBA to reduce sneak path current. Among other RRAM models, $Pt/Ta_2O_5/TaO_x/TiO_2/Pt$ selector with Ta_2O_5/TaO_x RRAM has shown better nonlinearity of 1000 with a reduced sneak path current of 56 nA when connected in a crossbar array. Also, it is reported that the V/3 scheme is suitable scheme to perform write to a nano crossbar memory array. Further, a comparison of the 1S1R with CRS is also demonstrated to show that 1S1R model is a better candidate to mitigate sneak current compared to the back-to-back connected CRS counterpart.

Chapter 7

Fabrication and characterization of a novel self-rectifying RRAM device and Complementary Resistive Switching device for sneak path current mitigation

Chapter Summary

This chapter discusses two solutions to eliminate sneak path current such as self-rectifying RRAM device and CRS device. RRAM with the self-rectification feature is obtained from the asymmetric metal-insulator-metal (MIM) structure made with Au/Al_2O_3/FTO stack. Subsequently, the electrical/structural characterization is done to show that the device characteristics vary in accordance with the polarity of forming voltage. Moreover, the device has shown a highly asymmetric self-rectifying characteristic with a non-zero crossing feature, and after multiple cycles, it turned in to 1D1R kind of characteristic, hence it is proposed that the device can be used in crossbar array to reduce sneak path current. However, when compared to 1D1R characteristics, complementary resistive switching (CRS) devices can reduce sneak current in a better way. Therefore, another design is proposed by including an additional switching layer, 'ZnO ', on the proposed RRAM stack to attain the bilayer complementary switching characteristics. Moreover, the device characteristics are promising due to its nonlinear nature, which reduces sneak path current. Moreover, the switching response, read/write process, and memory power consumption is measured. In addition, the switching mechanism as well the conduction mechanism occurring in the bilayer structure is explained.

Related publications

1. Complementary Resistive Switching in ZnO/ Al_2O_3 bi-layer devices, IEEE transaction on Nanotechnology (under review)
2. Arya Lekshmi, T. Nandha Kumar, A. F. Haider, and K. B. Jinesh, "Self-rectifying self-limited Resistive switching in Au/Al2O3/FTO Devices," 2021 IEEE 21st International Conference on Nanotechnology (NANO), 2021, pp. 17-20, doi: 10.1109/NANO51122.2021.9514299.

This chapter proposes two different solutions to reduce sneak current in a crossbar array, such as self-rectifying self-limited devices and complementary switching devices. The former is a recently evolved concept in the field. The first part of the chapter describes the fabrication and characterization of a self-rectifying device based on Au/Al_2O_3/FTO structure. Further, a complementary resistive switching device is fabricated, and characterization is performed.

Several advancements have been seen in the field of resistive random-access memory (RRAM), including the developments in the design of device structure and exploration of different materials other than transition metal oxides [82] such as ZnO [178], Al_2O_3 [179], MoOx [180], etc.. However, in this work, the Al_2O_3 material has been selected to obtain the switching characteristics. In our experiment, we deposited Al_2O_3 ALD with sequential exposures of $Al(CH_3)_3$ and O_3, where water is acted as the oxidizer. However, during the deposition, it is certain that dangling bonds and native defects form within the structure may cause the formation of energy states within the bandgap to facilitate the current conduction, whereby it is functioning as a RRAM device. The Al_2O_3 is a promising material for microelectronic applications due to its high dielectric constant, excellent stability, and thermal conductivity.

Moreover, the material is booming in the industry due to its memory property and versatility in various flexible electronic applications. Deposition of Al_2O_3 with Atomic Layer Deposition (ALD) technique provides a homogenous compact layer, and most importantly, the thickness of Al_2O_3 deposit is controllable on Ågstrom level [181]. Therefore, ALD is one of the most effective methods used in Al_2O_3 thin film fabrication. In this study, ALD deposited Al_2O_3 is used to ensure the precision in thickness of the thin layer. The next switching material used in CRS design is ZnO, which is preferred due to the presence of multiple defects in its atomic structure that can source oxygen vacancies/defects for resistive switching. ZnO is a direct wide bandgap semiconductor from group II-IV, with a bandgap of 3.37 eV; it is also an emerging material for manufacturing flexible electronic devices and neuromorphic computing applications. Based on growing/depositing conditions, ZnO can take nanoribbon, nanorod, nanowire, thin-film forms, etc. [182]. Among these morphologies, the FESEM images of the ZnO deposition appear as a thin film.

7.1 Fabrication and Characterization of self-rectifying $Au/Al_2O_3/FTO$ device

7.1.1 Experiment Procedure

The fabrication starts with the preparation of Fluorine doped Tin Oxide (FTO) coated glass slide of thickness 2.3 mm with the resistivity of 7 Ohm/sq, where FTO is the conductive material which is sonicated and prepared to act as the bottom electrode (BE). Further, the active layers are formed with the atomic layer deposition (ALD) technique. For the entire deposition process, the temperature at the top chamber of ALD is set at 110 ^{o}C, pressure is maintained below 0.4 mbar, and the bottom chamber temperature is set to 200 ^{0}C. Under this ambiance, the active switching layer Al_2O_3 is deposited by controlling the purge gas (N_2) exposure time with a controlled flow of precursor (TMA) and oxidizer (water). One cycle of the ALD process can deposit Al_2O_3 with 0.12 nm thickness; therefore, to deposit 10 nm of Al_2O_3, 80 ALD cycles had been run. Subsequently, the Gold (Au) top electrode (TE) is deposited with a thermal evaporator. In this thermal evaporation step, multiple devices are defined with a top electrode using a shadow mask of 960 µm diameter. The schematic/ structural layout of the devices are shown in Fig 7.1(a), where TE is Au (100 nm), the oxide layer is Al_2O_3 (10 nm), and the bottom electrode is FTO. Fig. 7.1(b) shows the top view of devices where each circle represents the individual device.

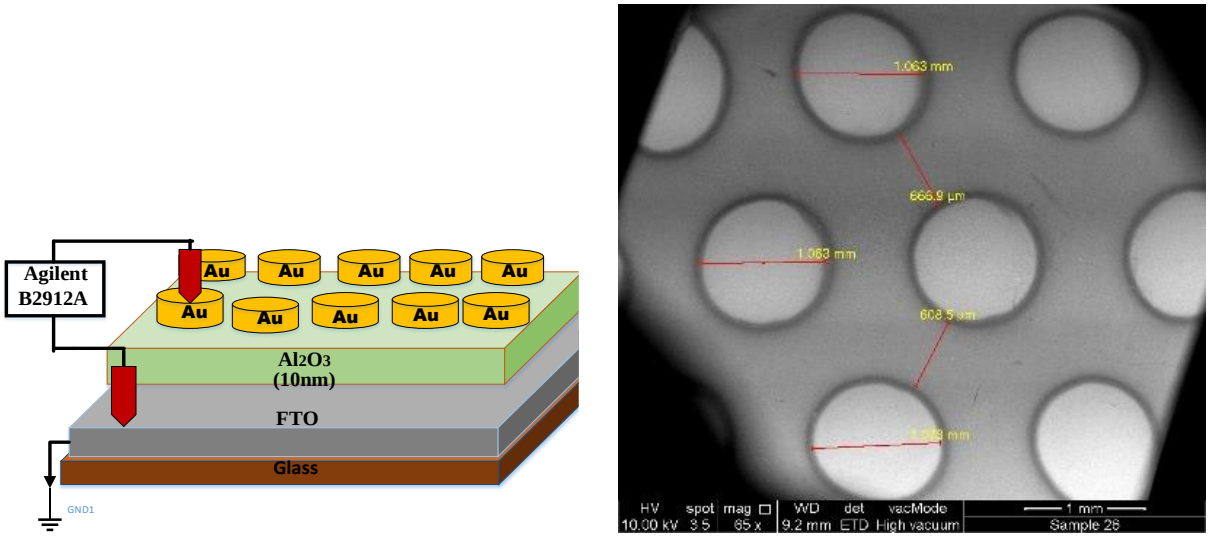


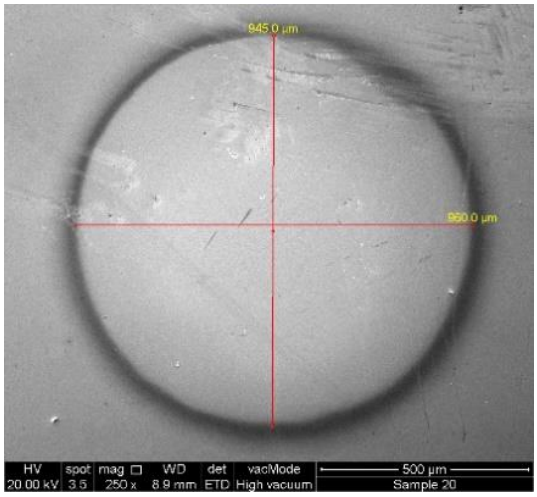
Fig. 7.1 (a) Structural lay out of the device showing three layers $Au/Al_2O_3/FTO$ (b) Top view of a sample with the devices arranged in the sample(with a minimum of 600 µm distance between devices to ensure no conduction between devices)

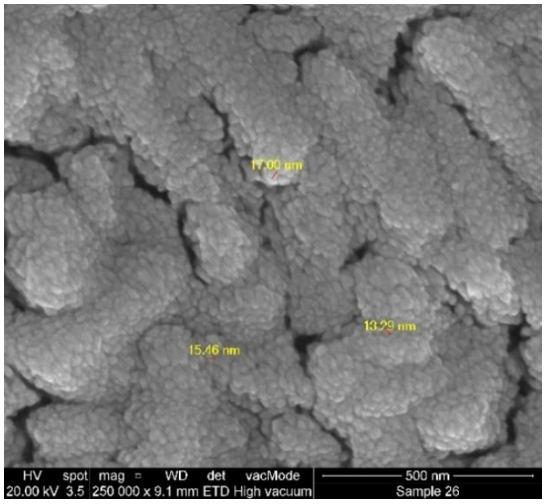
Thus, the proposed device stack is Au/ Al2O3/FTO corresponding to the metal-insulator-metal (MIM) structure, as shown in Fig. 7.1. The input voltage is applied on the top electrode, and the bottom electrode is kept grounded.

7.1.2 Structural characterization of the device

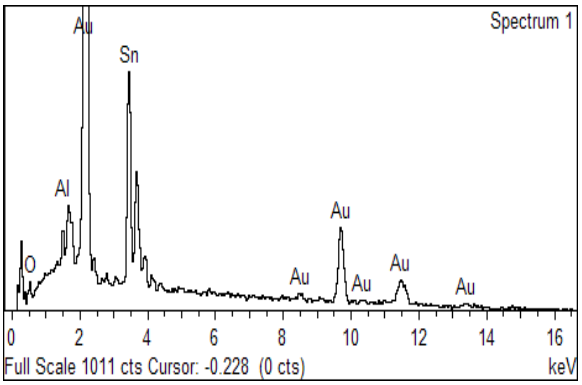
Further, the structural characterization is performed using FEI Quanta 400F FESEM (Field emission scanning electron microscopy) with EDX (energy dispersive x-ray spectroscopy). We observed that each device has a diameter of ~960 µm and the electrode material deposition is uniform from the surface morphology

a) **b)**





c) **d)**



Element	Weight%	Atomic%
O K	2.23	18.44
Al K	0.84	4.13
Sn L	27.65	30.85
Au M	69.28	46.58
Total	100	

Fig. 7.2 (a) Top view of the Diameter of one device (b) Uniform Gold deposition on the surface (c)&(d) EDX analysis of Au/Al_2O_3/FTO and distribution of atomic weight and percentage weight of each element

Fig. 7.2(a)shows a single device with the measured diameter, and Fig. 7.2(b) depicts the uniformly deposited Gold. From the FESEM measurements, the gold particle size is found to be approximately 17 nm. Besides, the EDX analysis is also done for the device, and the elemental distribution is shown in Fig. 7.2 (c), and its atomic weight is listed in the table shown in Fig. 7.2 (d). EDX shows a spectrum of various elements in the sample/device, plotting its intensity (arbitrary unit) versus the energy in kilo electron volt (keV). Fig. 7.2 (c) shows a spectrum of elements with Au and Sn peaks representing the Gold and Tin depositions from the electrodes. Meantime, we can identify the presence of Aluminum (Al) and Oxygen (O) as well. From Fig. 7.2(d), we can recognize all the sample's deposited elements and atomic weights.

7.1.3 Electrical characterization and Results

Electrical characterization of the device is performed with an Agilent B2912A precision source measure unit (SMU) by keeping the sample in the dark chamber at room temperature. The onset of characterization starts with the evaluation of resistance of the device at a pristine state. As-deposited devices have shown high resistance of ~ one tera Ohm ($1e^{12}$). The initial step to start the electrical characterization is the electroforming step. So, all the devices are electroformed with either positive or negative polarity of input voltage. Even though devices are formed with the positive or negative input voltage, all devices showed resistive switching. The devices switched to Low resistance state (LRS) at the negative polarity of input voltage and RESET to high resistance state (HRS) at positive polarity. As the device structure is MIM, due to asymmetry in top and bottom electrode materials, the device shows asymmetry in its I-V characteristics irrespective of the polarity of forming voltage.

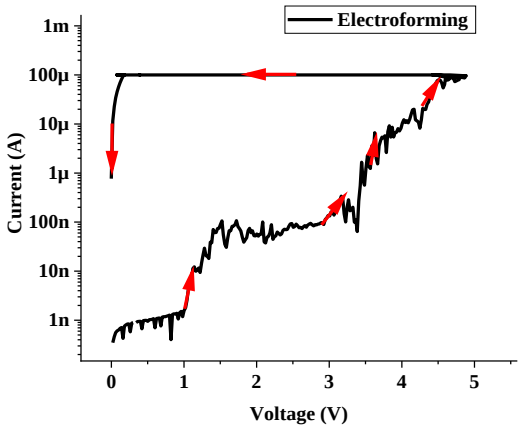


Fig. 7.3 Electroforming with a positive voltage

Besides, it is noticed that the I-V characteristics exhibited by both positively and negatively formed devices seem to be different. Therefore, the study of characteristics obtained from both types of devices is given in detail. At first, the characteristics of the positively formed device is discussed below.

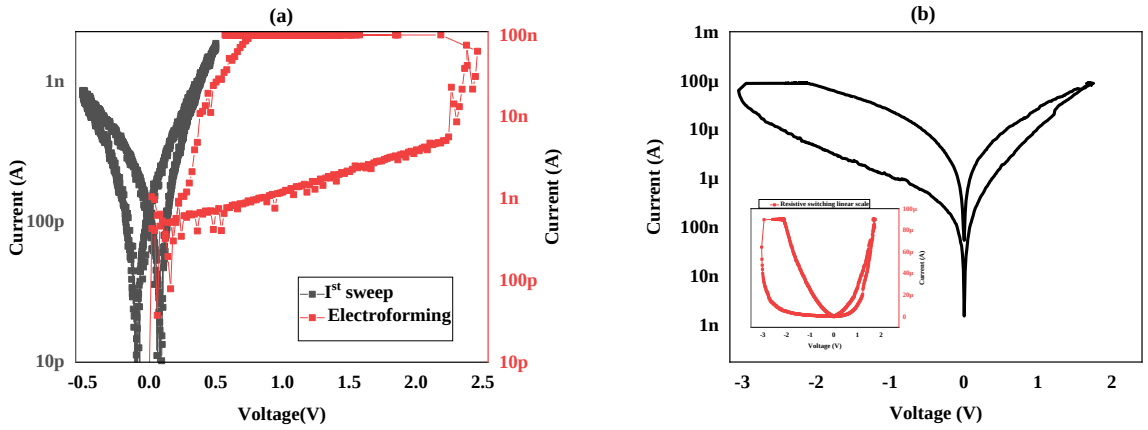


Fig. 7.4 (a) Electroforming (red symbols) and butterfly characteristics obtained with initial sweeps (black symbols) (b) First resistive switching characteristics with compliance current 100 µA, inset shows the linear I-V characteristics.

/During the forming, the device is subjected to a positive input voltage sweep from 0 to 10 V, and the device showed an increase in current from 1 nA to 100 µA at 0 to 5 V as in Fig. 7.3, it is noticed that the complete forming occurs through multiple intermediate resistance levels. However, it is beneficial to electroform the device with a low magnitude of the current so that the operating current can be limited. For instance, a device is electroformed with a positive dc sweep voltage from 0 to 10 V with external compliance of 100 nA, where the current is ramped up to the compliance current (Ic) level at ~2.2 V as shown in Fig7.4 (a). On the subsequent cycle, a low magnitude of input voltage (|0.5|) is swept to obtain a butterfly curve [180] as plotted in Fig. 7.4(a) (black symbols). At this stage, the device resistance is decreased a few orders compared to the pristine device, which means that the device is still in high resistance due to weak electroforming.

However, performing strong electroforming with increased Ic ($9e^{-5}$ A) and high voltage (15 V) resulted in the normal bipolar resistive switching behavior (BRS). The I-V characteristics of a positively formed device on response -4 to 2 V is shown in Fig. 7.4 (b), where the switching is analog with a gradual SET start at -3 V, and a slow reset occurs at ~2 V (Inset of Fig. 7.4(b) shows the characteristics on a linear scale). Moreover, the device switching behavior is

analyzed with different current compliance levels for multiple cycles, as shown in Fig. 7.5(a), where the maximum current in the device changes with Ic. However, the device displays an asymmetric switching behavior with self- rectification [183], and it is likely to be due to incomplete rupture of the conduction filament during RESET switching.

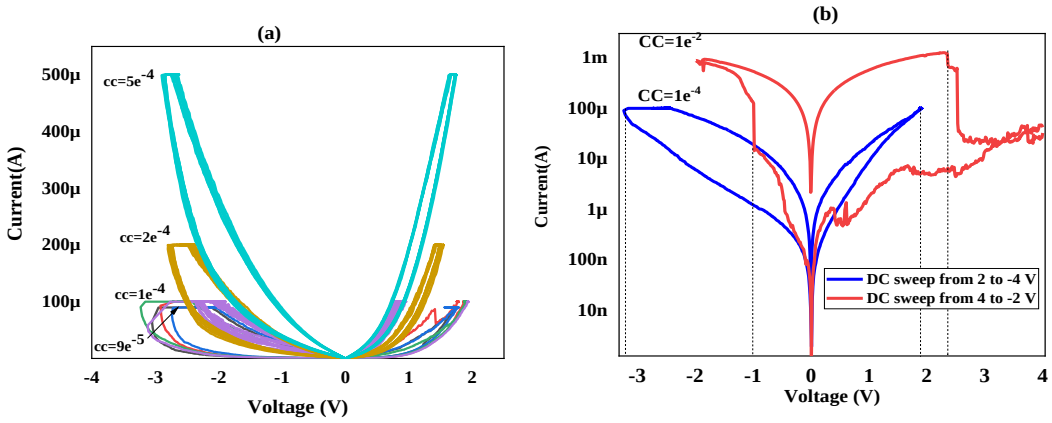


Fig. 7.5 (a) Multiple switching cycles at different compliance current (b) Initial analog characteristics (solid blue lines) and digital switching obtained after extending the RESET voltage to 4 V (solid red lines).

Therefore, the positive sweep voltage is further extended to 4 V, so the device is completely turned off by rupturing the filament, creating a depleted area between the top and bottom electrodes. Hence, a strong electric field across it shows that deep resetting provides a large memory window in Al_2O_3 devices, as reported in [184]. In addition to self-rectification, the device has demonstrated self-limited switching, meaning the maximum current in the device is limited due to internal mechanisms. Further, the device has shown a perfect digital resistive switching characteristic with a high Roff/Ron ratio >400 and non-linearity measured with respect to read and SET voltage ~5 and 4. However, the device's asymmetrical analog characteristics are promising to use in neuromorphic applications [185]; therefore, if the applied voltage and Ic fine-tune the behavior of the proposed device, we can use it in various applications [180].

On the contrary, an analysis is carried out on the negatively formed devices, where the device EF by applying -15 V after setting up external compliance of 1 µA. Subsequently, an input dc sweep from 3 to -3 V with a compliance of 10 mA is applied to the formed device. In response, the device exhibited an asymmetric resistive switching, as shown in Fig. 7.6(a). Also, the device displays the self-rectification feature prominently at LRS. The device's rectification factor is measured by taking the ratio of current at low resistance state (LRS) obtained with

forward bias (positive polarity) and reversed bias (negative polarity) measured at a specific voltage. In the proposed device, the rectification ratio measured at LRS is 200 (I forward bias /I reverse bias, at V=1V), which demonstrates the possibility of reducing the cross-talks or sneak current in the passive nano crossbar array, which has got tremendous attention in recent years [186]. However, an interesting phenomenon of device current with zero input voltage is also noticed; such phenomenon is reported in many RRAM devices and is termed as non-zero crossover characteristics marked in Fig. 7.6(a), with a dotted circle.

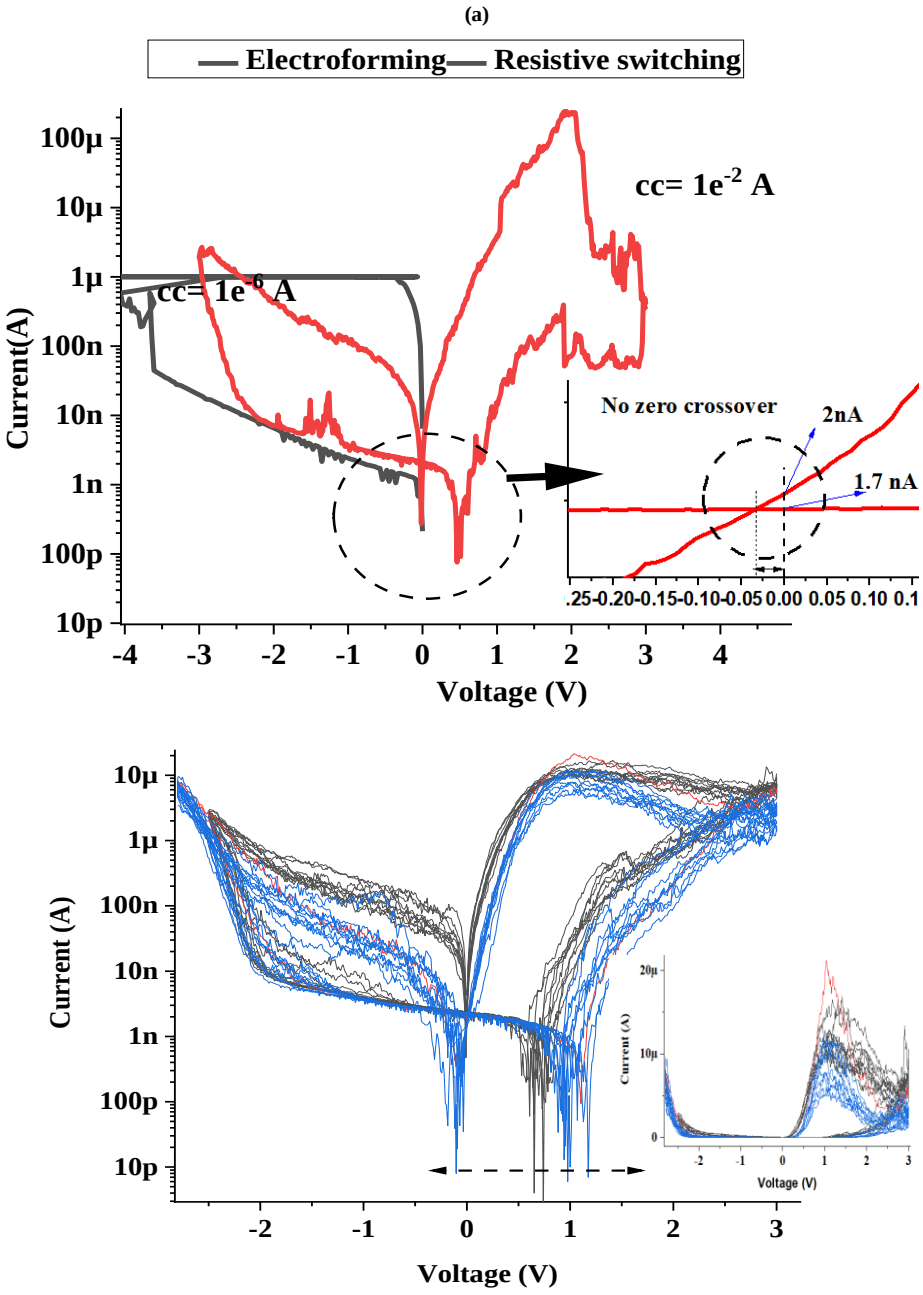


Fig. 7.6(a) electroforming (solid black lines) and initial resistance switching (red lines) in a negatively formed device (inset: the non-zero crossover) (b) multiple I-V cycles of the negatively formed device (inset shows the multiple cycles on a linear scale)

Besides, the zoomed view of the circled region is shown in the inset of Fig. 7.6(a), where it illustrates the non-zero crossover phenomenon by demonstrating the presence of ~2 nA current that flows through the device when the device input voltage dropped to zero. Besides, the crossing point is shifted to the third quadrant showing that the device is beneficial to neuromorphic applications due to the coexistence of memcapacitive/meminductive properties [187]. Moreover, after multiple cycles, the device exhibited a shift in crossover point to the left of the x axis, which means the non-zero crossover is additive the device characteristics are turning to a 1diode-1RRAM kind of characteristics [188]. Several arguments are going on to explain the non-zero crossover process [189], which includes the presence of an internal electric field generated due to the capacitance effect of the MIM devices or due to the formation of electromotive force developed within the device or due to ferroelectric nature of the device. In this case, the third probability is ruled out as the proposed material is not reported as a ferroelectric material. Hence, the former suits well with the non-zero crossover phenomenon in this proposed device due to the asymmetric MIM structure.

The I-V characteristics obtained with multiple devices are also tested (device-to-device variability) to analyze the property. However, the variability is evident in various devices as shown in Fig. 7.7, where the negatively formed device has shown a significant level of non-zero crossover. In contrast, a few positively EF devices also showed a negligible non-zero crossover level after multiple cycles. Also, it is conspicuous that the I-V curves follow a clockwise switching (CWS) direction, which ensures that resistive switching of the device is filamentary and can be explained after the formation and rupture of a conduction filament [187].

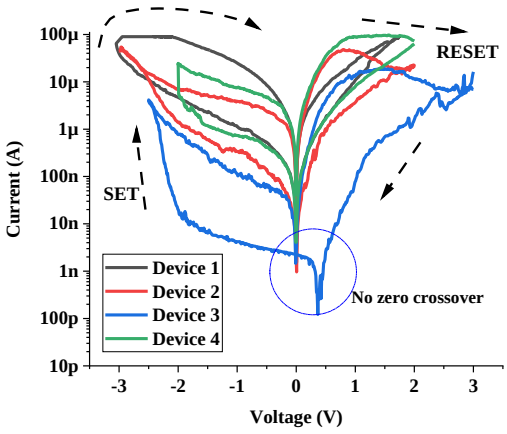


Fig. 7.7 I-V curve shown by various devices (D2D variability), blue circle shows the non-zero crossing

Next, the device's reliability is tested using multiple cycles of input read/write cycles known as retention and endurance. The retention of the device is measured at room temperature on response to a read voltage of 0.25 V for $>10^3$ sec and found that the device maintains its LRS and HRS levels (Fig. 7.8(a)). Further, the device's endurance is tested at room temperature for more than 10^3 cycles with write voltages 2 V and -2.8 V and found that the device maintains its resistance levels (Fig. 7.8(b)). Then, the device's response to input read and write pulses are analyzed, as shown in Fig. 7.9.

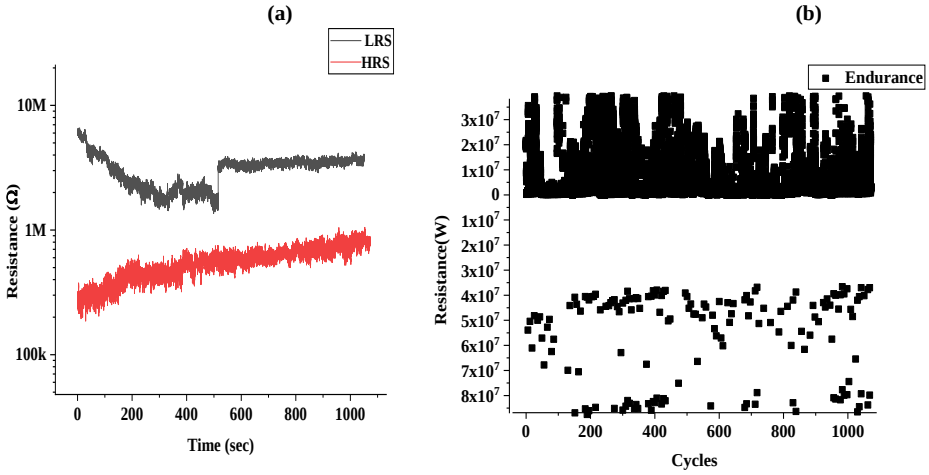


Fig. 7.8 (a) Retention characteristics obtained from a device at a read voltage of 0.25V. b) Endurance of the device with consecutive cycles of 2V and -2.8 V

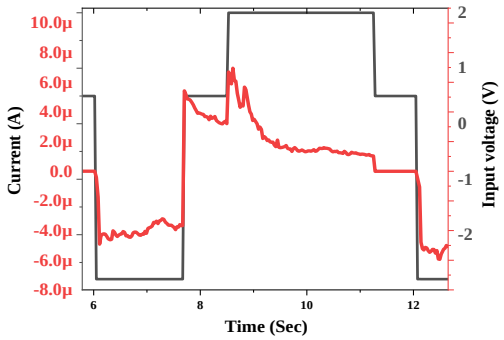


Fig. 7.9 Response of the device to pulse inputs

Consecutive write and read cycles with data '1' is written with a voltage of -2.8 V, data '0' is written with 2 V, and read voltage is 0.5 V. Thus, the pattern of input becomes -2.8 V, -0.5 V,-2 V, -0.5 V. From the output current, device read-out current measured is -5 µA.

Next, another single layer device with Au/ZnO/FTO stack is fabricated, and its electrical analysis is conducted to show that the device is more conductive. Its switching window is insignificant to decode memory states, likely due to multiple defects present at the ZnO material. Therefore, the single-layer device cannot be used as a memory device but associating the conductive layer with a more resistive Al_2O_3 layer may provide memory properties by facilitating multiple defects/ions for switching. Fig. 7.10(a) shows the voltage and current with respect to time, and the resistance plot is given in Fig. 7.10(b), in which the resistance switching can be seen, but it is insignificant compared to other devices. The corresponding current characteristics are shown in Fig. 7.10(c). Since RRAM devices with low non-linearity are prone to sneak path current formation, various solutions are available, as discussed in previous chapters. Among them, complementary switching devices are found to be a better solution to mitigate sneak path current.

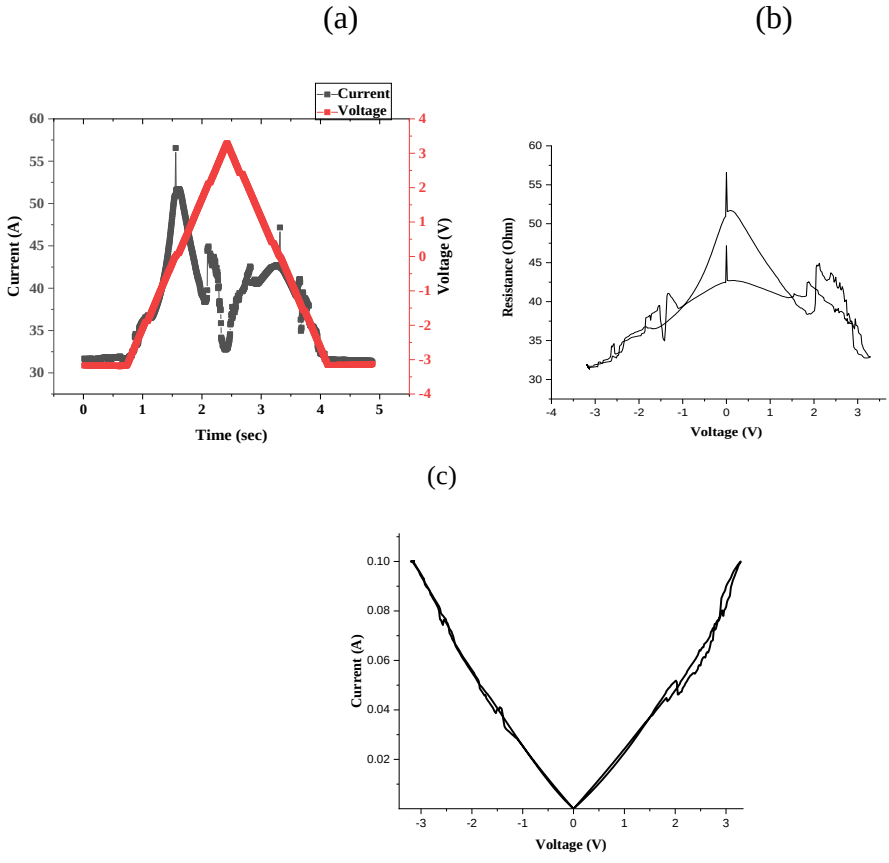


Fig. 7.10 (a) Plot of I and V with respect to time (b)Resistance across the device (c) I-V curves of Au/ZnO/FTO device

Complementary resistive switching (CRS) devices were first proposed in [28] to use in large crossbar arrays (CBA) to mitigate the sneak path current problem. The high resistance achieves the sneak current mitigation in CRS offered at the low voltage regimes and by encoding the data to different high resistance states (HRS), namely HRS/LRS, LRS/HRS. Generally, the complementary switching devices are developed with an anti-serial configuration of bipolar resistive random-access memory devices (RRAM) [190] made by metal oxides such as Ta_2O_5, HfO_2, and Nb_2O_5 [131], [132], [191], [192]. However, many drawbacks are present in such configurations like; the deposition of metal layer between the switching layers is a poor design, and the formation of multiple metal-semiconductor interfaces might cause a deviation of device characteristics from the expected ones. Instead, several single layer RRAM devices such as HfO_x [193], Cu_2O[194], and bilayer devices such as Ta_2O_5/Ta, Nb_2O_{5-x}/NbO_y, HfO_x/Al_2O_3 [28], [131], [132] also exhibit CRS characteristics, and this approach is adopted in this research work to develop CRS device.

Next, a novel bilayer Au/ZnO(10nm)/Al_2O_3(10nm)/Fluorine doped tin oxide (FTO) structure with CRS functionality was proposed that consists of two resistive switching layers such as Al_2O_3 and ZnO. The rest of this chapter focuses on the fabrication, I-V characteristics, performance of the CRS device as memory, and switching mechanism.

7.2 Fabrication and characterization of Complementary Resistive Switching device

Even though incorporating a selector device with RRAM memory is an excellent solution to mitigate sneak path current, in reality, such a configuration is not practical due to scaling issues. Since the memory technology follows the “More Moore” concept, by which the expansion of the CMOS platform is achieved by the dimensional and functional scaling. Therefore, in memory-selector configuration nodes, the scaling should be applied to both devices. However, in storage nodes, the scaling can be done up to 10 nm. Still, the selector device limits the scaling so that the complementary resistive switching devices can be accomplished as an alternative solution to sneak path current. Generally, complementary resistive switching (CRS) is developed with anti-serially connected RRAM devices; nonetheless, various disadvantages of such a design are identified. So, the following section discusses the formation of a ‘bilayer’ CRS device made using two different switching oxides stacked between metal electrodes.

7.2.1 Experiment Procedure

The Fluorinated Tin Oxide (FTO) coated glass is initially prepared to use as the bottom electrode (BE). Further, the active layers are formed with atomic layer deposition (ALD). The chamber conditions are kept the same as the previous device. Additionally, the active switching layers ZnO and Al_2O_3 were deposited with the controlled flow of precursors (Trimethylaluminum (TMA), Diethyl Zinc) and oxidizer (water). The bottom chamber temperature is set to 200 ^{0}C for Al_2O_3 and 150 ^{o}C for ZnO deposition. The growth per cycle (GPC) of Al_2O_3 and ZnO are 0.12 nm and 0.2 nm, respectively. Therefore, to deposit 10 nm of Al_2O_3, 80 ALD cycles had been run, while 10 nm of ZnO is deposited by running 56 ALD cycles. Subsequently, the Au top electrode is deposited with a thermal evaporator. In this thermal evaporation step, a shadow mask of 960 µm diameter is used through which the top electrode is deposited. The structure of the device under test (DUT) is shown in Fig. 7. 11, where TE is Au (100 nm), oxide layers are ZnO (10 nm), Al_2O_3 (10 nm), and the bottom electrode is FTO. Similarly, for comparison and optimization, various samples of different devices are prepared; among them, two devices with varying thicknesses of ZnO and Al_2O_3 are prepared, such as ZnO (10 nm)/ Al_2O_3 (20 nm) and ZnO (20 nm)/Al_2O_3 (20 nm) with the same top and bottom electrodes as in the device under test. The depositions of materials are uniform on the device structure. Fig. 7.12 (a) depicts the uniform deposition, and the gold particle size appears to be~ 200 nm, and Fig. 7.12(b) denotes the cross-section of the device showing distinct areas. However, the ZnO /Al_2O_3 layers are not distinctly seen due to their small dimension. However, in the top view of some devices, we have observed the formation of defects corroborating the formation of conduction filament. In literature, it has been reported that the conduction filament formation occurs due to percolating oxygen vacancy paths [141], [195], and the probability of formation of a conduction filament at a specific position cannot be predicted. Hence many differently shaped conduction filaments have been identified in many devices.

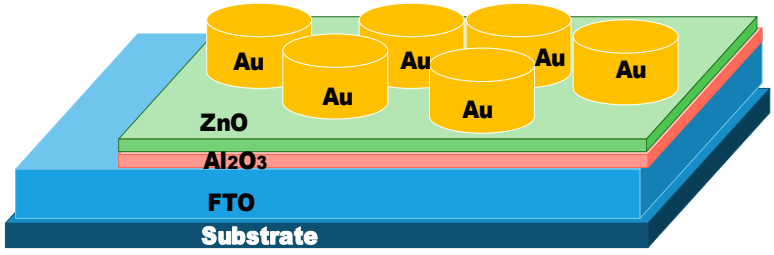


Fig. 7.11 Schematic of Au/ZnO(10nm)/Al_2O_3(10nm)/Fluorine doped tin oxide (FTO)

Fig. 7.13 depicts the example of the formation of defects in two different devices after electroforming and subsequent SET- RESET cycles. Fig. 7.13(a) shows the conduction filament (CF) formed at the center of the device, whereas in another device (Fig. 7.13 (b)), shape of the filament is different.

Besides, it is noticed that the formed area diameter is in the micrometer range. EDX associated with FESEM has been used to verify the formation of filament and elemental distribution at filament area carried out at certain areas shown in Fig. 7.13 (b). The results of EDX analysis is given in Fig. 7.14, wherein Fig. 7.14(a), elemental distribution of oxygen is shown. However, the distribution is not uniform at the given area; most oxygen atoms accumulate at the defect area, as shown in Fig. 7.13(b).

(a) (b)

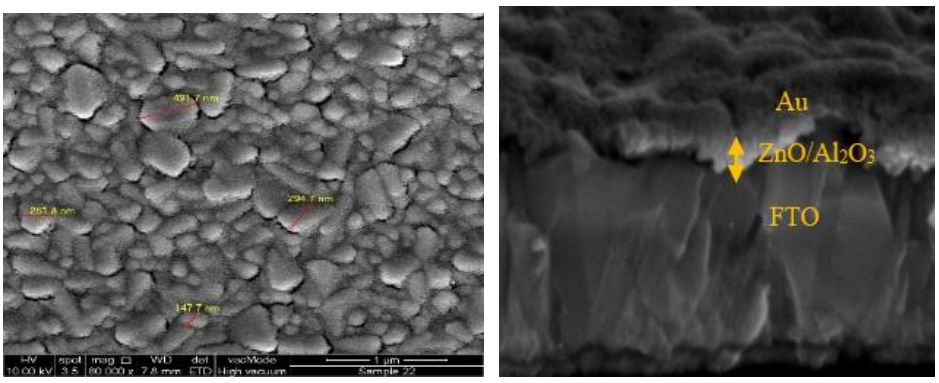


Fig. 7.12 SEM and element mapping (a)Top view of the Gold deposited device surface (b) Cross section layers obtained with a scale of 1µm.

(a) (b)

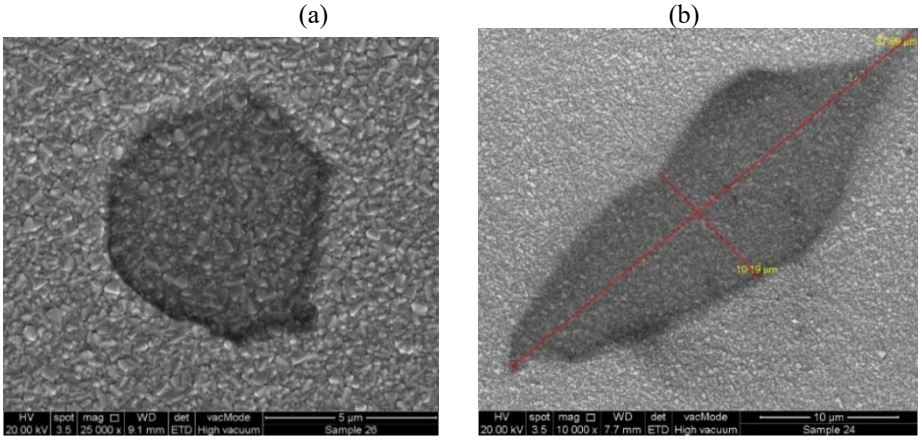


Fig. 7.13 a) top view of a device showing the defect/conduction filament formation b) Another defect/CF formation

It confirms that the oxygen vacancy-based defect (filament) formation might have occurred in this area. In the next section, I-V behavior and the device's response to pulse input are described. Further, various parameters, as well as reliability measures, are discussed. Then, the optimization of the device with different thicknesses of active switching layers is also presented. Finally, a theoretical study on the proposed bilayer device's possible switching mechanism and conduction mechanism is discussed.

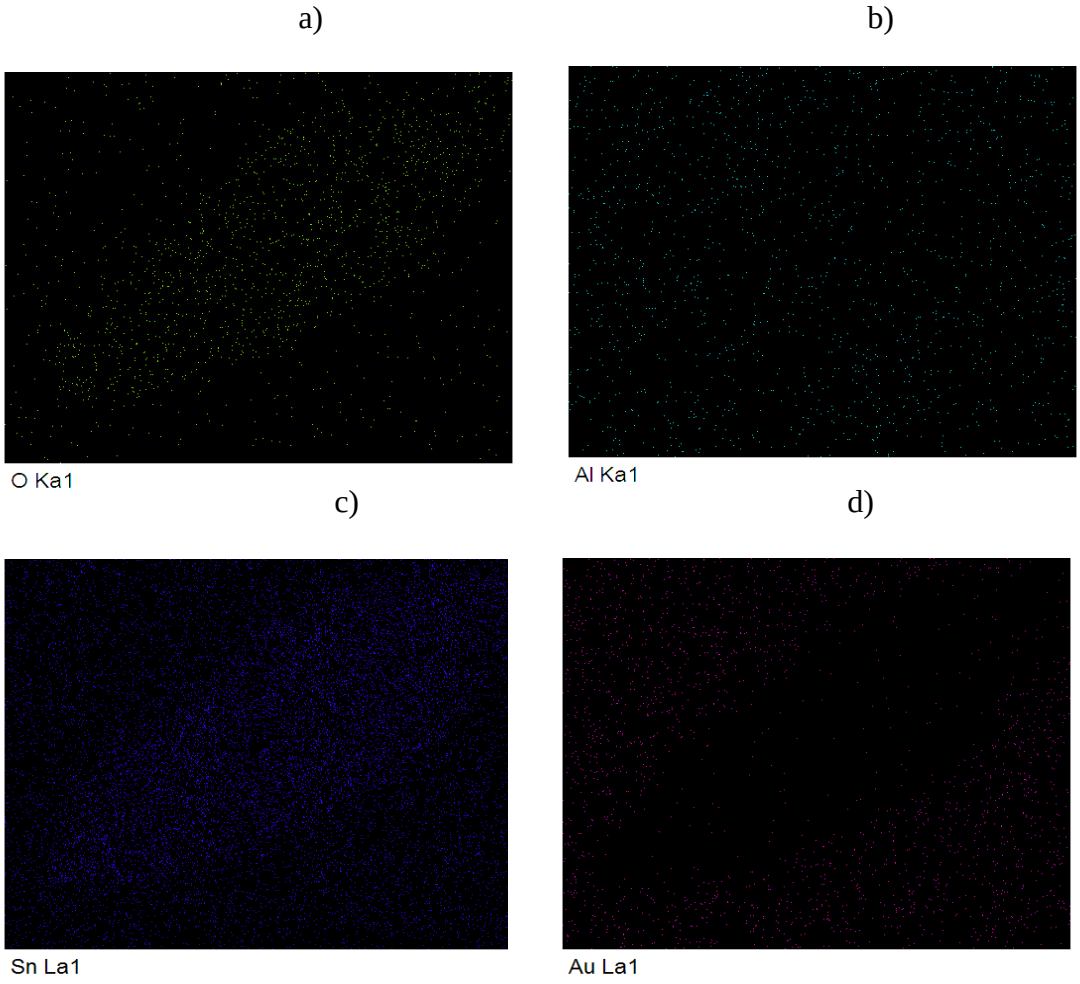


Fig. 7.14 (a) EDX analysis of the defect shown in 7.13(b) showing oxygen distribution (b) distribution of Sn from the bottom electrode (c) elemental distribution of Al (d) elemental distribution of Au. From FESEM analysis, the reactions are happening on both top and bottom interfaces to substantiate the filament formation.

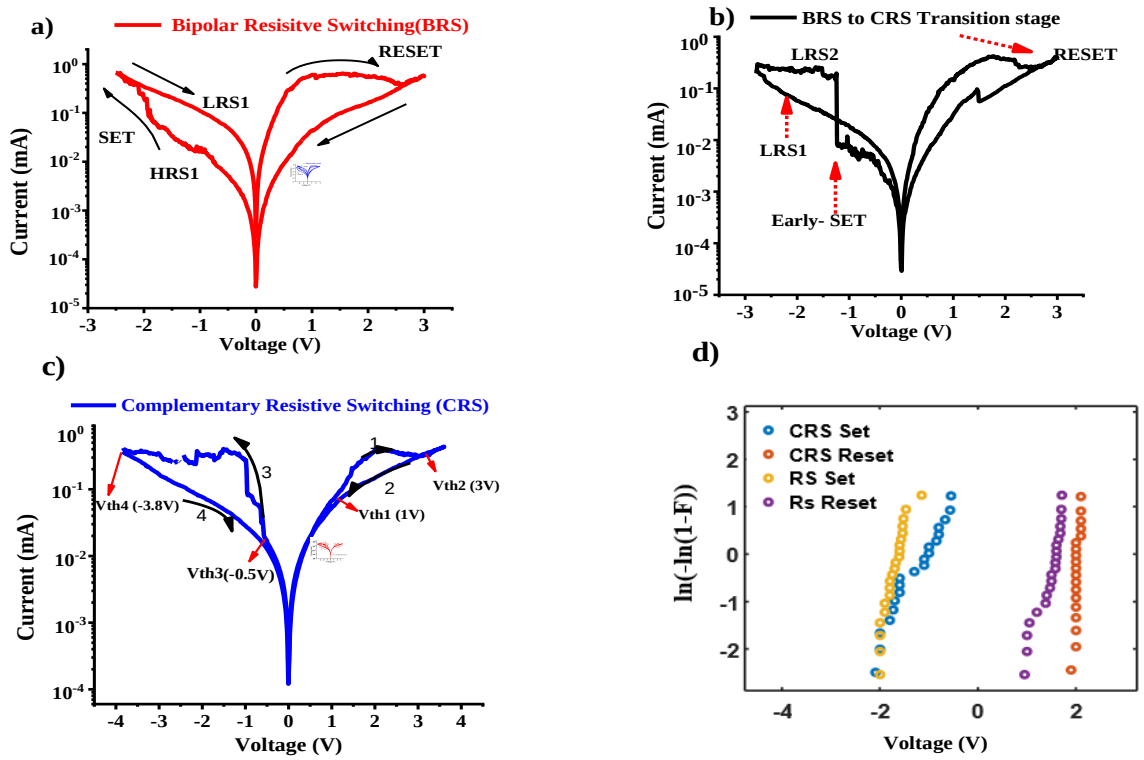


Fig. 7.15 I-V curves of Au/ZnO/Al_2O_3/FTO device demonstrating BRS, intermediate transition stage and CRS. a) Bipolar Resistive switching characteristics (inset shows multiple cycles of BRS) obtained with a DC sweep from -2.5 to 3.5 V with Ic=5 mA b) Momentary transition stage from BRS characteristics to CRS characteristics obtained with a DC sweep from -3.5 to 3.5 V with Ic=5 mA c) CRS behaviour obtained when a voltage is swept from -4.0 V to 4.0 V with Ic=5 mA (inset shows multiple cycles of CRS). Insets of (b) and (c) shown to demonstrate repeatability of the characteristics. d) Weibull distribution of the SET and RESET voltages measured during BRS and CRS

7.2.2 Electrical characterization and Results

Electroforming (EF) is the initial step carried out in the electrical characterization of most RRAM devices. Likewise, CRS devices have no exception but, in some devices, the forming process has a significant role in defining the device characteristics [193], [197], whereas in some others, the forming step has no relevance [135], [198]. In the proposed device, the electroforming has been performed at both positive and negative polarity of the input voltage with a low compliance current. However, it has been observed that forming with negative voltage showed high variability in its I-V characteristics with insignificant Roff/Ron ratio due to uneven distribution of excessive defects present in the device, whereas EF with the positive voltage provided consistent characteristics [199], therefore this work is focusing on positively formed devices and their characteristics. In the proposed device, the EF is performed

by applying a voltage sweep of 0 to 8 V at a compliance current of 100 nA. After EF, various SET/ RESET cycles are followed, and at initial cycles, the device exhibited bipolar resistive switching (BRS) behavior, then it has undergone a momentary transition before permanently changing to complementary resistive switching (CRS) behavior. The BRS characteristics are shown in Fig. 7.15(a), which occurred at a compliance current of 5 mA with continuous input sweep from -2.5 V to 3 V at a stepping voltage of 0.01 V, which results in an average value of SET and RESET voltages, -1.73 V and 1.5 V respectively. Besides, the maximum device current in BRS is limited by the self-compliance feature of the device; the maximum current measured is 500 µA. In Fig. 7.15(a), the low resistance state (LRS) of BRS characteristics is indicated as LRS1, and the high resistance state (HRS) is marked as HRS1. However, after a few cycles (~12), the device exhibited a transition from BRS behavior as in Fig. 7.15(b), where the SET current of the intermediate stage is increased beyond the SET current achieved with BRS(LRS1), which is marked as early-SET in Fig. 7.15(b), and the new low resistance state is marked as LRS2. After that, the device started exhibiting CRS behavior as plotted in Fig. 7.15(c), which is irreversible since the device never drives back to the initial BRS as the state transition from LRS1 to LRS2 has made a permanent change in the device. The transition from BRS to CRS characteristics is reported in several devices. A few devices exhibit transition while modulating the SET compliance current [190], whereas others show transition while extending the input SET sweep voltage [132], [200].

In our study, a steady compliance current (Ic) has been applied to the device throughout the characterization, and the transition is observed while extending the input sweep voltage from -2.5 to -2.8 V with a variation in stepping voltage from 0.011 V to 0.0116 V. This transition in BRS to CRS characteristics is owing to the change in characteristics of the conduction filament (CF) [133], [190], [201].

The CRS characteristics are given in Fig. 7.15(c) can be examined with four threshold voltages: Vth1, Vth2, Vth3, and Vth4. At threshold voltages Vth1 and Vth3, the device enters to completely ON-state with both active layers switch into LRS state, whereas during Vth2 and Vth4, the device transit to one of the two high resistance states, i.e., state-0 (LRS/HRS) or state-1 (HRS/LRS). In CRS devices, the data is stored in one of the high resistance states with read voltage defined between a range of voltages limited by the threshold voltages |Vth1-Vth2| or |Vth2-Vth3|. For the proposed device, the read window is measured as ~1.8 V.

From multiple cycles of BRS and CRS, as shown in insets of Fig. 7.15(a) and 7.15(c), it has been noticed that a shift is occurred in the SET and RESET voltages of the device when its characteristics permanently changed from BRS to CRS. The statistical distribution of this voltage shift is analyzed using the Weibull distribution that is plotted in Fig. 7.15(d), where CRS SET means the SET process occurred at a threshold voltage Vth3 and CRS RESET means the RESET occurs with threshold Vth2. The self-compliance feature is desirable for a RRAM device by that the maximum current in the device is limited by the internal mechanism within the device irrespective of external compliance set to avoid the over conduction of the device.

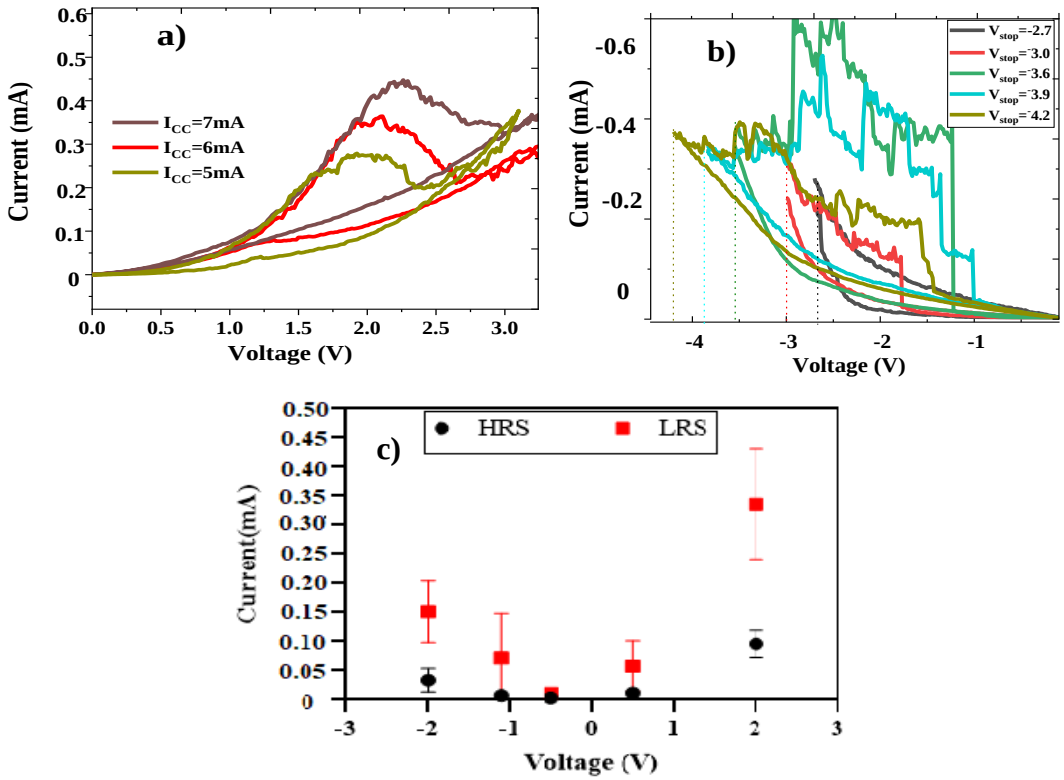


Fig. 7.16 (a) Device characteristics measured under the various current compliance values (b) current at different stop voltages (c) mean and error plot of current during HRS and LRS during multiple cycles of BRS, intermediate and CRS states at -2 V, -1.1 V,-0.5 V, 0.5 V, and 2 V.

Even though the proposed CRS device exhibits self-compliance, the device characteristics obtained with different external current compliance levels are given in Fig. 7.16(a).

In Fig. 7.16(a), the device current at LRS and HRS increases with an increase in compliance current that can be described as the change in the properties of the conduction filament such as diameter or number of oxygen vacancies with increased external compliance

current. Similarly, an analysis based on the stop voltage is also carried out as given in Fig. 7.16(b), showing that at Vstop of -2.7V, the device switched to SET state as part of BRS. As the stop voltage extends further (beyond 2.7V), the device exhibited both SET and RESET switching as part of CRS. The initial resistance of the device at low voltages (from 0 to -1.5V) is slightly decreasing with an increase in stop voltage. However, the LRS shows variations irrespective of the stop voltages. Fig. 7.16(c) plots the mean error in the measured current value at various voltages during multiple cycles, revealing that current at HRS and LRS are distinguishable beyond 1.5V irrespective of the applied input polarity.

7.2.3 Performing read and write with pulse input

The device's response to pulse input is tested with various pulse trains. We observed that the RESET transition occurs from 2 V to 3 V during the positive polarity of input voltage and ~ -2.4 V to -3.8 V during the negative polarity of the input. Therefore, based on the write scheme given in [202], the write voltage can be selected from within the above-given ranges. The write voltages chosen for the particular device are -2.5 V, 2.1 V, and read voltage set as 1.3 V.

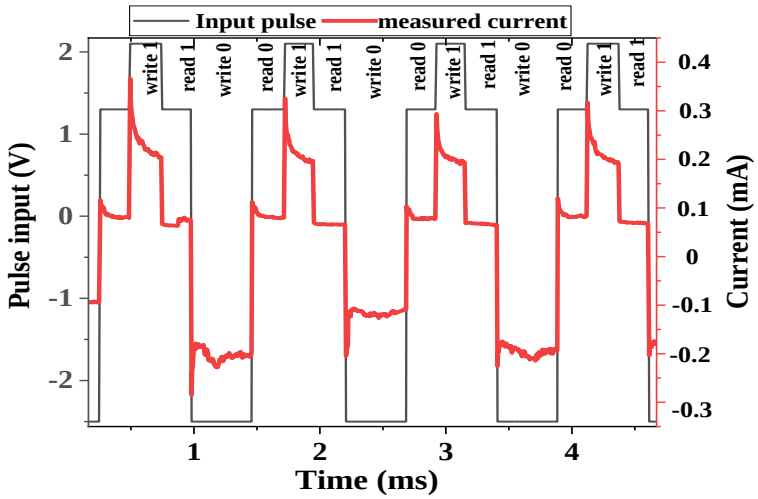


Fig. 7.17 The device's response to pulse input (solid red line) indicates measured device current, and the thin black line represents the input pulse of amplitudes 2.1 V, -2.5 V as write voltage, and 1.3 V as reading voltage.

Further, to demonstrate the write/read processes, the device is subjected to several read/write pulses. Among them, three consecutive cycles of write and read are shown in Fig. 7.17 where alternate processes run to perform write-1, read-1, followed by write-0 and read-0.

The multiple consecutive read scenarios have not been considered in this study. From Fig. 7.17, we detected that read current obtained while reading data bits 1 and 0 are distinguishable with ~ 60µA difference, also termed readout current. Similarly, write-1 and write-0 are showing the current values of 300 µA and 200 µA, respectively. Thus, the device is operating under low magnitudes of write voltage (< |3| V), and current (in µA) enables it to use in medium power (µW) memory applications. Moreover, the PD measured in response to pulse input while writing is observed as ~450 µA as portrayed in Fig. 7.18(a). Similarly, reading the data bits '1' and '0' require a PD of 130 and 65 µW, respectively as shown in Fig. 7.18(a).

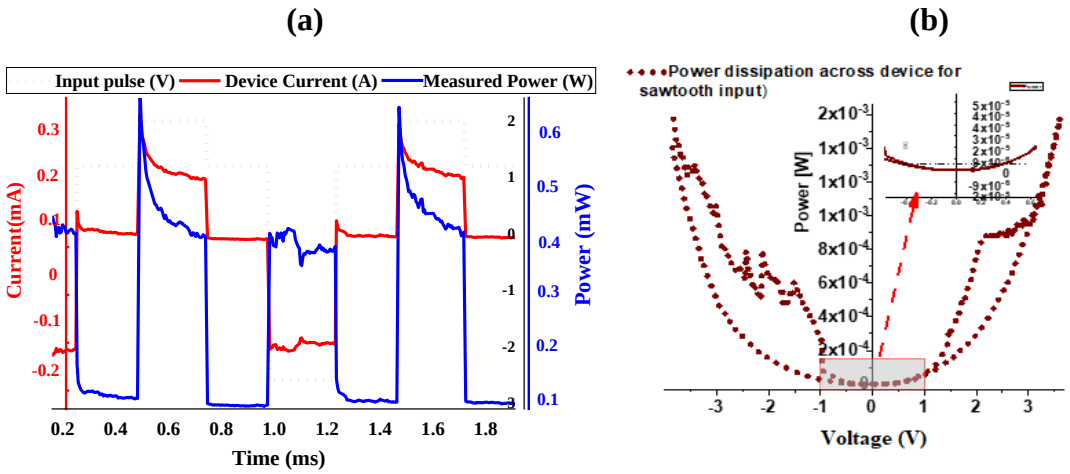


Fig. 7.18 a) Power dissipation across the device (solid red line) while performing read and write operation with pulses. b) Power dissipation across the device on response to sawtooth input

However, as expected, the power dissipation during the read process is comparatively lower than that of data write, which signifies the use of the device in medium power memory applications. The power dissipation (PD) across the device in response to a sweep of a sawtooth waveform (Fig. 7.18 (b)) reveals that PD is zero at lower voltages describing the possibility of sneak path current reduction.

The device's response to pulse / DC inputs indicates that the device can be used in CBA to mitigate sneak path current owing to low off-current of ~$3x10^{-7}$ A present at low input voltage ≤|0.5| V, which effectively blocks the possible leakage current originating from the memory array. Therefore, when connecting the device in a cross-bar array, read bias voltage (Vread/2) applied to unselected cells in the array can be ≤|0.5| V, read margin of selected cell

(Vread) can be in the range of ~1.0 V to 1.8 V, and the nonlinearity factor (I(Vread)/I(Vread/2)) measured for this device is ~11.

Next, the device's switching time and reliability studies are given in Fig. 7.19 and 7.20, respectively. In Fig. 7.19(a), the device displays SET and RESET switching at both positive and negative polarities of DC sweep voltage. The SET process at negative polarity is abrupt, which occurs in 20 µs, whereas the SET switching at positive bias is gradual and happens at 0.30 ms as marked in Fig. 7.19(b). However, the device shows a microsecond switching time when performing read and write with pulse input. While reading the data, the read current increases to a maximum value in 5 µs of the read pulse as given in Fig. 7.19(b), while writing to the device responds in 8 µs as shown in Fig. 7.19(c). Fig. 7.20(a) illustrates the device's endurance for multiple cycles, and Fig. 7.20(b) demonstrates the device retention capability when performing multiple read at 1.3 V, at room temperature.

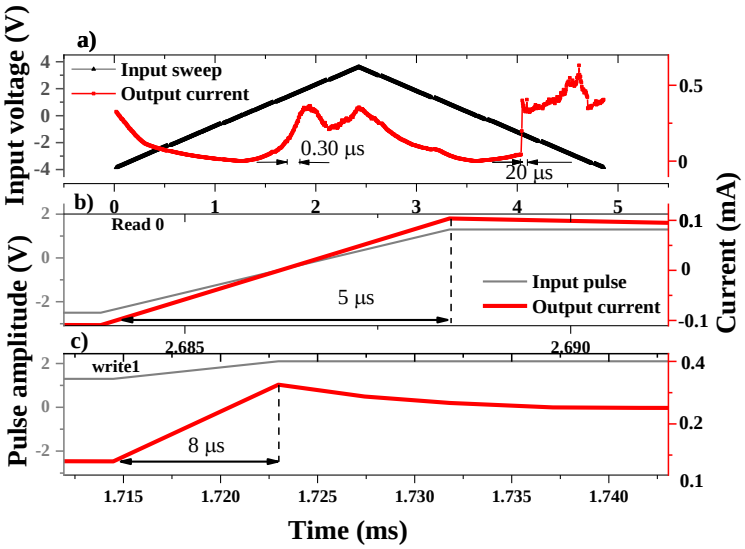


Fig. 7.19 Switching time response of the device(a) with DC sweep input (b) switching time when reading with pulse input (c) switching time while writing with pulse input

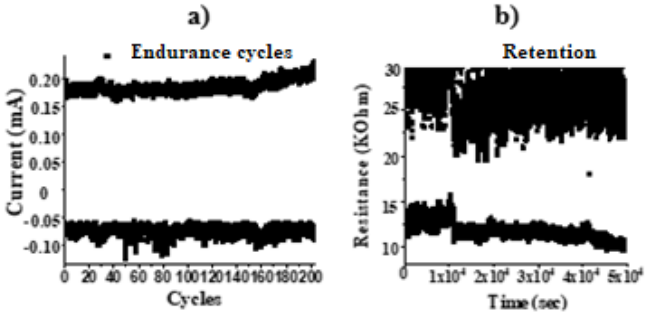


Fig. 7.20 (a) Endurance of the device with multiple cycles (b) Retention of states measured at read voltage of 1.3 V

7.2.4 Optimization with different active layer thickness

With a focus to optimize the device performance, three different sets of samples with different active layer thicknesses are tested and resulting CRS characteristics obtained for these devices are represented in Fig. 7.21 (a), (b), and (c). While comparing, it could be observed that the off current in devices with 10 nm active layer is higher than that of the devices with 30 nm and 40 nm active layer thickness.

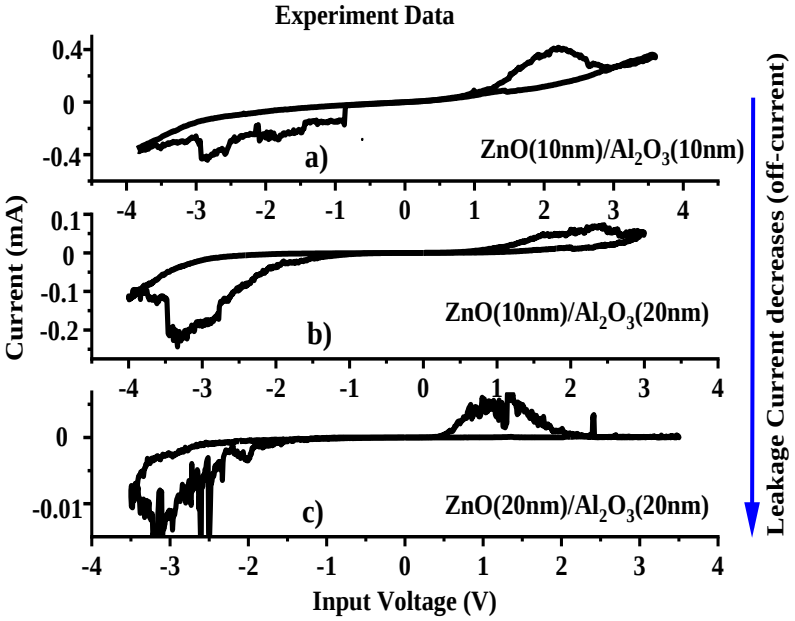


Fig. 7.21. Optimization of CRS design with varying active switching layer thickness a) device with ZnO(10nm)/Al_2O_3(10nm) structure b) device with ZnO(10nm)/Al_2O_3(20nm) structure c) ZnO(20nm)/Al_2O_3(20nm) structure, demonstrating the decrease in leakage current with increase in active layer thickness.

Moreover, the leakage current is found to be decreasing with an increase in active layer thickness. Likewise, the devices with thicker oxide show a better on-off ratio. A better Roff/Ron ratio could be obtained with the ZnO(20nm)/Al_2O_3(20nm) stack. The theoretical approach on the possible mechanism of CRS switching as well as current conduction in the bilayer device has also been described in the following section.

7.2.5 Possible Mechanism of forming and switching in CRS device

Generally, the switching process in RRAM devices can be explained based on the formation of conduction filament. As discussed in chapter 2, two major mechanisms are associated with filament formation are; valance change mechanism (VCM) [134] and

Electrochemical metallization mechanism (ECM) based switching. As the electrodes used in the proposed device are inert (Au and FTO) [182], [203], [204], and the active layers are well-known oxides switching with oxygen vacancies, the possibility of ECM-based switching is eliminated. Similarly, in our study, the influence of protons or moisture on switching is not considered [205]. From various experiments conducted, it has been interpreted that the establishment of filament in the proposed device is based on oxygen vacancies. In addition, the results of elemental distributions obtained from the structural analysis also reveals that the filament is formed of Oxygen vacancies. However, the effect of interface charges at metal/oxide interface may also be contributing for the switching process. From the analysis it is clear that the metallic cations seldom participate in switching process. Therefore, the device is likely to be falling under the category of VCM [206].

In the single-layer device (Au/Al_2O_3/FTO), and (Au/ZnO/FTO) as discussed in the previous section of this chapter, we have observed that the ZnO layer is more conductive due to the presence of excessive defects, and that might leads to the degradation of device performance [182]. Hence, the as-deposited device had been subjected to EF with a positive sweep, which in turn limit the number of defects in the layer, and the possible switching mechanism can be explained with the migration of positively charged defects to the bottom of the ZnO layer, leaving a depletion layer at the top interface. However, further increase in voltage causes the presence of maximum electric field at that region, which results in the formation of oxygen ions and may further limit the number of oxygen vacancies in the ZnO layer to form uniform or constant distribution of oxygen vacancies the device [199].

Subsequent initial SET/RESET cycling at higher compliance current results in the formation and rupture of filament at the ZnO layer. That too can be obtained with negative and positive polarity of the input voltage, respectively. In this case, rupture of conduction filament occurs when performing the RESET switching at a higher external compliance current and the possible mechanism is associated with Joule heating [134], [199].

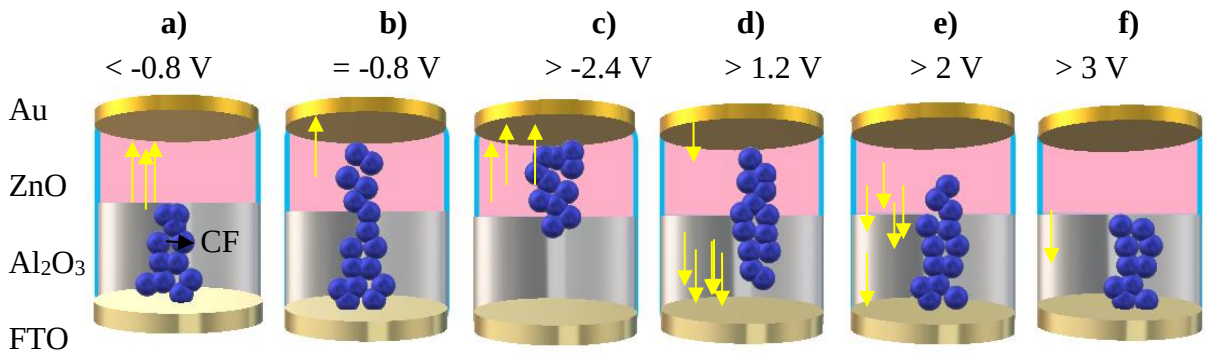


Fig. 7.22 Mechanism of switching in CRS: the golden color top plane represents the Au top electrode, underlying light color denotes the ZnO layer below that, the silver color represents Al_2O_3 layer, and the plane at the bottom is FTO electrode. Blue color circles represent oxygen vacancy-based conduction filament, and yellow arrows denoted the direction of vacancy movement. a)Initial state HRS/LRS b) complete filament representing LRS/LRS or ON-state c)LRS/HRS state d) LRS/LRS (ON-state) e)Oxygen vacancy drift towards bottom electrode to settle HRS/LRS f) device reached back to initial state f (or a).

Further, the transition from BRS to CRS occurs due to the second electroforming process at the Al_2O_3 layer with the modulation of input voltage at a higher compliance current [134]. In this study, the mechanism of CRS in ZnO/ Al_2O_3 bilayer structure is explained with the concept of redistribution [132], [135] of oxygen vacancies within ZnO and Al_2O_3 layers.

The switching process that occurs at CRS is explained in Fig. 7.22, where at input voltages <-0.8 V, the device is at HRS with filament-free ZnO layer and presence of oxygen vacancy filament at Al_2O_3 (LRS) layer. Thus, the resistance state of the device becomes HRS/LRS or state-1 as indicated in Fig. 7.22(a). Then, as the input sweep reaches -0.8 V, the oxygen vacancies migrate toward the top electrode to form filament in the ZnO layer [204], thereby the device enters to LRS/LRS state or completely ON-state as shown in Fig. 7.22(b). On further increase in voltage beyond -2.4 V causes more oxygen vacancies to migrate towards the top electrode resulting in the rupture of filament from the bottom electrode interface. As a result, the lower Al_2O_3 layer becomes depleted, as shown in Fig, 7.22(c), where the device state changes to LRS/HRS state or state-0 [203].

Next, a sweepback of the input signal causes the device to remain in the current state-0 until the applied input voltage reaches ~1.2 V of the positive cycle. Subsequently, when a positive input voltage of 1.2 V is applied to the top electrode, an electric field set up across the device, through most of the field appears across depleted resistive Al_2O_3 layer, and the more

concentrated electric field appears at the tip of the conduction filament than at the top flat interface [207].

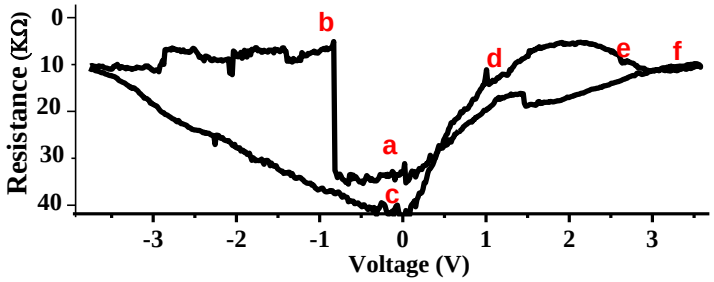


Fig. 7.23 Device resistance marking a, b, c, d, e, and f are corresponding to the mechanism marked in Fig 7.19. (linear scale)

As a result, instead of rupturing the conduction filament from the top electrode interface, oxygen vacancies present at ZnO/ Al_2O_3 interface drift towards the bottom electrode and eventually forms a filament spanning across Al_2O_3 and ZnO layer as demonstrated with Fig. 7.22(d), where the arrows show the dominance of the electric field at bottom electrode interface than at the top interface and the corresponding current state achieved by the device becomes LRS/LRS. On further increase in positive voltage causes oxygen vacancies to get detached from the top electrode and upper part of the filament breaks to attain HRS/LRS state as shown in Fig. 7.22(e) and eventually to reach the final stage shown in Fig. 7.22(f) which is the same as initial state given in Fig. 7.22(a). The mechanism illustrated in Fig. 7.22 is correlated with the resistance developed across the device as shown in Fig. 7.22, described with six points a, b, c, d, e, and f. In Fig. 7.23, the device's initial state achieved with the negative polarity of input voltage is HRS/LRS or state-0 (marked as a in Fig. 7.23) with the resistance value ~32 KΩ. As the magnitude of input voltage increases further, the device switch to ON-state (as marked as b in Fig. 23) with its resistance as low as 10 KΩ. Subsequently, when the input sweep reaches -2.4 V, the device switches to a higher resistance state of approximately 42 KΩ i.e., state-1 (marked as c in Fig. 7.23). During the positive voltage sweep, the current through the filament increases and finally settles at a resistance of approximately 32 KΩ as marked with f in Fig. 7.23 after going through completely ON-state (marked as d, e in Fig. 7.23). From the figure, it is noteworthy that the resistance at points a (state-0) and c (state-1) are distinguishable with an approximate difference between them is 10 KΩ which indicates that the HRS arise due to the rupture of filament in ZnO and Al_2O_3 layers, respectively as indicated in Fig. 7.22(a) and (c).

Next, the current conduction mechanism associated with the device is illustrated with the help of experimental data and fitting models. The I-V characteristics re-plotted on the logI-logV scales to analyze the conduction mechanism, as shown in Fig. 7.24. The negative voltages are converted into absolute values for plotting the data and then converted to log scale. The voltages and currents are not normalized during the experiment. As shown in Fig. 7.24, at HRS (for both positive and negative polarities), the ZnO/Al_2O_3 bilayer device is due to trapping controlled-space charge limited conduction (TC-SCLC) [208].

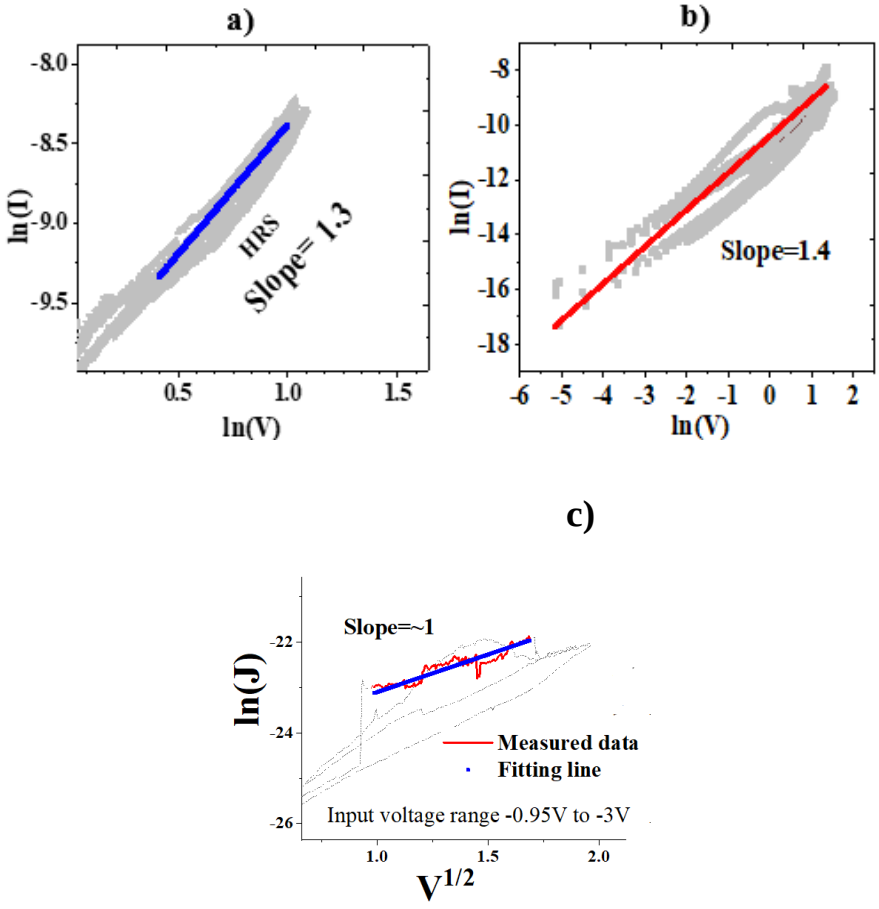


Fig. 7.24 Current conduction mechanisms a) ln(I) vs. ln(V) indicates SCLC conduction with slope=1.3 at HRS attained with the negative polarity of input b) ln(I) vs. ln(V) indicates SCLC conduction with slope=1.4 at HRS obtained with positive polarity(c) lnJ Vs $V^{1/2}$ plot showing the Schottky conduction at LRS.

Similarly, at LRS (positive polarity), the relationship between ln (I) and $V^{1/2}$ depict that the current conduction (Fig. 7.23(c)) at Au/ZnO interface is due to Schottky conduction [190], which is also consistent with the conduction mechanism reported for ZnO based switching

memories. Thus, it is reported that both devices are useful to use in crossbar array to eliminate sneak path current.

In conclusion, the chapter presents two novel resistive switching devices with structures Au/ZnO/Al_2O_3 /FTO and Au/ Al_2O_3/FTO, respectively. The former has shown high asymmetry in its characteristics with an interesting phenomenon of non-zero crossover, pointing to its application in memcapacitive and inductive applications as reported in the literature. Also, the 1D1R kind of characteristics makes it a better solution to mitigate sneak path current, without using any external device (selector). In contrast, the latter gives a potential solution to mitigate sneak path current by exhibiting a complementary resistive switching behavior. The oxygen vacancy-based switching mechanism in CRS is demonstrated, and it is reported that the dominant current conduction mechanism in CRS devices is SCLC. Further, the optimization of device characteristics is achieved by testing with different devices of varying active layer thickness and found that the devices with thicker active layer provide low leakage current. Further,the device's response to pulse / DC inputs indicates that the device can be used in CBA to mitigate sneak path current owing to low off-current of ~$3x10^{-7}$ A present at low input voltage ≤|0.5| V, which effectively blocks the possible leakage current originating from the memory array.

Chapter 8

Characterization of multilevel CBRAM and RRAM devices for the implementation of hypothetical 1S1R architecture to mitigate sneak path current

Chapter Summary

Two resistive switching devices are proposed in this chapter to use in association with the selector. The first part of the chapter reports a conductive bridge RRAM(CBRAM) with multi-level resistive switching property. The structure of the device is Ag/Al_2O_3 (10 nm)/ZnO(5 nm)/FTO device, which exhibits five discrete states; LRS, IRS1, IRS2, IRS3, and HRS, prevailing at certain fixed voltage levels. The switching mechanism in the device is identified as the formation/ rupture of multiple filaments due to REDOX reactions. The conduction mechanism at LRS is due to metallic/ohmic conduction substantiating the formation of metallic filament. Similarly, SCLC is the current conduction mechanism that occurs during the HRS of the device. Moreover, the device exhibits a better Roff/Ron ratio for HRS/LRS and HRS/intermediate states. A RRAM device is proposed with Au/ Al2O3/ZnO/FTO structure in the second part. The device exhibited bipolar resistive switching characteristics with excellent retention and endurance properties (>10^3) and a Roff to Ron ratio of 200. Further, both CBRAM and RRAM are connected with a Pt/Ta_2O_5/TaO_x/TiO_2 /Pt selector hypothetically. The obtained I-V characteristics show that the former can provide multilevel 1S1R in high-density applications, whereas the latter provides bipolar characteristics. Also, it is reported that both devices offered a very low OFF-current in the order of nano Amperes with a high non-linearity and Roff/Ron ratio.

Related Publications

1. Jagath Arya Lekshmi, T. Nandha Kumar, K.B. Jinesh," Multilevel non-volatile memory based on Al_2O_3/ZnO bilayer device," IET Micro & Nano Letters, pp. 1–5 doi: 10.1049/mnl.2020.0335.

2. Arya Lekshmi, T. N. Kumar, K.B Jinesh," Self-limited Bipolar Au/ Al2O3/ZnO/FTO RRAM and its comparison with Ag/ Al2O3/ZnO/FTO devices", Elsevier's Microelectronic Engineering, Volume 250,2021,111637,ISSN 0167-9317,https://doi.org/10.1016/j.mee.2021.111637.

In this chapter, two variants of resistive switching devices such as CBRAM ($Ag/Al_2O_3/ZnO/FTO$) and RRAM (Au/Al2O3/ZnO/FTO) are fabricated and characterized. They are further combined with a $Pt/Ta_2O_5/TaO_x/TiO_2$ /Pt selector device hypothetically to form 1S1R structure, which is one of the promising architectures to mitigate sneak path current.

Even though Al_2O_3 is an insulator, in our experiment, we deposited Al_2O_3 ALD with sequential exposures of $Al(CH_3)_3$ and O_3, where water is acted as oxidizer. However, during the deposition, it is certain that dangling bonds and native defects form within the structure may cause the formation of energy states within the band gap to facilitate the current conduction, thereby it functions as a RRAM device showing conductance, thereby the term semiconducting denotes its conductance nature. The role/behaviour of the Al_2O_3 layer is equivalent to the Ta_2O_5 layer in $Pt/Ta_2O_5/TaO_x/Pt$ RRAM model (which we have used in chapter 4) due to the presence of defects in both material.

The first part of the chapter describes the fabrication and characterization of a CBRAM device based on $Ag/Al_2O_3/ZnO/FTO$ structure and reports its multilevel functionality. Further, to implement the one selector-one resistor (1S1R) architecture, the proposed device has been connected with a selector device hypothetically to analyze its I-V characteristics, to ensure that the combined devices can reduce sneak path current along with providing multiple bit storage enabled by the multilevel capability. Further, the second part of the chapter discusses the implementation of $Au/Al_2O_3/ZnO/FTO$ RRAM structure. It demonstrates the combined characteristics with selector (1S1R) that enhance the performance in crossbar array by eliminating sneak path current.

8.1 Fabrication/characterization of $Ag/Al_2O_3/ZnO/FTO$ CBRAM device and 1S1R formation

The most accepted theory to fit with the switching mechanism of resistive memories is conduction filament (CF), either with oxygen vacancies or metallic ions. Conductive bridge random-access memory (CB-RAM) [6], [27], [42]–[46]cells are made with switching layer stack sandwiched between two electrodes where at least one of the electrodes would be reactive to facilitate the cations to participate in switching. For example, active metals like Silver (Ag), or Copper (Cu) is used as top electrodes in CBRAM devices [37], [59], [209]. Interestingly, several CBRAM devices exhibited multilevel-cell (MLC) capability, which can be utilized in high-density memory applications [40], [41] with $4F^2$ memory cells where F is the minimum

feature size. MLC is becoming an emerging field as it has applications in neuromorphic computing, LUT implementation in FPGA, etc.

However, it has been observed that CBRAM devices are prone to exhibit multilevel capability than the VCM devices due to the high possibility of formation of multiple metallic as well as vacancy-rich filaments. CBRAM devices exhibiting the MLC characteristics are TiN/HfO_x /Al/Pt [210], Ni/TiO_2/HfO_2/Ni [211], Al/CeOx/Pt [212], and VCM device such as TaO_x based RRAM [213].

To achieve multilevel functionality, a novel device is proposed with an active Silver electrode as the top electrode. The following section of the chapter reports the fabrication and study of multilevel characteristics of bipolar CBRAM device made of Ag/Al_2O_3 (10 nm)/ZnO(5nm)/FTO bilayer structure for the first time, followed by an analysis of the conduction mechanism and the switching mechanism of the proposed device. The end of the subsection discusses the cycle-to-cycle (C2C) variability and device-to-device (D2D) variability studied across multiple devices.

8.1.1. Experiment Procedure:

The proposed device is Ag/ Al_2O_3 (10 nm)/ZnO (5 nm)/FTO with FTO as the bottom electrode and Silver (Ag) as the top electrode (TE). TE is prepared by thermal evaporation, and at that stage, the devices in the sample are confined by using a shadow mask with via holes of 960 µm diameter. For the experiment, multiple samples are fabricated to analyze multiple devices behavior. The layers below TE are Al_2O_3 and ZnO oxide layers deposited using atomic layer deposition (ALD) technology and their thicknesses are 10 and 5 nm, respectively. Both layers are deposited using ALD cycles where precursor, oxidizer (H_2O), and purge gas (N_2) were exposed to the bottom electrode material (FTO) in sequence. Precursors used to form Al_2O_3 and ZnO are TMA, diethyl zinc, respectively. The deposition temperature, pressure, and environmental conditions are the same as that of the devices discussed in the previous chapter. To deposit 10 nm of Al_2O_3, 80 ALD cycles had been run, whereas to deposit 5 nm of ZnO, 25 ALD cycles were run [214]. Fig. 8.1 represents the layout of the device depicting each layer where the top electrode (TE) is Silver (Ag) with a thickness of 100 nm, and oxide layers are; ZnO (5 nm) and Al_2O_3(10 nm).

Electrical characterization of the device is done at room temperature at a dark chamber using an Agilent B2912A precision source measure unit. During the electrical characterization,

the bottom electrode FTO is grounded, and the input voltage is applied to the top Ag electrode. Surface morphology obtained from the structural analysis shows that the material deposition was uniform, as in Fig. 8.2 (a)showing the uniform deposition of Silver at the device area, and Fig. 8.2(b) depicts underlying Al_2O_3/ZnO layers without top electrode deposition. In this proposed device, the presence of the ZnO layer acts as a tunneling layer that limits the leakage current. In contrast, a similar configuration of the device with Au top electrode (Au/Al_2O_3/ZnO/FTO) behaves as ox-RRAM due to the difference in the reactivity of the electrodes chosen.

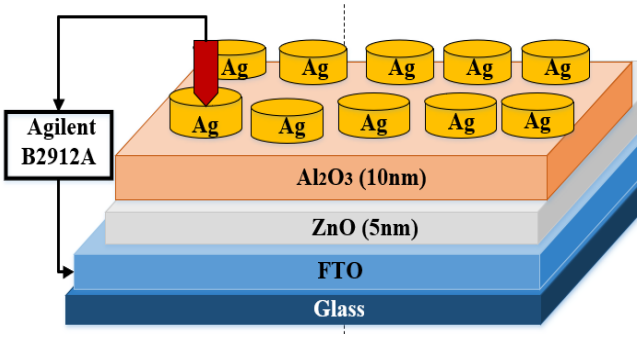


Fig. 8.1 Structure of the proposed device with Al_2O_3, ZnO active layers with Ag top electrode and FTO bottom electrode.

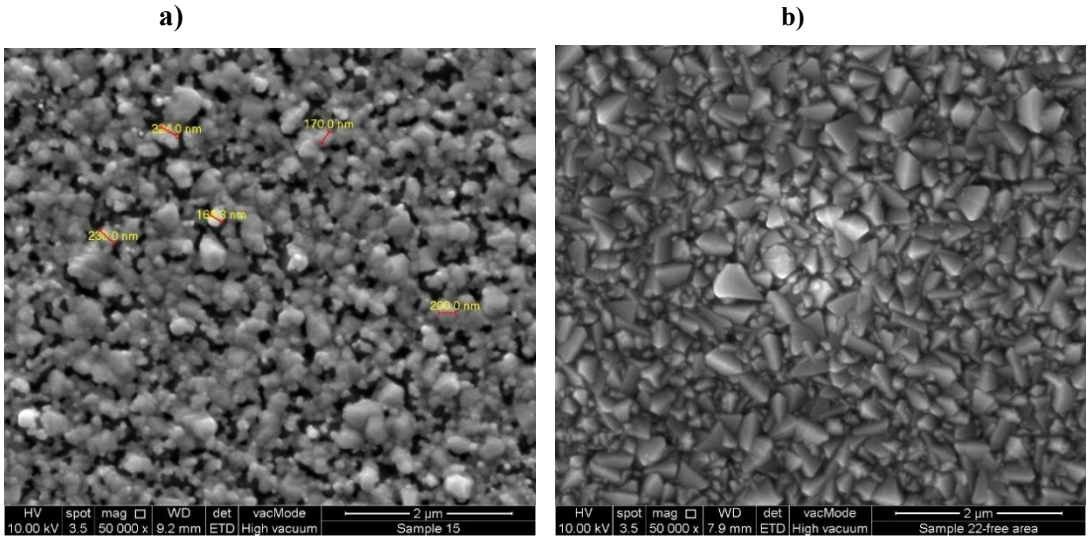


Fig. 8.2 FESEM image showing the uniform distribution of (a) Silver top electrode deposition (b) Underlaying Al_2O_3/ZnO layers (both at 2µm magnification) device-free area without Ag

8.1.2. Results and Discussions:

Initially, an electroforming step is carried out in the device at a high input voltage sweep with external compliance of 100 nA. Then, a DC input sweep of -4 V to 2 V in steps of 0.01 V is applied to the device at a compliance current of 0.1 A; in the response, the device showed self-compliance multilevel resistive switching characteristics with SET and RESET switching achieved at the positive and negative polarity of input voltage as shown in Fig. 8.3. However, while transiting from LRS to HRS, the device exhibited two distinct intermediate memory levels with an abrupt transition between them whereas, during the transition from HRS to LRS, the device exhibited one intermediate memory state in addition to LRS

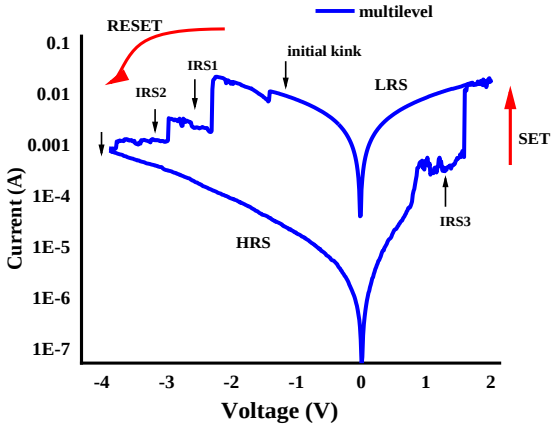


Fig. 8.3 I-V characteristics obtained with the proposed device showing five distinct resistive switching levels

with the maximum current is limited by the self-compliance feature of the device[19]. The maximum current in the multilevel device at LRS is measured as 15.80 mA. Then, the response of the device to DC sweep signal is studied. Its I-V characteristics are given in Fig. 8.3, which is marked up with five distinct resistance levels obtained with the entire span of sweep from -4 V to 2 V. In Fig. 8.3, the initial kink is observed. In contrast, the device resets initially at a potential of -1.4 V. At this point, even though there was a 60 Ω upsurge in resistance value than the LRS, it is insignificant to encode data bits. Therefore, the initial kink is not considered a stable state, which might be due to the rupture of an unstable filament.

When the input voltage is increased further up to -2.3 V, the first stable intermediate state (IRS1) is achieved, which showed a resistance of 1300 Ω, as shown in Fig. 8.4(a). Then, a rise in reset voltage to -3.0 V resulted in resistive switching of the device to another intermediate resistance level (IRS2) of resistance 2470 Ω, and this resistance state persists for an input voltage ranging from -3.0 to -3.7 V. Finally, the device turned off at -3.8 V after the

transition from IRS2 reaching the HRS of resistance 4320 Ω. Subsequently, a sweep of positive voltage is applied to the device, and at 0.8 V, it has driven to an intermediate SET state of resistance ~3000 Ω as marked in Fig. 8.4(b). At this stage, the device showed trivial changes in resistance values, though compared to the resistance value of LRS, these variations are insignificant. Hence, it is considered the first stable state attained with SET voltage; thereby, it is termed the third intermediate state (IRS3). On further increase in the input voltage beyond 1.7 V causes the device to switch to LRS which has a resistance value of 100 Ω. However, it has been interpreted that the LRS and IRS3 states can be achieved by controlling the SET compliance current [215]. Next, the Roff/Ron ratio of the proposed multi-level memory has been calculated as a measure to analyze the device performance. In this case, in addition to the LRS/HRS ratio, Roff/Ron ratio has been calculated for each intermediate state by taking the ratio of resistance at the intermediate state to HRS. Primarily, the LRS /HRS ratio of the device is measured at -1.4 V is 354. The ratio obtained for IRS1 at -2.38 V is 15, the ratio measured at IRS2 state shows a factor 4. Similarly, Roff/Ron ratio is also accessed for the stable state (IRS3) obtained with SET voltage and its value is 27.20. Table 8.1 shows the resistance values, switching voltage, and the Roff/Ron ratio measured for each state.

To analyze/predict the reliability of the data set, statistical data analysis is required. Among various analysis tools, Weibull is selected in the research due to the flexibility to analyze variable data sets. The Weibull distribution [216] of SET and RESET voltages is plotted as depicted in Fig. 8.4(c), showing that SET and RESET voltages display a right shift on the voltage axis while maintaining the minimum difference (~3 V) between them. The device current at multiple cycles obtained with SET, RESET, and intermediate voltage levels are shown in Fig. 8. 5, where the plot can also be used to describe the stability of the device states by illustrating the distinct current levels achieved with various voltage levels.

Table 8.1 Five resistive states and their resistance values, Roff/Ron ratio and corresponding switching voltage (All entries are showing the measured data)

State	Resistance (Ω)	Roff/Ron	Switching voltage (V)
IRS3	~3000	27	1.0 V
LRS	100	354	1.5 V
IRS1	1300	15	-2.3 V
IRS2	2470	04	-3.0 V
HRS	4320	-	-3.8 V

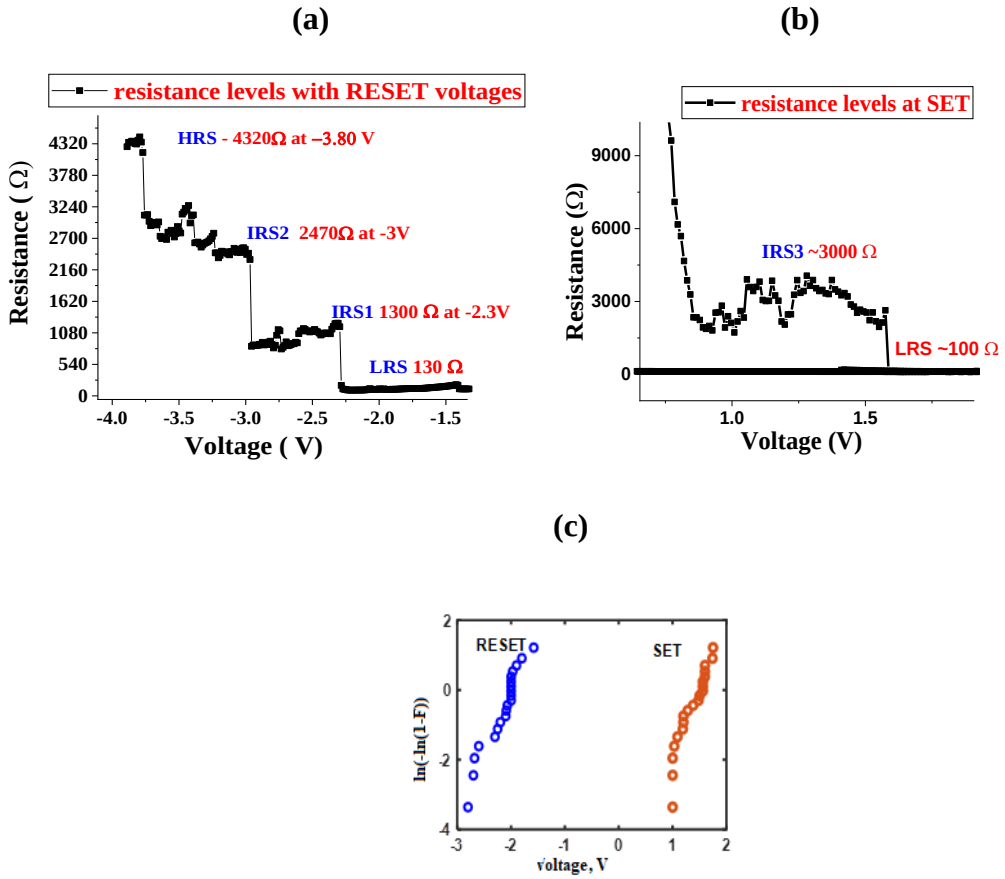


Fig. 8.4 (a) Multiple resistance levels obtained with RESET voltages and (b) SET voltages (c) Weibull distribution of SET and RESET voltages

From Fig. 8.5, it is observed that each state maintains at least ~0.7 V between each RESET/SET voltage. This feature of the multi-level memory makes it efficient to distinguish the data bits. Afterward, two major mechanisms associated with CBRAM devices, such as the current conduction mechanism and switching mechanism, are analyzed for the proposed device.

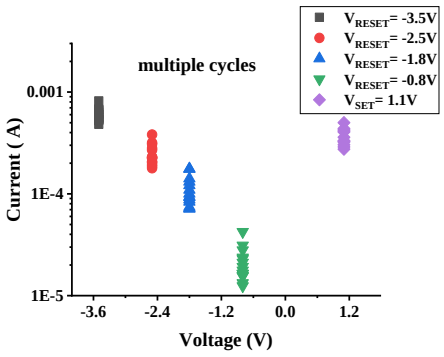


Fig. 8.5 Device current attained with multiple cycles of SET, RESET, and intermediate voltage levels

8.1.3. Conduction mechanism and switching mechanism associated with the proposed multilevel device

The conduction mechanism associated with proposed CBRAM memory has been evaluated from the slopes obtained with log-log plots shown in Fig. 8.6. The line resulting from LRS has a slope of ~1, indicating that the conduction mechanism at LRS is metallic/ohmic conduction [217]. Similarly, a linear fit to the log-log plot obtained at HRS is also plotted in Fig. 8.6 with the bold red line. Its slope is found to be ~1.9, indicating that the conduction mechanism at HRS follows child's law (Iα V^2) and current conduction is likely to be space charge limited current (SCLC) [18], [218]. The fitting models for current conduction mechanisms are plotted with solid red lines, as shown in Fig. 8.6. The possible switching mechanism of the proposed device is also investigated. In the proposed device, the switching characteristics are resulting from the electrochemical metallization (ECM) process, where the filaments formation/rupture is due to the oxidation and reduction (REDOX) reactions taking place at the top Ag/Al_2O_3 interface [43], [44], [219], [220] and its extension towards the bulk Al_2O_3 layer—owing to the REDOX reaction, metallic filament made of Ag cations forms. Then, the resistive switching is occurred due to the creation and rupture of the filaments.

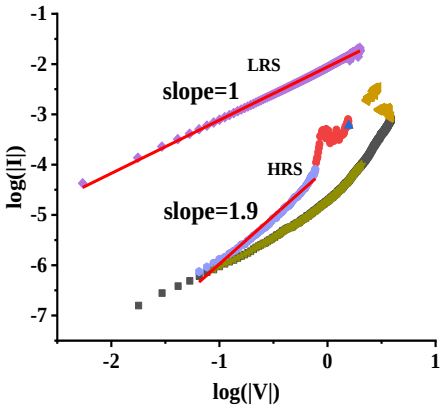


Fig. 8.6 log I vs log V plots showing the slope =1 during LRS and slope=1.9 during HRS

The study of ZnO single-layer device shows that it has a very small window of switching. Consequently, the active ZnO layer at the bottom interface has a thickness of 5 nm is likely to provide the least Oxygen vacancies, and more likely to act as tunneling oxide to limit current. Therefore, the switching is prominent in the resistive Al_2O_3 layer.

The multi-level characteristics of the proposed device are obtained by the formation of multiple filaments [212] within the Al_2O_3 active layer with different features such as diameter, length, the number of metallic ions/oxygen vacancies constituting the filament [25, 26].

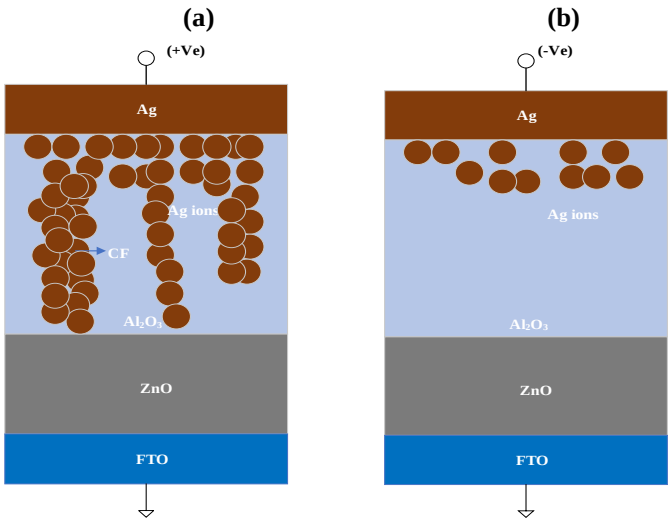


Fig. 8.7 Device structure showing the switching mechanism (a) Filaments formed during LRS at +ve polarity of input, the arrow shows the conduction filament. (b) Ruptured filament during HRS occurs at the -ve polarity of the input

When a positive voltage is applied to TE with respect to FTO, the reactive metal (Ag) cations transport from the TE to BE as given in Fig. 8.7(a), thereby driving the device to ON-state [27], whereas the negative polarity of input applied to TE leads to the oxidation of the metallic filament that results in the rupture of the filaments as given in Fig. 8.7(b). However, the device has multiple filaments formed, hence the filaments with different thicknesses require different activation energy to break. Therefore, the filaments rupture occurs at different input voltages. For instance, the initial kink shown in Fig. 8.3 might be due to the rupture of a feeble filament. Further increase in the magnitude of input voltage causes the rupture of multiple filaments resulting in a transition of states from more conductive LRS to stable IRS1, subsequently to IRS2 and finally reaches high resistance state. Thus, the device passes through several stable resistive states while sweeping the input from 0 to -4.

Further, the cycle-to-cycle variability (C2C) and device to device (D2D) variability of the devices are studied. For C2C variability, multiple I-V characteristics obtained on the response of multiple input cycles applied to a single selected device are analyzed and plotted as shown in Fig. 8.8(a). From the figure, it could be observed that the device characteristics show stable MLC states at both SET and RESET voltages with minimum-

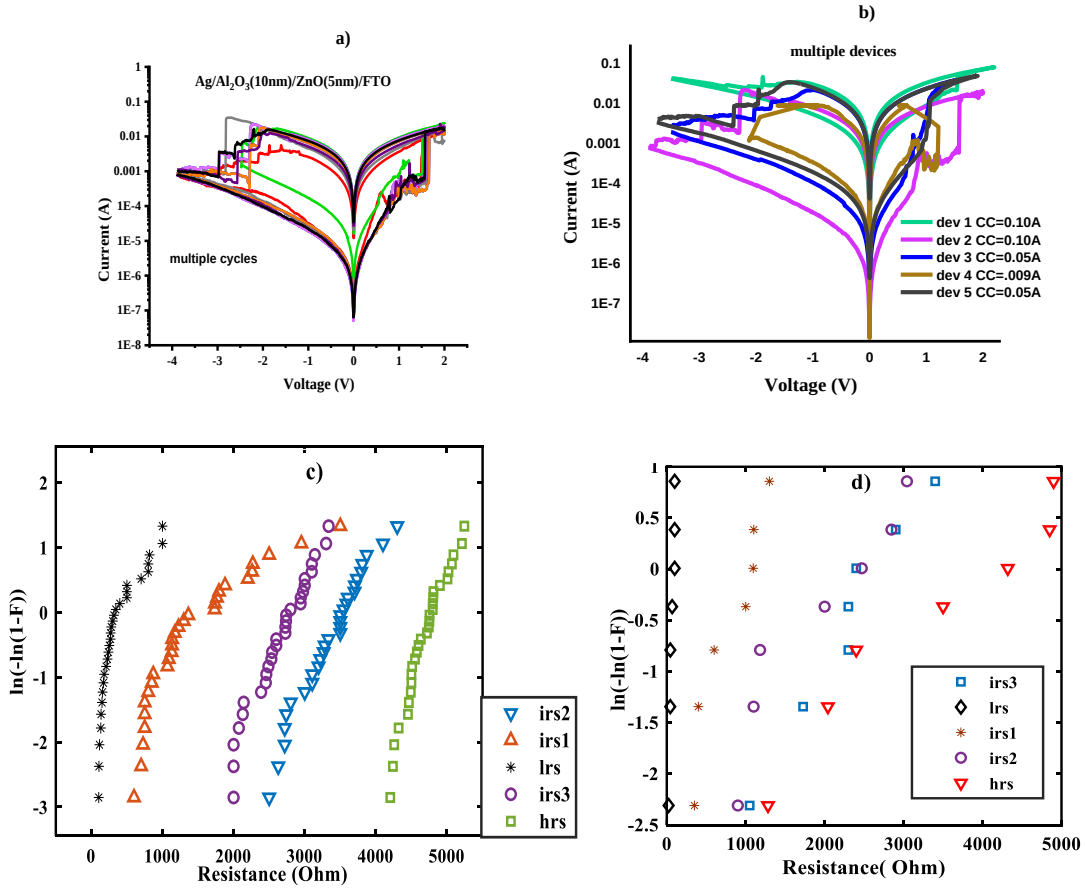


Fig. 8.8 I-V characteristics obtained with(a) a Single device with multiple cycles of input showing C2C variability(b) Multiple devices are illustrating D2D variability and the existence of multiple levels.(c) Statistical distribution of resistance during the cycle to cycle variation in a single device (d) Statistical distribution of resistance state for multiple devices filament rupture result in the RESET of the device.

variability during LRS, IRS, and HRS. Similarly, to understand D2D variability, multiple devices are chosen, and their responses are plotted. Device to device variations at different compliance current is also devised to show that all devices show multi-level characteristics as displayed in Fig. 8.8(b). From observation, it is verified that multiple resistance states are existing at different devices incongruent with the selected device and have good endurance in holding its resistance levels. The LRS exhibited by the devices shows the least variability compared to the variations in HRS. Subsequently, the statistical variation of resistance during HRS, LRS, IRS1, IRS2, and IRS3 is measured where it is observed that the resistance states achieved are distinguishable during multiple cycles of a single device(Fig. 8.8(c)). Similarly, the statistics of the distribution of resistive levels achieved with various devices are also studied and plotted in Fig. 8.8(d). From the figure, the LRS and HRS states can clearly distinguish though in some devices the resistive state IRS3 achieved with SET voltage shows a similar resistive state as that of IRS2 and IRS1.

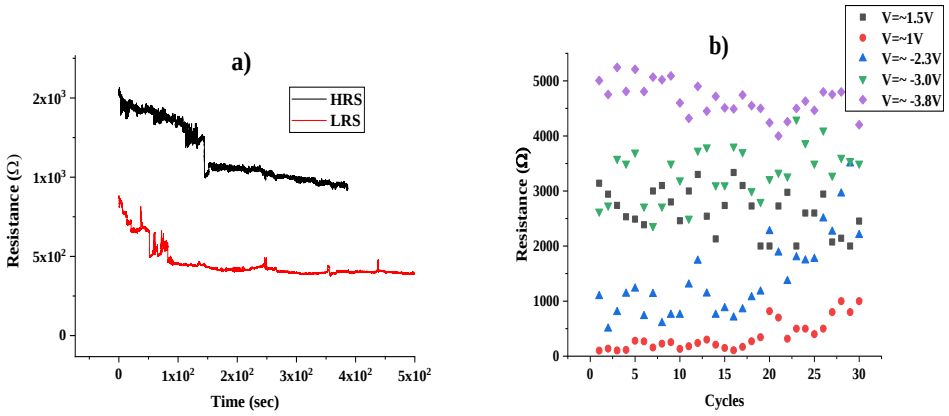


Fig. 8.9 Characteristics obtained with; (a) Retention of the device states (b) Endurance of the device during multiple cycles.

However, the mixing up of IRS3 and IRS2 or IRS1 states do not affect the device performance as IRS3 is obtained with the positive polarity of the input voltage whereas IRS1 and IRS2 are achieved with negative polarities of the input voltage.

Next, a reliability study is conducted on the device and found that the device has good retention of its states as given in Fig. 8.9(a). Then, the resistance of the device during multiple cycles (Fig. 8.9(b)) shows that the device has good endurance in holding its resistance levels.

8.1.4. Hypothetical implementation of one selector-one resistor (1S1R) with the multilevel capability

The fabricated multilevel device has connected with the $Pt/Ta_2O_5/TaO_x/TiO_2$ selector hypothetically, assuming that top electrodes, Ag and Pt are compatible. The hypothetical characteristics are derived by using MATLAB tool (Fig. 8.10). In this design, the assumptions are; when connecting the multilevel bilayer device in series with the selector device, the effect of total resistance offered by both selector and RRAM will reflect on combined characteristics, another assumption is that in series-connected devices, the selector has a major role in determining the resulting current until a potential of ~1.2 V, after that the device characteristics follows the CBRAM characteristics. The resulting characteristics showed 1S1R characteristics with low OFF-current at an input voltage range of -3V to 0 V, and the measured current is several tens of nano amperes (20 nA) that indicates the efficiency in reducing the sneak path current.

In addition, it is noted that the integrated device characteristics show the multilevel feature as obtained from the proposed CBRAM, which entitles the use of device combination in a crossbar array to store multiple bits as well. Also, it is observed that the Roff/Ron ratio of the combination is $>10^2$. Similarly, the SET, RESET voltages are also known in advance, that is the SET voltage would be somewhere near 2 V, and SET current becomes approximately 11 mA. Also, RESET voltage is approximately 1.5 V, but due to the multilevel facility, the RESET happens in steps. The first RESET occurred at -4V, and further, the device combination RESET to 3.2 mA at -4.3 V and then switches to another intermediate state of current 1.2 mA by ~4.8 V. Nevertheless, it is noticed that the difference in RESET voltage between each intermediate level is get reduced compared to that in the proposed multilevel CBRAM. In sequence, an important parameter to be assessed to measure the circuit usage in reducing sneak current is non-linearity. The non-linearity of the characteristics is estimated to find that it is ~25, which is indicating that if both devices are combined, it can be useful in large crossbar arrays. Hence it is predicted that the actual device integration will be beneficial as the combination can be used in high-density applications with the least sneak current [222].

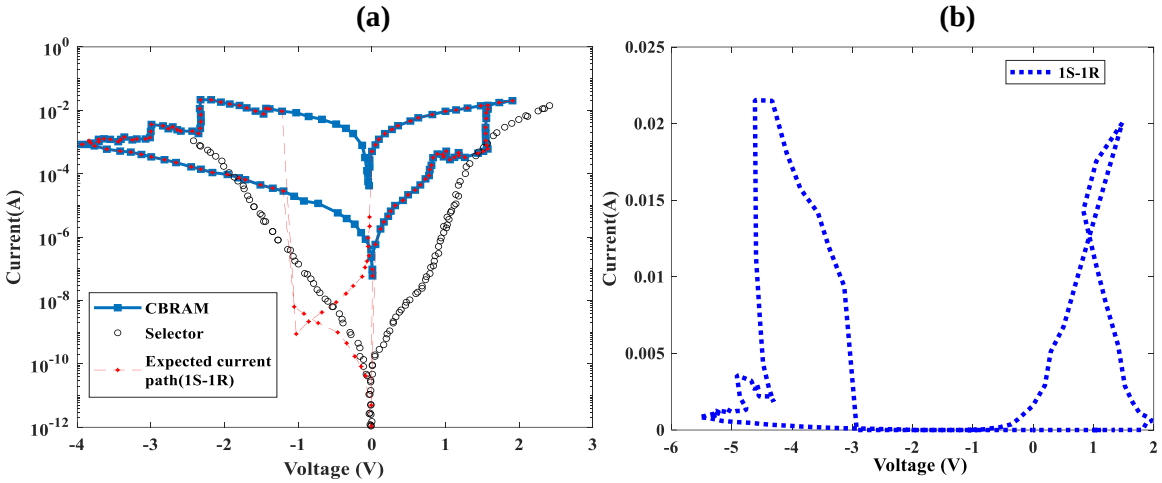


Fig. 8.10 The hypothetical realization of 1S1R device characteristics(a) RRAM, selector, approximate 1S1R current characteristics shown in logarithmic scale (b) 1S1R I-V characteristics in linear scale

8.2 Characterization of bilayer RRAM devices and implementation of 1S1R to mitigate sneak path current

To optimize the device designs and to combine with selector device, bilayer device with reverse stacking order of previously proposed CRS device (Au/ Al_2O_3 (10nm)/ZnO(15nm)/FTO) has been fabricated with Gold (Au) top electrode and Fluorine doped tin oxide (FTO) as the bottom electrode. The device structure is shown in Fig. 8.11. The preparation of the layers except the top electrode is the same as that of the multilevel memory as discussed in the previous section. In this device, the active layers Al_2O_3 and ZnO have been developed through the atomic layer deposition (ALD) method, where the top electrode is deposited using the thermal evaporation method.

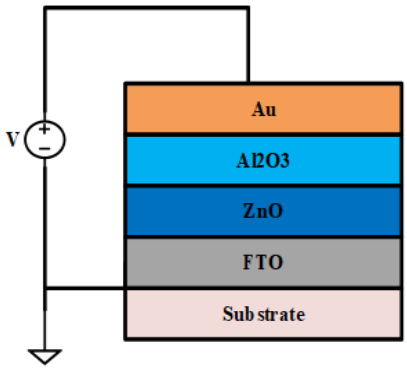


Fig. 8.11 The layout of Au/ Al_2O_3/ZnO/FTO device

The thickness of top electrode is ~100 nm, Al_2O_3 is 10 nm and ZnO is 15 nm. The pristine device shows very low current of magnitude ~5 Pf. The electroforming is performed with -10 to 10 V with a compliance current of 100 nA as shown in Fig 8.12(a).

On subsequent input sweeps the device exhibited resistive switching with SET switching occurred at ~ -1.2 V and RESET occurs at 2.5 V, marked in Fig. 8.12(b). The LRS resistance of the device measured at a read voltage of 1 V is 500 Ω and HRS is approximately 100 MΩ. The Roff/Ron ratio of the device is calculated as ~200. From the device behavior, it is interpreted that the resistive switching occurs due to the drift of oxygen vacancies under an electric field. SET switching seen in the device is abrupt, which substantiates that it has filamentary switching behavior, where a conduction filament (CF) formation depends on the electric field applied across the device. Besides, it shows gradual RESET switching as the CF rupture occurs at a lower rate as the strength of the electric field is less.

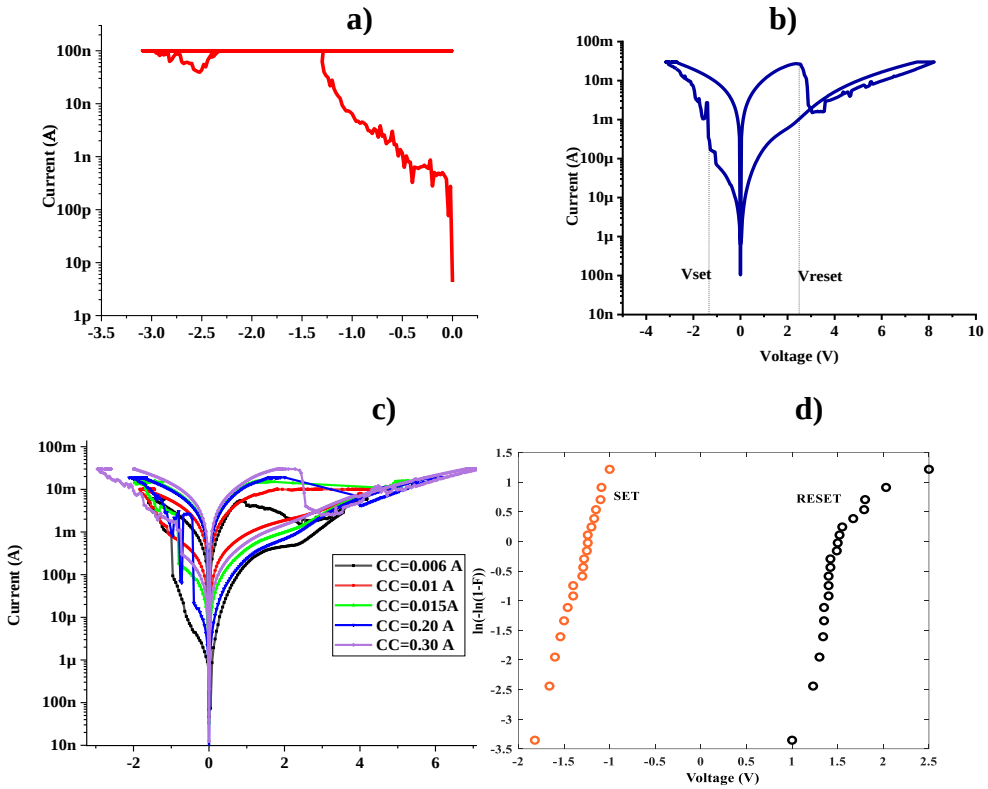


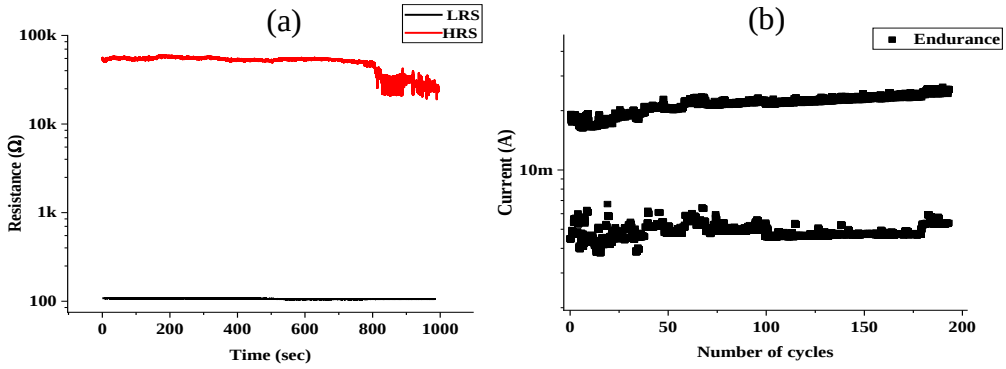
Fig. 8.12 a) Electroforming of the device with compliance current 100 nA b) I-V characteristics of the device with a sweep from -10 to 10 V and a compliance current of 0.3 A. c) Device characteristics with various compliance current levels d) Weibull distribution of SET and RESET voltages

However, it has been noticed that in a few devices, an increase in input voltage beyond RESET voltage causes a slight decrease in current as seen from Fig. 8.12(b) at voltage levels 3 to 10 V, which is due to the diffusion of the oxygen vacancies out of the conduction filament (CF). Even though the device exhibited the self-compliance feature, the current saturation level at LRS is defined with various compliance current levels applied through an external source, Fig. 8.12(c) depicts the LRS levels with different compliance currents (CC). Therefore, the inference is that the external compliance set for a device directly relates to the physical properties of conduction filament, which in turn affects the device's self-compliance level.

For further performance analysis, the statistical distribution of switching voltages is performed using Weibull distribution, which shows distinguished SET and RESET voltage levels as depicted in Fig. 8.12(d). Next, the non-linearity of the device is measured with reference to V_{SET} and V_{Read}. Non-linearity in device characteristics with respect to SET is defined as the ratio of the magnitude of the current attained at SET voltage and the magnitude of current attained at half of SET voltage. The value of non-linearity measured at V_{SET} =-1.2

V is 100. Similarly, the non-linearity with reference to read voltage is also measured and which gives a factor ~7. Next, the retention of the Al_2O_3/ZnO device is measured at the compliance of 0.03 A and a read voltage of 0.25 V at room temperature shows that the device is exhibiting excellent retention of its states, which is displayed in Fig. 8.13(a). Similarly, the endurance of the device for multiple cycles is also shown in Fig. 8.13(b). The input SET and RESET voltages

Fig. 8.13 (a) Retention of the device obtained at a read voltage of 0.25V (b)Endurance of the device



states with multiple cycles

applied to perform the endurance test of states for multiple cycles are -1.2 and 2.8V, respectively [19]. To evaluate the device performance as a memory unit, the device's response to read and write cycles is tested with multiple cycles of input pulses. The test pattern used is SET-read-RESET-read as given in Fig. 8.14. The data bit '0' is encoded with a SET pulse of amplitude -1 V with pulse width 2.2 µs, and the corresponding output current value measured is ~13mA.

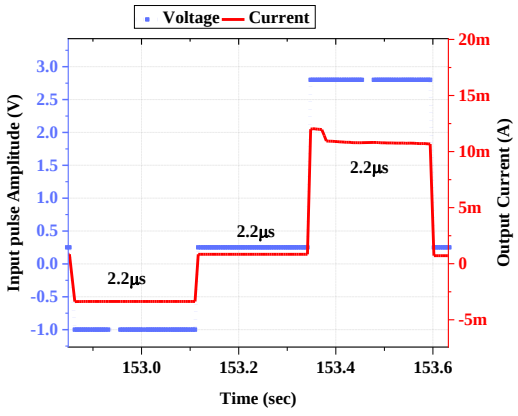


Fig. 8.14 The read and write cycles of the device with –2.8 V for writing data 0 and -1.2 V for writing the data bit 1. The blue line shows the input pulse amplitude, and the red line represents the output current X-axis showing the time scale.

Subsequent read pulse has an amplitude of 0.25V and pulse width 2.2 µs, whereas the RESET pulse has the same pulse width as that of SET. However, its pulse amplitude is 2.8 V. Corresponding states are also distinguishable during the read cycles, and there is a 0.13 mA difference in magnitude of output current between data '0' and data'1' states. In Fig. 8.14, the levels of the input pulses are shown with blue lines, and the output current from the device is marked with red lines.

8.1.5. Current conduction mechanism

The current conduction mechanism of the device is explored through the fitting models. The analysis is done based on the log I-log V plot, which reveals that the device follows different conduction characteristics at different voltage levels, as depicted in Fig. 8.15. As reported in other RRAM devices, at low resistance state (LRS), the device shows a slope ~1 verifies the ohmic conduction whereas, at high resistance state (HRS), the device exhibits ohmic conduction at lower voltage and a step-by-step transition from ohmic to space charge limited current conduction (SCLC) is noticed from the input voltage ranging from -1 to 1V. Beyond RESET voltage, the device exhibited a slope ~3, showing the trap-filled SCLC mechanism.

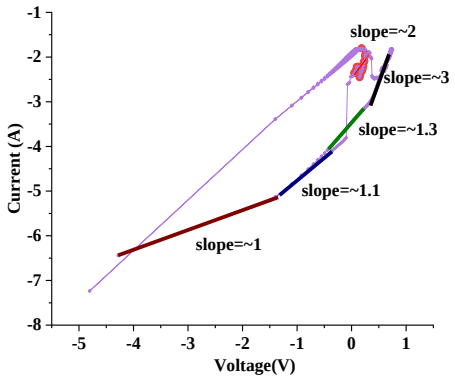


Fig. 8.15 Fitting model of conduction mechanisms exhibited by the proposed device.

8.1.6. Hypothetical implementation of 1S1R with proposed selector and RRAM

A hypothetical analysis is carried out virtually to study the possibility of combining the Pt/Ta_2O_5/TaO_x/TiO_2/Pt selector with the proposed Au/Al_2O_3/ZnO/FTO RRAM. For that, some assumptions are made, such as the top electrode/bottom electrode(s) and range of current values of both devices are also comparable. The figure corresponding to the expected combined result is given in Fig. 8.16, presented on a logarithmic scale.

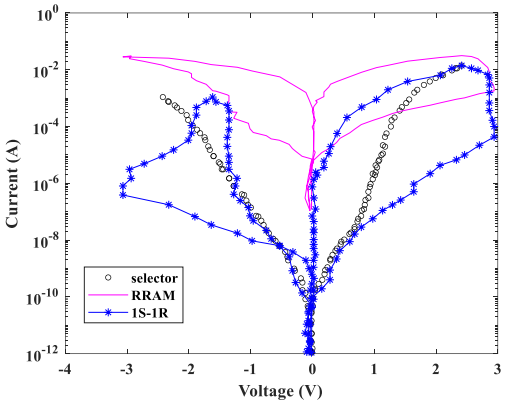


Fig. 8.16 The expected combined result of 1S1R was obtained after hypothetically connecting the proposed RRAM with the selector device.

However, in this case, both Au and Pt are not reactive. The next prediction is made on the resulting switching voltages. In this case, the SET switching occurs at -3 V, and RESET switching occurs at ~4 V.

Next, the Roff /Ron ratio is measured as ~$10^{4,}$ which shows that an excellent window presented by the RRAM cell. The nonlinearity to be obtained from the device is ~100 which is also a desirable value to accept the combined architecture.

8.1.7. Comparison of the proposed device characteristics with Au/ Al_2O_3/FTO single layer device

The I-V characteristics obtained with the proposed device structure are compared with Au/ Al_2O_3/FTO single-layer structure. The resistive switching characteristics of the proposed device are obtained by the drift of oxygen vacancies with an applied electric field across the semiconducting materials.

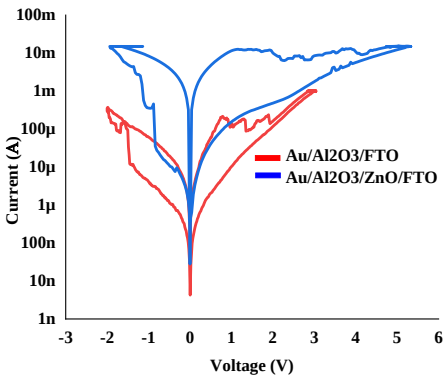


Fig. 8.17 A comparison on the I-V characteristics of the single layer as well as bi-layer (proposed) RRAM structure.

Fig. 8.17 demonstrates the I-V characteristics of the devices obtained with the current compliance level of 5 mA. However, it has been noticed that the maximum current attained with the proposed device structure is 10 mA, which is higher compared to the Au/ Al_2O_3/FTO device (~100 ΩA) and it is interpreted as the excess of oxygen vacancies and defects present at the ZnO layer is contributing for a high current level. Similarly, the SET switching in single layer device occurred at 2 V whereas in the proposed device it occurs well before 2 V due to excess of defects. Next, a comparison of RESET voltages in both devices is compared and found that the voltage required to RESET bilayer device requires more potential as shown in Fig. 8.17 due to more voltage required for rupturing a large filament. From the characteristics, it is clear that the Roff to Ron ratio of a single-layer device is approximately 30, which is less compared to the proposed device. Comparing the non-linearity of both devices where the single-layer device shows ~2.8 while the bilayer device offers a factor of ~7. Overall, the advantages of the proposed bilayer device outweigh the single-layer device.

8.3 Comparison of the proposed device and similar material stack with the active top electrode (Ag)

Next, a comparison of the behavior of the proposed device stack and an available similar stack with an active top electrode is done. The device structure used for the comparison is Ag/ Al_2O_3/ZnO/FTO and its characteristics are reported in [19], in which the RS is described as due to the presence of metal cations thereby the mechanism is mentioned as electrochemical metallization (ECM), hence such devices are falling under the category of CBRAM. Yet another comparison on the I-V characteristics of both Ag/ Al_2O_3/ZnO/FTO and Au/ Al_2O_3/ZnO/FTO are shown in Fig. 8.18, where it is clear that the SET and RESET transition in latter occurs at opposite polarity compared to that of the proposed device.

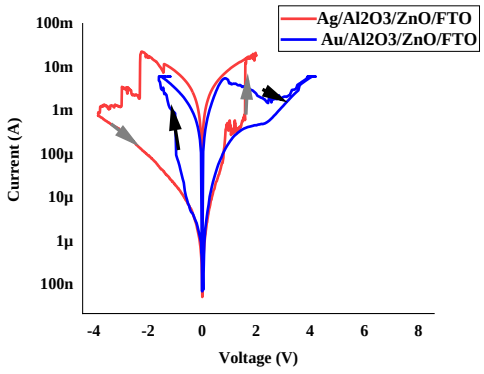


Fig. 8.18 Comparison of I-V characteristics of single-layer Au/Al_2O_3/FTO and proposed device

Moreover, the magnitudes of the SET and RESET voltages also differ. Similarly, the switching mechanisms present in both devices are different. In the proposed device the switching is contributed by the Oxygen vacancies, whereas in the device with the active electrode, the switching is contributed by the metallic cations. Also, multiple filaments form within the device with Ag top electrode owing to the presence of metallic cations, therefore multilevel switching is reported in [19] thereby useful in dense memory implementation. However, the initial resistance in both devices are the same as both are electroformed with a current compliance(CC) of $1e^{-7}$ A. The comparisons show that the top electrode plays a major role in determining the switching process whereas the materials and stacking determine the current conduction mechanisms. Here both devices showed similar slope at low voltages before reaching the switching voltage, hence current conduction during LRS state is ohmic and at HRS, it is SCLC. A comparison proposed device and the device with Ag top electrode is given in Table 8.2.

Table 8.2 Comparison on Al_2O_3/ZnO active stack with Au and Ag top electrode All entries are measured from the experiment

	Au/ Al_2O_3/ZnO/FTO Proposed	**Ag/ Al_2O_3/ZnO/FTO** [19]
Application	A single level binary memory	Multilevel high-density
Switching mechanism	Oxygen vacancy based	Metal cation based
Current transport mechanism	Ohmic, SCLC, and trap-filled SCLC	Ohmic and SCLC
SET Switching	~1 V	~2 V
RESET switching	~ -1.5 -3 V	~2 V
Roff/ Ron ratio	~200	~354

To summarise, various solutions to mitigate sneak path current are discussed in the research through modelling and fabrication. The outcome of different solutions is reported in table 8.3, where the significant parameters that determine the device's performance in reducing the sneak current in the crossbar array are evaluated. Firstly, the nonlinearity across all devices and models shows that fabricated devices exhibit better nonlinearity in the order of 10^3 to 10^6. It attributes the freedom of choosing the required voltage to be applied to selected and unselected cells so that the sneak current will be minimum. Another parameter to consider while deciding on the device configuration is the off-current, the minimum leakage current through the

unselected devices while performing read/write to a selected cell. A low off-current is desirable. Among the designs displayed in Table 8.3, a self-rectifying memristor is the best, providing 1.5 nA. A distinguishable Roff/Ron ratio is an essential parameter to use a device as a memory unit. CRS devices are showing poor Roff/Ron ratio, 1S-1R showing moderate and self-rectifying device offers a good window in the order of 4. On-current in all devices are either in micro or milli Ampers.

Table 8.3 Comparison of various parameters of proposed models/ devices favouring to mitigate sneak path current. Reading obtained for the devices with the hypothetical model is a prediction-based model with assumptions.

	1S1R Selector:Pt/Ta_2O_5/TaO_x/TiO_2					**CRS**		**Self-rectifying**
	Ta_2O_5/TaO_x (model)	**HfO_x/TiO_x (model)**	**TiO_2/TiO_{2-x} (model)**	**RRAM (experiment+hypothetic selector)**	**CBRAM (experiment+hypothetic selector)**	**Back-to-back (model)**	**Bilayer (Experiment)**	**MIM (Experiment)**
Nonlinearity	~10^3	~10	~$4x10^2$	~10^6	~10^6	~$4x10^1$	10^1	$4x10^3$
Off -current	70 nA	8 nA	0.01 A	~8 nA	~10 nA	1 µA	~1 µA	1.5 nA
Roff/Ron	~500	~100	~15	~$5*10^4$	~$5x10^2$	~10	~10	10^4
On- current	~70 µA	0.4 mA	2.8 mA	~9 mA	~20 mA	~1 mA	0.4 mA	10 µA
SET/RESET Voltage	~ -2.7/4.4 V	>-3.0 V/ 2.5V	5/-3 V	~-3.2/3 V	~2/-4 V	|3|/|5|V	|0.8|/|4| V	-2/1 V
Sneak current (calculated)	56 nA	6 nA	1.5 µA	-	-	-	-	-

Similarly, in memory devices, the SET/RESET voltages are among the major factors deciding the power dissipation across the device structure. A low SET/RESET voltage is desirable for cost-effective working. The 1S1R and CRS devices obtained by back-to-back configuration require more switching voltages, considering the drop across the multiple layers. However, the self-rectifying device offers the minimum potential to achieve switching (SET voltage:-2 V and RESET voltage:1 V); hence it promises reduced power consumption.

The chapter concludes with the fabrication and characterization of a novel, highly stable multi-level device (CBRAM) and a bilayer RRAM structure to be used in association with a selector to mitigate sneak path current. The multilevel capability of the CBRAM enables

it to use in high-density crossbar memory arrays. The device has five distinct memory states, such as HRS, LRS, IRS1, IRS2, and IRS3, their statistical variation of resistance are distinguishable during multiple cycles of a single device. In addition, the device-to-device characteristics are also studied to show that the devices show stable multilevel switching. Further, a comparative study of various parameters is carried out across the fabricated devices /models and found that the self-rectifying memristor with Au/Al_2O_3/FTO (MIM) structure, multilevel CBRAM devices (in association with selector) are the most promising devices to be used in crossbar array to mitigate the sneak path current. Among models, Pt/ Ta_2O_5/TaOx/ Pt, with Pt/ Ta_2O_5/TaOx/TiO_2/Pt selector is a better candidate to mitigate sneak current.

Chapter 9

Conclusion and Future works

The research work is focused on different methods to mitigate sneak path current in resistive random-access memory (RRAM) nano crossbar arrays, including the 1S1R architecture, CRS, and self-limited self-rectifying resistive random-access memories. The first part of the research work adopted a modeling approach to analyze the sneak path current reduction using 1S1R as well as CRS methodology. For that, the analytical/electrical model of the selector device and selector-RRAM models (1S1R) are developed to demonstrate the role of the selector in reducing sneak path current. In particular, the sneak current reduction is illustrated by connecting different RRAM models such as Ta_2O_5/TaO_x, HfO_x/TiO_x , TiO_2/TiO_{2-x} with $Pt/Ta_2O_5/TaO_x/TiO_2$ selector (1S1R) and found that their low dimension crossbar arrays efficiently reduced the sneak path current by 98%, 99.8%, and 96% respectively on compared to their RRAM array counterparts, whereas the CRS device model formed by back-to-back connected TiO_2/TiO_{2-x} RRAM has shown a reduction of 93% in the total sneak path current. Similarly, the nonlinearity of the 1S1R circuits is improved such that the non-linearity factor becomes ~400, 100, 15, respectively in sequence for 1S1R while the CRS circuit has shown a non-linearity of ~8. Similarly, the OFF-current shown by 1S1R circuits have shown in the order of several 10-100 nA, whereas the CRS model has shown OFF-current in the order of several μA.

In addition, in this work, an interesting phenomenon of substantial reduction in device resistance is noticed beyond the RESET voltage of several RRAM devices (Ta_2O_5/TaO_x device structures in particular) and is reported that this additional current is due to the current component present at outside of the conduction filament (OCF), which is modelled by considering the trap assisted tunneling (TAT) mechanism. Both electrical and analytical models explain the concept where the oxygen vacancy traps at OCF enable the electrons to transport across the switching layer.

In the second part of the research, different RRAM devices are proposed to reduce sneak current in crossbar arrays; initially, a RRAM device with MIM ($Au/Al_2O_3/FTO$) structure exhibiting self-limited self-rectifying characteristics is fabricated, which is a recent trend in reducing sneak current with where the capacitive nature of the device has shown a non-

zero crossover switching characteristics, which is found to be more beneficial to use in crossbar arrays as the self-rectifying nature reduces the sneak path current. The Roff/Ron ratio attained with the Au/Al_2O_3/FTO structure is ~400, while the nonlinearity is found to be ~5. However, the rectification ratio obtained for the device is ~200, which makes it desirable for sneak current reduction. Moreover, the research progresses with the fabrication of a novel bilayer complementary resistive switching device of Au/ZnO/Al_2O_3/FTO structure, its reliability analysis, and its response to read/write pulses. The device has shown a nonlinearity of ~11 and better retention and switching time (µsec). In addition, it is reporting here that the Roff/Ron ratio of the device can be increased by optimizing the thickness of the switching layers.

Alternatively, a CBRAM and RRAM device have been fabricated/characterized to analyze their performance as an individual cell and in 1S1R configuration. The CBRAM device is obtained with an active top electrode (Ag) on top of the Al_2O_3/ZnO stack, thereby reporting five distinguishable memory states available for the device suggesting its potential use in high-density memory applications. It has been reported that the device can achieve five distinctive resistive levels such as 1300, 2700 and 4320 Ω, 3000 and 100 Ω, at a distinguishable range of input voltages with each voltage level separated by at least ~0.7 V. The first three resistance levels are attained with RESET voltages, and last two are attained with SET voltages. Moreover, the proposed device excels in its Roff/Ron ratio of 354 obtained with HRS/LRS and the ratio of intermediate states IRS1, IRS2, IRS3 to HRS becomes 15, 04, and 27, respectively. Likewise, the proposed RRAM formed out of Au/ Al_2O_3/ZnO/FTO has exhibited bipolar switching with a Roff/Ron ratio of 100 and has shown better retention as well as endurance ($>10^3$), which shows that the RRAM device is suitable for reliable memory applications.

Further, both CBRAM and RRAM are hypothetically connected with the Pt/Ta_2O_5/TaO_x /TiO_2 selector to form a 1S1R structure. After that, their I-V characteristics are analyzed, such as high nonlinearity, Roff/Ron ratio, current density, and low OFF-current to ensure that the devices are promising to reduce sneak current while connected in 1S1R configuration. The Roff/Ron ratio obtained with hypothetical 1S1R CBRAM and RRAM devices are 10^2 and $10^{4,}$ respectively. Similarly, the non-linearity obtained from combined architectures is (hypothetical) ~25 and ~100, respectively. Moreover, the off-currents observed in both multilevel-CBRAM and RRAM are negligibly low as in the range of nano Amperes.

Analysis of all device combinations show that self-rectifying memristors are the better candidate to use in crossbar array, as it neither need any additional devices do not require any

complicated processes to fabricate. Moreover, they provide better Roff/Ron ratio (10^4) and high non-linearity($4x10^3$) with low off current (nA). Another observation from the results is that connecting the multilevel device with appropriate selector may promise efficient ultra-high-density memory with low sneak path current. Also, suggests that bilayer CRS devices are beneficial than back-to-back connected CRS configuration.

In the future, more study on the material composition while obtaining the intermediate states will be done. Also, the developed devices would be implemented in a crossbar array to test for the sneak path current and be used for specific neuromorphic applications such as pattern matching, and data identification, etc. Also, the proposed devices can be used in large memory arrays due to low sneak path current and can be used in embedded devices and sensor applications to store data. Data analytics/big data applications are another horizon to utilize the CRS or 1S1R RRAM arrays.

9.1 The unique contributions of the research

i. Implementation of the physics-based electrical, and analytical models of the selector to use with RRAM for reducing the sneak current.
ii. Different RRAM -selector combinations are studied to analyze the effect of selector in sneak path current reduction.
iii. Physics-based RRAM model explaining the role of outside conduction filament on device current characteristics.
iv. Various resistive switching devices have been fabricated based on Al_2O_3 and ZnO materials, showing different switching characteristics upon stack ordering/arranging the switching layers and using different top electrodes
v. Proposed a multilevel device with the selector to achieve ultra-density memory with reduced sneak path current

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