

SVPWM Zero-Sequence Voltage Elimination for the Dual Fed Common dc-link Open-End Winding PMSM High-Speed Starter-Generator

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Abstract

The dual-inverter topology has been widely investigated for Open-End Winding (OEW) machines such as induction motors and Permanent Magnet Synchronous Motors (PMSMs). The extensive work done on this topology showed that three-level inversion can be realized with two two-level inverters connected at each end of the machine terminals. Furthermore the dual-fed OEW topology allows for increased fault-tolerant capability, reduction of the dc-link voltage by half and redundant space-vector combinations. In this PhD work, a dual-inverter made of a Si-based 3ph full-bridge converter and one SiC-based 3ph full-bridge connected across the same dc link has been used to drive an high-speed starter-generator OEW-PMSM for aerospace application. The mixed technology dual-inverter allows to achieve higher system efficiency by exploiting the different nature of the two Voltage Source Converters (VSCs). While on one hand the common dc bus configuration significantly simplifies and reduces the costs of the topology, on the other hand it allows the Zero-Sequence Current (ZSC) to flow freely in the system. Previous work focused on the study of modulations which aim to either reduce or control the average Zero-Sequence Voltage (ZSV) on the controller sample time. The low phase inductance, which characterizes high speed machines implies low Zero-Sequence Impedance (ZSI). Therefore any ZSV applied to the zero-sequence circuit would result in a high frequency, high intensity ZSC ripple with the risk of harming the switching devices. This work presents a novel hybrid Space Vector Pulse Width Modulation (SVPWM) that allows to instantaneously eliminate the ZSV produced by the dual-inverter by square wave modulating the IGBT VSC. The non-sinusoidal machine's back Electro Magnetic Force (back-EMF) has been considered and the effect of the converters Dead Time (DT) on the ZSV has been analysed. Since the ZSV generated by the dual-inverter causes high ZSC to circulate in the machine, the voltage distortion introduced by the DT has been considered as a possible control action to eliminate the ZSC flowing due to the non-sinusoidal machine's back-EMF. A novel SVPWM for instantaneous ZSV

elimination and a zero-sequence DT hysteresis controller have been investigated and experimentally tested both on a scaled-down OEWM and the full-scale high-speed starter-generator prototype.

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List of Terms

AC - Alternate Current

APU - Auxiliary Power Unit

CM - Common Mode

$CPWM$ - Continuous Pulse Width Modulation

CVG - Constant Velocity Gearbox

DC - Direct Current

DM - Differential Mode

$DPWM$ - Discontinuous Pulse Width Modulation

DSP - Digital Signal Processor

DT - Dead Time

EMF - Electro-Motive Force

EV - Electric Vehicle

$FCMLI$ - Flying Capacitor Multilevel Inverter

FFT - Fast Fourier Transform

$FPGA$ - Field Programmable Gate Array

$FS-MPC$ - Finite State-Model Predictive Controller

HEV - Hybrid Electric Vehicle

$IATA$ - International Air Transport Association

$IGBT$ - Insulated Gate Bipolar Transistor

MAF - Moving Average Filter

MEA - More Electric Aircraft

MLC - Multilevel Converter

NPC - Neutral-Point Clamped

$NPCMLI$ - Neutral Point Clamped Multilevel Inverter

OEW - Open-End Winding

$OEWM$ - Open-End Winding Motor

$PBDTC$ - Pulse Based Dead Time Compensator

PE - Power Electronic

PGU - Power Generation Unit

PI - Proportional Integral

PIR - Proportional Integral Resonant

PM - Permanent Magnets

$PMSM$ - Permanent Magnet Synchronous Motor

PV - Photovoltaic

PWM - Pulse Width Modulation

Si - Silicon

SiC - Silicon Carbide

SVM - Space Vector Modulation

$SVPWM$ - Space Vector Pulse Width Modulation

THD - Total Harmonic Distortion

VF - Variable Frequency

VSC - Voltage Source Converter

$VSCF$ - Variable-Speed Constant Frequency

VSI - Voltage Source Inverter

WF - Wild Frequency

ZSC - Zero Sequence Current

ZSI - Zero Sequence Impedance

ZSV - Zero Sequence Voltage

ZVR - Zero Vector Redistribution

Nomenclature

t - Time [s].

T_s - Controller sample time [s].

t_{dt} - Converter's Dead-Time [s].

p - Pole pairs number.

$\mathbf{T}_P(\vartheta_e)$ - qd0 reference frame transformation matrix [-].

ϑ_e - Electrical rotor angular position [rad].

ϑ_m - Mechanical rotor angular position [rad].

ω_e - Electrical rotating speed [rad/s].

ω_m - Mechanical rotating speed [rad/s].

I_{rated} - Rated machine current [A].

ω_{rated} - Rated Mechanical rotating speed [rad/s].

V_{dc} - dc link Voltage [V].

R - Stator Resistance Matrix.

R_s - Machine phase stator resistance [Ω].

N_s - Number of stator coil turns [−].

μ_r - PM relative permeability.

B_{res} - Residual PM flux density [T].

l - Active machine length [m].

g_0 - Airgap length [m].

h_m - Magnet thickness [m].

L_{Sabc} - Static machine inductances matrix. [−].

L_{Mabc} - ϑ_e dependant machine inductances matrix. [−].

L_{abc} - Machine inductances matrix. [−].

L_d - d-axis machine inductance. [H].

L_q - q-axis machine inductance. [H].

L_0 - 0-axis machine inductance. [H].

L_{Ls} - Machine leakage inductance. $[H]$.

I_{abc} - Machine phase currents vector. $[-]$.

i_a - Current of phase a $[A]$.

i_b - Current of phase b $[A]$.

i_c - Current of phase c $[A]$.

i_0 - ZSC $[A]$.

V_{abc} - Machine phase voltages vector. $[-]$.

λ_{abc} - Machine phase fluxes vector $[-]$.

Λ_r - rotor's permanent magnet flux linkage with the stator windings. $[Wb]$.

Λ_{1r} - Fundamental component of Λ_r. $[Wb]$.

Λ_{3r} - Third harmonic component of Λ_r. $[Wb]$.

λ_m - Peak flux linkage established by the rotor's permanent magnets. $[Wb]$.

$k_{3\lambda}$ - ratio between the third harmonic flux and λ_m. $[-]$.

I_{qd0} - Machine qd0 currents vector. $[-]$.

V_{qd0} - Machine qd0 voltages vector. $[-]$.

Λ_{qd0} - Machine qd0 fluxes vector. $[-]$.

e_a - machine's phase a back-EMF. $[V]$.

e_b - machine's phase b back-EMF. $[V]$.

e_c - machine's phase c back-EMF. $[V]$.

V_{a0} - Output phase a voltage of VSC A. $[V]$.

V_{b0} - Output phase b voltage of VSC A. $[V]$.

V_{c0} - Output phase c voltage of VSC A. $[V]$.

$V_{a'0}$ - Output phase a voltage of VSC B. $[V]$.

$V_{b'0}$ - Output phase b voltage of VSC B. $[V]$.

$V_{c'0}$ - Output phase c voltage of VSC B. $[V]$.

$V_{a'a}$ - Phase a voltage of the OEW-PMSM. $[V]$.

$V_{b'b}$ - Phase b voltage of the OEW-PMSM. $[V]$.

$V_{c'c}$ - Phase c voltage of the OEW-PMSM. $[V]$.

$\overline{V}_A$ - VSC A output phase voltages. $[V]$.

$\overline{V}_B$ - VSC B output phase voltages. $[V]$.

$\overline{V}_{OEW}$ - OEW-PMSM phase voltages. $[V]$.

$\overline{V}_{OEW}^{qd0}$ - OEW-PMSM qd0 voltages. $[V]$.

$\overline{V}_A^{qd0}$ - VSC A qd0 output voltages. $[V]$.

$\overline{V}_B^{qd0}$ - VSC B qd0 output voltages. $[V]$.

$\overline{V}_{OEW}^{q}$ - q-axis voltage component of the OEW-PMSM $[V]$.

$\overline{V}_{OEW}^{d}$ - d-axis voltage component of the OEW-PMSM $[V]$.

$\overline{V}_{OEW}^{0}$ - 0-axis voltage component of the OEW-PMSM $[V]$.

$\overline{V}_A^*$ - VSC A reference voltages $[V]$.

$\overline{V}_B^*$ - VSC B reference voltages $[V]$.

$\overline{V}_{OEW}^*$ - OEW-PMSM reference voltages $[V]$.

$\overline{V}_A^{*SW}$ - Square Wave reference signals for VSC A $[V]$.

T_0 - Phase voltage fundamental period $[s]$.

V_0^A - ZSV component of the output VSC A voltage $[V]$.

V_0^B - ZSV component of the output VSC B voltage $[V]$.

V_0^{OEW} - ZSV component of the output OEW-PMSM voltages $[V]$.

$\overline{V}_{OEW\alpha\beta}^*$ - Fixed reference frame reference OEW-PMSM voltages $[V]$.

V - Module of the Inverter output voltage vectors in the fixed reference frame $\alpha\beta 0$ $[V]$.

s_j - State of the top switch of the j^{th} leg.

$s_j^{'}$ - State of the bottom switch of the j^{th} leg.

s_j^{old} - Previous sample time State of the top switch of the j^{th} leg.

t_j - Dwelling time of the j^{th} voltage vector.

$\overline{V}_j$ - Voltage vectors applied by VSC A.

$\overline{V'}_j$ - Voltage vectors applied by VSC B.

Φ - Discrete state matrix of the PMSM $[-]$.

Γ - Discrete input matrix of the PMSM $[-]$.

i_k^q - q-axis current at the k^{th} time instant $[A]$.

i_k^d - d-axis current at the k^{th} time instant $[A]$.

i_k^0 - 0-axis current at the k^{th} time instant $[A]$.

t_{min} - Smallest dwelling time among the three active vectors SVM.

t_{med} - Medium dwelling time among the three active vectors SVM.

t_{max} - Biggest dwelling time among the three active vectors SVM.

t_{jinf}^x - time instant at which the leg carrier changes slope.

t_{jsup}^x - time instant at which the leg carrier changes slope.

i_{0lim} - ZSC controller Hysteresis band amplitude $[A]$.

A - State matrix of the plant.

B - Input matrix of the plant.

C - Output matrix of the plant.

K - Feedback Gain.

x - State vector of the plant.

u - input vector of the plant.

y - Output vector of the plant.

r - Reference vector of the plant.

$\mathbf{x}_B$ - State vector of the current loop plant extended with the integrator.

Φ_B - Discrete State matrix of the extended state current loop.

Γ_B - Discrete Input matrix of the current loop.

$\tilde{V_q}$ - Decoupled reference q-axis voltage of the current loop controller.

$\tilde{V_d}$ - Decoupled reference d-axis voltage of the current loop controller.

K_i - Current loop integrator controller gain.

ω_0 - Current loop controller bandwidth.

R_{dcs} - dc link equivalent series resistance.

C_{dc} - dc link capacitance.

R_{Cdc} - series resistance of the dc link capacitor.

V_{abc}^{SiC} - SiC based devices VSC phase voltages.

V_{abc}^{IGBT} - IGBT based devices VSC phase voltages.

V_0^{SiC} - ZSV of the SiC based devices VSC phase voltages.

V_0^{IGBT} - ZSV of the IGBT based devices VSC phase voltages.

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Chapter 1

Introduction

This Chapter is an introduction to the thesis. In particular, the objectives of the PhD project are provided and the concepts of the More Electric Aircraft (MEA) and the Open-End Winding Machine (OEWM) are presented.

1.1 Objectives of the PhD project

The main objective of the PhD project is to develop a modulation for the instantaneous elimination of the ZSV produced by the dual-inverter feeding a high-speed OEW-PMSM starter-generator. Furthermore, the ZSV distortion introduced by the DT is considered as a zero-sequence axis control action to eliminate the sinusoidal ZSC flowing because of the machine back-EMF's harmonic content. Therefore a portion of the PhD effort has been spent on studying and formulating the analytical model of the OEW-PMSM in terms of its voltage equations. An equivalent circuit has been obtained to be used for the simulative work. As a starting point previous modulations proposed in literature to reduce or eliminate the problem of the ZSV produced by the VSCs have been considered. Interesting work has been carried out for both the

standard two-level VSC and the dual-inverter with different dc-link topologies. The aim is to reduce the ZSV variation to reduce premature deterioration of ball bearings caused by the flow of parasitic capacitance currents. The machine considered in this work is an high-speed OEW-PMSM starter-generator. The machine is characterized by extremely low phase inductance and, consequently, by low equivalent ZSI. The ZSC flowing due to the ZSV generated by the dual-inverter under standard PWM is not acceptable. Furthermore the modulations previously developed in literature for the dual-inverter topology either aim to eliminate the average ZSV applied on the controller sample time or suppose that both VSCs switch at the same switching frequency. In order to increase the system efficiency the dual-inverter designed and built for this project is made of two VSCs using different semiconductors technology. One is a Si-based 3ph full-bridge converter while the other is a SiC-based 3ph full-bridge. The proposed modulation achieves the ZSV instantaneous elimination and allows to exploit the different nature of the technologies used. The IGBT converter is modulated in six-step mode while the SiC VSC is modulated in order to eliminate the voltage distortion introduced by the other. Since the ZSV applied is strictly related to the sequence of switching states used by the converter to synthesize the reference voltage vector, the modulation proposed aims to use the voltage vectors which produce the same ZSV on both VSCs. Furthermore the non-sinusoidal back-EMF of the machine has been considered, which is responsible for the additional flow of ZSC. The low ZSI does not allow for the application of any ZSV, which would result in high ZSC flowing in the system. Therefore the ZSV distortion introduced by the DT is considered as a possible control action to eliminate the ZSC flowing because of the non-sinusoidal machine back-EMF. A novel DT hysteresis controller to suppress the ZSC has been developed.

1.2 The Open-End Winding Topology

One of the transportation sectors which has seen a major penetration of the electrical systems over the mechanical ones is the aerospace industry. The main target of the MEA is the reduction of the take-off weight obtained through the replacement of the mechanical, pneumatic and hydraulic systems with their electrical equivalent. The on board electrical power is mainly generated by means of electrical generators driven by an accessory gearbox mounted on the gas turbines. The OEW configuration of the PMSM stator windings is a very promising architecture for a starter-generator connected to the turbine for the reasons explained in the following.

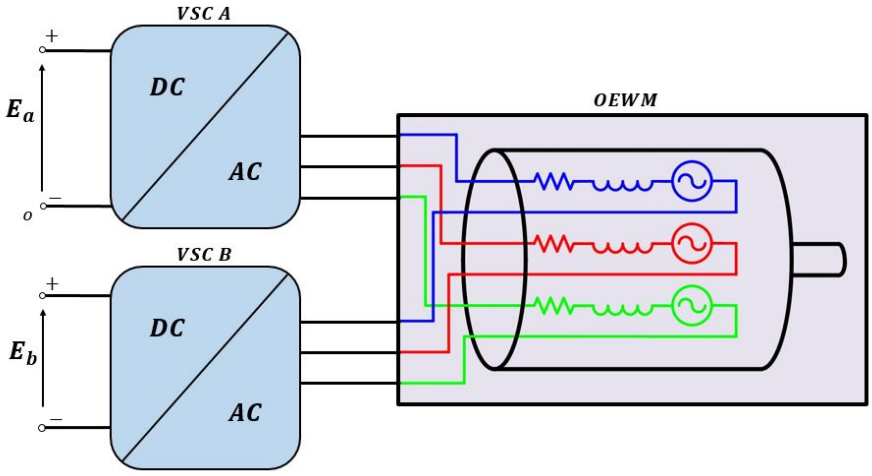


Figure 1.1: The OEW Machine configuration

In most of the cases an OEWM is obtained from a standard machine of which its stator windings are connected in star configuration. Fig. 1.1 shows an OEW-PMSM machine connected to two VSCs. The advantages of the OEW configuration for ac machines drives were already investigated by Stemmler and Guggenbach in 1993 [2] showing how three-level inversion could be realized with two 2-level inverters connected at each end of the machine. Furthermore the dual-fed OEW topology allows

for increased fault-tolerant capability [3, 4], reduction of the dc-link voltage by half and redundant space-vector combinations. Because of its advantages the dual-fed OEW configuration has found a wide range of applications such as wind power generation [5, 6], electric vehicles [7, 8], high power electric propulsion [9] and aircraft starter-generator systems [10–12]. Referring to Fig. 1.1 different dc link topologies can be adopted for the dual-inverter: two isolated dc power supplies [13], one dc supply and a floating bridge [14] or a single dc supply [15]. While on one hand the common dc bus configuration significantly simplifies and reduces the costs of the topology, on the other hand it allows the ZSC to flow freely in the system. As widely discussed in [5, 16] the causes of a circulating ZSC can be attributed to ZSV generated by the converters, third harmonic component of the back-EMF, devices' DTs, device's voltage drops. The magnitude of the ZSC depends on the equivalent ZSI which is generally low as reported in [17, 18]. With a particularly low phase inductance, and consequently even smaller ZSI the equivalent zero sequence circuit is less able to filter out the high-frequency components of the switched voltage. In other words, a small time constant of the zero-sequence circuit produces a high frequency, high intensity current ripple with the risk of harming the switching devices. The more the machine inductance is low the more problems, associated with the circulation of a ZSC, are going to be relevant leading to high intensity ZSC ripple. The ZSC reduces the overall system efficiency therefore many works focused on VSCs' modulations to reduce or eliminate the zero-sequence component of the voltage supplied to the machine [5, 17, 19, 20].
The manuscript is organised as follows:

- Chapter 1: introduction. The content and objectives of the PhD project are presented and the concept of the OEW configuration is given.
- Chapter 2: literature review and state of the art of the More Electric Aircraft (MEA) concept, of the dual-inverter topologies and the possible solutions to reduce the ZSV in both two-level VSCs and dual-inverters.

- Chapter 3: electromagnetic model of the PMSM and extension to its OEW configuration. The analytical model is characterized in terms of voltage equations.
- Chapter 4: reference voltage split strategy for the two individual 2-level VSCs. The reference voltages are chosen in order to exploit the different technology of the power converters. Furthermore, the three active vectors SVM for the instantaneous elimination of the ZSV generated by the dual-inverter are presented.
- Chapter 5: analysis of the ZSV distortion introduced by the DT and DT hysteresis controller. The effect of the DT on the ZSV for the proposed SVPWM is evaluated and exploited to eliminate the ZSC flowing due to the non-sinusoidal back-EMF of the machine.
- Chapter 6: current and speed loop controllers design. Based on the state-space approach, the synthesis and determination of the gains of the full state feedback current controller is given. Furthermore, the speed loop controller and the speed and load torque observer gains calculation are presented.
- Chapter 7: numerical simulation results under both standard PWM and the proposed SVPWM for instantaneous ZSV elimination. Both the high-speed starter-generator and the scaled-down OEWM performances are tested.
- Chapter 8: experimental validation of the proposed SVPWM. The experimental rig is described in all its parts. The proposed modulation is used to suppress the ZSV generated by the dual-inverter and the novel DT hysteresis controller is used to eliminate the additional ZSC flowing due to the machine non-sinusoidal back-EMF.
- Chapter 9: summary of achievements, conclusions and tasks for future works.

1.3 Chapter Summary

In this Chapter the objectives of the PhD project are presented together with a brief description of the MEA and the OEW topology concepts. Then the advantages of the open-end configuration have been presented. Finally a detailed overview of the thesis structure has been given.

Chapter 2

Literature Review

2.1 Introduction

This Chapter is the result of the bibliographic research that has been carried out to study the dual-inverter topology with single dc-link. At first, the motivations that lead to investigate this topology are presented. The importance of variable speed AC drives in the transportation sector is discussed with particular attention to the aerospace field. The MEA concept is presented and different on-board Power Ground Unit (PGU) architectures are discussed. An overview of the multilevel inversion principles is given. The dual-inverter topology is selected and the possible dc link configurations are investigated. Among the possible solutions, the topology with single dc link has the advantage of being the easiest to be implemented but on the other hand the main drawback is the circulation of additional ZSCs. The problem of circulating ZSCs due to the ZSVs produced by the VSI has been extensively studied in the literature. Here the possible solutions for standard two level VSCs drives and for the dual-inverter topology with separate and common dc link are presented. The modulation techniques adopted for the dual-inverter to reduce the ZSV based on the

zero-sequence vector redistribution are investigated. In the end, the influence on the drive performances of the VSI non-linearities is evaluated. In particular the ZSV distortion introduced by the DT distortion in the dual inverter topology is analysed. In this PhD project the dual-inverter, mixed technology IGBT-SiC with single dc link topology is chosen to feed the OEW-PMSM Starter-Generator.

2.2 The Importance of Variable Speed Drives and their Applications

During the last decades the global demand for electricity grew. Electricity generation increased by 3.1%, or 780 TWh, worldwide in 2017 as electricity demand rose faster than overall global energy demand growth. Power industries account for 42% of all the electricity used. Two thirds of this energy is used to power electrical motors. Therefore significant attention has been given to obtain improvements in the efficiency of electrical machines. Over the last few decades, the transportation sector has been deeply penetrated by electrical motor drives comprising of power electronic converters and advanced electric machines. With the intent of improving the efficiency of electric transports, grater demand is put on power electronics system, electrical motors and control structures. Control architectures for variable speed drives and efficient motors are the key aspects in order to increase the overall efficiency of the electrical systems. The applications of variable speed drives are numerous and therefore their requirements vary from case to case. Some of the performance often required for the motor drives are: high torque capability from zero speed to base speed, high efficiency over a wide range of operating conditions, constant power capability over a speed range of typically above base speed, low weight, small volume, low cost, good controllability, low torque ripple and high reliability to only name a few.

One of the transportation sectors which has seen a major penetration of electrical sys-

tems over the mechanical ones is the aerospace industry. The main target of the MEA is the reduction of take-off weight obtained through the replacement of mechanical, pneumatic and hydraulic systems with their electrical equivalent. The implementation of MEA technologies leads to a reduction of the take-off weight by about 6.5% and an increase in the mean time before two consecutive failures of 5.4% [21]. The expansion of the air transportation system is proven by the past years numbers. Between 2012 and 2017 the civil air traffic has grown at an average rate of 9% per year [22] and, according to airlines [23], it increased by 31% in passenger numbers. Furthermore, the International Air Transport Association (IATA) forecasts that by 2036 air passengers will nearly double to 7.8 billion. One of the reasons of this quick growth can be identified in the availability of new technological improvements for aircraft. In particular the reduced take-off weight, achieved with the use of new materials, and optimized propulsion engines have led to a reduction in fuel consumptions and maintenance related costs.

2.3 The More Electric Aircraft

From the point of view of the conservative aerospace industry, even if the possibility to switch to a full electric structure for the on board equipment is feasible and capable to introduce considerable improvements in efficiency and reliability, the risks involved in this complete technology change have been considered too large. Therefore the aerospace industry decided to approach the electrification of the aircraft with a step-wise approach. Among the supporters of the MEA the US Air Force [24] has embraced the concept as a mean to securely increase the reliability, the fault tolerance capabilities, the power density and the performance of fighter aircrafts [25]. The introduction of electronic systems as also been spotted by civil aircraft producers as the key point to further increase the efficiency and reduce both the fuel related costs and CO2 emissions [26].

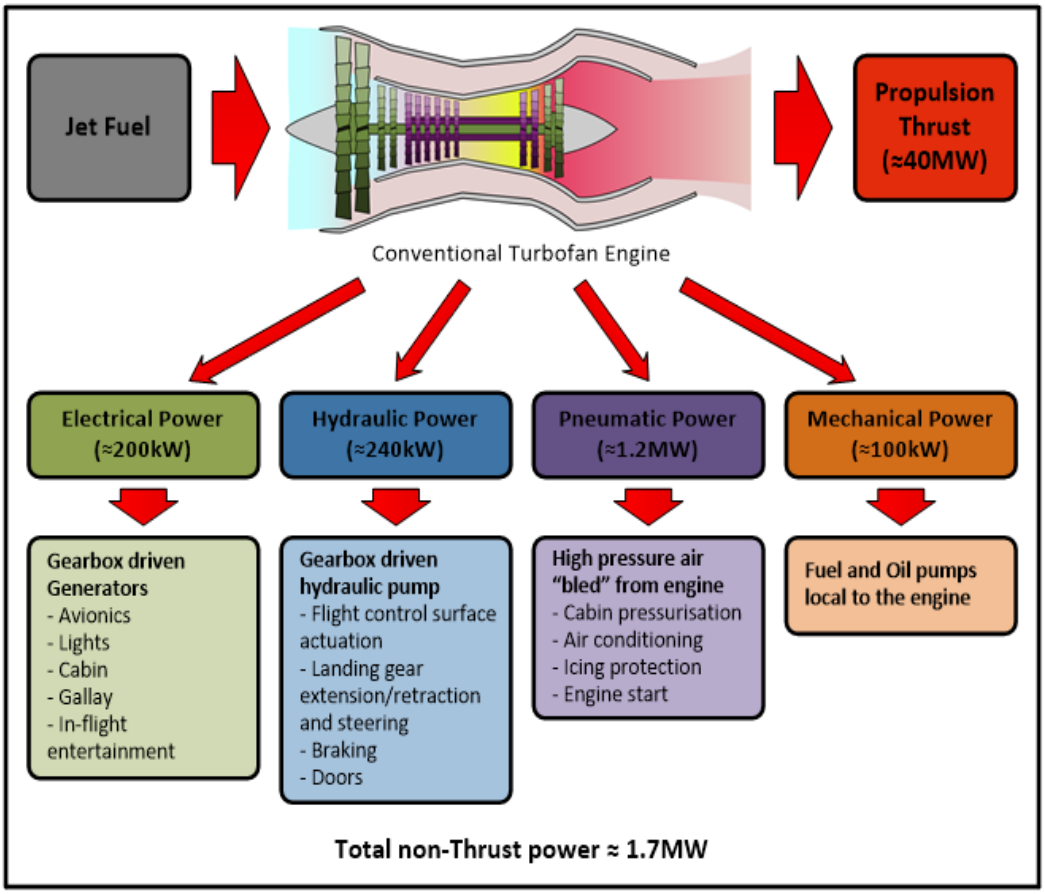


Figure 2.1: Conventional aircraft power architecture (Airbus A330)

Fig. 2.1 depicts the power architecture of a conventional aircraft as the Airbus A330 [21]. The on board power is generated by the turbine engines. The power can be divided into two parts: the primary power which provides the thrust (i.e. the majority of the power obtained from fuel combustion), and the secondary power which feeds all the on board systems. The secondary one can be divided into electrical power, pneumatic power, hydraulic power and mechanical power. The mechanical power derived from the turbine engine is utilized to drive fuel and oil pumps directly placed on the engine itself. The hydraulic power is used to operate the flight control surfaces, thanks to the possibility to obtain hydraulic actuators with high torque density and low volume. It is moreover used for the extraction/retraction of the landing

gears, for the breaking system, doors opening and closing and other minor actuators. Pneumatic power is obtained from bleed hot (200^oC) air taken directly from the high pressure turbine shaft and is used for cabin conditioning and pressurizing, as well as wings de-icing and engine starting. Electrical power is mainly generated by means of electrical generators driven from an accessory gearbox mounted on the gas turbines. A Constant Velocity Gearbox (CVG) connects the accessory gearbox with the generator, maintaining constant its speed and thus its fundamental electric frequency at 400 Hz [27, 28]. Electrical power is used for lights, avionics, on-board entertainment, fans, galley and other electrical loads. Beside the main Engine-Driven generator, an Auxiliary Power Unit (APU) driven generator is present, and meant to be used when the main generators fail. During ground operations, the subsystem can be connected to the airport facility grid or to a Ground Power Supply Unit (GPU). The final power architecture expected for the new MEA aircraft is depicted in Fig. 2.2 [21]. The bleed air taken from the engine for cabin pressurization and air conditioning, produces a considerable drop in engine efficiency, thus its complete removal is desirable. Moreover, the removal of the additional conduits required to connect the engine to the pneumatic subsystem, will lead to a considerable weight reduction and engine simplification.

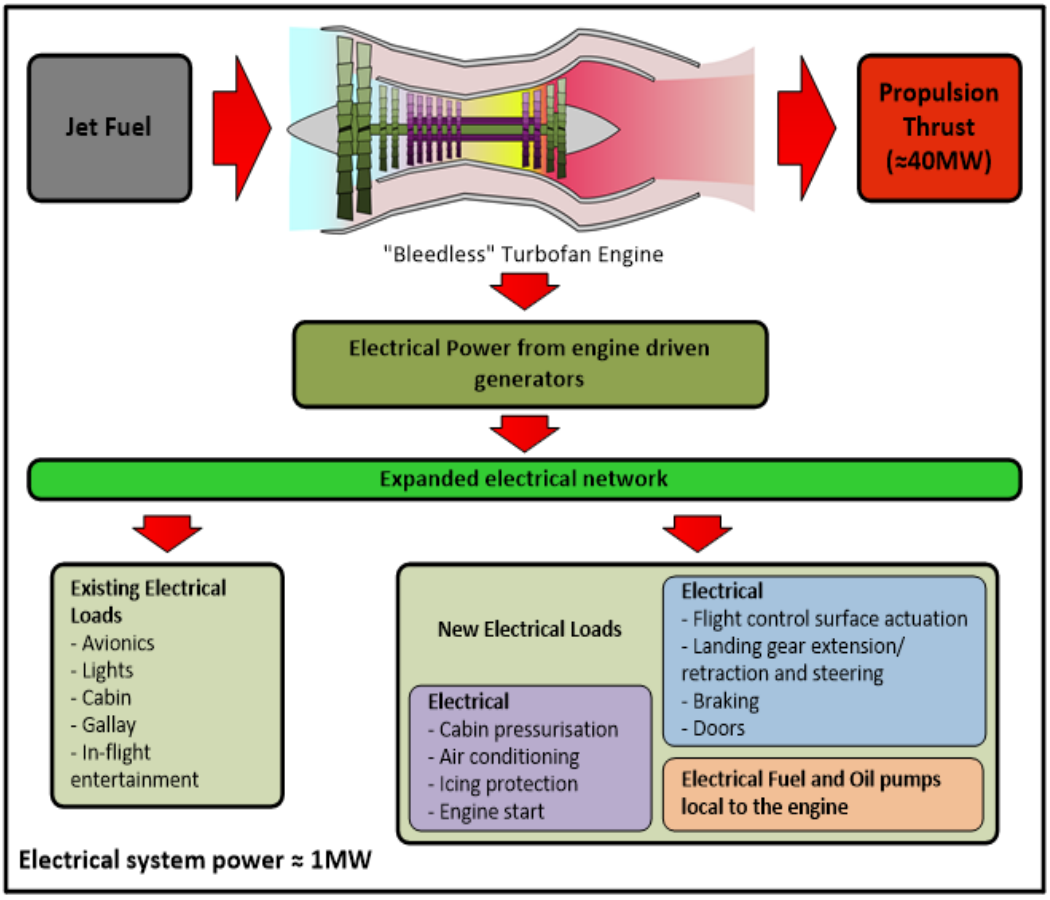


Figure 2.2: MEA aircraft power architecture

However, to obtain this result, new electrical systems would be required for cabin pressurization, conditioning, wings icing protection and engine starting. The hydraulic power distribution system is constituted by an intricate triple-redundant titanium pipes system which is also extremely rigid and heavy. The replacement of the hydraulic subsystem with its electrical equivalent is highly attractive and is one of the main objectives of the MEA initiative. The replacement of all the non-electric systems with their electric counterparts will result in a remarkable increase in the electrical power requirements, in terms of on-board power generating capability. In fact, if on conventional aircrafts as the Airbus A330 the on-board power generating capability is around 300kVA, for recently released MEA aircrafts this capability is raised to

around 600kVA, as in the case of the Airbus A380, and to around 1.5MVA for the Boeing 787 Dreamliner [21]. In particular the latter can actually be considered the most MEA civil aircraft in active service, hosting four 250kVA engine-driven and two 225kVA APU-driven PGU, in order to operate a wide range of new electrical on board utilities.

2.3.0.1 Topologies for the on-board Power Generation Unit

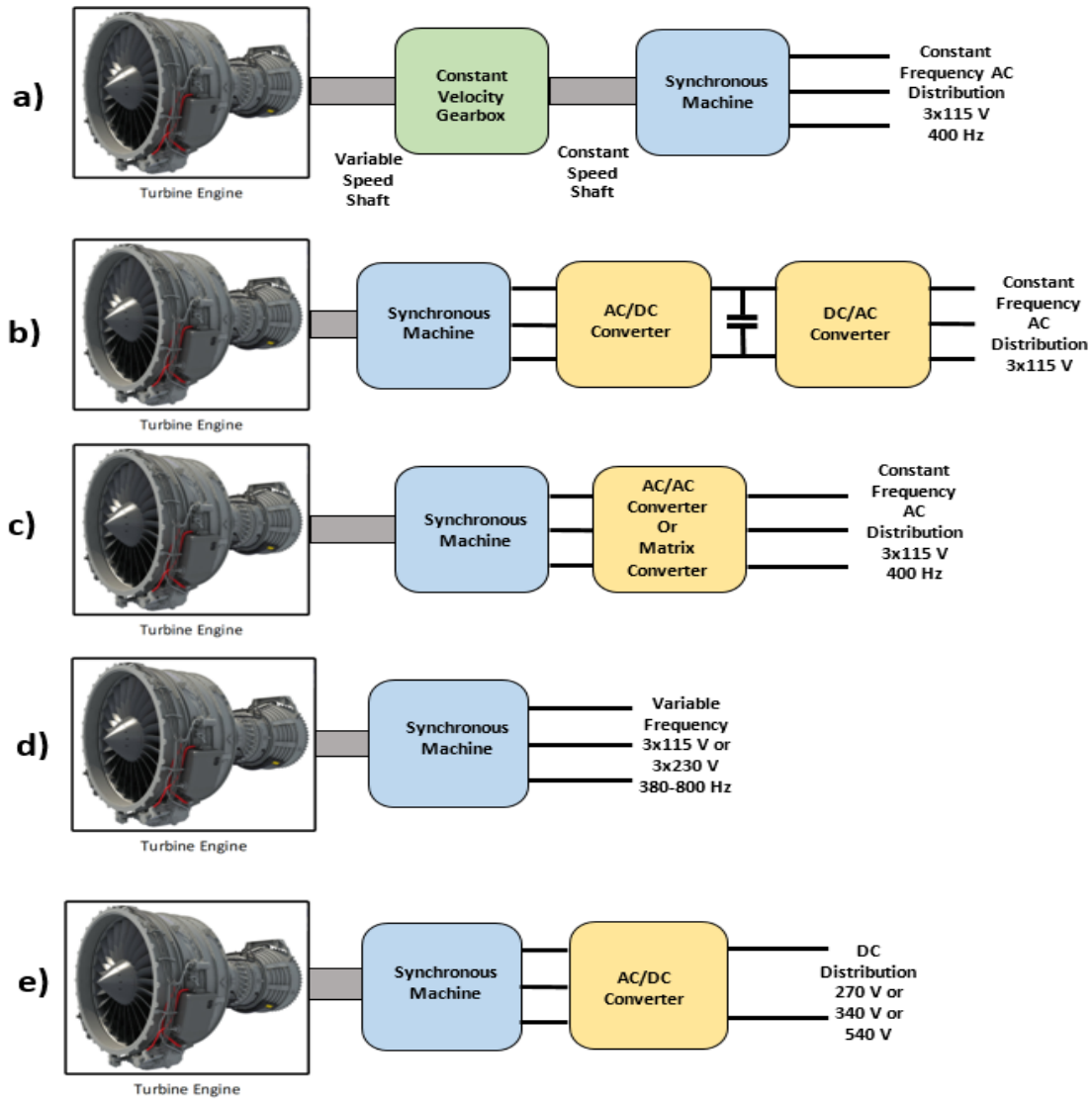


Figure 2.3: Possible architectures for the on board PGU.

Fig. 2.3 shows the possible architectures for the on board PGU. Fig. 2.3 a) shows the standard architecture composed by a three-stage regulated wound field synchronous generator with a PM exciter stage connected to the gas turbine engine shaft by means of a mechanical CVG which couples the variable speed engine to a constant-

speed shaft. The supplied voltage has constant frequency and amplitude, a three-phase 115V AC with 400 Hz frequency. A reduction in the weight of the system is obtained with an integration of the drive and the generator into a single unit. Fig. 2.3 b) shows the Variable-Speed Constant Frequency (VSCF) strategy [29]. With this topology there is a direct coupling between the generator and the gas engine shaft. A dc link is formed between the generator side and the AC loads using an AC/DC and a DC/AC power converter in back to back arrangement to provide the constant frequency voltage. Another possible arrangement consider the use of a Cycloconverter (AC/AC converter) or a Matrix Converter [30] as shown in Fig. 2.3 c). During the generating mode the aircraft engine, which has a variable speed, provides mechanical input power to the electric generator. The electric generator supplies a variable frequency AC power to the bi-directional power converter which provides constant frequency AC voltage to the main bus. In the motoring mode the constant frequency AC voltage system provides, input electric power to the machine, operating as a starter for the aircraft engine. The Variable Frequency (VF) strategy, also called Wild Frequency (WF) is shown in Fig. 2.3 d). The direct connection of the generator to the engine shaft leads to variable frequency voltage, typically in the range from 360 Hz to 800 Hz. For drive-type loads, as fans, pumps, actuating systems, this means the use of a local AC/DC DC/AC or AC/AC conversion. The VF system is diffused among civil aircrafts, while military ones often prefer a bidirectional AC/DC converter connected to the starter/generator in order to obtain a distribution system based on a constant voltage dc link (typically 270V, but also 350V or 540V depending on the aircraft model and capabilities [31]) as shown in Fig. 2.3 e). The constant dc link system uses only two wires and does not suffer of skin effect in conductors. Furthermore it allows for an easy paralleling of different PGUs and the integration of next generation energy storage devices. On the other hand, the main disadvantages when using high voltage dc links are the difficulties from protection and insulation. In fact, common and relatively inexpensive AC circuit breakers are not suitable for such a structure, and cables insulation needs to be chosen carefully. Since one of the main challenges for the aircraft industry is to reduce the overall system weight,

using a DC based distribution system is it possible to reduce this weight and reduce power losses [32]. An AC VF distribution system operating up to 800 Hz would require an increase of the conductors sections or the paralleling of smaller conductors to compensate for, or at least mitigate, the skin effect in addition to the necessity of using three cables, meaning a higher weight of the distribution system. Considering the power requirements trends already discussed in the previous paragraph, dc link buses up to 540V are getting more and more consideration as a means to provide the increased required powers, still maintaining a congruent weight for the distribution system also in civil aircrafts [33].

In [11,12,34] the evaluation of the performances of different power electronics topologies for the 100 KW - 150 KVA on board PGU has been carried out. The considered machine is a six poles PMSM, operating in a speed range of 7 to 33 krpm. Fig. 2.5 and Fig. 2.6 report the comparison results obtained from [11, 34], where different power electronics topologies have been compared in terms of efficiency and current THD. Based on the previous considerations and on the analysis based on the efficiency and phase current THD the topology that has been selected is the dual-inverter mixed technology with single dc link as shown in Fig. 2.4.

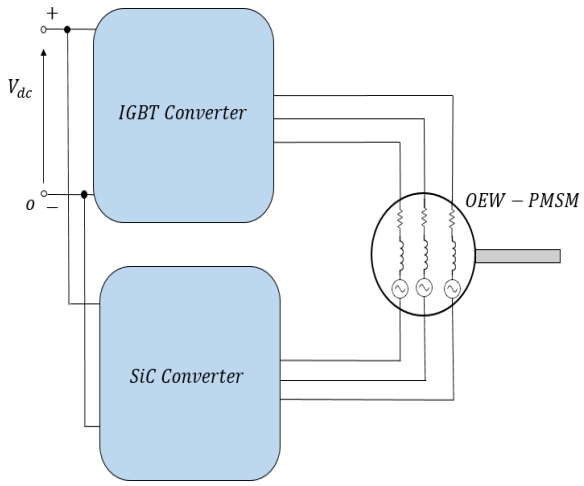


Figure 2.4: Mixed Technology Power Electronics for the OEW-PMSM Starter/Generator on-board PGU

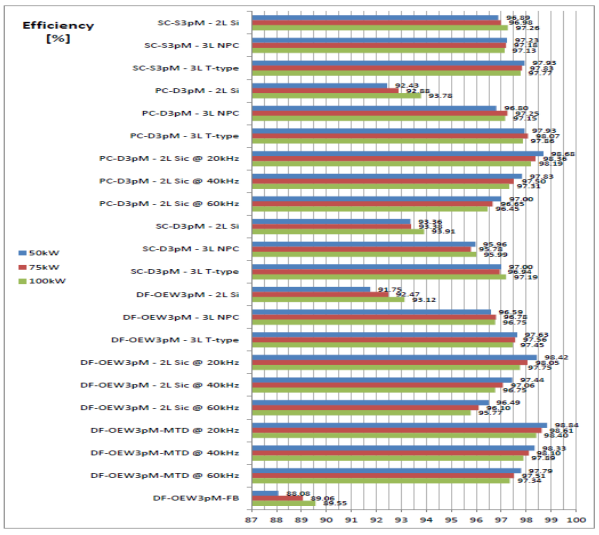


Figure 2.5: Comparison results: topologies efficiency at 50 kW (blue), 75 kW (red) and 100 kW (green)

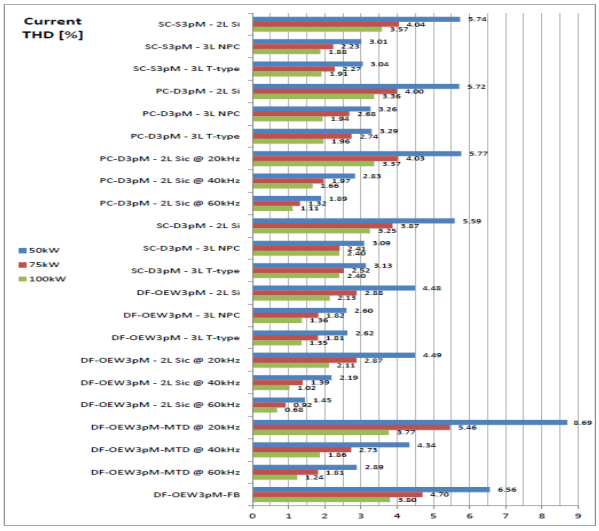


Figure 2.6: Comparison results: topologies current THD at 50 kW (blue), 75 kW (red) and 100 kW (green)

Supposing that the star centre of a standard PMSM can be opened six terminals are available to feed the machine. Therefore the benefits of the PMSM in conjunction with the OEW ones are obtained with a single configuration.

PMSMs offer several advantages in the field of variable-speed AC drives. They have higher efficiency, higher performance, compact construction and higher torque per volume ratio. Firstly, the field current needed for an induction machine is not necessary, and secondary copper loss does not occur in the rotor, therefore high efficiency can be achieved. Secondly, magnetic flux can be dense thanks to the use of rare earth magnets, and thus the overall motor size can be reduced. PMSMs gained continuous popularity because of the development of the high-energy PM materials over the past decades.

The OEWM fed by a dual-inverter allows to obtain multilevel effect on the output voltages equivalent to a three level converter, but using standard 2-level VSI. Another advantage consists in the phase voltage increase seen by the machine, in fact consid-

ering a set dc link voltage the phase voltage seen by each phase is double if compared to a standard 2-level VSI. High degree of fault tolerant capability is achieved since both a fault on one converter or on the machine can be handled. Furthermore, this topology is particularly suited for the simultaneous use of different power devices technologies (Si and SiC), which is going to be referred to as mixed technology. The most evident benefit is the potential massive losses reduction when SiC-based power modules are used in substitution of conventional IGBT power modules. The benefit is mostly obtained when the reduced switching losses obtained with the SiC devices are not cancelled by the higher switching frequency. In [11, 12, 34] the best efficiency and phase current THD are obtained when the IGBT converter is switched at the machine fundamental frequency and the SiC VSI is switching at 40 KHz. On the other hand the main problem of this topology is the flowing of additional ZSC due to the common dc link used to feed both the two-level VSIs. As widely discussed in [5, 16] the causes of a circulating ZSC can be attributed to ZSV generated by the converters, third harmonic component of the back EMF, devices' DTs and voltage drops. The circulation of additional currents reduces the overall system efficiency, therefore many works focused on VSCs' modulations to eliminate the zero-sequence component of the voltage supplied to the machine for both OEW induction machines [17,35] and OEW-PMSM. ZSC flowing due to the machine 3^{rd} harmonic back-EMF is also present in the system of Fig. 2.4. The magnitude of the ZSC depends on the equivalent ZSI, which is generally low [17, 18]. A small time constant of the zero-sequence circuit produces a high frequency, high intensity current ripple with the risk of harming the switching devices. Hence, particular attention needs to be given to the ZSI when a machine is operated in OEW configuration.

In the following sections the analysis of different power electronics topologies that allow to achieve multilevel inversion are presented. Among them the dual-inverter is analysed in detail and the proposed modulations in the literature to eliminate the ZSV are presented.

2.4 Overview of the Multilevel Inversion

This section presents an overview of the different possibilities to achieve multilevel inversion, Multilevel Converters (MLC) and the dual-inverter topology are considered. Explanation of the principles behind the multilevel inversion are given and advantages and disadvantages are evaluated.

Several multilevel converter topologies have been developed over the years [36, 37]. Increasing the voltage steps is a viable solution for increasing the voltage level of power converters as it was patented for the first time in 1971 [38]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. The use of multilevel power converter topologies improves output quality for a given switching frequency by tracking the sinusoidal reference more closely [39–41].

There are multiple applications of multilevel converters, for example water pumping stations [42], reactive power compensator [43], grid integration of renewable energy sources [44], steel rolling mills in metal industry and traction applications [45], fans in cement industry [46], pumps in the petrochemical industry [47], laminators, conveyors, blowers, compressors and others.

Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The topology of the power switches allows to use these multiple dc sources in order to achieve high voltage at the output. The rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. Previous solutions consisted in connecting in series or parallel multiple switching devices. In the case of series connection the possibility of shoot through of one device are particularly high because of the fact that perfect synchronisation of the turn on and turn off is almost impossible. Mod-

ular MLC are therefore preferred due to their ease of implementation. Multilevel converter technology is very attractive for medium to high voltage range (2-13kV) applications, which includes motor drive systems, power distribution, power quality and power conditioning applications. There are three main topologies of inverters that are commonly known as multilevel inverters, which are the Diode-Clamped or Neutral Point Clamped Multilevel Inverter (NPCMLI), the Flying Capacitor Multilevel Inverter (FCMLI) and the Cascaded H-bridge Multilevel Inverter. Along with these categories, there are number of derivative schemes which can be the combination of these categories [48]. Multilevel inversion can also be achieved using two inverters feeding both ends of the machine stator coils, whose star centre has been previously opened.

2.4.0.1 Principles of Multilevel Inversion

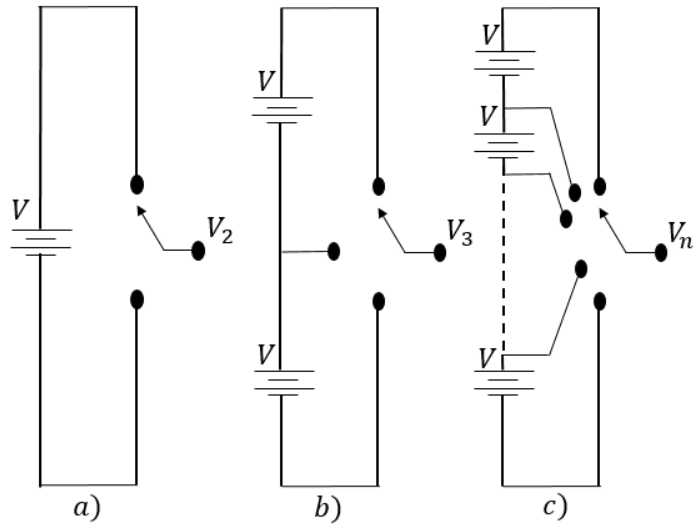


Figure 2.7: Inverter phases. a) 2-level inverter, b) 3-level inverter, c) n-level inverter

Fig. 2.7 a) shows a single leg of a 2-level converter. An ideal dc source V and an ideal switch are considered. The voltage output can be either V or 0. In Fig. 2.7

b) a 3-level converter's leg is presented, the dc supply is split into two units of value V. The output voltage can assume the values 0, V and 2V. In Fig. 2.7 c) a n-level leg is introduced which can generate a voltage output of n-levels. Some assumptions have been implicitly made. In particular, it is considered that the dc voltage sources have the same value and are series connected. In practice the voltage levels can be different. A three-phase inverter composed by n-level legs will be considered for the analysis which leads to n output voltage levels for the phase-to-neutral voltage. The number j of the line-to-line voltage levels is given by (2.1).

$$j = 2n - 1 \tag{2.1}$$

The higher the number of levels the better is the quality of the output voltage which is generated by a greater number of steps with a better approximation of a sinusoidal wave. So, increasing the number of levels gives a benefit to the harmonic distortion of the generated voltage, but a more complex control system is required, with the respect to the 2-level inverter. MLC are characterised by the possibility of having different switching combinations which give the same output voltage. Two or more switching states that produce the same output voltage are called redundant states. The MLC has many advantages when compared to a standard two-level VSC. The MLC provides higher voltage capability, reduction of input and output harmonic content, lower switching losses, higher amplitude fundamental and lower dv/dt. The main disadvantages of MLC include the larger number of switching semiconductors required, difficulties with capacitor voltage balancing, unequal current stresses, and higher implementation cost.

2.4.0.2 Cascaded H-bridge Multilevel Inverter

Fig. 2.8 shows a m level single phase cascaded H-bridge converter. This is one of the simplest cascade converter solutions and provides modularity which reduces the

cost of commissioning and maintenance as well as introducing some fault tolerant capacity [49, 50]. Among the applications where this topology can be found there are STATCOM [51] and applications where independent voltage sources are inherent such as photovoltaic (PV) power applications and grid connected battery storage systems [52, 53].

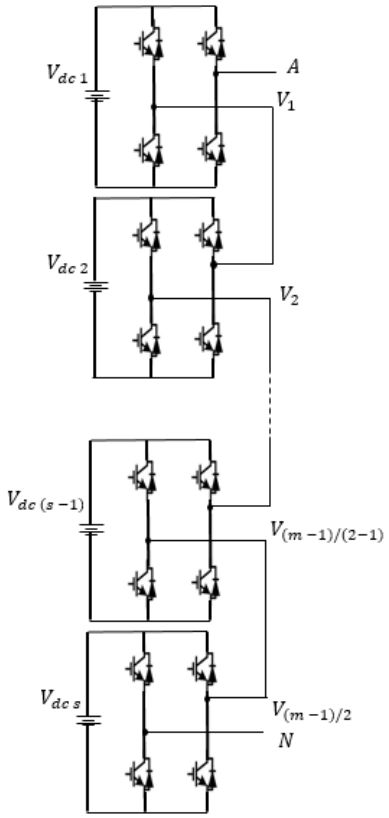


Figure 2.8: Single phase m level cascaded H-bridge

The main disadvantage of this converter configuration is the necessity of separate dc voltage sources for each H-bridge which leads to increased costs and weights. On the other hand the topology is composed of commercialised and reliable parts making implementation easier.

2.4.0.3 Flying Capacitor Multilevel Inverter

Fig. 2.9 shows a 3-level flying capacitor converter. The 3-level topology requires two capacitors to split the input dc voltage plus three other capacitors are needed as clamping capacitors. Each leg can produce three voltage levels as $\frac{V_{dc}}{2}$, 0, and $\frac{-V_{dc}}{2}$. The flying capacitor topology does not require separate voltage sources and it has multiple switching states for balancing of the voltage levels. The increased number of capacitors makes the converter costly and bulky. Most of the research work done on this configuration has focused on understanding the natural balancing behaviour that maintains the correct capacitor voltages [54–56].

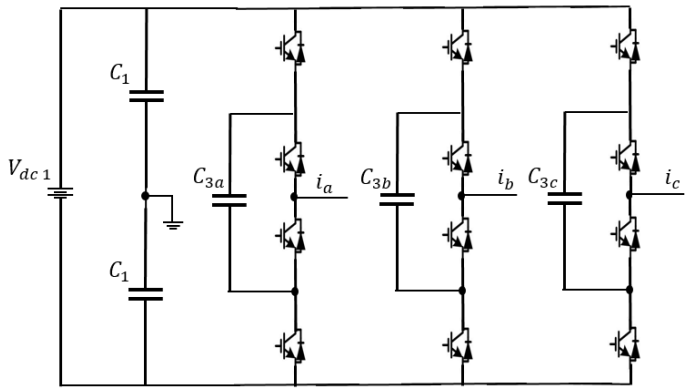


Figure 2.9: Three phase Capacitor Clamped Multilevel Inverter

2.4.0.4 N-level Neutral Point Clamped Inverter

Neutral point clamped inverters are also known as Diode clamped inverter. This MLC is the most widely multilevel inverter used in all types of industrial applications [57]. Fig. 2.10 shows a 3-level inverter NPC. The circuit consists of two series capacitors to divide the voltage of the dc source into smaller voltages. The main disadvantage of this converter is the large number of clamping diodes required with the increase of voltage levels. On the other hand only one dc bus is needed. The high losses and

their uneven distribution in the switching devices makes this topology less attractive for high number of levels [58]. Regarding this topology most of the research focused on overcoming the problem of maintaining an equal split in the dc link voltage ratio over the dc link capacitors. In fact the voltage vectors that connect the phase to the neutral point of the converter cause the dc link capacitors to charge or discharge. The majority of the neutral point voltage balancing schemes used in SVM relies on some form of manipulation of the voltage vectors in a pair that causes both charge and discharge of the capacitors, where the relative duration of positive and negative vectors in a pair is usually adjusted in order to compensate for the error in neutral point. The flow of the load current can cause unbalance especially during transients or unbalanced operation. In [59] the balancing of the neutral point is modelled for a full operating range of the converter. Other methods for balancing the neutral point are proposed in [60, 61].

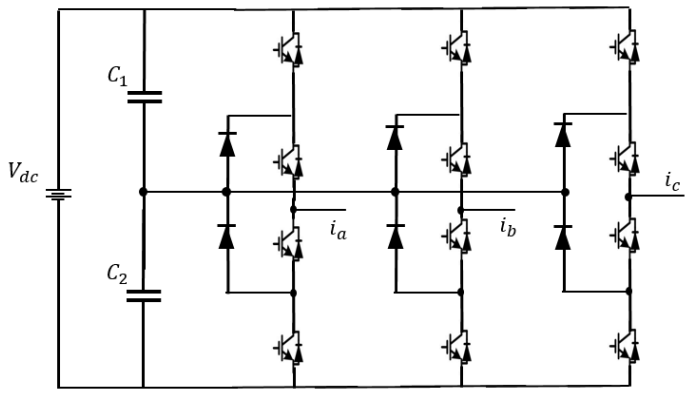


Figure 2.10: Three phase 3-level neutral point clamped inverter

2.4.1 Dual-Inverter Converter as a Multilevel Converter

In 1993 Stemmler and Guggenbach [2] proposed the dual two-level converter as a viable solution to obtain the same voltage output of a three-level converter. Any three phase load which has both terminals for each phase available can be supplied

by the dual-inverter configuration. The dual-inverter can be fed by different topologies for the dc link: a single dc supply in series or parallel configuration, two separate dc sources or a dc source and a floating capacitor. Independently of the topology used for the dc source, what made this system of particular interest is the possibility of using reliable, well known and available components, such as the standard two-level converters, to realise a more complex converter architecture. Each single two-level VSC can provide 8 different voltage vectors that lead, for the dual fed architecture, to 64 possible voltage states. The same configuration of the voltage vectors produced by a three-level converter is obtained, furthermore the increment of the voltage levels if compared to a standard two-level inverter leads to a better output voltage profile. The dual fed configuration is also able to provide high redundancy for the voltage vectors and there is no need to enforce voltage balancing in the neutral point. Furthermore this topology allows for a better exploitation of the dc link voltage. Compared to the single inverter topology, each phase of the three phase load sees the full dc link voltage instead of half as in a standard 2 level VSC. The dual-inverter topology allows to work with half of the rated power when one single inverter completely fails [3, 4]. The inverter that sustains the fault needs to be short circuited on the three-phase terminal for current circulation. As an example, if one converter fails, the motor can be operated at the rated current (that means rated torque) up to the half of the rated voltage (that means half of the rated speed). In recent years dual fed drives have attracted a growing interest from research and industry. The dual-fed OEW configuration has found a wide range of applications such as wind power generation [5,6], electric vehicles [7,8], high power electric propulsion [9] and aircraft starter-generator systems [10,11]. Two isolated dc power supplies [13], one dc supply and a floating bridge [62] or a single dc supply can be adopted for the dual-fed OEW.

The standard solution for industrial electric drives nowadays is the 2 level VSC feeding an induction motor. Safety reasons impose to use dc link voltages lower than 100 V, which leads to practical problems when realising drives of power ratings higher than 20 kW due to the high costs of the switching devices that need to carry high

intensity currents. In EV one solution is to divide the battery pack and use it to feed both converters or for HEV both the converters can be supplied with two separate generators, thus no isolation transformer will be required [63]. Other possible applications of the dual-inverter are grid connected photovoltaic applications. The two two-level VSI are fed from two separate PV arrays. An OEW transformer is used to connect to the dual-inverter on one side and to the grid on the other [64–67]. Other applications of the dual-inverter topology in the aerospace field are the three-phase ground power unit supply for aircraft servicing [68] and the Starter/Generator system for aircraft applications [11,12]. The dual three phase two-level inverter topology achieves multilevel output voltage waveforms and has received research attention due to the simplicity of the power stage. The circuit implementation requires fewer capacitors than the flying capacitor topology, fewer isolated supply than a three phase H-bridge converter and it requires fewer diodes than the three-level NPC converter. The major drawbacks of this converter topology depend mostly on the arrangement that is chosen for the dc link. If a single voltage source is adopted, the common mode current will flow through the system. Therefore often isolated supplies are used, increasing size, weight and losses of the system. When asymmetric voltage source operation is used, one of the main issues is the complexity of the modulation that needs to be implemented taking also into account that the lower voltage converter can overcharge.

2.5 Dual-Inverter dc link Topologies

As previously mentioned, different dc link topologies for the dual-inverter configuration can be adopted. Here the state of the art of each configuration is presented.

2.5.1 Dual level Inverter with Separate Voltage Sources

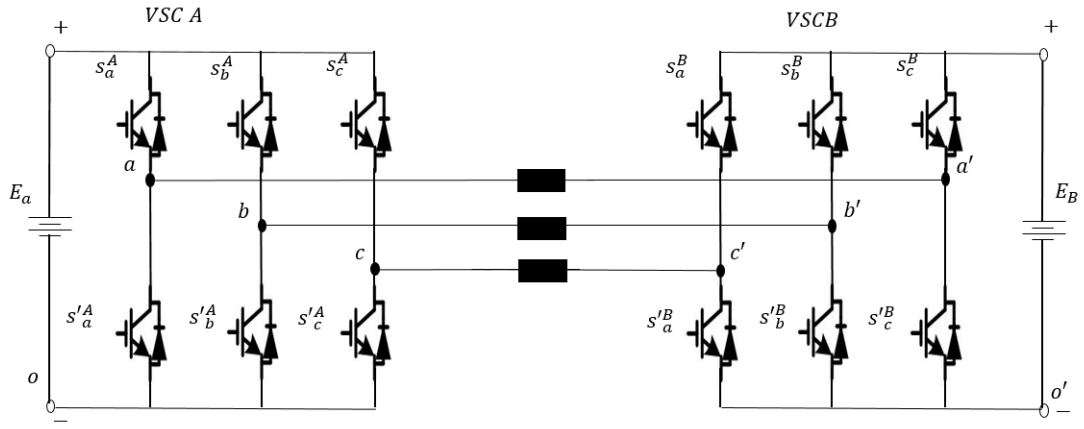


Figure 2.11: Dual Inverter topology with separate dc sources.

As shown in [63,69] one of the main features offered by the separate dc links topology is the capability to regulate the load power sharing between the two dc sources within the switching period. This means that it is possible to balance exactly the power flow from the two sources, or to unbalance the power flow in order to restore the same state of charge of two battery banks. Some interesting features of the topology can be studied when the ratio between the two voltage sources E_A and E_B is not equal to 1. It is intuitive to think that different ratios of the source voltages lead to different space vector diagrams. Common ratios used are $E_B = 0.5E_A$, $E_B = 2E_A$ and $E_B = 3E_A$. The dual inverter offers, therefore, a method of increasing the voltage to the motor [70]. The dual inverter with a dc link voltage ratio of 2:1 can achieve multilevel inversion similar to a traditional four-level converter topology [71]. The voltage levels can be increased by increasing the dc link voltage ratio to 3:1, but this will increase the complexity of modulation techniques due to uneven distribution of voltage vectors.

In [72] an induction motor drive powered by a dual inverter where VSC A and VSC B are fed from two isolated supply voltages of $\frac{2}{3}V_{dc}$ and $\frac{1}{3}V_{dc}$ respectively is considered. A

regenerative dc link supply or one with dynamic breaking is needed for this topology, otherwise the high voltage converter can over charge the dc link capacitor of the lower converter in some space phasor combinations in PWM operation. In [48] an accurate description of how to implement a Space-vector based PWM switching strategy for the dual Inverter drive with separate dc link is shown. To implement the PWM pattern, the criteria of how to identify the the triangular sector in which the tip of the reference space-vector is situated is presented and the sub-hexagon to which it belongs is found. In [73] the Space Vector PWM (SVPWM) with phase shift of the carrier is introduced studying its effect on the phase voltage THD.

The presence of two insulated dc supplies allows to maximize the output voltage avoiding the common mode impedance. This multilevel converter presents some advantages: no generation of common mode (zero sequence) currents in the motor winding, best dc bus voltage utilization, use of two standard three-phase two-level inverters. On the other hand the dual inverter topology with separate dc links has the disadvantage of being less practical and more expensive. Two separate dc sources must be available and often they are obtained by means of separate isolated voltage transformers. For EV applications, having on board two separate batteries is not convenient for obvious reasons such as weight and costs.

2.5.2 Dual-Inverter with a Single Voltage Source and a Floating Capacitor

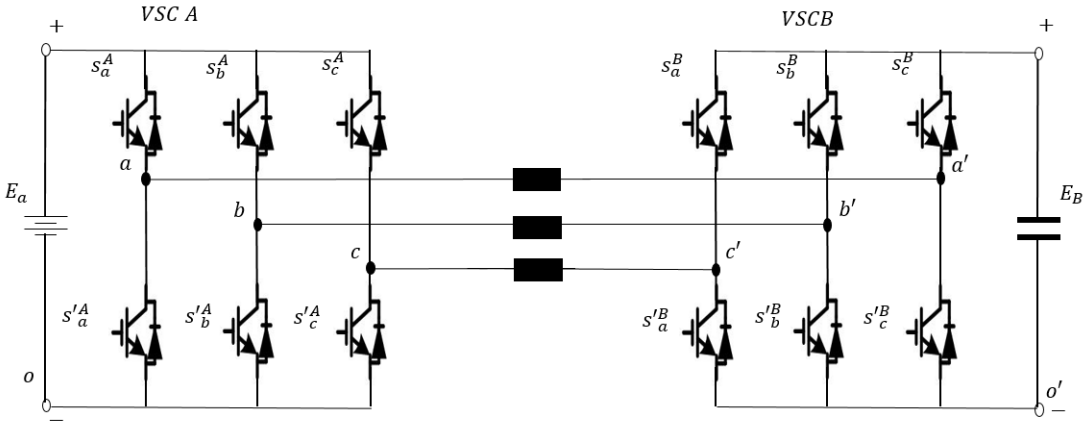


Figure 2.12: Dual Inverter topology with Floating Capacitor.

The dual inverter with a floating capacitor shown in Fig. 2.12 has been intensely investigated in the literature [14, 74–78] because of its many advantages and applications such as EV and naval propulsion. As the dual inverter topology with separate dc sources, the one with the floating capacitor does not allow for the ZSC to flow in the system [74, 75]. In EV applications often a dc-dc converter is used before the inverter that feeds the electrical motor to have a voltage boost; the dual inverter with floating capacitor can provide the boost allowing for a reduction in costs and weights [79]. Furthermore, the converter connected to the floating capacitor can be used to feed to the machine the required reactive power by controlling the VSC B capacitor voltage. It is therefore possible to allow VSC A to work at unity power factor [14,74,75]. In the high speed region, the reactive voltage requested by the machine increases with the speed, therefore a significant part of the stator voltage supplied to the machine is used exclusively to feed the reactive power needed, therefore making it hard to produce torque. Using the VSC connected to the floating capacitor to provide for the reactive power, the primary inverter reserves more voltage to extend the operating speed. The

final objective of this topology is to increase the operation speed range. The floating capacitor dual inverter topology has been studied also with the intention to increase the constant torque region of the machine [79]. As seen for the dual inverter structure with separate dc links also in the one with a floating capacitor the dc sources can be operated with different voltages $\frac{E_A}{E_B}$ ratios. In [80] it is shown that in induction motors it is possible to improve the efficiency of the open-ended drive by controlling the dc link voltage of the floating bridge depending on the operating conditions. In fact, since the rise in the converter losses is a drawback of the dual inverter topology, [80] investigates the efficiency improvement resulting from a variable voltage across the dc link of the floating bridge. A dual inverter with a floating capacitor feeding a PMSM is resented in [78]. The floating bridge inverter is used to compensate the reactive power of the main inverter and, hence, to maximize the active power delivered to the motor in compliance with the current and voltage constraints.

For the VSC B the direct component of the voltage is used to control the floating capacitor voltage, while the quadrature component to achieve the compensation of the reactive power requested by the PMSM to the VSC A, i.e. the one connected to the main supply. The voltage of VSC A is instead used to achieve the speed and current control of the PMSM.

2.5.3 Dual-Inverter with a Common Voltage Source

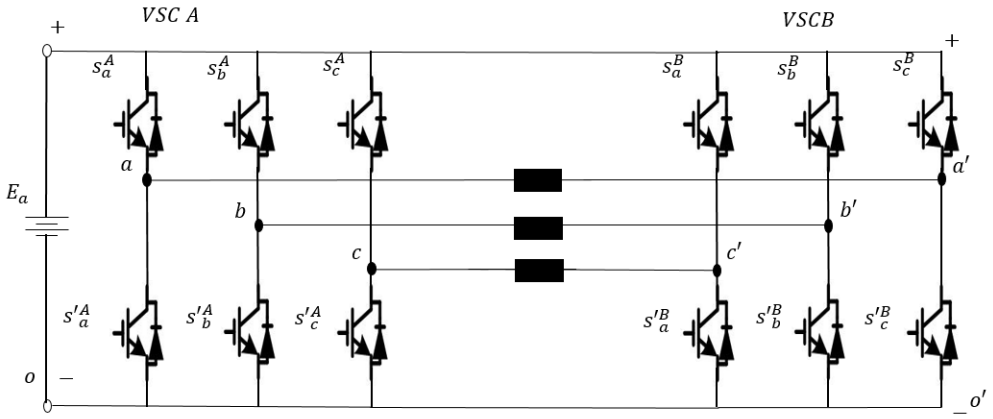


Figure 2.13: Schematic of Dual Inverter topology with Common dc link.

While on one hand the common dc link configuration significantly simplifies and reduces the costs of the topology, on the other hand it allows the ZSC to flow freely in the system. The possibility of reducing significantly the costs and weights of the converter topology and simplifying its structure are the main reasons why this configuration has attracted so much attention in the research community. The huge drawback of circulating currents is therefore the main issue to the real feasibility of the common dc link architecture. The dual-fed OEW configuration has found a wide range of applications such as pumping applications [81], wind power generation [5,6], electric vehicles [7,8], high power electric propulsion [9] and aircraft starter-generator systems [10, 11].

The problem of circulating ZSC has been investigated in [5, 16] where the authors focus on the causes of circulating currents from the converter point of view. When considering the circulation of ZSC in the system if the load is a PMSM particular, attention has to be given also to the back-EMF of the machine. In fact if the PMSM is obtained from a star connected machine, most probably when the stator windings would be opened a third harmonic component would be present and would cause the

circulation of a third harmonic ZSC [82]. In the following sections the ZSV produced by the two two-level VSCs is analysed by studying the voltage space vector synthesized by the individual converters and by both of them as if they were a single converter. Previous research work done to eliminate or attenuate the problem of ZSV and bearing currents in standard two-level PWM modulated VSI motor drives is discussed. In fact the solutions proposed for the standard two-level converter can be extended to the dual-inverter topology to eliminate the ZSV produced. Different PWM and SVM modulation techniques for ZSV reduction in the dual-inverter topology with single dc link are then presented. In order to evaluate completely the ZSC behaviour, the voltage non-linearities produced by the VSCs need also to be taken into account. The two major non-linearities that cause the circulation of ZSV are the semiconductor devices voltage drops and the switch DT used for shoot-through current protection.

2.6 Voltage Space Vectors Analysis of the Dual-Inverter Topology

In the previous sections, the open-end configuration has been briefly introduced mentioning its benefits and limits. In this topology, two standard three phase 2-level inverters are connected at both ends of the windings of the machine. The space voltage vectors configuration created is similar to those of 3-level inverter topologies. The dual converter used to supply the OEWM can be seen as two separate and identical 2-level VSCs, so it is important to visualize the modulation of a single VSC. By the principle of superposition the output voltage vectors for the dual 2-level converter can then be obtained. Therefore particular attention is given to the voltage space vector distribution of the single 2-level VSC.

2.6.1 Two-Level Inverter Voltage Space Vector Representation

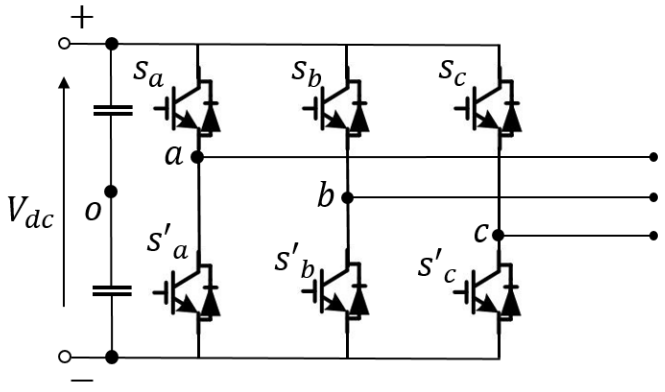


Figure 2.14: Standard two-level VSC.

Considering Fig. 2.14 each switch can be either open or close, the upper and lower switches of the same leg can never be turned on at the same time to avoid the leg short circuit over the dc supply. The inverter leg state is uniquely identified by the upper power switch state, therefore the identification of the upper leg switch state is sufficient to determine the lower switch state too. The switch state can assume the values -1 or 1 if open or close respectively and it is identified by s_x where the subscript x identifies the converter leg, which for the three phase systems considered can be either a, b or c. If the apex ' is present then the state considered is the one of the lower device on the converter's leg. Since there are three legs and each upper leg switch can assume two values there are $2^3 = 8$ possible inverter output voltages. Each voltage state is identified with 3 digits, each of them representing one of the converter's legs from a to c. Each leg voltage can be written as a function of the upper switch state as

$$\begin{cases} v_{ao} = \frac{V_{dc}}{2} s_a \\ v_{bo} = \frac{V_{dc}}{2} s_b \\ v_{co} = \frac{V_{dc}}{2} s_c \end{cases} \tag{2.2}$$

Table 2.1 shows the 8 possible switching states for the 2-level VSC and the leg phase voltages. By means of Clark transform (Appendix A) the phase voltages can be transformed into fixed reference frame obtaining the $\alpha\beta 0$ voltages. Table 2.2 shows the 8 possible switching states for the 2-level VSC and the normalised $\alpha\beta 0$ voltages with respect to the dc link voltage V_{dc}. The representation of the voltage vector as a complex number is obtained applying (2.3).

$$\overline{V}_s = V_{ao} + V_{bo} e^{j\frac{2\pi}{3}} + V_{co} e^{j\frac{4\pi}{3}} \tag{2.3}$$

There are 8 possible voltage output vectors of which 6 are active while 2 are the so called zero vectors V0 (000) and V7 (111). When the zero vectors are applied, there is no power flow between source and load and the load current free-wheels through the inverter. On the $\alpha\beta$ plane the null vectors are vectors of length zero placed in the axis origin.

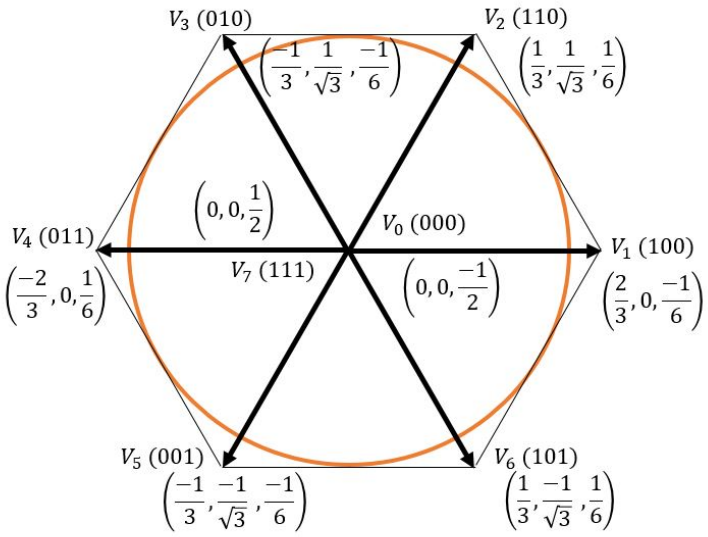


Figure 2.15: Space Voltage Vectors of the 2-level VSC in the $\alpha\beta$ plane.

Fig. 2.15 shows the voltage vectors for the standard 2-level VSC on the $\alpha\beta$ plane. The vertices of the six active voltage vectors form an hexagon centred at the origin of the plane and divide the plane into six 60^o sectors. The ZSV of the standard two-level VSC for each voltage vector is shown in 2.2 and it can be calculated using the transformation matrix to the stationary reference frame. The maximum dc link voltage utilization can be obtained with the third harmonic injection, which corresponds to the voltage limit identified by the circle of radius $\frac{V_{dc}}{\sqrt{3}}$ in the $\alpha\beta$ plane.

Table 2.1: Standard 2-level VSC Voltage Vectors, gate signals and phase voltages

Voltage Vector	Gate Signals	V_{ao}	V_{bo}	V_{co}
V_0	[0 0 0]	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
V_1	[1 0 0]	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
V_2	[1 1 0]	$V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$
V_3	[0 1 0]	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$
V_4	[0 1 1]	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
V_5	[0 0 1]	$-V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$
V_6	[1 0 1]	$\frac{V_{dc}}{2}$	$-V_{dc}/2$	$V_{dc}/2$
V_7	[1 1 1]	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

Table 2.2: Standard 2-level VSC Voltage Vectors, gate signals and normalised $\alpha\beta 0$ voltages

Voltage Vector	Gate Signals	V_α	V_β	V_0
V_0	[0 0 0]	0	0	$-1/2$
V_1	[1 0 0]	$2/3$	0	$-1/6$
V_2	[1 1 0]	$1/3$	$1/\sqrt{3}$	$1/6$
V_3	[0 1 0]	$-1/3$	$1/\sqrt{3}$	$-1/6$
V_4	[0 1 1]	$-2/3$	0	$1/6$
V_5	[0 0 1]	$-1/3$	$-1/\sqrt{3}$	$-1/6$
V_6	[1 0 1]	$1/3$	$-1/\sqrt{3}$	$1/6$
V_7	[1 1 1]	0	0	$1/2$

2.6.2 Dual 2-Level Inverter Voltage Vectors Representation

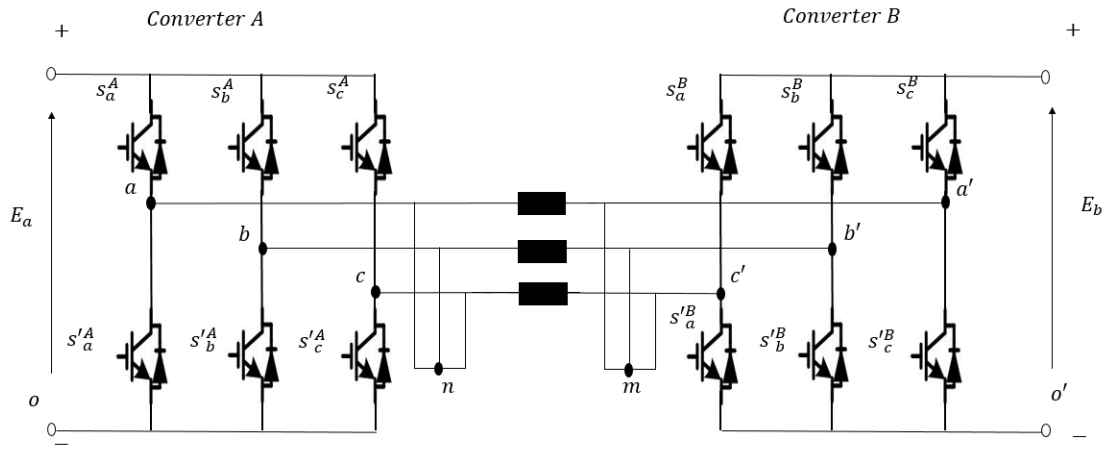


Figure 2.16: Dual Inverter topology with a general three-phase load.

Fig. 2.16 shows the structure of a dual 2-level VSC with a generic three-phase load connected to it. The converter arrangement also has good dc link voltage utilisation and therefore reduces the blocking voltage requirement for the power semiconductor devices in a similar way to a multilevel converter. The analysis of the dual 2-Level Inverter can be carried out considering two separate and independent standard 2-level VSCs. The dual 2-level inverter utilises twelve switching semiconductor devices (usually IGBTs or MOSFETs), driven dually in couples to avoid the dc source short circuit, and twelve anti parallel diodes. The general case of two different dc supplies E_A, E_B for the two VSCs is considered. Each converter's switch is identified by its state s_k^h, which indicates the switching state of the inverter leg and it can be equal to 1 if the switch device on the upper bridge turns on or 0 if the switch device turns off. It is therefore possible to identify the state of the inverter leg exclusively by the state of the upper switch. Subscript k indicates the phase while superscript h stands for the VSC A when equal to A or the VSC B when equal to B. As seen in Section 2.6.1 the single VSC is able to produce 8 different voltage vectors. For the dual 2-level VSC there are 6 legs corresponding to a number N_v of voltage vectors where

$$N_v = 2^3 * 2^3 = 2^6 = 64 \tag{2.4}$$

The relationship between the converter phase voltages and the leg's states can be deduced by looking at Fig. 2.16. Two imaginary star centres named n and m can be placed at both sides of the load. The phase voltages v_{an}, v_{bn} and v_{cn} can be expressed as

$$\begin{cases} v_{an} = \frac{1}{3}[2v_{ao} - v_{bo} - v_{co}] \\ v_{bn} = \frac{1}{3}[-v_{ao} + 2v_{bo} - v_{co}] \\ v_{cn} = \frac{1}{3}[-v_{ao} - v_{bo} + 2v_{co}] \end{cases} \tag{2.5}$$

considering the switching states s_k^h (2.5) can be written as

$$\begin{cases} v_{an} = \frac{1}{3}E_a[2s_a^A - s_b^A - s_c^A] \\ v_{bn} = \frac{1}{3}E_a[-s_a^A + 2s_b^A - s_c^A] \\ v_{cn} = \frac{1}{3}E_a[-s_a^A - s_b^A + 2s_c^A] \end{cases} \tag{2.6}$$

The same relationship can be written for the voltages of the second inverter B as

$$\begin{cases} v_{a'm} = \frac{1}{3}[2v_{a'o'} - v_{b'o'} - v_{c'o'}] \\ v_{b'm} = \frac{1}{3}[-v_{a'o'} + 2v_{b'o'} - v_{c'o'}] \\ v_{c'm} = \frac{1}{3}[-v_{a'o'} - v_{b'o'} + 2v_{c'o'}] \end{cases} \tag{2.7}$$

which again can be written considering the switching states s_k^h obtaining (2.8)

$$\begin{cases} v_{a'm} = \frac{1}{3}E_b[2s^B_{a'} - s^B_{b'} - s^B_{c'}] \\ v_{b'm} = \frac{1}{3}E_b[-s^B_{a'} + 2s^B_{b'} - s^B_{c'}] \\ v_{c'm} = \frac{1}{3}E_b[-s^B_{a'} - s^B_{b'} + 2s^B_{c'}] \end{cases} \tag{2.8}$$

Finally the phase voltages of the OEW load can be written as the difference of the output voltages of the two two-level VSCs

$$\overline{V}_{OEW} = \overline{V}_A - \overline{V}_B \tag{2.9}$$

Where $\overline{V}_{OEW}$, $\overline{V}_A$ and $\overline{V}_B$ are respectively the OEW load phase voltages, the output phase voltages of VSC A and VSC B. The voltages are all column vector of dimension 3x1 as shown in (2.10).

$$\overline{V}_{OEW} = \begin{bmatrix} v_{aa'} \\ v_{bb'} \\ v_{cc'} \end{bmatrix} ; \ \overline{V}_A = \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} ; \ \overline{V}_B = \begin{bmatrix} v_{a'm} \\ v_{b'm} \\ v_{c'm} \end{bmatrix} ; \tag{2.10}$$

By substituting (2.5) and (2.7) in (2.9) the following system is obtained

$$\begin{cases} v_{aa'} = \frac{1}{3}[2(v_{ao} - v_{a'o'}) - (v_{bo} - v_{b'o'}) - (v_{co} - v_{c'o'})] \\ v_{bb'} = \frac{1}{3}[-(v_{ao} - v_{a'o'}) + 2(v_{bo} - v_{b'o'}) - (v_{co} - v_{c'o'})] \\ v_{cc'} = \frac{1}{3}[-(v_{ao} - v_{a'o'}) - (v_{bo} - v_{b'o'}) + 2(v_{co} - v_{c'o'})] \end{cases} \tag{2.11}$$

(2.11) can be rearranged in a matrix form for simplicity as done below

$$\overline{V}_{OEW} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} - \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{a'o'} \\ v_{b'o'} \\ v_{c'o'} \end{bmatrix} \tag{2.12}$$

The ZSV between the two two-level VSCs is identified by the voltage v_{nm} which can be different from zero due to an unbalanced load. Its expression is presented in (2.13)

$$v_{nm} = \frac{1}{3}(v_{an} + v_{bn} + v_{cn}) - \frac{1}{3}(v_{a'm} + v_{b'm} + v_{c'm}) \tag{2.13}$$

As it will explained in detail the ZSV is produced by the two VSC according to which voltage state is selected. On the other hand, the ZSC can flow exclusively if it exists a path for its circulation, i.e. when a single dc link supply is used for both the VSCs.

The relationship between the dual converter output voltages and the leg switches states is now presented. The load phase voltages can be written in the following form applying Kirchhoffs Voltage Law (KVL) to Fig. 2.16

$$\begin{cases} v_{aa'} = v_{ao} - v_{a'o'} + v_{oo'} \\ v_{bb'} = v_{bo} - v_{b'o'} + v_{oo'} \\ v_{cc'} = v_{co} - v_{c'o'} + v_{oo'} \end{cases} \tag{2.14}$$

If a single dc supply is used to feed the two VSCs the voltage between the negative poles o and o' is zero and (2.14) becomes

$$\begin{cases} v_{aa'} = v_{ao} - v_{a'o} \\ v_{bb'} = v_{bo} - v_{b'o} \\ v_{cc'} = v_{co} - v_{c'o} \end{cases} \tag{2.15}$$

2.6.3 $\alpha\beta$ Plane Voltage Vectors Diagram for the Dual 2-Level Inverter

The analysis of the voltage vectors of the dual two-level converter is carried out in detail in [1] where the different switching states are reported. The voltage vectors for the dual inverter can be derived considering that it can be seen as two separate and independent standard VSCs. It can be seen from (2.9) that the output voltages $\overline{V}_B$ oppose the voltages $\overline{V}_A$. This opposition of the pole voltages of inverter B can be taken into account for simplicity into the the vector diagram of the VSC B as shown in Fig. 2.17

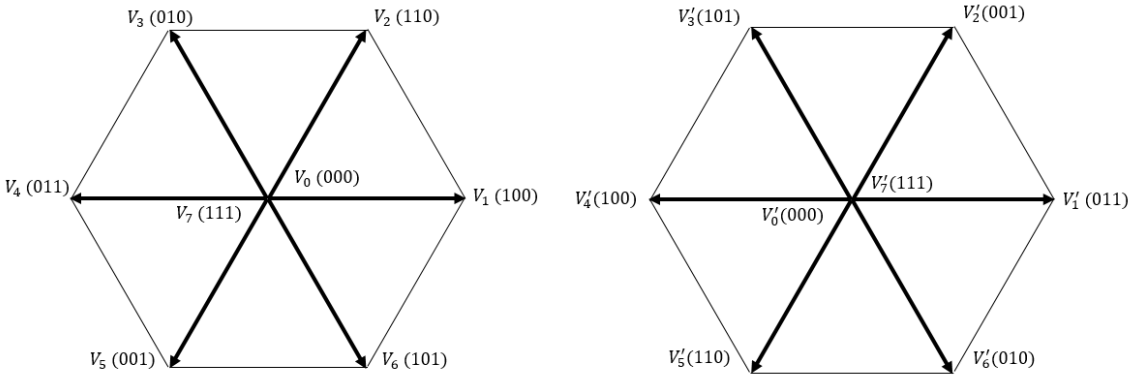


Figure 2.17: Space vector diagram on the stationary voltage reference frame for the two two-level VSCs of the dual inverter.

It can be noticed that the voltage vectors for VSC B are specular to the one of VSC A. The phase voltages of the OEW load as a function of the switch states can be found substituting to (2.15) the relationship that exists between the leg phase voltage and the switch state

$$\begin{cases} v_{aa'} = E_a s_a^A - E_b s_a^B \\ v_{bb'} = E_a s_b^A - E_b s_b^B \\ v_{cc'} = E_a s_c^A - E_b s_c^B \end{cases} \tag{2.16}$$

Tables 2.4, 2.5 and 2.6 report the voltage vectors for the dual-inverter showing all the switching states of the upper devices and their $\alpha\beta$ components in the polar form. In Fig. 2.18 the voltage vectors produced by the dual inverter are shown, it can be seen how the 64 possible vectors are distributed over 19 possible vectors. Each voltage vector of the dual inverter topology can be obtained as a combination of one vector of VSC A and one of VSC B. As an example the point P in Fig. 2.18 can be obtained as the combination of vector $V_1(100)$ of VSC A and vector $V_5^{'}(001)$ of VSC B. Another combination consists in the vectors $V_2(110)$ of VSC A and vector $V_4^{'}(011)$ of VSC B. The high redundancy is already evident since the same point P can be reached by other combinations of vectors of VSC A and VSC B.

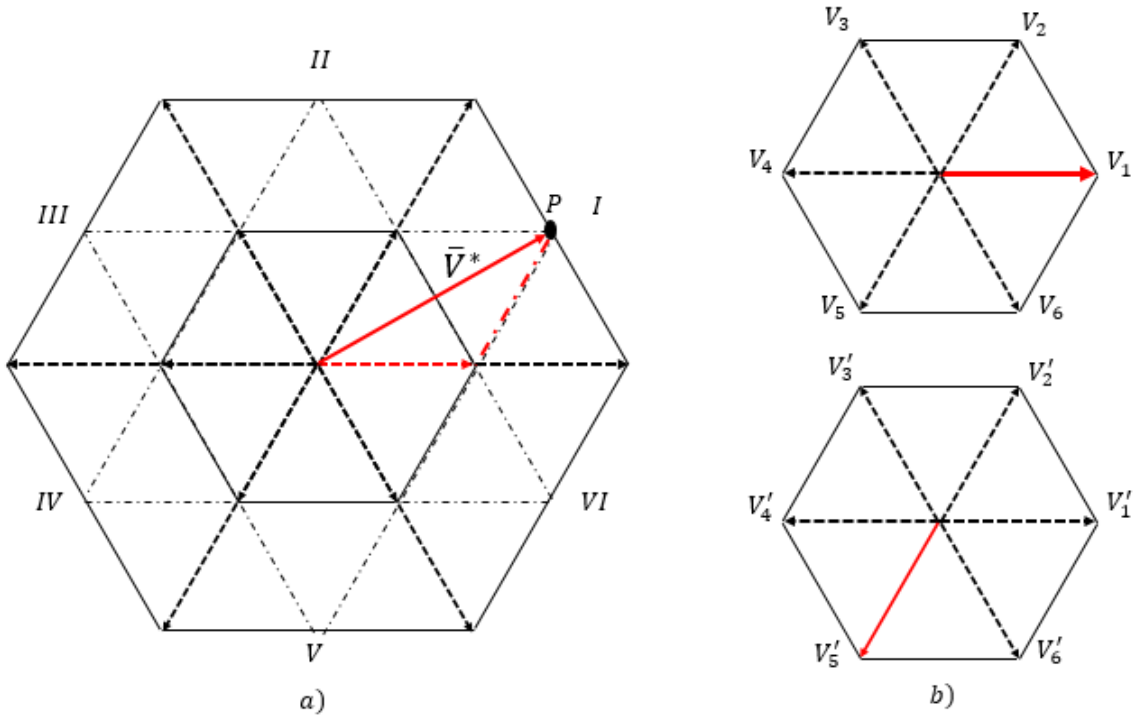


Figure 2.18: a) Voltage Space vectors generated by the Dual Inverter. b) Voltage Space vectors of the individual VSIs.

The overall space vector diagram in the $\alpha\beta$ plane is composed by 64 vectors allocated in 19 different positions. 24 small triangles can be identified, each one of them delimited by three active vectors. The total number of active vectors sums to 54 while the null vectors, located at the origin are 10. The active vectors can be divided according to their length, 36 are of module V_{dc}, 12 of module $\sqrt{3}V_{dc}$ and 6 of length $2V_{dc}$. In order to implement different modulations the hexagon formed by the voltage vectors of the dual inverter can be divided in 6 sectors each of them covering 60° and indicated in Fig. 2.19 with a Roman numeral. Redundant switching states are referred to different switching states, which result in the same voltage space vector. In Fig. 2.18 the hexagon of the dual inverter is obtained considering all the possible combinations of each inverter leg state. As done for the standard VSCs where a state s_k^h has been identified to determine the state of each converter leg an equivalent state

s_k for the dual inverter can be identified as if it was a single converter, where the subscript k stands for the leg a,b or c. Table 2.3 shows the relationship between the two VSC A and B leg states and the one of the dual converter equivalent leg. Since each leg state can be either 1 or 0, the common dc link dual converter equivalent leg state s_k can assume values of 1, 0 or -1.

Table 2.3: Dual Inverter equivalent leg state s_k

s_k^A	s_k^B	s_k
1	1	0
1	0	1
0	1	-1
0	0	0

In Fig. 2.19 a detail of the space voltage diagram for the dual inverter is shown highlighting the amplitude of the voltage vectors. The maximum rotating vector admissible by the dual inverter topology is the one that can rotate inside the larger outer hexagon. The radius of the circumference inscribed in the outer large hexagon gives the maximum voltage vector that can be synthesized. From Fig. 2.19 it can be observed that the maximum vector has module of $\frac{2}{\sqrt{3}}V_{dc}$.

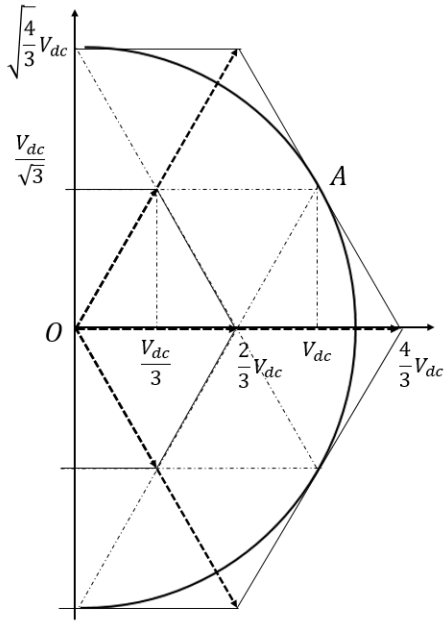


Figure 2.19: Dual Inverter Space vectors and maximum rotating vector.

Open-end winding loads fed by a dual 2-level inverters has more redundant states in comparison to a 3-level NPC and it can provide more flexibility in controlling the phase voltages. Moreover, the magnitude of the large voltage vectors is twice the length of the large active vector in the conventional 3-level NPC. Similarly as done in (2.3) the load voltages in the $\alpha\beta$ plane can be found using (2.17)

$$\overline{V}_{OEW} = V_{aa'} + V_{bb'}e^{j\frac{2\pi}{3}} + V_{cc'}e^{j\frac{4\pi}{3}} \tag{2.17}$$

Tables 2.4, 2.5 and 2.6 report gate signals, magnitude and phase of all the possible space voltage vectors that the dual-inverter topology can generate.

Table 2.4: Dual-inverter space Voltage Vectors from 00' to 72'.

n	s_a^A	s_b^A	s_c^A	s_a^B	s_b^B	s_c^B	Magnitude and Phase	Name
0	0	0	0	0	0	0	$0\angle 0$	00
1	1	0	0	0	0	0	$V_{dc}\angle 0$	10'
2	1	1	0	0	0	0	$V_{dc}\angle \frac{\pi}{3}$	20'
3	0	1	0	0	0	0	$V_{dc}\angle \frac{2\pi}{3}$	30'
4	0	1	1	0	0	0	$V_{dc}\angle \pi$	40'
5	0	0	1	0	0	0	$V_{dc}\angle \frac{4\pi}{3}$	50'
6	1	0	1	0	0	0	$V_{dc}\angle \frac{5\pi}{3}$	60'
7	1	1	1	0	0	0	$0\angle 0$	70'
8	0	0	0	1	0	0	$V_{dc}\angle \pi$	01'
9	1	0	0	1	0	0	$0\angle 0$	11'
10	1	1	0	1	0	0	$V_{dc}\angle \frac{2\pi}{3}$	21'
11	0	1	0	1	0	0	$\sqrt{3}V_{dc}\angle \frac{5\pi}{6}$	31'
12	0	1	1	1	0	0	$2V_{dc}\angle \pi$	41'
13	0	0	1	1	0	0	$\sqrt{3}V_{dc}\angle \frac{7\pi}{6}$	51'
14	1	0	1	1	0	0	$V_{dc}\angle \frac{4\pi}{3}$	61'
15	1	1	1	1	0	0	$V_{dc}\angle \pi$	71'
16	0	0	0	1	1	0	$V_{dc}\angle \frac{4\pi}{3}$	02'
17	1	0	0	1	1	0	$V_{dc}\angle \frac{5\pi}{3}$	12'
18	1	1	0	1	1	0	$0\angle 0$	22'
19	0	1	0	1	1	0	$V_{dc}\angle \pi$	32'
20	0	1	1	1	1	0	$\sqrt{3}V_{dc}\angle \frac{7\pi}{6}$	42'
21	0	0	1	1	1	0	$2V_{dc}\angle \frac{4\pi}{3}$	52'
22	1	0	1	1	1	0	$\sqrt{3}V_{dc}\angle \frac{3\pi}{2}$	62'
23	1	1	1	1	1	0	$V_{dc}\angle \frac{4\pi}{3}$	72'

Table 2.5: Dual-inverter space Voltage Vectors from 03' to 75'.

n	s_a^A	s_b^A	s_c^A	s_a^B	s_b^B	s_c^B	Magnitude and Phase	Name
24	0	0	0	0	1	0	$V_{dc}\angle\frac{5\pi}{3}$	03'
25	1	0	0	0	1	0	$\sqrt{3}V_{dc}\angle\frac{11\pi}{6}$	13'
26	1	1	0	0	1	0	$V_{dc}\angle 0$	23'
27	0	1	0	0	1	0	$0\angle 0$	33'
28	0	1	1	0	1	0	$V_{dc}\angle\frac{4\pi}{3}$	43'
29	0	0	1	0	1	0	$\sqrt{3}V_{dc}\angle\frac{3\pi}{2}$	53'
30	1	0	1	0	1	0	$2V_{dc}\angle\frac{5\pi}{3}$	63'
31	1	1	1	0	1	0	$V_{dc}\angle\frac{5\pi}{3}$	73'
32	0	0	0	0	1	1	$V_{dc}\angle 0$	04'
33	1	0	0	0	1	1	$2V_{dc}\angle 0$	14'
34	1	1	0	0	1	1	$\sqrt{3}V_{dc}\angle\frac{\pi}{6}$	24'
35	0	1	0	0	1	1	$V_{dc}\angle\frac{\pi}{3}$	34'
36	0	1	1	0	1	1	$0\angle 0$	44'
37	0	0	1	0	1	1	$V_{dc}\angle\frac{5\pi}{3}$	54'
38	1	0	1	0	1	1	$\sqrt{3}V_{dc}\angle\frac{11\pi}{6}$	64'
39	1	1	1	0	1	1	$V_{dc}\angle 0$	74'
40	0	0	0	0	0	1	$V_{dc}\angle\frac{\pi}{3}$	05'
41	1	0	0	0	0	1	$\sqrt{3}V_{dc}\angle\frac{\pi}{6}$	15'
42	1	1	0	0	0	1	$2V_{dc}\angle\frac{\pi}{3}$	25'
43	0	1	0	0	0	1	$\sqrt{3}V_{dc}\angle\frac{\pi}{2}$	35'
44	0	1	1	0	0	1	$V_{dc}\angle\frac{2\pi}{3}$	45'
45	0	0	1	0	0	1	$0\angle 0$	55'
46	1	0	1	0	0	1	$V_{dc}\angle 0$	65'
47	1	1	1	0	0	1	$V_{dc}\angle\frac{\pi}{3}$	75'

Table 2.6: Dual-inverter space Voltage Vectors from 06' to 77'.

n	s_a^A	s_b^A	s_c^A	s_a^B	s_b^B	s_c^B	Magnitude and Phase	Name
48	0	0	0	1	0	1	$V_{dc}\angle\frac{2\pi}{3}$	06'
49	1	0	0	1	0	1	$V_{dc}\angle\frac{\pi}{3}$	16'
50	1	1	0	1	0	1	$\sqrt{3}V_{dc}\angle\frac{\pi}{2}$	26'
51	0	1	0	1	0	1	$2V_{dc}\angle\frac{2\pi}{3}$	36'
52	0	1	1	1	0	1	$\sqrt{3}V_{dc}\angle\frac{5\pi}{6}$	46'
53	0	0	1	1	0	1	$V_{dc}\angle\pi$	56'
54	1	0	1	1	0	1	$0\angle0$	66'
55	1	1	1	1	0	1	$V_{dc}\angle\frac{2\pi}{3}$	76'
56	0	0	0	1	1	1	$0\angle0$	07'
57	1	0	0	1	1	1	$V_{dc}\angle0$	17'
58	1	1	0	1	1	1	$V_{dc}\angle\frac{\pi}{3}$	27'
59	0	1	0	1	1	1	$V_{dc}\angle\frac{2\pi}{3}$	37'
60	0	1	1	1	1	1	$V_{dc}\angle\pi$	47'
61	0	0	1	1	1	1	$V_{dc}\angle\frac{4\pi}{3}$	57'
62	1	0	1	1	1	1	$V_{dc}\angle\frac{5\pi}{3}$	67'
63	1	1	1	1	1	1	$0\angle0$	77'

2.6.4 ZSV in the standard two-level VSC and in the Dual-Inverter Topology

The ZSV produced by the standard two-level VSC for each space vector is shown in Table 2.2. It can be noticed that all vectors produce a ZSV V_0 different from zero.

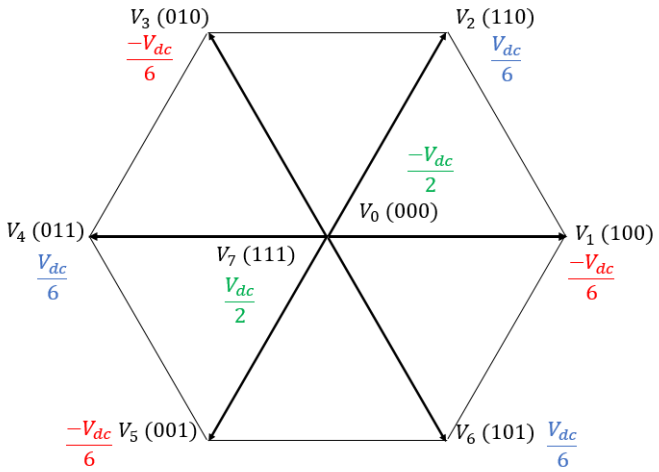


Figure 2.20: ZSV for the Voltage Space Vectors of the Standard VSC.

Fig. 2.20 shows the space voltage vectors for the two-level converter, next to each vector the corresponding ZSV is displayed. It can be noticed that the vectors can be grouped in three groups. Three active vectors produce a positive ZSV of $\frac{V_{dc}}{6}$, other three active voltage vectors produce a negative ZSV of $\frac{-V_{dc}}{6}$ while the two remaining zero vectors produce a positive and negative ZSV of module $\frac{V_{dc}}{2}$.

The ZSV produced by each vector of the dual-inverter can be found transforming the space voltage vectors reported in Tables 2.4, 2.5 and 2.6 in the $\alpha\beta 0$ fixed reference frame. The 64 space voltage vectors locations on the $\alpha\beta$ plane are shown in Fig. 2.21 (b). The green small hexagon of Fig. 2.21 (a) represents the locus of points obtained by connecting the space voltage vectors generated by the standard two-level inverter while the red hexagon is the one obtained using exclusively the voltage vectors which generate zero ZSV.

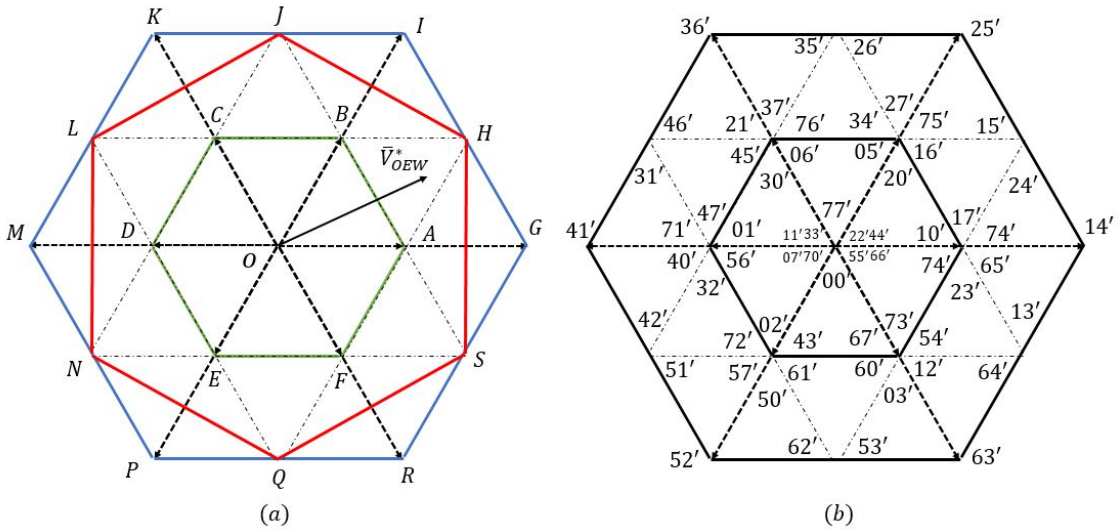


Figure 2.21: (a) Single VSC voltage vectors (green hexagon), Dual Inverter voltage vectors (blue hexagon) and dual-inverter voltage vectors with zero ZSV (red hexagon). (b) Voltage space vectors locations on the $\alpha\beta$ plane for the dual inverter.

According to Fig. 2.21 (a) and (b) it can be understood which dual-inverter voltages generate a zero ZSV. All the vectors that form the red hexagon plus the one laying at the origin of the plane have zero ZSV.

2.6.5 Decoupled Control of the Dual level Inverter Topology

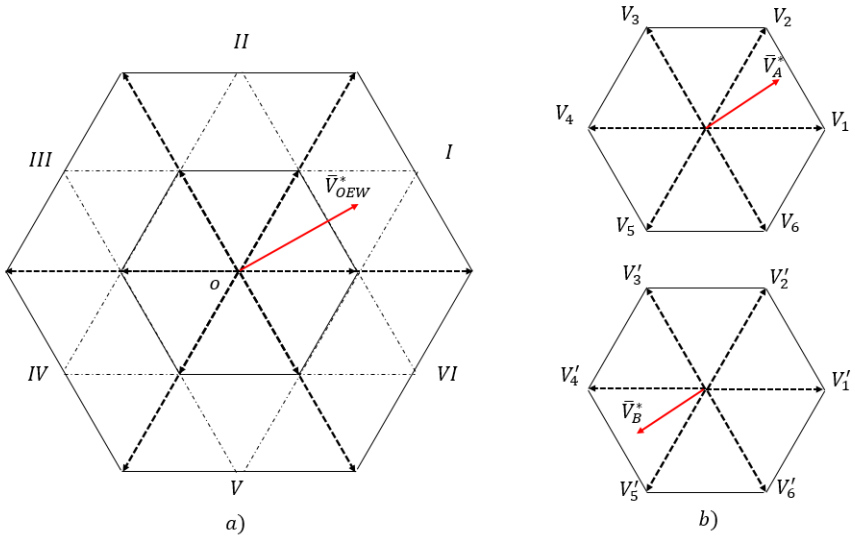


Figure 2.22: Decoupled control representation on the space vector diagram for the dual two-level inverter scheme and space vector diagrams of individual inverters.

The state variables to control in a OEW load are the three phase currents, by achieving their full control the dynamic and steady state performances can be controlled. Current control for the OEW load is achieved by generating the desired voltages at the terminals of the phase windings. The reference phase voltages for the OEW load have to be split between the two standard two-level VSCs; a common technique is the decoupled control of the two VSCs as discussed in [83, 84]. In general, the dual-inverter reference voltage vector represented in Fig. 2.22 can be realized by the inverters using a SVPWM in the average sense by switching among the three nearest vectors in the proximity of the tip of the reference vector $\overline{V}_{OEW}$. The decoupled control consists in splitting the reference vector $\overline{V}_{OEW}$ into two equal and opposite vectors $\overline{V}_A$ and $\overline{V}_B$, to get synchronized PWMs, and each one is realized in the average sense by the individual two 2-level inverters. According to (2.9) the reference vectors for the two VSCs can be calculated and the converters are controlled inde-

pendently. The desired reference space vector $\overline{V}_{OEW}$ to be generated by the dual VSI is synthesized by independently synthesizing the vectors $\overline{V}_A$ by VSC A and $\overline{V}_B$ by VSC B. It is therefore clear how it is possible to independently control the two VSCs. Furthermore, another degree of freedom consists in the independent switching of the single inverters. Many different switching patterns can be chosen in order to synthesize on average the reference voltage vector which needs to be synthesized [85].

2.7 Reduction of the ZSV in the standard two-level VSI and in the Dual Inverter Topology with Separate dc links

In this section the main techniques for the reduction of the ZSV both for the standard two-level VSI and the dual-inverter topology with separate dc links are presented. The modulation techniques used to achieve the reduction of the ZSV for these configurations are of particular interest since they can be used as a starting point to develop modulation strategies for the dual-inverter with common dc link to eliminate the its ZSV.

2.7.1 Reduction of ZSV and Bearing Currents for the Standard two-level VSI

The increasing switching frequencies adopted in modern drives allow on one hand to increase their dynamic performances, but on the other hand they introduce unwanted effects such as premature deterioration of ball bearings and high intensity electromagnetic emissions. These effects are caused by the flowing of parasitic capacitance currents often referred to as ZSC. The flow of ZSC is strictly related to the

sequence of switching states used by the converter to synthesize the reference voltage vector as already seen from Table 2.2. The higher the fluctuation of ZSV the higher will be the ZSC flowing in the system. For the case of a standard two-level converter, as it can be seen from Table 2.2, the ZSV produced cannot be completely eliminated since every voltage vector produces a ZSV different from zero [85]. Therefore different modulations have been studied to keep the ZSV as constant as possible. The ZSV produced by a standard two-level VSC is always different from zero and may take the values of $\pm\frac{V_{dc}}{6}$ or $\pm\frac{V_{dc}}{2}$, depending on the inverter switch states selected. Among the possible solutions to suppress the ZSV produced by a two-level VSC many have investigated the possibility to use additional hardware circuitry. In [86–89] passive filters are used while in [90] an active filter solution has been proposed. All these methods involve additional hardware, and thus, they significantly increase the drive cost and complexity. The other possibility is to consider the cause itself of the ZSV and modify the PWM pulse pattern. In [85] an accurate comparison between various PWM pulse-patterns to achieve a reduction of the ZSV is reported. The different modulations can be classified as Reduced ZSV PWM (RZSV-PWM) methods. All the modulations proposed to reduce the ZSV variation for the two-level converter [91–94] achieve reduction of ZSV from $\pm\frac{V_{dc}}{2}$ of the conventional PWM methods to $\pm\frac{V_{dc}}{6}$. The characteristics of the conventional Continuous PWM (CPWM) and Discontinuous PWM (DPWM) methods are well known [95, 96]. The pulse pattern of the CPWM and DPWM methods involves utilization of at least one of the two zero-voltage vectors V_0 and V_7 during each PWM cycle. The pulse pattern of the standard SVPWM when the reference vector falls into sector I is shown in Fig. 2.23.

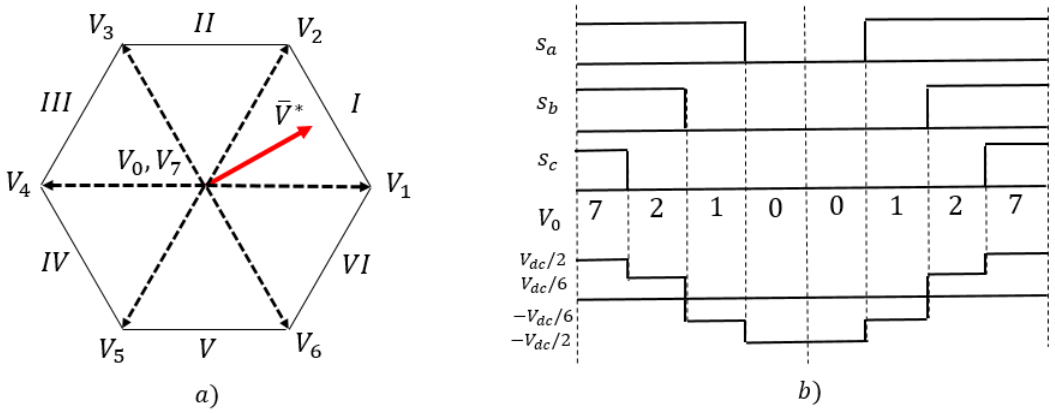


Figure 2.23: a) Standard two-level Voltage vectors. b) Inverter switch state and ZSV pulse patterns of the CPWM method.

It can be noticed how this pulse pattern yields to high ZSV $\pm\frac{V_{dc}}{2}$ making it not suitable for all the applications which require small variations of the ZSV. Among the modulations techniques proposed to reduce the ZSV in [94, 97] a PWM modulation that uses only three inverter states of the eight available is proposed to keep constant the ZSV. The idea is to use exclusively only the voltage vectors that have the same ZSV. As shown in Table 2.7 there are three groups of voltage vectors that have the same ZSV and are identified as ODD, EVEN and NULL.

Table 2.7: Standard Two-level VSC Voltage Vectors grouped according to their ZSV

Voltage Vectors	ZSV	Type
$\overline{V}_1, \overline{V}_3, \overline{V}_5$	$\frac{-V_{dc}}{6}$	ODD
$\overline{V}_2, \overline{V}_4, \overline{V}_6$	$\frac{V_{dc}}{6}$	EVEN
$\overline{V}_0, \overline{V}_7$	$\frac{-V_{dc}}{2}, \frac{V_{dc}}{2}$	NULL

Fig. 2.24 shows the two groups of vectors that produce the same ZSV, the two triads are connected by segments to form two triangles which delimit the area that can be covered with the exclusive use of these active vectors. The reference voltage $\overline{V}^*$ is

obtained each sample time by switching among the three ODD or EVEN vectors. The dwelling times of the ODD vectors are calculated at each ample time T_s as shown in (2.18)

$$\begin{cases} \overline{V}^* = \overline{V}_1 T_1 + \overline{V}_3 T_3 + \overline{V}_5 T_5 \\ T_s = T_1 + T_3 + T_5 \end{cases} \tag{2.18}$$

Similarly it can be done for the EVEN vectors, their dwelling times can be derived from the system of (2.19)

$$\begin{cases} \overline{V}^* = \overline{V}_2 T_2 + \overline{V}_4 T_4 + \overline{V}_6 T_6 \\ T_s = T_2 + T_4 + T_6 \end{cases} \tag{2.19}$$

The radius of the circle inscribed in the triangle that has as vertices the three voltage vectors that have same ZSV is $V_{dc}/3$, therefore any higher voltage cannot be synthesized exclusively with the three vectors. If the reference vector would have higher module than $V_{dc}/3$ than the resultant ZSV cannot be kept to $\pm\frac{V_{dc}}{6}$ since the zero vectors have to be used as well. In [98] the same modulation is applied considering also the DT effect with the intention of reducing the common mode emissions by reducing the ZSV fluctuation.

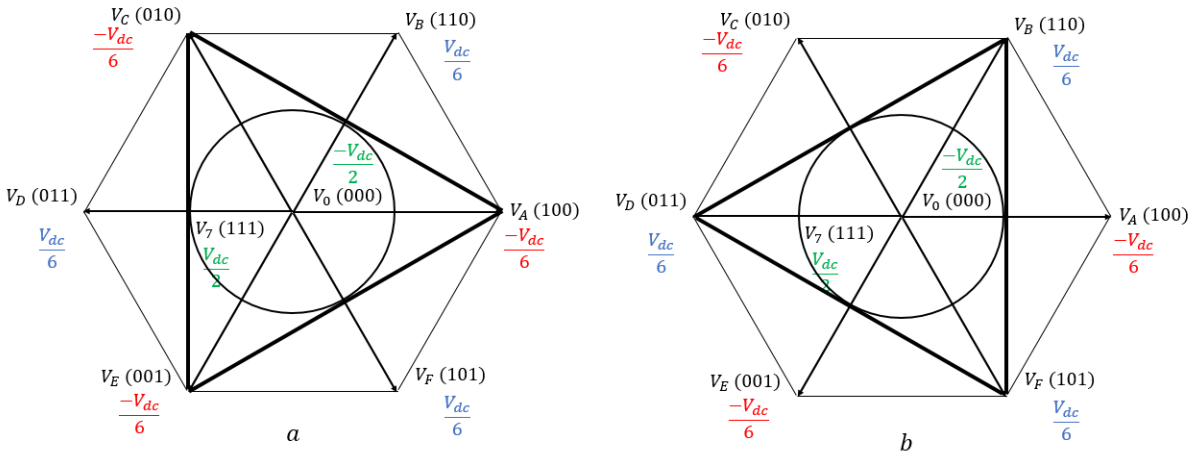


Figure 2.24: Standard VSC voltage vectors. a) Group of ODD vectors b) Group of EVEN vectors

Fig. 2.25 instead shows the surface of the $\alpha\beta$ plane that can be covered by the modulation that uses active vectors when both the triangles formed by the ODD and EVEN vectors are considered. The red circle's radius corresponds to the maximum voltage vector's module that can be synthesized by keeping the ZSV constant. The module is $\frac{2V_{dc}}{3\sqrt{3}}$, which is slightly higher than the one calculated from the circle inscribed in the triangle that has as vertices the voltage vector with the same ZSV.

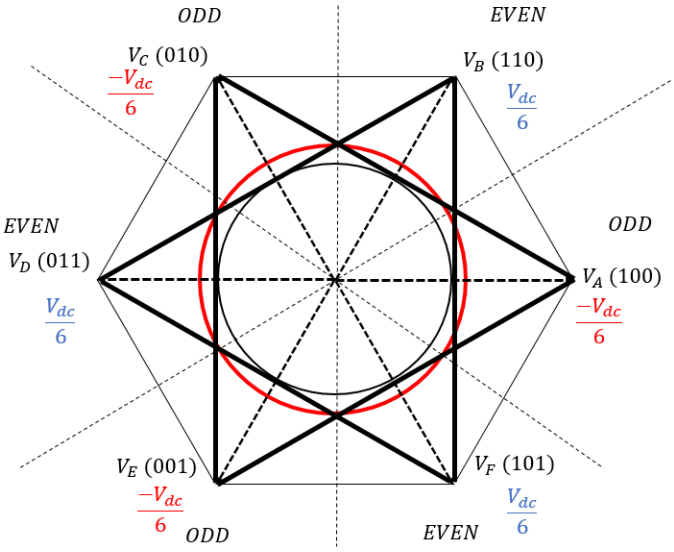


Figure 2.25: ODD and EVEN vectors modulation for the standard two-level VSC.

The modulation proposed in [94] allows to keep the ZSV constant for every sample time where the same group of three active vectors is used; the transition between ODD and EVEN vectors happens every 60 according to the reference voltage vector position. The main drawback of this modulation is the reduced maximum voltage reference that can be synthesized if compared to the maximum voltage vector that can be synthesized if a standard SVM or PWM is implemented. In particular there is a reduction of 33% if the reduced ZSV modulation is used. Particular attention is given to these techniques for ZSV reduction for the standard two-level inverter because they will be used as a starting point for the study of a novel modulation for the elimination of the ZSV produced by the dual-inverter topology.

2.7.2 Reduction of ZSV and Bearing Currents for the Dual Inverter Topology with separate dc links

The problem and analysis of the ZSV produced in the dual-inverter system for OEW loads has been considered for topologies with separate dc links. An ac machine driven by a dual inverter with separate dc link is considered in [1]. The machine's shaft can assume a voltage depending on the ZSV produced by the two converters. Investigation in the past decades of the high-frequency ZSV produced by power inverters has found that there are voltage drops across the bearings that may cause bearing currents that could lead to premature bearing failure [99–101]. Increased costs of downtime and maintenance led to increasing attention to the bearing current problem and how to protect them. Many solutions have been proposed such as insulated bearings and electrostatic shielding. Also PWM methods for reducing the ZSV produced by the converter have been proposed with the intention of eliminating the problem at its roots. The dual inverter system investigated with the purpose of reducing the bearing current is shown in Fig. 2.26.

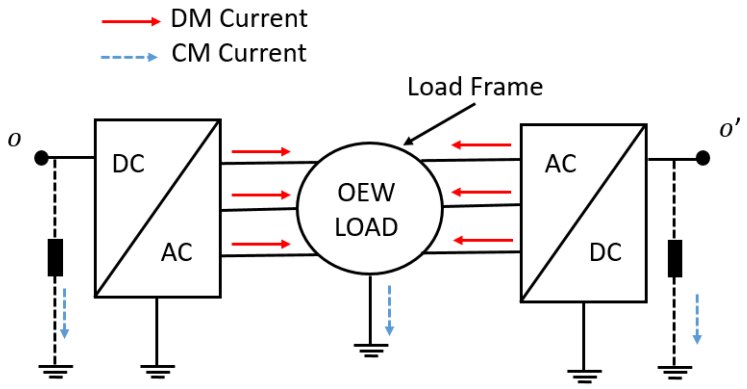


Figure 2.26: Common and Differential mode currents in the dual inverter topology with separate dc links.

The differential mode (DM) and common mode (CM) currents are identified. The

CM currents, also known as ZSC, flow through the load frame and returns to the inverters and/or input ac mains. The differential mode current instead flows between the inverter legs and the motor phase windings. It is important not only to eliminate the ZSV when possible but also to reduce the ZSV variation, i.e. the $\frac{dv}{dt}$. In [1] different PWM hybrid modulations that aim to reduce the ZSV produced by the converter are presented. Firstly the voltage reference vectors for the two separate VSCs have to be defined, a possible solution is the decoupled control as shown in Section 2.6.5. Referring to Fig. 2.22 if the voltage vector $\overline{V}_A$ has to be realised in the average sense during a sample time using VSC A there are various options in terms of switching patterns that can be chosen. Similarly also the vector $\overline{V}_B$ can be obtained in the average sense with different voltage vectors of VSC B. There are many switching combinations that the dual inverter structure is capable of, therefore giving multiple options in terms of switching pattern that reduces the ZSV produced. The case of a standard sinusoidal PWM is firstly analysed. The switching pattern of the six legs is shown in Fig. 2.27; the ZSV that is supplied to the motor is plotted showing that there are as many as seven different voltage levels. Considering the reference voltage vector for the dual inverter shown in Fig. 2.22; the individual reference vectors for VSC A and VSC B lay in the first and fourth sub-sectors of the hexagon respectively. $\overline{V}_A$ is synthesized from the voltage vectors $\overline{V}_1$ and $\overline{V}_2$ while $\overline{V}_B$ is produced as a combination of $\overline{V}_4$ and $\overline{V}_5$.

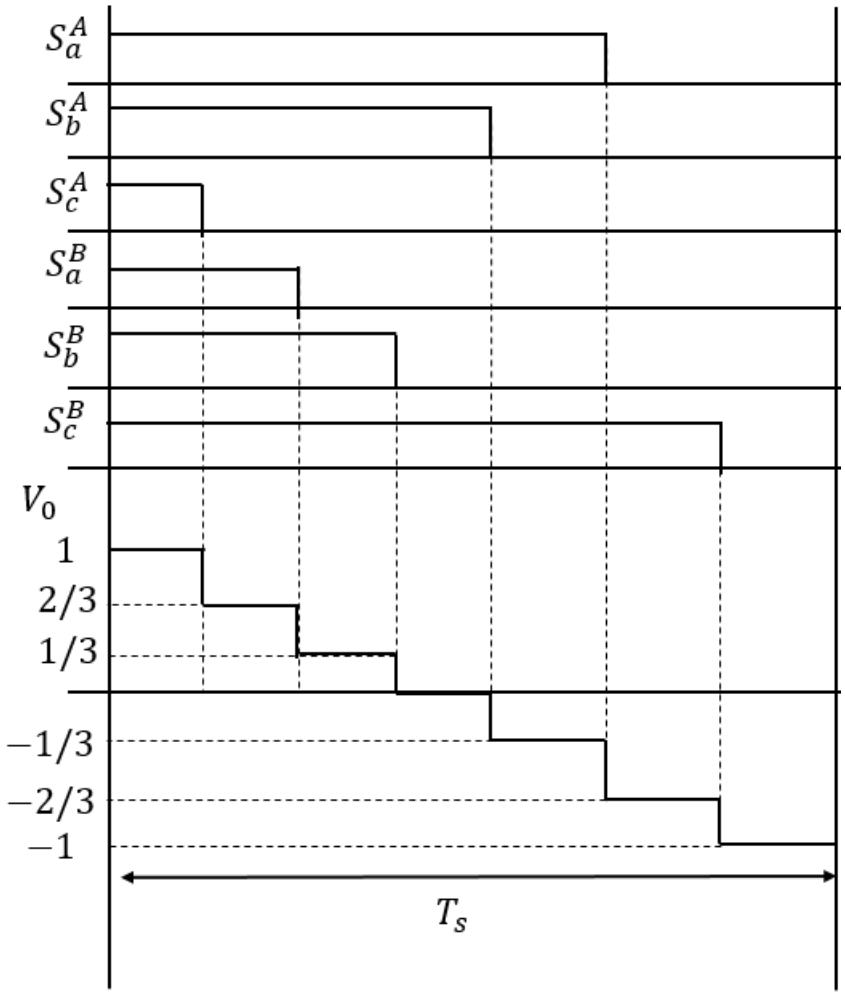


Figure 2.27: Switching status of the dual inverter and ZSV profile for the case of standard sinusoidal PWM.

Other possible switching strategies that aim at reducing the voltage levels of ZSV are shown in Table 2.8 and Fig. 2.28.

Table 2.8: Dual-Inverter switching patterns possibilities for the ZSV reduction.

Switching state combinations	ZSV Levels	No of ZSV Changes
7-2-1-8/7'-4'-5'-8'	$V_{dc}/2, V_{dc}/6, 0, -V_{dc}/6, -V_{dc}/2$	5
7-2-1-8/4'-4-5'-1'	$V_{dc}/3, V_{dc}/6, 0, -V_{dc}/6, -V_{dc}/3$	5
3-2-1-6/3'-4-5'-6'	$V_{dc}/3, V_{dc}/6, 0, -V_{dc}/6, -V_{dc}/3$	5
3-2-1-6/4'-4-5'-1'	$V_{dc}/6, 0, -V_{dc}/6$	5
4-2-1-1/4'-4'-5'-1'	$V_{dc}/6, 0, -V_{dc}/6$	3

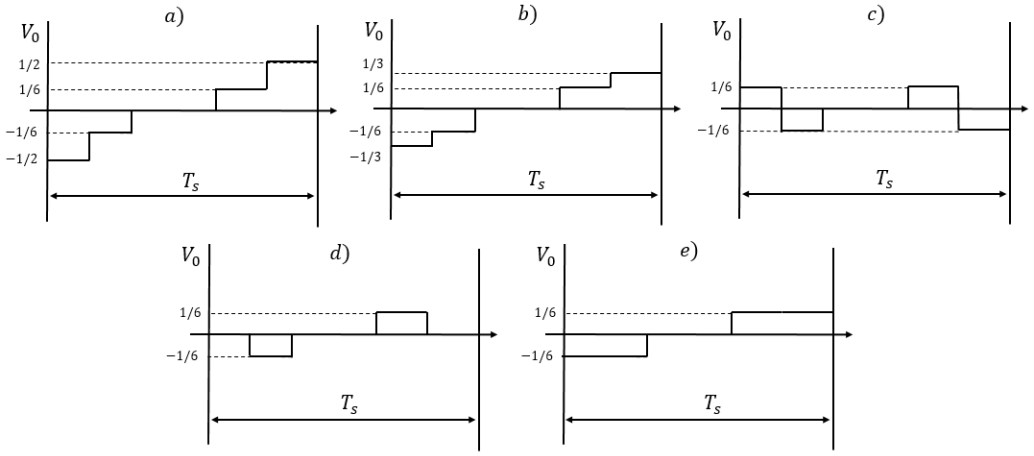


Figure 2.28: CMV profiles with reduced CMV PWMs proposed in [1] and reported in Table 2.8.

Among them there are switching combinations which are able to reduce the ZSV levels at three. In [1] the ZSV is reduced or eliminated with the intention to reduce the machine's shaft voltage so that it is always below its threshold limit that avoids the lubricant breakdown around the bearing. If the voltage would be higher there could be possible discharge, flow of charges and potential damage of the bearings. The principle used to reduce the ZSV is based on the observation that once the dwell times are calculated for the VSC A the switching times of the other converter are carefully selected in relation of the VSC A phase switching times. The switching states of VSC B are chosen in such a manner that they are always opposite to that of inverter A. The same ideas and principles used to reduce the ZSV for the dual-inverter

structure with separate dc links can be adopted for the topology with a single voltage source. In fact with a single dc link the problem of circulating currents cannot be neglected and a reduction of the ZSV produced is mandatory.

2.8 Circulating Current Suppression Strategies for the Dual-Inverter Topology with Common dc link

Mainly two different strategies can be identified for suppressing the ZSC flowing in the dual-inverter topology:

1. Common-Mode Chokes
2. VSCs Modulation techniques

2.8.1 Common-Mode Chokes

One of the earliest solutions proposed to the problem of circulating currents is the introduction in series to the three-phase load of common-mode choke [2, 102]. The zero-sequence choke with three windings at the same core (without air-gap) fulfils the task to suppress the ZSC without impeding the phase currents. Fig. 2.29 shows the positioning of the common-mode choke between the VSC and the motor.

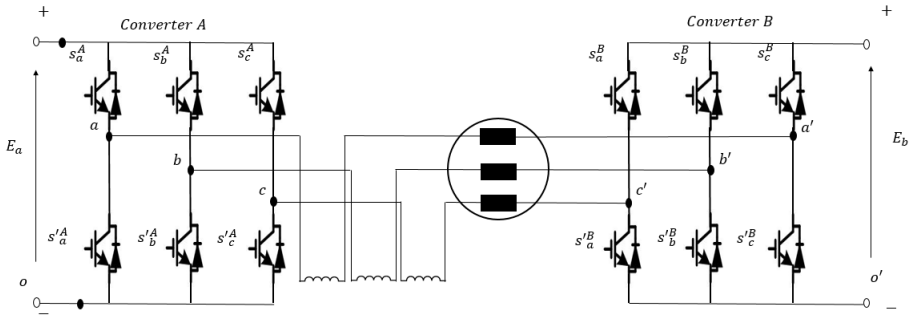


Figure 2.29: Dual-Inverter with common-mode choke.

The voltage equations for the three-phase common-mode choke are shown in (2.20)

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.20}$$

where M is the mutual coupling between the phase inductors and it can be expressed as

$$M = kL \tag{2.21}$$

If k is equal to 0 it means independent inductors while if it is 1 it consists in perfect coupling. Transforming (2.20) on the synchronous reference frame the phase inductances matrix becomes

$$\mathbf{T}_P(\vartheta_e) L_{CM} \mathbf{T}_P^{-1}(\vartheta_e) = \begin{bmatrix} L(1-k) & 0 & 0 \\ 0 & L(1-k) & 0 \\ 0 & 0 & L(2k+1) \end{bmatrix} \tag{2.22}$$

If perfect coupling is achieved it can be seen how the common-mode choke does not affect at all the q- and d- axis while it increases the zero-sequence inductance, therefore increasing the ZSI and opposing the circulation of ZSC. The modelling and design of a three-phase inductor is discussed in [103, 104]. Even if the common-mode choke solution is able to suppress the ZSC, it does not eliminate its source, i.e. the ZSV. Furthermore it adds weight and size to the whole topology reducing the power density of the system. For these reasons even though its effectiveness in reducing the ZSC the common-mode choke is often the least desired solution.

2.8.2 Modulations for ZSV Reduction for the Dual-Inverter Topology

When the OEW load is connected to a dual inverter with common dc link the ZSC can flow freely in the system. The circulating current causes additional losses and therefore reduces the overall system efficiency. Increased current ripple can lead to the power switch damage or complete failure depending on the zero sequence current entity. The main drawback of this topology is indeed the ZSC flow, therefore many works in literature focused on the reduction or elimination of the ZSV produced by the converters feeding the OEW load. The problem of circulating ZSC exists independently of the type of load used therefore the focus is on the converter side, in particular on how to synthesize the reference vector considering the added constraint of reducing or eliminating the ZSV. As it will be shown later when discussing the PMSM machine model, it will be highlighted how the equivalent zero-sequence circuit affects the magnitude of the ZSC.

The problem of ZSV and circulating ZSC has been extensively studied in the literature. Many works focused on the elimination of the ZSV of the dual-inverter system by forcing the ZSV of the individual inverters to a value of zero, in the average sense, in each sampling-time interval. During a sample time T_s, the vectors that can be

applied are either active vectors or zero vectors; it will be referred to the zero-vector time period T_0 when talking about the time that the zero vectors are applied during a sample time. Instead the effective time period T_{eff} is the time at which it corresponds the amount of effective dc link voltage applied to the load, namely when the $\alpha - \beta$ voltages are different from zero. Therefore the following relationship can be written

$$T_s = T_0 + T_{eff} \tag{2.23}$$

The importance and effect of the placement of the zero-vector time period in a sampling-time interval for a standard two-level inverter has been discussed in [105]. Placing the effective time period at the centre of the sample time it has been shown giving a better spectral performance compared to the other cases when the effective time is placed elsewhere. The additional degree of freedom represented by the possibility of moving the effective time in a sample time has been used also in the dual-inverter topology with the aim of eliminating the average ZSV produced by the two converters [106]. The concept of imaginary switching times is introduced considering the phase reference voltages of VSC A v^*_{an}, v^*_{bn} and v^*_{cn}

$$T_x = \frac{T_s}{V_{dc}} v^*_k \tag{2.24}$$

where the subscript k stands for the phase a, b or c. In [106] the reference vector for the dual-inverter is split among the two individual VSCs as described in Section 2.6.5. If the reference vectors for the two converters are $\overline{V}_A$ and $\overline{V}_B$ respectively as shown in Fig. 2.30, they can be synthesized in the average sense using SVM by switching among the states $T_0/2 - T_1 - T_2 - T_0/2$ for VSC A and $T_0/2 - T'_1 - T'_2 - T_0/2$ for VSC B. The sample-averaged ZSV produced can be calculated as:

$$V_0^A = \frac{1}{T_s}\Big[(\frac{-V_{dc}}{2}\frac{T_0}{2}) + (\frac{-V_{dc}}{6}\frac{T_1}{2}) + (\frac{V_{dc}}{6}\frac{T_2}{2}) + (\frac{V_{dc}}{2}\frac{T_0}{2})\Big] = \frac{1}{T_s}\Big[\frac{V_{dc}}{12}(T_2 - T_1)\Big] \tag{2.25}$$

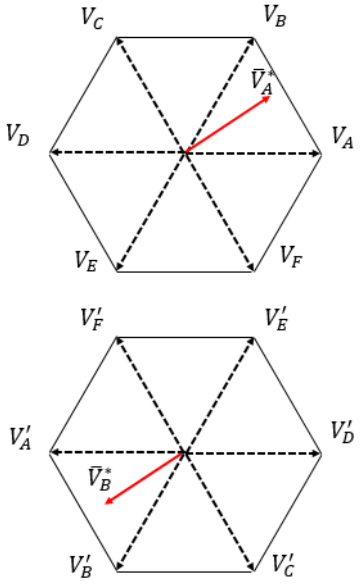


Figure 2.30: Space vector representation of the two standard two-level VSCs and their reference vectors.

It can be noticed from (2.25) that the sampled-averaged ZSV is zero exclusively if $T_1 = T_2$. If the zero vector time is unequally distributed among the voltage vectors V_0 (000) and V_7 (111), which produce opposite ZSVs of $-V_{dc}/4$ and $V_{dc}/4$, it is possible to eliminate the average ZSV. So for the case of $\overline{V}_A$ laying in the first sector of the space voltage plane of VSC A, if the possibility of unequal distribution of the zero vectors is considered, the ZSV can be written as

$$V_0^A = \frac{1}{T_s}\left[\left(\frac{-V_{dc}}{2}(xT_0)\right) + \left(\frac{-V_{dc}}{6}\frac{T_1}{2}\right) + \left(\frac{V_{dc}}{6}\frac{T_2}{2}\right) + \left(\frac{V_{dc}}{2}((1-x)T_0)\right)\right] = 0 \tag{2.26}$$

From (2.26) the ratio of unbalancing x of the zero vectors in order to eliminate the average ZSV can be calculated. Furthermore the degree of freedom represented by the possibility to shift all the three imaginary times, is used to place the effective time block in the centre of the sample time. As described in [107] the time shift that

would be required to centre the effective time is

$$T_{offset} = (1 - x)T_0 - T_{min} \tag{2.27}$$

where T_{min} is the minimum switching time among the three imaginary switching times $T_{min} = min\{T_a, T_b, T_c\}$. The offset time T_{offset} can be summed to all the imaginary switching times to balance the ZSV produced by the converter. As demonstrated in [108] the offset to be applied in order to have central positioning of the effective time and to achieve the elimination of the average ZSV is

$$T_{offset} = \frac{T_0}{2} - T_{min} \tag{2.28}$$

As described in [109] the turn on times for the upper switches of VSC B can be obtained by subtracting to the sample time the turn on times of VSC A. With this modulation the placement of the effective time is used as a possible degree of freedom to eliminate in the average sense the ZSV produced by the converters. Nevertheless instantaneously the ZSV produced is different from zero. Fig. 2.31 shows the placement of the effective time blocks for VSC A and VSC B and the resultant effective time block positioning for the dual-inverter.

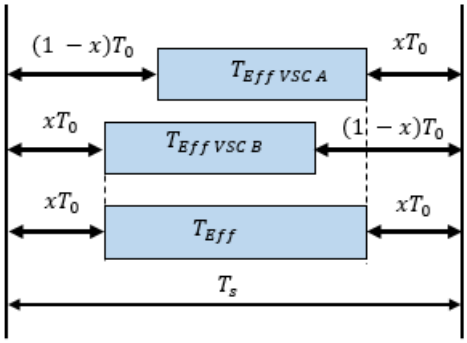


Figure 2.31: Effective-time placement of the individual inverters and the dual inverter.

The authors Somasekhar and Srinivas developed also another modulation for the dual-inverter drive with the same aim of eliminating on the sample average the ZSV. The modulation is presented in [110, 111] where the dual-inverter space vector plane is divided in Sub-Hexagonal spaces as shown in Fig. 2.32.

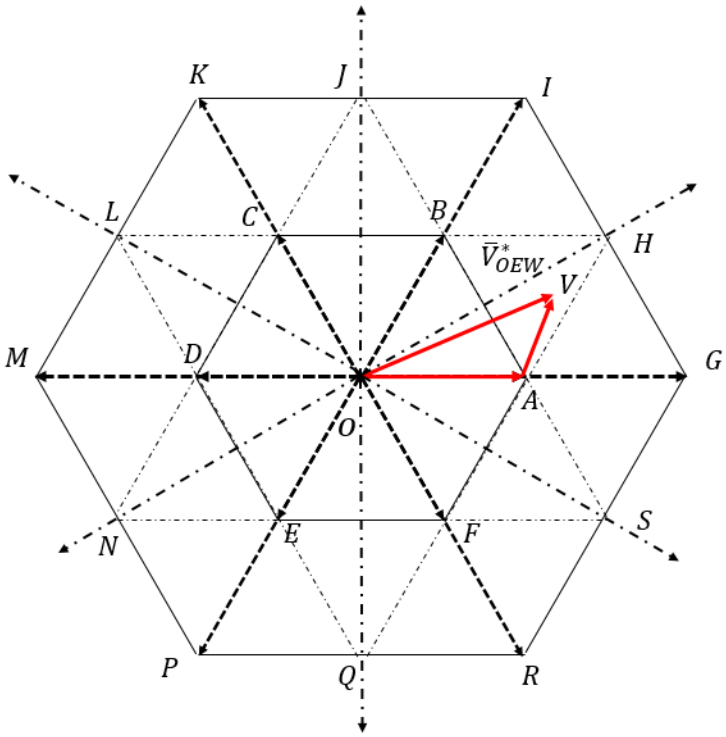


Figure 2.32: Principle of alternate-sub-hexagonal centre PWM switching strategy.

There are six hexagons which have as centres the points A, B, C, D, E and F respectively. For example the hexagon with centre A id delimited by GHBOFS. The reference vector for the dual-inverter is split among the two converters as shown in Fig. 2.32, according in which sub-hexagon the reference vector falls the dual-inverter vector is decomposed in two vectors where one of the two is clamped to the centre of the sub-hexagon. If the case of Fig. 2.32 is considered, it corresponds to clamp VSC A to the vector (100) and modulating converter B to obtain the vector AV with the principle of volts-seconds balance. To ensure an equal switching duty, the two

inverters alternate their roles for every 60 electrical degrees. Therefore if the reference vector falls in the area OSGH VSC A is not switching while if it falls in the area HIJO VSC B is clamped to the voltage vector (001) while VSC A is switching. The additional degree of freedom offered by the SVM in the placement of the zero-vector could be well exploited in this situation. In this case, the effective time period block can be pushed to one of the corners of sampling time interval, which clamps one of the phases, switching only the other two. Consequently, the number of switching is reduced by 33% with a corresponding reduction in the switching power loss. As the zero-sequence current flow is reduced, the ripple in the motor phase current is also reduced.

Similarly to what has been done in [106] the effective time is shifted in order to achieve the ZSV balancing. In this case the constraint added by the modulation that requires one converter to be clamped to one voltage vector is added. The offset necessary to place the effective time either at the beginning of the sample time or at the end is $T_{offset} = -T_{min}$ and $T_{offset} = T_s - T_{max}$ respectively as shown in [111]. This means that a simple relocation of the effective time period within the sampling time period eliminates the zero-sequence voltage in the average sense. Thus, the degree of freedom in the placement of effective time period and the observation that certain space vector combinations have a zero value of ZSVs is exploited to the advantage in the proposed PWM strategy. However, such a non-centre-spaced PWM results in a higher current ripple and consequently a higher THD.

In the work proposed in [35] by Baiju et al. the dual-inverter modulation is developed considering the two standard two-level VSCs as a whole single converter.

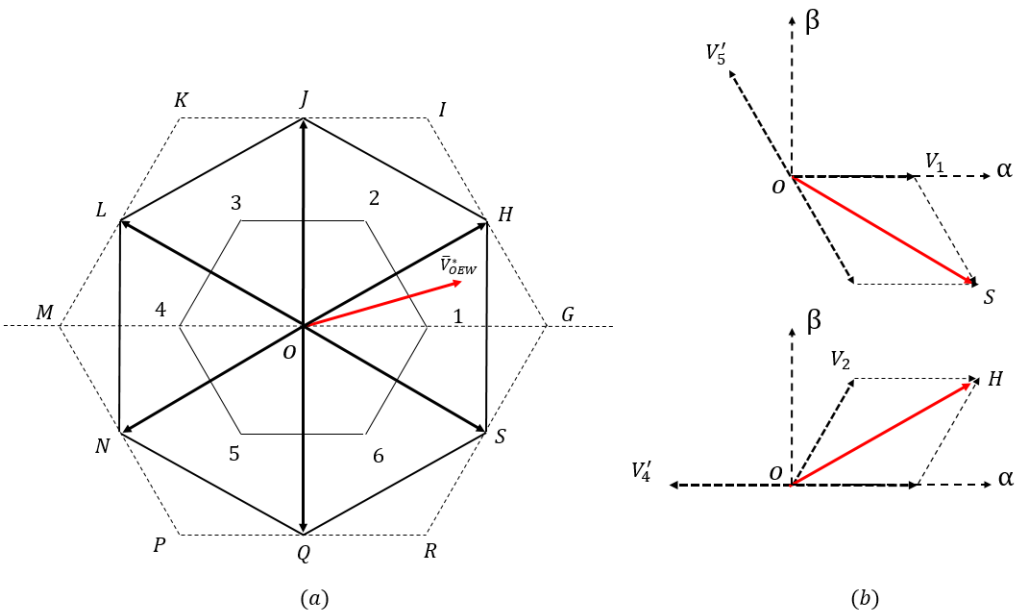


Figure 2.33: (a) Space vector combinations for the vectors which produce zero ZSV. (b)Mapping of single VSC vectors into the dual-inverter ones.

Fig. 2.33(a) shows the 19 voltage space vectors for all the possible combinations of the states of the individual inverters. As already mentioned before, among these vectors we can identify 7 voltage vectors which do not produce any ZSV. These vectors are the ones that form the hexagon HJLNQS plus the zero vector in O. The proposed modulation strategy aims to achieve the elimination of the ZSV produced by the dual-inverter. Two sequences of vectors, which have the same ZSV for the single inverter, can be identified as already presented in Section 2.7.1. Moving among the vectors 1, 3 and 5 the ZSV produced remains the same. The other sequence of vectors, which do not produce any ZSV change when transitioning from one to the other is made by the vectors 2, 4 and 6. When the reference vector $\overline{V}^*_{OEW}$ for the dual-inverter falls into sector 1 the vectors OS, OH and zero vectors are used to synthesize it. From Fig. 2.33(b) it can be noticed that the vector OS can be obtained as a combination of vectors V_1 from VSC A and V_5' from VSC B. Vector OH instead can be seen as the sum of the vectors V_2 from VSC A and V_4' from VSC B. This means that sector 1 of

VSC A and sector 3 of VSC B are uniquely mapped into sector 1 of the dual-inverter. Therefore it is intuitive to understand how every vector of the dual inverter laying on the hexagon HJLNQS can be obtained as the sum of two vectors of the individual converters. The zero vector to be used with the sequence of vectors 1,3 and 5 is obtained with the combination of vectors 1 and 1' or 3 and 3' or 5 and 5'. Similarly with the sequence of vectors 2, 4 and 6 the vectors 2 and 2' or 4 and 4' or 6 and 6' form the zero vector for the dual-inverter. The reference vector for the dual-inverter is firstly split among the two individual VSCs. Observing Fig. 2.33(b) it can be noticed that OS is transformed to $\overline{V}_1$ in VSC A which is leading OS by 30°, similarly OH is transformed in $\overline{V}_2$ which is also leading OH of 30°. Therefore also the instantaneous reference voltage $\overline{V}_A^*$ has to lead the reference vector of the dual-inverter by 30 deg as shown in (2.29)

$$\overline{V}_A^* = \frac{1}{\sqrt{(3)}} \overline{V}_{OEW}^* e^{-j30} \tag{2.29}$$

The $\alpha - \beta$ voltage reference components are then obtained; the abc reference voltages are calculated and the dwelling times are derived according to (2.24). The gate signals for VSC B are known from the knowledge of the ones of VSC A since, as explained before, each sector of VSC A is mapped into a sector of VSC B, which together they map into a sector of the dual-inverter. It should be noticed how with this modulation both the VSCs A and B are required to switch at the same switching frequency. The main drawback of any modulation that uses exclusively the combination of vectors which produce a zero ZSV is that the maximum vector that can be synthesized must be contained in the circle inscribed inside the hexagon HJLNQS, which is smaller than the circle inscribed inside the hexagon GIKMPR as seen in Fig. 2.33. In particular the radius of the larger circle is $2/\sqrt{(3)}$, while the one of the smaller circle is 1. Therefore 15% of the available dc link with the dual-inverter configuration is lost. If the same voltage limits and the additional constraint of operating inside the hexagon HJLNQS want to be kept, it is necessary to boost the dc voltage of 15% in order to

achieve the same performance.

Another modulation strategy for the dual-inverter topology based on the zero vector redistribution has been considered in [5]. The dual-inverter is used to feed an OEW-PMSM where the third harmonic of the back-EMF has been considered. In this work the elimination of the ZSC third harmonic is achieved with a proportional resonant controller (PR) placed on the 0-axis. In order to make this possible, a modulation that allows to synthesize the desired reference ZSV is necessary. Furthermore, as described in Section 2.6.5, the split of the dual-inverter voltage reference vector $\overline{V}^*_{OEW}$ among the two VSCs is done with the reference vector decomposition in two vectors of half length and opposite phase. Considering Fig. 2.22 the time of application of the individual converter vectors are

$$\begin{cases} \overline{V}^*_A T_s = \overline{V}_0 t_0 + \overline{V}_1 t_1 + \overline{V}_2 t_2 + \overline{V}_7 t_7 \\ \overline{V}^*_B T_s = \overline{V}'_0 t'_0 + \overline{V}'_5 t'_5 + \overline{V}'_4 t'_4 + \overline{V}'_7 t'_7 \\ T_s = t_0 + t_1 + t_2 + t_7 = t'_0 + t'_4 + t'_5 + t'_7 \end{cases} \tag{2.30}$$

From 2.30 the dwell times for the voltage vectors can be calculated. On the other hand if the the zero-axis voltage reference wants to be modulated the zero vector dwell times should be redistributed. According to the volt-second equivalent principle the zero vector dwell time has to be calculated to modulate the ZSV reference vector V^*_0. Each active vector and zero vector produces a ZSV, therefore according to 2.30 and Table 2.2 the reference ZSV for the two converters can be expressed as:

$$\begin{cases} V^*_{A0} T_s = -\frac{V_{dc}}{2} t_0 - \frac{V_{dc}}{6} t_1 + \frac{V_{dc}}{6} t_2 + \frac{V_{dc}}{2} t_7 \\ V^*_{B0} T_s = \frac{V_{dc}}{2} t'_0 + \frac{V_{dc}}{6} t'_4 - \frac{V_{dc}}{6} t'_5 - \frac{V_{dc}}{2} t'_7 \end{cases} \tag{2.31}$$

Furthermore, considering that the voltage on the load can be expressed as the difference of the voltages produced by the two VSCs, the following can be written:

$$V_0^* T_s = (V_{A0}^* - V_{B0}^*) T_s = \frac{V_{dc}}{2}(t_0' - t_0) + \frac{V_{dc}}{6}(t_5' - t_1) + \frac{V_{dc}}{6}(t_2 - t_4') + \frac{V_{dc}}{2}(t_7 - t_7') \quad (2.32)$$

According to (2.32) the dwell time of the zero vectors should be kept equal to V_0^* to modulate the desired ZSV. The time of application of the zero-vectors is defined as zero vector redistribution (ZVR). The ZVR is distributed equally and arranged in $\overline{V}V_0$ and $\overline{V}V_7$. Instead the dwell time of the active vectors is calculated as it would be done for a standard space vector modulation according to the references $\overline{V}_A^*$ and $\overline{V}_B^*$. The control block diagram for the proposed technique is presented in Fig. 2.34.

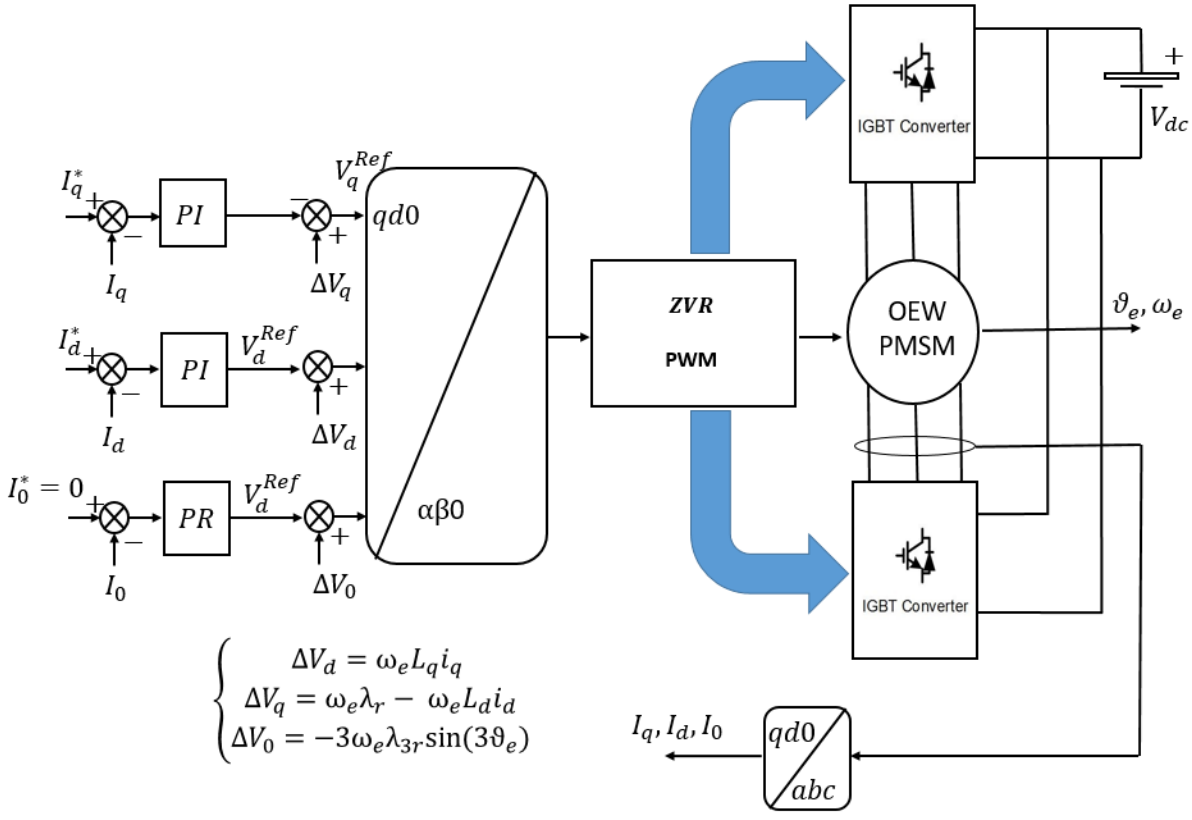


Figure 2.34: Control scheme of the OEW-PMSM system with ZVR PWM.

In [5] the machine used is a 1 kW OEW-PMSM with inductances L_q and L_d of 107.4

mH and 77.56 mH respectively. As it will be shown later, the more the machine inductances are lower the more the ZSC issues are magnified. The modulation here proposed still uses the concept of the redistribution of the zero vectors dwelling times to reduce the ZSV produced by the converters. Furthermore here the 0-axis voltage is used to eliminate the sinusoidal third harmonic back-EMF produced by the machine.

In [19] an OEW-PMSM with a self-inductance of 8.5 mH fed by a dual-inverter with common dc link is considered and the problem of circulating ZSC is addressed. The effect of the VSCs' DT on the ZSV is discussed, but no compensation method is proposed. An alternative modulation for the reduction of the ZSV is instead proposed. In order to explain the modulation introduced, a detail of the hexagon of Fig. 2.32 is shown in Fig. 2.35. Firstly the judgement of the sector in which the reference vector OV locates is done. The reference vector for the dual-inverter can be split into two segments as OV = OX + XV, where X is the centre (A, B, C, D, E and F) of the smaller hexagons. Once the hexagon of interest is located, VSC B is used to modulate the vector XV. The sub-sector in which the vector XU falls is then identified. Considering Fig. 2.32 it can be noticed that the hexagon in which the dual-inverter reference vector is the one with centre A and the sub-sector is number 1 as shown in 2.35. The dwell times are calculated as it would be done for a standard SVM; in this case the sequence of vectors $V_0 - V_1 - V_2 - V_0$ is obtained. As already done for the previous modulations, the ZSV produced by the sequence of vectors used to modulate the reference vector can be calculated. A redistribution factor x that splits the zero-sequence vector is proposed as

$$T_0 = x\frac{T_0}{2} + (1-x)\frac{T_0}{2} \tag{2.33}$$

As already seen for previous works, the redistribution factor x can be used to modulate the reference ZSV. In [19] the converter that is clamped to the centre of the hexagon is always VSC A while in [110, 111] the two VSCs are alternatively clamped to a voltage vector.

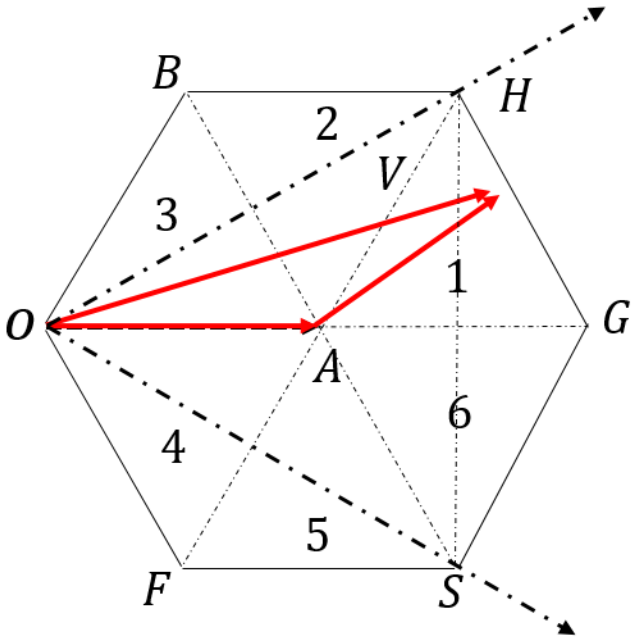


Figure 2.35: Dual-space Vector Control principle for sector I.

Furthermore in [110, 111] the zero-vectors redistribution is used to eliminate the average ZSV while in [19] the redistribution factor is used to modulate the reference ZSV coming from a 0-axis PI. In this modulation [19] VSC A is always clamped to one of the 6 active vectors while VSC B is switching, furthermore VSC B can use all the vectors as it would be done in a standard SVM. Consequently the whole hexagon GIKMPR can be exploited; on the other hand the ZSV synthesized will not be instantaneously zero.

A more interesting approach to the elimination of the ZSV produced by the dual-inverter structure has been investigated in [112]. A generalized carrier-based PWM technique for OEWM drives that completely eliminates the ZSV has been proposed. The method has been applied to both dual two-level VSC and dual matrix converter

based OEW drives. Furthermore the computation resources for PWM and SVM methods have been compared showing that the carrier-based method requires significantly less computational effort. As done in 2.33 the smaller hexagon HJLNQS is used to modulate the reference vector for the dual-inverter. This hexagon is made of the space voltage vectors which have a zero ZSV component. The output vector could be in one of the six sectors and the two space vectors bounding that sector are used to synthesize the output voltage vector on an average over a switching cycle. For example in Fig. 2.33 the output voltage vector is in sector 1, so the space vectors OS and OH are to be used to synthesize it. Suppose, the duty ratios of OS, OH and the zero vector are d1, d2, and d_{zero} (where $d_{zero} = 1-(d1+d2)$) respectively. Then, the output voltage vector is synthesized as

$$\overline{V}^{*}_{OEW} = d_1\overline{V}_{OS} + d_2\overline{V}_{OH} + (1 - d_1 - d_2)\overline{V}_{zero} \tag{2.34}$$

Considering that the voltage vectors OS and OH can be written as

$$\begin{cases} \overline{V}_{OH} = \overline{V}_1 + \overline{V}^{'}_5 \\ \overline{V}_{OS} = \overline{V}_2 + \overline{V}^{'}_4 \\ \overline{V}_{zero} = \overline{V}_1 + \overline{V}^{'}_4 \end{cases} \tag{2.35}$$

and substituting 2.35 into 2.34 the following equation is obtained

$$\overline{V}^{*}_{OEW} = \overline{V}_1 + d_1\overline{V}^{'}_5 + d_2\overline{V}^{'}_2 + (1 - d_1 - d_2)\overline{V}^{'}_4 \tag{2.36}$$

From 2.36 it is observed that the VSC A vector $\overline{V}_1$ is ON for the entire switching period. The VSC B vectors $\overline{V}^{'}_5$ and $\overline{V}^{'}_2$ are ON with duty ratios d1 and d2 , respectively, while the vector $\overline{V}^{'}_4$ is ON for the remaining period, i.e., with a duty ratio of d_{zero} in a switching cycle. It can be noticed that in this modulation strategy for the dual VSC,

the proposed PWM scheme uses only one set of vectors out of the two sequences that have same ZSV produced. The advantage of the method proposed is the possibility to apply the duties as it would be done for a standard PWM. Furthermore, it can be noticed that for the dual-inverter the reference modulation indexes (MIs) for each phase are

$$\begin{cases} m_x = \frac{V^*_{aa'}}{V_{dc}} \\ m_y = \frac{V^*_{bb'}}{V_{dc}} \\ m_z = \frac{V^*_{cc'}}{V_{dc}} \end{cases} \tag{2.37}$$

For the dual two-level inverter, the MIs are equal to reference phase voltages divided by the dc bus voltage (V_{dc}). Fig. 2.36 shows the voltage vectors of VSC A and VSC B used to obtain the voltage vectors of the hexagon HJLNQS which have zero ZSV.

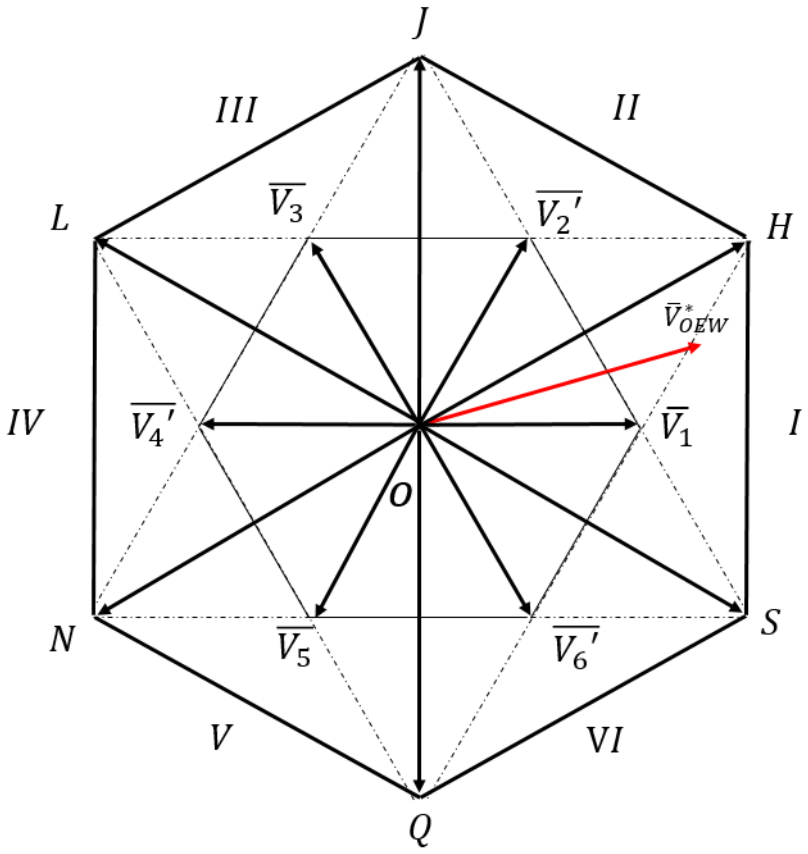


Figure 2.36: Space Vectors used for the dual-inverter reference voltage modulation.

When the reference vector $\overline{V}^*_{OEW}$ falls in sectors I, III and V, VSC A is clamped while VSC B is switching. Similarly when the reference falls in sectors II, IV and VI, VSC B gets clamped while the VSC A is switching. The duty cycles for the two converters for each sector are show in Table 2.9.

Table 2.9: Duty Ratios in terms of MIs for the SVPWM

Duty Ratio	I	II	III	IV	V	VI
$d_{\overline{V}_1}$	1	0	0	$1-m_x$	m_x	m_x
$d_{\overline{V}_3}$	0	1	0	m_y	$1-m_y$	m_y
$d_{\overline{V}_5}$	0	0	1	m_z	m_z	$1-m_z$
$d_{\overline{V}_2'}$	$1-m_x$	m_x	m_x	1	0	0
$d_{\overline{V}_4'}$	m_y	$1-m_y$	m_y	0	1	0
$d_{\overline{V}_6'}$	m_z	m_z	$1-m_z$	0	0	1

From Table 2.9 the MIs for the two standard VSCs of the dual-inverter topology are shown. If sector I is considered, for VSC A the voltage vector $\overline{V}_1$ is applied for the entire sample time, while the vectors $\overline{V}_3$ and $\overline{V}_4$ are not applied at all. VSC B modulates between the vectors $\overline{V}_2^{'}, \overline{V}_4^{'}$ and $\overline{V}_6^{'}$ with the duties $1-m_x, m_y$ and m_z respectively. Therefore from the knowledge of the MIs from (2.37) and how they should be applied in every sector (Table 2.9), the duties for the two converters to be applied to a standard sawtooth PWM can be found. Fig. 2.37 shows the duties for the two VSCs. It can be noticed how at each duty is associated a space voltage vector and not the state of an individual inverter leg.

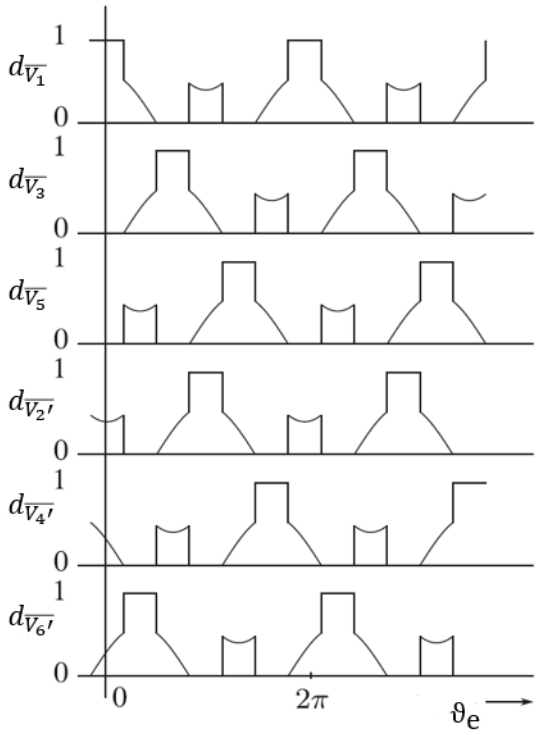


Figure 2.37: Duty ratio waveforms for VSC A and VSC B.

In [112] a detailed analysis shows the relationship and a comparison in terms of computational effort of the PWM method with the space-vector-based modulation technique. The performance of the carrier-based method in terms of resources consumed and execution time is confirmed by implementation of both algorithms on an FPGA-based real-time control platform.

Concluding, it can be highlighted that among all the modulation proposed, many are based on the ZVR to achieve the reduction of the average ZSV [19, 106, 109–111]. [5] is still based on the ZVR, but this technique is used to modulate the zero-sequence reference voltage calculated from a resonant PI to achieve the elimination of the third harmonic back-EMF ZSV. Both [35] and [112] use the smaller hexagon HJLNQS to achieve instantaneous ZSV elimination and require both VSCs A and B to switch

alternatively.

2.9 Power Converter's non-linearities Influence on Drives' Performance and ZSV analysis

It is well known that power devices behaviour is far from linear, especially at low current amplitudes. A distortion of the output voltage of the power converter is caused by its non-linearities. Particularly for high performance drives, where accurate voltage needs to be applied, the voltage non-linearities can cause a significant degradation of the performances. If the distortion is not accurately modelled, the voltage that is thought to be supplied will be different from the real one. The total distortion of the output voltage can be attributed to two main non-linear behaviours:

1. the switch Dead-Time (DT) used for avoiding short-circuit occurrence on the converter leg.
2. Voltage Drops across current carrying semiconductor devices.

The DT and the voltage drops represent the 80% and 15% of the total distortion respectively, the remaining 5% can be attributed to other effects such as turn on/off delays of active switches, effects of parasitic capacitance on rise/fall times and the zero current clamping effect [113]. Accurate modelling of the DT has been done in [114, 115]. As the switching frequency and/or the desired performances are pushed up, the distortions on the output voltages due to the non ideal inverter behaviour may become unacceptable, not only in open-loop systems [116] but also in closed-loop controlled systems especially when advanced techniques such as sensorless control [117, 118], parameters estimation [119] or predictive current control [118, 120] are used. In [118] the Finite State Model Predictive Controller (FS-MPC) has been implemented for a PMSM drive with a sensorless position control. The machine voltage equations are used to predict the current future state therefore any mismatch in the model would cause a prediction error and therefore performance reduction. Techniques for

feed-forward compensation of the DTs and voltage drops are proposed in [114, 121, 122]. These methods need an off-line identification of the inverter parameters while in [123] the identification is done at the start up by injecting a set of dc and ac currents. In [124] a self-commissioning algorithm for the identification of the VSC's non-linearities has been proposed. In a current-controlled drive the fast response of the current regulators deforms the reference voltage in order to keep the currents sinusoidal. In this case, the motor voltages are sinusoidal, and the reference voltages are deformed instead. If such deformed signals are used for flux estimation, both the amplitude error and harmonic distortion that affect the voltages are reflected onto the flux estimate. At low speed, the voltage reference distortion becomes evident in comparison with the fundamental motor voltage and gives a relevant flux estimation error. The estimated flux is also deformed, and field orientation becomes inaccurate. The dual-inverter topology can be better analysed if approached with the study of the individual standard two-level VSCs. Firstly the voltage non-linearities of the standard two-level converter are analysed and after the analysis is extended to the dual-inverter topology. In this Thesis the devices voltage drops are neglected since this voltage is negligible compared to the dc bus voltage. The effect of the dead-time on the ZSV is the main focus of this thesis and it will be discussed in the following chapters.

2.9.1 VSC DT Compensation Techniques

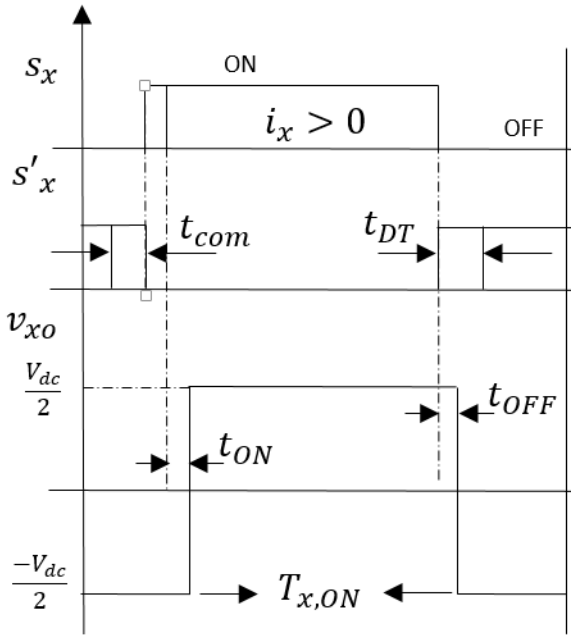


Figure 2.38: Dead time effect on inverter pole voltage

VSC's voltage distortion due to the DT has been investigated in many works [125–130]; only few papers have mentioned the voltage distortion caused by the non-ideal characteristic of the switching device such as turn-on and turn-off time [129], voltage transition slope [130], and voltage drop effect [129]. To accurately compensate these effects, all the previously mentioned parameters of the switching device should be known, and these are not exactly measurable and are dependent on the operating point. In some works the knowledge of the switching device characteristics is assumed [129]. Consequently, if all these parameters are not taken into account the voltage distortion compensation is not guaranteed. In the following the most relevant DT compensation methods for the work done in this thesis are presented. From Fig. 2.38 the actual deviation of the desired reference time for a converter leg from the real one due to the DT can be written as

$$t_d = t_{off} - t_{on} + t_{com} - t_{DT} \tag{2.38}$$

where t_{off} and t_{on} are the off and on times for the upper switching device, t_{com} is the compensation time that can be set to avoid the voltage distortion and t_{DT} is the DT. t_{com} has to be considered as a control variable; $t_{com} = 0$ correspond to the case in which no compensation strategy is implemented. Therefore for each converter leg the reference time can be corrected according to

$$T_{x,ON} = T^*_{x,ON} + t_d sign(i_x) \tag{2.39}$$

where x stands for the converter phase a,b or c and $sign(i_x)$ is 1 if the current flows to the load and -1 if it flows to the dc link. In [125] an additional circuit is used to measure the phase voltage distortion due to the DT effect. A comparison between the phase voltage signal and the ideal gate pulse is made, the delay introduced by the DT effect is measured and stored to be applied at the next gate change of state. The method proposed not only needs additional hardware components, but also introduces a phase shift in the applied voltages. In [131] the most simple DT compensation is presented, a feed forward compensation is used according to (2.39). When the phase current is positive the output voltage is reduced and when the current is negative the output voltage is increased. In [114] the analysis of the voltage distortion is discussed with consideration of the DT effect and voltage drop of the power devices. The characteristic of the switching devices have been considered in the analysis, but it is shown that the compensation method used does not require their knowledge. Another compensation technique, which is going to be adapted in this work to be used in conjunction with the SVM developed for the dual-inverter configuration, is the Pulse Based Dead Time Compensator (PBDTC) [132]. With the PBDTC the DT compensation is achieved by updating the turn-on time of the power devices at the beginning of a PWM cycle and the turn-off time at the midpoint of the PWM

cycle. The compensation is based on the phase current polarity detection. The PBDTC method achieves the optimum correction since a compensation pulse by pulse is applied. The method provides stable operation since it does not introduce any change in magnitude and phase of the applied voltage. Furthermore the PBDTC is independent of operating frequency, carrier frequency and load. Furthermore it is also compatible with digital controllers. The compensation technique is applied individually for every converter leg, this feature makes it particularly easy to be extended to different converter topologies such as the dual-inverter structure.

2.9.2 Dual-Inverter DT Analysis

The analysis of the DT effect on the dual-inverter topology has been carried out in [16, 19]. Let's consider the case of Fig. 2.36 where the reference voltage vector lays in sector I. In order to determine the ZSV distortion introduced by the DT the current paths have to be identified.

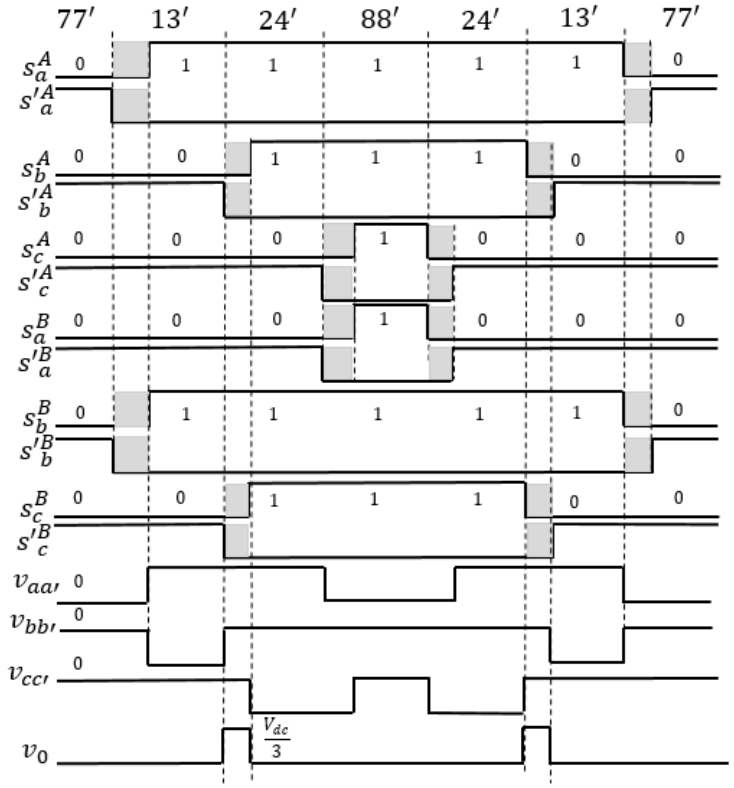


Figure 2.39: ZSV caused by DT during when the reference vector is in Sector I and the phase currents are $i_a > 0$, $i_b < 0$, $i_c < 0$

The reference vector is obtained with the switching pattern of Fig. 2.39 where the phase currents are supposed to be $i_a > 0$, $i_b < 0$, $i_c < 0$. The DT distortion happens in the transitions from vector 77' to 13', from 13' to 24' and from 24' to 88'. The leg gate signals and the currents paths during the DT are shown in Fig. 2.40 where the DT is highlighted with a grey area.

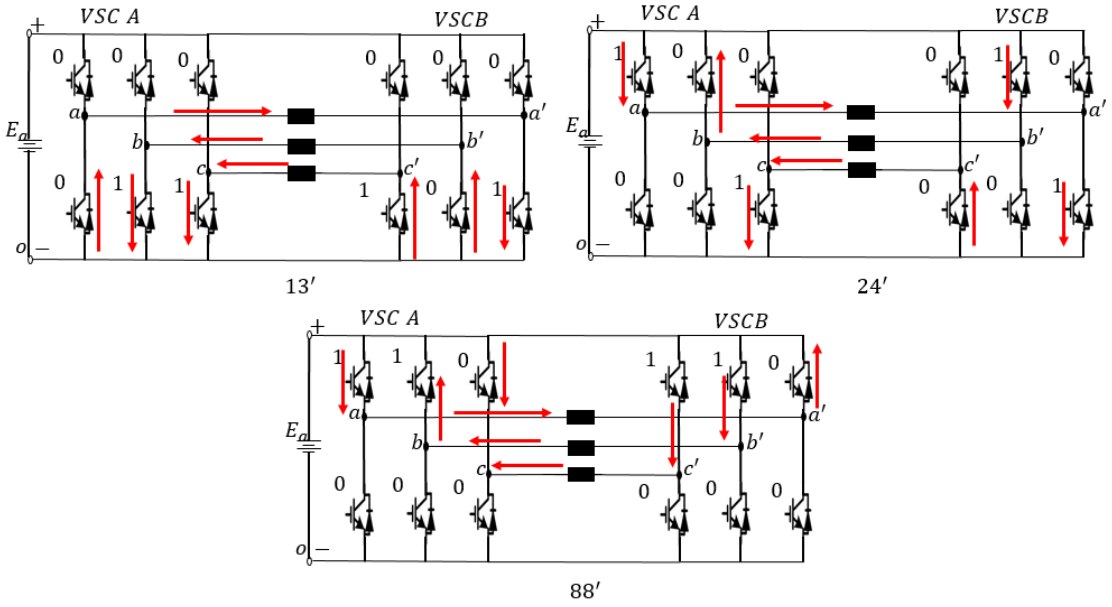


Figure 2.40: Current conducting paths during DT for 13', 24' and 88' under $i_a > 0$, $i_b < 0$, $i_c < 0$

For example, during the DT, when the voltage vector 13' is applied, s_a^A and $s_a^{'A}$ are both turned off therefore leaving the lower diode as the only possible path for the positive phase current. In the switching mode 24' the three phase voltages are V_{dc}, 0 and 0 respectively which leads to the ZSV with amplitude $\frac{V_{dc}}{3}$. It can be noticed that in the process of transition from 77' to 13' there are two simultaneous rising edges for s_a^A and s_b^B and two simultaneous trailing edges for $s_a^{'A}$ and $s_b^{'B}$. The rise and fall time of a switching device are different but the rise times of different switching devices in the same converter are approximately identical and the same can be said for the falling times. Therefore the rising slope of the phase voltage $v_{aa'}$ and the trailing slope of $v_{bb'}$ are almost the same. The rise and fall times have an effect on the ZSV pulse amplitude caused by the DT, but considering that the DT is chosen in order to allow the switching device to completely turn on and off the effect of the rise and fall times can be neglected.

Table 2.10: Zero-Sequence Voltages caused by the DT

Current Modes	+ - -	+ + -	- + -	- + +	- - +	+ - +
ZSVs	$V_{dc}/3$	$-V_{dc}/3$	$V_{dc}/3$	$-V_{dc}/3$	$V_{dc}/3$	$-V_{dc}/3$
Legs	b^A, c^B	a^A, b^B	c^A, a^B	b^A, c^B	a^A, b^B	b^A, c^B

The ZSV distortion introduced by the DT does not depend on the sector but exclusively on the top switch leg transition and the phase current sign. We can define the current mode as the sign of the three phase currents which can therefore assume 3*2*1 values. For a certain current mode, the same voltages are produced in the dead time for the same switching signals, and thus they have the same zero-sequence voltages. The ZSV caused by the DT are only related to the current conducting modes, not to the sectors. Table 2.10 sums up the amplitudes of the ZSV pulses and their corresponding legs for the DT in each current mode. For the same current mode, the ZSV caused by the DT take on a series of pulses with the same amplitude of $\pm V_{dc}/3$. The ZSV caused by the DT changes every 60° therefore its frequency is three times of the fundamental waveform as shown in Fig. 2.41. Many of the work proposed in the literature either do not compensate the DT distortion [35, 111, 112] or they account for it in the average sense [19]. The mean value of the ZSV distortion caused by the DT in one switching period can be calculated observing that under the same current mode there are two pulses with the same time duration t_{DT}. Therefore, the mean of the ZSV pulses in each switching period is

$$\begin{cases} v_{0av} = \frac{2t_{DT}}{T_s}\frac{V_{DC}}{3} for(+--),(-+-),(--+) \\ v_{0av} = -\frac{2t_{DT}}{T_s}\frac{V_{DC}}{3} for(+-+),(++-),(-++) \end{cases} \tag{2.40}$$

The ZSV average within one switching period is proportional to the dc link voltage, the DT duration and the switching frequency $f_{sw} = 1/T_s$, but it is unrelated to the current amplitudes.

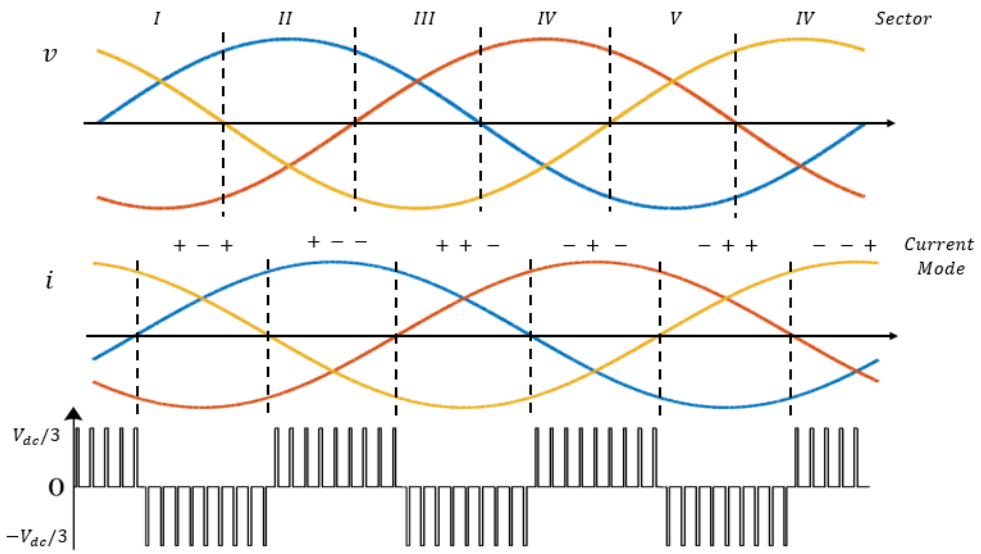


Figure 2.41: Zero-sequence voltages under different current modes. Top: Phase Voltages. Middle: Phase Currents. Bottom: DT ZSV.

2.10 Chapter Summary

In this Chapter the reasons behind the penetration of variable speed ac drives in the transportation sector have been given. In particular the case of the aerospace industry and the MEA concept have been introduced. Different topologies for the on-board PGU have been presented and because of its advantages the OEW-PMSM starter/generator fed by a dual-inverter with single dc link has been chosen as a case study for this PhD project. Different power electronics topologies that allow to achieve multilevel inversion have been presented and particular attention has been given to the dual inverter one. The possible dc link configurations have been presented and the analysis of the voltage space vectors generated by the dual inverter has been carried out. The solutions adopted to resolve the problem of circulating currents and ZSV generated by the power electronics in machine drives has been presented. The

state of the art for the modulation strategies for the dual inverter configuration with common dc link to reduce the ZSV have been presented. Furthermore the impact of the VSI non linearities on the drive performance and the ZSV generated in the dual inverter topology has been analysed.

Chapter 3

Electromagnetic Model of the Permanent Magnet Synchronous Machine

3.1 Introduction

In this chapter the electromagnetic model of a three-phase PMSM is presented as well as the OEW three phase PMSM. Firstly, the machine phase voltage equations formulation for the star connected windings is presented, secondly the state space form of the machine's equations is obtained. The machine equations are then transformed on the stationary and rotor synchronous reference frame. The transformed model is then presented in its discretized form. The equivalent circuits of the machine voltage equations both in the phase and synchronous reference frame are presented. Furthermore, the torque equation of the machine is derived and particular attention is given to the ZSC impact on the torque ripple. The PMSM equations that describe its behaviour when the star centre of the stator windings is opened are discussed. The

effects of flow of zero sequence current due to the machine non-sinusoidal back EMF is reported and analytical expression of the ZSC is given. Finally the parameters of the machines used for the simulation and experimental work are listed.

3.2 PMSM Phase Voltages Equations

From an electromechanical energy conversion point of view, a permanent magnet motor with n equally displaced identical windings is equivalent to m almost decoupled pairs of RL circuits as reported in (3.1), whose currents define the contribution of each phase current harmonic to the overall torque production [133, 134].

$$\begin{cases} m = \frac{n-1}{2} & \text{if n odd} \\ m = \frac{n}{2} & \text{if n even} \end{cases} \tag{3.1}$$

In fact, the n-dimensional space described by phase currents can be decomposed in m orthogonal two-dimensional qd subspaces, due to the circular symmetric structure of the inductance matrix of a healthy motor [135]. In case of a motors with an odd number of phases, such a decomposition identifies an additional one-dimensional subspace, still orthogonal to the m qd subspaces, which does not contribute to the electromechanical energy conversion process and it is consequently defined as zero subspace. Additionally, n-order current harmonics cannot exist on a star connected balanced motor fed by balanced voltages. All the matrix transformations that are used to do the change of variables are reported in Appendix A.

The model of the PMSM can be derived in its most generic form taking into account also a possible rotor saliency. A 2-pole, 3-phase, star connected salient-pole synchronous machine is shown in Fig. 3.1 where saliency is highlighted with an exaggerated variable air-gap between rotor and stator. Usually the synchronous machines

have more than one pole pair p but for simplicity here a single pole pair is considered since its analysis gives a model that is easily generalised. The stator windings are identical sinusoidally distributed windings, displaced 120, with N_s equivalent turns and resistance R_s and characterized by self and mutual inductances which depend on winding spatial distribution and, in case of salient rotor, also on rotor position. The a, b and c axes are the magnetic axes oriented in the positive direction of each phase winding. The rotor is equipped with a permanent magnet. The performance of nearly all types of synchronous machines may be adequately described by straightforward modifications of the equations describing the performance of the machine shown in Fig. 3.1 a). The new generic reference frame is introduced with the q and d axes. Fig. 3.1 b) shows the electrical representation of the machine stator windings when they are connected in star configuration.

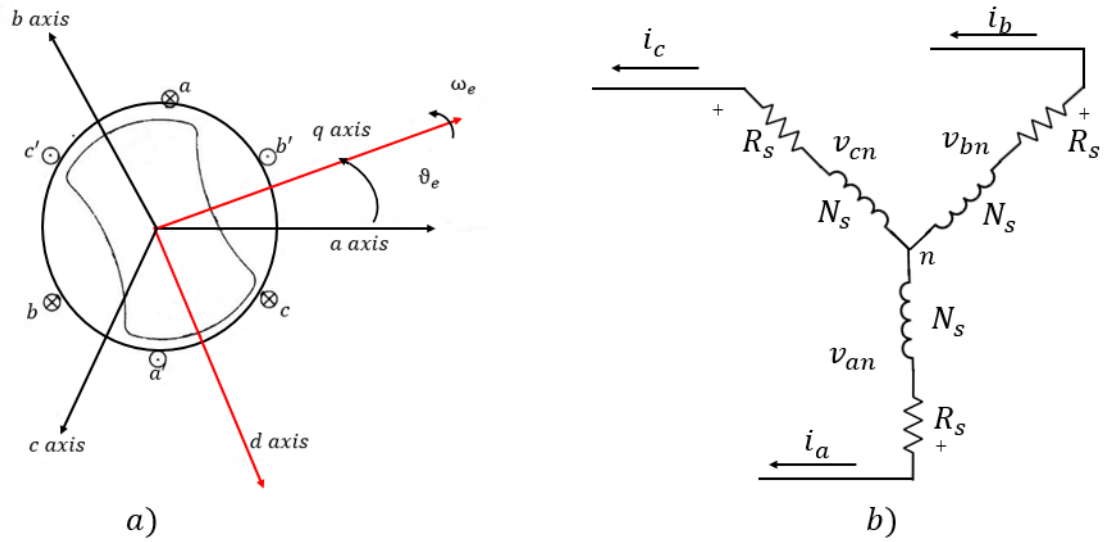


Figure 3.1: a) Two pole, 3-phase, wye-connected, salient-pole synchronous machine. b) Electrical representation of the two pole, 3-phase, wye-connected, salient-pole synchronous machine.

The following assumptions are made in the modelling derivation:

1. Core saturation is neglected.
2. Hysteresis and eddy currents losses are negligible.
3. The back-EMF is non-sinusoidal, only the third harmonic component is considered

The machine voltage and flux equations in the abc reference frame are reported in the matrix form in (3.2)

$$\begin{cases} V_{abc} = RI_{abc} + \frac{d}{dt}\lambda_{abc} \\ \lambda_{abc} = (L_{Sabc} + L_{Mabc})I_{abc} + \Lambda_r = L_{abc}I_{abc} + \Lambda_r \\ \Lambda_r = \Lambda_{1r} + \Lambda_{3r} \end{cases} \tag{3.2}$$

where R is a diagonal matrix with R_s on the diagonal. The column vectors V_{abc}, I_{abc} and λ_{abc} are the machine phase voltages, the phase currents and fluxes respectively and can be are expressed as:

$$V_{abc} = \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix}, I_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \lambda_{abc} = \begin{bmatrix} \lambda_a \\ \lambda_b \\ \lambda_c \end{bmatrix} \tag{3.3}$$

the matrices L_{Sabc}, L_{Mabc} and R are

$$L_{Sabc} = \begin{bmatrix} L_{ls} + \frac{L_d+L_q-2L_{ls}}{3} & -\frac{1}{2}\frac{L_d+L_q-2L_{ls}}{3} & -\frac{1}{2}\frac{L_d+L_q-2L_{ls}}{3} \\ -\frac{1}{2}\frac{L_d+L_q-2L_{ls}}{3} & L_{ls} + \frac{L_d+L_q-2L_{ls}}{3} & -\frac{1}{2}\frac{L_d+L_q-2L_{ls}}{3} \\ -\frac{1}{2}\frac{L_d+L_q-2L_{ls}}{3} & -\frac{1}{2}\frac{L_d+L_q-2L_{ls}}{3} & L_{ls} + \frac{L_d+L_q-2L_{ls}}{3} \end{bmatrix} \tag{3.4}$$

$$L_{Mabc} = \frac{L_q - L_d}{3} \begin{bmatrix} cos(2\theta_e) & cos2(\theta_e - \frac{\pi}{3}) & cos2(\theta_e + \frac{\pi}{3}) \\ cos2(\theta_e - \frac{\pi}{3}) & cos2(\theta_e - \frac{2\pi}{3}) & cos2(\theta_e + \pi) \\ cos2(\theta_e + \frac{\pi}{3}) & cos2(\theta_e + \pi) & cos2(\theta_e + \frac{2\pi}{3}) \end{bmatrix} \tag{3.5}$$

$$R = \begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix} \tag{3.6}$$

where L_{ls} is the leakage inductance of each stator winding, θ_e is the electrical rotor position, L_q and L_d are the q-axis and d-axis inductances whose significance will be cleared later. The matrices were determined under these assumptions:

1. stator windings are identical and sinusoidally distributed
2. machine airgap length varies along stator inner circumference.

L_{Sabc} is a matrix describing the static self and mutual inductances due to windings reciprocal position and spatial distribution, L_{Mabc} is a matrix describing the influence of rotor position, due to its magnetic anisotropy, on self and mutual inductances. The phase inductances matrix L_{abc} which takes into considerations both the L_{Sabc} and L_{Mabc} components is defined as follows

$$L_{abc} = L_{Sabc} + L_{Mabc} \tag{3.7}$$

Λ_r is the matrix that describes the permanent magnets flux linkage on each motor phase as a function of the rotor position. The rotor's permanent magnets flux linkage with the stator windings Λ_r can be decomposed with the Fourier series in its fundamental Λ_{1r} and third harmonic component Λ_{3r}. Λ_{1r} and Λ_{3r} are reported in (3.8) and (3.9) respectively. λ_m is the peak flux linkage established by the rotor permanent magnets. $k_{3\lambda}$ is defined as the ratio between the third harmonic flux and λ_m.

$$\Lambda_{1r} = \lambda_m \left[sin(\theta_e) \quad sin(\theta_e - \tfrac{2\pi}{3}) \quad sin(\theta_e + \tfrac{2\pi}{3}) \right]^T \tag{3.8}$$

$$\Lambda_{3r} = \lambda_m k_{3\lambda} \left[sin(3\theta_e) \quad sin(3\theta_e) \quad sin(3\theta_e) \right]^T \tag{3.9}$$

The machine model in phase coordinates is described by (3.2). The state-space representation of the system is particularly useful both for control design and machine equations simulation, in fact the differential of the state variables (i.e. the phase currents) can be integrated to find the present values of the currents, their measurement can then be used to close a control loop and simulate the behaviour of the entire system. Rearranging (3.2) by firstly substituting the fluxes expression in the phase voltages equation and secondly rewriting it according to the state-space representation the following equations are obtained (3.10)

$$\frac{d}{dt} I_{abc} = L_{abc}^{-1} \left[V_{abc} - R I_{abc} - \frac{d}{dt}(L_{abc}) I_{abc} - \frac{d}{dt}(\Lambda_r) \right] \tag{3.10}$$

The inputs $I_{abc}, V_{abc}, \omega_e$ and ϑ_e are fed into (3.10). The output state is then integrated to obtain the phase currents. Another, and equivalent method to the one previously discussed to simulate the machine's behaviour is to use the equivalent electrical circuit representation of (3.2). The model can be implemented with its equivalent circuit as shown in Fig. 3.2. The equivalent circuit is obtained from (3.2) simply by expanding the equations. It can be noticed that the derivative terms are obtained from the voltage drops over the phase inductors. This representation of the machine will be used later when simulating the entire system composed by the machine, the PE and the digital controller.

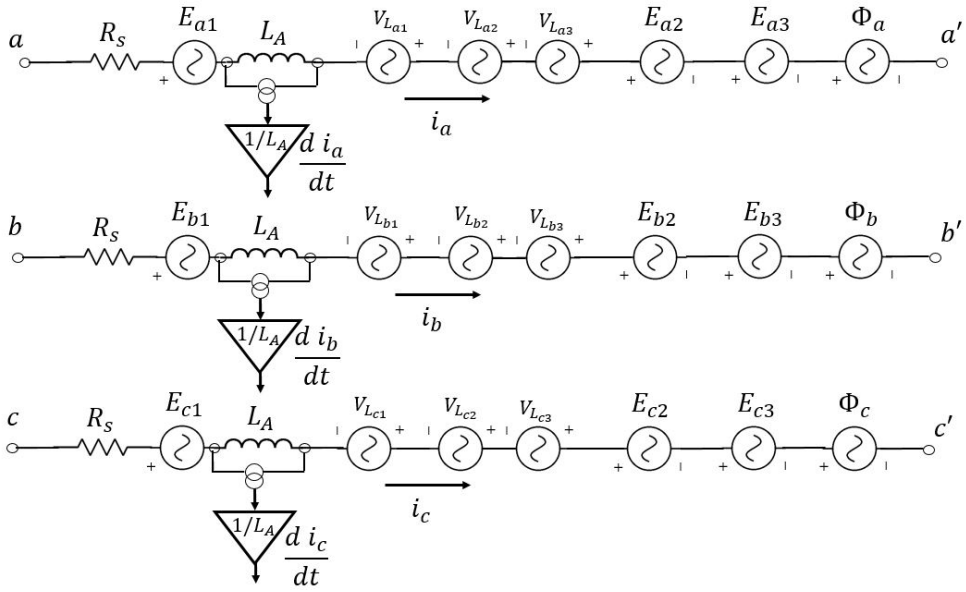


Figure 3.2: Phase voltages equivalent circuit.

By expanding the equations (3.10) the terms $E_{j1}, E_{j2}, E_{j3}, L_{j1}, L_{j2}, L_{j3}$ and Φ_j where j can assume the values a, b or c representing the three machine phases can be found and are reported in (3.11), (3.12) and (3.13).

$$\begin{cases} E_{a1} = 2L_B\omega_e sin(2\theta_e)i_a \\ E_{a2} = 2L_B\omega_e sin(2\theta_e - \frac{2\pi}{3})i_b \\ E_{a3} = 2L_B\omega_e sin(2\theta_e + \frac{2\pi}{3})i_c \\ V_{L_{a1}} = [L_{ls} - L_B cos(2\theta_e)]\frac{di_a}{dt} \\ V_{L_{a2}} = [\frac{L_A}{2} + L_B cos(2\theta_e - \frac{2\pi}{3})]\frac{di_b}{dt} \\ V_{L_{a3}} = [\frac{L_A}{2} + L_B cos(2\theta_e + \frac{2\pi}{3})]\frac{di_c}{dt} \\ \Phi_a = \lambda_m\omega_e cos(\theta_e) + 3\lambda_m K_{3\lambda}\omega_e cos(3\theta_e) \end{cases} \tag{3.11}$$

$$\begin{cases} E_{b1} = 2L_B\omega_e sin(2\theta_e + \frac{2\pi}{3})i_b \\ E_{b2} = 2L_B\omega_e sin(2\theta_e - \frac{2\pi}{3})i_a \\ E_{b3} = 2L_B\omega_e sin(2\theta_e)i_c \\ V_{L_{b1}} = [\frac{L_A}{2} + L_B cos(2\theta_e - \frac{2\pi}{3})]\frac{di_a}{dt} \\ V_{L_{b2}} = [L_{ls} - L_B cos(2\theta_e + \frac{2\pi}{3})]\frac{di_b}{dt} \\ V_{L_{b3}} = [\frac{L_A}{2} + L_B cos(2\theta_e)]\frac{di_c}{dt} \\ \Phi_b = \lambda_m\omega_e cos(\theta_e - \frac{2\pi}{3}) + 3\lambda_m K_{3\lambda}\omega_e cos(3\theta_e) \end{cases} \tag{3.12}$$

$$\begin{cases} E_{c1} = 2L_B\omega_e sin(2\theta_e - \frac{2\pi}{3})i_c \\ E_{c2} = 2L_B\omega_e sin(2\theta_e + \frac{2\pi}{3})i_a \\ E_{c3} = 2L_B\omega_e sin(2\theta_e)i_b \\ V_{L_{c1}} = [\frac{L_A}{2} + L_B cos(2\theta_e + \frac{2\pi}{3})]\frac{di_a}{dt} \\ V_{L_{c2}} = [\frac{L_A}{2} + L_B cos(2\theta_e)]\frac{di_b}{dt} \\ V_{L_{c3}} = [L_{ls} - L_B cos(2\theta_e - \frac{2\pi}{3})]\frac{di_c}{dt} \\ \Phi_c = \lambda_m\omega_e cos(\theta_e + \frac{2\pi}{3}) + 3\lambda_m K_{3\lambda}\omega_e cos(3\theta_e) \end{cases} \tag{3.13}$$

The inductances L_A and L_B can be expressed as a combination of the q and d inductances as shown in (3.14)

$$\begin{cases} L_A = \frac{L_d + L_q - 2L_{ls}}{3} \\ L_B = \frac{L_d - L_q}{3} \end{cases} \tag{3.14}$$

3.3 Mathematical model in rotor qd0 coordinates

The machine phase voltages model can be transformed on the synchronous reference frame by using the matrix transformation of Appendix A. The qd0 PMSM model is obtained multiplying (3.2) for the transformation matrix $\mathbf{T}_P(\vartheta_e)$.

$$\begin{cases} V_{qd0} = \mathbf{T}_P(\vartheta_e)V_{abc} = \mathbf{T}_P(\vartheta_e)R\mathbf{T}_P^{-1}(\vartheta_e)I_{qd0} + \mathbf{T}_P(\vartheta_e)\frac{d}{dt}(\mathbf{T}_P^{-1}(\vartheta_e)\lambda_{qd0}) \\ \lambda_{qd0} = \mathbf{T}_P(\vartheta_e)\lambda_{abc} = \mathbf{T}_P(\vartheta_e)L_{abc}\mathbf{T}_P^{-1}(\vartheta_e)I_{qd0} + \mathbf{T}_P(\vartheta_e)\Lambda_r \end{cases} \tag{3.15}$$

where V_{qd0}, I_{qd0} and λ_{qd0} are

$$V_{qd0} = \begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix}, \; I_{qd0} = \begin{bmatrix} i_q \\ i_d \\ i_0 \end{bmatrix}, \lambda_{qd0} = \begin{bmatrix} \lambda_q \\ \lambda_d \\ \lambda_0 \end{bmatrix} \tag{3.16}$$

and where

$$\begin{cases} \mathbf{T}_P(\vartheta_e)R\mathbf{T}_P^{-1}(\vartheta_e) = R \\ \\ \mathbf{T}_P(\vartheta_e)L_{abc}\mathbf{T}_P^{-1}(\vartheta_e) = L_{qd0} = \begin{bmatrix} L_q & 0 & 0 \\ 0 & L_d & 0 \\ 0 & 0 & L_{Ls} \end{bmatrix} \end{cases} \tag{3.17}$$

The inductances matrix transformed on the qd0 reference frame is a diagonal matrix that has as elements the L_q, L_d and L_{Ls} inductances. It can be noticed that on the zero-axis the equivalent inductance is the leakage inductance L_{Ls}. Exclusively for ease of reference we will refer to the zero-axis inductance as L_0 instead of L_{Ls}. By substituting the qd0 fluxes equation into the qd0 voltage one, (3.18) is obtained

$$V_{qd0} = RI_{qd0} + \mathbf{T}_P(\vartheta_e)\frac{d}{dt}(\mathbf{T}_P^{-1}(\vartheta_e)L_{qd0}I_{qd0} + \Lambda_r) = RI_{qd0} + \\ \mathbf{T}_P(\vartheta_e)\frac{d}{dt}(\mathbf{T}_P^{-1}(\vartheta_e))L_{qd0}I_{qd0} + \mathbf{T}_P(\vartheta_e)\mathbf{T}_P^{-1}(\vartheta_e)\frac{d}{dt}(L_{qd0}I_{qd0}) + \mathbf{T}_P(\vartheta_e)\frac{d}{dt}\Lambda_r \tag{3.18}$$

Developing the matrices products the terms of (3.18) become

$$\mathbf{T}_P(\vartheta_e)\frac{d}{dt}(\mathbf{T}_P^{-1}(\vartheta_e))L_{qd0} = \omega_e \begin{bmatrix} 0 & L_d & 0 \\ -L_q & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{3.19}$$

$$\mathbf{T}_P(\vartheta_e)\frac{d}{dt}\Lambda_r = \mathbf{T}_P(\vartheta_e)(\frac{d}{dt}\Lambda_{1r} + \frac{d}{dt}\Lambda_{3r}) = \lambda_m\omega_e \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} + \lambda_m\omega_e k_{3\lambda} \begin{bmatrix} 0 \\ 0 \\ 3cos(3\vartheta_e) \end{bmatrix} \tag{3.20}$$

Finally the machine voltage equations in the qd0 synchronous reference frame are

$$V_{qd0} = \begin{bmatrix} R_s & \omega_e L_d & 0 \\ -\omega_e L_q & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix} \begin{bmatrix} i_q \\ i_d \\ i_0 \end{bmatrix} + L_{qd0}\frac{d}{dt} \begin{bmatrix} i_q \\ i_d \\ i_0 \end{bmatrix} + \begin{bmatrix} \omega_e\lambda_m \\ 0 \\ 3\omega_e\lambda_m k_{3\lambda} cos(3\theta_e) \end{bmatrix} \tag{3.21}$$

where ω_e is the machine electrical pulsation. For a PMSM with the stator windings connected in star configuration the third line of 3.21 can be neglected since no circulation of ZSC is allowed. The PMSM state variables therefore reduce to two phase currents since the sum of the three phase currents is zero. The machine equations neglecting the 0-axis are described by

$$V_{qd} = \begin{bmatrix} R_s & \omega_e L_d \\ -\omega_e L_q & R_s \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} L_q & 0 \\ 0 & L_d \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} \omega_e\lambda_m \\ 0 \end{bmatrix} \tag{3.22}$$

3.3.1 State-space representation in the qd0 Synchronous Reference Frame

The state space representation in the qd0 coordinates is of particular interest because it can be used for the controller synthesis. Rearranging (3.21) according to the state space form by collecting the machine states, i.e. the phase currents, the following system is obtained

$$\frac{d}{dt}I_{qd0} = \begin{bmatrix} \frac{-R_s}{L_q} & \frac{-\omega_e L_d}{L_q} & 0 \\ \frac{\omega_e L_q}{L_d} & \frac{-R_s}{L_d} & 0 \\ 0 & 0 & \frac{-R_s}{L_0} \end{bmatrix} \begin{bmatrix} i_q \\ i_d \\ i_0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_q} & 0 & 0 \\ 0 & \frac{1}{L_d} & 0 \\ 0 & 0 & \frac{1}{L_0} \end{bmatrix} \begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} - \begin{bmatrix} \frac{\omega_e \lambda_m}{L_q} \\ 0 \\ \frac{3\omega_e \lambda_m k_{3\lambda} cos(3\theta_e)}{L_0} \end{bmatrix} \tag{3.23}$$

where

$$A = \begin{bmatrix} \frac{-R_s}{L_q} & \frac{-\omega_e L_d}{L_q} & 0 \\ \frac{\omega_e L_q}{L_d} & \frac{-R_s}{L_d} & 0 \\ 0 & 0 & \frac{-R_s}{L_0} \end{bmatrix}; B = \begin{bmatrix} \frac{1}{L_q} & 0 & 0 \\ 0 & \frac{1}{L_d} & 0 \\ 0 & 0 & \frac{1}{L_0} \end{bmatrix}; B_\lambda = \begin{bmatrix} \frac{\omega_e \lambda_m}{L_q} \\ 0 \\ \frac{3\omega_e \lambda_m k_{3\lambda} cos(3\theta_e)}{L_0} \end{bmatrix}$$

3.3.2 PMSM Equivalent Circuits in the qd0 Synchronous Reference Frame

As it has been done for the PMSM model in the phase voltages abc reference frame the equivalent circuit of the machine can be obtained from the mathematical model also in the qd0 reference frame. It is particularly useful to have a circuital representation of the machine model because it could be used for simulation analysis and evaluation

of the behaviour of the motor on the individual axes. Considering each row of 3.21 the machine equivalent circuits for the qd0 coordinates can be obtained.

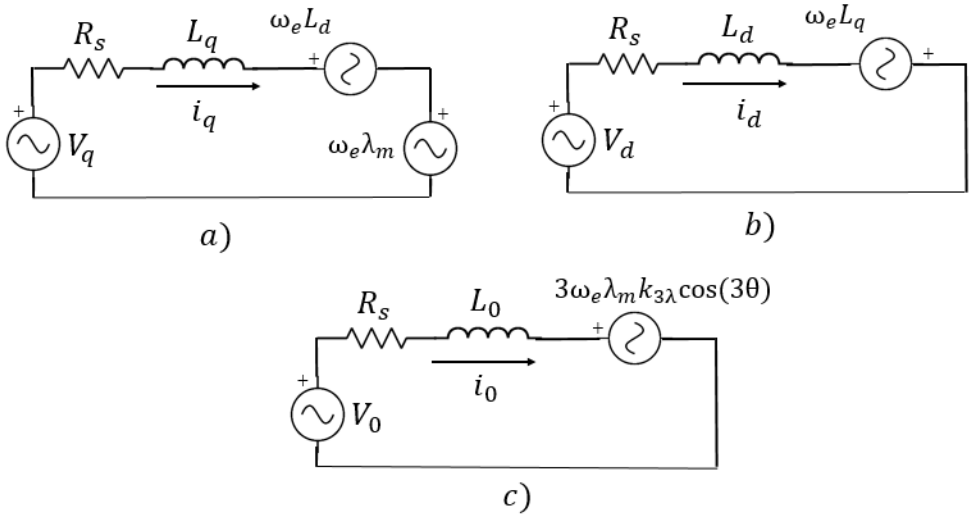


Figure 3.3: Equivalent circuits of the PMSM in the qd0 reference frame. (a) q-axis equivalent circuit; (b) d-axis equivalent circuit; (c) 0-axis equivalent circuit

It can be noticed that each axis is characterized by an RL circuit excited by the corresponding voltage component produced by the converter feeding the machine. The q and d axis also present mutual couplings which need to be taken into account when designing a controller. Furthermore, the q and 0 axis present the fundamental and third harmonic back EMF voltages, respectively. The equivalent circuits in the qd0 reference frame will be particularly useful when making considerations on the zero-axis machine behaviour.

3.4 Discretisation of the qd0 PMSM Model

Since the PMSM models will be used in simulations and for practical implementation it is necessary to make them suitable for numerical evaluation and implementation on

digital controllers. In this paragraph the process that leads to the discretized PMSMs model is presented. In order to solve the model equations we need to go through the solution of differential equations that constitute the system model. According to Appendix B and (3.23) the discrete expression of the system matrices is

$$\Phi = e^{AT_s}; \Gamma = \int_0^{T_s} e^{A\tau} d\tau B \tag{3.24}$$

By Taylor expansion of the exponential matrix and truncating it at the first order the matrices Φ and Γ become

$$\Phi = \begin{bmatrix} 1 - \frac{R_s T_s}{L_q} & -\frac{\omega_{ek} L_d T_s}{L_q} & 0 \\ \frac{\omega_{ek} L_q T_s}{L_d} & 1 - \frac{R_s T_s}{L_d} & 0 \\ 0 & 0 & 1 - \frac{R_s T_s}{L_0} \end{bmatrix} \Gamma = \begin{bmatrix} \frac{T_s}{L_q} & 0 & 0 \\ 0 & \frac{T_s}{L_d} & \\ 0 & 0 & \frac{T_s}{L_0} \end{bmatrix} \tag{3.25}$$

Finally the discretized equations of the PMSM are the following

$$\begin{bmatrix} i_{k+1}^q \\ i_{k+1}^d \\ i_{k+1}^0 \end{bmatrix} = \Phi \begin{bmatrix} i_k^q \\ i_k^d \\ i_k^0 \end{bmatrix} + \Gamma \begin{bmatrix} V_k^q \\ V_k^d \\ V_k^0 \end{bmatrix} + \begin{bmatrix} -\frac{\omega_{ek} \lambda_m}{L_q} \\ 0 \\ \frac{-3\omega_{ek} \lambda_m k_{3\lambda} cos(3\theta_{ek})}{L_0} \end{bmatrix} \tag{3.26}$$

The discretized equations allow to solve for the machine currents at the sample time $k+1$ knowing the qd0 currents, qd0 voltages, machine speed and rotor position at the time instant k.

3.5 Extension of the PMSM Mathematical Model to the OEW Configuration

It can be observed that for a PMSM with the stator windings connected in star configuration the sum of the phase currents is zero as shown in (3.27)

$$i_a + i_b + i_c = 0 \tag{3.27}$$

In the case where the machine is operated in star configuration only two phase currents are necessary to describe the machine behaviour, therefore the third row of (3.26) can be neglected. If the PMSM is operated in OEW configuration then all the three phase currents are necessary to describe the dynamic and steady state performance of the machine, i.e. the order of the system increases from two to three, as shown in (3.26).

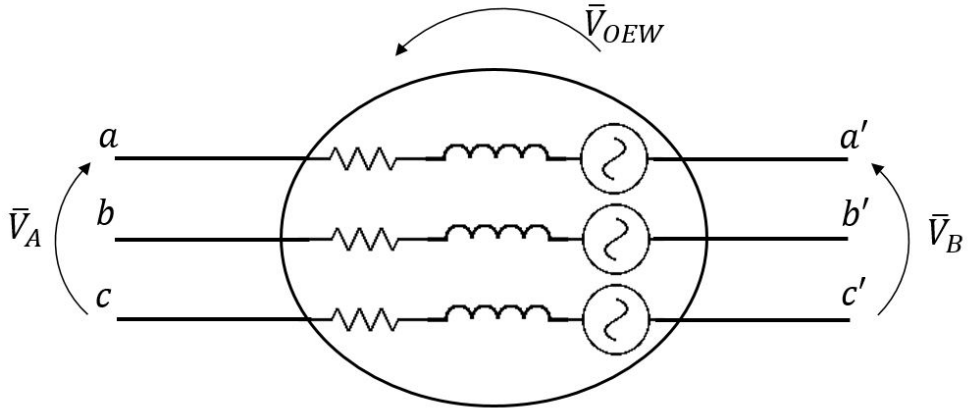


Figure 3.4: OEW-PMSM Voltages

The model for the 6-terminals PMSM can be obtained from the star connected one, a change of name variables is made for sake of clarity. By looking at Fig. 3.4 the phase voltages V_{abc} are renamed V_{OEW}. From Fig. 3.4 the vector $\overline{V}_{OEW}$ can be expressed

as

$$\overline{V}_{OEW} = \overline{V}_A - \overline{V}_B = \begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} - \begin{bmatrix} V_{a'o} \\ V_{b'o} \\ V_{c'o} \end{bmatrix} = \begin{bmatrix} V_{aa'} \\ V_{bb'} \\ V_{cc'} \end{bmatrix} \tag{3.28}$$

where the hypothesis that the same potential reference is used for both voltages $\overline{V}_A$ and $\overline{V}_B$. Applying Clark transform the ZSC and ZSV can be calculated as (3.29) and (3.30) respectively

$$i_0 = \frac{i_a + i_b + i_c}{3} \tag{3.29}$$

$$V_0 = \frac{V_{aa'} + V_{bb'} + V_{cc'}}{3} \tag{3.30}$$

Transforming (3.28) on the synchronous reference frame qd0 the following equation is obtained

$$\overline{V}_{OEW}^{qd0} = \mathbf{T}_P(\vartheta_e)\overline{V}_{OEW} = \mathbf{T}_P(\vartheta_e)\overline{V}_A - \mathbf{T}_P(\vartheta_e)\overline{V}_B = \overline{V}_A^{qd0} - \overline{V}_B^{qd0} \tag{3.31}$$

From (3.31) it can be noticed that as in the abc reference frame the motor phase voltages were the difference between the voltages $\overline{V}_A$ and $\overline{V}_B$ supplied by the two VSCs, in the qd0 reference frame each q-, d- or 0- axis voltage applied to the machine can be seen as the difference of the q-, d- or 0- axis voltage produced by converter A minus the q-, d- or 0- axis voltage supplied by converter B. The OEW-PMSM equations in the abc reference frame are

$$\begin{cases} V_{OEW} = RI_{abc} + \frac{d}{dt}\lambda_{abc} \\ \lambda_{abc} = L_{abc}I_{abc} + \Lambda_r \\ i_a + i_b + i_c = 3i_0 \end{cases} \tag{3.32}$$

where the meaning of each vector and matrix has been previously presented. The machine equations in the qd0 synchronous reference frame correspond to the system composed by (3.21) and (3.29).

3.6 PMSM Torque Equation

The following relationship exists between the electrical power produced by the machine and the one transferred to the shaft:

$$T_e = \frac{1}{\omega_m}(e_a i_a + e_b i_b + e_c i_c) \tag{3.33}$$

where ω_m is the mechanical speed of the machine and e_a, e_b, e_c are the phase back-EMFs. (3.33) can be rewritten in a matrix form as

$$T_e = \frac{1}{\omega_m} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}^T \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.34}$$

applying the Park transform the torque equation in the qd0 reference frame is obtained

$$T_e = \frac{1}{\omega_m} \begin{bmatrix} e_q \\ e_d \\ e_0 \end{bmatrix}^T \mathbf{T}_P^{-1}(\vartheta_e)^T \mathbf{T}_P^{-1}(\vartheta_e) \begin{bmatrix} i_q \\ i_d \\ i_0 \end{bmatrix} = \frac{1}{\omega_m} \begin{bmatrix} e_q \\ e_d \\ e_0 \end{bmatrix}^T \begin{bmatrix} 3/2 & 0 & 0 \\ 0 & 3/2 & 0 \\ 0 & 0 & 3 \end{bmatrix} \begin{bmatrix} i_q \\ i_d \\ i_0 \end{bmatrix} \tag{3.35}$$

which can be rewritten as

$$T_e = \frac{3}{2\omega_m}(e_q i_q + e_d i_d + 2e_0 i_0) \tag{3.36}$$

The qd0 back-EMF is know from (3.21) and it is reported in (3.37)

$$\begin{cases} e_q = \omega_e L_d i_d + \omega_e \lambda_m \\ e_d = -\omega_e L_q i_q \\ e_0 = 3\omega_e \lambda_m k_{3\lambda} cos(3\theta_e) \end{cases} \tag{3.37}$$

substituting (3.37) into (3.35) the final expression for the torque equation is found

$$T_e = \frac{3}{2} p \Big[\lambda_m i_q + (L_d - L_q) i_d i_q + 6\lambda_m k_{3\lambda} cos(3\theta_e) \Big] \tag{3.38}$$

We can identify two terms from (3.38): the first one is the torque produced by the d-axis and q-axis currents while the second one is the torque produced by the ZSC i_0. It can be noticed that the torque due to i_0 is a fluctuating component with six times the frequency of the fundamental. This is an unwanted torque which would not transfer any mechanical power but would lead only to speed fluctuations. Therefore, it is a key factor for OEW-PMSM applications with common dc bus to suppress the torque ripple. For the sake of completeness, the speed differential equation is reported

$$\begin{cases} T_e - T_l = J\frac{d\omega_e}{dt} + B\omega_e + Dsign(\omega_e) \\ \vartheta_e(t) = \int_{t_0}^{t} \omega_e(\tau)d\tau + \vartheta_e(0) \end{cases} \tag{3.39}$$

where T_l is the load torque, B is the viscous friction and D is the static friction depending on the speed sign, which is 1 if the speed is positive, -1 if negative or 0 otherwise.

3.7 ZSC Flow due to Non-Sinusoidal Machine back-EMF

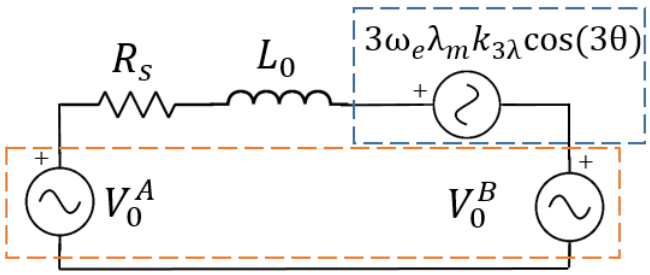


Figure 3.5: Zero-Sequence Equivalent Circuit. Orange box: ZSV due to the power converter. Blue box: ZSV of the machine non-sinusoidal back-EMF.

Fig. 3.5 shows the equivalent circuit for the zero-sequence axis where the ZSV produced by the dual inverter has been split in the two terms V_0^A and V_0^B. It can be noted that even if the ZSV produced by the converter would be zero, if the OEW-PMSM has a third harmonic component the ZSC flowing would still be different from zero. The ZSC due to the third harmonic component of the machine can be calculated from the zero-sequence equivalent circuit and it corresponds to the solution of a first order differential equation with sinusoidal input voltage as shown in (3.40)

$$\begin{cases} 3\omega_e\lambda_m k_{3\lambda} cos(3\omega_e t) = L_0\frac{di_0(t)}{dt} + R_s i_0(t) \\ i_0(0) = 0 \end{cases} \tag{3.40}$$

which leads to the solution (3.41)

$$i_0(t) = \frac{3\omega_e\lambda_m k_{3\lambda}}{L_0\sqrt{(\frac{R_s}{L_0})^2 + (3\omega_e)^2}}\Big[cos(\phi)e^{\frac{-R_s t}{L_0}} + cos(3\omega_e t - \phi)\Big] \tag{3.41}$$

where

$$\phi = tg^{-1}\Big(\frac{3\omega_e L_0}{R_s}\Big) \tag{3.42}$$

Since the torque ripple introduced by the ZSC is unwanted it is necessary to eliminate it. In the literature there are works that aim to eliminate the ZSC due to the non-sinusoidal machine back-EMF. In [19] a simple PI controller is used to synthesize the ZSV necessary to eliminate the one produced by the machine's back-EMF. The ZSV is synthesized thanks to the method of the ZVR. In [5, 136] the ZSC is eliminated thanks to a Proportional Resonant (PR) Controller and the ZSV is still synthesized thanks to the ZVR method. The technique used to eliminate the ZSC used in [82] is instead based on the injection of an additional q-axis current component. The additional oscillating reference current can be determined from the torque equation (3.38) which is injected into the current reference in the q-axis. This method utilizes the extra torque generated by the injected current to counteract the part of torque fluctuation due to i_0. A Proportional Integral Resonant (PIR) Controller is used to track the desired oscillating reference.

3.8 PMSM Parameters

The parameters of the high speed starter-generator under test are listed in Table 3.1.

Table 3.1: High-Speed Starter-Generator OEW-PMSM parameters.

L_q	403 [μH]	L_d	403 [μH]
R_s	1.44 [$m\Omega$]	p	3 [-]
λ_m	0.086532 [V s]	$k_{3\lambda}$	0.01891367 [-]

The high-speed machine was initially not available, therefore another OEW machine had to be used. In order to test and verify the proposed control and modulation the tests have been initially carried out on a scaled-down OEW-PMSM and later on the high-speed starter-generator. A conventional 18 slot - 6 poles surface mounted PMSM, that was available within the facilities of the Power Electronic Machine and Control (PEMC) group of the University of Nottingham, has been adopted as test machine. The machine parameters are presented in Table 3.2 while additional details of the considered machine are listed in Table 3.3.

Table 3.2: Scaled-down OEW-PMSM under test parameters

L_q	1.35 [mH]	L_d	1.35 [mH]
R_s	0.8434 [Ω]	p	3 [-]
λ_m	0.087789 [V s]	$k_{3\lambda}$	0.0017904235 [$-$]

Table 3.3: Machine parameters

Parameter	**Value**
Pole number ($2p$)	6
PM material	NdFeB
PM remanence flux density B_{res}	1.24 T
PM relative permeability μ_r	1.031
Power rating	1.5 kW
Peak value of the current (I_{rated})	13 A
Rated Speed (ω_{rated})	3000 rpm
Turn/coil (N_s)	22
PM flux (λ_m)	0.0852 Wb
Outer Stator diameter	95 mm
Inner Stator diameter	49.5 mm
Axial length (l)	90 mm
Airgap length (g_0)	1 mm
Magnets thickness (h_m)	4 mm

3.9 Chapter Summary

The first part of this Chapter provides a detailed description of the electrical model of the machine considered. The phase voltages model and its equivalent electrical circuit has been presented. In particular, the $d-q$ axis voltage equations have been determined and expressed in state space form. The equivalent electrical circuit in the qd0 reference frame has been proposed and the extension of the PMSM equations to the OEW configuration has been discussed. Finally, the parameters of the machine used to validate the control algorithm proposed in simulation and experimental have been presented.

Chapter 4

ZSV Elimination SVM for the Mixed Technology Dual-Inverter

4.1 Introduction

This Chapter deals with the design of the reference duty cycles for the OEW-PMSM fed by the mixed technology dual-inverter. The objective is to exploit the different nature of the IGBT power modules and the SiC-based switching devices. Firstly the motivations behind the use of different technologies for the two two-level VSCs is given, then the technique adopted to split the reference voltages coming out of the current loop is presented. The IGBT VSC is required to switch in square-wave mode to reduce at the minimum the switching losses. The output voltages for the square-wave converter are presented and the ZSV expression over an electrical period is given. According to the constraint added for the IGBT-based VSC to switch in square-wave mode the reference signals for the SiC-based VSC are determined. Furthermore the criteria behind the selection of the space voltage vectors for the synthesis of the reference voltage vector is discussed. The three active vectors modulation is presented

and its voltage limits in the $\alpha\beta$ plane are evaluated. The expressions to calculate the dwelling time for the active vectors are obtained and the overall logic of reference voltages generation is discussed.

4.2 Reference Voltages Generation for the Dual-Fed OEW-PMSM

As demonstrated in [11, 12] the mixed technology IGBT-SiC dual-inverter is the one that achieves better phase current THD and lower converter losses among the different power electronics topologies that can be adopted to feed the OEW-PMSM starter-generator. The higher system efficiency is obtained by exploiting the different nature of the two VSCs switching devices. First there is a potential massive losses reduction when SiC-based power modules are used in place of conventional IGBT power modules, when operating the SiC devices at the same frequency of the IGBTs. The main benefit of SiC-based power modules are the lower switching losses, therefore SiC technology is effectively advantageous when the reduction in the conduction losses is not associated with higher switching losses due to a higher switching frequency. The mixed technology structure has also the flexibility to operate at different switching frequencies to increase the efficiency of the configuration. Therefore, the modulation strategy for the two VSCs has to be selected to operate the two converters at different switching frequencies and to exploit the different nature of the two technologies used, IGBT and SiC devices. Furthermore the selected duty cycles have to be synthesized in order to have instantaneously zero V_0 .

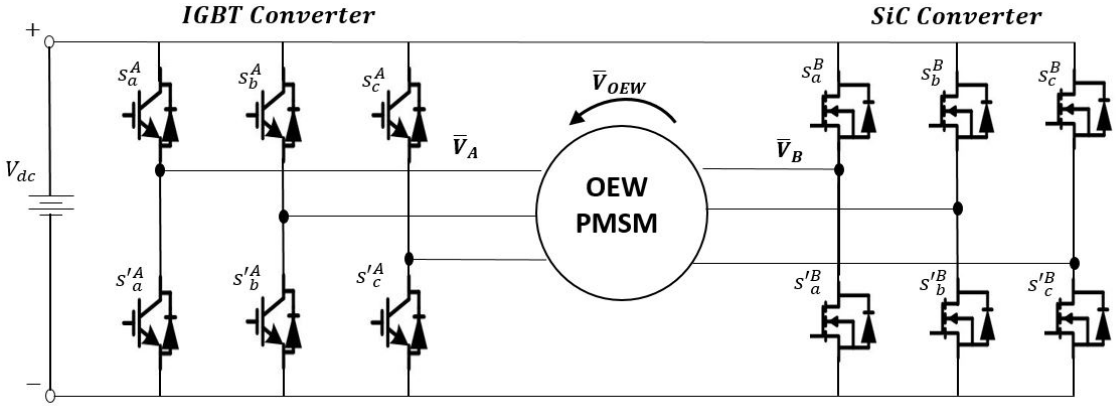


Figure 4.1: Dual-Fed common dc-link mixed technology OEW-PMSM.

Let's suppose to have the three machine abc reference voltages $\overline{V}^*_{OEW}$ coming out of the current loop controller as described in Chapter 6, these signals have to be split among the two VSCs. As already pointed out in previous works [83, 84] a common approach is to equally split the reference voltage among the two two-level VSCs and having them switching at the same frequency. Given the different nature of the power modules used for the two VSCs this standard solution is not the optimal one since it would force the SiC devices to switch at much lower frequency then they actually could. The degree of freedom given by the possibility to split the $\overline{V}^*_{OEW}$ phase voltage references among the two converters is used to allow the IGBT converter to switch at the lowest possible switching frequency. From Fig. 4.1 the phase voltages of the OEW-PMSM can be expressed as the difference between the VSC A voltages $\overline{V}_A$ and the B one $\overline{V}_B$ (3.28). The same relationship is used to generate the reference voltages for the two VSCs as shown in (4.1)

$$\overline{V}^*_{OEW} = \overline{V}^*_A - \overline{V}^*_B \tag{4.1}$$

Where $\overline{V}^*_{OEW}$ are the OEW-PMSM reference phase voltages, $\overline{V}^*_A$ and $\overline{V}^*_B$ are respectively the reference phase voltages of the A and B VSCs. Since the $\overline{V}^*_{OEW}$ are known

and they are obtained from the current loop as explained in Chapter 6 they can be used to determine the reference voltages for the VSC A as follows

$$\overline{V}_A^{*SW} = \frac{V_{dc}}{2} sign(\overline{V}_{OEW}^*) \tag{4.2}$$

where

$$sign(a) = \begin{cases} 1 & \text{if } a > 0 \\ -1 & \text{if } a < 0 \\ 0 & \text{if } a = 0 \end{cases}$$

$\overline{V}_A^{*SW}$ are the square wave reference signals for the VSC A which is going to be the one using the IGBT power modules. (4.2) shows that the VSC A reference voltages consist in three square-wave voltages of amplitude $\frac{V_{dc}}{2}$ with the same phase displacement of the OEW-PMSM reference voltage signals. The reference signals for the VSC B are obtained from (4.1) substituting $\overline{V}_A^{*SW}$ to $\overline{V}_A^*$

$$\overline{V}_B^* = \overline{V}_A^{*SW} - \overline{V}_{OEW}^* \tag{4.3}$$

In fact having selected $\overline{V}_A^*$, $\overline{V}_B^*$ are uniquely defined by (4.1). The reference voltages are split for the two VSCs as described in (4.1)-(4.3) and consist of a square wave control of the IGBT converter allowing it to switch at the fundamental frequency set by the motor speed. Fig. 4.2 shows the $\overline{V}_{OEW}^*, \overline{V}_A^{*SW}$ and $\overline{V}_B^*$ normalised voltage references profiles over an electrical period.

The six-step modulation of VSC A introduces elevated harmonic distortion, therefore VSC B needs to switch at higher frequency in order to compensate for it. The slow

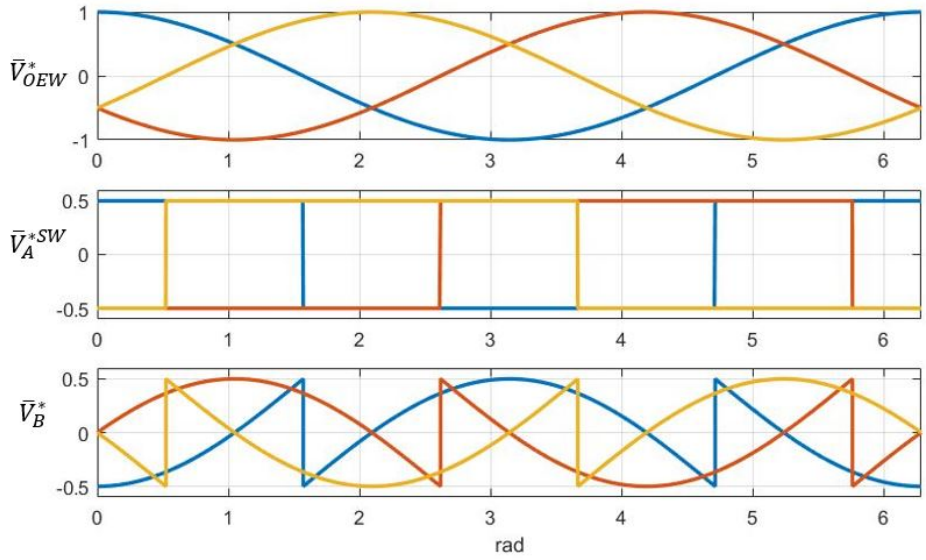


Figure 4.2: Normalised Reference Voltages for the Dual-Fed OEW-PMSM Drive. Top: $\overline{V}^*_{OEW}$ reference voltages. Middle: Square Wave reference voltages for VSC A. Bottom: Reference voltages for the VSC B.

switching VSC A can be realised with IGBT devices while VSC B with SiC power modules. As it will be shown later the role of the SiC converter in this configuration can be interpreted as an active filter that eliminates the harmonic distortion introduced by the low switching IGBT one simultaneously providing the high switching frequency necessary to synthesize the fundamental of the machine. Considering the different switching frequencies of the two converters the IGBT is mainly responsible for the conduction losses while the SiC is responsible for the switching losses. E.g. for the starter-generator considered in this work, supposing a rotating speed of 20 krpm, the IGBT converter switching frequency would be the same of the fundamental frequency of the machine resulting in 1 kHz. If we consider the OEW-PMSM of which described in Chapter 3 Section 3.8, given 3 pole pairs and supposing a rotating speed of 3000 rpm the IGBT converter switching frequency would be 150 Hz.

4.3 Square Wave Modulation for the IGBT VSC

Observing Fig. 4.2 it can be noted that modulating a VSC in square wave mode means applying consequently the 6 active space voltage vectors of Table 2.1. Considering a counter-clockwise sense of rotation of the reference voltage vector which lays initially on the α axis the active vectors are applied in the sequence $'100',' 110',' 010',' 011',' 001'$ and $'101'$ for 60° each. In particular the vector $'100'$ is applied for $\vartheta_e \in [-\frac{\pi}{6}, \frac{\pi}{6}]$, $'110'$ is applied for $\vartheta_e \in [\frac{\pi}{6}, \frac{2\pi}{3}]$ and so on for the other active vectors. The phase voltages of VSC A under square wave modulation can be written as a Fourier series expansion as

$$\begin{cases} V_{ao} = \frac{2V_{dc}}{\pi} \sum_n^{\infty} \frac{1}{n} sin(\frac{2\pi n}{T_0}) \\ V_{bo} = \frac{2V_{dc}}{\pi} \sum_n^{\infty} \frac{1}{n} sin(\frac{2\pi n}{T_0} + \frac{2\pi}{3}) \\ V_{co} = \frac{2V_{dc}}{\pi} \sum_n^{\infty} \frac{1}{n} sin(\frac{2\pi n}{T_0} - \frac{2\pi}{3}) \end{cases} \tag{4.4}$$

where n is the harmonic order and it assumes only the odd integer values and T_0 is the phase voltage square wave period. The square wave modulation allows to apply the highest possible voltage on the fundamental but on the other hand it introduces all the odd harmonics. VSC B will be responsible for cancelling the distortion introduced by the square wave modulated converter.

Table 4.1: Standard 2-level VSC Voltage Vectors, gate signals and phase voltages

Voltage Vector	Gate Signals	V_{ao}	V_{bo}	V_{co}
V_0	[0 0 0]	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
V_1	[1 0 0]	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
V_2	[1 1 0]	$V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$
V_3	[0 1 0]	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$
V_4	[0 1 1]	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
V_5	[0 0 1]	$-V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$
V_6	[1 0 1]	$\frac{V_{dc}}{2}$	$-V_{dc}/2$	$V_{dc}/2$
V_7	[1 1 1]	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

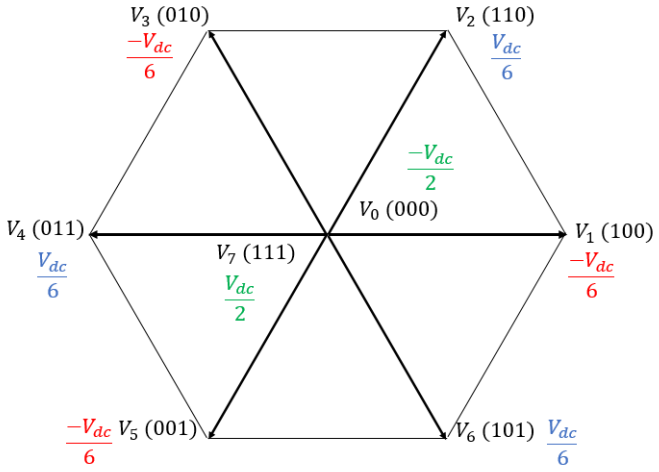


Figure 4.3: ZSV for the Voltage Space Vectors of the Standard VSC.

Referring to Table 4.1 and to Fig. 4.3 the ZSV profile produced by VSC A when square wave modulated can be derived. Moving on the active vectors means having a ZSV that alternatively assumes the values $-\frac{V_{dc}}{6}$ and $\frac{V_{dc}}{6}$. In order to have zero V_0^{OEW} applied on the machine the ZSVs produced by the two VSCs V_0^A and V_0^B must be instantaneously the same. An efficient solution to achieve zero V_0^{OEW} is to define the ZSV produced by one of the two VSCs as a function of the converter reference voltage angle. I.e. if the VSC A is modulated in six-step mode its ZSV V_0^A has a well known profile which can be expressed as

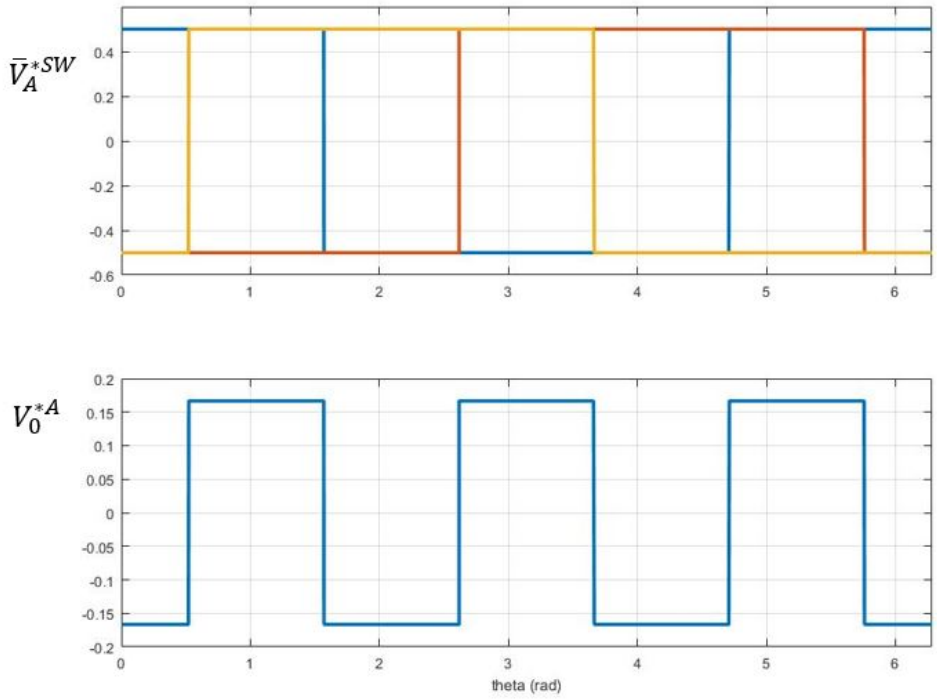


Figure 4.4: ZSV for the single three phase VSCdrive when modulated in six-step. Top: Normalised phase voltages of the square wave modulated VSC. Bottom: normalised ZSV V_0^A.

$$V_0^A = \begin{cases} -\frac{V_{dc}}{6} & \text{if } \vartheta_e \in [\frac{11\pi}{6}, \frac{\pi}{6}] \cup [\frac{\pi}{2}, \frac{5\pi}{6}] \cup [\frac{7\pi}{6}, \frac{3\pi}{2}] \\ \frac{V_{dc}}{6} & \text{if } \vartheta_e \in [\frac{\pi}{6}, \frac{\pi}{2}] \cup [\frac{5\pi}{6}, \frac{7\pi}{6}] \cup [\frac{3\pi}{2}, \frac{11\pi}{6}] \end{cases}$$

Fig. 4.4 shows the phase references voltages for the VSC A and the associated ZSV produced by the converter. From now on when using the terminology ODD and EVEN voltage space vectors we will refer to the groups $'100', '010', '001'$ and $'110', '011', '101'$ respectively. When the ODD vectors $'100', '010'$ and $'001'$ are applied the ZSV is negative while when the EVEN vectors are applied the ZSV is positive. The ZSV produced by the VSC A changes polarity every 60 electrical degrees when the change of active vector happens. Fig. 4.5 shows in blue the voltage limits of a two-level VSC and in red the fundamental voltage of the the square wave reference voltage

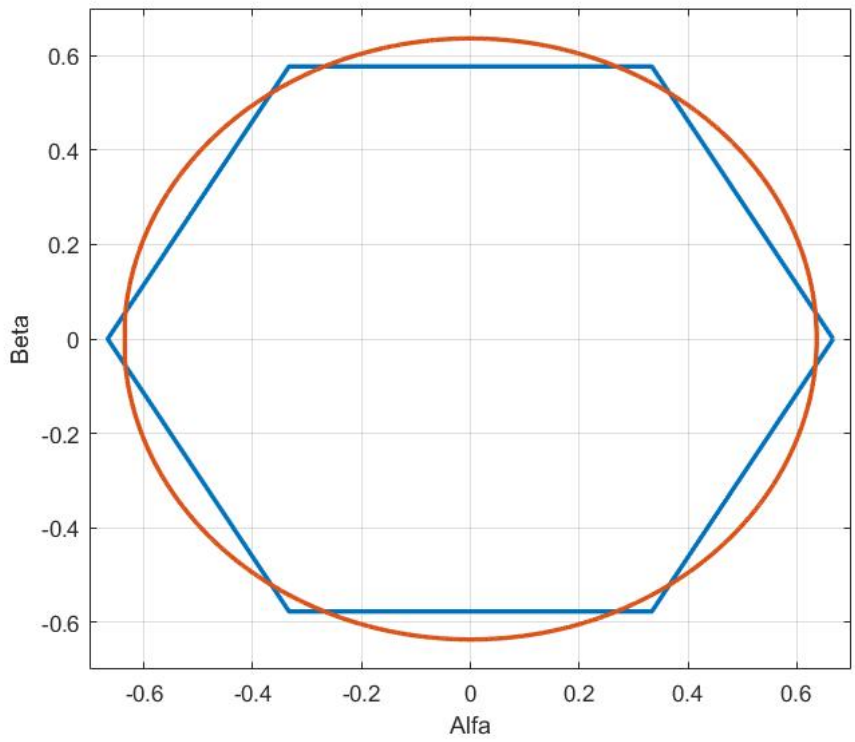


Figure 4.5: Voltage limits of the two-level VSC (blue). Trajectory of the fundamental voltage of the square wave reference vector $\overline{V}_A^{*SW}$ (red)

vector $\overline{V}_A^{*SW}$. The trajectory associated with the square wave modulated VSC is discontinuous and exclusively composed by the six vertices of the blue hexagon of Fig. 4.4.

4.4 Three Active Vectors SVM for the SiC VSC

The reference phase voltages for VSC B are calculated with (4.3) having set the VSC A to modulate in square wave. It is straightforward to notice that with the reference voltage split adopted the harmonic distortion introduced by the square-wave modulated converter is automatically cancelled by the other converter. Observing

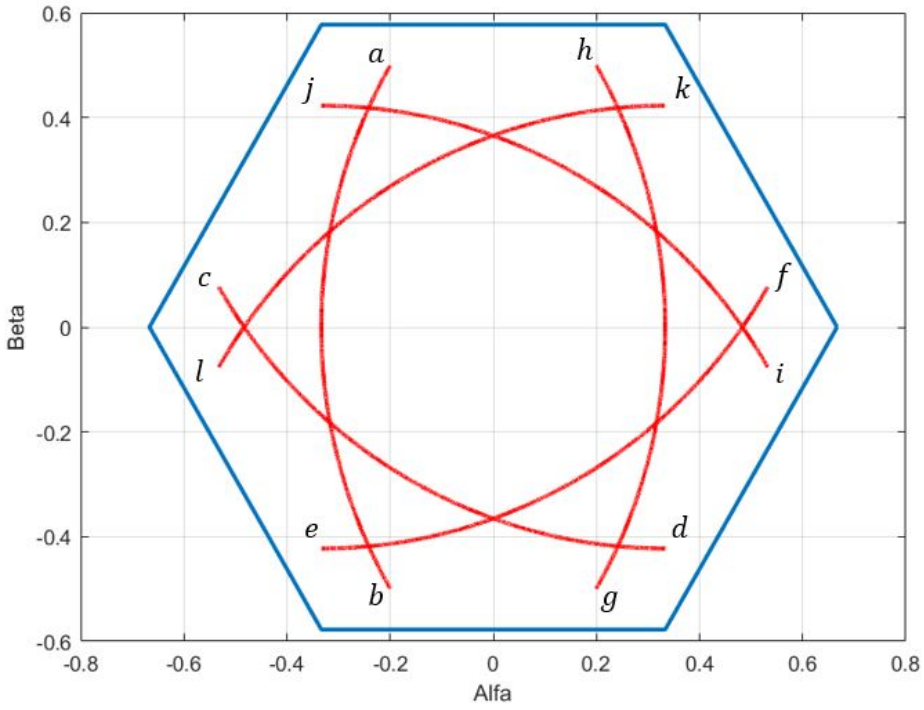


Figure 4.6: Trajectory of the space voltage reference vector $\overline{V}_B^*$ (red). Standard two-levels VSC modulation limits (blue)

(4.3) the voltage reference vector for VSC B carries the same harmonic content of the square-wave modulate VSC except for the machine reference voltages $\overline{V}_{OEW}^*$. In this simple way a feed-forward cancellation of the harmonic distortion introduced by VSC A is accomplished. In fact it would be much more complex eliminating all the square-wave harmonics by using multiple resonant filters on the VSC B. By looking at Fig. 4.2 it can be noticed that in the time domain there are discontinuities in the abc reference voltages $\overline{V}_B^*$ which are evident also in the $\alpha\beta$ plane trajectory of Fig. 4.6. The trajectory can be reconstructed by following in alphabetical order the letters that are at the extremes of the arcs described by the reference vector $\overline{V}_B^*$. The analytical expression of $\overline{V}_B^*$ in the $\alpha\beta$ reference frame can be easily found applying the Clark transform to (4.3).

$$\overline{V}^*_{B\alpha\beta} = \begin{cases} \overline{V}_1 - \overline{V}^*_{OEW\alpha\beta} & \text{if } \vartheta_e \in [\frac{11\pi}{6}, \frac{\pi}{6}] \\ \overline{V}_2 - \overline{V}^*_{OEW\alpha\beta} & \text{if } \vartheta_e \in [\frac{\pi}{6}, \frac{\pi}{2}] \\ \overline{V}_3 - \overline{V}^*_{OEW\alpha\beta} & \text{if } \vartheta_e \in [\frac{\pi}{2}, \frac{5\pi}{6}] \\ \overline{V}_4 - \overline{V}^*_{OEW\alpha\beta} & \text{if } \vartheta_e \in [\frac{5\pi}{6}, \frac{7\pi}{6}] \\ \overline{V}_5 - \overline{V}^*_{OEW\alpha\beta} & \text{if } \vartheta_e \in [\frac{7\pi}{6}, \frac{3\pi}{2}] \\ \overline{V}_6 - \overline{V}^*_{OEW\alpha\beta} & \text{if } \vartheta_e \in [\frac{3\pi}{2}, \frac{11\pi}{6}] \end{cases}$$

(4.4) shows the expression of the reference voltages for the VSC B in the $\alpha\beta$ plane over an electrical period. Once the trajectory has been defined the vectors to select to synthesize it need to be chosen. The decision of which vectors to be used among the 8 space voltage vectors available for a standard VSC needs to be done by taking into consideration the VSC A modulation in order to ensure to have instantaneously $V_0^A - V_0^B$ equal to zero. A SVM modulation that allows to satisfy at each sample time the conditions set by (4.3) and V_0^{OEW} equal to zero needs to be developed. The ZSV profile produced by the VSC A is known over the whole electrical period as shown in Fig. 4.4 and described by (4.3). The space voltage vectors used by the square-wave modulated converter are exclusively the active vectors $\overline{V}_1, \overline{V}_2, \overline{V}_3, \overline{V}_4, \overline{V}_5$ and $\overline{V}_6$. Therefore also VSC B can apply only the active vectors $\overline{V'}_1, \overline{V'}_2, \overline{V'}_3, \overline{V'}_4, \overline{V'}_5$ and $\overline{V'}_6$ in order to have $V_0^A - V_0^B$ equal to zero. When referring to the voltage vectors applied by VSC A and B we will indicate them with $\overline{V}_j$ and $\overline{V'}_j$ respectively.

When the VSC A is applying one the three ODD vectors $\overline{V}_1, \overline{V}_3, \overline{V}_5$ the VSC B can use at maximum three vectors among $\overline{V'}_1, \overline{V'}_3, \overline{V'}_5$ to synthesize the reference vector $\overline{V}^*_B$. Similarly when one of the three EVEN vectors $\overline{V}_2, \overline{V}_4, \overline{V}_6$ is applied by the VSC A, VSC B can use only the active vectors $\overline{V'}_2, \overline{V'}_4, \overline{V'}_6$ in order to keep the ZSV applied on the machine equal to zero. Firstly the possibility to use only two of the three active vectors available is considered. Any of the two groups of ODD or EVEN vectors can be considered, here the ODD vectors are selected. If the reference vector $\overline{V}^*_B$ falls in the light blue area of Fig. 4.7 the vectors $\overline{V'}_1$ and $\overline{V'}_2$ are used to

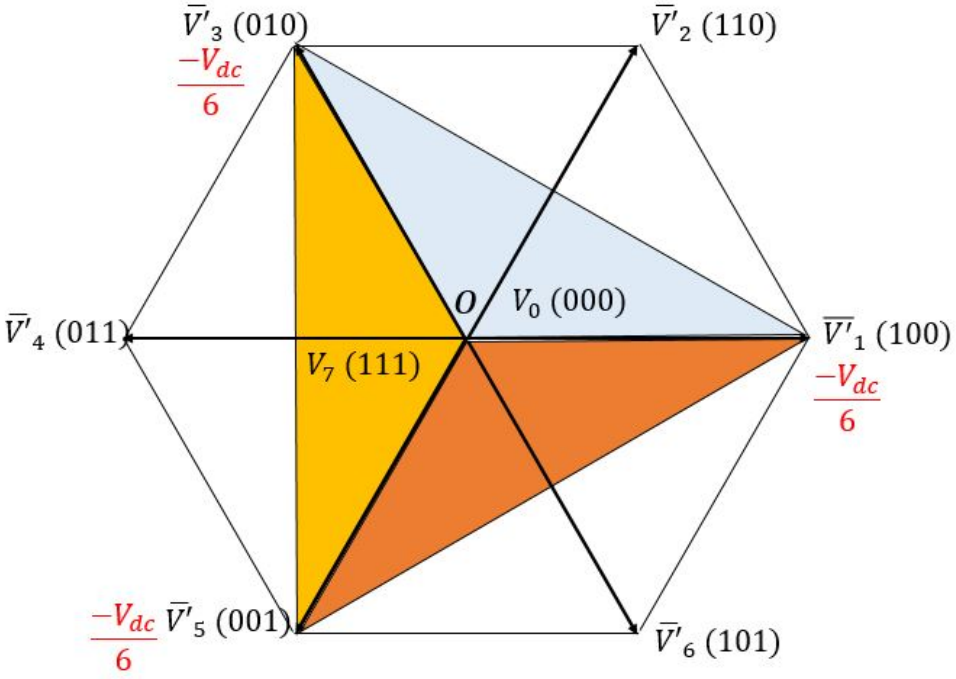


Figure 4.7: 2 Vectors SVM for the VSC B where the ODD Vectors are considered.

synthesize it. The following system needs to be solved to find the dwelling times of the two active vectors.

$$\begin{cases} T_s\overline{V}^*_B = t_1\overline{V'}_1 + t_3\overline{V'}_3 \\ T_s = t_1 + t_3 \end{cases} \tag{4.5}$$

t_x stands for the dwelling time of the x vector where x can assume the values from 0 to 7. T_s is the digital controller sample time. It can be noticed that two vectors are not sufficient to modulate the reference vector. In fact if $\overline{V}^*_B$ lays on the α axis with a module smaller than $\frac{2V_{dc}}{3}$ the vector $\overline{V'}_1$ needs to be applied for a fraction of T_s. During the time left $T_s - t_1$, according to the 2 active vector modulation chosen, the vector $\overline{V'}_3$ should be applied. It is easy to see that the reference vector cannot be synthesized since the vector $\overline{V'}_3$ contains also an imaginary component. Therefore all the three active vectors are necessary to synthesize any reference vector that falls

into the area delimited by the tips of the three vectors.

Fig. 4.8 (a) and (b) show graphically the limits of the three active vectors modulation on the $\alpha\beta$ plane for the ODD and EVEN vectors respectively. The black triangles of Fig. 4.8 (a) and (b) identify the locus of points that can be synthesized by using the three active vectors modulation. The red arcs, as previously described, are the trajectory described by $\overline{V}^*_B$. For both groups of ODD and EVEN vectors the locus of points described by $\overline{V}^*_B$ falls inside the black triangle, therefore by using the three active vectors modulation it is always possible to synthesize the desired reference vector. The two VSCs can be seen as two independent converters or as a single one, the voltage space vectors of the dual-inverter are shown in Fig. 4.9. The ODD and EVEN vectors for the VSC A are highlighted in red and blue respectively. The limits of the proposed modulation on the $\alpha\beta$ plane can be found in a simple graphical way as explained in the following lines. E.g. when the VSC A applies $\overline{V}_1$, VSC B can apply exclusively $\overline{V'}_1, \overline{V'}_3$ and $\overline{V'}_5$. The vectors $\overline{OO}, \overline{OH}$ and $\overline{OS}$ are obtained summing to $\overline{V}_1$ the vectors $\overline{V'}_1, \overline{V'}_3$ and $\overline{V'}_5$ respectively. The locus of points that can be synthesized is delimited by the dashed red triangle that contains $\overline{V}_1$. By constructing the remaining triangles for all the other vectors applied by the square-wave modulated VSC A the locus of points that can be synthesized with the proposed modulation is found. It can be noticed that it corresponds to the same region of points obtained when exclusively the vectors with zero ZSV are applied for the dual-inverter.

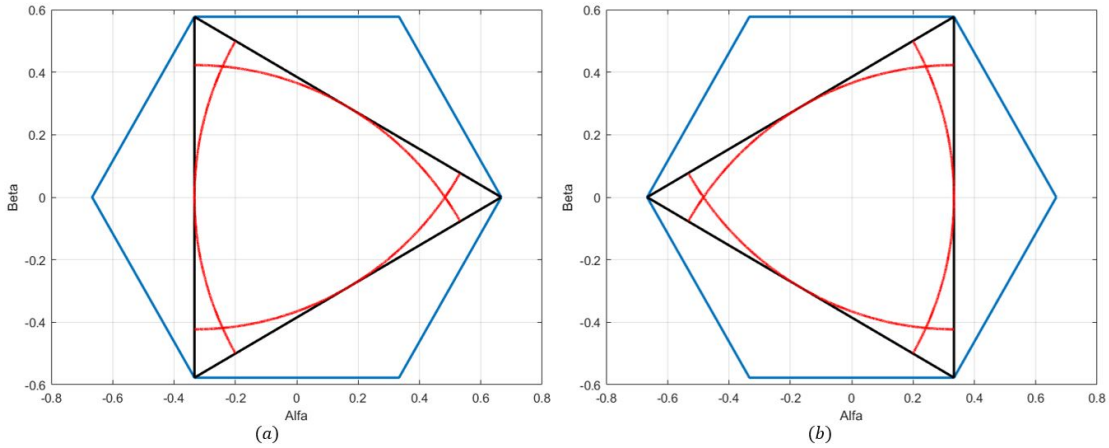


Figure 4.8: (a)Area delimited by the three ODD active vectors (black). Trajectory described by $\overline{V}_B^*$ when the ODD vectors are applied by VSC A (red). Voltage limits of the two-level VSC (blue). (b)Area delimited by the three EVEN active vectors (black). Trajectory described by $\overline{V}_B^*$ when the EVEN vectors are applied by VSC A (red). Voltage limits of the two-level VSC (blue).

As mentioned in Chapter 2 the three active vector modulation was already investigated for the standard two-level VSC in [94,97,98]. This modulation was investigated with the purpose of reducing the common-mode currents in PWM drives. Fluctuations in the ZSV generates ZSC that flows through parasitic capacitances, always existing between the stator windings and the motor case, usually grounded for safety reasons. The modulation achieves a reduction in the variation of the ZSV produced by the standard 3-phases two-level VSC. Here the modulation is adapted to be used for the dual-inverter with the reference voltages proposed in Section 4.2. The dwelling times for the three active vectors can be found similarly as done for a standard SVM. For the ODD set of vectors $\overline{V'}_1, \overline{V'}_3$ and $\overline{V'}_5$ the following system can be written

$$\begin{cases} T_s\overline{V}_B^* = t_1\overline{V'}_1 + t_3\overline{V'}_3 + t_5\overline{V'}_5 \\ T_s = t_1 + t_3 + t_5 \end{cases} \tag{4.6}$$

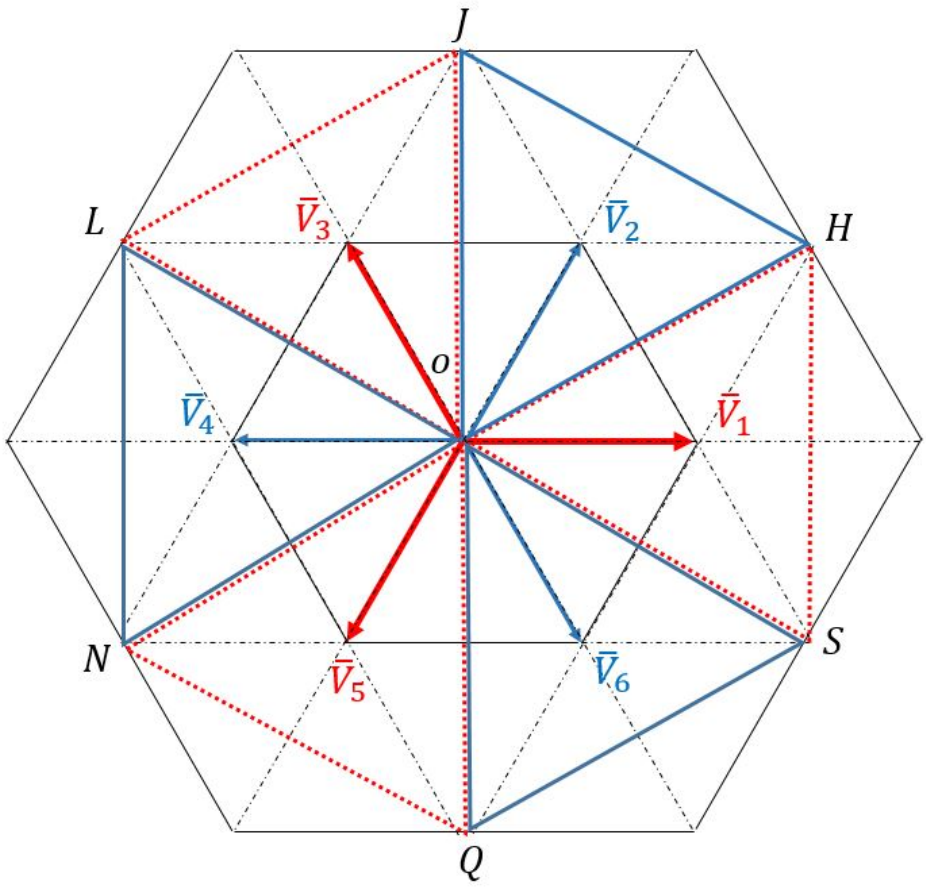


Figure 4.9: Voltage limits of the proposed three active vector SVM on the $\alpha\beta$ plane.

Similarly it can be done for the EVEN set of vectors $\overline{V'}_2, \overline{V'}_4$ and $\overline{V'}_6$

$$\begin{cases} T_s\overline{V}^*_B = t_2\overline{V'}_2 + t_4\overline{V'}_4 + t_6\overline{V'}_6 \\ T_s = t_2 + t_4 + t_6 \end{cases} \tag{4.7}$$

Both (4.6) and (4.7) can be split considering the Real and Imaginary part of the space voltage vectors. For the ODD vectors the following system of equations is obtained

$$\begin{cases} T_s Re(\overline{V}_B^*) = t_1 V - t_3 \dfrac{V}{2} - t_5 \dfrac{V}{2} \\ T_s Im(\overline{V}_B^*) = t_3 \dfrac{\sqrt{3}V}{2} - t_5 \dfrac{\sqrt{3}V}{2} \\ T_s = t_1 + t_3 + t_5 \end{cases} \tag{4.8}$$

For the EVEN set of vectors the following system is obtained instead

$$\begin{cases} T_s Re(\overline{V}_B^*) = t_2 \dfrac{V}{2} - t_4 V + t_5 \dfrac{V}{2} \\ T_s Im(\overline{V}_B^*) = t_2 \dfrac{\sqrt{3}V}{2} - t_6 \dfrac{\sqrt{3}V}{2} \\ T_s = t_2 + t_4 + t_6 \end{cases} \tag{4.9}$$

Where V is the module of the VSC's vectors in the $\alpha\beta$ plane corresponding to $\dfrac{2V_{dc}}{3}$. By solving the system of equations (4.8) and (4.9) for t_1, t_3, t_5 and t_2, t_4, t_6 respectively the dwelling times for the space voltage vectors of the VSC B can be found.

$$\begin{cases} t_1 = T_s \dfrac{3Re(\overline{V}_B^*) + V_{dc}}{2V_{dc}} \\ t_3 = T_s \dfrac{V - Re(\overline{V}_B^*) + \sqrt{3}Im(\overline{V}_B^*)}{2V_{dc}} \\ t_5 = T_s \dfrac{V - Re(\overline{V}_B^*) - \sqrt{3}Im(\overline{V}_B^*)}{2V_{dc}} \end{cases} \tag{4.10}$$

$$\begin{cases} t_2 = T_s \dfrac{V + Re(\overline{V}_B^*) + \sqrt{3}Im(\overline{V}_B^*)}{2V_{dc}} \\ t_4 = T_s \dfrac{V - 2Re(\overline{V}_B^*)}{2V_{dc}} \\ t_6 = T_s \dfrac{V + Re(\overline{V}_B^*) - \sqrt{3}Im(\overline{V}_B^*)}{2V_{dc}} \end{cases} \tag{4.11}$$

At each controller sample time either (4.10) or (4.11) are used to calculate the dwelling times of the three active vectors used to synthesize the reference vector $\overline{V}_B^*$.

4.5 Reference Voltage Split Logic For the Dual-Inverter Mixed Technology Drive

Fig. 4.10 shows the block diagram that explains the square-wave modulation introduced for the instantaneous ZSV elimination for the mixed technology dual two -level converter. Firstly (4.2) and (4.3) are used to calculate the reference voltage vectors for the VSC A and B. Secondly it is checked if the actual vector applied by the VSC A belongs to the ODD or EVEN set. With this information and the knowledge of the reference voltage vector for VSC B either (4.10) or (4.11) is used to determine the dwelling times for the three active vectors. It can be noticed that for both verses of rotation the square-wave modulated converter applies alternatively an ODD and EVEN vector, therefore also VSC B will alternatively apply the thee ODD or EVEN vectors calculated with (4.10) and (4.11) respectively.

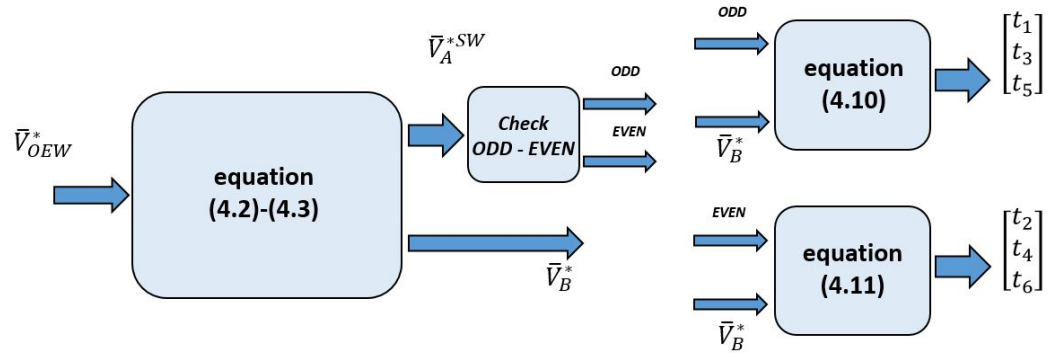


Figure 4.10: Block diagram of the reference voltage split logic for the dual-inverter mixed technology drive.

4.6 Conclusions

In this Chapter the modulation strategy used in this work for the mixed technology dual-fed common dc-link OEW-PMSM for instantaneous ZSV elimination has been presented. Firstly the strategy for the generation of the voltage references for the two two-level converters has been discussed. Then the square wave modulation for the VSC A has been presented, the harmonic content of the well know square-wave waveform has been discussed in relationship with the harmonic content of the voltages generated by VSC B. Furthermore the reference signals for VSC B are obtained. The set of space voltage vectors to select to synthesise the reference voltages in order to have instantaneous elimination of the ZSV are studied. Finally the three active vectors SVM is presented, as well as the equation for the calculation of the dwelling times.

Chapter 5

Dead-Time Hysteresis Control of the ZSC

5.1 Introduction

This Chapter presents the analysis of the effect of the power electronics non-linearities and non-sinusoidal machine back-EMF on the motor drive. In particular, attention of these effects on the zero-sequence equivalent circuit has been given in order to model and understand the effects on the drive performance. A general introduction to the VSC's non-linearities is given followed by an in depth analysis of the voltage distortion introduced by the DT on the zero-sequence equivalent circuit for both the standard two-level VSC and the dual-inverter topology. The PBDTC algorithm as a DT compensation method is presented and its logic of implementation and advantages are shown. Furthermore, it is presented how the PBDCT method can be applied in conjunction with the modulation proposed for the instantaneous ZSV elimination. Since the ZSV cannot be applied on the machine terminals due to the extremely low leakage inductance a ZSC controller which exploits the ZSV distortion introduced

by the DT has been proposed. The DT is always considered as an undesired effect on which there is no possibility to achieve any control. Thanks to the modulation proposed and the PBDTC the DT can be identified and it can be decided if to compensate it or not. In this way a variable band hysteresis controller for the ZSC has been obtained and it is presented in the following sections.

5.2 Power Converter's non-linearities Influence on the Dual-Inverter Drive

The modulation proposed in Chapter 4 achieves simultaneously the synthesis of the VSCs reference voltages and the instantaneous elimination of the ZSV produced by the dual-inverter. The other sources of ZSV are the VSCs' non-linearities and the non-sinusoidal machine's back EMF. In the ideal case the modulation developed in Chapter 4 would be enough to eliminate any cause for additional flow of ZSV. Fig. 5.1 helps to identify the causes of circulation of ZSC. If the modulation proposed in this work is implemented the terms V_0^A and V_0^B are instantaneously the same, therefore except for the VSCs' non-linearities the ZSV sources from the converter side are compensated. In the following sections the analysis of the DT effect on the ZSV produced by the individual VSCs will be carried out as well as the influence of the voltage non-linearities on the ZSV produced by the dual-converter and its effect on the ZSC flow.

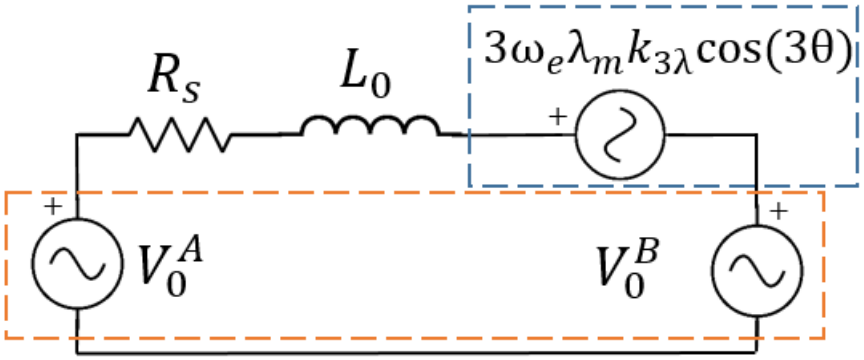


Figure 5.1: Zero-Sequence Equivalent Circuit. Orange box: ZSV due to the power converter. Blue box: ZSV of the machine non-sinusoidal back-EMF.

The main and only source of ZSV on the zero-sequence equivalent circuit produced by the machine is the non-sinusoidal machine's back-EMF. In the literature there are works that report different modulation techniques to mitigate the ZSV produced by the dual-inverter having considered the machine's back-EMF purely sinusoidal [19,137]. Even if it is possible to achieve such condition by proper shaping of the rotor magnets most of the OEW machines show a significant third harmonic content on the back-EMF since their electromagnetic design was initially thought for the operation of the stator windings connected in star configuration. It is in fact often convenient to simply take a previously designed OEW machine and open the star connected windings to reconfigure it for the OEW operation. As reported in [138, 139] the magnetization type, magnet shaping and teeth saturation can all impose influence on the third harmonic flux density distribution inducing zero-sequence back-EMF. Furthermore, it can be observed from the equivalent zero-sequence circuit of Fig. 5.1 that the ZSC dynamic is simply the one of an RL circuit. The time constant of the circuit is strictly dependant from the stator winding resistance R_s and the zero-sequence inductance L_0 which, as it was shown in Chapter 3, corresponds to the machine leakage inductance L_{ls}. It is straightforward to observe that the lower is the time constant $R_s L_0$ the higher is going to be the ZSC variation under a given voltage for a finite time. The lower the L_0 the higher is going to be the ZSC ripple, which could

potentially harm the switching devices. As already described the ZSC is an unwanted consequence of connecting the two VSCs to the same dc-link, it significantly reduces the performance of the drive by reducing the system efficiency and introducing torque oscillations. Given that the additional flow of ZSC is negative for the system whether the ZSC is acceptable or not depends on the machine parameters and converter's voltages according to Fig. 5.1.

5.3 Power Converter's non-linearities Effects

It is well known that power devices behaviour is far from linear, especially at low current amplitudes. These non-linearities cause a distortion of the output voltage of the power converter. Particularly for high performance drives where accurate voltage needs to be applied the voltage non-linearities can cause a significant degradation of the performance. If the distortion is not accurately modelled the voltage that is thought to be supplied will be different from the real one. The total distortion of the output voltage can be attributed to two main non-linear behaviours:

1. the switch Dead-Time (DT) used for avoiding short-circuit occurrence on the converter leg;
2. Voltage Drops across current carrying semiconductor devices. .

The DT and the voltage drops represent the 80% and 15% of the total distortion respectively, the remaining 5% can be attributed to other effects such as turn on/off delays of active switches, effects of parasitic capacitance on rise/fall times and the zero current clamping effect [113]. Accurate modelling of the DT has been done in [114,115]. As the switching frequency and/or the desired performance are increased, the distortions on the output voltages due to the non ideal inverter behaviour may become unacceptable, not only in open-loop systems but also in closed-loop controlled systems especially when advanced techniques such as sensorless control, parameters

estimation or predictive current control are used. The analysis of the effect of the PE non-linearities on the dual-inverter topology can be carried out better if approached with the study of the individual standard two-level VSCs first. Firstly the voltage non-linearities of the standard two-level converter are analysed and after the analysis is extended to the dual-inverter topology. In this Thesis the devices voltage drops are neglected since this voltage is negligible in compare to the dc bus voltage. The effect of the DT on the ZSV is the main focus of this thesis and it will be discussed in the following sections.

5.3.1 Two-level VSC DT Analysis

Failure of the switching devices and even of the whole inverter is possible if a DT is not added in the control scheme to ensure proper operation of the inverter. In this way the bridge shoot through can always be avoided eliminating additional losses or even thermal runaway. Usually several microseconds are required for the DT which are no longer ignorable in the inverter modelling. A generic leg of a two-level converter is shown in Fig. 5.2. It is considered a phase current to be positive when flowing from the dc-link source to the load, it is considered negative otherwise. There are four possible combinations of phase current sign and top switch state:

a. top switch s_j turned on and phase current i_j positive
b. top switch s_j turned off and phase current i_j positive
c. top switch s_j turned on and phase current i_j negative
d. top switch s_j turned off and phase current i_j negative

where i is the phase current, s is the switching state of the leg top device and j stands for the j^{th} inverter leg.

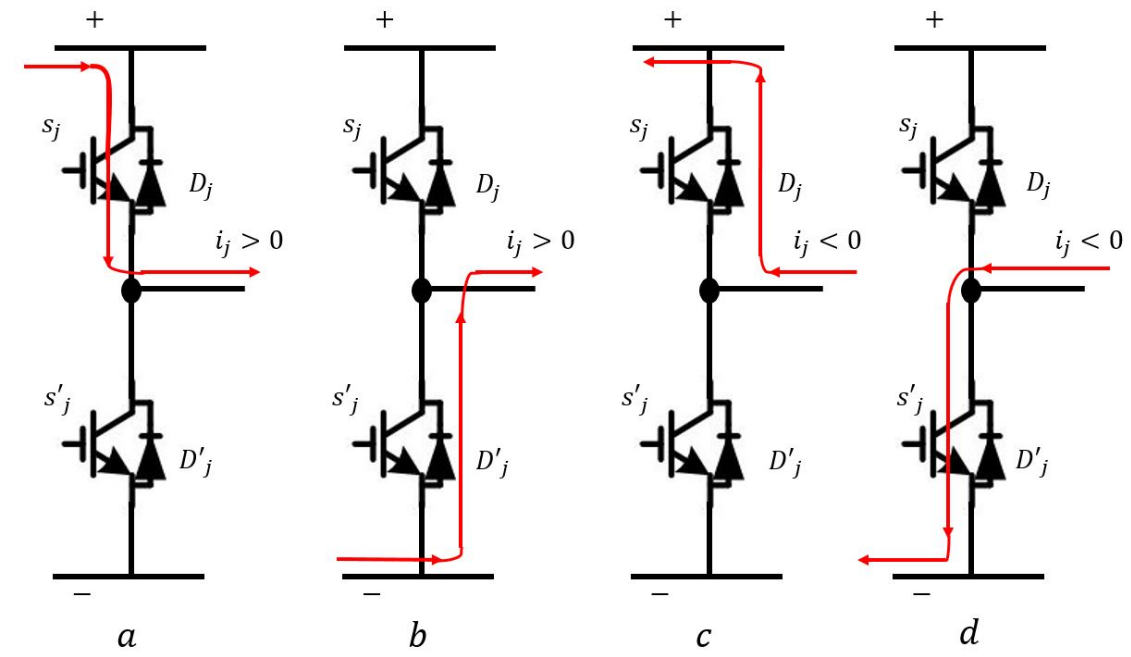


Figure 5.2: Single leg of a two-level converter. Four combinations of switch state and phase current.

The DT is implemented as a delay of a few microseconds from the time instant at which a switching device is supposed to turn on. Even if the DT is always applied to the gate signal coming from the modulator the phase voltage distortion happens only in two of the four cases of which discussed previously. The phase voltage distortion happens in the following situations: when s_j switches from 0 to 1 and $i_j > 0$ (case a) or s_j switches from 1 to 0 and $i_j < 0$ (case d). To clarify the effect of the DT, lets consider the leg switch states and the leg voltage.

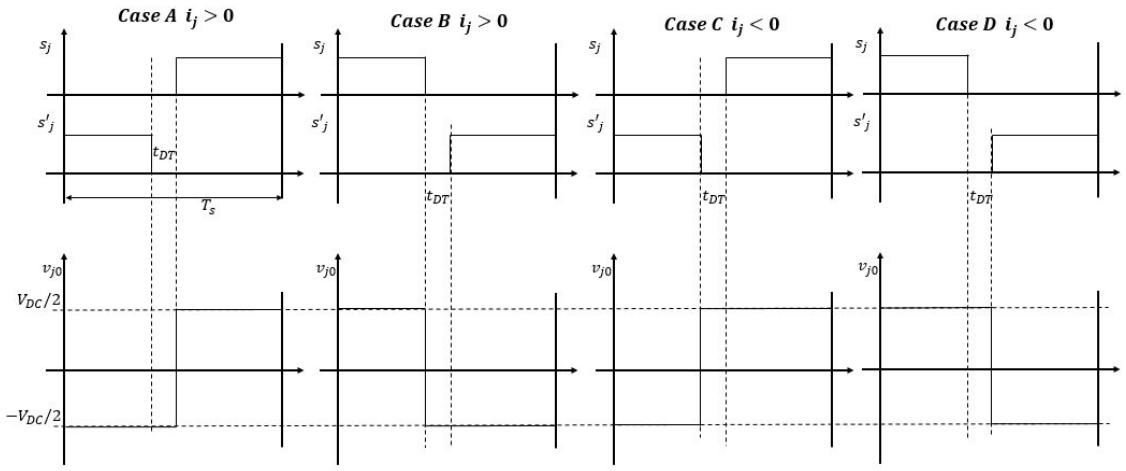


Figure 5.3: Top: switch states of converter's leg. Bottom: phase voltage

By looking at case (a) of Fig. 5.2 it can be seen that during the DT since the phase current is positive and both top and bottom switches are off the lower diode D'_j is conducting, therefore clamping the phase voltage at $-\frac{V_{dc}}{2}$. The detail of the upper and lower gates states and the converter output voltage are shown in 5.3. When both switches are off during the DT since the current is positive it flows through the lower diode. In case b and case c no distortion happens, in fact when both the switches are off the current flows thorough the diode. Case d is similar to case a where a distortion of the output phase voltage happens. During the DT the voltage is clamped at $\frac{V_{dc}}{2}$ while it should be $-\frac{V_{dc}}{2}$ instead.

5.3.2 Dual-Inverter DT Analysis

The manifestation of the voltage distortion due to the DT is dependant on the phase current sign and the transition of state of the upper switching device of the converter leg. In [19] the analysis of the DT in the dual-inverter topology when the modulation proposed in [35] is applied is carried out. The effect of the DT on the ZSV in this particular case has been previously discussed in Chapter 2 to give a comparison of

what has been done in previous works in the field. The presence of the DT is strictly related to the type of modulation used since changing the modulation means changing the switching pattern used to synthesise the reference voltage vector. In the following the analysis of the DT for the modulation proposed in Chapter 4 is carried out.

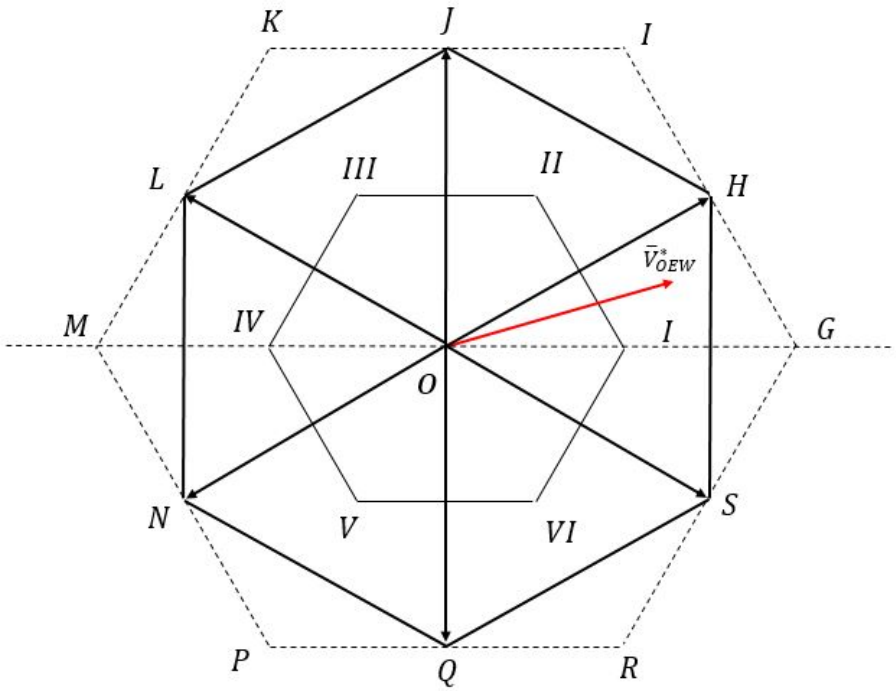


Figure 5.4: Dual-Inverter space voltage vectors and OEW Reference Voltages $\overline{V}^*_{OEW}$

Firstly two cases are considered, one for the ODD vectors and one for the EVEN ones, to study the effect of the DT on the machine ZSV. Let's first consider the case of Fig. 5.4 where the reference voltage vector $\overline{V}^*_{OEW}$ lays in sector I. According to the modulation proposed VSC A is clamped for the whole time at $\overline{V}_1$ therefore producing a constant ZSV of $-V_{DC}/6$. VSC B is forced to apply exclusively the vectors $\overline{V'}_1, \overline{V'}_3$ and $\overline{V'}_5$ in order to keep the ZSV applied on the machine zero. Fig. 5.5 shows the gate signals for the VSC A and the VSC B when the phase currents signs are $+-+$. For the sake of clarity the notation $+-+$ is adopted to indicate the phase currents polarity, when $+$ the phase current exits the converter leg while when $-$ flows from

the load to the source. There are three DTs happening in one sample time but only one leads to a voltage distortion on the OEW-PMSM. For leg b and c of VSC B the DT happens when the transition from $\overline{V'}_3$ to $\overline{V'}_5$ happens. It can be noticed that because of the fact that the DT on the two legs happens simultaneously there is no distortion on V_0^{OEW}. The transition from $\overline{V'}_5$ to $\overline{V'}_1$ with the considered currents polarities causes a distortion on leg a. The phase voltage $v_{aa'}$ during the DT is kept at V_{DC} instead of transitioning to 0. The resultant distortion on the ZSV applied to the machine consists in a spike of amplitude $V_{DC}/3$ and duration t_{DT}. Fig. 5.6 shows the same case of Fig. 5.5 where VSC A is clamped to $\overline{V}_1$ and the VSC B applies the 3 ODD vectors in the sequence $\overline{V'}_3, \overline{V'}_5$ and $\overline{V'}_1$. The current polarities are supposed to be $+--$. The DT distortion happens in the transition from $\overline{V'}_3$ to $\overline{V'}_5$ when on the leg b of VSC B with negative current there is a transition of the upper switch from 1 to 0. The resultant voltage distortion is a spike of $-V_{DC}/3$ and duration of t_{DT}. Summarizing for the ODD vectors when a DT distortion due to a transition from 0 to 1 happens the resultant ZSV is $V_{DC}/3$ while when the DT distortion happens because of a transition from 1 to 0 with negative current the ZSV is $-V_{DC}/3$. Similarly as done for the ODD vectors the same analysis can be carried out for the EVEN ones. The case of a reference vector laying in sector II of Fig. 5.4 is considered. VSC B is clamped to $\overline{V}_2$ while VSC B applies the three EVEN vectors in the order $\overline{V'}_2, \overline{V'}_6$ and $\overline{V'}_4$.

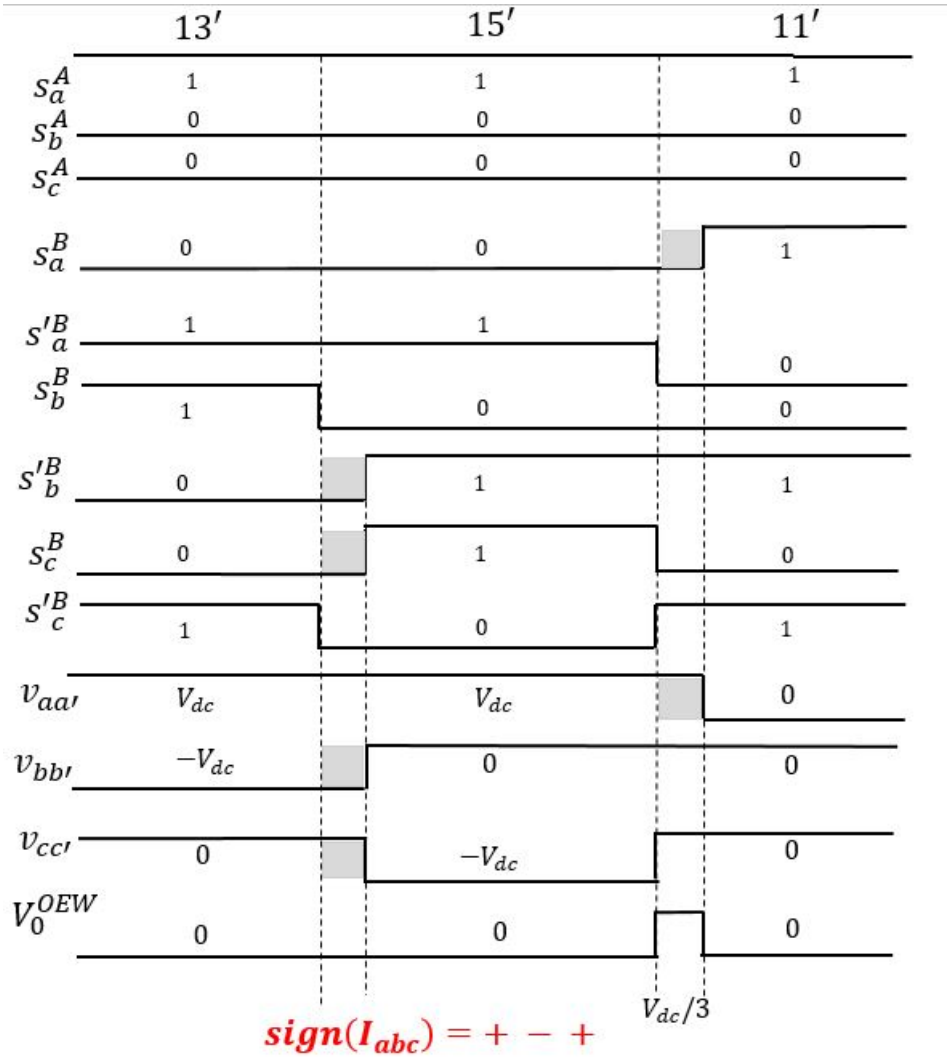


Figure 5.5: DT effect on V_0^{OEW} for the ODD vectors with phase current polarities of $+-+$. From top: top gate signals of VSC A. top and bottom gate signal of VSC B. Machine phase voltages $v_{aa'}, v_{bb'}$ and $v_{cc'}$. OEW-PMSM ZSV V_0^{OEW}.

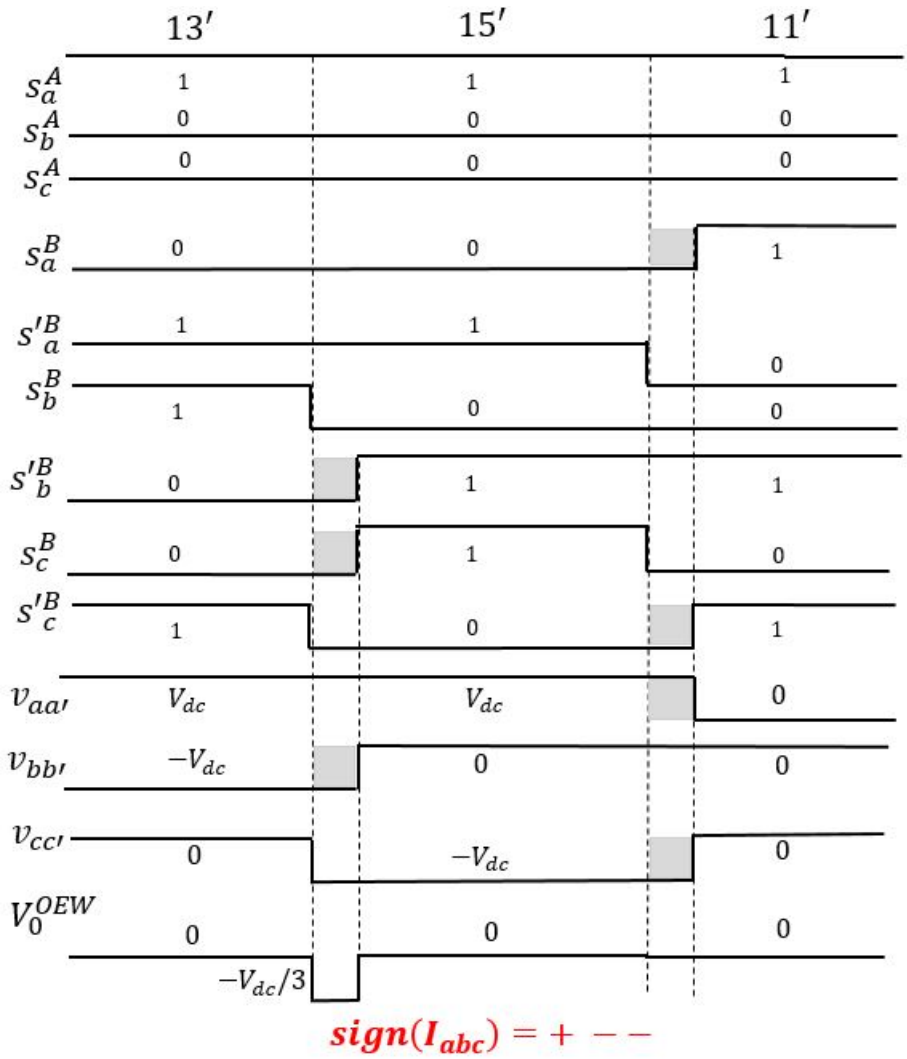


Figure 5.6: DT effect on V_0^{OEW} for the ODD vectors with phase current polarities of $+--$. From top: top gate signals of VSC A. top and bottom gate signal of VSC B. Machine phase voltages $v_{aa'}, v_{bb'}$ and $v_{cc'}$. OEW-PMSM ZSV V_0^{OEW}.

In 5.7 during the transition from $\overline{V'}_2$ to $\overline{V'}_6$ leg c of VSC B is subject to a transition from 0 to 1 with positive phase current leading to a ZSV distortion of $V_{DC}/3$. During the transition from $\overline{V'}_6$ to $\overline{V'}_4$ both legs a and b are subject to the DT distortion therefore cancelling each other and not causing any distortion on the ZSV V_0^{OEW} applied to the machine. In Fig. 5.8 the current polarities considered are $--+$. In

the first vector switch the DT distortion is present on both legs b and c therefore even if the phase voltage gets distorted the resulting ZSV is not. In the transition from $\overline{V'}_6$ to $\overline{V'}_4$ leg a is subject to DT when switching from 1 to 0 with negative phase current leading to a ZSV on the OEW load of $-V_{DC}/3$. It can be noticed that the behaviour under the DT is identical for both groups of ODD and EVEN vectors. Table 5.1 summarises the effect of the DT on the ZSV V_0^{OEW} for both sets of vectors.

Table 5.1: DT Effect on the ZSV V_0^{OEW}

Current Polarity	Switch Transition	V_0^{OEW}
+	$0 \rightarrow 1$	$V_{DC}/3$
-	$1 \rightarrow 0$	$-V_{DC}/3$

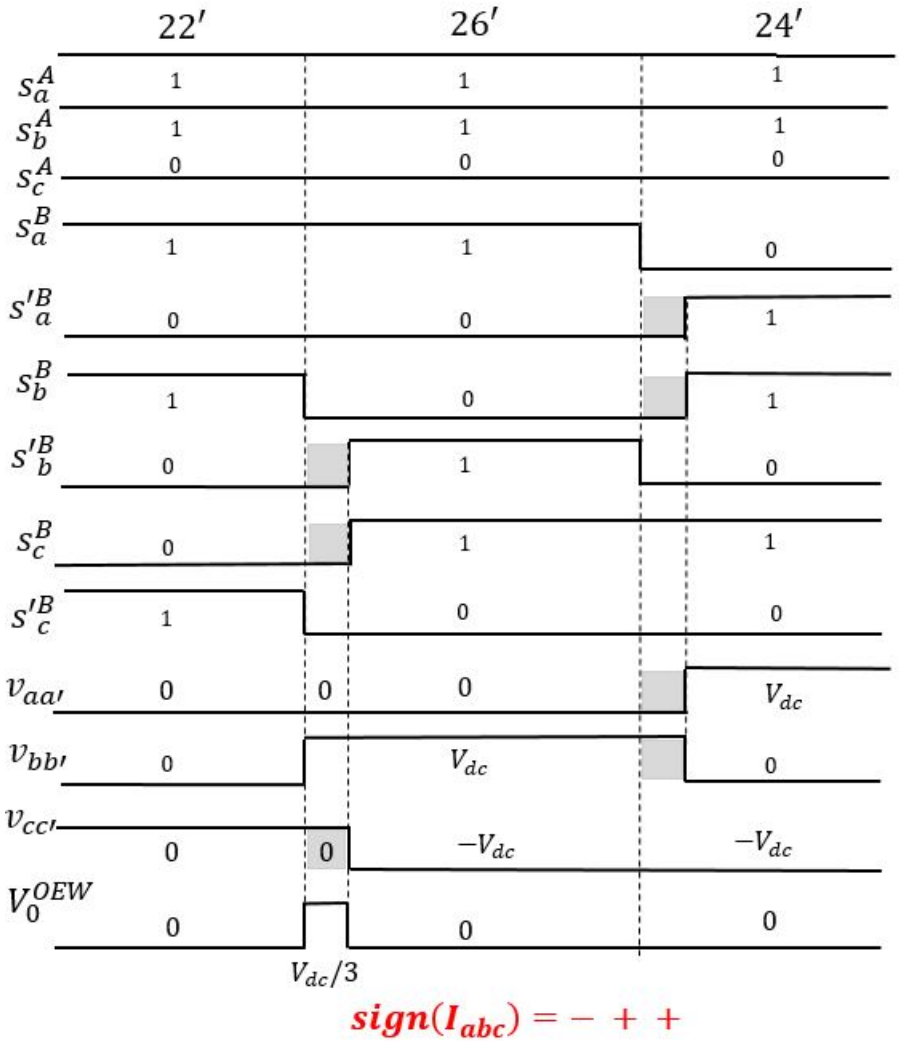


Figure 5.7: DT effect on V_0^{OEW} for the EVEN vectors with phase current polarities of $-++$. From top: top gate signals of VSC A. top and bottom gate signal of VSC B. Machine phase voltages $v_{aa'}, v_{bb'}$ and $v_{cc'}$. OEW-PMSM ZSV V_0^{OEW}.

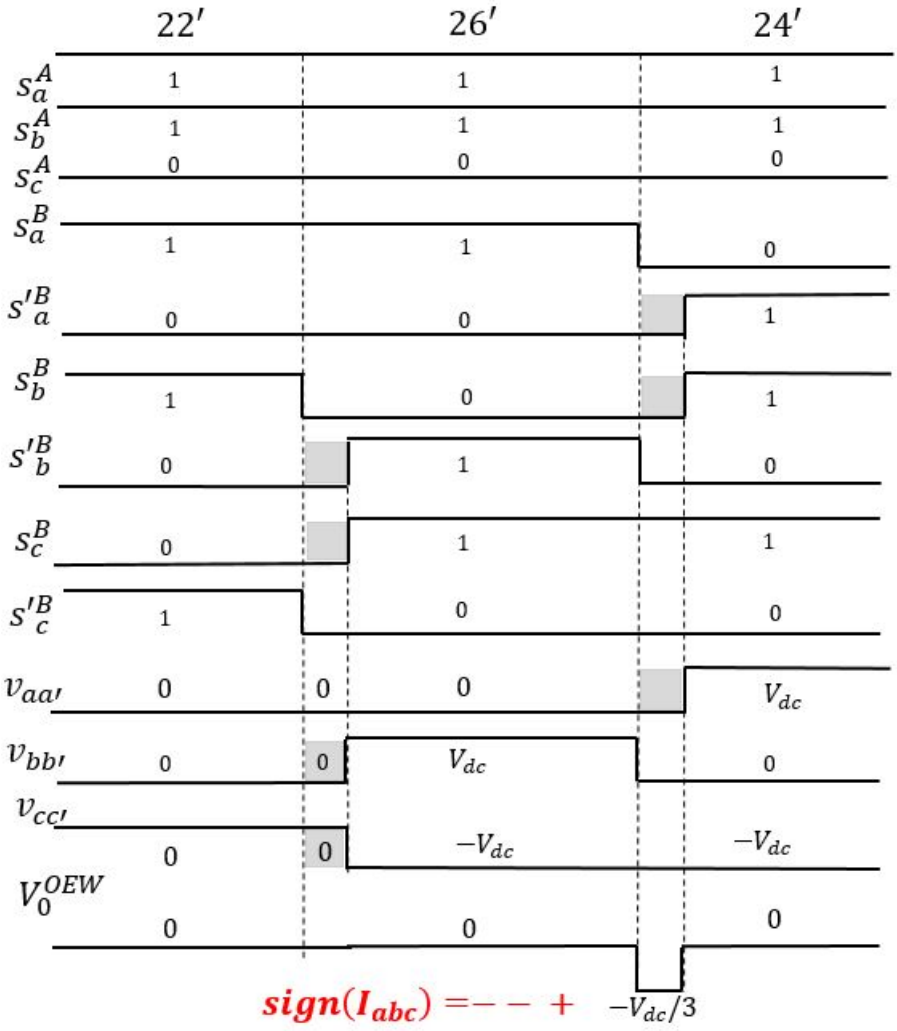


Figure 5.8: DT effect on V_0^{OEW} for the EVEN vectors with phase current polarities of $--+$. From top: top gate signals of VSC A. top and bottom gate signal of VSC B. Machine phase voltages $v_{aa'}, v_{bb'}$ and $v_{cc'}$. OEW-PMSM ZSV V_0^{OEW}.

5.3.3 Permutations of the Three Active Vectors

An additional degree of freedom for the three active vectors SVM is the order in which the voltage vectors are applied. Different strategies for organising the order

of the active vectors can impact on the number of switching per sample time and on the phase current THD. The three vectors could be applied contiguously or could be split over the sample time. As a first analysis the easier case of not splitting the application time of each active vector is considered. According to the modulation proposed the space voltage vectors used are three, therefore leading to six possible permutations. It is interesting to observe the distortion introduced by the DT for each permutation according to the phase currents sign. Since the phase currents signs can also assume six possible combinations there are 36 combinations among the phase currents signs and the three active vectors permutations. Table 5.2 reports the possible permutations of the order of application for the group of the three ODD vectors. When the voltage distortion on the ZSV is positive the transition from 0 to 1 with positive current polarity is highlighted in Table 5.2 in blue, while if the distortion on the ZSV is negative the transition is highlighted in red. Similarly Table 5.3 shows the possible combinations for the six phase currents polarities and the three EVEN active voltage vectors permutations.

Table 5.2: Number of DT per sample time T_s according to the phase current currents sign and the ODD space voltage sequence

Current Modes	①			②			③			④			⑤			⑥		
+	0	**0**	**1**	0	**0**	**1**	**0**	**1**	0	1	0	0	1	0	0	**0**	**1**	0
−	0	**1**	**0**	**1**	**0**	0	0	0	1	0	0	1	0	**1**	**0**	**1**	**0**	0
−	**1**	**0**	0	0	**1**	**0**	**1**	**0**	0	0	**1**	**0**	0	0	1	0	0	1
+	0	**0**	**1**	0	**0**	**1**	**0**	**1**	0	1	0	0	1	0	0	**0**	**1**	0
+	**0**	**1**	0	1	0	0	0	**0**	**1**	0	**0**	**1**	**0**	**1**	0	1	0	0
−	**1**	**0**	0	0	**1**	**0**	**1**	**0**	0	0	**1**	**0**	0	0	1	0	0	1
−	0	0	1	0	0	1	0	**1**	**0**	**1**	**0**	0	**1**	**0**	0	0	**1**	**0**
+	**0**	**1**	0	1	0	0	0	**0**	**1**	0	**0**	**1**	**0**	**1**	0	1	0	0
−	**1**	**0**	0	0	**1**	**0**	**1**	**0**	0	0	**1**	**0**	0	0	1	0	0	1
−	0	0	1	0	0	1	0	**1**	**0**	**1**	**0**	0	**1**	**0**	0	0	**1**	**0**
+	**0**	**1**	0	1	0	0	0	**0**	**1**	0	**0**	**1**	**0**	**1**	0	1	0	0
+	1	0	0	**0**	**1**	0	1	0	0	**0**	**1**	0	0	**0**	**1**	0	**0**	**1**
−	0	0	1	0	0	1	0	**1**	**0**	**1**	**0**	0	**1**	**0**	0	0	**1**	**0**
−	0	**1**	**0**	**1**	**0**	0	0	0	1	0	0	1	0	**1**	**0**	**1**	**0**	0
+	1	0	0	**0**	**1**	0	1	0	0	**0**	**1**	0	0	**0**	**1**	0	**0**	**1**
+	0	**0**	**1**	0	**0**	**1**	**0**	**1**	0	1	0	0	1	0	0	**0**	**1**	0
−	0	**1**	**0**	**1**	**0**	0	0	0	1	0	0	1	0	**1**	**0**	**1**	**0**	0
+	1	0	0	**0**	**1**	0	1	0	0	**0**	**1**	0	0	**0**	**1**	0	**0**	**1**

From Tables 5.2 and 5.3 it can be noted that independently of the group of active vectors considered, ODD or EVEN, and independently of the vector permutation the sign of the voltage distortion introduced depends on the phase currents polarities. The polarities (+ - +), (+ + -) and (- + +) cause positive voltage distortion on the zero axis while (+ - -), (- + -) and (- - +) are responsible for negative voltage distortions. As it was shown in Fig. 5.5 and Fig. 5.7 for the ODD and EVEN vectors respectively, when two DT distortions of opposite sign happen simultaneously on two

Table 5.3: DT per sample time T_s according to the phase current currents sign and the space voltage sequence for the EVEN group.

Current Modes	①			②			③			④			⑤			⑥		
+	1	**0**	**1**	**0**	**1**	1	1	1	0	1	1	0	1	**0**	**1**	**0**	**1**	1
−	0	1	1	**1**	**0**	1	0	1	1	**1**	**0**	1	1	**1**	**0**	1	**1**	**0**
−	1	**1**	**0**	1	**1**	**0**	**1**	**0**	1	0	1	1	0	1	1	**1**	**0**	1
+	1	**0**	**1**	**0**	**1**	1	1	1	0	1	1	0	1	**0**	**1**	**0**	**1**	1
+	**0**	**1**	1	1	**0**	**1**	**0**	**1**	1	1	**0**	**1**	1	1	0	1	1	0
−	1	**1**	**0**	1	**1**	**0**	**1**	**0**	1	0	1	1	0	1	1	**1**	**0**	1
−	**1**	**0**	1	0	1	1	1	**1**	**0**	1	**1**	**0**	**1**	**0**	1	0	1	1
+	**0**	**1**	1	1	**0**	**1**	**0**	**1**	1	1	**0**	**1**	1	1	0	1	1	0
−	1	**1**	**0**	1	**1**	**0**	**1**	**0**	1	0	1	1	0	1	1	**1**	**0**	1
−	**1**	**0**	1	0	1	1	1	**1**	**0**	1	**1**	**0**	**1**	**0**	1	0	1	1
+	**0**	**1**	1	1	**0**	**1**	**0**	**1**	1	1	**0**	**1**	1	1	0	1	1	0
+	1	1	0	1	1	0	1	**0**	**1**	**0**	**1**	1	**0**	**1**	1	1	**0**	**1**
−	**1**	**0**	1	0	1	1	1	**1**	**0**	1	**1**	**0**	**1**	**0**	1	0	1	1
−	0	1	1	**1**	**0**	1	0	1	1	**1**	**0**	1	1	**1**	**0**	1	**1**	**0**
+	1	1	0	1	1	0	1	**0**	**1**	**0**	**1**	1	**0**	**1**	1	1	**0**	**1**
+	1	**0**	**1**	**0**	**1**	1	1	1	0	1	1	0	1	**0**	**1**	**0**	**1**	1
−	0	1	1	**1**	**0**	1	0	1	1	**1**	**0**	1	1	**1**	**0**	1	**1**	**0**
+	1	1	0	1	1	0	1	**0**	**1**	**0**	**1**	1	**0**	**1**	1	1	**0**	**1**

separate legs the resultant distortion on the ZSV is cancelled. Nevertheless for each current sign and permutation theoretically the ZSV distortion introduced by the DT can assume both polarities if only one of the two DT happening simultaneously would be compensated. This observation is particularly important because it highlights the fact that independently of the current polarity and vectors permutation it is possible to introduce either a positive or negative ZSV due to the DT distortion if a suitable DT compensation method is introduced. Since the main interest is related to the ZSC i_0 control less attention as been given to which permutation of the three active vectors to select.

5.4 Pulse Based Dead Time Compensation Method

Among the different DT compensation techniques the one described in [132] is particularly easy to implement achieving good results in cancelling the voltage distortion introduced by the DT. The proposed method is known under the name of Pulse Based Dead Time Compensation (PBDTC). The DT compensation is achieved by updating the turn-on time of the power devices at the beginning of a PWM cycle and the turn-off time at the midpoint of the PWM cycle.

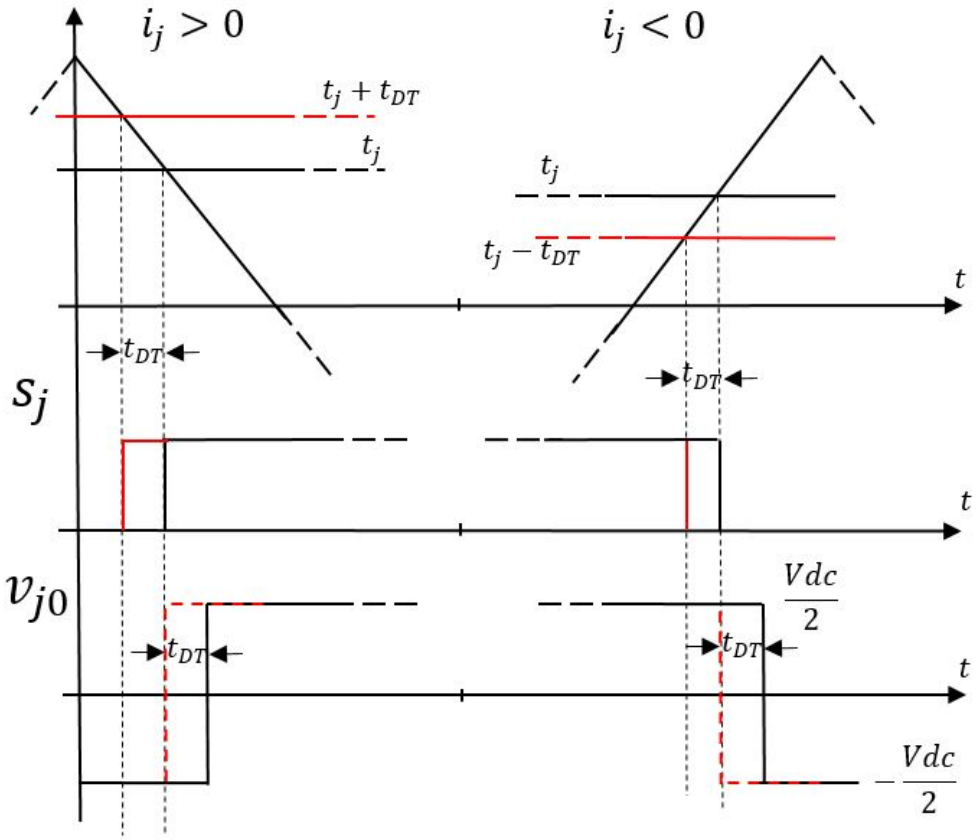


Figure 5.9: Pulse patterns for PBDTC correction for positive and negative i_x.

To compensate for the possible voltage distortion introduced by the DT the PBDTC

algorithm acts by simply correcting the pulse time. As it can be seen from Fig. 5.9 the DT introduces a delay of t_{DT} on the reference gate signal, the new gate signals corrected by the DT action is therefore responsible for possible deviations of the leg voltage from the desired one depending on the phase current polarity. Indeed the PBDTC is based on the phase current polarity detection. Fig. 5.9 shows how the two cases in which the DT causes a voltage distortion. In the first case the transition of the upper power devices is from off to on (0 to 1) and the phase current flows to the load (positive current) while in the second case the transition of the upper power devices is from on to off (1 to 0) and the phase current flows from the load to the dc-link source (negative current). In the first case, to avoid the leg voltage distortion, the switching is anticipated by t_{DT}, similarly in the second case when the transition is from on to off the switching is also anticipated. Firstly the current polarity is checked, then the slope of the carrier is checked. If the slope is negative it means that at a certain instant in the sample time T_s there will be a transition from 0 to 1, if the phase current is positive then to the modulating signal is added t_{DT} to anticipate the switching. Similarly if the carrier slope is positive it means that a transition from 1 to 0 will happen, if the phase current is negative then to the modulating signal is subtracted t_{DT} to anticipate the switching. With these two simple checks the condition in which the DT causes a voltage distortion is identified. The PBDTC uses minimal software code and it also allows to modify the switching DT to account for dissimilar turn-on and turn-off characteristics of the power devices, thus eliminating the need for power device measurement. Fig. 5.10 reports the block diagram that explains the PBDTC implementation. The sign of the i_j phase current is checked, secondly the value of the top gate signal s_j at the previous time instant and the carrier slope are checked. In fact if s_j is 1 and the carrier slope is positive it means there will be a transition from 0 to 1, vice versa if s_j is 0 and the carrier slope is negative the commutation will be from 1 to 0, the leg switch will be affected by voltage distortion depending on the phase current sign according to Fig. 5.9. By lowering or rising the leg's duty cycle of t_{DT} the gate's switch is anticipated of t_{DT} therefore obtaining the leg voltage to change at the ideal switching instant avoiding

any voltage distortion.

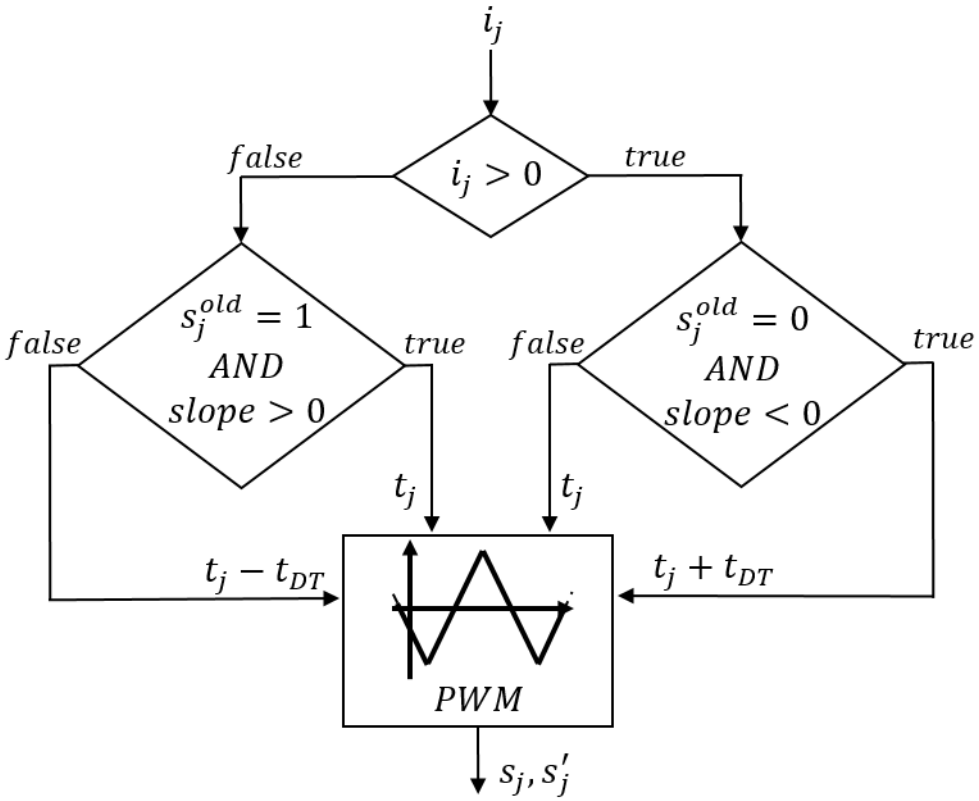


Figure 5.10: PBDTC block diagram.

The PBDTC method achieves the optimum correction since a compensation pulse by pulse is applied. The method provides stable operation since it does not introduce a any change in magnitude and phase of the applied voltage. Furthermore the PBDTC is independent of operating frequency, carrier frequency and load. Furthermore it is also compatible with digital controllers. The compensation technique is applied individually for every converter leg, this feature makes it particularly easy to be extended to different converter topologies such as the dual-inverter structure.

5.4.1 Application of the PBDTC to the Active Vector SVM for ZSV Elimination

The PBDTC compensation method is particularly easy to implement but is designed to be used for a carrier based PWM, on the other hand the modulation proposed for the fast switching VSC B is a space vector modulation one. If the PBDTC wants to be used in combination with the three active vectors SVM developed for instantaneous ZSV elimination firstly the SVM needs to be converted in a carrier based PWM. If a standard triangular carrier PWM would be used it would lead to have the zero vectors to be applied, which are not desired in order to have zero ZSV instantaneously on the machine. In order to apply the PBDTC method to the SVM used to synthesize VSC B reference voltages $\overline{V}_B^*$ it is necessary to use an hybrid SVPWM technique. It is easy to observe why a standard triangular PWM cannot be used to implement the proposed modulation for instantaneous ZSV elimination, Fig. 5.11 shows the triangular carrier, the reference signals and the corresponding leg gate signals. The zero vector is present and divided among $\overline{V}_0$ and $\overline{V}_7$, which is not acceptable since the modulation proposed uses exclusively active vectors.

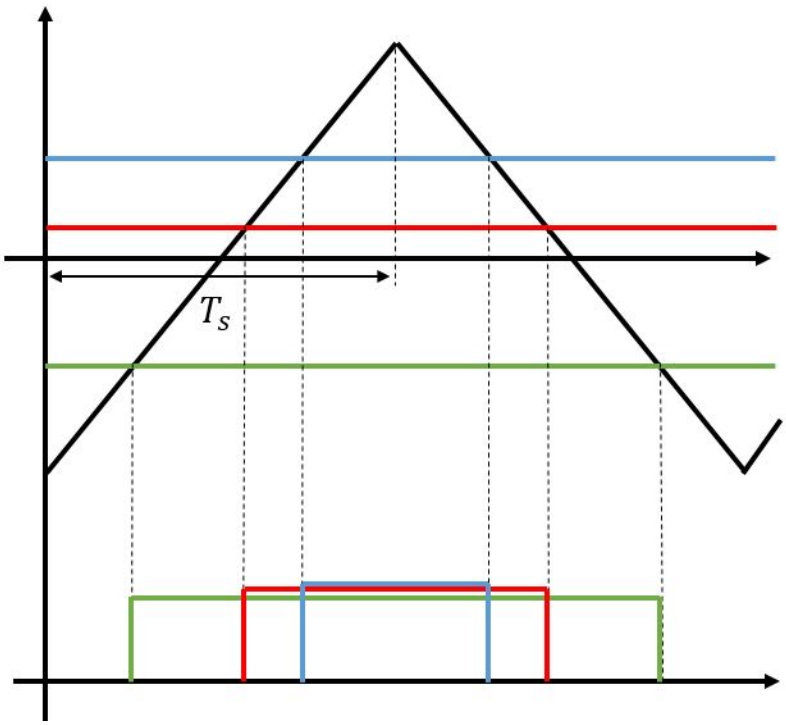


Figure 5.11: Top: triangular carrier and reference phase signals. Bottom: reference gate signals

In order to have a carrier based modulation that allows to apply exclusively the active vectors it is necessary to have either a carrier with variable slope or a modulation with variable reference modulating signals in a controller sampling time. Let's consider the case where the three active ODD voltage vectors $\overline{V'}_1, \overline{V'}_3$ and $\overline{V'}_5$ are selected to synthesize the reference vector over the controller sample time. Let's suppose that the vectors will be applied also in the order $\overline{V'}_1, \overline{V'}_3$ and $\overline{V'}_5$. The active vectors dwelling times are known and calculated using (4.10), we will refer to them as t_1, t_3 and t_5. The time instants at which there is the switch from one vector to the other are $t_1, t_1 + t_3$ and $t_1 + t_3 + t_5$ which corresponds to T_s. The first option is to use a sawtooth carrier based modulator and variable reference signals over the sample time as shown in Fig. 5.12.

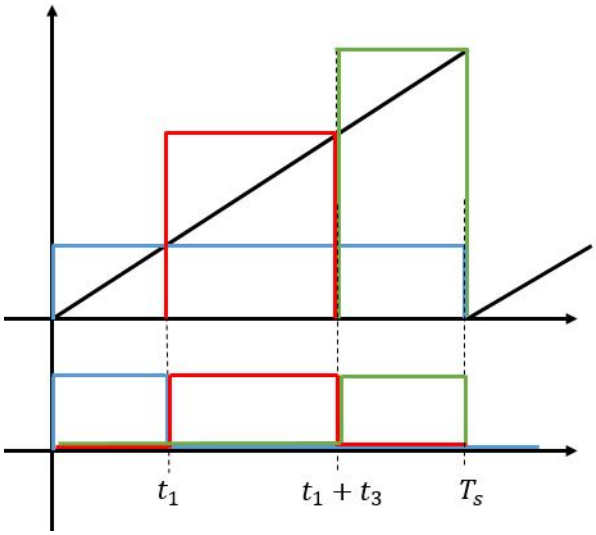


Figure 5.12: Three active vectors modulator. Top: sawtooth carrier and reference phase signals v'_a(blue), v'_b(red), v'_c(green). Bottom: reference gate signals s_a^B(blue), s_b^B(red), s_c^B(green)

The application of the PBDTC to the solution proposed in 5.12 is not straightforward. Let's suppose that the phase current polarities are - - +, the voltage distortion caused by the DT happens on leg a' in the transition from $\overline{V'}_1$ to $\overline{V'}_3$ and on legs b' and c' when switching from $\overline{V'}_3$ to $\overline{V'}_5$. In the first case, according to the PBDTC method, the reference signal of phase a' can be lowered by t_{dt} to anticipate the switching. On the other hand, for leg c' when switching from 0 to 1 a shift of t_{dt} would not result in an anticipated commutation of the reference gate signal. Another alternative is to use three separate carriers with variable slope for the three converter's legs.

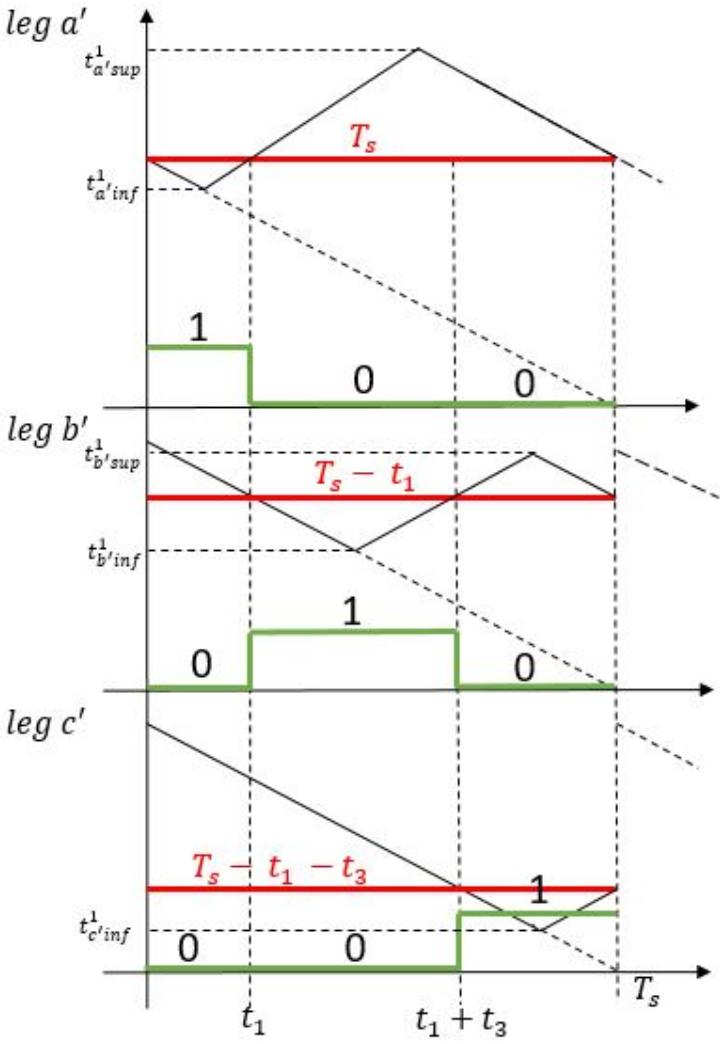


Figure 5.13: Proposed SVPWM carriers (black line), modulating signals (red line) and gate signals (green line) for the set of active ODD voltage vectors.

Fig. 5.13 shows the three carriers for each converter's leg. Each leg carrier starts at each sample time T_s from the value T_s and decreases with slope -T_s so that it would reach zero at T_s. At each sample time the dwelling times are know as well as the sequence of application of the three active vectors. As already mentioned before, the active vectors calculated at every sample time can be organised according to their

dwelling time length as t_{min}, t_{med} and t_{max}, from the shortest to the longest. For both the ODD and EVEN group of active voltage vectors if it is considered to apply them always in the sequence $t_{min}, t_{med}, t_{max}$ the possible permutations of the three vectors are six. The legs duty cycles can easily be found by observing the order in which the converter's legs are subject to the commutation. For the case considered in Fig. 5.13 the order is a', b' and c' where $t_1 = t_{min}, t_3 = t_{med}$ and $t_5 = t_{max}$. Since the switching instants are t_1 and $t_1 + t_3$ the corresponding values for the three legs duties are T_s, $T_s - t_1$ and $T_s - t_1 - t_3$ respectively. In order to have the interceptions at the desired time instants the leg carriers need to change slope after that half of the vector dwelling time has passed. Considering leg a', the upper switch is kept at 1 for t_1 and 0 for the remaining time. The time instants at which the legs carriers change slope in order to have the leg switch at the desired time are identified with t^x_{jinf} and t^x_{jsup}, where j stands for the phase and can be a', b' and c' while the suffix x determines the number of the inferior or superior point of slope change. I.e. for leg a' there are two time instants $t^1_{a'inf}$ and $t^1_{a'sup}$ where the leg carrier changes slope and are $T_s - \frac{t_1}{2}$ and $T_s + \frac{t_3+t_5}{2}$ respectively. Similarly for leg b' $t^1_{a'inf}$ and $t^1_{a'sup}$ correspond to $T_s - t_1 - \frac{t_3}{2}$ and $T_s - \frac{t_5}{2}$ respectively. Leg c' has only one inferior point of slope change which corresponds to $T_s - t_1 - t_3 - \frac{t_5}{2}$.

Table 5.4: Duty Cycles for the possible permutations of the set of ODD Voltage Vectors.

Permutation	leg $\begin{bmatrix} a' \\ b' \\ c' \end{bmatrix}$: t_{min}, t_{med}, t_{max}	Duty Cycles
①	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} T_s - t_{min} - t_{med} \\ T_s - t_{min} \\ T_s \end{bmatrix}$
②	$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} T_s - t_{min} - t_{med} \\ T_s \\ T_s - t_{min} \end{bmatrix}$
③	$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} T_s - t_{min} \\ T_s - t_{min} - t_{med} \\ T_s \end{bmatrix}$
④	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} T_s \\ T_s - t_{min} - t_{med} \\ T_s - t_{min} \end{bmatrix}$
⑤	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} T_s \\ T_s - t_{min} \\ T_s - t_{min} - t_{med} \end{bmatrix}$
⑥	$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} T_s - t_{min} \\ T_s \\ T_s - t_{min} - t_{med} \end{bmatrix}$

Table 5.4 summarizes the duty cycles for the six possible permutations of the three ODD active voltage vectors according to their dwelling time length. The same observations that have been done for the ODD vectors can be similarly done for the EVEN vectors group.

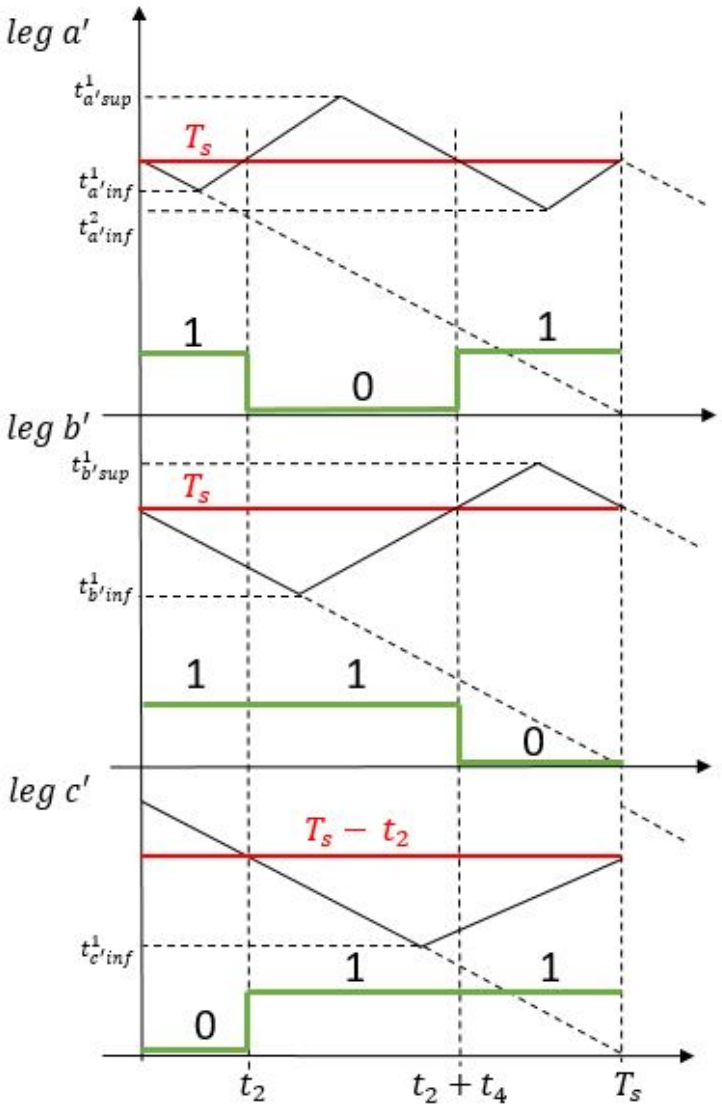


Figure 5.14: Proposed SVPWM carriers (black line), modulating signals (red line) and gate signals (green line) for the set of active EVEN voltage vectors.

Fig. 5.14 shows the case where the EVEN vectors $\overline{V'}_2, \overline{V'}_4$ and $\overline{V'}_6$ are applied and where the dwelling times correspond to $t_2 = t_{min}, t_4 = t_{med}$ and $t_6 = t_{max}$. The time instants at which there is a vector switch are t_2 and $t_2 + t_4$ for the transition from $\overline{V'}_2$ to $\overline{V'}_4$ and from $\overline{V'}_4$ to $\overline{V'}_6$ respectively. The duty cycles for the three legs are

T_s, T_s and $T_s - t_2$. The time instants of slope change can be easily identified. For leg a' $t^1_{a'inf}$, $t^1_{a'sup}$ and $t^2_{a'inf}$ are $T_s - \frac{t_2}{2}$, $T_s + \frac{t_4}{2}$ and $T_s - \frac{t_6}{2}$ respectively. For leg b' $t^1_{b'inf}$ is $T_s - t_2 - \frac{t_4}{2}$ while $t^1_{b'sup}$ is $T_s + \frac{t_6}{2}$. Leg c' has exclusively one inferior limit for the carrier of $T_s - t_2 - \frac{t_4}{2}$. Table 5.5 summarizes the duty cycles for the six possible permutations of the three EVEN active voltage vectors according to their dwelling time length.

Table 5.5: Duty Cycles for the possible permutations of the set of EVEN Voltage Vectors.

Permutation	leg $\begin{bmatrix} a' \\ b' \\ c' \end{bmatrix}$: t_{min}, t_{med}, t_{max}	Duty Cycles
①	$\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} T_s \\ T_s - t_{min} \\ T_s \end{bmatrix}$
②	$\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} T_s - t_{min} \\ T_s \\ T_s \end{bmatrix}$
③	$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} T_s \\ T_s - t_{min} \\ T_s \end{bmatrix}$
④	$\begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} T_s \\ T_s \\ T_s - t_{min} \end{bmatrix}$
⑤	$\begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} T_s \\ T_s \\ T_s - t_{min} \end{bmatrix}$
⑥	$\begin{bmatrix} 0 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} T_s - t_{min} \\ T_s \\ T_s \end{bmatrix}$

As it has been done for the duty cycles, also the carrier limits t^x_{jinf} and t^x_{jsup} at which the slope transition happens for each permutation can be identified. After having considered both group of ODD and EVEN vectors and their possible permutations, it has been observed that t^x_{jinf} and t^x_{jsup} can assume the following values

$$\begin{cases} tr_1 = T_s - t_{min} + t_{med} + \frac{t_{max}}{2} \\ tr_2 = T_s - \frac{t_{med}}{2} \\ tr_3 = T_s + \left(\frac{t_{min}+t_{max}}{2}\right) \\ tr_4 = T_s - t_{med} - \frac{t_{min}}{2} \\ tr_5 = T_s - t_{med} - \left(\frac{t_{min}+t_{max}}{2}\right) \\ tr_6 = T_s + \frac{t_{min}}{2} \\ tr_7 = T_s - \left(\frac{t_{min}+t_{max}}{2}\right) \\ tr_8 = T_s + \frac{t_{max}}{2} \\ tr_9 = T_s - t_{med} + \frac{t_{max}}{2} \\ tr_{10} = T_s - \frac{t_{max}}{2} \end{cases} \tag{5.1}$$

Table 5.6 and Table 5.7 report the values assumed by t^x_{jinf} and t^x_{jsup} for the leg carriers for each permutation for the ODD and EVEN active vectors groups respectively.

Table 5.6: Leg Carrier thresholds for the six possible permutations of the set of ODD Voltage Vectors.

Permutation	$\begin{bmatrix} t^1_{a'inf} & t^1_{a'sup} \\ t^1_{b'inf} & t^b_{b'sup} \\ t^1_{c'inf} & t^1_{c'sup} \end{bmatrix}$
①	$\begin{bmatrix} tr_1 & T_s \\ tr_2 & tr_3 \\ tr_4 & inf \end{bmatrix}$
②	$\begin{bmatrix} tr_1 & T_s \\ tr_4 & inf \\ tr_2 & tr_3 \end{bmatrix}$
③	$\begin{bmatrix} tr_4 & inf \\ tr_1 & T_s \\ tr_2 & tr_3 \end{bmatrix}$
④	$\begin{bmatrix} tr_2 & tr_3 \\ tr_1 & T_s \\ tr_4 & inf \end{bmatrix}$
⑤	$\begin{bmatrix} tr_2 & tr_3 \\ tr_4 & inf \\ tr_1 & T_s \end{bmatrix}$
⑥	$\begin{bmatrix} tr_4 & inf \\ tr_2 & tr_3 \\ tr_1 & T_s \end{bmatrix}$

Table 5.7: Leg Carrier thresholds for the six possible permutations of the set of EVEN Voltage Vectors.

Permutation	$\begin{bmatrix} t^1_{a'inf} & t^1_{a'sup} & t^2_{a'inf} \\ t^1_{b'inf} & t^b_{b'sup} & t^2_{b'inf} \\ t^1_{c'inf} & t^1_{c'sup} & t^2_{c'inf} \end{bmatrix}$
①	$\begin{bmatrix} tr_2 & tr_6 & T_s \\ tr_5 & T_s & 0 \\ tr_7 & tr_8 & 0 \end{bmatrix}$
②	$\begin{bmatrix} tr_5 & T_s & 0 \\ tr_2 & tr_6 & T_s \\ tr_7 & tr_8 & 0 \end{bmatrix}$
③	$\begin{bmatrix} tr_7 & tr_8 & 0 \\ tr_5 & T_s & 0 \\ tr_2 & tr_6 & T_s \end{bmatrix}$
④	$\begin{bmatrix} tr_7 & tr_8 & 0 \\ tr_2 & tr_6 & T_s \\ tr_5 & T_s & 0 \end{bmatrix}$
⑤	$\begin{bmatrix} tr_2 & tr_6 & T_s \\ tr_7 & tr_8 & 0 \\ tr_5 & T_s & 0 \end{bmatrix}$
⑥	$\begin{bmatrix} tr_5 & T_s & 0 \\ tr_7 & tr_8 & 0 \\ tr_2 & tr_6 & T_s \end{bmatrix}$

The DT distortion can happen not only during the sample time but also in the vectors transitions from one sample time to the following. The transition can happen from one permutation to another belonging to the same group of vectors, ODD or EVEN, or to different ones. In all these cases the transition can be taken into consideration and the leg carriers can be adapted to allow for DT compensation through the PBDTC.

5.5 Dead-Time Hysteresis Control of the ZSC

The PBDTC method applied to the proposed SVM for instantaneous ZSV elimination is useful to achieve the compensation of the ZSV distortion introduced by the DT and consequently the elimination of the associated ZSC. Possible imperfections in the compensation of the DT are caused by neglecting the real behaviour of the switching devices. The turn-on and turn-off of the devices is dependant on the current amplitude, therefore they change depending on the machine operating point. At a first analysis the switching devices are considered to be ideal. Further on, in the experimental validation of the proposed work the real behaviour cannot be neglected and its impact will be discussed showing that for the purpose of this work the initial assumption is not restrictive.

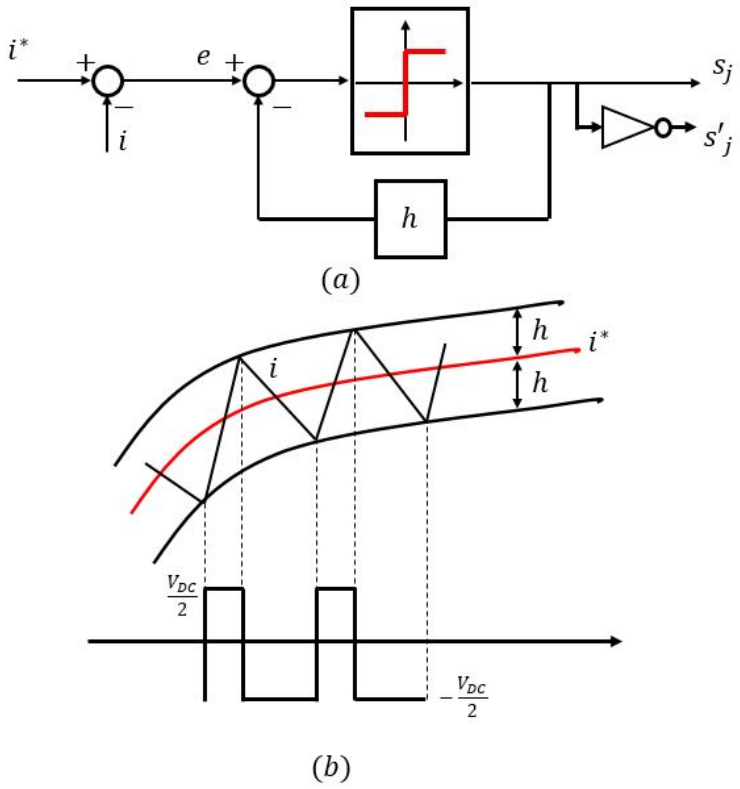


Figure 5.15: Implementation Logic of the proposed SVPWM for the three active voltage vectors modulation.

As it can be seen from the zero-axis equivalent circuit of 5.1 even if the ZSV produced by the dual-inverter is eliminated by implementing the proposed modulation and by compensating the DT distortion the resultant ZSV on the circuit would still be different from zero. In fact when the machine is rotating the non-sinusoidal back-EMF induces a voltage also on the zero-axis which, consequently causes the circulation of a ZSC. The harmonic content of the ZSC due to the back-EMF depends on the harmonic content of the back-EMF itself. Since the ZSV applied by the VSCs cannot be applied due to the low zero-sequence inductance an alternative method for controlling the ZSC is needed. The PBDTC method of which discussed previously allows for the identification of the ZSV distortion introduced by the DT. In order to eliminate the

ZSC the non-linear DT action is considered. The proposed DT compensation method allows to identify when the voltage distortion happens. It also allows to eliminate the voltage distortion by anticipating of t_{DT} the switching time. On the other hand the ZSV DT distortion can be seen as a control action since it can be identified when it will happen and its sign, dependent on the phase current polarity and the switch transition. In fact the distortion introduced by the DT on the ZSV can be foreseen and it has a well known value as described in Section 5.3.2. The DT introduces a distortion on which theoretically there is no control, in particular on the time at which it manifests itself and on the intensity of the ZSV distortion introduced. As shown previously the magnitude of the voltage distortion is either $\pm\frac{V_{DC}}{3}$, while the time at which the DT distortion happens is possibly at any transition from one vector to the other depending on the phase current polarity. Theoretically the intensity could be changed by simply changing the DT duration, this would result in a distortion of the q- and d- axes since extending the DT duration would result in reducing the time of application of the space voltage vectors selected to synthesize the reference vector $\overline{V_B^*}$. Furthermore, the time at which the DT distortion is introduced could be anticipated or delayed by accurately selecting the order of the space voltage vectors according to the phase current polarity. Even though both solutions are possible, the proposed ZSC control does not exploit these possibilities in order to avoid to complicate the control strategy or to introduce distortions on the q- and d- axes.

Given the non-linear behaviour of the DT control action implementing any controller which requires to apply a control action proportional to the error between the reference and the actual i_0 current value would be infeasible. Therefore, an hysteresis control, given its simplicity of implementation, seems to be the most suitable solution. For the conventional hysteresis control a fixed-band hysteresis h is defined for the PWM inverter as shown in Fig. 5.15. Fig. 5.15(a) shows the schematic diagram of a conventional fixed-band hysteresis current-controlled PWM scheme of a generic phase current, and Fig. 5.15(b) sketches its typical current and voltage waveforms. The same logic is used to implement the DT control. The i_0 current is firstly calcu-

lated as the sum of the phase currents divided by three. The ZSC hysteresis band h is set and since the i_0 is an unwanted element in the system the reference value i_0^* is set identically to zero. In order to achieve the DT control three conditions must be satisfied:

1. Identify when the DT distortion happens and the polarity of the distortion introduced, $\pm\frac{V_{DC}}{3}$;

2. It is necessary to know the sequence of active voltage vectors and their dwelling time;

3. Being able to compensate or not the DT distortion introduced.

Whether the ZSC i_0 falls into the hysteresis band has to be checked first. A new variables DT_{en} is introduced to take into consideration if the ZSC is higher of the upper limit of the hysteresis band or lower than the inferior limit. If the ZSC is higher than the upper limit of the hysteresis band than the distortion introduced by the DT when transitioning from 1 to 0 with negative phase current is desired and the variable DT_{en} is set to 1. Similarly, if the ZSC is lower than the inferior limit of the hysteresis band a positive ZSV is desired to keep the ZSC in the hysteresis band. Therefore a switch transition from 0 to 1 with positive phase current is required and the variable DT_{en} is set to -1. Fig. 5.16 shows an example of the ZSC behaviour and the associated values of the control variable DT_{en}.

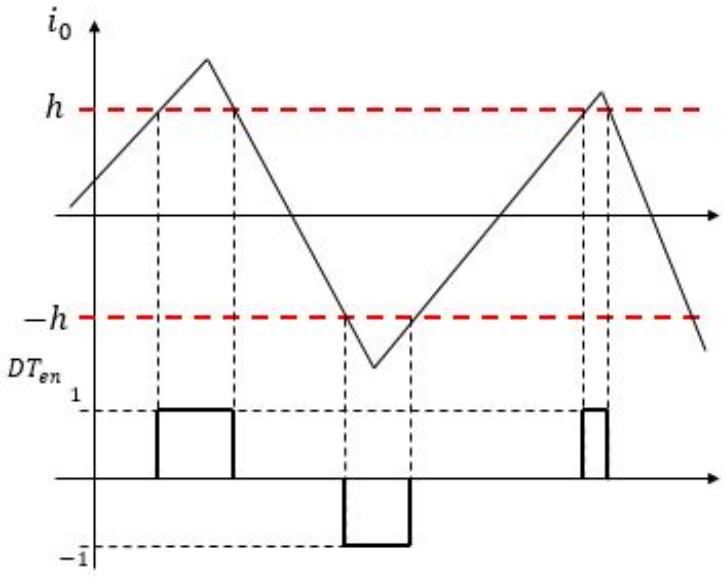


Figure 5.16: ZSC i_0, hysteresis band limits h and DT_{en} behaviour.

Now in order to achieve the DT control the variable DT_{en} is used to determine whether to compensate the DT distortion or not. For all the time in which DT_{en} is zero the DT needs to be compensated since the i_0 falls into the hysteresis band. On the other hand when DT_{en} is 1 or -1 then a DT which would cause a distortion of value $-\frac{V_{DC}}{3}$ or $\frac{V_{DC}}{3}$ respectively should not be compensated. The PBDTC logic used to compensate the DT is modified to make possible to not compensate the leg DT when needed. Also the DT control is approached for each converter leg independently. At the beginning of every sample time it is known which group of active vectors will be used, either ODD or EVEN, and the permutation in which they will be applied. Therefore given a permutation the switching pattern for every leg is defined and known. To each leg two variables k_j^{01} and k_j^{10} are associated to take into consideration the switch transition. If the ZSC i_0 is higher than the upper hysteresis limit DT_{en} is set to 1 and the desired switch transition to obtain a negative ZSV is from 1 to 0. To compensate for the DT to the voltage vector dwelling time would be subtracted the t_{DT}, if instead the DT distortion is desired the dwelling time is not corrected. Table 5.8 and 5.9

show for each permutation for the ODD and EVEN vectors which leg is subject to a switch that according to the current polarity could possibly lead to a DT control action. Observing Table 5.8 and considering the 1^{st} permutation it can be seen that the vectors are applied in the order $\overline{V'}_5, \overline{V'}_3$ and $\overline{V'}_1$. The vector $[k_b k_a k_c]$ identifies which leg switches from 0 to 1 for the transitions from $\overline{V'}_5$ to $\overline{V'}_3$, from $\overline{V'}_3$ to $\overline{V'}_1$ and from $\overline{V'}_1$ to $\overline{V'}_5$ respectively. Similarly the another vector is built considering the transitions from 1 to 0. In this way for each permutation all the commutations are identified. Table 5.8 shows the transitions for the first three permutations while Table 5.9 for the remaining three. For each permutation the case in which the same permutation is applied in the following sample time is considered.

Table 5.8: Leg transitions for the first three permutations for the ODD and EVEN vectors.

	ODD	EVEN
①	$\left[\begin{array}{ccc:c} 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \end{array}\right]$	$\left[\begin{array}{ccc:c} 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ 1 & 1 & 0 & 1 \end{array}\right]$
$DT_{en} = -1$	$\left[\begin{array}{ccc} k_b^{01} & k_a^{01} & k_c^{01} \end{array}\right]$	$\left[\begin{array}{ccc} k_b^{01} & k_a^{01} & k_c^{01} \end{array}\right]$
$DT_{en} = 1$	$\left[\begin{array}{ccc} k_c^{10} & k_b^{10} & k_a^{10} \end{array}\right]$	$\left[\begin{array}{ccc} k_a^{10} & k_c^{10} & k_b^{10} \end{array}\right]$
②	$\left[\begin{array}{ccc:c} 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \end{array}\right]$	$\left[\begin{array}{ccc:c} 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 \end{array}\right]$
$DT_{en} = -1$	$\left[\begin{array}{ccc} k_c^{01} & k_a^{01} & k_b^{01} \end{array}\right]$	$\left[\begin{array}{ccc} k_a^{01} & k_b^{01} & k_c^{01} \end{array}\right]$
$DT_{en} = 1$	$\left[\begin{array}{ccc} k_b^{10} & k_c^{10} & k_a^{10} \end{array}\right]$	$\left[\begin{array}{ccc} k_b^{10} & k_c^{10} & k_a^{10} \end{array}\right]$
③	$\left[\begin{array}{ccc:c} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{array}\right]$	$\left[\begin{array}{ccc:c} 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 \end{array}\right]$
$DT_{en} = -1$	$\left[\begin{array}{ccc} k_a^{01} & k_b^{01} & k_c^{01} \end{array}\right]$	$\left[\begin{array}{ccc} k_b^{01} & k_c^{01} & k_a^{01} \end{array}\right]$
$DT_{en} = 1$	$\left[\begin{array}{ccc} k_c^{10} & k_a^{10} & k_b^{10} \end{array}\right]$	$\left[\begin{array}{ccc} k_c^{10} & k_a^{10} & k_b^{10} \end{array}\right]$

Table 5.9: Leg transitions for the second three permutations for the ODD and EVEN vectors.

	ODD	EVEN
④	$\left[\begin{array}{ccc:c} 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \end{array}\right]$	$\left[\begin{array}{ccc:c} 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \end{array}\right]$
$DT_{en} = -1$	$\left[\begin{array}{ccc} k_c^{01} & k_b^{01} & k_a^{01} \end{array}\right]$	$\left[\begin{array}{ccc} k_c^{01} & k_b^{01} & k_a^{01} \end{array}\right]$
$DT_{en} = 1$	$\left[\begin{array}{ccc} k_a^{10} & k_c^{10} & k_b^{10} \end{array}\right]$	$\left[\begin{array}{ccc} k_b^{10} & k_a^{10} & k_c^{10} \end{array}\right]$
⑤	$\left[\begin{array}{ccc:c} 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{array}\right]$	$\left[\begin{array}{ccc:c} 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{array}\right]$
$DT_{en} = -1$	$\left[\begin{array}{ccc} k_b^{01} & k_c^{01} & k_a^{01} \end{array}\right]$	$\left[\begin{array}{ccc} k_c^{01} & k_a^{01} & k_b^{01} \end{array}\right]$
$DT_{en} = 1$	$\left[\begin{array}{ccc} k_a^{10} & k_b^{10} & k_c^{10} \end{array}\right]$	$\left[\begin{array}{ccc} k_a^{10} & k_b^{10} & k_c^{10} \end{array}\right]$
⑥	$\left[\begin{array}{ccc:c} 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{array}\right]$	$\left[\begin{array}{ccc:c} 0 & 1 & 1 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \end{array}\right]$
$DT_{en} = -1$	$\left[\begin{array}{ccc} k_a^{01} & k_c^{01} & k_b^{01} \end{array}\right]$	$\left[\begin{array}{ccc} k_a^{01} & k_c^{01} & k_b^{01} \end{array}\right]$
$DT_{en} = 1$	$\left[\begin{array}{ccc} k_b^{10} & k_a^{10} & k_c^{10} \end{array}\right]$	$\left[\begin{array}{ccc} k_c^{10} & k_b^{10} & k_a^{10} \end{array}\right]$

Fig. 5.17 shows how the variables k_j^{01} and k_j^{10} are used to implement the DT hysteresis control. At each sample time for all the three legs k_j^{01} and k_j^{10} are initialized to 1 in order to always compensate the DT distortion if present. A the higher possible frequency, the highest possible given by the controller used, it is checked if the ZSC i_0 is inside or outside the hysteresis band and consequently the variable DT_{en} is assigned. Knowing which group of vectors is used (ODD or EVEN), knowing the permutation and the dwelling times the variables k_j^{01} and k_j^{10} are assigned. With the same frequency the PBDTC algorithm is evaluated, firstly the current polarity is checked and secondly it is checked if there will be a DT distortion or not. If the DT distortion is identified it would be compensated by either summing or subtracting

t_{DT} to the duty cycle t_j. By pre-multiplying the t_{DT} by k_j^{01} or k_j^{10} it can be decided to not compensate the DT if the variables k_j^{01} or k_j^{10} are set to 0. In this way the DT is compensated when the ZSC is inside the hysteresis band and left free to introduce the desired distortion when needed.

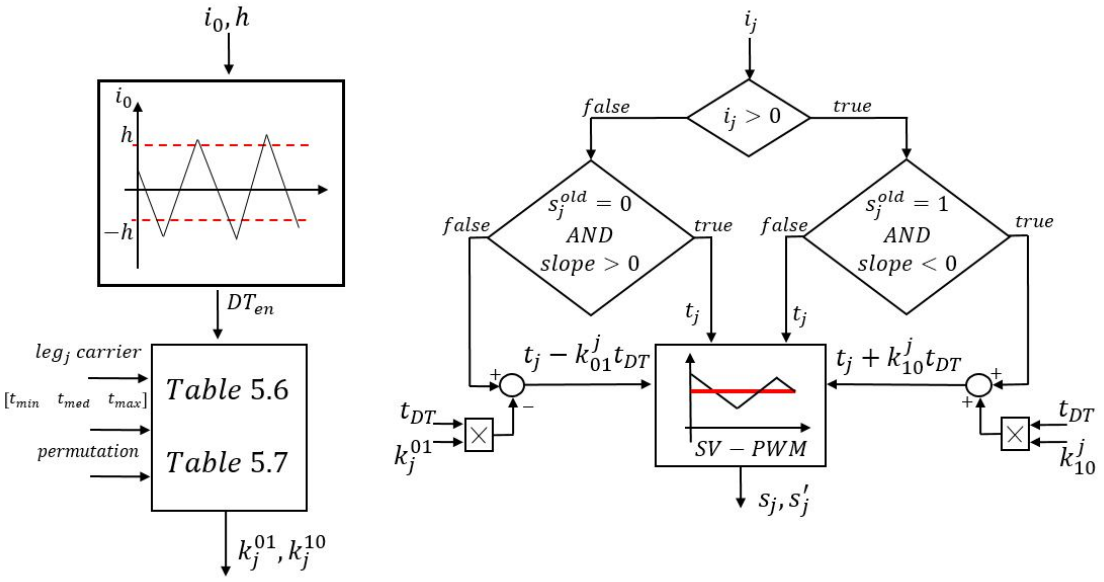


Figure 5.17: DT hysteresis control logic.

A more synthetic, but explicative, block diagram of the proposed DT hysteresis control is shown in Fig. 5.18. The logic consists in three consecutive if conditions. Firstly the phase current sign is checked, then whether a turn on or turn off of the device happens is verified. The DT is compensated by changing the modulating signal if the ZSC lays outside the hysteresis band otherwise is left unchanged in order to obtain the desired voltage distortion on the zero-axis.

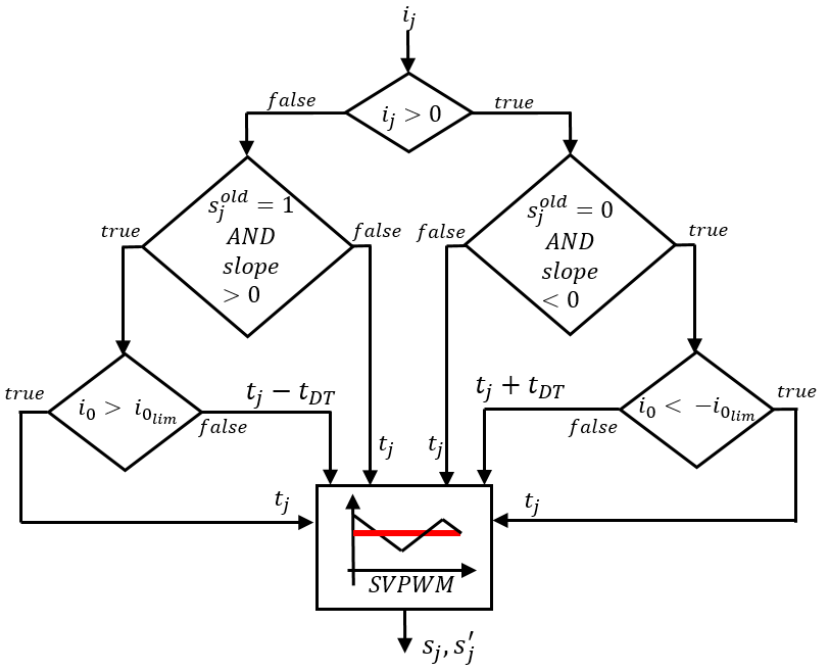


Figure 5.18: DT hysteresis control logic.

5.5.1 DT Hysteresis Control Variables

For the DT control proposed in this work the DT duration and the VSC B switching frequency have been considered constant. The number of DT control actions corresponds to the number of switching available in a sample time. Therefore, increasing the switching frequency would result in an increased number of switching events in the time unit. For simplicity in this work the switching frequency has been considered constant but theoretically could be varied. The limit associated to the proposed controller lays in the number of control actions available in the unit time and the duration of the DT itself. Here the control variables for the DT hysteresis controller are listed:

1. VSC B switching frequency;
2. DT duration;

3. Order of the three active vectors applied;

In the case that the control action provided by the DT is not sufficiently high, either the switching frequency or the DT duration can be increased. The obvious drawback would be the increase in the VSC B switching losses or the increment of the voltage distortion.

5.5.2 ZSC Amplitude due to the DT Hysteresis Control

The DT control action is applied for a fixed time of t_{DT}, the resulting ZSC can be easily evaluated by observing the zero-axis equivalent circuit. The ZSV produced by the two converters is identically zero thanks to the modulation introduced. An easy simplification is to consider the equivalent circuit to be composed exclusively by the zero-sequence inductance. Considering that the only ZSV introduced is the one due to the inverter DTs V_{DT} the following statement can be done

$$V_{DT} = L_0 \frac{d}{dt} i_0(t) \tag{5.2}$$

Discretizing (5.2) the current variation due to the ZSV introduced by the DT can be evaluated:

$$i_{0_{k+1}} - i_{0_k} = \frac{V_{DT} t_{DT}}{L_0} = \frac{V_{DC} t_{DT}}{3L_0} \tag{5.3}$$

Considering the values used for the high-speed starter generator the ZSC variation during a DT is

$$i_{0_{k+1}} - i_{0_k} = \frac{540 * 1 * 10^{-6}}{3 * 78.5 * 10^{-6}} = 2.29A \tag{5.4}$$

According to (5.4) each time a DT distortion is introduced a ZSC variation of 2.29 A is caused, either positive or negative according to the sign of the ZSV introduced by the DT. Multiple DT allow for a hysteresis DT control of the ZSC. Similarly the entity of the ZSC variation caused by the DT for the OEW-PMSM used to experimentally validate the control strategy proposed is

$$i_{0_{k+1}} - i_{0_k} = \frac{100 * 1 * 10^{-6}}{3 * 0.49 * 10^{-3}} = 0.067A \tag{5.5}$$

5.6 Conclusions

In this Chapter the the effect of the power converter's non-linearities on a VSC drive have been considered. In particular, attention has been given to the DT effect on the standard two-level VSC since the dual-inverter is simply made of two two-level VSCs. The analysis of the DT effect in conjunction with the modulation proposed for the ZSV elimination has been carried out. The PBDTC strategy has been presented and it is shown how it is possible to adapt it to the dual-inverter topology in order to achieve the DT compensation. Finally it has been shown how the ZSV distortion introduced by the DT can be used as a zero-axis control action for the third harmonic ZSC. A switch commutation from 0 to 1 or from 1 to 0 could lead to a V_0 of $\frac{V_{DC}}{3}$ or $-\frac{V_{DC}}{3}$ respectively. Based on the previous observation an hysteresis i_0 controller as been developed. It is checked if the the i_0 current is bigger or smaller of the desired hysteresis band and accordingly is decided if to compensate the DT or not. In the following chapters the simulation results and the implementation of the proposed strategy are proposed.

Chapter 6

Current and Speed Loop Control Design

6.1 Introduction

This Chapter deals with the design and tuning of the current and speed loop controllers. The state space approach is used to design the current controller. First, a general overview of the design method is given, furthermore how to select the poles locations and calculate the controller gains is explained. The electrical plant is presented and the current loop gains calculated are provided. Finally, the current loop performances are evaluated by means of frequency response and step response. Regarding the speed loop controller, first, the structure of the mechanical plant is given. Then a brief explanation of how to design the speed and load torque observer is provided. The observer gains are calculated and the controller gain is selected.

6.2 State Space Design Approach

The state space design technique is often referred to as modern control design even though it has been in use for more than 50 years. It allows to synthesize a dynamic compensation by working directly with the state variables of the system. Advantages in the state space approach are particularly evident when complex controllers have to be designed because it allows treating the overall system as a whole, hence the controller gains that guarantee stability and good performance can be easily calculated. The state feedback control action structure is shown in Fig. 6.1 where r is the $\mathbb{R}^{(nx1)}$ reference signal, x is the $\mathbb{R}^{(nx1)}$ plant state and u is the $\mathbb{R}^{(nx1)}$ control action. The calculation of the feedback gain K can be done if the system is controllable. In fact systems that are not controllable have certain modes or subsystems that are unaffected by the control. A system is said to be controllable at time t_0 if it is possible to transfer the system from any initial state x_0 to any other state x_1 in a finite interval of time by means of a controller [140].

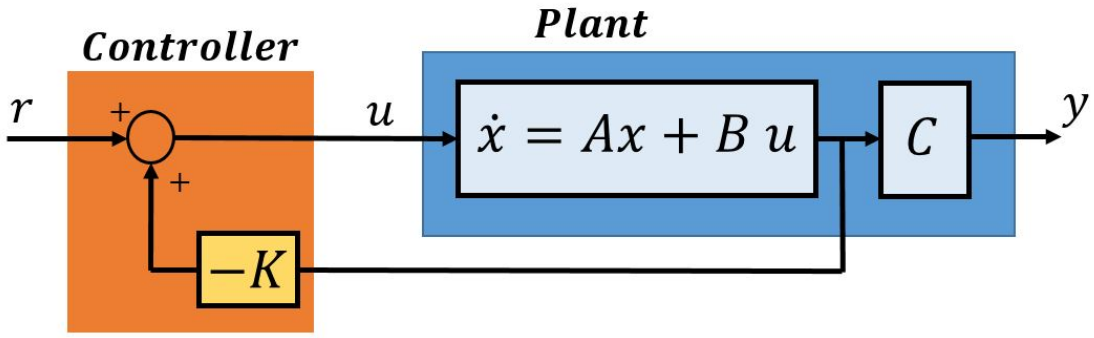


Figure 6.1: Schematic diagram of state-space design elements

If the system is controllable by means of the control law design it is possible to select the gains K so that the closed loop poles would be in the arbitrary selected location. The plant equation and the control law are summarized in (6.1)

$$\begin{cases} \frac{d}{dt}x = Ax + Bu; \\ u = -Kx \end{cases} \tag{6.1}$$

Substituting the feedback law into the plant yields to

$$\frac{d}{dt}x = (A - BK)x \tag{6.2}$$

Where the characteristic equation of this closed loop system is

$$det[sI - (A - BK)] = 0 \tag{6.3}$$

Supposing that all the pole locations $s_1, s_2, ..., s_n$ are known the gains K can be found by matching the coefficients of the polynomial described by (6.3) and the one made by the selected poles as shown in (6.4)

$$det[sI - (A - BK)] = (s - s_1)(s - s_2)...(s - s_n) \tag{6.4}$$

6.3 Current Loop Controller

As explained in the previous chapters the i_0 current is not controlled in a standard way by synthesizing the zero-sequence voltage reference with the dual-inverter, instead the ZSC is controlled by means of the DT hysteresis controller developed in Chapter 5. Therefore, according to the modulation developed there is no need of a zero-sequence axis controller. Here the q- and d- axis controller are presented. A standard PI controller has been implemented in a state feedback form. For the current loop

all the state variables (i_q and i_d) are measurable. A basic approach to design the controller is to insert an integrator between the error comparator and the plant in order to obtain a zero steady state error [141]. The resultant controller block scheme is shown in Fig. 6.2, which has been selected for both the q and d axis.

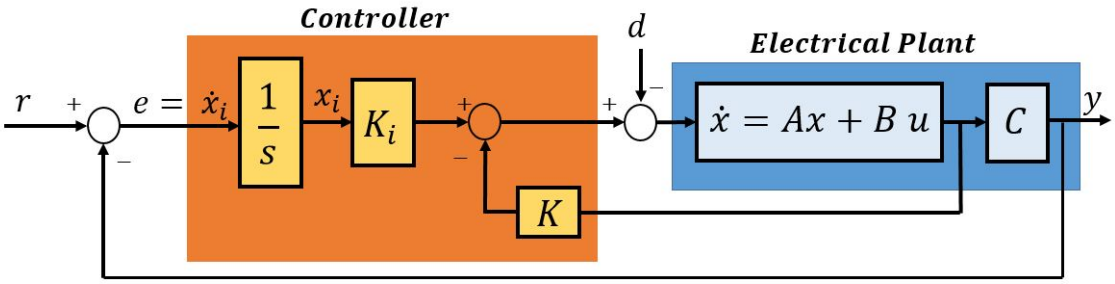


Figure 6.2: Current Control Loop structure

The electrical plant corresponds to the one described in Chapter 3. A further simplification can be done observing that the q and d axis can be decoupled implementing the following approach:

$$\begin{cases} \tilde{V_q} = V_q^* + \omega_e L_d i_d + \omega_e \lambda_m; \\ \tilde{V_d} = V_d^* - \omega_e L_q i_q \end{cases} \tag{6.5}$$

The state feedback controller references V_q^* and V_d^* are used with the machine equations to achieve the decoupling, therefore the new reference signals become $\tilde{V_q}*$ and $\tilde{V_d}$. Furthermore, since the machine considered do not present any anisotropy the q and d axis equations are identical and correspond to

$$\frac{di}{dt} = \frac{-R_s}{L} i + \frac{1}{L} V \tag{6.6}$$

where

$$A = \frac{R_s}{L}; B = \frac{1}{L}; C = 1; \tag{6.7}$$

Hereafter only one axis is considered. According to the simplifications made the current loop is the on described by Fig. 6.3.

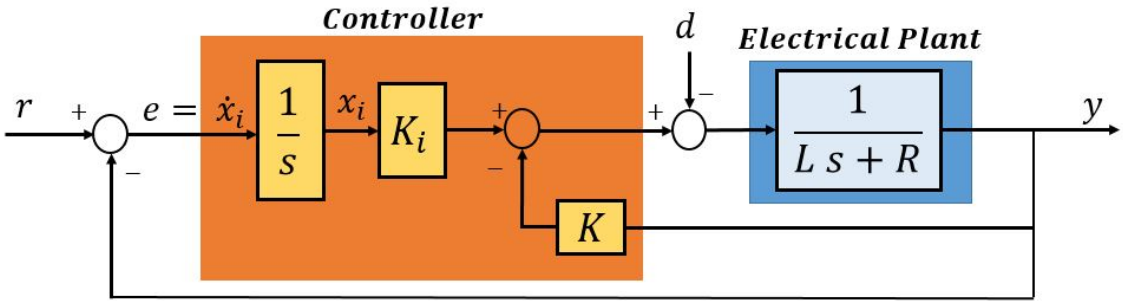


Figure 6.3: Current Control Loop structure with q and d axis decoupling

Even if the state space design approach is used to determine the controller gains the closed loop transfer function of the current loop is given in (6.8) for completeness.

$$T_{cl}(s) = \frac{\frac{K_i}{L}}{s^2 + \frac{R+K}{L}s + \frac{K_i}{L}} \tag{6.8}$$

The roots of the denominator of $T_{cl}(s)$ are the poles of the closed loop system of Fig. 6.3. Observing Fig. 6.2 it is possible to write the following equalities:

$$\begin{cases} \frac{d}{dt}x = Ax + Bu \\ y = Cx \\ u = -Kx + K_i x_i \\ e = r - y = r - Cx \end{cases} \tag{6.9}$$

Considering that the controller will be implemented on a digital processor and that the electrical plant time constant is comparable with the controller sample time T_s, it is necessary to design the controller in the discrete time domain. According to (3.25) and (3.26) the system (6.9) becomes

$$\begin{cases} x_{k+1} = \left(1 - \frac{R_s T_s}{L}\right) x_k + \frac{T_s}{L} u_k; \\ u_k = -K x_k + K_i x_{i_k} \\ e_k = r_k - y_k \\ x_{i_{k+1}} = x_{i_k} + T_s e_k = x_{i_k} + T_s r_k - T_s x_k \end{cases} \tag{6.10}$$

The plant state space system can be extended adding the integrator as

$$x_{B_{k+1}} = \Phi_B x_{B_k} + \Gamma_B u_k \tag{6.11}$$

where x_{B_k} is the augmented state vector, Φ_B and Γ_B are the augmented state and input matrix respectively, defined as

$$x_{B_k} = \begin{bmatrix} x_k & x_{i_k} \end{bmatrix}^T ; \Phi_B = \begin{bmatrix} \left(1 - \frac{R_s T_s}{L}\right) & 0 \\ -T_s & 1 \end{bmatrix} ; \Gamma_B = \begin{bmatrix} \frac{T_s}{L} \\ 0 \end{bmatrix} ; \tag{6.12}$$

and where the control action can be rewritten as

$$u_k = - \begin{bmatrix} K & -K_i \end{bmatrix} \begin{bmatrix} x_k \\ x_{i_k} \end{bmatrix} ; \tag{6.13}$$

The calculation of the controller gains K and K_i can be done by selecting the desired poles locations in the continuous domain, converting it into discrete and then using the new system matrices Φ_B and Γ_B to place them correctly. The sample time delay

introduced by the calculation time is here on purpose omitted in the synthesis of the controller. Since an accurate tuning of the current controller was not the main goal of this work it is acceptable to not take it into account.

6.3.1 Current Loop Gain Calculation

The position of the closed loop poles of the system presented in Fig. 6.3 can be arbitrarily chosen. Two possible configurations of the poles locations have been considered. The first approach is to select the two poles to be coincident at the pulsation ω_0, which leads to the corresponding characteristic polynomial shown in (6.14).

$$(s + \omega_0)^2 = s^2 + 2\omega_0 s + \omega_0^2 \tag{6.14}$$

The second solution considered is to tune the controller parameters according to the second order Butterworth filter as shown in (6.15).

$$s^2 + \sqrt{2}\omega_0 s + \omega_0^2 \tag{6.15}$$

Furthermore, ω_0 is the actual bandwidth of the closed loop system since, by definition, the amplitude response of a n-order Butterworth filter is equal to $1/\sqrt{2} = -3dB$ at the pulsation ω_0. The choice of the poles pulsation ω_0 is a trade off between having a fast reacting controller and not exceeding the intrinsic limits given by the current control bandwidth. After different attempts, the poles pulsation ω_0 has been chosen equal to $2\pi 1200 rad/s$. Table 6.1 and Table 6.2 report the current controller gains for the coincident poles and for the Butterworth poles configuration respectively.

Table 6.1: Controller Gains for Coincident Poles Configuration.

Gain	**Value**
K	19.51
K_i	7.67e4

Table 6.2: Controller Gains for Butterworth Poles Configuration.

Gain	**Value**
K	13.25
K_i	5.88e4

For the case of the two coincident poles configuration they have the same position on the real axis and no imaginary part, which corresponds to a damping of 1. In the Butterworth case one pairs of complex conjugate poles is obtained. The damping associated with this poles configuration is $1/\sqrt{2}$ which is smaller than the one associated with coincident poles leading to a bigger overshoot as it can be seen from the step response plotted in Fig. 6.4. Finally, in Fig. 6.5 the frequency response of the transfer function from the reference current to the output current for the Butterworth and the coincident poles are presented. In this work the Butterworth pole configuration has been chosen because of the faster transient response, the gains used are the ones of Table 6.2.

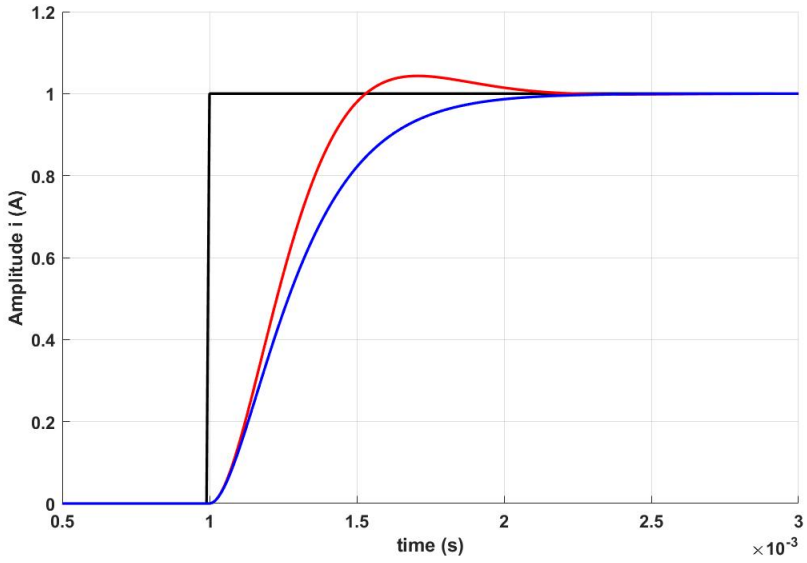


Figure 6.4: Step response map of the closed current loop for coincident (blue) and Butterworth (red) pole configuration.

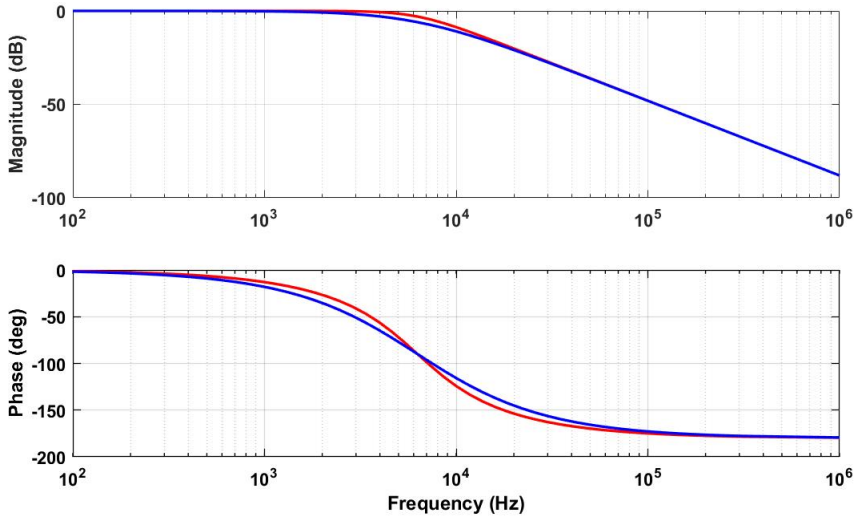


Figure 6.5: Bode plots map of the closed current loop for coincident (blue) and Butterworth (red) pole configuration.

6.4 Speed Loop Controller

Even though the easiest way to obtain the machine speed is by derivation of the position as shown in (6.16), this is not the best solution regarding the noise added on the measurement.

$$\omega_{e_k} = \frac{\theta_{e_k} - \theta_{e_{k-1}}}{T_s} \tag{6.16}$$

Any measured quantity carries inevitably with itself some noise, therefore the derivative operation is critical since it would amplify the measurement noise. An observer is introduced to identify the machine speed. Furthermore to improve the system performance also the load torque T_L and the angular position θ_m are estimated. A state observer estimates the state variables based on the measurements of the output and control variables. The considered plant is shown in the following equations

$$\begin{cases} \frac{d\theta_m}{dt} = \omega_m \\ \frac{d\omega_m}{dt} = \frac{1}{J}\Big(T_e - T_L - B\omega_m\Big) \\ \frac{dT_L}{dt} = 0 \end{cases} \tag{6.17}$$

which can be rearranged in the state space form as

$$\begin{cases} \dot{\mathbf{x}} = A\mathbf{x} + BT_e \\ y = C\mathbf{x} \end{cases} \tag{6.18}$$

where

$$\mathbf{x} = \begin{bmatrix} \theta_m \\ \omega_m \\ T_L \end{bmatrix}, A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & -\frac{B}{J} & -\frac{1}{J} \\ 0 & 0 & 0 \end{bmatrix}, B = \begin{bmatrix} 0 \\ \frac{1}{J} \\ 0 \end{bmatrix}; C = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \tag{6.19}$$

The observer is a subsystem to reconstruct the state vector of the plant. The mathematical model of the observer is basically the same as that of the plant, except that we include an additional term that includes the estimation error to compensate for inaccuracies in matrices A and B and the lack of the initial error. The estimation error, or observation error, is the difference between the measured output and the estimated output. A full order observer to estimate the angular position, the rotational speed and the load torque has been implemented as described in [141]. The mathematical model of the observer is defined as

$$\begin{cases} \dot{\hat{\mathbf{x}}} = \hat{A}\hat{\mathbf{x}} + \hat{B}T_e + L(y - \hat{y}) \\ \hat{y} = \hat{C}\hat{\mathbf{x}} \end{cases} \tag{6.20}$$

where

$$\hat{\mathbf{x}} = \begin{bmatrix} \widehat{\theta_m} \\ \widehat{\omega_m} \\ \widehat{T_L} \end{bmatrix}, \hat{A} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & -\frac{B}{J} & -\frac{1}{J} \\ 0 & 0 & 0 \end{bmatrix}, \hat{B} = \begin{bmatrix} 0 \\ \frac{1}{J} \\ 0 \end{bmatrix}; \hat{C} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \tag{6.21}$$

It can be noticed that the plant and observer matrices are assumed identical. Furthermore, given the discrete nature of the controller the observer equations should be implemented in the discrete form. On the other hand, if we consider that the plant time constants are much bigger then the controller sample time, then for a certain dynamic the poles locations do not change significantly if the synthesis is carried out in continuous or discrete. For this reason the continuous full order observer is considered. To obtain the observer error equation, let us subtract the observer state form

the plant one obtaining:

$$\dot{\mathbf{e}} = \dot{\mathbf{x}} - \dot{\hat{\mathbf{x}}} = (A - LC)\mathbf{e} \tag{6.22}$$

(6.22) gives the error dynamics. In order to set the desired dynamic performance the gain L needs to be calculated. From (6.22), a third order system is obtained, it can be noticed that one state is measurable, i.e. θ_m. Therefore the system reduces to a second order and the gains can be calculated resolving (6.23)

$$det\left(sI - \begin{bmatrix} -\frac{B}{J} & -\frac{1}{J} \\ 0 & 0 \end{bmatrix} + L\begin{bmatrix} 1 & 0 \end{bmatrix}\right) = s^2 + 2\omega_0\xi s + \omega_0^2 \tag{6.23}$$

which leads to the following gains

$$\begin{bmatrix} L_1 \\ L_2 \end{bmatrix} = \begin{bmatrix} \frac{2J\xi\omega_0 - B}{J} \\ -J\omega_0^2 \end{bmatrix} \tag{6.24}$$

The overall speed loop controller structure is made of the observer previously described and the proportional controller as shown in Fig. 6.6.

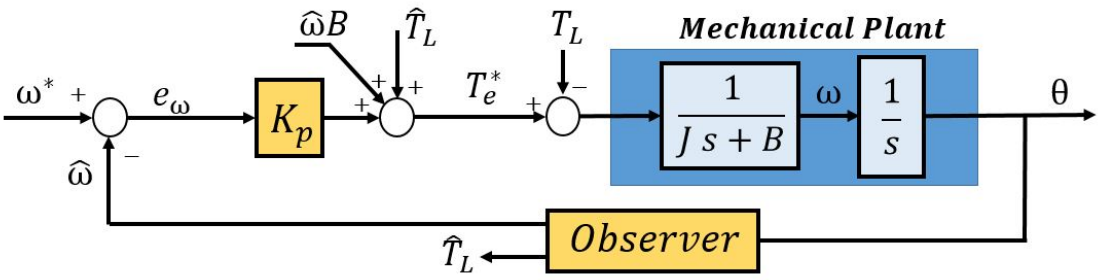


Figure 6.6: Speed Loop controller block scheme.

The controller K_p gain calculation is quite straightforward. In fact, when tuning the

proportional controller a simplification of the plant can be made observing that in the control structure the term $\hat{\omega_m}B$ is compensated in feed-forward. This allows to consider the plant as being exclusively made of the moment of inertia J when tuning the proportional gain. The closed loop transfer function of the controller and plant is shown in (6.25).

$$T_{cl,\omega}(s) = \frac{\frac{K_p}{J}}{s + \frac{K_p}{J}} \tag{6.25}$$

K_p can then be easily found by selecting the pole location for the speed loop controller as shown in 6.26

$$s + \frac{K_p}{J} = s + \omega_c \tag{6.26}$$

6.5 Conclusions

In this Chapter the current controller and speed regulator structures have been presented. The state space approach to design the current controller has been used. The electrical plant and controller have been presented and the closed loop transfer function is given. The new plant with the added integral state is described and used to design the controller after the closed loop poles locations have been selected. The current loop performance are evaluated by means of frequency response and step response. The speed loop regulator structure is presented. The design of the reduced order speed and load torque is presented. The observer gains are analytically determined and its performance are evaluated.

Chapter 7

Simulation Results

7.1 Introduction

This Chapter presents the simulation results for both the high-speed starter-generator OEW-PMSM and the scaled-down machine. The main focus of this work is to validate the proposed modulation and ZSC controller for the high-speed PMSM but since at the moment of the experimental validation the actual starter-generator was not available a scaled-down OEWM has been used. Therefore, also the simulation results for this machine are provided. This chapter is organised as follows: firstly the structure of the simulation is described, the individual elements such as the OEWM, the dual-inverter, the controller and the modulator are shown. Then the simulation results for the high-speed machine are presented. The performance under the standard PWM are shown highlighting how the ZSV, and consequently the ZSC, are not acceptable. The results for the proposed SVPWM for the instantaneous elimination of the ZSV are shown and finally the DT hysteresis controller is added and its performance in suppressing the ZSC flowing because of the non-sinusoidal machine back-EMF are shown.

7.2 Structure of the Simulation Model

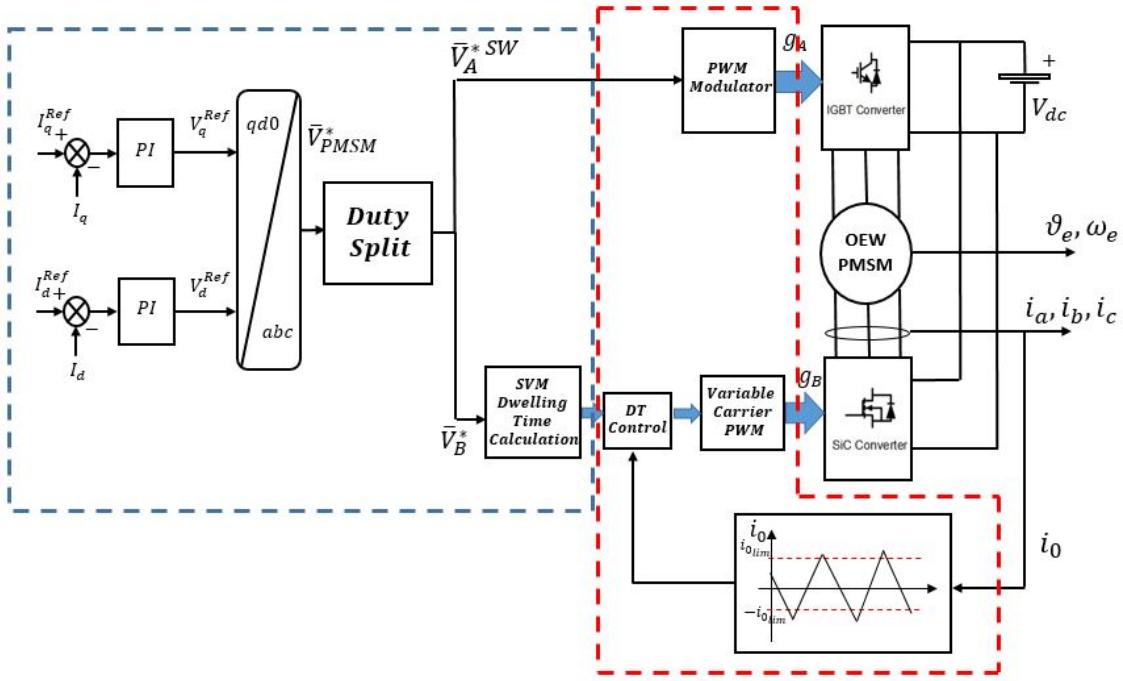


Figure 7.1: Overall control scheme of the OEW-PMSM. In the blue dashed box : DSP controller. In the red box: modulators and ZSC controller implemented in FPGA.

The simulation results that will be presented were obtained in the Matlab-Simulink environment. The discrete controllers, the machine and the PE have been all simulated with the Matlab-Simulink tools. In order to simulate the modulators and the ZSC DT hysteresis controller the System Generator toolbox of the Xilinx Blockset has been used. The modulators and controllers have been developed in the Xilinx Vivado Enviroment using the VHDL language. It is therefore possible to directly simulate in the Matlab-Simulink environment the VHDL code written for the modulation of the power converters, which will be exactly the same run on the experimental control platform. A simulation model has been built following the control scheme shown in Figure 7.1. The machine phase currents are measured, the ZSC is calculated in the FPGA and then fed to the controller. The position of the machine is acquired from

the encoder, and in conjunction with the phase currents it is used to calculate the q- and d- axis currents as shown in Appendix A. The currents are then fed to the PI controllers as presented in Chapter 6. The reference voltage split among the two VSCs is done in the DSP controller as described in Chapter 4. The square wave phase voltage references are directly fed to the PWM modulator for the IGBT converter. The reference voltages of the SiC VSC are used to calculate the dwelling times for the three active vectors SVM used to instantaneously eliminate the ZSV produced by the dual-inverter as shown in Chapter 4. The dwelling times are then fed to the modified PWM modulator described in Chapter 5. All the controllers confined in the blue dashed box of Fig. 7.1 have to be considered implemented in the DSP and running at the sampling rate T_s of 25 μs. The modulators and ZSC controller run at the FPGA clocking frequency of 100 MHz equivalent to 10 ns period. The OEW-PMSM is simulated in the continuous time domain with the equivalent phase circuit described in Section 3.2 of Chapter 3. In this way it is possible to have all the six terminals of the machine available to be connected to the power electronics. The VSCs have been modelled using the universal bridge block provided from Simulink. The on resistance of the switching devices and the forward voltage drop has been introduced to emulate the voltage non-linearity. The common dc link for the converters has been modelled as shown in Fig. 7.2. R_{dcs} is the equivalent series resistance of the dc link which has been set to 5 $m\Omega$. The dc link capacitor is split among the two converters, C_{dc} corresponds to 160 μF while its series resistance R_{Cdc} is 5 $m\Omega$.

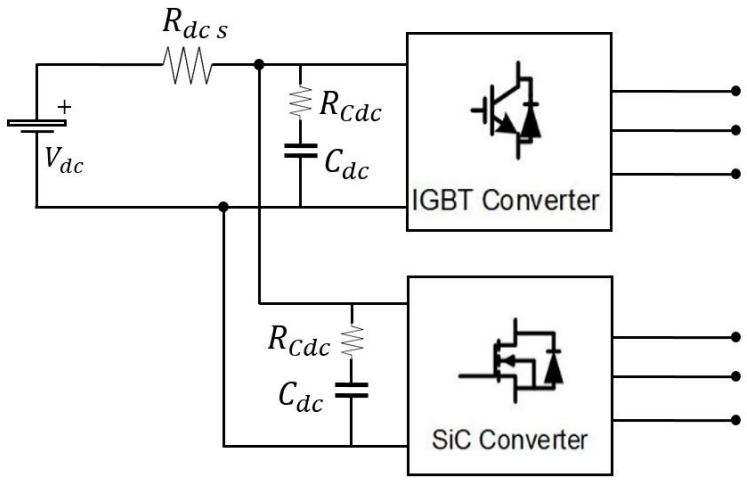


Figure 7.2: dc link modelling for the OEW-PMSM simulation.

Firstly the simulation results for the high speed starter-generator are given, particular attention is given to the steady state operation of the machine. The phase currents profiles, the ZSC and the phase voltages are reported. In simulation it is possible to isolate the effect on the ZSV of the modulation implemented to synthesize the reference voltages for the VSCs and the ZSV contribute of the DTs. The isolation of the two effects on the ZSV allows to better understand how the ZSC distortion affects the machine performance. On the other hand, this is not possible on the experimental rig since for the safety operation of the power modules the DT can never be omitted. In Section 7.4 the simulative results for the scaled-down OEW-PMSM are presented. From the notation point of view, in order to highlight the fact that different power modules have been used, we will refer to VSC A as the IGBT VSC and to VSC B as the SiC VSC. The same change of notation can be found in the voltages.

7.3 High-Speed Starter-Generator OEW-PMSM Numerical Simulation Results

Firstly the simulation results for the high-speed starter-generator are presented. The machine electrical and mechanical parameters are reported in Table 3.2 and the dc link voltage is set to 540 V. The simulative results under both standard PWM and the proposed SVPWM for instantaneous ZSV elimination are shown. The focus is given on the ZSV profile that is applied on the machine by the dual-inverter when the different modulations are used.

7.3.1 Standard PWM Numerical Simulation Results

Since the two converters use different technologies for the power modules, the switching frequencies have been selected to be 10 kHz for the IGBT converter and 40 kHz for the SiC one. The resulting phase current waveforms when a standard PWM is used to control the machine are shown in Fig. 7.3. The high-speed starter-generator is driven by an external load which makes it spin at the reference speed of 4 krpm. A q- axis reference current of 70 A is requested. It can be noticed the high intensity ZSC flowing in the system due to the common dc link connection. The low ZSI in conjunction with the high voltage applied to the machine results in high intensity ZSC ripple which is superimposed on the phase currents. Therefore the operating range of the machine gets significantly limited. The phase currents reach peaks of 115 A when the requested phase current module is 70 A. On top of the third harmonic ZSC flowing due to the non-sinusoidal back-emf of the machine, it can be noticed the high frequency ZSC ripple due to the PWM modulation applied. Fig. 7.4 shows in red the ideal profile of the machine phase current as if the ZSC would be completely eliminated. It is evident how the distortion introduced by the ZSC because of the ZSV applied by the dual-inverter is not acceptable.

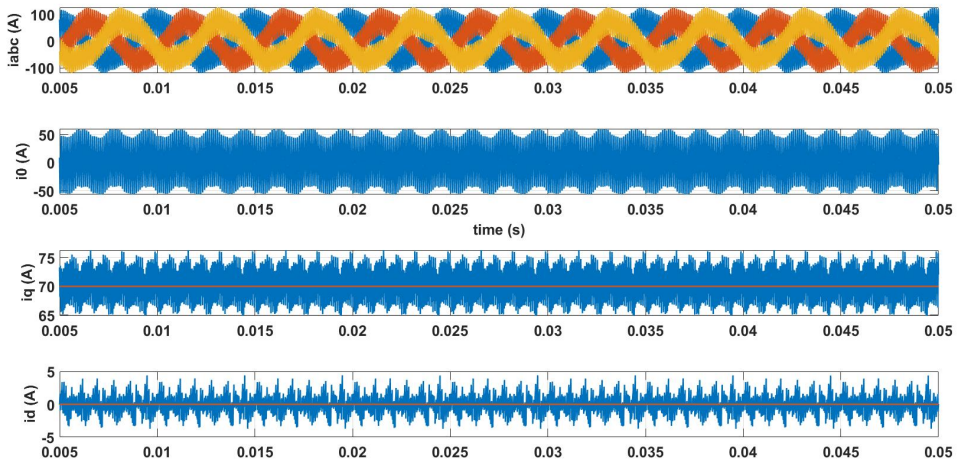


Figure 7.3: High-speed OEW-PMSM performance under standard PWM at 4 krpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

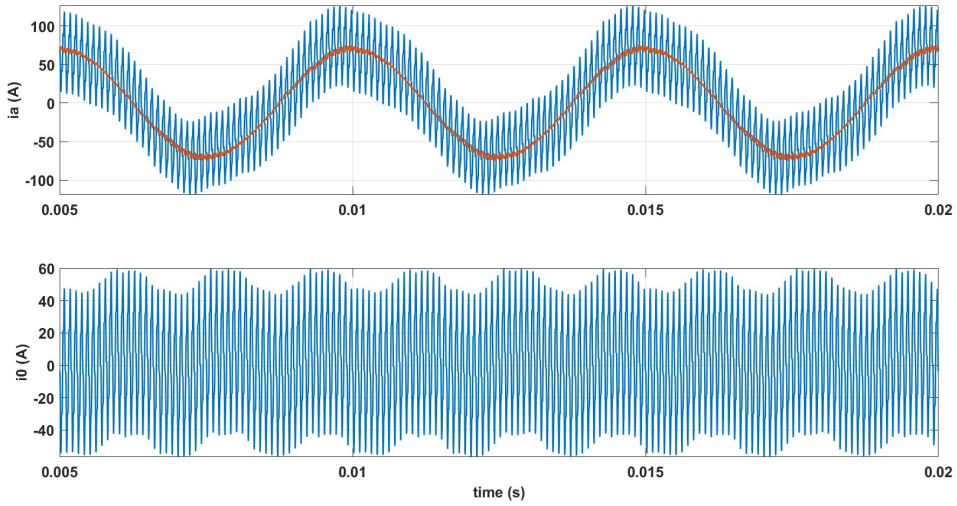


Figure 7.4: Phase current and ZSC profiles for the high-speed OEW-PMSM under standard PWM at 4 krpm. Top: actual i_a phase current (blue) and ideal i_a phase current (red). Bottom: ZSC i_0.

The individual VSCs phase voltage profiles and the resultant ZSVs when standard PWMs are used for both converters are presented in Fig. 7.5. Firstly, it can be noticed how the two VSC switch at different switching frequency, therefore also the resultant ZSVs have significantly different profiles. It can be noticed that since there is no restriction on which voltage vectors can be applied all the ZSV levels are present. This causes the ZSV to assume values that reach the dc link voltage of 540 V. Consequently, high oscillations in the ZSC caused by the ZSV applied to the OEWM are summed to the sinusoidal ZSC flowing due to the third harmonic component of the back-EMF. Fig. 7.6 shows a detail of the ZSV applied to the machine, it is clear how the high oscillations in the ZSV associated with the low ZSI cause the ZSC to oscillate with a peak to peak value of 100 A.

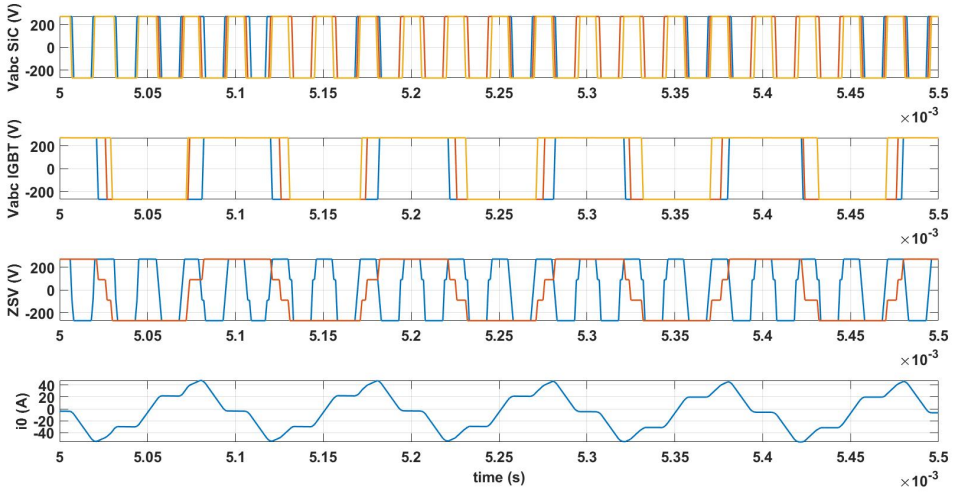


Figure 7.5: Dual-Inverter phase Voltages and ZSVs. Starting from top: V_{abc}^{SiC}, V_{abc}^{IGBT}, V_0^{SiC} (blue) and V_0^{IGBT} (red), ZSC i_0.

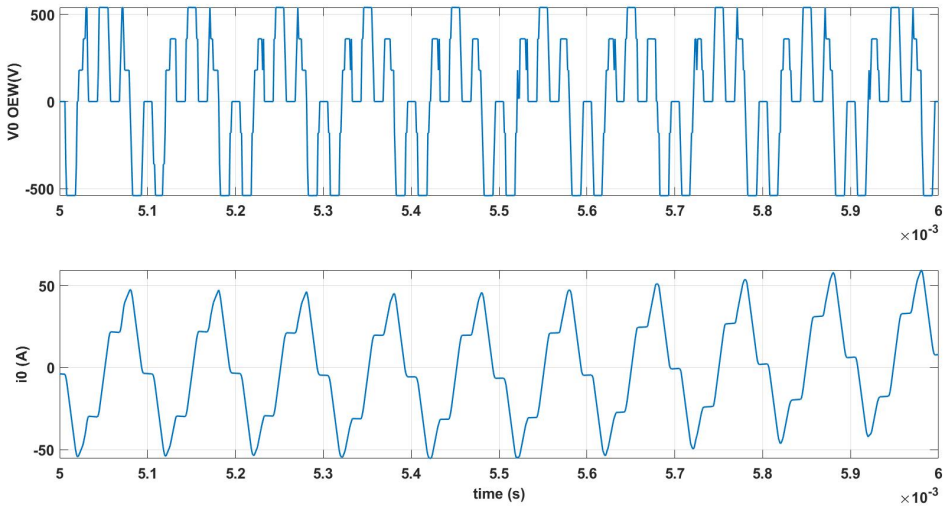


Figure 7.6: Detail of the ZSV applied to the machine and the resulting ZSC. Top: V_0^{OEW} ZSV. Bottom: ZSC i_0.

7.3.2 ZSV Elimination Modulation Numerical Simulations Results

In order to eliminate the ZSV applied by the dual-inverter the modulation proposed in this work is here tested on the OEWM. The SVPWM developed in this work achieves the instantaneous elimination of the ZSV produced by the dual-inverter by square-wave modulating the IGBT converter and synthesizing the necessary voltage with the SiC VSC in order to have the requested sinusoidal voltages on the machine. Only the active voltage vectors that produce the same ZSV introduced by the square-wave modulate IGBT VSC are used to have instantaneously the same ZSV profile. The resulting performance are presented in Fig. 7.7. It can be noticed that the ZSC flowing is not a pure sinusoidal current, in fact the zero-sequence voltage distortion introduced by the DT causes an additional ZSV which changes the total ZSV applied to the zero-sequence circuit. The voltage reference signals for the individual VSCs

are shown in Fig. 7.8 while the VSCs phase voltages and the corresponding ZSV are presented in Fig. 7.9. It can be noticed how the IGBT converter is switching at the same fundamental frequency of rotation of the machine while the SiC VSC is fast switching to compensate for the harmonic distortion introduced by the square-wave modulated converter. The ZSV profile of the IGBT converter is a square wave of amplitude $\frac{V_{dc}}{6}$ and three times the fundamental frequency. Similarly the ZSV produced by the fast switching SiC VSC has also the same profile since the space voltage vectors used to synthesize the reference voltage vector have been chosen in order to have instantaneously the same ZSV of the slow switching IGBT VSC.

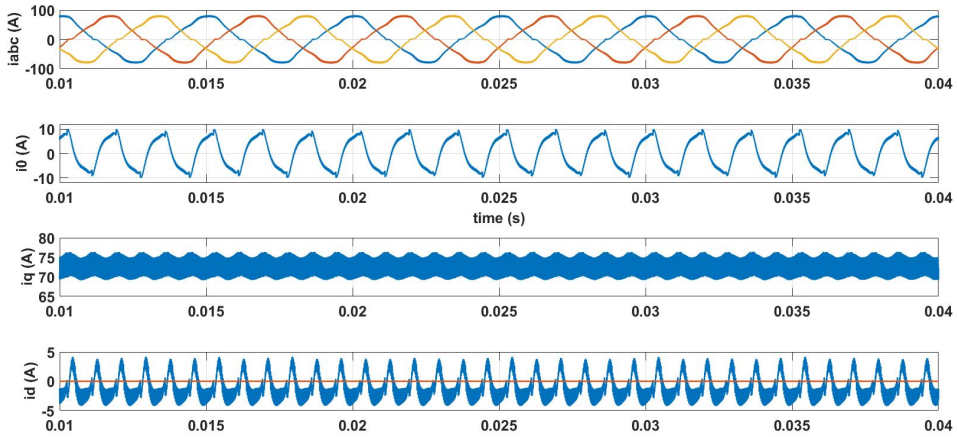


Figure 7.7: Phase current and ZSC profiles for the high-speed OEW-PMSM under ZSV elimination SVPWM at 4 krpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

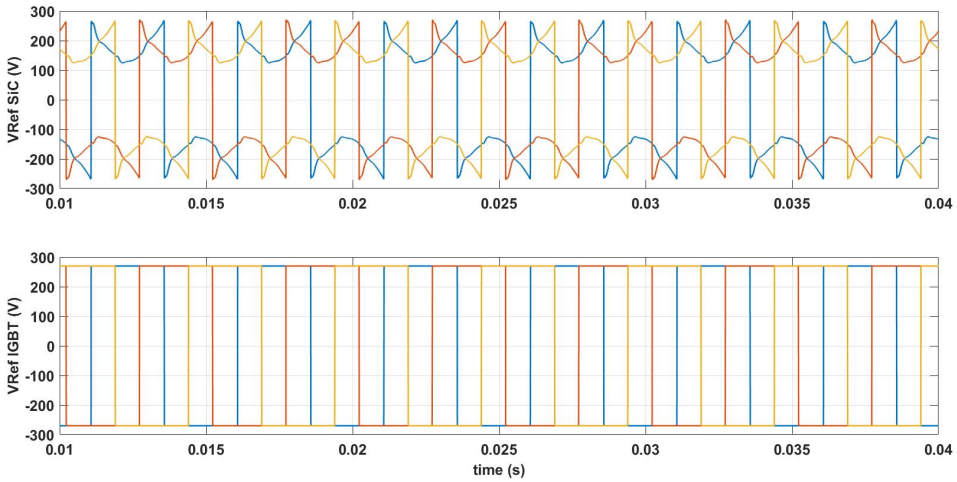


Figure 7.8: Dual-Inverter Reference Voltages. Top: $\overline{V}^{*}_{SiC}$. Bottom: $\overline{V}^{*SW}_{IGBT}$.

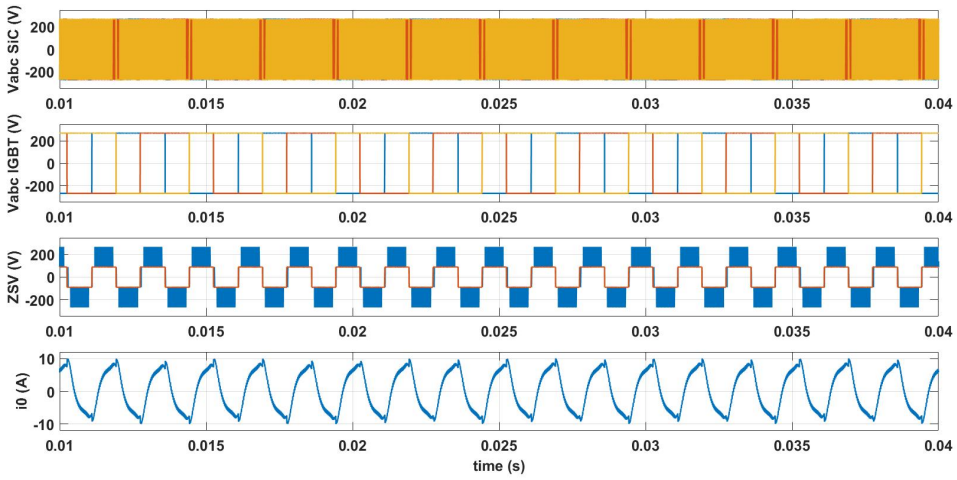


Figure 7.9: Dual-Inverter phase Voltages and ZSVs. Starting from top: V^{SiC}_{abc}, V^{IGBT}_{abc}, V^{SiC}_{0} (blue) and V^{IGBT}_{0} (red), ZSC i_0.

A detail of the ZSV applied on the machine is shown in Fig. 7.10. The only ZSV applied is the one caused by the voltage distortion introduced by the DT. In fact the ZSV applied is either 0 or $\pm\frac{V_{dc}}{3}$. Furthermore it can be noticed that when the phase

current is clamped to zero, during the zero crossing, the voltage distortion introduced by the DT is not present.

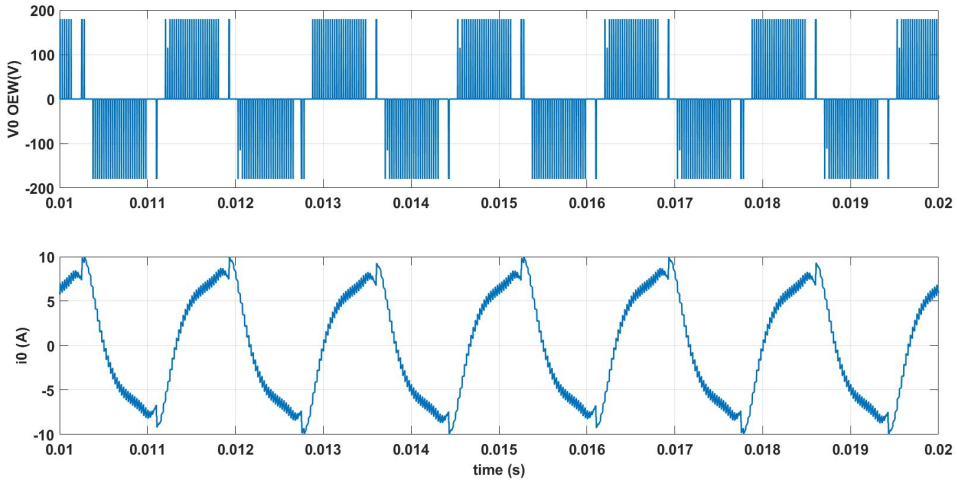


Figure 7.10: Detail of the ZSV applied to the machine and the resulting ZSC. Top: V_0^{OEW} ZSV. Bottom: ZSC i_0.

The SVPWM proposed allows for a significant reduction of the ZSC flowing in the system. In particular the ZSV produced by the two converter is eliminated, leaving exclusively the ZSV distortion introduced by the DT. The ZSC flowing is still not acceptable since its circulation is responsible for a reduction of the system efficiency and additional torque ripple. The simulation analysis of the proposed DT hysteresis controller performance are now presented to show the effectiveness of this method to eliminate the remaining ZSC flowing due to the third harmonic back-EMF of the machine.

7.3.3 DT Hysteresis Controller Numerical Simulations Results

The performance of the proposed DT hysteresis controller described in Chapter 5 are here tested in simulation for the high-speed OEWM. Fig. 7.11 shows the abc and qd0 current profiles when the DT hysteresis controller is used to suppress the ZSC flowing because of the non-sinusoidal machine back-EMF. The machine is spinning at 4 krpm while the q- axis reference current is changed from 100 A to 25 A. Meanwhile the ZSC DT controller hysteresis band is changed from 5 A to 0 A and finally to 4 A to show the effectiveness of the proposed method in controlling the additional flow of unwanted ZSC. The steady state performance of the machine when is spinning at 10 krpm and the ZSC is suppressed thanks to the proposed controller are shown in Fig. 7.12.

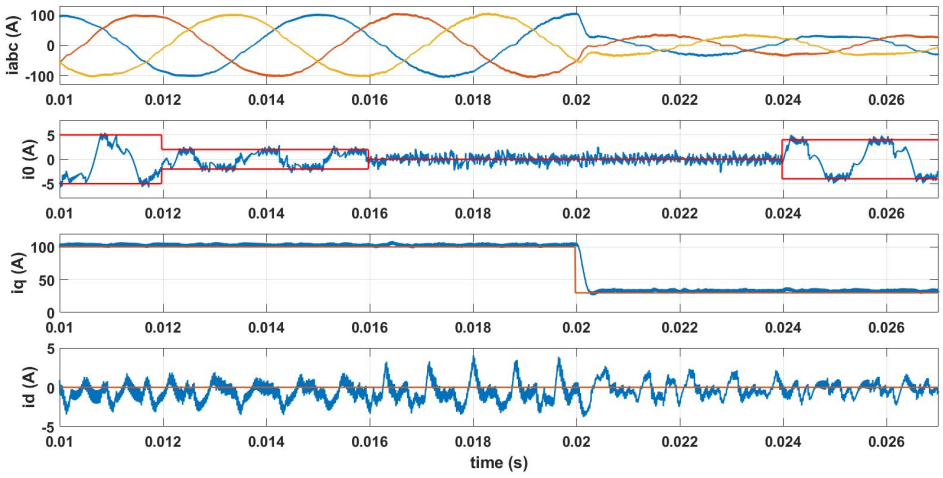


Figure 7.11: Phase current and ZSC profiles for the high-speed OEW-PMSM with the DT hysteresis at 4 krpm. Starting from the top: phase currents, ZSC i_0 (blue) and i_0 hysteresis band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

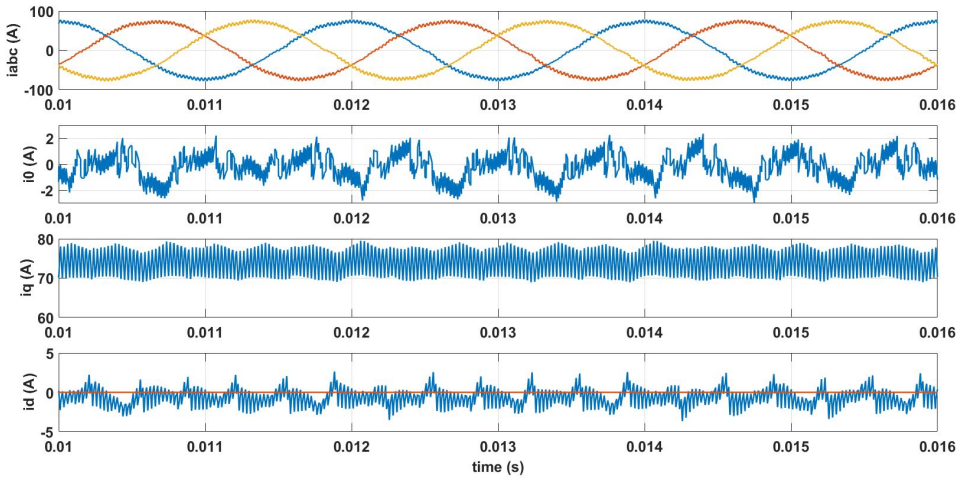


Figure 7.12: Phase current and ZSC profiles for the high-speed OEW-PMSM with the DT hysteresis at 10 krpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue), d axis current i_d (blue) and reference current i_d^* current (red).

A detail of the machine i_a phase current at 10 krpm when the ZSC has been eliminated is shown in Fig. 7.13. The actual phase current is shown in blue while the ideal phase current in red, where with ideal is intended the phase current subtracted of the additional ZSC flowing in the system. It can be seen how thanks to the proposed method the real and ideal phase currents are almost identical. The individual VSCs voltages and the corresponding ZSVs applied to the machine are shown in Fig. 7.14. The DT voltage distortion is accurately introduced on the SiC converter to control the ZSC to zero while the IGBT converter is modulated in six-step mode. Fig. 7.15 shows a detail of the ZSV applied to the machine by the dual-inverter when the proposed modulation in combination with the DT hysteresis controller are used. The i_0 band has been set to 4 A. It can be noticed how the DT voltage distortion is introduced exclusively when the ZSC goes beyond the ZSC hysteresis band limits to push it back inside the desired range. It can be noticed how, even when the ZSC hysteresis band is set to 0 A ripple of 4 A is still present, this is inevitable given the ZSI of the machine.

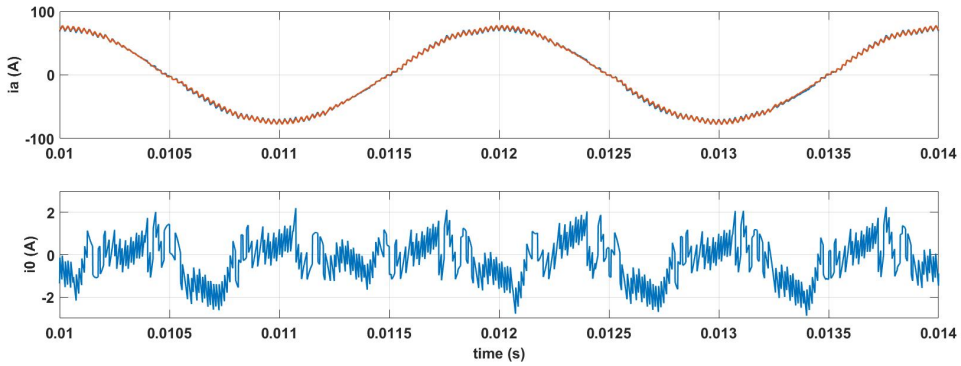


Figure 7.13: Phase current and ZSC profiles for the high-speed OEW-PMSM with the DT hysteresis controller at 10 krpm. Top: actual i_a phase current (blue) and ideal i_a phase current (red). Bottom: ZSC i_0.

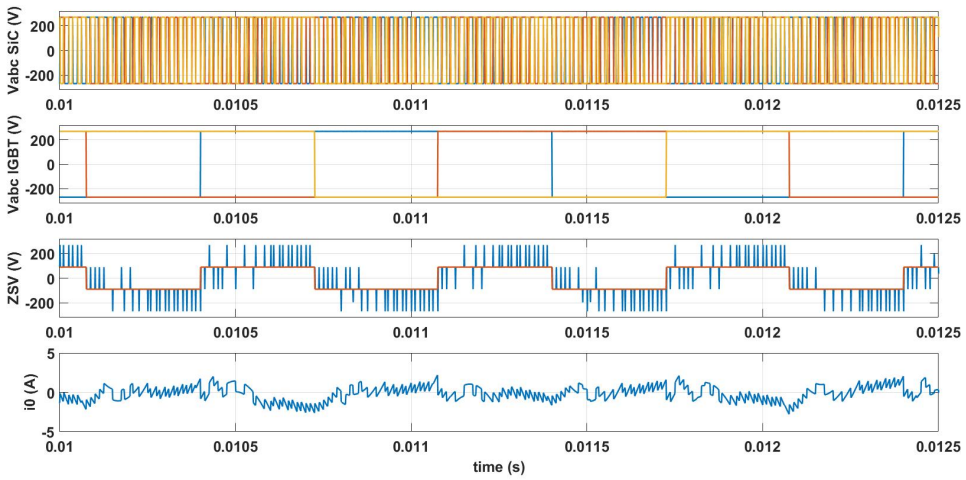


Figure 7.14: Dual-Inverter phase Voltages and ZSVs. Starting from top: V_{abc}^{SiC}, V_{abc}^{IGBT}, V_0^{SiC} (blue) and V_0^{IGBT} (red), ZSC i_0.

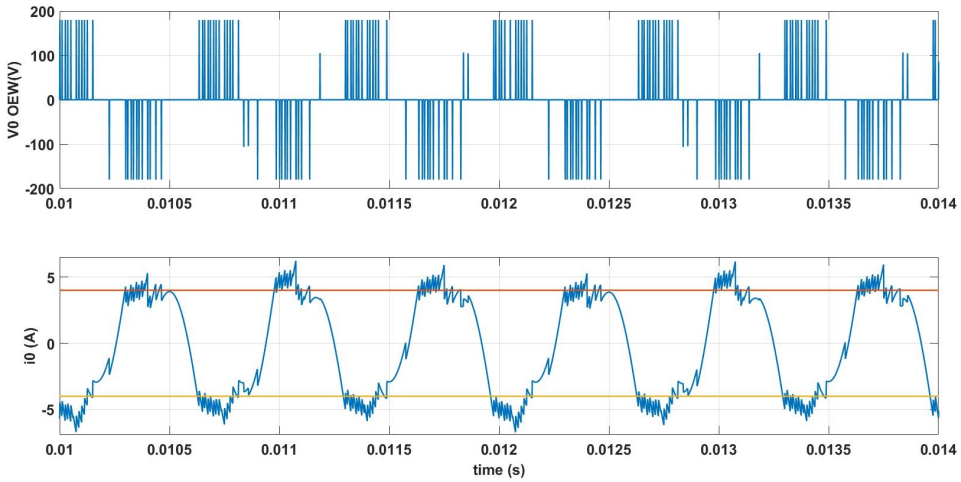


Figure 7.15: Phase current and ZSC profiles for the high-speed OEW-PMSM under standard PWM at 4 krpm. Top: actual i_a phase current (blue) and ideal i_a phase current (red). Bottom: ZSC i_0.

7.4 Scaled-down OEW-PMSM Numerical Simulation Results

At the moment of the experimental testing the high-speed OEWM was still not available, therefore another machine to test the proposed modulation and controller had to be found. The scaled-down OEW-PMSM used for the initial experimental tests is the one reported in Tables 3.2 and 3.3. Here the numerical simulation results for the scaled-down motor are reported in order to have a reference of comparison with the experimental results that will be shown later in this manuscript. As it has been done for the high-speed OEWM the performance of the system under standard PWM, with th proposed modulation and with the DT hysteresis controller are evaluated. The dc link voltage has been chosen to be 100 V, which is high enough to allow to run the machine at the rated speed without going in flux weakening mode.

7.4.1 Standard PWM Numerical Simulation Results

Fig. 7.16 shows the abc and qd0 current profiles under the standard PWM at 1000 rpm. VSC A is switched at 10 kHz while VSC B at 40 kHz. It can be noticed that the ZSC is characterized by an high frequency ripple due to the ZSV introduced by the pulse-width modulated dual-inverter. The additional ZSC flowing is not acceptable since it causes a significant reduction in the system efficiency and increases the phase currents THD. From Fig. 7.17 it is evident how the ideal phase current, i.e. the one that would circulate if the ZSC would be zero would have a much better profile. Fig. 7.18 shows the phase voltages of the two VSCs and the resultant ZSVs. It can be noticed that the profiles are exactly the same that were obtained for the high-speed OEW-PMSM. The resultant ZSV on the machine is obtained subtracting the ZSC produced by VSC B V_0^B to the one generated by VSC A V_0^A. A detail of the resultant ZSV is shown in Fig. 7.19, the ZSV ranges from -V_{dc} to V_{dc} causing an intense variation of the ZSC because of the low ZSI.

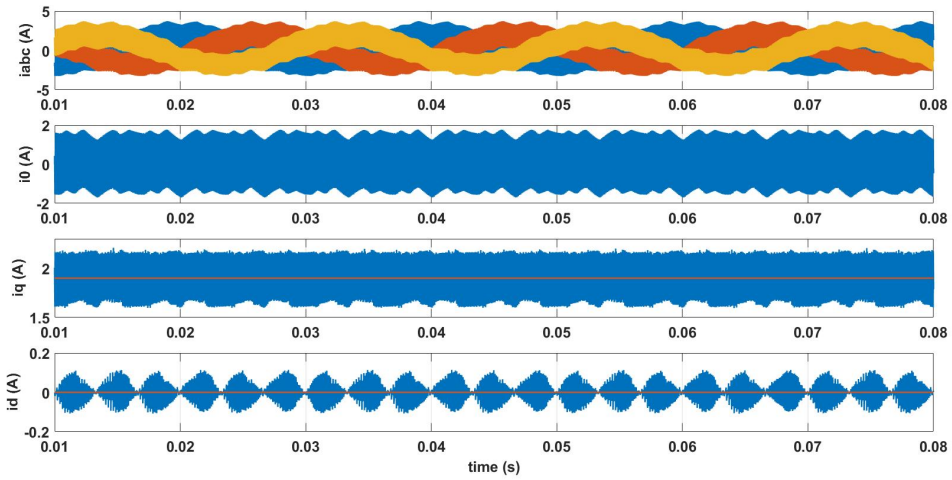


Figure 7.16: Scaled-down OEW-PMSM performance under standard PWM at 1 krpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

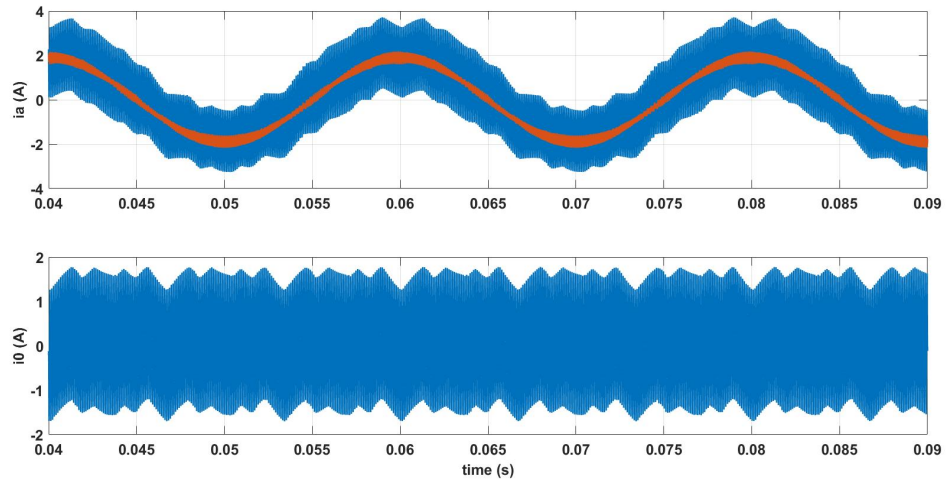


Figure 7.17: Phase current and ZSC profiles for the scaled-down OEW-PMSM under standard PWM at 1 krpm. Top: actual i_a phase current (blue) and ideal i_a phase current (red). Bottom: ZSC i_0.

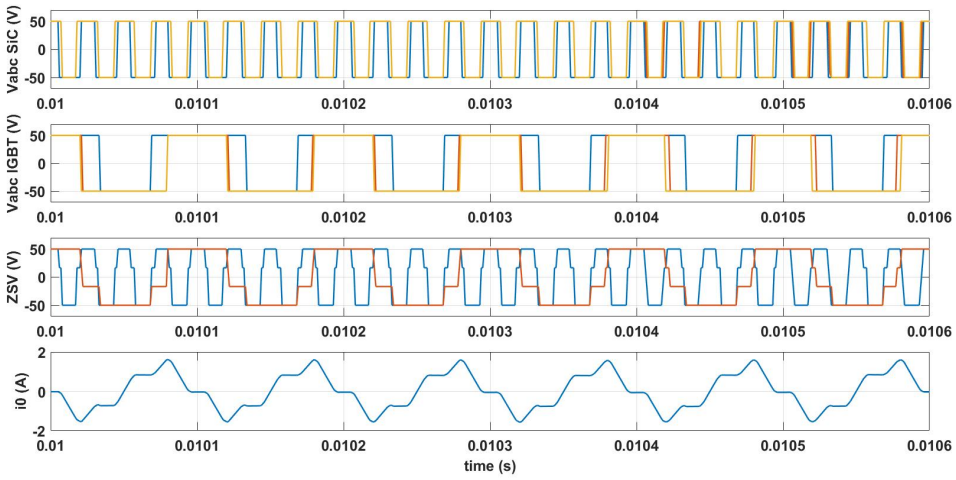


Figure 7.18: Dual-Inverter phase Voltages and ZSVs. Starting from top: V_{abc}^{SiC}, V_{abc}^{IGBT}, V_0^{SiC} (blue) and V_0^{IGBT} (red), ZSC i_0.

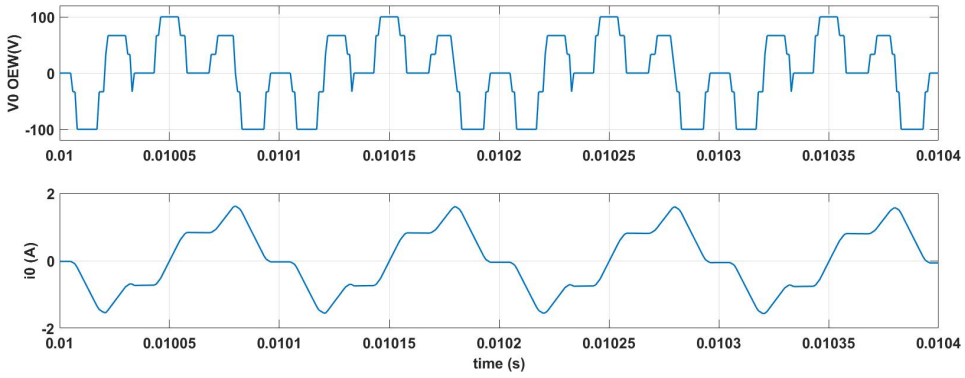


Figure 7.19: Detail of the ZSV applied to the machine and the resulting ZSC. Top: V_0^{OEW} ZSV. Bottom: ZSC i_0.

7.4.2 ZSV Elimination Modulation Numerical Simulations Results

Similarly as it has been done in Section 7.3.2, the performance of the machine under the proposed SVPWM for the ZSV instantaneous elimination are here presented for the scaled-down OEW-PMSM. Fig. 7.20 and 7.21 show the phase currents profiles at 500 rpm and 1000 rpm respectively. In both cases it can be seen the third harmonic ZSC flowing due to the machine non-sinusoidal back-EMF. The ZSC profile is not purely sinusoidal since the ZSV distortion introduced by the DT affects it. The real and ideal profile, as if the ZSC would be zero, of the phase current are shown in Fig. 7.22. The phase voltages applied by the VSCs are shown in Fig. 7.23, thanks to the proposed modulation, apart from the ZSV distortion introduced by the DT the ZSVs profiles of the two VSCs are identical.

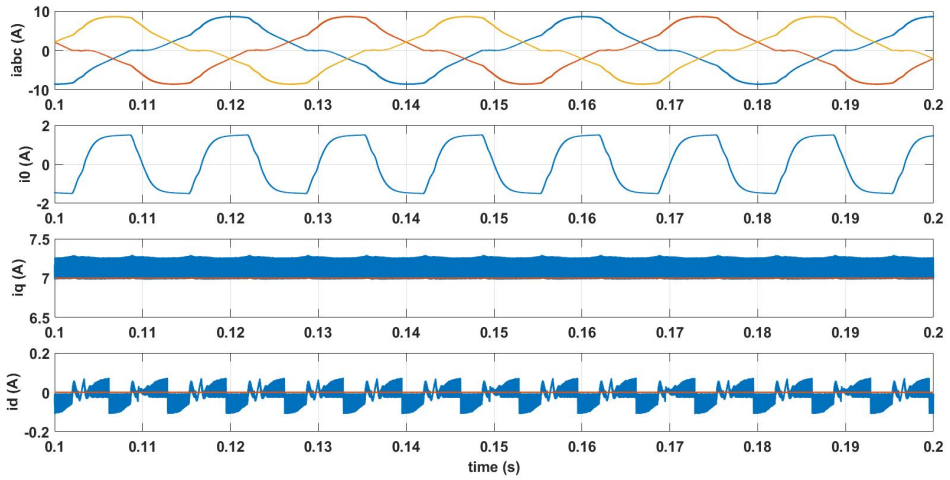


Figure 7.20: High-speed OEW-PMSM performance under standard PWM at 4 krpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

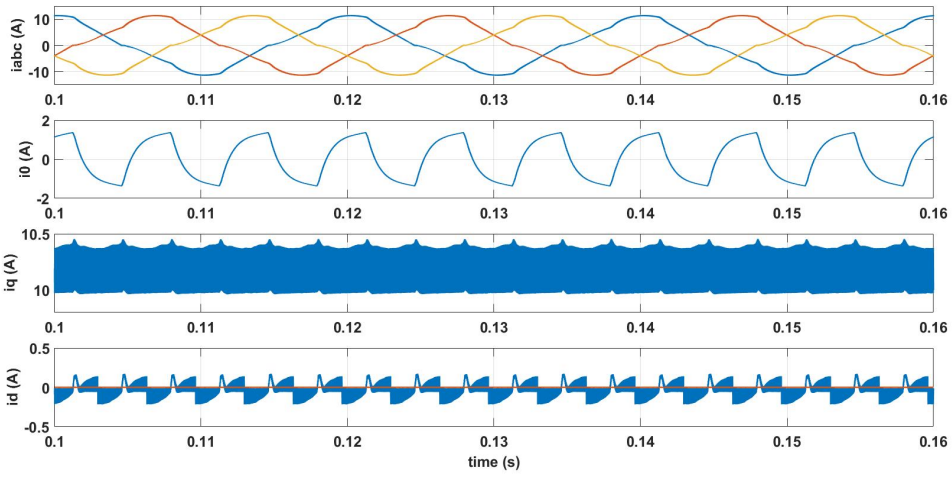


Figure 7.21: High-speed OEW-PMSM performance under standard PWM at 4 krpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

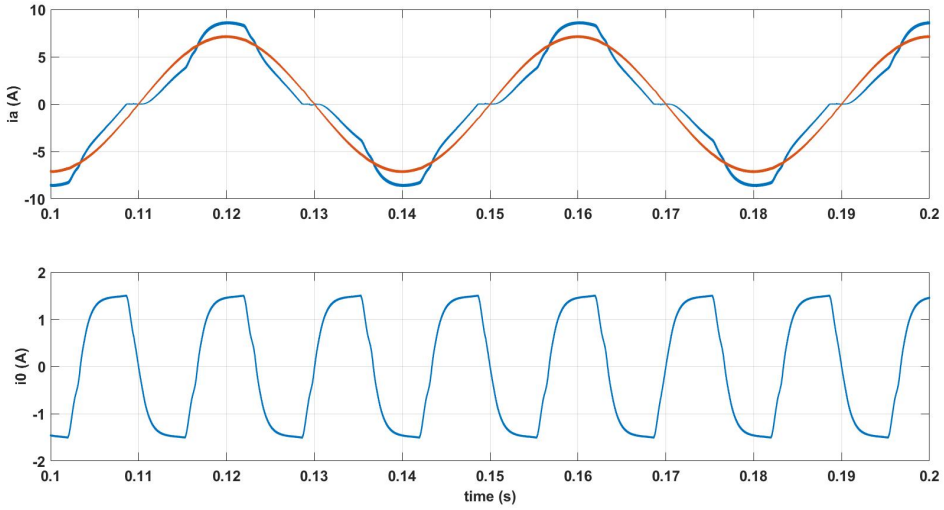


Figure 7.22: Phase current and ZSC profiles for the high-speed OEW-PMSM under standard PWM at 4 krpm. Top: actual i_a phase current (blue) and ideal i_a phase current (red). Bottom: ZSC i_0.

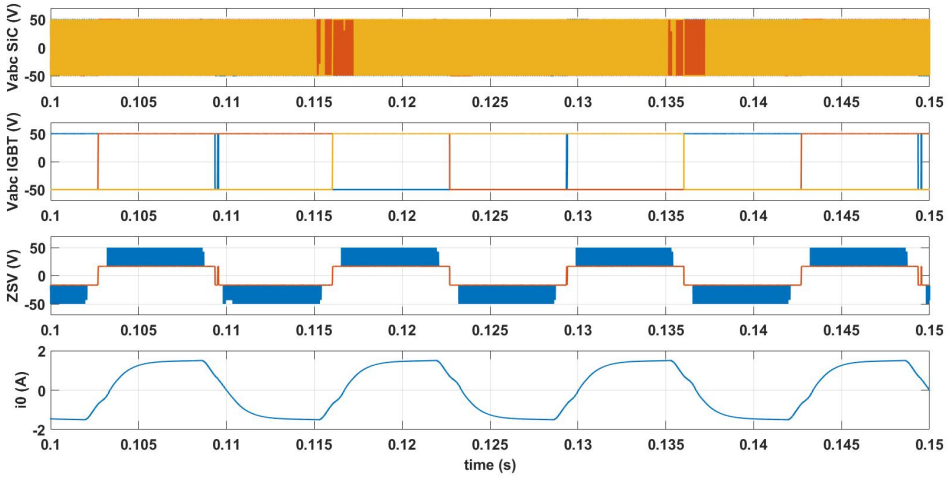


Figure 7.23: Dual-Inverter phase Voltages and ZSVs. Starting from top: V_{abc}^{SiC}, V_{abc}^{IGBT}, V_0^{SiC} (blue) and V_0^{IGBT} (red), ZSC i_0.

7.4.3 DT Hysteresis Controller Numerical Simulations Results

The performance of the proposed DT hysteresis controller applied to the scaled-down OEW-PMSM are here presented. The performance of the ZSV elimination modulation in conjunction with the ZSC controller at the rated speed are presented in Fig. 7.24 and Fig. 7.25. Fig. 7.24 shows the abc and qd0 current profiles at steady state when the DT hysteresis controller is used to suppress the ZSC flowing because of the non-sinusoidal machine back-EMF. The ZSC is completely eliminated significantly improving the phase currents profiles. In Fig. 7.25 two ZSC hysteresis band steps are performed. the first one from 0.5 A to 0.1, and the second from 0.1 to 0 A. The band limits can be changed from the controller even though for the best system performance the band wants to be kept at 0 A. Furthermore it can be noticed that the control of the ZSC is basically instantaneous. In fact the control action, i.e. the voltage introduced by the DT, is applied as soon as there is a voltage space vector commutation on the SiC VSC. All the simulation results presented for the scaled-down OEW-PMSM show the same behaviour of the one obtained for the actual high-speed machine but on a smaller scale.

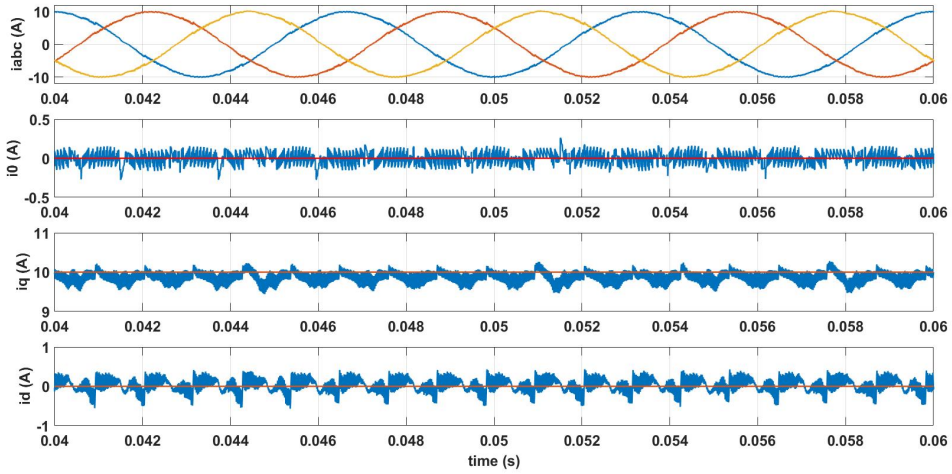


Figure 7.24: Scaled-down OEW-PMSM performance under standard PWM at 3 krpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

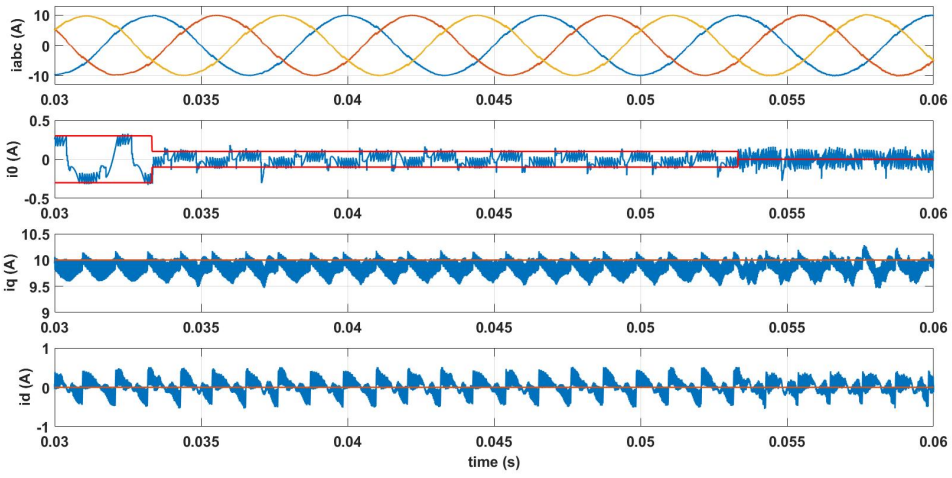


Figure 7.25: Scaled-down OEW-PMSM performance under standard PWM at 3 krpm. ZSC hysteresis band transient. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

7.5 Conclusions

In this Chapter, the performance of the proposed SVPWM for the instantaneous elimination of the ZSV generated by the dual-inverter, which was described in Chapter 4, are presented. Furthermore the effectiveness of the novel DT hysteresis controller of Chapter 5 is tested. Firstly the structure of the simulation developed in the Simulink environment has been shown. Then the results for both the high-speed starter-generator and the scaled-down OEWM have been presented. The standard PWM has been used to synthesize the reference voltage vectors for both VSCs showing how the resultant ZSV is not acceptable, in fact it oscillates between plus and minus the dc link voltage. The resultant ZSC for the high-speed OEWM has a ripple of more or less 100 A, therefore being not acceptable for the operation of the system. One third of the high frequency ZSC is summed to all the three phase currents leading to the reduction of the maximum effective current that is allowed. The proposed SVPWM shows to be able to significantly reduce the ZSV, both VSCs generate the same ZSV profile leading to a resultant zero ZSV applied on the machine. Furthermore the DT hysteresis controller is tested for different operating points of the machine showing its effectiveness in eliminating the ZSC flowing because of the non-sinusoidal machine back-EMF. The same results, but on a smaller scale, are obtained when the PWM, the proposed modulation and the DT hysteresis controller are tested on the scaled-down OEW-PMSM.

Chapter 8

Experimental Results

8.1 Introduction

This Chapter presents the experimental validation of the proposed SVPWM for the instantaneous elimination of the ZSV produced by the dual-inverter feeding the OEW-PMSM. Both the scaled-down 1.5 kW OEWM and the high-speed starter-generator have been tested. The individual elements that compose the experimental set-up are described. Then the machine electrical and mechanical parameters have been identified. The performance of the PMSM are tested under both standard PWM and the proposed SVPWM through THD and FFT analysis. The novel DT hysteresis controller is also tested on the experimental rig to verify its effectiveness in eliminating the ZSC flowing due to the third harmonic back-EMF of the machine. Particular attention is given to the VSCs phase voltages profiles and resultant ZSVs to show the ability of the proposed modulation to eliminate the ZSV produced by the dual-inverter.

8.2 Experimental Rig Description

The experimental rig used to verify the work of this thesis is presented in Fig. 8.1.



Figure 8.1: Experimental set-up: Mixed technology IGBT-SiC common dc link VSC (white rectangle), control board (orange rectangle), chiller for liquid cooling of VSCs (yellow rectangle) and OEW-PMSM (blue rectangle)

A LAB-HP 15600 15 kW, 25 A and 600 V dc power supply is used to feed the power

converters dc link. The dual-inverter feeds the OEW-PMSM, which is mechanically connected to a dc motor that acts as a load for the PMSM. In the following Sections additional detail of the elements that compose the rig are given.

8.2.1 Dual-Inverter

The dual-inverter topology uses both Si and SiC based power modules arranged in a back-to-back structure: one Si-based 3ph full-bridge converter and one SiC-based 3ph full-bridge are connected across the same dc link. As described in Chapter 4, the IGBT converter is operated at the machine fundamental frequency, while the SiC converter provides for the conventional switching. Using this arrangement it is possible to reduce the IGBTs switching losses and still granting a reduced current THD and a high efficiency. Figure 8.2 shows the prototype converter, which has been designed by Dr. Giovanni Lo Calzo during his PhD [34]. The dual-inverter is based on two sub-units: the first built around the R-OHM Semiconductors 1200V 180A BSM180D12P2C101 SiC power module [142] and the second built around the Infineon FF400R12KT3 IGBT power module [143]. The maximum current considered for the design of the converter was 170A. This was in order to allow for flux weakening operation above the nominal speed of 20 krpm. The dc link capacitance is split across the two sub-units and it sums up to 320μF. The cooling system of the converter is a single liquid cooled heat-sink for the two sub-units in order to reduce both volume and weight of the complete PGU, furthermore it is able to handle up to 3 kW of losses, with a flow rate of just 8 liters per minute and a temperature difference between the coolant and the surface of the cold plate of 24^oC.

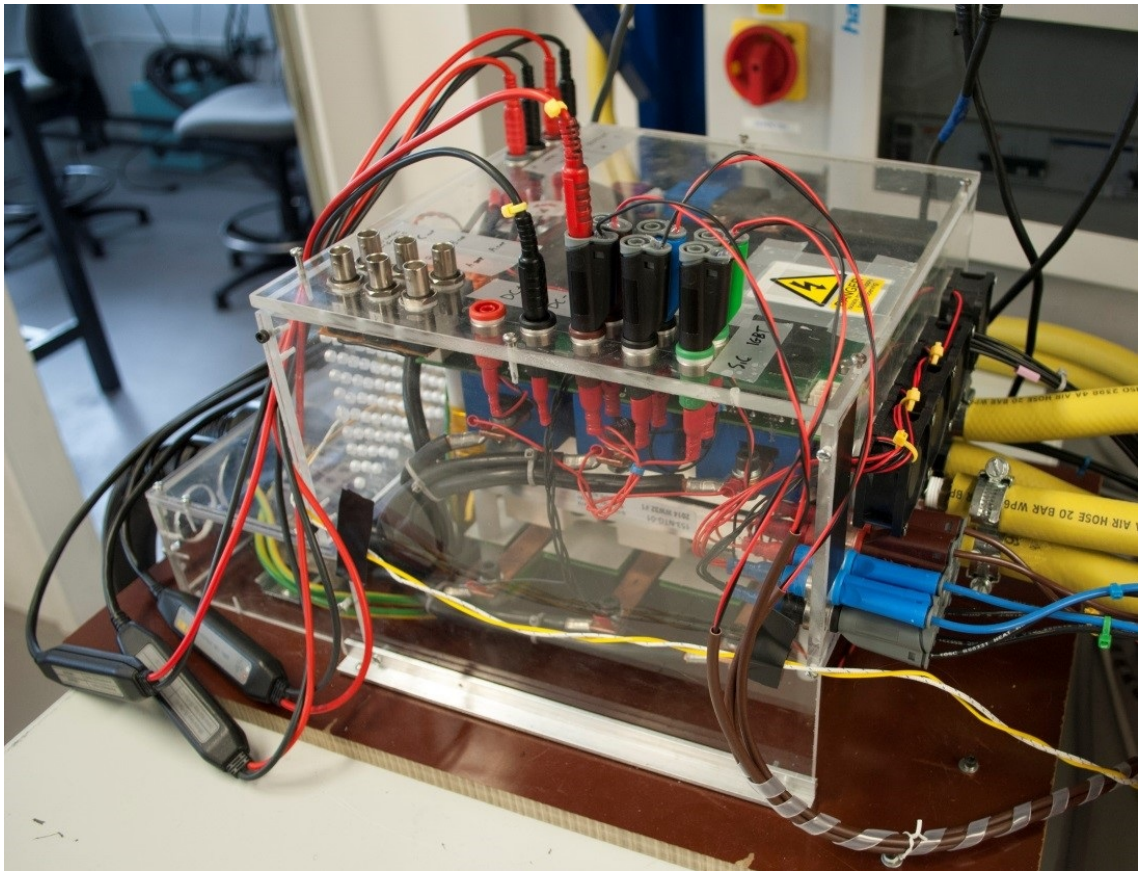
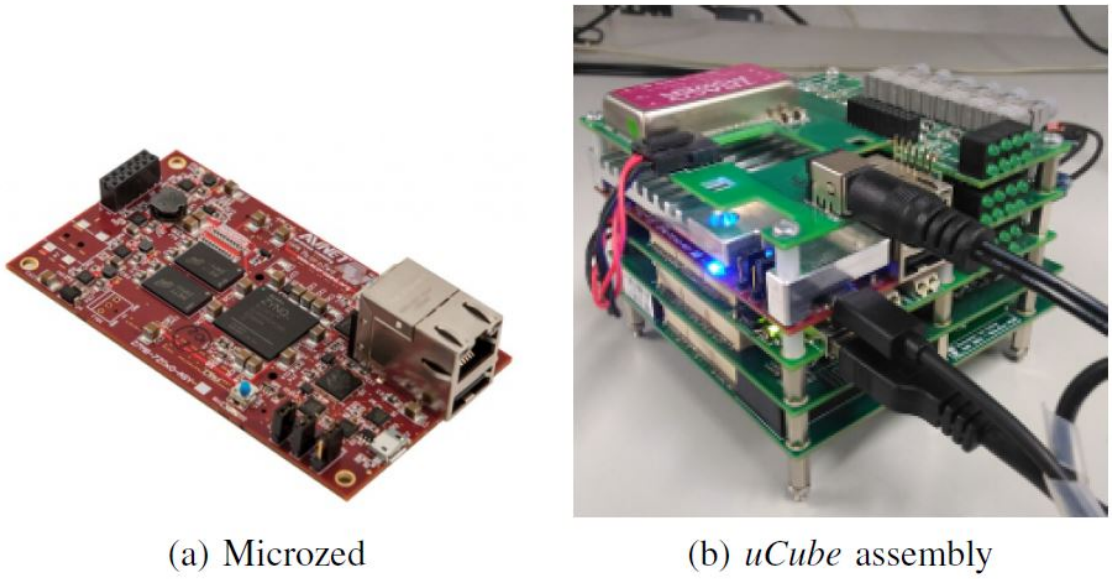


Figure 8.2: The single dc link dual-inverter with mixed technology

8.2.2 Control Platform

The custom made control platform (uCube) shown in Figure 8.3 b) has been designed by Dr. Giovanni Lo Calzo, Dr. Adrea Formentini and Dr. Alessandro Galassini. Fig. 8.3 a) shows the low-cost development board based on the Xilinx Zynq-7000 All Programmable SoC [144], on which the uCube platform is been based on. The Zynq integrates in a single device a dual-core ARM CortexA9 based Processing System (PS) and a FPGA Programmable Logic (PL) [144]. The uCube board has been used in many research works, in particular in [145] the high calculation performance of the board have been used to implement an oversampled model based controller in

the FPGA in order to eliminate the calculation delays associated with the use of a conventional micro-processor and to increase the system robustness to parameters variation.



(a) Microzed (b) *uCube* assembly

Figure 8.3: The Avnet Microzed board (a) and the uCube control board (b)

The FPGA deals with some of the standard functionalities that are necessary to control the VSCs such as the acquisition of the phase currents, dc link voltage, implementation of the modulators and DT logics and fault thresholds setting. Furthermore also the ZSC controller described in Chapter 5 has been implemented. In fact the ZSC is characterized by high frequency dynamics, which to be observed require an high frequency sampling. The DSP speed and current controller runs at 25 μs, which happens to be too slow to be used to implement the DT hysteresis controller. The overall controller structure is therefore characterized by a tight interaction between the DSP and FPGA controllers which will be explained in detail in Section 8.4.

8.2.3 Electrical Parameters Identification

In Chapter 3 the electrical model of the OEW-PMSM was given as well as the electrical parameters of both the high-speed starter generator and the OEW which has been used to experimentally verify the proposed modulation and ZSC control technique. The high speed starter generator initially was not available, therefore the tests have been firstly carried out on another OEW machine. Only later the high-speed machine was available and tested in a dedicated high-speed room in the University of Nottingham facilities. In this section the electrical machine parameters identification procedure is given. Considering the electrical model of the machine given in Chapter 3 the back EMF and machine inductances are calculated thanks to the experimental measurement carried out.

8.2.3.1 Back-EMF

The machine fundamental λ_m and third harmonic component $\lambda_m k_{3\lambda}$ of the permanent magnet flux have been obtained by driving the machine at various rotational speed (within the machine operating range) by means of an external load and measuring the voltage between consecutive phases with an oscilloscope. Fig. 8.4 presents the experimental line to line back-EMF waveforms of the OEW-PMSM at the motor speed of 666.6 rpm.

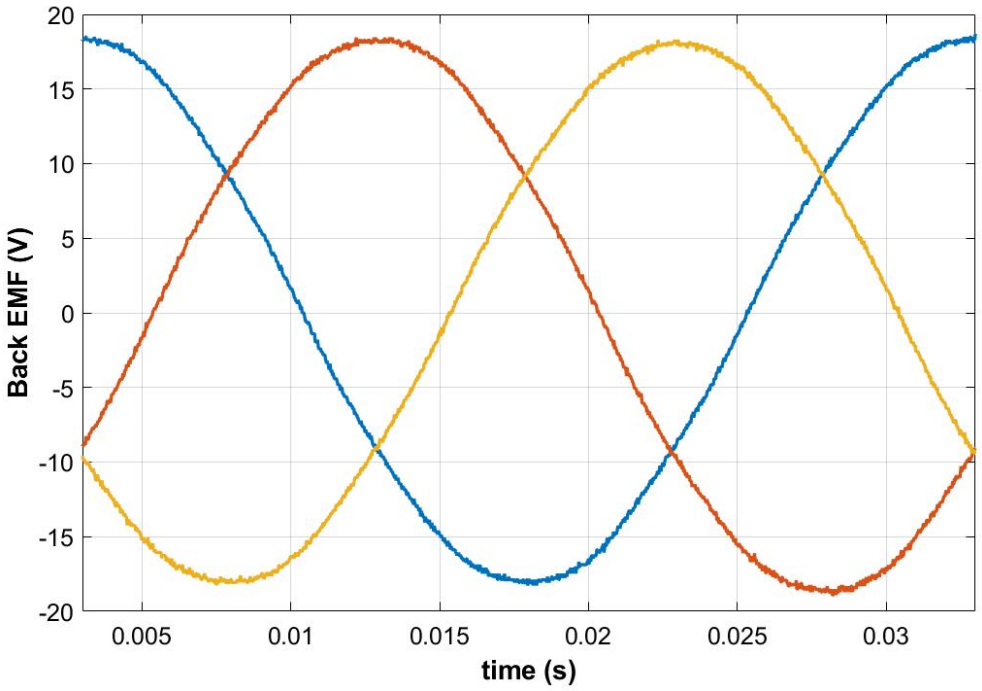


Figure 8.4: Experimental line to line back-EMF waveforms of the three sectors of the PMSM motor at 666.6 rpm.

Fig. 8.5 shows the harmonic spectrum of the experimental waveform of the back-EMF of one motor phase. The fundamental and third harmonic voltage values obtained are used to analytically determine the fundamental and third harmonic flux of the machine as shown in (8.1).

$$\begin{cases} \lambda_m = \frac{V_{BEMF}}{2\pi f_0} \\ \lambda_{3m} = \frac{V_{3BEMF}}{2\pi 3 f_0} \end{cases} \tag{8.1}$$

where, according to the fft results shown in Fig. 8.5 V_{BEMF}, V_{3BEMF} and f_0 are 18.15 V, 0.1063 V and 33.27 Hz respectively. The constant $k_{3\lambda}$ obtained is 0.0017904235, which has been calculated as the ratio between λ_{3m} and λ_m.

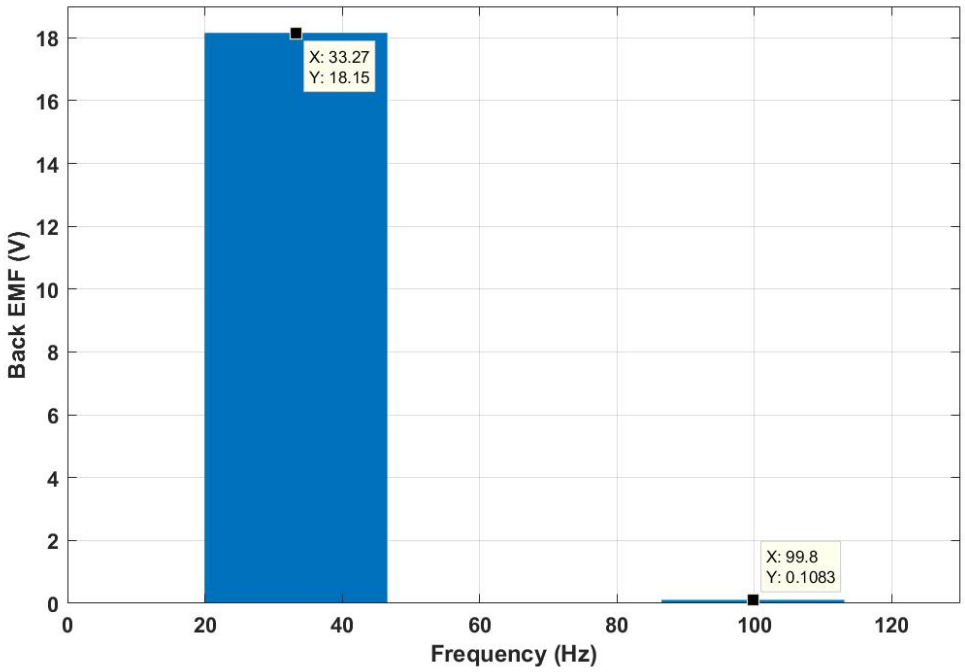


Figure 8.5: Harmonic spectrum of the measured back-EMF of phase b.

8.2.3.2 Machine Inductance Estimation

The machine inductances have been experimentally identified using the Least Square Estimate method as reported in [146]. The system considered is the first order differential equation represented by the RL equivalent circuit of the q and d axes. The control loop considered is shown in Fig. 8.6.

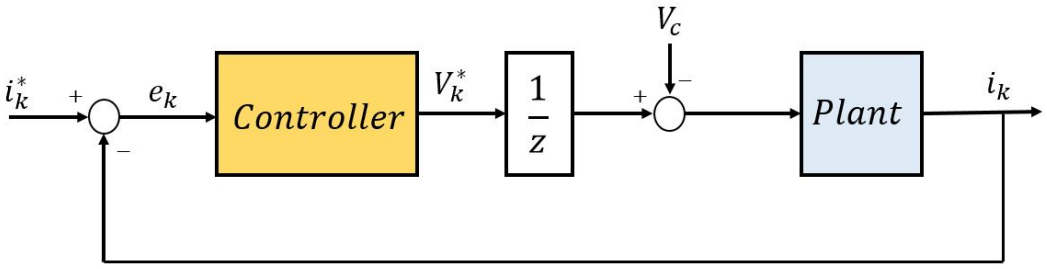


Figure 8.6: Block diagram of the system considered for the electrical parameters identification.

The delay of application due to the finite time of calculation required by the micro controller has been taken into account since the electrical system time constant is comparable to the controller sample time. The discretized form of the RL circuit is reported in (8.2).

$$V_{k-1}^* = L\frac{i_{k-1} - i_k}{T_s} + R_s i_k + V_c \tag{8.2}$$

(8.2) can then be rearranged obtaining

$$i_{k+1} = i_k + V_{k-1}^*\frac{T_s}{L} - \frac{R_s T_s}{L} i_k - V_c\frac{T_s}{L} \tag{8.3}$$

Considering to have the vector of measurements i_k and V_k^*, using the Least Square Estimate method R, L and Vc are identified. The experimental identification of L_d was carried out performing a closed loop current control and recording input and output values of the system: $d-$axis reference voltage V_k^* and current i_{dk}. In a post-processing stage, the least square estimation technique has been employed to identify the unknown parameters of the system such as the phase resistance R_s, the inductance L_d and constant voltage drop on the switches and diodes V_c. The reference i_d current requested has been chosen to be a square wave of frequency 200 Hz and with amplitude

ranging from 3 to 1 A. Figure 8.7 shows the comparison between the actual i_d current and the simulated $i_{d,sim}$ one obtained using the known analytical model of the system, the measured voltage and the parameters obtained by using the least square method. It can be noticed that the output $i_{d,sim}$ of system (8.3) matches the real current output i_d meaning that, in a good approximation, the identified parameters can be considered correct. In Fig. 8.7 the x-axis is given in number of samples, in order to have it in seconds it is necessary to multiply the number of samples times the sampling frequency of 50 μs. The least square estimate identification gave as output 0.8434 Ohm, 1.35 mH and 2.72 V for R_s, L_d and V_c, respectively.

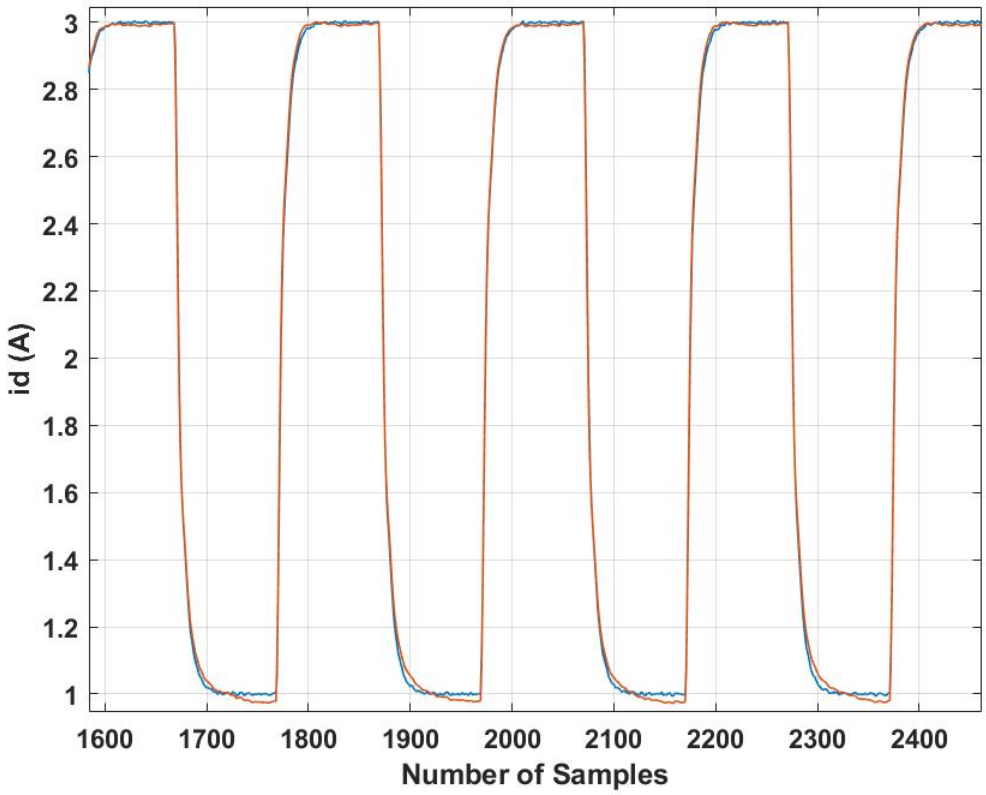


Figure 8.7: Comparison between the measured current i_d (blue) and the output of the simulated system $i_{d,sim}$ (red).

The inductance L_q was not experimentally identified since a mechanical clamp or a load motor controlled in position would have been necessary to avoid the rotor to start spinning when the $q-$ axis current was supplied to the winding. At that time they were not available, hence only the L_d inductance could be experimentally identified. Since the machine does not show any significant anisotropy, the inductance L_q has been assumed equal to L_d.

The identification of the zero-sequence inductance is not necessary for the operation of the DT hysteresis controller proposed in this thesis. In fact for its correct operation the only information necessary is the DT duration. Nevertheless a simple measurement has been carried out to identify the machine L_0 inductance. In order to measure the equivalent zero-sequence inductance the machine model developed in Chapter 3 has been used. From the transient response of the ZSC when a ZSV is applied the machine inductance can be obtained. VSC A is kept with all the three legs connected at the positive dc bus (i.e. $\overline{V}_7$) while VSC B is switched from $\overline{V'}_7$ to $\overline{V'}_0$. In particular VSC B applies $\overline{V'}_0$ for the sample time duration of 25 μs. The resultant ZSC transient with a dc link voltage of 80 V is shown in Fig. 8.8. The resultant ZSV applied is equal to the dc link when the voltages applied are $\overline{V}_7$ and $\overline{V'}_0$ for VSC A and B respectively. Since the machine is not rotating the third harmonic back-EMF is zero, furthermore also the machine phase resistance can be neglected during the transient.

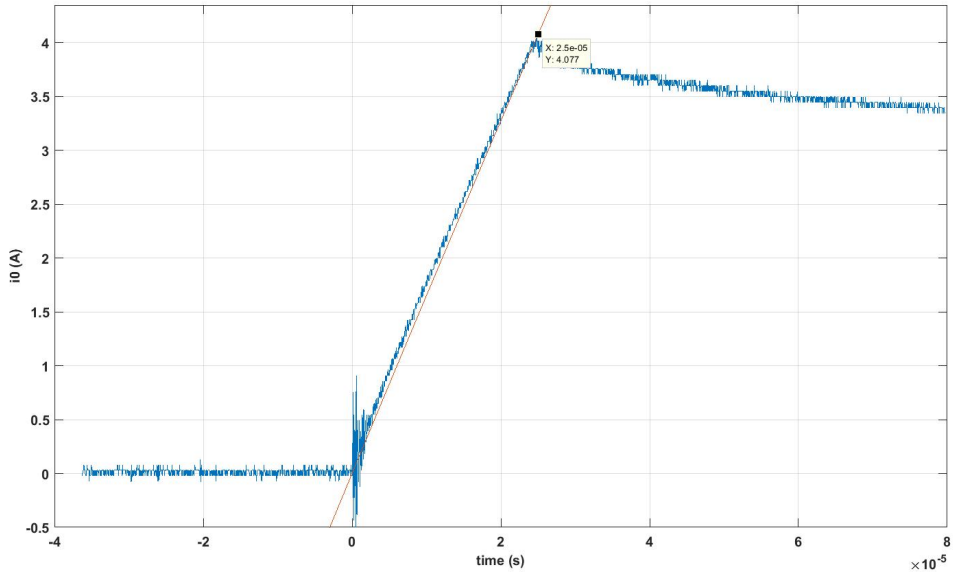


Figure 8.8: ZSC transient for the L_0 estimation. i_0 (blue), calculated i_0 with the estimated L_0 (red).

The calculated L_0 is shown in (8.4)

$$L_0 = \frac{V_{dc}\Delta t}{\Delta i_0} = \frac{80 * 25 * 10^-6}{4.077} = 0.49mH \tag{8.4}$$

Fig. 8.8 shows the actual i_0 and the ZSC calculated with the L_0 obtained in (8.4) when the machine resistance and the third harmonic back-EMF are neglected.

8.2.4 Mechanical Parameters Identification

The mechanical system under identification is the one described by (8.5).

$$T_m - T_l = \frac{3}{2}\lambda_m i_q - T_l = J\frac{d\omega_m}{dt} + B\omega_m + Dsign(\omega_m) \tag{8.5}$$

Considering that the terms $\frac{3}{2}\lambda_m$ can be grouped under a single parameter k_t, (8.5) can be rewritten as

$$i_q - \frac{T_l}{k_t} = \frac{J}{k_t}\frac{d\omega_m}{dt} + \frac{B}{k_t}\omega_m + \frac{D}{k_t}sign(\omega_m) \tag{8.6}$$

The identification is carried out measuring i_q and the mechanical speed. The whole mechanical system constituted by the PMSM coupled with the dc load has been considered. The Least Square Estimation Method has been applied also for the mechanical parameters. The measured quantities i_q and w_m are necessary to obtain the unknown quantities $J/k_t, B/k_t$ and D/k_t. An open loop control has been performed where a constant torque, i.e. a constant i_q current is controlled until the machine reaches a certain speed, then the torque is inverted in order to change the direction of rotation of the machine. Since the converter used is not provided with a breaking chopper the regenerative brake is not allowed. The speed variation that could be achieved was limited by the maximum dc link voltage variation that the capacitors could handle.

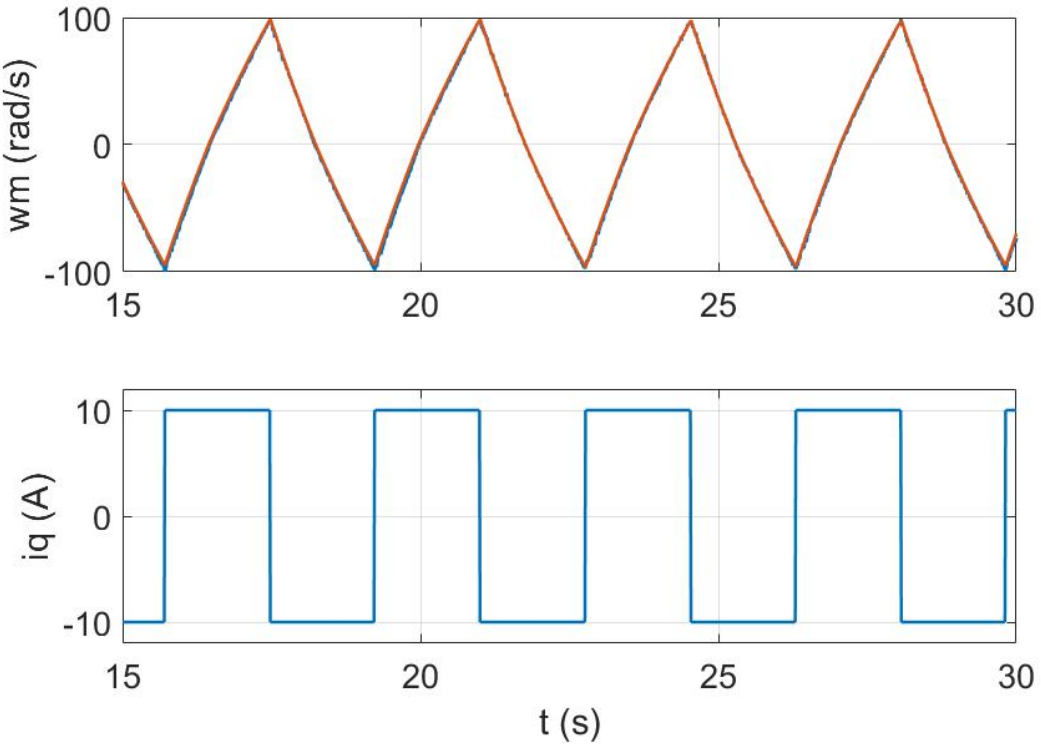


Figure 8.9: Top: Comparison between the measured speed ω_m (blue) and the output of the simulated system $\omega_{m,sim}$ (red). Bottom: Input i_q current.

Fig. 8.9 shows the mechanical speed transient when a square wave i_q current is applied to the machine. The identification of the mechanical parameters is done with the same method applied for the electrical parameters. It can be noticed that the output ω_m of system (8.5) matches the real speed output ω_m meaning that, in a good approximation, the identified parameters can be considered correct. The identification gave as output 0.0886 As^2, 0.0228 As and 0.3822 A for J/k_t, B/k_t and D/k_t, respectively.

8.3 Standard PWM Experimental Results

Firstly the experimental results when a standard PWM is applied on both VSCs are presented. Since the two converters use different technologies for the power modules the switching frequencies have been selected to be 10 kHz for the IGBT converter and 40 kHz for the SiC one. The performance in star connected configuration are presented in order to be compared with the OEW mode of operation of the machine. All the experimental results presented in this paragraphs are carried out employing the current loop controller and speed loop regulator designed in Chapter 6.

8.3.1 PMSM performance in star connected configuration under Standard PWM

The main benefit of the OEW stator coils configuration over the star connected one consists in the higher dc link voltage available. Until the dc link voltage available is higher then the back EMF of the machine it is possible to provide higher torque and therefore accelerate the machine. As previously explained the OEW configuration allows to apply to each phase the full dc link voltage instead of only half as it happens for the star connected topology. Therefore, in the latter case, the maximum speed that can be reached is half of what is possible to obtain in the OEW configuration. Fig. 8.10 shows the speed transient response of the PMSM when connected in star configuration. A reference speed of 3000 rpm is requested, it can be noticed that the actual speed that the machine can reach is around 1920 rpm, corresponding to the saturation of the reference voltages at the maximum value of $\frac{V_{dc}}{\sqrt{(3)}}$ that can be supplied with a standard 2-level VSC.

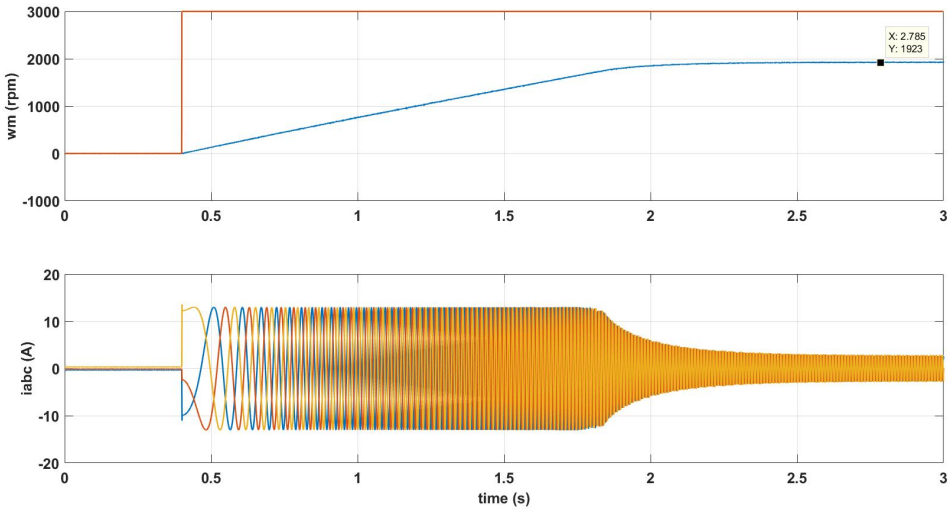


Figure 8.10: Speed transient of the star connected PMSM. Top: mechanical speed in rpm (blue) and reference mechanical speed (red). Bottom: phase currents i_{abc}.

8.3.2 OEW-PMSM performance under Standard PWM

Fig. 8.11 shows the performance of the OEW drive when two standard PWM modulators are used to control the machine. The measurements have been taken using the control board sampling at $25\mu s$. It can be noticed how the ZSC high frequency ripple is superimposed on the phase currents reducing significantly the waveform quality. The q and d axis currents are not affected by the ZSC distortion and are also reported in Fig. 8.11. The reference i_q^* current is provided by the external speed loop while the direct axis current is set to 0. A reference speed of 1000 rpm is requested.

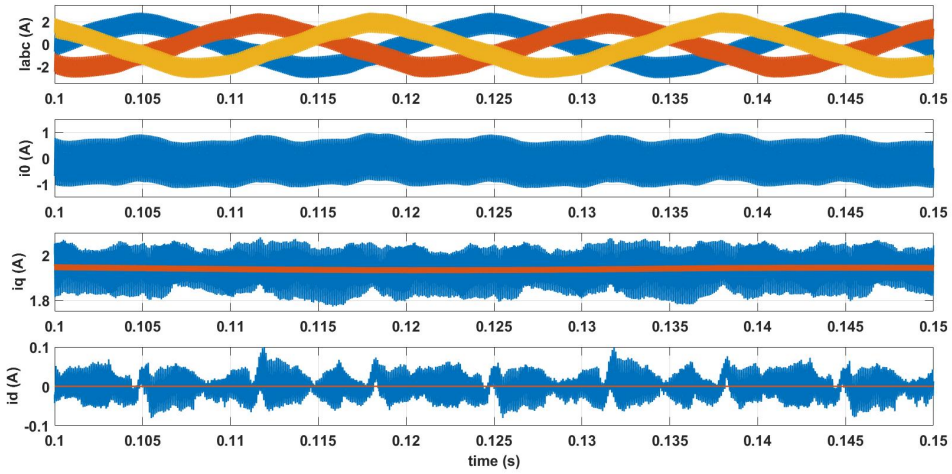


Figure 8.11: OEW-PMSM performance under standard PWM at 1000 rpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^*.

Since one third of the ZSC is summed up to all the three phase currents it is possible to determine the phase current waveform as if the i_0 would be zero. Fig. 8.12 shows the actual i_a phase current profile in blue and the ideal one in red, as if there would not be any ZSC. It is clear how the ZSV generated by the two VSCs significantly reduces the drive performance due to the additional i_0 circulating.

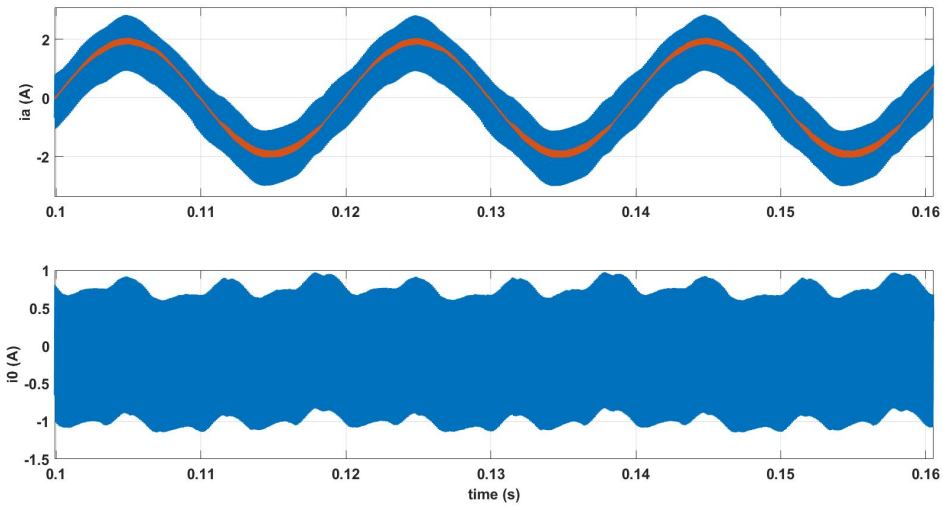


Figure 8.12: OEW-PMSM performance under standard PWM at 1000 rpm. Top: actual i_a phase current (blue) and ideal i_a phase current (red). Bottom: ZSC i_0.

The OEW-PMSM performance at the rated speed of 3000 rpm are shown in Fig. 8.13. The measurements here are acquired with an oscilloscope and then post processed with Matlab. The three converter voltages $V_{aa'}, V_{bb'}$ and $V_{cc'}$ have been measured and used to derive V_0^{OEW}. It can be noticed that as expected when using a standard PWM the ZSV varies from $-V_{dc}$ to $+V_{dc}$ since all the possible space voltage vectors can be applied as demonstrated in Chapter 4. Fig. 8.13 shows ZSV applied by the dual-inverter, the i_a phase current profile and the circulating ZSC, which is characterized by an high frequency ripple caused by the ZSV introduced by the standard PWM.

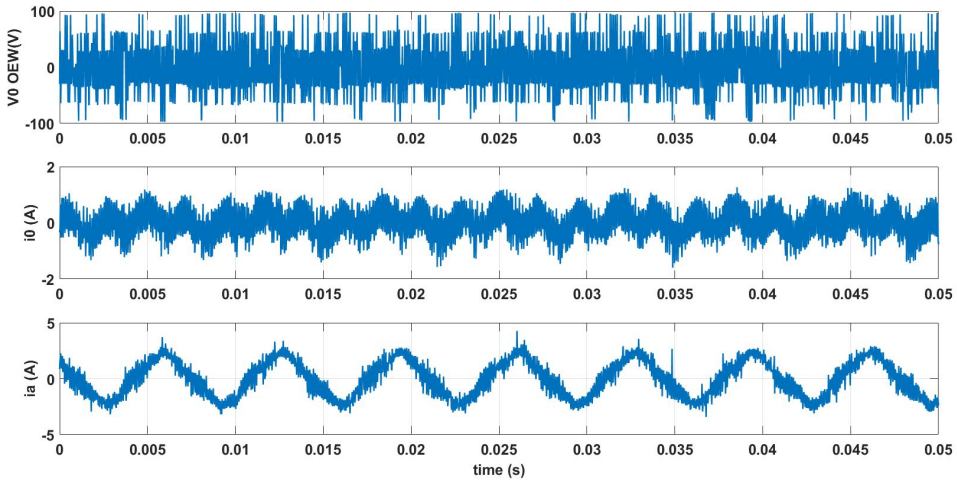


Figure 8.13: OEW-PMSM performance under standard PWM at 3000 rpm. Starting from the top: V_0^{OEW} ZSV, ZSC i_0, phase current i_a.

Fig. 8.14 shows the phase voltages for the SiC and IGBT VSCs and the resultant phase voltage applied to the machine. In Fig. 8.15 the phase voltages of both SiC and IGBT converters are shown and used to calculate the respective ZSVs. It can be seen how the two ZSVs produced have significantly different profiles. A detail of the V_0^{OEW} ZSV applied to the machine when the standard PWM is used for both converters is shown in Fig. 8.16. The resultant ZSV assumes values from -V_{dc} to +V_{dc} causing an high intensity ripple on the ZSC which is superimposed on the sinusoidal third harmonic ZSC flowing due to the machine non-sinusoidal back-emf.

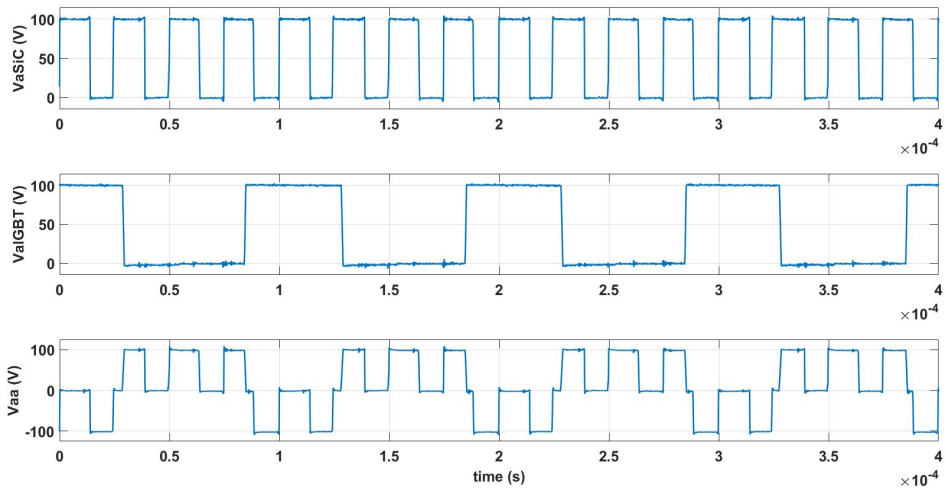


Figure 8.14: Dual-Inverter Voltages. Top: V_{a0}^{SiC}. Middle: V_{a0}^{IGBT}. Bottom: $V_{aa'}^{OEW}$.

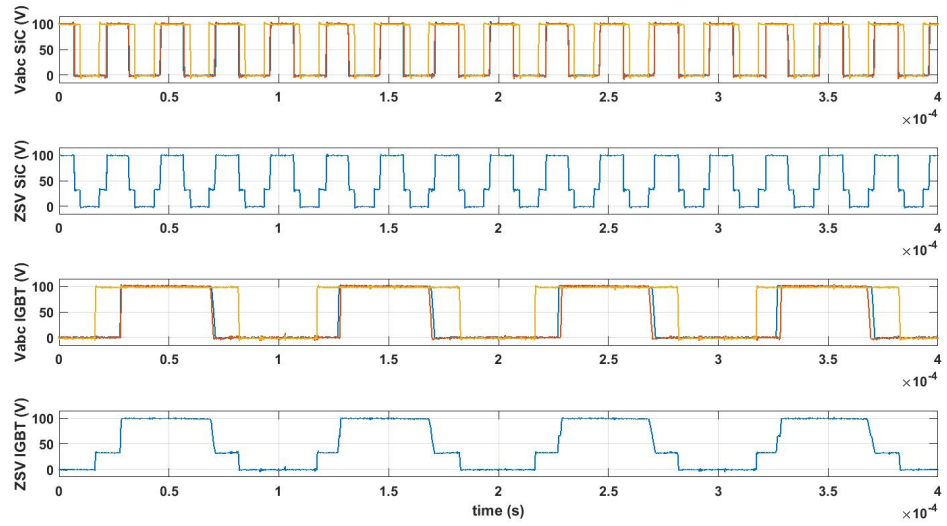


Figure 8.15: Dual-Inverter Voltages and ZSVs. Starting from top: V_{abc}^{SiC}, V_{0}^{SiC}, V_{abc}^{IGBT}, V_{0}^{IGBT}.

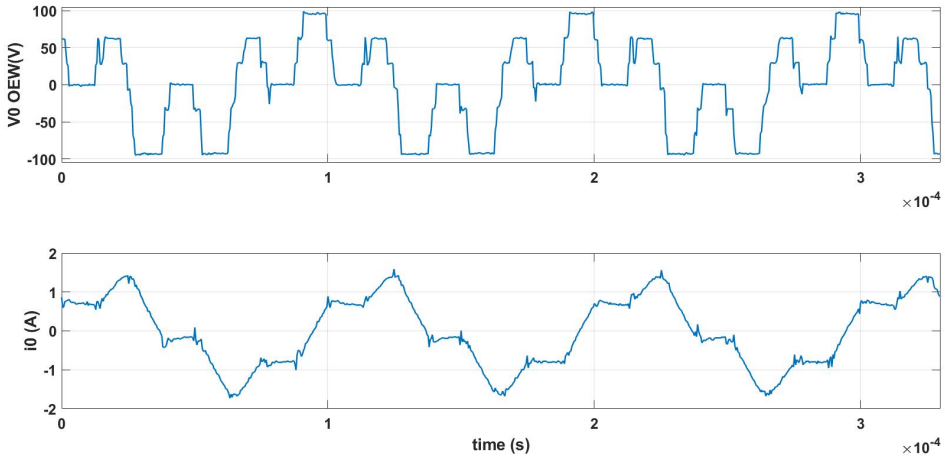


Figure 8.16: Detail of 8.13. Top: V_0^{OEW} ZSV. Bottom: ZSC i_0.

Fig. 8.17 shows the comparison of the experimental and simulative ZSV waveforms. It can be noticed that the ZSV profile obtained, and consequently the circulating ZSC perfectly match with the waveform profiles obtained in simulation.

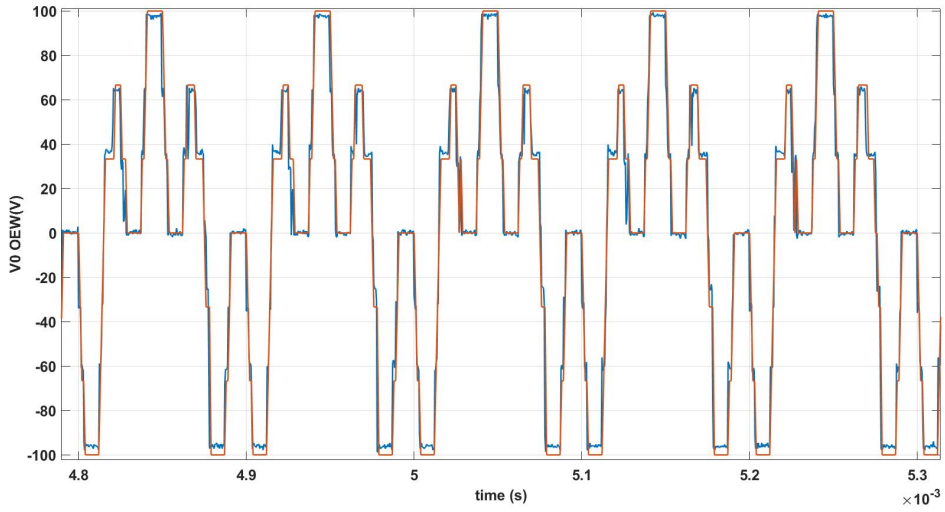


Figure 8.17: Comparison of the experimental (blue) and simulative (red) V_0^{OEW} profile.

Since for both VSCs a standard PWM is used to synthesize the reference voltages, no restriction on which voltage vectors to be applied by the VSCs is introduced. Therefore the maximum dc link utilization for this topology can be achieved. Referring to Fig. 2.19 the maximum voltage available corresponds to $\sqrt{(\frac{4}{3})}V_{dc}$. The maximum speed achieved is 3777 rpm. Fig. 8.18 shows the speed response to a speed step reference of 5000 rpm.

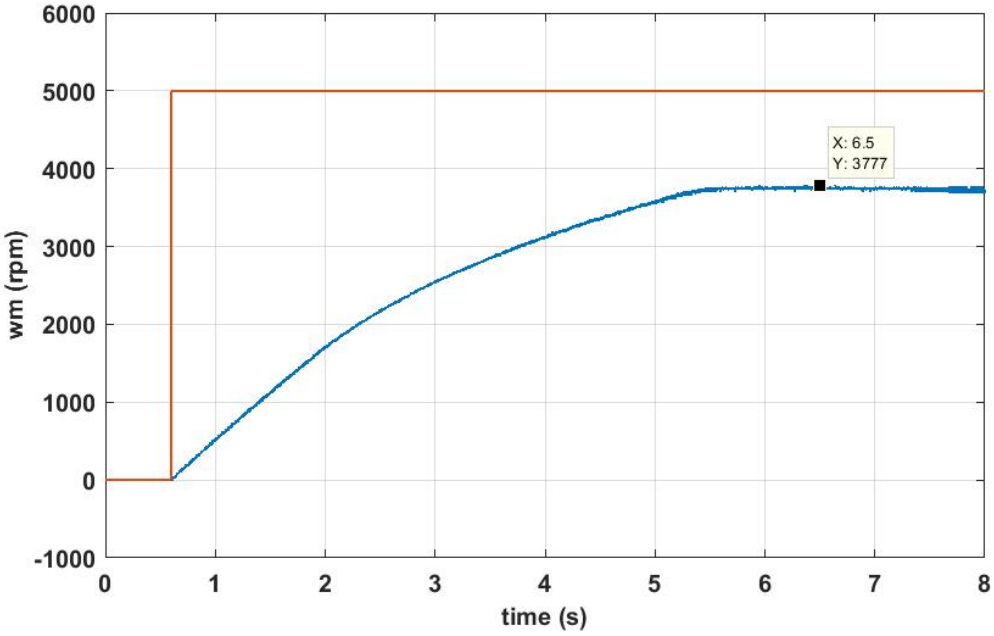


Figure 8.18: Speed transient of the star connected PMSM. Top: mechanical speed in rpm (blue) and reference mechanical speed (red). Bottom: reference phase voltages.

8.4 SVPWM for instantaneous ZSV Elimination Experimental Results

This section presents the experimental results when the proposed SVPWM for ZSV elimination is used to control both VSCs. In the first paragraph a brief explanation

of how the controllers have been implemented is given, in particular the synchronization between the regulators running in DSP and the modulators and ZSC hysteresis controller is discussed. Then the performance of the OEW-PMSM under the new modulation are given. Particular attention is given to the voltages produced by the two VSCs and the ZSVs respectively produced. The single converter phase voltages are measured and the corresponding ZSV produced is calculated. Afterwards the performance when the DT hysteresis controller is implemented are evaluated. A brief explanation of the DT hysteresis controller is given to help understand the interaction between the speed and q-, d- axis current controllers running in the DSP and the zero-sequence current controller implemented in the FPGA.

8.4.1 Implementation Logic of the SVPWM for the three Active Voltage Vectors SVM

As previously explained in Chapter 5 in order to achieve the control of the ZSC, and in particular its suppression, high sample time rates are necessary to appreciate the fast dynamics that characterize the 0-sequence axis. The digital controller sample time is $25\mu s$, which corresponds to the SiC VSC switching frequency, which would be too slow to sample correctly the ZSC and apply the DT hysteresis control. The SiC VSC DT is set to $1\mu s$, it is a constant quantity previously selected in order to allow the correct turn on and turn off of the power modules. A minimum sample time, at least equal to the DT is necessary. The motor phase currents are acquired every $1\mu s$ using the external ADCs described in [147], and then acquired by the FPGA. Since the DT hysteresis controller is highly dependant from the phase currents sign a precise offset correction of the ADCs measurement is necessary. To achieve a correct elimination of the current offset a Moving Average Filter (MAF) has been implemented in the FPGA. The measurements from the ADCs are 16 bit signed logic vectors, for ease of implementation all the arithmetic operations in the FPGA are implemented as fixed point arithmetic. The 16 bit data has to be interpreted as a Q15, which means 1 sign

bit and 15 fractional bit. The calculation of the i_0 current is done as the sum of the three phase currents divided by three, therefore it requires two sum operations and a product. These operations have been pipelined in order to have available the ZSC value at every FPGA clock. In order to implement the three active vectors SVPWM for the fast switching SIC VSC it is necesary to synchronize the variable carriers phase modulators implemented in FPGA with the reference dwelling times calculated by the DSP controller according to (4.10) and (4.11). Fig. 8.19 shows a block diagram which explains the DSP and FPGA synchronization. The FPGA generates the interrupt at the desired sample time of $25\mu s$ for the DSP, once the calculations of the dwelling times is done these signals are written into the FPGA together with the signal acp_{idle}, which indicates that the DSP controller has ended all its calculations.

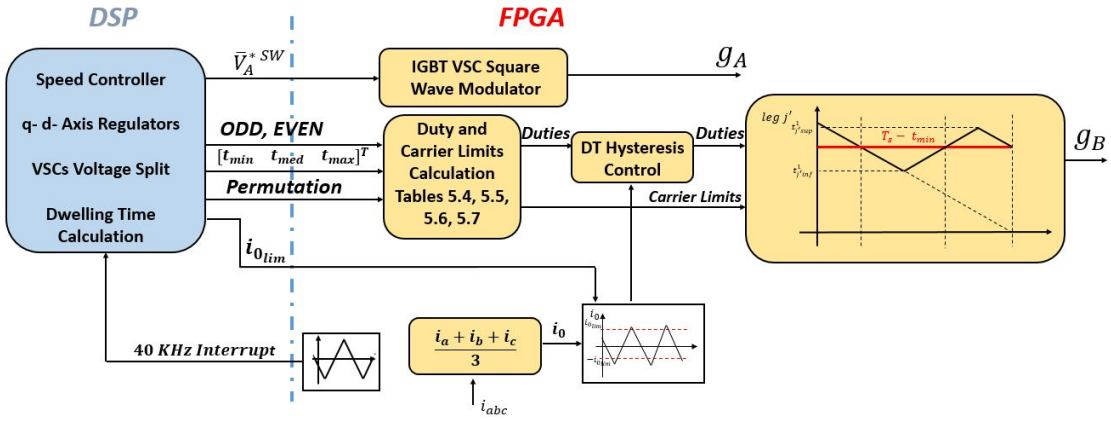


Figure 8.19: Block Diagram of the DSP and FPGA implementation logic of the proposed SVPWM.

As soon as the acp_{idle} signal rises, the FPGA starts calculating the duty cycles and leg carrier limits according to Tables 5.4 and 5.5 for the duty cycles calculation and Tables 5.6 and 5.7 for the calculation of the leg carrier limits. Fig. 8.20 shows the time calculation management for the DSP and FPGA. It can be noticed that there is one sample time delay in the application of the reference duties due to the intrinsic DSP calculation delay. All together the DSP and FPGA calculation times sum up to

$12\mu s$ for the specific controllers, which is less than half of the sampling time.

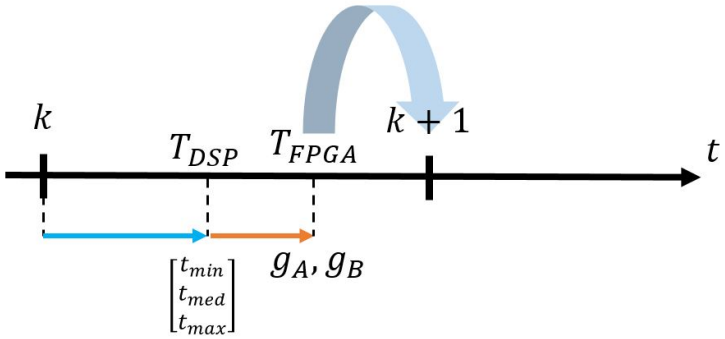


Figure 8.20: DSP and FPGA Calculation times.

8.4.2 SVPWM for Instantaneous ZSV Elimination and DT Effect on the ZSV

Firstly the performance of the proposed instantaneous ZSV elimination without taking into account the DT hysteresis controller are shown. Instead of the standard PWM modulation the proposed ZSV elimination SVPWM is used. Fig. 8.21 shows the performance of the OEW-PMSM at different operating speeds. It can be noticed that, compared with the standard PWM, the high frequency ripple caused by the circulating ZSC due to the applied ZSV has been eliminated.

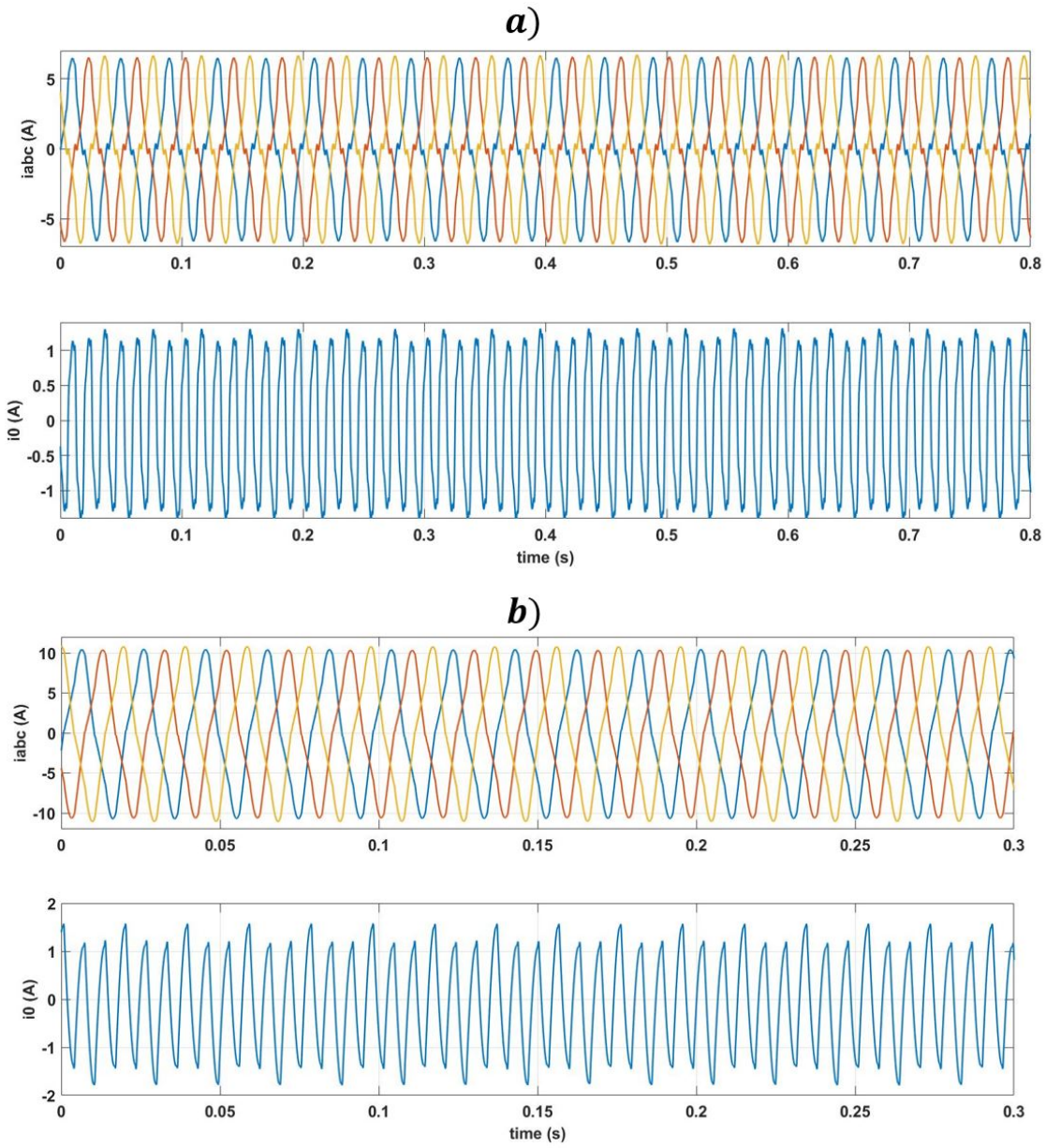


Figure 8.21: Phase currents and ZSC of the OEW-PMSM under the ZSV elimination modulation. a) phase currents and ZSC i_0 at 500 rpm. b) phase currents and ZSC i_0 at 1000 rpm.

Fig. 8.22 show the reference voltages for the two VSCs and the resultant refer-

ence voltages for the OEW-PMSM, which are obtained as $\overline{V}_A^* - \overline{V}_B^*$. As explained in Chapter 4 the slow switching IGBT converter is square wave modulated at the fundamental frequency of rotation of the machine while the SiC technology based converter is controlled in order to have the sinusoidal reference voltages on the machine. The associated reference dwelling times for the three active vectors used to synthesize the SiC VSC reference voltage vector are shown in Fig. 8.23 when the machine is rotating at 1000 rpm. The reference duty cycles are expressed in number of FPGA clocks. Since the FPGA frequency is 100 MHz, 2500 clock cycles correspond to $25\mu s$.

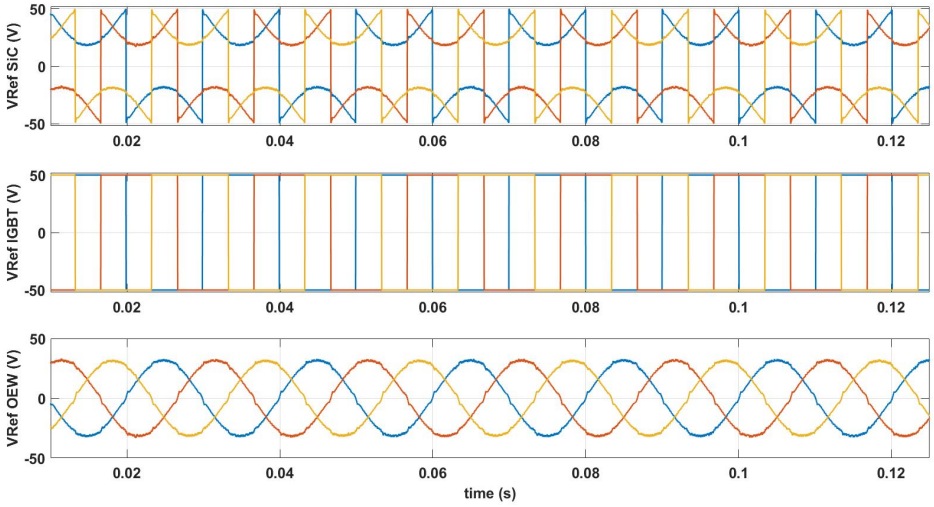


Figure 8.22: Dual-Inverter reference voltages. Starting from top: V_{abc}^{*SiC}, V_{abc}^{*IGBT}, V_{abc}^{*OEW}.

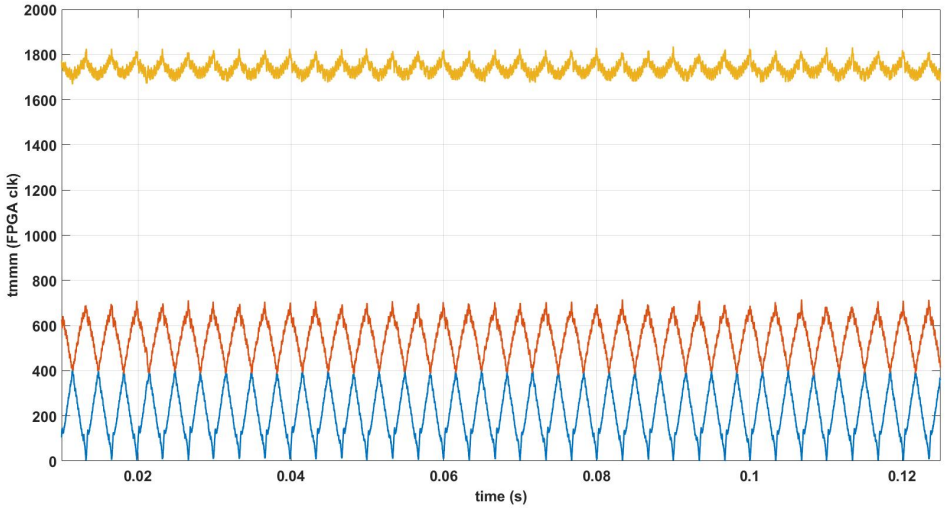


Figure 8.23: Reference dwelling times for the three active vectors used to modulate the fast switching SiC VSC. t_{min} (blue), t_{med} (red) and t_{max} (yellow).

Fig. 8.24 shows the phase voltages of the two VSCs composing the dual-inverter. Compared with the PWM, now the VSC is switching at the fundamental frequency of the machine. Fig. 8.25 shows the normalised IGBT phase voltage and the normalised motor phase current i_a. It is evident that the switching frequency of the IGBT converter corresponds to the fundamental frequency of the machine since the phase voltage and phase current have the same period.

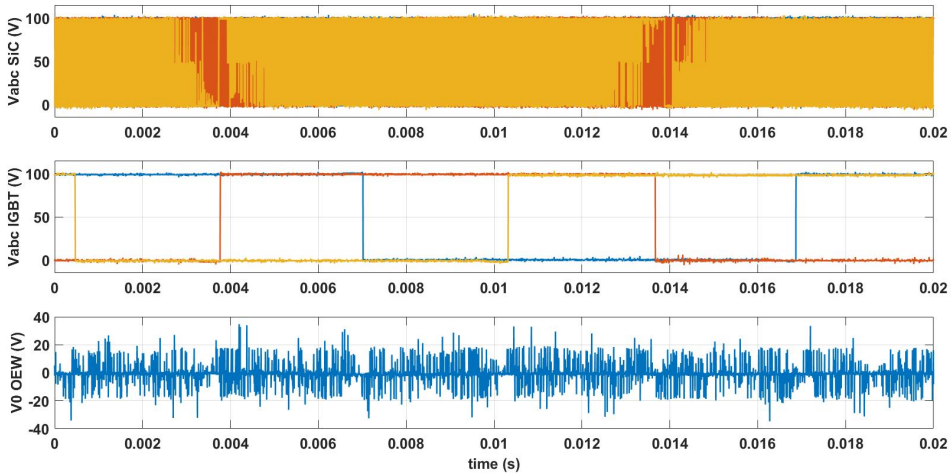


Figure 8.24: Dual-Inverter Voltages profiles for the ZSV Elimination SVPWM. Starting from top: V_{abc}^{SiC}, V_{abc}^{IGBT}, ZSV V_0^{OEW}.

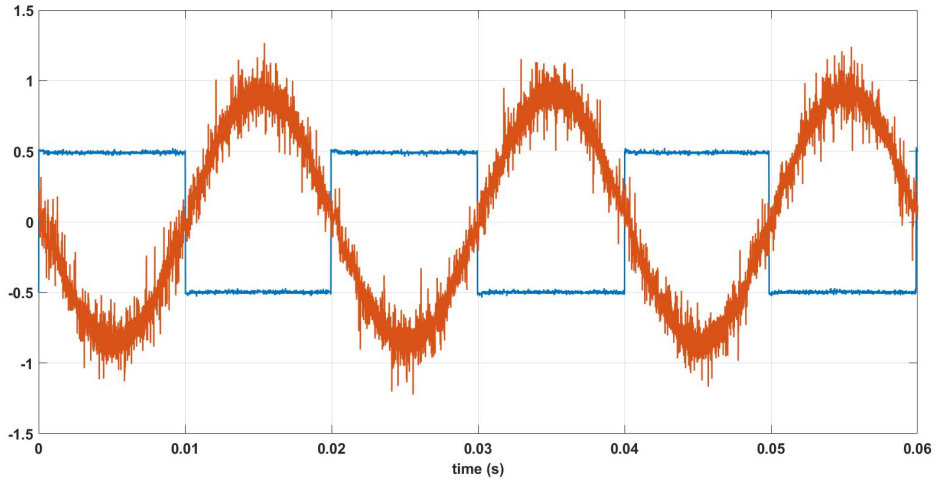


Figure 8.25: Normalised IGBT phase voltage V_{a0}^{IGBT} and normalised phase current i_a at 1000 rpm.

The phase voltages and the resultant ZSV produced by the fast switching SiC VSC are shown in Fig. 8.26. The expected square wave profile is obtained. The additional

ZSV distortion is introduced by the DT. In order to better understand its behaviour two enlargements of Fig. 8.26 are shown in Figures 8.27 and 8.28. Spike A of Fig. 8.27 is equivalent to the case reported in Fig. 5.5. Phase a (in blue), delays to turn off because of the DT distortion, theoretically this would introduce a voltage distortion of value V_{dc} and duration of $1\mu s$ on the SiC ZSV. It can be noticed that, because of the real behaviour of the power modules, the turn on of phase b (in red) is not instantaneous therefore causing a reduction in the voltage distortion introduced (spike A). The case presented in Fig. 5.6, which causes a negative voltage distortion on the SiC ZSV is shown in 8.28. The turn on of phase a is delayed by the DT but the turn off of phase c (in yellow) is not instantaneous therefore causing a voltage distortion pulse with reduced duration. The turn on and turn off of the switching devices is highly dependant from the amount of current flowing. The voltage distortion spikes B and D of Fig. 8.27 and 8.28 show the case in which the turn on and turn off of two different legs overlap causing a reduction in the maximum voltage reached.

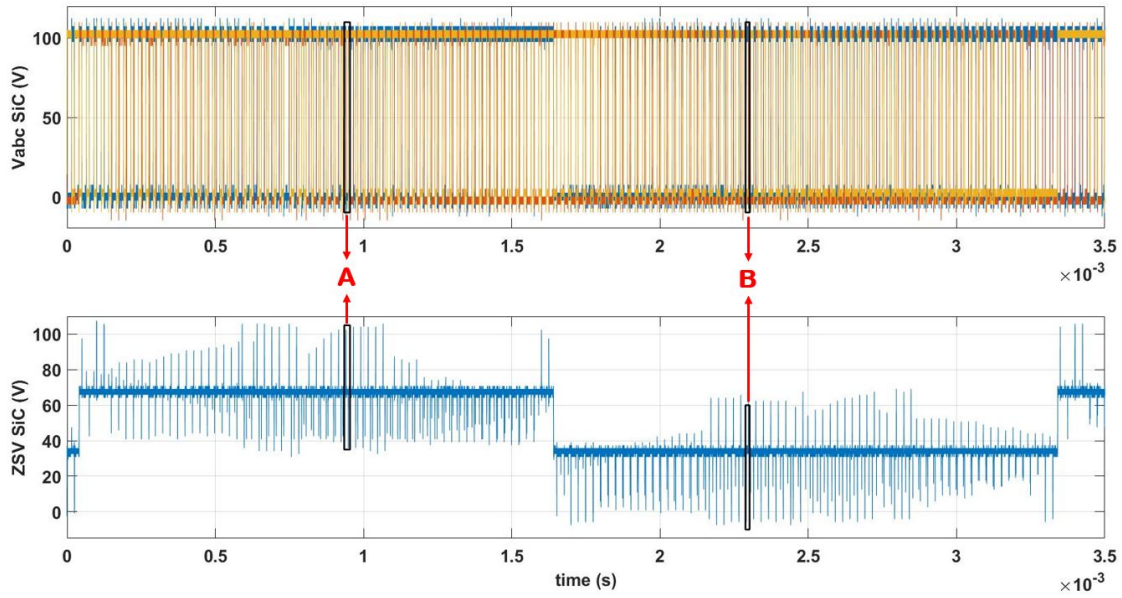


Figure 8.26: Dual-Inverter Voltages profiles for the ZSV Elimination SVPWM. Starting from top: V_{abc}^{SiC}, V_0^{SiC}.

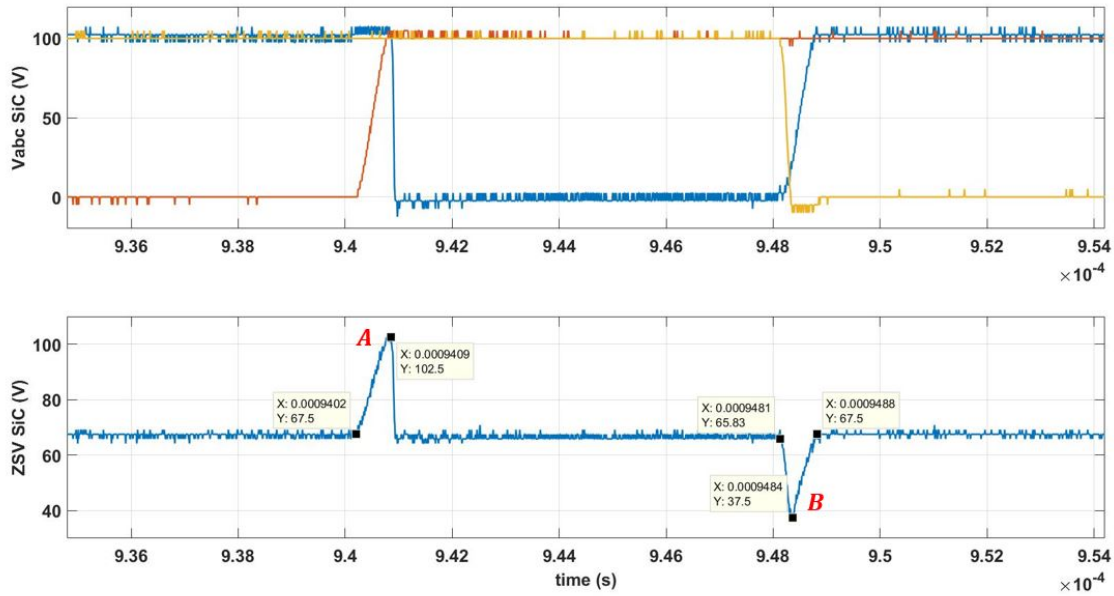


Figure 8.27: Detail A of Fig. 8.26. Starting from top: V_{abc}^{SiC}, V_0^{SiC}.

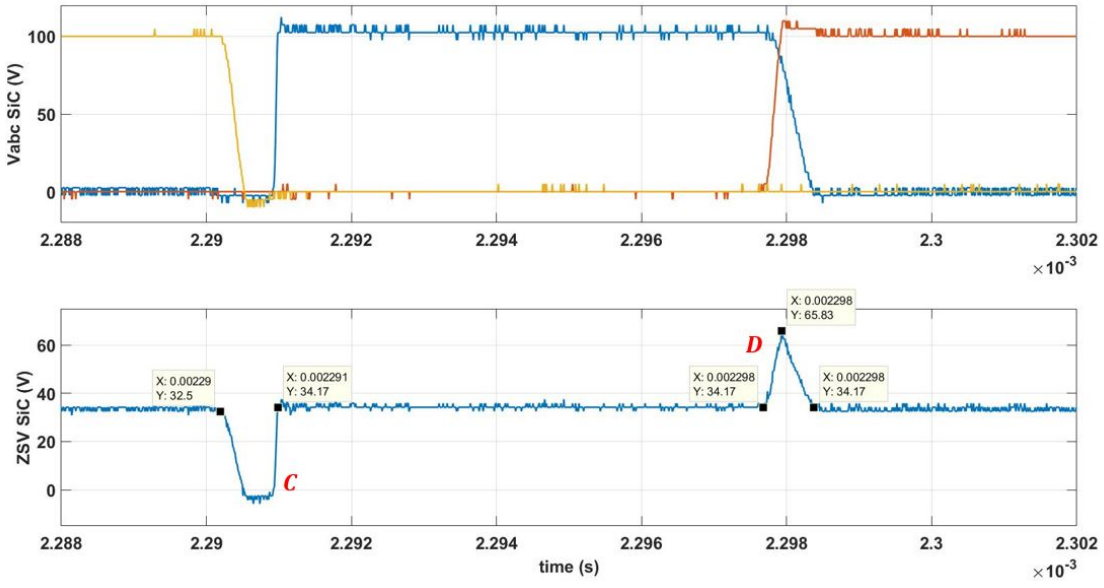


Figure 8.28: Detail B of Fig. 8.26. Starting from top: V_{abc}^{SiC}, V_0^{SiC}.

The effect of the turn on and turn off of the devices changes the entity of the distortion

of the DT, taking it into account would significantly increase the complexity of the DT compensation algorithm. In fact it would need to take into account the turn on and turn off times and their dependency from the instantaneous phase currents values. Therefore the real behaviour of the devices would not allow to fully compensate the voltage distortion introduced by the DTs with the algorithm proposed in Chapter 5. The duration of the ZSV voltage distortion due to the DT is set to be a constant quantity and equal to t_{DT} in the proposed algorithm while in reality it changes because of the real behaviour of the power switches. As it will be shown in Section 8.4.3, the variable turn on and off times of the devices does not influence the DT hysteresis controller. The compensation of the DT is actuated as an open loop action, which depends on the exact knowledge of the DT duration. Therefore any error in the DT duration used to compensate the voltage distortion would result in an additional distortion on the zero sequence axis. On the other hand, the ZSC DT hysteresis controller is based on the i_0 current feedback. Even though the DT distortion is bigger or smaller than the ideal one, the controller will require to compensate or not the DT according to the error between the ZSC hysteresis band and the ZSC i_0 value.

8.4.3 DT Hysteresis Control of the ZSC i_0

In this paragraph the performance of the DT hysteresis controller for the elimination of the ZSC circulating due to the non-sinusoidal back EMF are evaluated. As presented in Chapter 5, the hysteresis DT controller allows to select the i_0 hysteresis band. It can be set from the DSP controller during the machine operation. Figures 8.29, 8.30 and 8.31 show the controller performance at the mechanical rotational speed of 500, 2000 and 3000 rpm respectively. It can be noted that the i_0 ZSC has been completely eliminated. Furthermore the DT hysteresis controller is independent from the operating point of the machine, in fact the only necessary condition for its correct operation is that the reference voltage vector for the dual-inverter lays inside the circle of radius V_{dc} in the $\alpha\beta$ plane, which represent the voltage limits of the

instantaneous ZSV elimination modulation proposed.

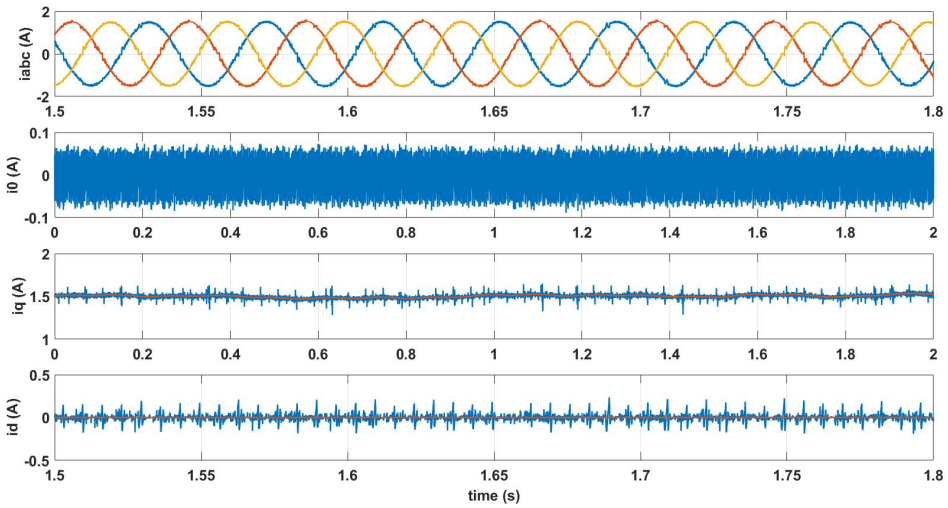


Figure 8.29: OEW-PMSM performance under ZSV elimination modulation at 500 rpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current.

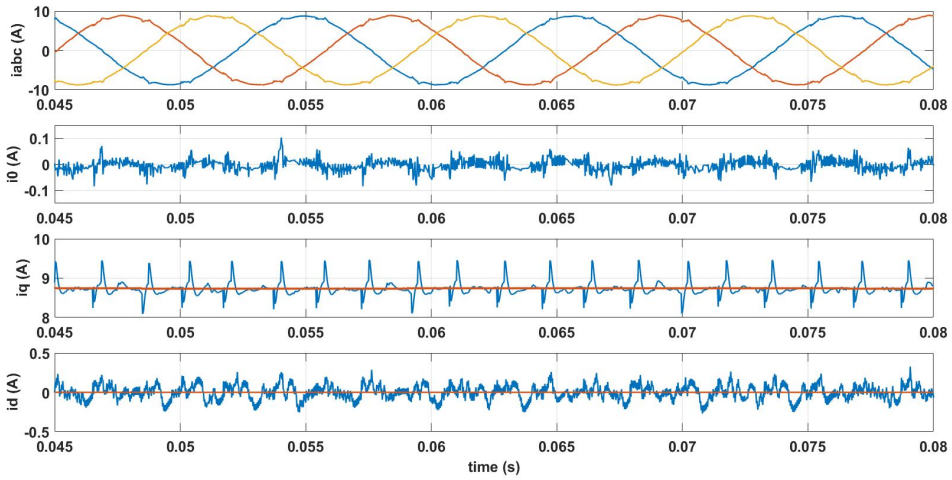


Figure 8.30: OEW-PMSM performance under ZSV elimination modulation at 2000 rpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current.

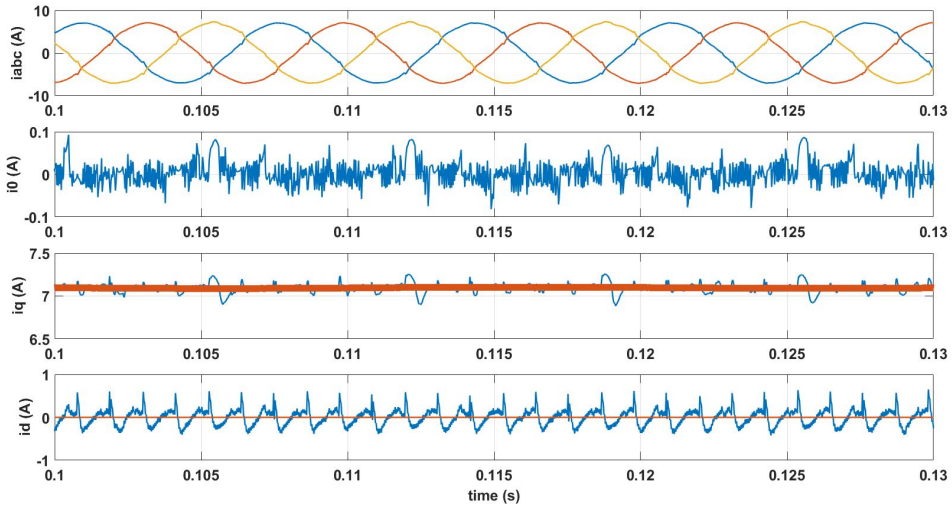


Figure 8.31: OEW-PMSM performance under ZSV elimination modulation at 3000 rpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current.

In order to show the effectiveness of the proposed ZSC hysteresis controller over the whole speed range a speed transient from 0 to the rated speed of 3000 rpm has been performed as shown in Fig. 8.32. The ZSC hysteresis band is set to 0 except for the speed range that goes from 100 to 150 rad/s where it is set to 0.5 A. In this way it is possible to observe that the ZSC can be controlled in any speed range independently from the the operating point.

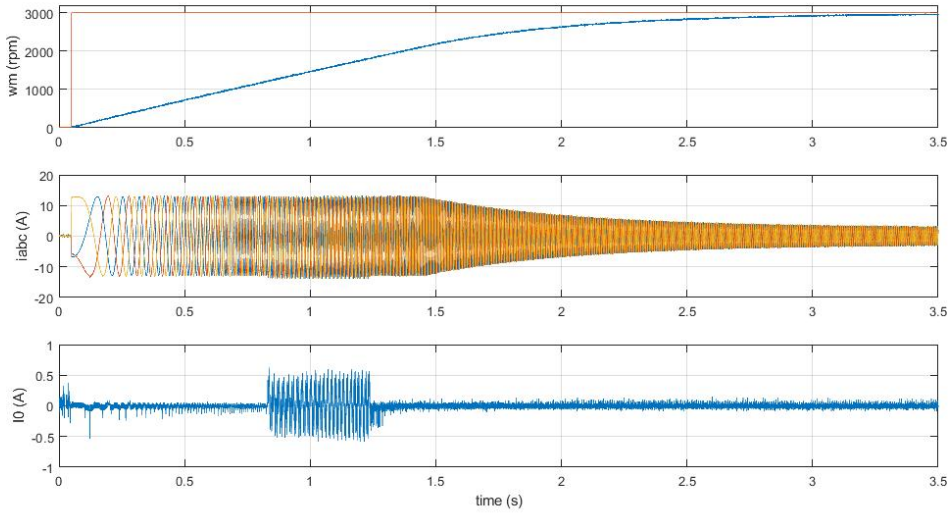


Figure 8.32: Speed transient from 0 to 3000 rpm. Top: reference speed (red) and actual mechanical speed (blue). Middle: phase currents. Bottom: ZSC

Figures 8.33, 8.34 and 8.35 show the machine performance when the hysteresis band is changed under different operating speeds. In Fig. 8.33 an $i_{0_{lim}}$ band step from 0.5 to 0.2 A is requested at the reference speed of 1000 rpm. In Fig. 8.34 it is shown the possibility to also request an increment in the zero sequence i_0 band, in this case a step from 0.1 to 0.6 A is requested. The most interesting case is shown in Fig. 8.35 where, at the rated machine speed, the $i_{0_{lim}}$ band is set to 0 A, therefore achieving the complete elimination of the zero sequence current. The ZSC can be completely eliminated, resulting in a significant improvement of the phase currents profiles.

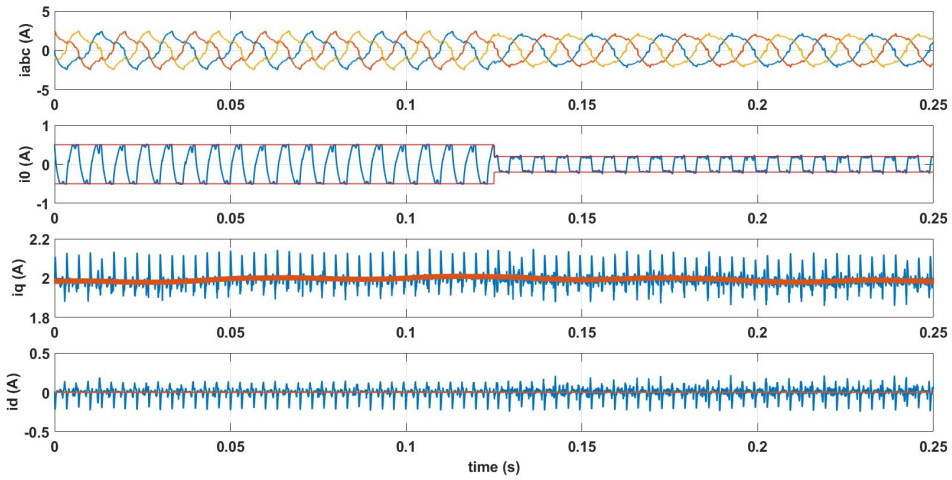


Figure 8.33: DT hysteresis band transient at 1000 rpm. Starting from the top: phase currents, ZSC i_0 (blue) and reference i_0 band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current.

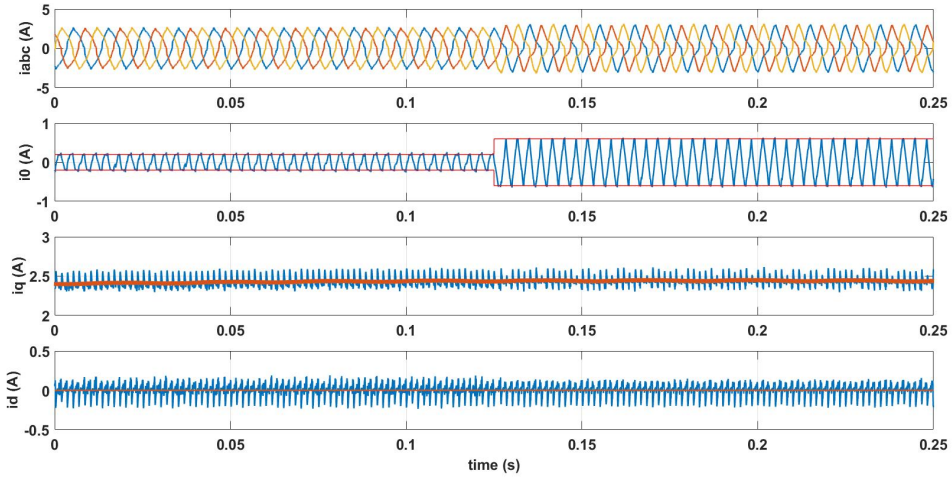


Figure 8.34: DT hysteresis band transient at 2000 rpm. Starting from the top: phase currents, ZSC i_0 (blue) and reference i_0 band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current.

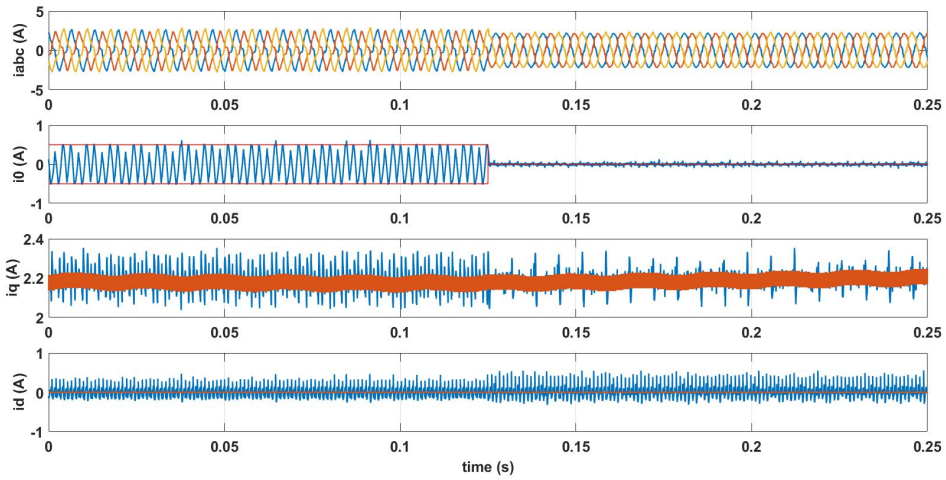


Figure 8.35: DT hysteresis band transient at 3000 rpm. Starting from the top: phase currents, ZSC i_0 (blue) and reference i_0 band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current.

The dual-inverter voltages are now presented to show the effectiveness of the proposed hysteresis controller in exploiting the ZSV distortion introduced by the DT in controlling the ZSC. Fig. 8.36 shows the phase voltages of the SiC and IGBT VSCs and the resultant phase voltage $V_{aa'}$ applied to the machine. It can be observed that the IGBT converter is square wave modulated while the SiC VSC is switching.

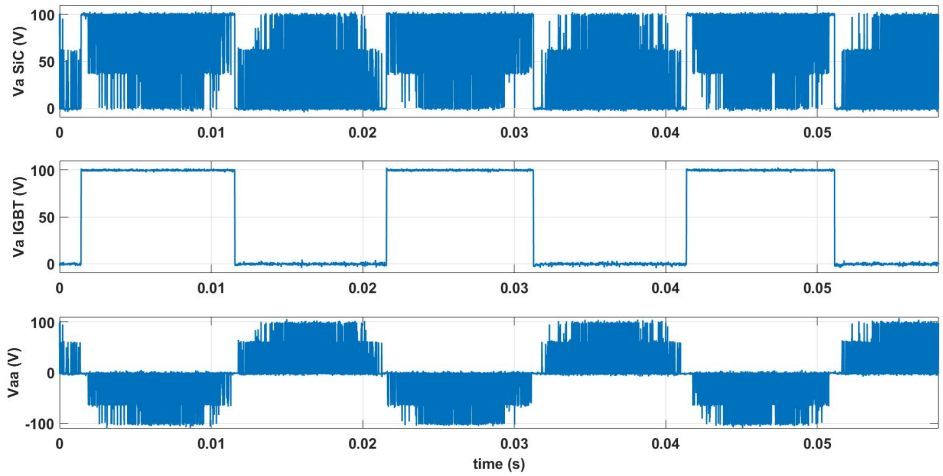


Figure 8.36: Dual-Inverter Voltages. Top: V_{a0}^{SiC}. Middle: V_{a0}^{IGBT}. Bottom: $V_{aa'}^{OEW}$.

Fig. 8.37 shows the phase voltages of the SiC and IGBT VSCs and the resultant phase ZSVs produced by the two individual VSCs. Considering that the reference voltage for the measurements corresponds to the dc link negative pole, the ZSV produced by the IGBT VSC correctly jumps from $\frac{2V_{dc}}{3}$ to $\frac{V_{dc}}{3}$. The same square wave behaviour is shown by the SiC VSC ZSV, which on top presents the voltage distortion caused by the DTs.

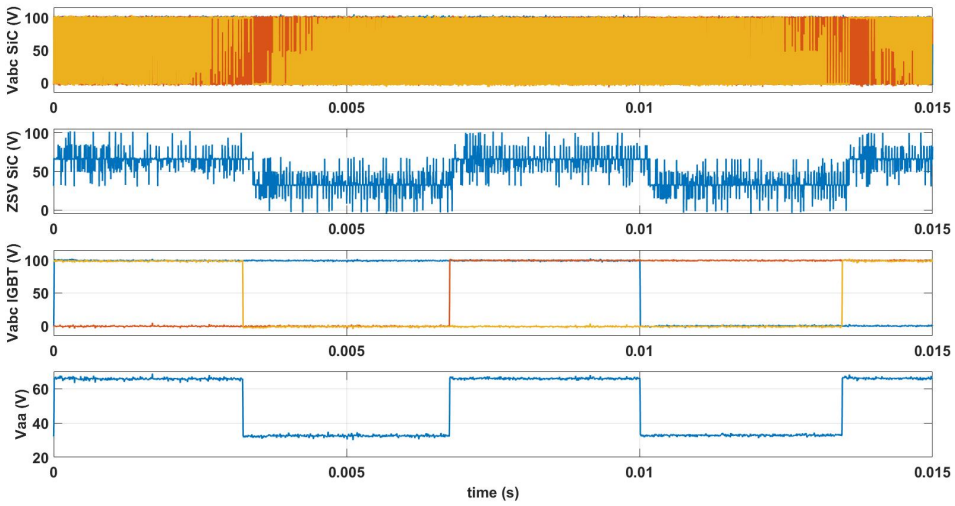


Figure 8.37: Dual-Inverter Voltages and ZSVs. Starting from top: V_{abc}^{SiC}, V_0^{SiC}, V_{abc}^{IGBT}, V_0^{IGBT}.

In Fig. 8.38 a detail of the ZSV is presented when the DT hysteresis band is set to 0 A. It can be noticed that the resultant ZSV applied on the machine goes from $\frac{V_{dc}}{3}$ to $\frac{-V_{dc}}{3}$, which corresponds to the ZSV distortion introduced by the DT. As it was shown in 8.4.3 it can also be observed how many DTs do not cause a full voltage distortion of $\frac{V_{dc}}{3}$ due to the real turn on and turn off times of the switching devices.

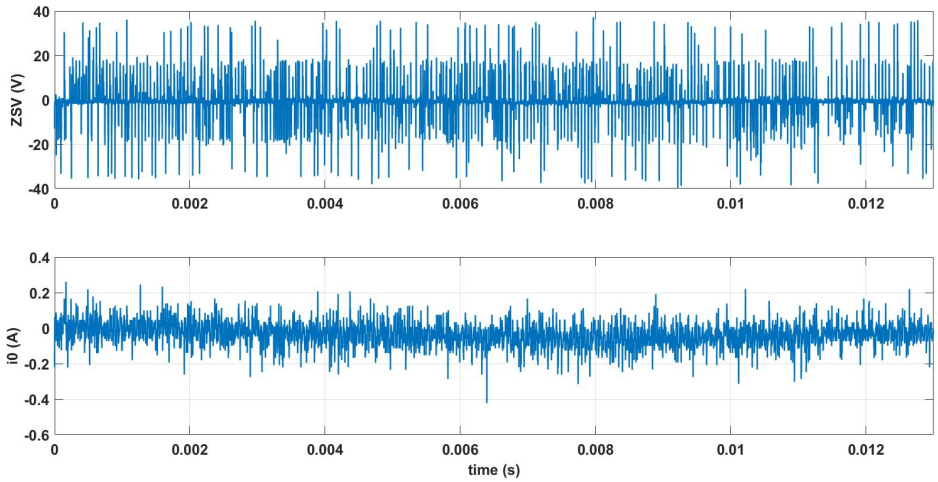


Figure 8.38: Detail of the ZSV and ZSC. Top: V_0^{OEW} ZSV. Bottom: ZSC i_0.

The maximum dc link utilization for the dual-inverter topology when exclusively voltage vectors that produce zero ZSV are used is V_{dc}, as it was shown in Fig. 2.19. Therefore the maximum speed that the machine can reach before saturating the dc link corresponds to 3380 rpm as shown in Fig. 8.39. It can be noticed that the maximum achieved speed is lower than the one that can be obtained when two standard PWM are used to control the two VSCs but it is still consistently higher than the maximum speed that can be reached when a star connected configuration for the PMSM stator coils is used.

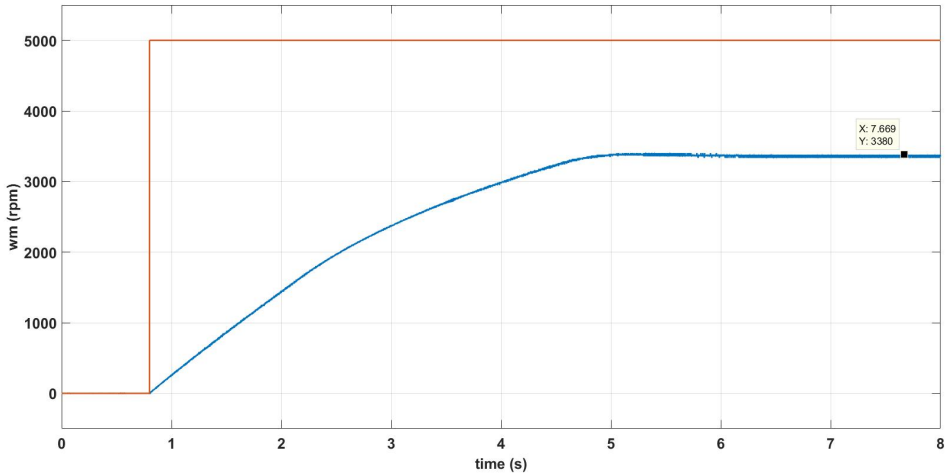


Figure 8.39: Speed transient of the star connected PMSM. Mechanical speed in rpm (blue) and reference mechanical speed (red)

8.4.4 THD and FFT measurements

In order to evaluate the performance of the proposed modulation and ZSC DT hysteresis controller the phase current THD has been evaluated. The comparison is made between the phase current THD under standard PWM modulation as presented in Section 8.3 and the phase current THD under the ZSV elimination modulation proposed, with and without the ZSC DT hysteresis controller. The same machine operating point has been considered for the comparison, the OEW-PMSM is run at 1000 rpm with a load torque of 77% of the rated torque. Fig. 8.40 shows the phase currents profiles in blue while the ideal fundamental component in red. The THD obtained are 2.8810^{-1}, 2.0510^{-1} and 1.3810^{-1} for the standard PWM the ZSV elimination modulation without DT hysteresis controller and the ZSV elimination modulation with DT hysteresis controller respectively.

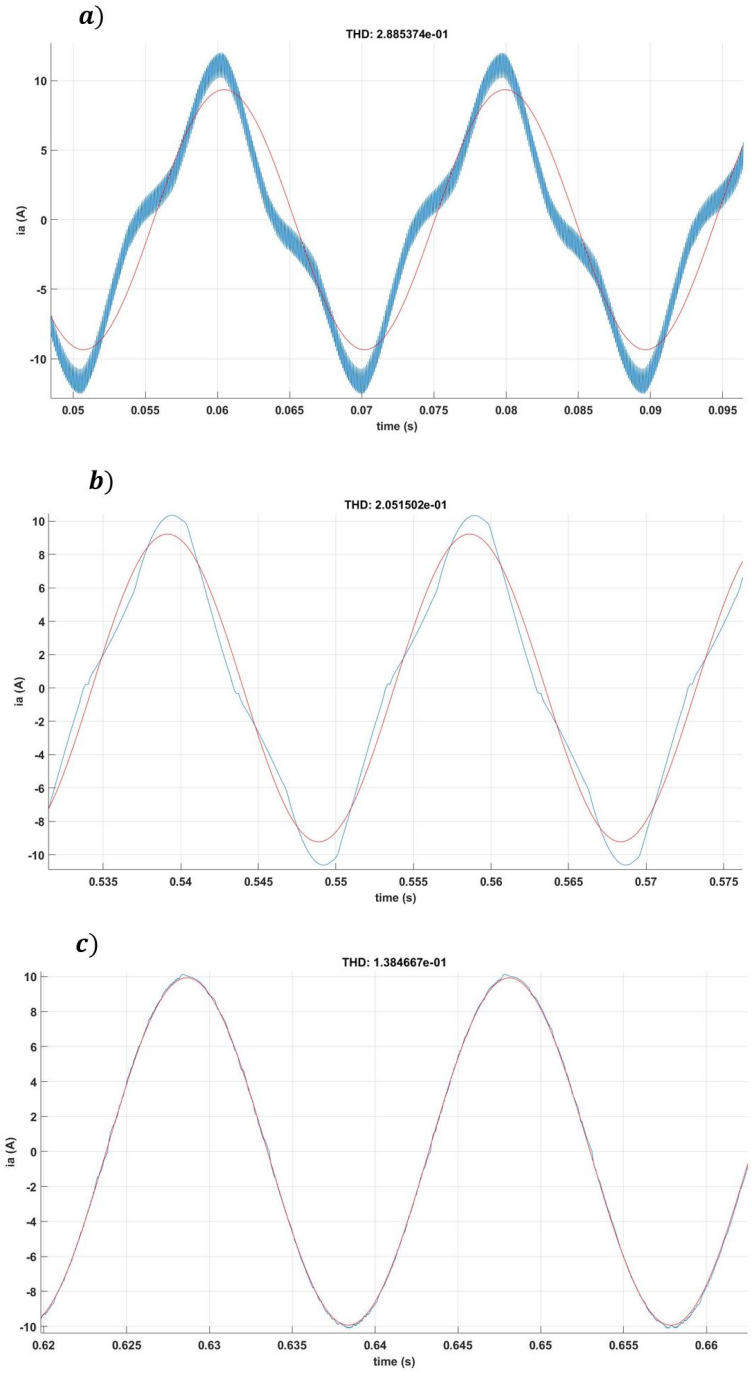


Figure 8.40: Phase current THD. a) Standard PWM. b) ZSV elimination modulation. c) ZSV elimination modulation with DT hysteresis controller.

Under the same operating point of the machine considered for the THD evaluation also an FFT of the phase current is performed to highlight the harmonic content. The current harmonics are normalised respect the amplitude of the fundamental component. It can be noticed that since the machine is rotating at 1000 rpm, corresponding at a 50 Hz fundamental frequency, the third harmonic current has a frequency of 150 Hz. In Fig. 8.41 a) the third harmonic has a value of 0.22 when a standard PWM is applied, it can be noticed that the third harmonic is slightly reduced with the ZSV elimination modulation and completely eliminated when the DT hysteresis controller is introduced, as shown in Fig. 8.41 c).

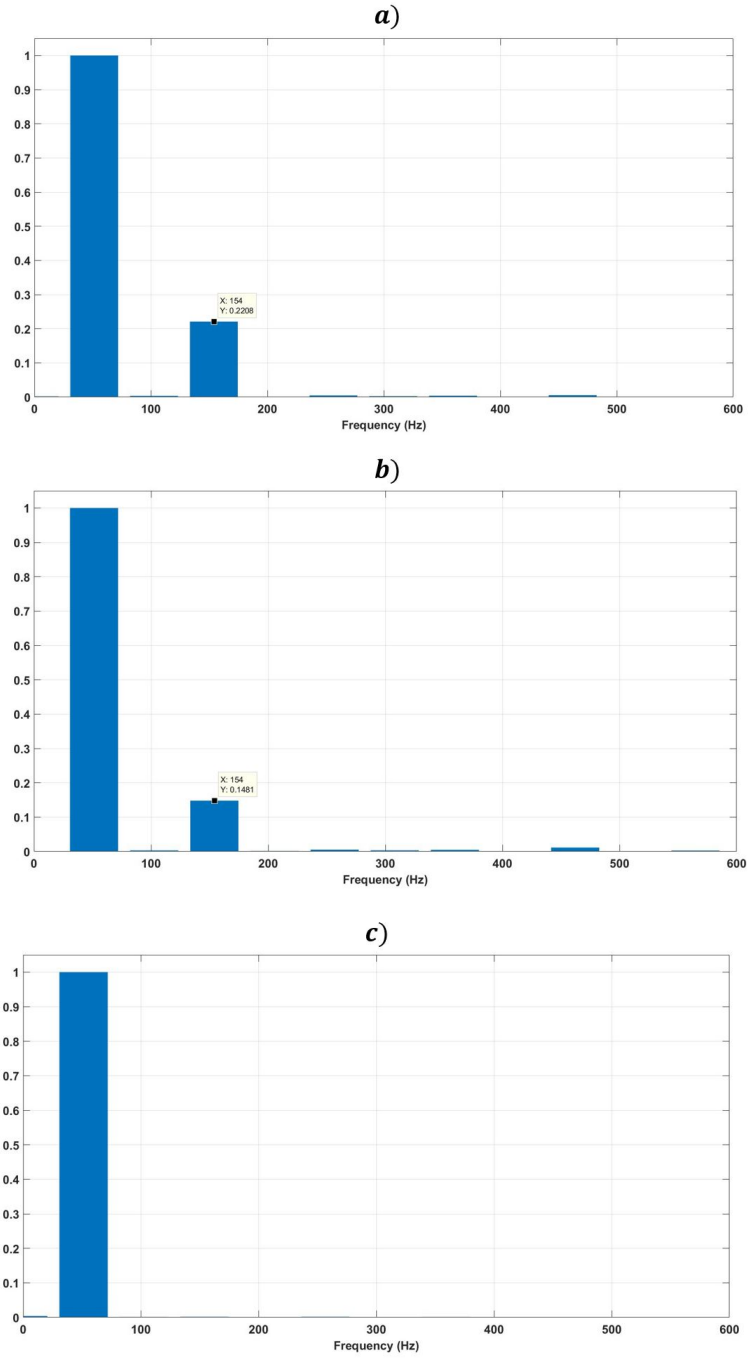


Figure 8.41: Phase current FFT. a) Standard PWM. b) ZSV elimination modulation. c) ZSV elimination modulation with DT hysteresis controller.

8.5 Experimental Results for the High-Speed Starter-Generator

In this section the experimental results for the high-speed starter-generator OEW-PMSM are proposed. Fig. 8.42 shows the experimental set-up used to verify the proposed modulation and controller. The high-speed starter-generator coupled with the load is shown in Fig. 8.42 a), while the 540 V dc power supply that feeds the dual-inverter dc link is presented in Fig. 8.42 b). The dc supply is also provided of an internal braking chopper that allows to work in regenerative mode. The same FPGA/DSP board previously used for the scaled down OEW rig has been used to drive the dual-inverter which feeds the starter-generator.

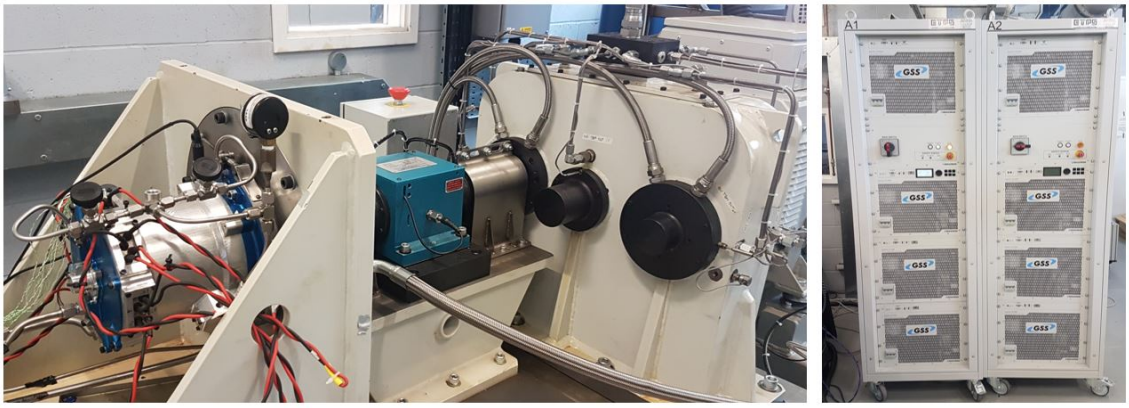


Figure 8.42: Experimental set-up for the high speed starter-generator: (a) High Speed PMSM coupled with load, (b) dc link power supply

Exactly the same procedure presented in Section 8.2.3 has been used to identify the electrical and mechanical parameters of the machine. The identification gave as output 1.444 $m\Omega$, 403 μH and 2.72 V for R_s, L_d and V_c. The same identification method for L_0 that has been used for the scaled-down OEWM has also been used for the high-speed starter generator obtaining a $80\mu H$ zero-sequence inductance. The

mechanical parameters identification instead led to the following values of 0.179548 As^2, 0.01171 As and 0.3822 A for J/k_t, B/k_t and D/k_t, respectively.

The performance of the machine could be tested only until 10 krpm due to mechanical limitations of the coupling between the machine and the load, in fact at the moment of the testing excessive mechanical vibrations did not allow to go beyond the 10 krpm. As it has been done for the scaled down OEW-PMSM, firstly the performance of the machine when both converters are modulated with a standard PWM are presented. Then the proposed SVPWM for the instantaneous elimination of the ZSV is applied in conjunction with the DT hysteresis controller.

8.5.1 High-speed Starter-Generator performance under Standard PWM

The individual VSCs that compose the dual-inverter used to drive the high-speed starter-generator are built around the IGBT and SiC technology respectively. When the standard PWM is used to control the converters different switching frequency must be adopted for the two VSIs. One VSC is switched at 10 kHz while the other at 40 kHz. Fig. 8.43 shows the phase current profiles, the zero sequence current and the q- and d- axis currents at 4 krpm. Observing Fig. 8.44, it can be noticed that the ZSV applied by the dual-inverter on the machine has exactly the same profile as the one previously shown in Fig. 8.17, with the difference that now the ZSV is much higher since the dc link is 540 V. The reduced ZSI and increased dc link voltage cause an high frequency, high intensity ZSC ripple which is not acceptable, leading to a flowing ZSC that reaches peaks of 70 A. Considering a rated current of 150 A, the ZSC ripple imposes a reduction in the maximum current that the machine can control in order to avoid the damage of the power modules. It is even more evident how the ZSV produced by the dual-inverter must be eliminated.

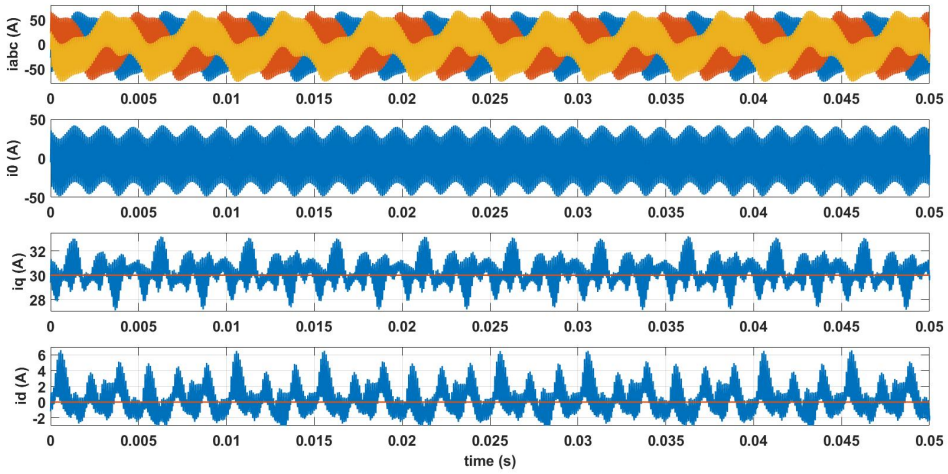


Figure 8.43: High-speed OEW-PMSM performance under standard PWM at 4 Krpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

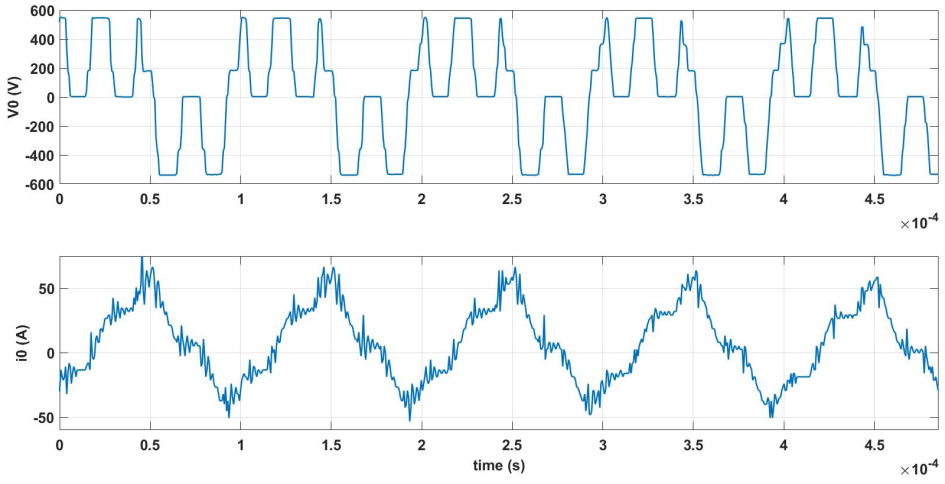


Figure 8.44: Detail of the ZSV and ZSC under standard PWM. Top: V_0^{OEW} ZSV. Bottom: ZSC i_0.

8.5.2 High-speed Starter-Generator performance under SVPWM for instantaneous ZSV Elimination

The performance of the OEW starter-generator under the proposed ZSV instantaneous elimination modulation are presented in Fig. 8.45. The ZSC is significantly reduced since no ZSV is applied on the machine from the dual-inverter.

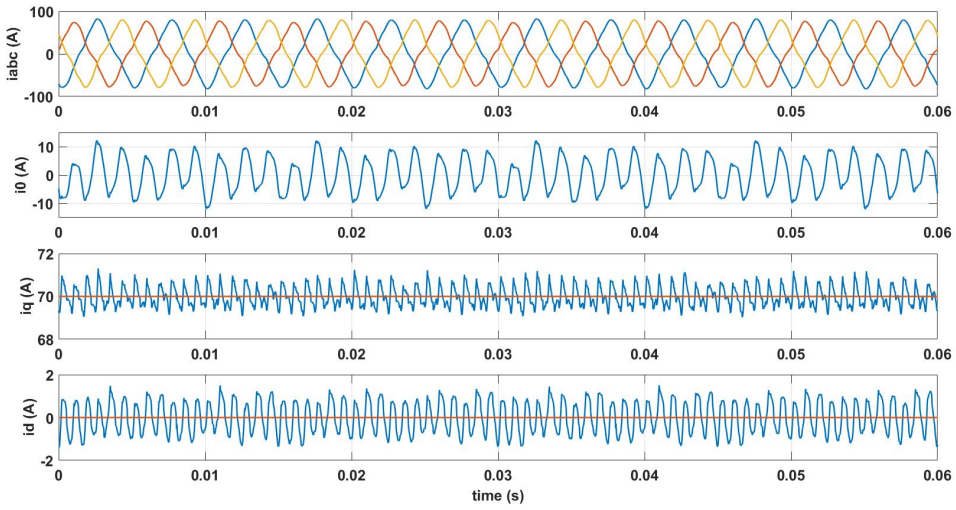


Figure 8.45: High-speed OEW-PMSM performance under ZSV elimination modulation at 4000 rpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current.

The individual VSCs voltages and the corresponding ZSVs when the proposed modulation is implemented are shown in Fig. 8.46. It can be noticed that the ZSV produced by the two VSCs have the expected square wave profile and are identical. Therefore the resulting ZSV applied on the machine is zero, apart from the voltage distortion introduced by the DT. The ZSV applied on the OEW machine, found as the sum of the phase voltages $V_{aa'}, V_{bb'}$ and $V_{cc'}$ divided three is shown in Fig. 8.47.

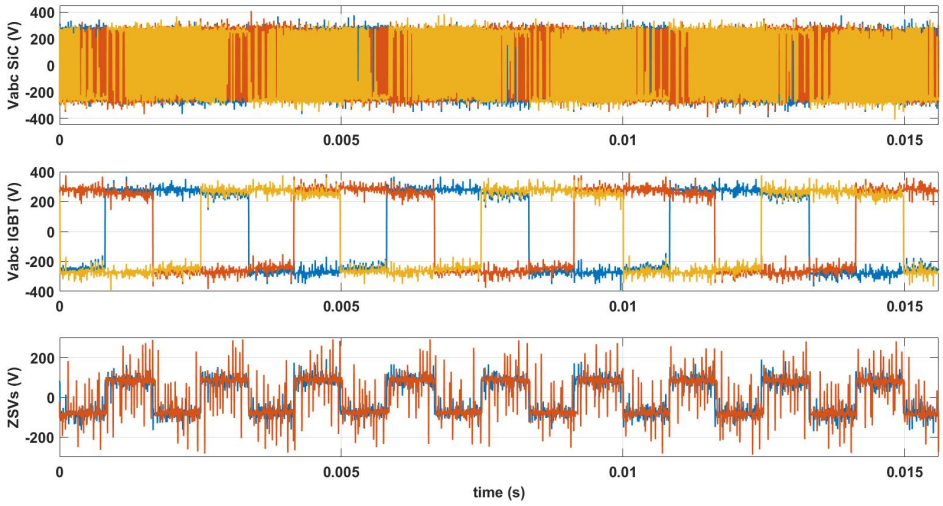


Figure 8.46: Dual-Inverter Voltages and ZSVs. Starting from top: V_{abc}^{SiC}, V_0^{SiC}, V_{abc}^{IGBT}, V_0^{IGBT}.

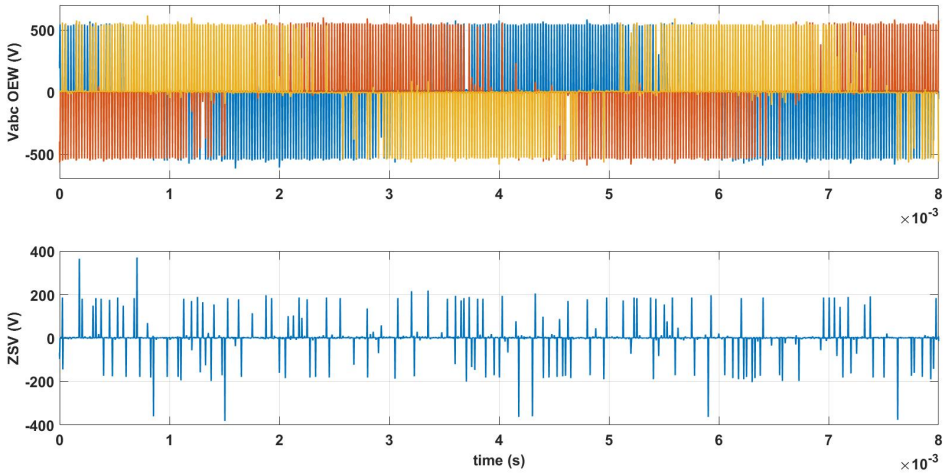


Figure 8.47: Dual-Inverter Voltages and ZSVs. Starting from top: V_{abc}^{SiC}, V_0^{SiC}, V_{abc}^{IGBT}, V_0^{IGBT}.

Finally the performance of the DT hysteresis controller are evaluated. The OEW-PMSM performance are tested under different operating speeds and changing the

ZSC DT hysteresis band to prove the effectiveness of the proposed method. Fig. 8.48 and 8.49 show the steady state performance of the starter-generator at the reference speed of 4 krpm with the DT hysteresis band set at 0 A and 4 A respectively.

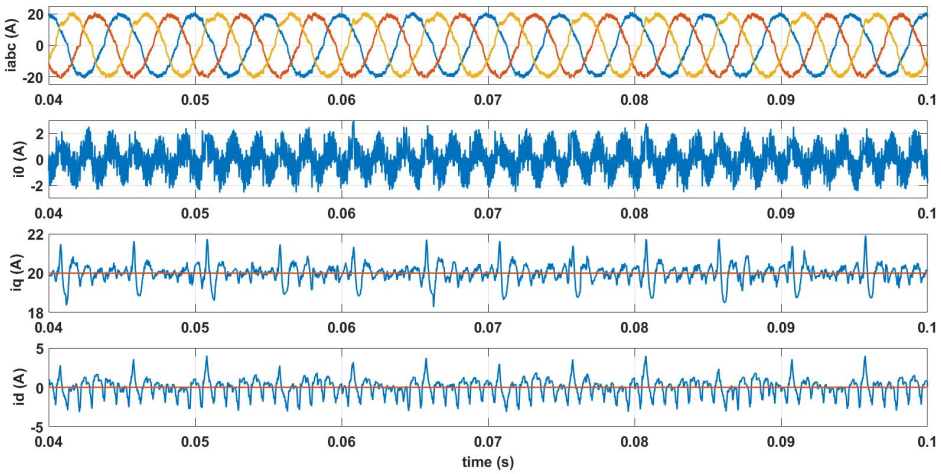


Figure 8.48: OEW-PMSM performance with the DT hysteresis controller at 4000 rpm. Starting from the top: phase currents, ZSC i_0, q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

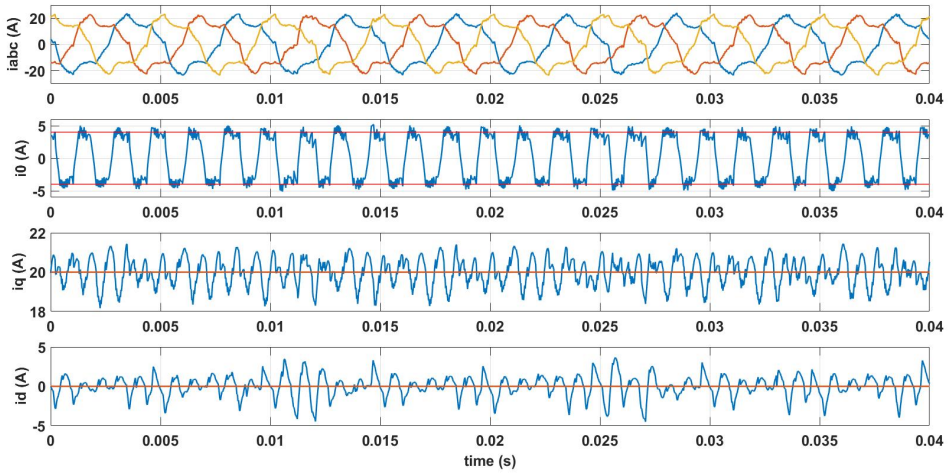


Figure 8.49: OEW-PMSM performance with the DT hysteresis controller at 4000 rpm. Hysteresis band set at 4 A. Starting from the top: phase currents, ZSC i_0 (blue) and reference i_0 band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

The possibility to vary the DT hysteresis band is shown in Fig. 8.50 and 8.51 where the band is in the first case incremented from 0 to 6 A while in the second case is reduced from 5.5 to 2 A. Fig. 8.52 shows the machine currents at 8000 rpm when the hysteresis ZSC band is set to 1 A while Fig. 8.53 shows the currents profiles when the ZSC band is set at 0 A and the machine is rotating at 10 krpm.

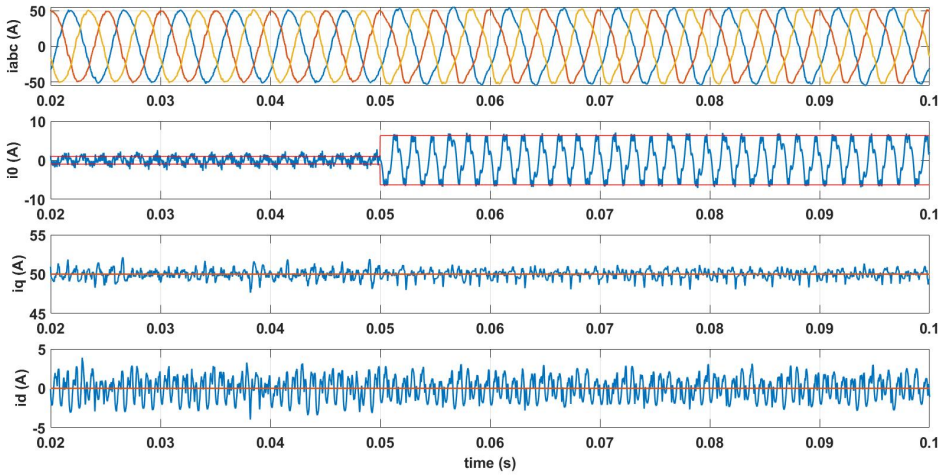


Figure 8.50: DT hysteresis band transient at 4000 rpm from 0 to 6 A. Starting from the top: phase currents, ZSC i_0 (blue) and reference i_0 band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

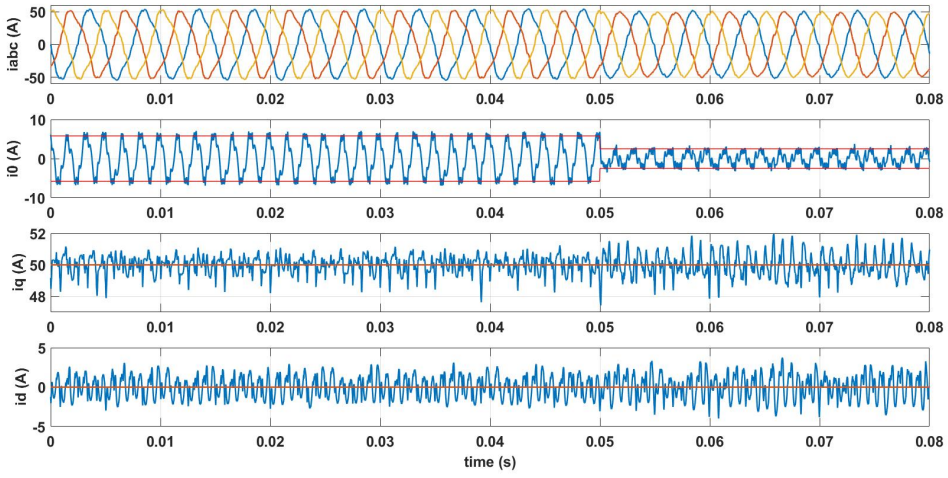


Figure 8.51: DT hysteresis band transient at 4000 rpm from 5.5 to 2 A. Starting from the top: phase currents, ZSC i_0 (blue) and reference i_0 band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

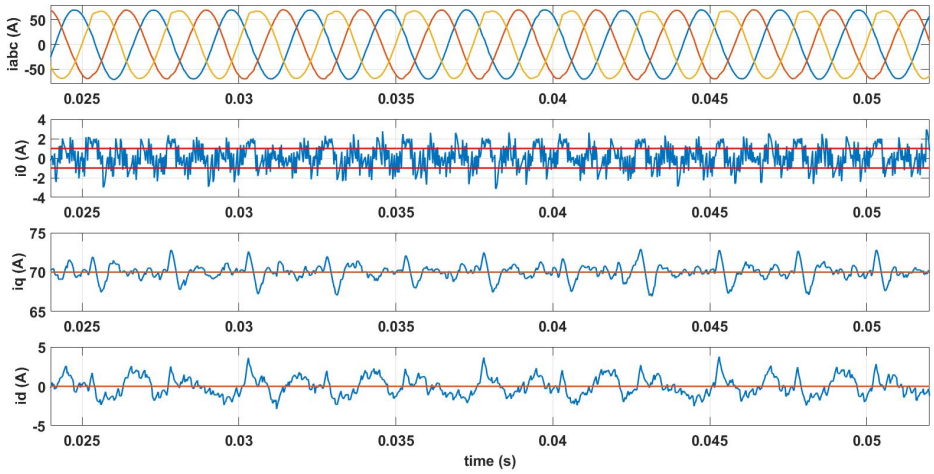


Figure 8.52: OEW-PMSM performance with the DT hysteresis controller at 8000 rpm. Hysteresis band set at 1 A. Starting from the top: phase currents, ZSC i_0 (blue) and reference i_0 band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

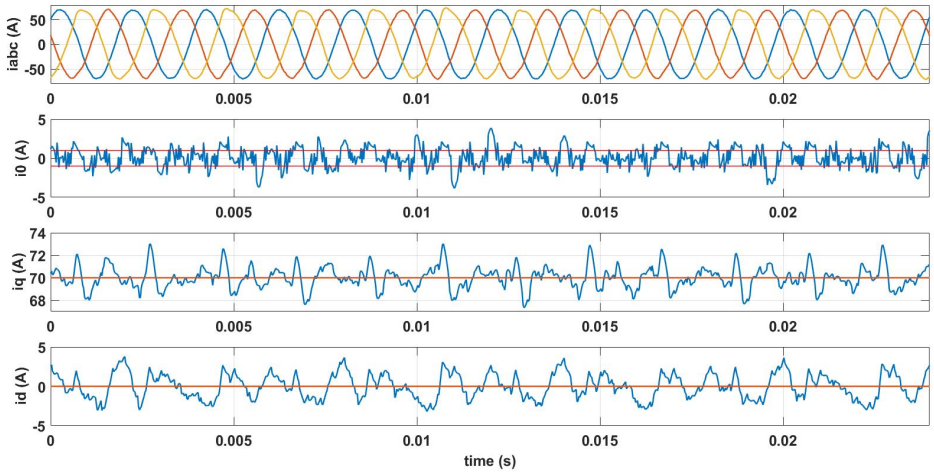


Figure 8.53: OEW-PMSM performance with the DT hysteresis controller at 10000 rpm. Hysteresis band set at 1 A. Starting from the top: phase currents, ZSC i_0 (blue) and reference i_0 band (red), q axis current i_q (blue) and reference current i_q^* (red), d axis current i_d (blue) and reference current i_d^* current (red).

8.5.3 THD and FFT measurements

In this section the phase current profile quality is evaluated by means of THD and FFT analysis. The comparison is made between the phase current profile when the ZSV elimination SVPWM is applied without the ZSC controller and the same modulation with the elimination of the ZSC. The case of the standard PWM is not considered given the significantly performance, which are not acceptable for the machine operation. The same machine operating point has been considered for the comparison: the starter-generator is operated in generating mode, it is run at 10 krpm with a load torque of 40% of the rated torque. Fig. 8.54 shows the phase currents profiles in blue while the ideal fundamental component in red. The THD obtained are 1.0510^{-1}, 4.7410^{-2} for the ZSV elimination modulation without DT hysteresis controller and the ZSV elimination modulation with DT hysteresis controller respectively.

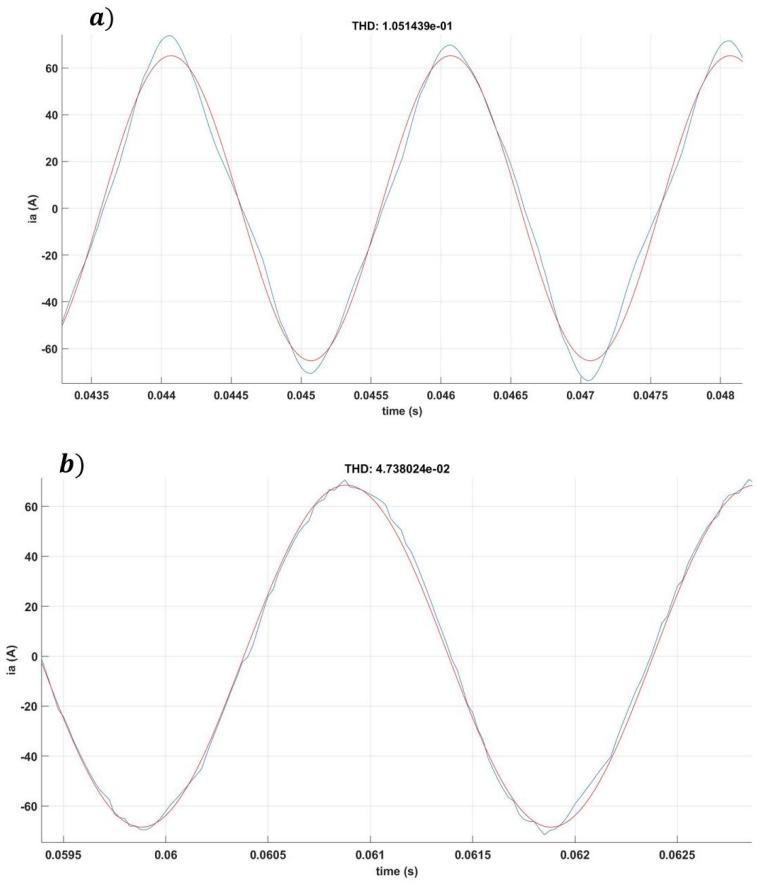


Figure 8.54: Phase current THD. a) ZSV elimination modulation. b) ZSV elimination modulation with DT hysteresis controller.

Under the same operating point of the machine that has been considered for the THD evaluation also an FFT of the phase current is performed to highlight the harmonic content. The current harmonics are normalised respect to the amplitude of the fundamental component. A speed of 10 krpm corresponds to a 500 Hz fundamental frequency while the third harmonic current has a frequency of 1.5 KHz. It can be noticed that the third harmonic is completely eliminated when the DT hysteresis controller is introduced, as shown in Fig. 8.55 b).

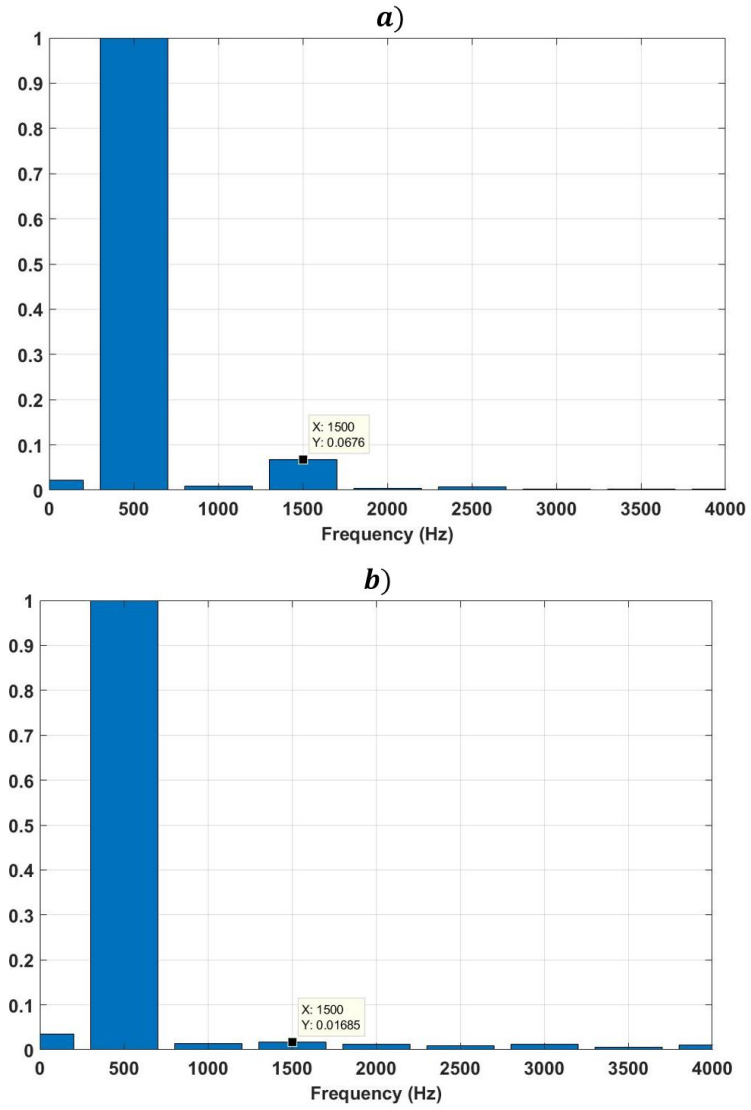


Figure 8.55: Phase current FFT. a) ZSV elimination modulation. b) ZSV elimination modulation with DT hysteresis controller.

8.6 Conclusions

This Chapter showed the experimental results obtained for the 1.5 kW OEW motor and for the high-speed starter-generator. At first the scaled-down OEW-PMSM test

rig is considered, a detailed description of the experimental set up has been provided. The identification method used to identify the main electrical parameters such as stator resistance and inductances is presented. The least square estimation method has been adopted to identify the inductance L_d together with the phase resistance R_s and voltage drop of the switches and diodes V_c. The $q-$axis inductance could not be identified at the time, hence this task is postponed to a future investigation. The same identification method has been used to evaluate the machine mechanical parameters. In the following section, the experimental results of the machine performance when both VSCs are controlled with a standard PWM are presented. It has been shown that the resulting ZSV, and consequently ZSC circulating, is not acceptable. Then the experimental results for the ZSV instantaneous elimination modulation are presented. The VSCs voltages profiles are shown, highlighting how the ZSVs profiles of the individual VSCs are identical, resulting in a zero ZSV applied on the machine. Furthermore a detail of the switching of the SiC-based VSC is given to better understand the behaviour of the voltage distortion introduced by the DT when the turn-on and turn-off of the power modules is considered. The effectiveness of the proposed DT hysteresis controller in eliminating the ZSC flowing due to the non-sinusoidal back-EMF of the machine is shown by testing the controller in different operating points of the machine. In order to evaluate the improvement obtained with the proposed modulation in conjunction with the DT hysteresis controller the phase current THD is computed and a FFT is carried out. In the last section the results for the high-speed starter-generator are presented. Similarly as it was done for the scaled-down OEWM the machine electrical and mechanical parameters are identified using the least square estimation technique. The machine is tested under both standard PWM modulation and the proposed ZSV elimination SVPWM. The results show that the standard PWM cannot be applied since it would result in a significant reduction of the maximum current that could be controlled or even in the harming of the power modules. The dual-inverter voltages are shown and the effectiveness of the ZSC hysteresis controller is validated through experimental results.

Chapter 9

Conclusions

9.1 Summary of Achievements and Conclusion

The first part of the PhD project dealt with the study of the state of the art of the existing modulations for ZSV reduction or elimination for both the standard 2-levels VSC and the dual-inverter topology. In particular, the dual-inverter with common dc link configuration has been investigated. The previously proposed modulations for the ZSV reduction for the dual-inverter with common dc link have been studied. Furthermore, initially the modelization and analysis of the PMSM electrical model has been carried out. The PMSM equations have been presented both in the abc coordinates and in the synchronous $qd0$ reference frame. The equations have been also rearranged in the state-space form and have been discretized to make them suitable for the digital controller synthesis. Then the mathematical model has been adapted to be used for the OEW configuration. From the abc representation of the machine equations in the OEW configuration, the equivalent electrical circuit has been obtained to be used for the numerical simulative analysis. The zero-sequence equivalent circuit of the machine has been studied and the equations, which describe its be-

haviour, have been presented.

The final goal of the PhD project was the development of a smart solution to exploit the different nature of the power modules devices of the dual-inverter used to control the OEW-PMSM high-speed starter-generator in conjunction with the elimination of the additional ZSC flowing in the system due to the common dc link connection adopted. The high-speed OEW-PMSM is characterised by extremely low inductances which result in a particularly low equivalent ZSI. Therefore the zero-sequence circuit is subject to fast dynamics when excited by a ZSV, which leads to the necessity to fully eliminate the ZSV produced by the dual-inverter. The dual-inverter selected to drive the high-speed OEWM is made of one 2-levels VSC built around IGBT technologies and the other VSC based on fast switching SiC devices. In order to exploit the different technologies used for the power modules of the two converters, a novel method of splitting the reference voltages among the two VSCs has been proposed. The IGBT converter is controlled in six-step mode while the reference voltage for the SiC one are chosen in order to have the sinusoidal reference voltages on the load. In this way the IGBT is switched at the fundamental frequency of rotation of the machine while the SiC converter is fast switching to compensate for the harmonic distortion introduced by the square wave controlled IGBT VSC. Furthermore a modulation for the fast switching VSC has been developed in order to instantaneously eliminate the ZSV produced by the dual-inverter. The solution adopted consists in using exclusively the space voltage vectors that give the same ZSV produced by the square wave modulated IGBT converter. In this way the ZSV profile generated by the SiC converter is identical to the one produced by the other VSC. To achieve such result the modulation developed for the SiC converter uses alternatively two groups of three active voltage vectors which generate the same ZSV. In this way the ZSV produced by the dual-inverter is eliminated significantly reducing the ZSC flowing.

Furthermore the effect of voltage distortion introduced by the power switches DT to avoid the leg short circuit on the ZSV has been investigated. The phenomenon has been studied for the particular modulation proposed observing that, according to the switch transition and phase current polarity the voltage distortion can assume both

positive and negative sign. The PBDTC method for the DT compensation has been adapted in order to be used in conjunction with the proposed three active vectors SVM. An hysteresis controller of the ZSC has been implemented thanks to the possibility to compensate or not the ZSV distortion introduced by the DT, in this way the ZSC produced by the non-sinusoidal back-EMF of the machine can be eliminated. To verify the system performance a simple digital current controller based on the state feedback approach has been developed as well as an external speed controller based on a speed and load torque disturbance observer to generate the necessary machine torque reference. An experimental set-up has been built to corroborate the theoretical predictions. At first, since the high-speed starter-generator was still not available, a scaled-down OEWM has been used to validate the proposed modulation strategy for the dual-inverter. The machine has been tested under both the standard PWM and the proposed SVPWM for the instantaneous ZSV elimination. The experimental results obtained confirm the better performance that can be achieved with the proposed modulation and the effectiveness of the DT hysteresis controller in eliminating the ZSC flowing due to the non-sinusoidal back-EMF of the machine. Only towards the end of the PhD the high-speed OEWM was available to be tested. The experimental results show the expected behaviour under the standard PWM which results in an unacceptable ZSC flowing into the system. The proposed modulation and the DT hysteresis controller have been tested confirming the same results obtained on the scaled-down OEWM.
The PhD project achievements can be summarized as follow:

- Full characterization of the analytical model of the OEW-PMSM in terms voltage equations.
- Development of a novel SVPWM for the instantaneous elimination of the ZSV produced by the dual-inverter.
- Suppression of the ZSV produced by the mixed technology dual-inverter.

- Elimination of the ZSC flowing due to the non-sinusoidal back-EMF of the machine by means of the novel DT hysteresis controller.
- Synthesis and tuning of the current and speed controllers.
- Implementation of the DSP/FPGA controllers and validation of the proposed methods.

9.2 Future Work

A list of tasks for future works that have been identified as promising and challenging is given as follows:

- Additional experimental tests for the high-speed starter-generator OEWM need to be carried out. In particular the procedure of cranking has to be performed as well as the rated speed operation.
- Until now the modulation proposed does not take into account the order in which the three active vectors are applied. The analysis of possible optimal patterns in the order of application of the three active voltage vectors can be studied. In particular the vectors order of application and its effect on the phase currents THD need to be evaluated. When applying the three vectors so far, it has not been considered to split their dwelling time, this would result in additional switching losses, but it could possibly lead to an improvement of the phase current profile.
- The whole analysis of the effect of the DT distortion introduced on the ZSV has been carried out supposing to have ideal switches. Therefore their turn-on and turn-off time have not been considered. The experimental results have shown how the dependency of the turn-on and turn-off times from the phase

current amplitude significantly affects the distortion introduced on the ZSV by the DT. Better performance could be achieved if the compensation time would be considered a variable, instead of a constant equal to the VSC DT. In order to do so, a complete characterization of the power modules has to be carried out. The turn-on and turn-off have to be mapped according to the amplitude of the current flowing. Then, by means of look-up tables, this the actual turn-on and turn-off times could be used to compensate the DT instead of considering it a constant quantity.

- The SiC VSC is actually able to switch at higher switching frequencies than 40 KHz. As a continuation of the work done in [34], a more in depth analysis of the dual-inverter losses and the phase current THD dependency from the switching frequency needs to be carried out. The higher is the phase current THD, the higher will be the harmonic content of the stator currents, resulting in increased losses in the machine. On the other hand, lower THD corresponding to higher switching frequency would result in lower losses in the machine and higher switching losses in the dual-inverter. Treating the system composed by the machine and the dual-inverter as a whole it would be interesting developing a control strategy that would take into account the losses of the drive and change the switching frequency according to the operating point of the OEWM to minimize the entire losses.

- Because of the higher power density, reduced costs and space that can be achieved with the single dc link configuration, the other dc link topologies have not been taken into account. Both for the aerospace and automotive applications the OEWM has attracted attention from the academic and industrial world but a detailed comparison of the pros and cons of the different dc link configurations for the dual-inverter depending from the application is missing in the literature.

- Sensorless control of machines is more and more an appealing feature since it gives the possibility of avoiding the installation of a position sensor resulting

in the elimination of a fragile component from the system and in a significant reduction of the overall drive cost and size. Therefore attention to the development of sensorless techniques that could be adapted to the dual-inverter OEWM topology could be given.

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Appendix A

Reference-Frame

The synchronous motor inductances are function of the rotor position, whereupon the coefficients of the differential equations (voltage equations) that describe the behaviour of this machine are time varying except when the rotor is stalled. A change of variables is often used to reduce the complexity of these differential equations. There are several changes of variables that are used but all these can be contained in one, this general transformation refers machine variables to a frame of reference that rotates at an arbitrary angular velocity. All known real transformations are obtained from this transformation by simply assigning the speed of the rotation of the reference frame. The reference-frame used in this work is here presented.

A change of variables that formulates a transformation of the 3-phase variables of stationary circuit elements to the arbitrary reference frame may be expressed as

$$f_{qd0} = \mathbf{T}_P(\vartheta_e) f_{abc} \tag{A.1}$$

where

$$f_{qd0} = \begin{bmatrix} f_q \\ f_d \\ f_0 \end{bmatrix} \; ; \; f_{abc} = \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{A.2}$$

$$\mathbf{T}_P(\vartheta_e) = \frac{2}{3} \begin{bmatrix} \cos(\vartheta_e) & \cos(\vartheta_e - 2\pi/3) & \cos(\vartheta_e - 4\pi/3) \\ \sin(\vartheta_e) & \sin(\vartheta_e - 2\pi/3) & \sin(\vartheta_e - 4\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{A.3}$$

$$\omega = \frac{d\theta}{dt} \tag{A.4}$$

It can be shown that for the inverse transformation we have

$$\mathbf{T}_P^{-1}(\vartheta_e) = \begin{bmatrix} \cos(\vartheta_e) & \sin(\vartheta_e) & 1 \\ \cos(\vartheta_e - 2\pi/3) & \sin(\vartheta_e - 2\pi/3) & 1 \\ \cos(\vartheta_e - 4\pi/3) & \sin(\vartheta_e - 4\pi/3) & 1 \end{bmatrix} \tag{A.5}$$

The relationship between the angular velocity and the angular displacement θ is expressed by (A.4), but can also be written in the definite integral form as

$$\theta = \int_0^t \omega(\xi) d\xi + \theta(0) \tag{A.6}$$

Where ξ is a dummy variable of integration.

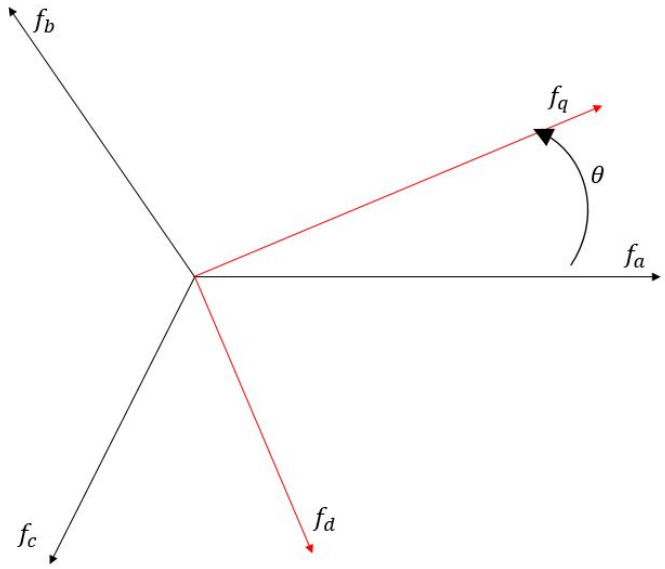


Figure A.1: qd0 reference frame transformation.

In the above equations f can represent either voltage, current or flux linkage. The angular displacement θ must be continuous, however the angular velocity associated with the change of variables is unspecified. The frame of reference may rotate at any constant or varying angular speed or it may remain stationary. The stationary reference frame, often referred as the $\alpha\beta 0$ reference frame can be obtained from the synchronous one of (A.3) by setting the rotor electrical position ϑ_e to 0. The matrix that allows to transform the phase variables into the stationary reference frame is shown in (A.7).

$$\mathbf{T}_P(0) = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_{aa'} \\ V_{bb'} \\ V_{cc'} \end{bmatrix} \tag{A.7}$$

The connotation of the arbitrary reference frame is that the angular velocity of the

transformation is unspecified and can be selected arbitrarily to expedite the solution of the system equations or to satisfy the system constraints. The change of variables may be applied to variables of any waveform and time sequence, however it is well known that is best suited for an abc sequence. Although the transformation to the arbitrary reference frame is a change of variables and needs no physical connotation, it is often convenient to visualize the transformation equations as trigonometric relationships between variables as shown in Fig. A.1. In particular, the equations of transformation may be thought of as if the f_q and f_d variables are directed along paths orthogonal to each other and rotating at an angular velocity of ω, whereupon f_a, f_b and f_c may be considered as variables directed along stationary paths, each displaced by 120. If f_a, f_b and f_c are resolved into f_q the first row of eq. (A.3) is obtained; and if f_a, f_b and f_c are resolved into f_d the second row is obtained. It is important to note that f_0 variables are not associated with the arbitrary reference frame. Instead, the zero variables are related arithmetically to the abc variables, independent of θ. It is also important not to confuse f_a, f_b and f_c with phasors. They are instantaneous quantities that may be any function of time. Portraying the transformations as shown in Fig. A.1 is particularly convenient when applying it to ac machines where the directions of f_a, f_b and f_c may also be thought of as the direction of the magnetic axes of the stator windings. The directions of f_q and f_d can be considered as the direction of the magnetic axes of the new windings created by the change of variables. The total instantaneous power may be expressed in abc variables as

$$P_{abc} = v_a i_a + v_b i_b + v_c i_c \tag{A.8}$$

The total power expressed in the qd0 variables must equal the total power expressed in the abc variables, hence substituting equation 1.3.1 in 1.3.7 we obtain

$$P_{qd0} = \frac{3}{2}(v_q i_q + v_d i_d) + 3 v_0 i_0 \tag{A.9}$$

Appendix B

State Space Representation of Dynamic Systems

A generic mathematical or physical system can be represented as a set of differential equations with a finite number of inputs, outputs and state variables related by differential equations. This representation is the well known state-space representation here proposed in (B.1).

$$\begin{cases} \frac{d}{dt}x(t) = f(x,u,t); \\ y(t) = g(x,u,t); \end{cases} \tag{B.1}$$

Where u is the mx1 array of the inputs, y is the qx1 array of the outputs, x is the nx1 array of the n state variables and t is the time variable. The functions f and g are generic functions of the state variables x, of the time and the inputs u. If the dynamic system is also linear then the differential equations and algebraic equations can be written in matrix form as shown in (B.2).

$$\begin{cases} \frac{d}{dt}x(t) = A(t)x(t) + B(t)u(t); \\ y(t) = C(t)x(t) + D(t)u(t); \end{cases} \tag{B.2}$$

If the matrices A, B, C and D are constant, i.e. the system parameters are time-invariant, the system is called stationary. Fig. B.1 shows a block diagram representation of (B.2)

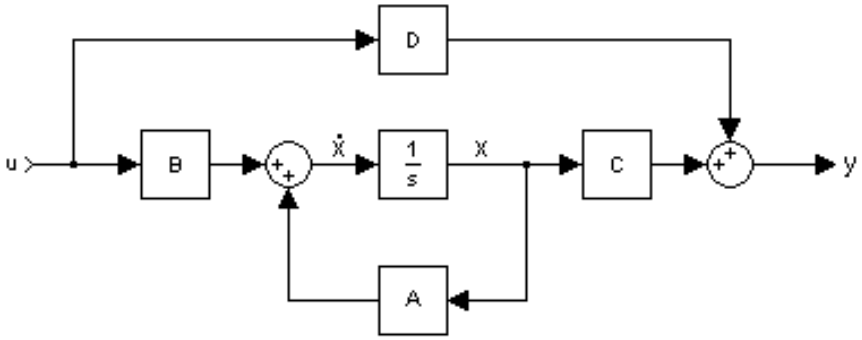


Figure B.1: Block diagram representation of the state space equation.

As previously shown, a generic mathematical system of differential and algebraic equations can be written in the form (B.2). The solution of such a system of differential equations is

$$x(t) = e^{A(t-t_0)}x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)}Bu(\tau)d\tau; \tag{B.3}$$

Now the solution is rewritten over one sample period $T_s$to obtain a difference equation

$$x(kT + T_s) = e^{AT_s}x(kT_s) + \int_{0}^{T_s} e^{A\tau}d\tau Bu(kT_s); \tag{B.4}$$

where

$$\begin{cases} \Phi = e^{AT_s} \\ \Gamma = \int_0^{T_s} e^{A\tau} d\tau B \end{cases} \tag{B.5}$$

(B.4) and (B.5) can be reduced to difference equations in a standard form

$$\begin{cases} x(k+1) = \Phi x(k) + \Gamma u(k) \\ y(k) = Hx(k) \end{cases} \tag{B.6}$$

Appendix C

Published Papers

The following papers were published during the PhD period:

L. Rovere, A. Formentini, G. L. Calzo, P. Zanchetta and T. Cox, "IGBT-SiC dual fed open end winding PMSM drive," 2017 IEEE International Electric Machines and Drives Conference (IEMDC), Miami, FL, 2017, pp. 1-7. doi: 10.1109/IEMDC.2017.8002155

L. Rovere, A. Formentini, G. Lo Calzo, P. Zanchetta and T. Cox, "Zero-Sequence Voltage Elimination for Dual Fed Common dc-link Open-End Winding PMSM High Speed Starter-Generator, Part I: Modulation," in IEEE Transactions on Industry Applications. doi: 10.1109/TIA.2019.2907073

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A. Amerise, L. Rovere, A. Formentini, M. Mengoni, L. Zarri and P. Zanchetta, "Control System for Open-End Winding Surface PM Synchronous Machines with a

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N. Hunter, T. Cox, P. Zanchetta, S. A. Odhano and L. Rovere, "Non-Intrusive Online Stator Temperature Estimation for Open-End Winding PMSM," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 6845-6851. doi: 10.1109/ECCE.2018.8558475

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L. Rovere, A. Formentini, A. Gaeta, P. Zanchetta and M. Marchesoni, "Sensorless Finite-Control Set Model Predictive Control for IPMSM Drives," in IEEE Transactions on Industrial Electronics, vol. 63, no. 9, pp. 5921-5931, Sept. 2016. doi: 10.1109/TIE.2016.2578281

R. Leuzzi, V. G. Monopoli, L. Rovere, F. Cupertino and P. Zanchetta, "Effects of Electrical Ageing on Winding Insulation in High-Speed Motors: Analysis and Mod-

elling," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 6886-6892. doi: 10.1109/ECCE.2018.8558376