University Of Nottingham

Single phase grid connected power converter topologies with power pulsation compensation

Author:

Davide Gottardo

Supervisors:

Dr. Liliana De Lillo

Dr. Lee Empringham

Dr. Alessandro Costabeber

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Abstract

Following the ever increasing penetration of grid connected distributed generation, EVs battery chargers, and distributed energy storage systems, the requirement for power converter having rated power ranging from 1 to 15kW is rising.

In order to facilitate the introduction of power converters in residential application, including single-phase systems, high power density is desirable, as long as it does not have significant negative impact on cost and reliability.

The topic of this work is the implementation of new topologies for single phase AC-DC systems. In the first part of the work, a literature review of existing solutions is presented, with focus on active ripple power decoupling and leakage current elimination in transformerless PV systems. Two converter topologies, the Double-Full-Bridge Converter (DFBC) and the Jumping-Capacitor Converter (JCC) are proposed, both able to achieve active ripple power cancellation using the concept of ripple port. The JCC particularly suitable for use as transformerless PV converter, thanks to its leakage currents filtering capability.

A new modulation technique capable of achieving zero voltage switching without the need for resonating LC circuits is proposed. The modulation takes advantage of the mutual coupling between the magnetic elements of different fundamental cells in order to shape the current ripple waveforms, achieving ZVS with a low ripple amplitude. The technique can be applied to the proposed topologies but also on many other topologies.

The proposed solutions are validated by simulations and experimental results.

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List of terms

DC	-	Direct current
AC	-	Alternated Current
PV	-	Photovoltaic
RMS	-	Root Mean Square
EMI	-	Electromagnetic Interference
DFBC	-	Double Full Bridge Converter
LFB	-	Low Frequency Bridge
HFB	-	High Frequency Bridge
PWM	-	Pulse Width Modulation
MIMO	-	Multi-Input-Multi-Output
SISO	-	Single-Input-Single-Output
MTTP	-	Maximum power point tracking
PI	-	Proportional Integral
PR	-	Proportional Resonant
SiC	-	Silicon Carbide
GaN	-	Gallium Nitride
FET	-	Field Effect Transistor
JCC	-	Jumping Capacitor Converter
FOM	-	Figure Of Merit
PFC	-	Power Factor Corrector
PWM	-	Pulse Width Modulation
DCM	-	Discontinuous Current Mode
ZCS	-	Zero Current Switching
ZVS	-	Zero Voltage Switching
TCM	-	Triangular Current Mode
eTCM	-	extended Triangular Current Mode
SeTCM	-	Simplified extended Triangular Current Mode
μCU	-	Microcontroller
DSP	-	Digital signal processor
CPU	-	Central Processing Unit

Nomenclature

P	-	Active power
Q	-	Reactive power
S	-	Apparent power
$P_R(t)$	-	Ripple power
ω	-	AC pulsation
f	-	AC frequency
E_R	-	Ripple energy
$\|x(t)\|_0$	-	Mean value of x(t)
$\|x(t)\|_1$	-	Fundamental component of x(t)
$\dot{X}$	-	Phasor
R_V	-	DC voltage utilization ratio
R_{E_C}	-	Energy utilization ratio
δX	-	Peak-to-Peak amplitude of X
d	-	Duty Cycle
$\tilde{X}$	-	Small signal value of X
$X^*(t)$	-	Low frequency component of X
$\hat{X}(t)$	-	Ripple component of X
$\hat{X}^+_{max}$	-	Maximum positive value of $\hat{X}(t)$ in a switching period
$\hat{X}^-_{min}$	-	Minimum negative value of $\hat{X}(t)$ in a switching period
$\mathcal{L}$	-	Inductance matrix
Γ	-	Inverse inductance matrix
l	-	Normalized inductance matrix
k_M	-	Mutual coupling coefficient
τ	-	Inductor ratio
δ	-	Phase shift
E_L	-	Maximum magnetic energy

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Chapter 1

Introduction

The last decade has been characterized by a fast rise in the penetration of distributed generation in the grid. According to the International Energy Agency, the installed power for distributed solar generation will increase worldwide by more than 300GW over the next six years [12].

Another sector that is growing rapidly is that of electrical vehicles (EV). EVs are considered to constitute an effective strategy in the reduction of dependence on fossil fuels, and consequently of emissions. In order to supply the EVs, a widespread availability of grid connected battery chargers is required [13, 14].

All those appliances exchange power through a DC connection, and have to be interfaced with the grid, therefore, to enable power transfer to the grid, a DC-AC converter is required. This converter require unidirectional power transfer, either from the DC port to the grid (as is the case for PV systems), or from the grid to DC, as is the case for battery chargers [15]. In other cases, the required power transfer capability can be bidirectional, for example in order to interface DC micro-grids to the AC grid, where the latter contain both loads and generators, or to interface distributed storage systems with the grid.

In order to cope with the intermittent nature of renewables, and to deal with residential power surges in a more efficient and cost-effective way, there is an interest in the development of distributed energy storage systems [16]. Another interesting application, regarding battery chargers, is the possibility to use EV

batteries to achieve the same benefits (the so-called Vehicle-to-Grid systems) [17, 18]. In this case, EV battery chargers have to be bidirectional as well.

When high levels of power are required, three phase connections are preferable, as single phase connections pose a number of challenges, both for the grid and the converter: an high power load/generator exchanging power through a single phase can lead to significant unbalance in the grid currents, that causes current stress on the neutral connection, can result in voltage unbalances, and may lead to the saturation of the MV-LV transformer [19]. For the converter, a single phase AC connection poses a problem, as the power exchanged through single phase systems is inherently pulsating, while the power exchanged through the DC port is continuous. This involves the need for a energy storage capable element in the converter, able to provide ripple power decoupling.

Despite those problems, three phase grid connection is often not available at low voltage [20], since in many countries low voltage distribution for residential installation is single phase with neutral, therefore, it is reasonable to expect a growing demand for single phase AC-DC converters in the near future.

To facilitate the introduction of AC-DC converters in residential applications, those characteristics are desirable:

- low cost;
- high reliability;
- high efficiency;
- high power density.

The requirements for high efficiency and high power density are concordant, since in order to achieve high power density, high efficiency is required, as heat-removal components are typically bulky; on the other hand, finding a balance between efficiency, reliability and costs is a design choice. Reliability is particularly relevant, considering the expected lifetime of the application in which those devices have to operate: for PV systems, for example, the expected working life can exceed 20 years [21].

Considerable research effort has been carried on in order to reach high levels of power density. An important contribution to this effort was the Little Box Challenge, a competition sponsored by Google and IEEE, that took place in 2015, whose target was the development of a single phase AC-DC converter having a power density higher than 3kW/dm^3 (>50W/in^3) [22]. Many of the participants managed to achieve this ratings making use of new materials for passive components and wide band gap semiconductors as active switching devices.

While improvements in terms of power density were significant, to meet these levels of power density those converters make use of very expensive materials and manufacturing techniques, making them unsuitable for commercial applications.

For this reason, further research is required to contain costs and improve the reliability of the converters, in order to bridge the gap between research prototypes and commercially viable products.

1.1 Objectives of the PhD project

The objective of this PhD project is the introduction of new topologies for single phase AC/DC converters.

To identify the challenges faced by single phase AC/DC converters, in order to find room for potential improvement, an extensive literature review was carried on. The main area for improvement that was identified is the minimization in size of the converter passives, to achieve better power density and lower costs.

Grid connected converter must comply with norms, defining, among other things, the quality of the current injected in the grid. For this reason, suitable filters must be present on the AC port of the converter. Since those filters contribute significatively to increase the cost and reduce the energy density of the converter, significative research effort is targeted to their minimization, both in terms of cost and physical size [23]. A convenient way to reduce the AC current ripple is to design the converter to have an high DC utilization ratio, and-or use LCL filters instead of simple inductors.

Another area for improvement is related to the necessity of integrating one

or more power decoupling elements in the converter, to cope with the pulsating nature of power transmitted through a single phase AC connection. The use of active power decoupling solutions enable the use of smaller-more reliable capacitors for power ripple decoupling.

Regarding PV systems, in the countries where galvanic isolation between the AC and DC port is not mandatory, it is possible to remove the transformer stage, increasing efficiency and reducing costs. To be able to do so, however, good filtering of leakage currents is required, ideally without the need for additional CM filters.

Those considerations are justified and discussed in detail in the first three chapters of this work.

Two new topologies are proposed in this work, the Double Full Bridge Converter (DFBC) and the Jumping Capacitor Converter (JCC). Both topologies use wide band-gap devices, in conjunction with LCL AC filters, and are capable of active power ripple decoupling. Both topologies are capable of bidirectional power transfer, however, the DFBC requires only two active switching devices if used for unidirectional power transfer from the grid to the DC, for this reason, its application is suitable for battery chargers. On the other hand, the JCC is capable of filtering leakage currents, for this reason, it is particularly suitable for use in transformerless PV systems.

In addition to the proposed topologies, a new modulation technique capable of achieving partial soft switching is introduced. While this technique can be applied to the proposed topologies, it can be used in many different topologies as well. For this reason, it is presented in a generalized form.

1.2 Chapter summary

The thesis is organized as follows.

In Chapter 2, a literature review regarding the state of the art topologies for single phase grid front-end is introduced.

In Chapter 3, a theoretical analysis of the power balance of a generic single

phase AC-DC converter is discussed, focusing on the use of the ripple port concept and the use of capacitors as power decoupling element.

In Chapter 4, an analysis of leakage currents occurring in transformerless AC-DC converters for PV application is discussed.

In Chapter 5 and 6, two novel topologies, named Double Full Bridge Converter (DFBC) and Jumping Capacitor Converter (JCC) are introduced and analysed.

In Chapter 7, a new modulation strategy, named extended Triangular Current Mode (eTCM), is introduced, and compared with the well-known Triangular Current Mode.

In Chapter 8, a simplified implementation of eTCM is implemented in the proposed JCC converter.

In Chapter 9, the experimental results concerning the two novel topologies and the SeTCM modulation technique are shown, together with the description of the hardware setup used to obtain them.

Finally, Chapter 10 summarises the achievements of this PhD project, including tasks for future work.

Chapter 2

Single phase AC front-end

Single phase AC front-end are the part of a system dedicated to the exchange of electric power via a single phase AC connection.

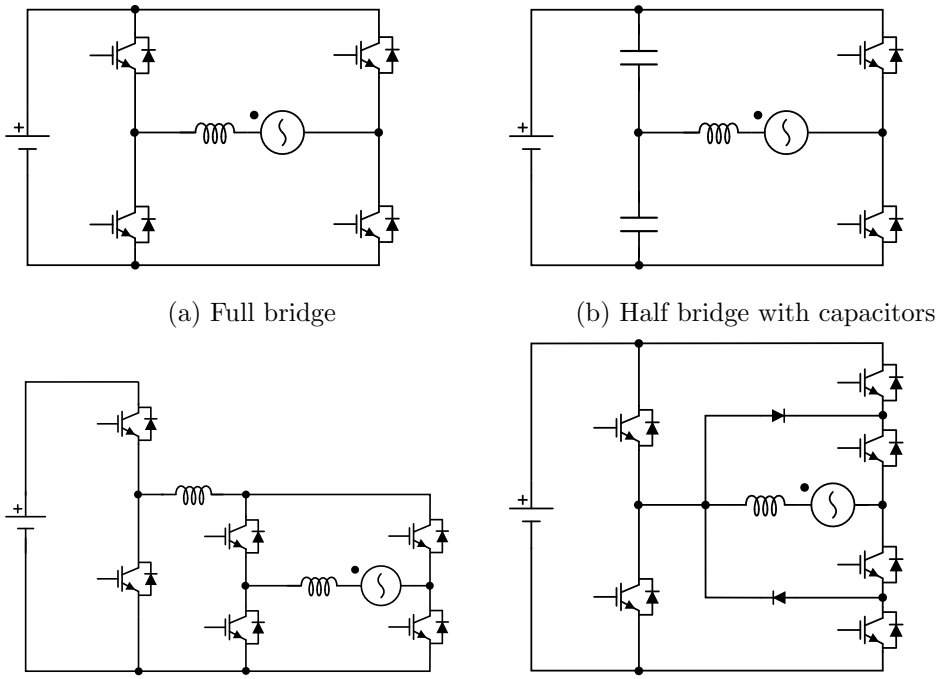
Several topologies are capable of performing this task, some of the most used are the following:

- full bridge;
- half bridge with recirculating capacitors;
- half bridge with unfolder-rectifier;
- neutral point clamp converters.

Full bridge converters are the most widely used topologies for grid front-end, due to their simple structure and control.

An alternative of the full bridge is shown in Fig.2.1b, where one half bridge is substituted by two capacitors. This solution has the advantage of requiring less active devices, and of preventing the injection of DC currents in the AC port. The big disadvantage of this solution lies in the size of the required capacitors, that have to absorb the AC current without their mid-point voltage drifting considerably from $V_{DC}/2$, to avoid overmodulation of the half bridge.

Another possibility is the use of a unfolder-rectifier stage, operated at grid frequency, cascaded with an half bridge switched at high frequency. The advantage of this kind of solution is the requirement of a reduced number of controlled active



(a) Full bridge

(b) Half bridge with capacitors

(c) Unfolder-rectifier

(d) NPC

Figure 2.1: Single phase AC front-end: common solutions

devices, especially if unidirectional power transfer from the AC to the DC port is required. The disadvantage is the reduced efficiency, due to the conduction losses in the unfolder-rectifier stage.

Neutral point clamp converters (NPC) have the capability of generating three voltage levels [24]. This translates in a reduced voltage ripple, and therefore the requirement of a smaller inductor to obtain a sufficient current ripple limitation. The downsides are the need for a higher number of active switching devices.

Many other solutions for single phase grid front-end are known in literature, however, an in-depth analysis of a large number of topologies is beyond the scope of this section, that is focused on the most common solutions. All the topologies described in wider detail in Section 2.4 are based on one of the configurations listed here, with some modifications, that allow active ripple power cancellation, an important feature that is described in the following Section.

2.1 Active ripple power cancellation

Single phase AC connections are characterized by the pulsating nature of the transferred power: in the assumption of current and voltage being sinusoidal and in phase, the instantaneous power, being the product of the two, is a sinusoid at double the AC frequency having an amplitude equal to its mean value. Assuming constant current to flow through the DC port, it follows, from the energy balance of the converter, that the AC ripple power has to be absorbed in the converter itself by one or more energy storage capable elements [1, 7].

Usually, this task is taken care of by a DC link capacitor. In order for the capacitor to exchange energy, its voltage cannot be constant, therefore, using this solution, a voltage ripple is present on the DC port of the converter. This voltage ripple is inversely proportional to the DC link capacitance; for this reason, a big capacitance is often required.

To limit size and cost, this solution often forces the use of electrolytic capacitors, that have the advantage of being cheap and energy-dense, but have poor reliability, making their utilization undesired in applications having a long operating life, such as PV systems [25].

To address this problem, a solution is to use an auxiliary part of the converter, able to independently control the voltage applied to a capacitor, in order to fully exploit its energy storage capability. Since the required capacitance in this case is much lower, other kind of capacitors can be used, such as film capacitors, which inherently exhibit longer life compared to electrolytic capacitors.

This solution offers a relevant improvement in terms of power density of the converter, at the price of an increased complexity and higher losses. The complexity is increased both in terms of control [26, 27] and/or increased number of active devices in the converter.

Several topologies make use of the ripple port concept [28, 29]. Some of them are described and compared in section 2.4.

An analytical study of the ripple power decoupling is presented in Chapter 3.

2.2 Leakage currents in PV inverters

Traditionally, PV systems make use of a transformer in the converter stage, having the advantage of providing galvanic isolation between the panels and the grid, and to increase the DC voltage obtained by the panels by an opportune choice of the turns ratio.

The use of a transformer, however, poses some disadvantages: because of the additional transformer stage, the converter has additional complexity, reduced reliability and higher losses. For these reasons, significative research effort is made in the development of transformerless converters.

Transformerless converters face the following challenges:

- galvanic isolation between the panels and the grid is mandatory in some countries;
- sufficiently high voltage levels has to be reached for the correct operation of the AC front end stage of the converter;
- due to the stray capacitance between the active parts of the PV panels and its chassis, which is connected to ground, a significant circulation of currents trough the ground can occur if a common mode voltage is applied between the DC and the AC port of the converter.

The required voltage gain can be achieved by series connection of a sufficient number of panels, or by a boost stage.

Extensive research addresses the issue of ground currents limitation [30]. The main methods used to achieve it are:

- reduction of common mode voltages via a CM filter stage;
- conduction path break;
- doubly grounded converters.

A more detailed analysis of leakage currents in transformerless PV inverters is presented in Chapter 4.

2.3 LCL filters

Grid-connected VSI require filtering in order to reduce the injection in the grid of current harmonics generated around switching frequency; to do so a large inductance is traditionally used. An alternative solution is the use of a LCL filter. Due to the higher-order the required inductances are smaller compared to simple L filter, leading to minor costs and potentially better dynamic performances, while providing the same grid current THD. In [31, 32] a sizing procedure is proposed.

The main drawback relative to the use of LCL filter is the introduction of two complex-conjugated poles, having a resonant frequency that must be smaller than the switching frequency, in order to obtain adequate filtering. In order to guarantee system stability, damping of these poles must be provided, either via active or passive methods. Passive damping can be achieved simply by placing a resistor in series with the capacitor [32], however this often leads to unacceptable power losses.

Active damping can be achieved by means of control, but this often imply the needing of additional sensor and complex tuning procedures, thus increasing costs and negatively affecting reliability. Various control architectures have been proposed to overcome these problems. In [33] the use of PI based current control with one set of current sensors (the same used for traditional L filters) is proposed. The advantage of this method is that it can be applied to common pre-existing inverters simply by replacing the existing filter and re-tuning the existing PI controller. In [34] the use of a genetic-algorithm based tuning of the controller poles-zeros is proposed.

The control and stability of LCL filters is still object of current research [35–41]. Many of the proposed control strategies require the measurement of additional signals (such as the capacitor voltage or current), and/or the knowledge of the model.

The majority of the literature refers to three-phase systems, however the same control strategies can easily be adapted for single-phase converters.

Despite the additional complexity, LCL filters are useful to reduce the size

of the AC filter, increasing the energy density of the converter. For this reason, LCL filter are used in the proposed topologies described in Chapter 5 and 6.

2.4 State-of-the-art topologies

In this section, various state-of-the-art topologies for single phase ac/dc converter are compared. The topologies are chosen among those that tackle the problems of ripple power decoupling and/or leakage currents. The comparison is focused on the main points that affect the cost and energy density of single phase converters, such as the number of active devices, and the size of the required power decoupling capacitor, that is strongly affected by the voltage constraints that the choice of converter topology imposes on it.

The required size for the power decoupling capacitor is dependent on the nominal power of the converter, on the frequency of the AC port, on the voltage capability of the required capacitor and on the voltage constraints on the amplitude of ripple voltage that can be applied to the capacitor, depending on the topology. In order to compare converters having different DC and AC nominal voltages, power decoupling capacitor size and AC frequency, a figure of merit (FOM) is calculated. The FOM is defined as the ratio between the required ripple energy E_R and the maximum energy stored in the power decoupling capacitor E_C:

$$FOM = \frac{E_R}{E_C} = \frac{P/\omega}{1/2\, C\, V_{C,MAX}^2} = \frac{P}{\pi\, f\, C\, V_{C,MAX}^2} \tag{2.1}$$

The calculations leading to the expression ripple energy E_R are shown in (3.7). A higher FOM involves the need for a smaller power decoupling capacitor, given the same ripple energy. This translates in lower costs and higher power density.

Another important parameter to consider in order to compare different topologies is the DC voltage ratio, defined as the ratio between the DC bus voltage and the AC peak voltage. Considering a full bridge VSI, to avoid overmodulation, the minimum DC voltage has to be higher then the peak AC voltage. If the DC voltage is higher, it is always possible to achieve the desired AC voltage mag-

nitude by acting on the modulation. However, a very high DC bus voltage is undesirable, as it causes higher losses on the switching devices and higher ripple current. Because of that, bigger filtering inductors are required, increasing costs and reducing power density.

	Nominal Power $[kW]$	Number of devices	DC port voltage $[V]$	DC bus voltage $[V]$	AC port voltage $[V_{RMS}]$	Frequency $[Hz]$	Power dec. Capacitance $[\mu F]$	Efficiency %	DC util. ratio %	FOM %
Wang *et.al.* [1]	15	6	540	540	150	233	200	93	39	35(100)*
Breazeale*et.al.* [2]	1	6	200-550	700	240	60	2·102	97	48	11
Xia *et.al.* [6]	1	4	200-475	950	120	60	45	96	18	13
Zhong *et.al.* [3]	1	4	400	400	110	50	30	92	39	13
Tang *et.al.* [5]	1	3+5diodes	380	380	110	60	2·90	93	41	40
Tang *et.al.* [4]	.5	4	250	250	110	60	2·60	96	62	35

Table 2.1: Comparison between state-of-the-art single phase topologies

Wang *et.al.* [1]

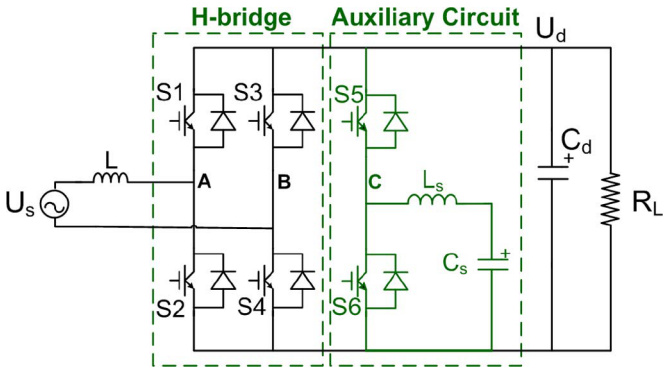


Figure 2.2: Wang *et.al.* [1]

The solution proposed by Wang *et.al.* consists in adding to the conventional inverter topology an additional half bridge connected to a power decoupling capacitor. This solution allows the use of a very small power decoupling capacitor, since the voltage applied to it can span across the full range from zero to the DC bus voltage V_{DC}. This comes with the disadvantage of additional losses in the auxiliary circuit. In order to reduce the losses, the inductor L_s and the capacitor C_s are designed so that the auxiliary bridge operates in discontinuous current mode (DCM). While this reduces switching losses, it has negative effect on the conduction losses in both the active devices, the inductor and the power decoupling capacitor, and on the DC link capacitor as well. While the topology allows full voltage swing from zero to V_{DC} on the power decoupling capacitor, that should correspond to a FOM of 100%, the choice of operating in DCM translates in a constraint on the voltage modulated by the auxiliary bridge. For this reason, the FOM of the system is relatively low, at about 35%.

Breazeale *et.al.* [2]

The topology presented by Breazeale *et.al.*, shown in Fig.2.3, is formed by a conventional full bridge connected to a modified boost stage. The power decoupling capacitor is connected between the negative terminal of the DC link and the negative terminal of the DC port. By allowing the DC link voltage to change, it is possible to independently control the voltage applied to the DC port and to the

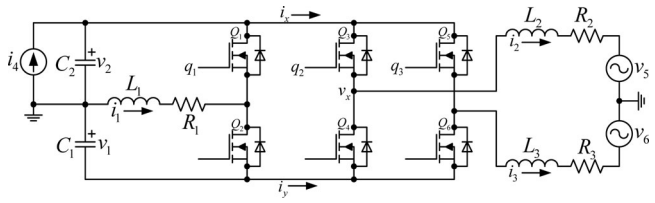


Figure 2.3: Breazeale *et.al.* [2]

power decoupling capacitor. This topology is also capable to boost the voltage applied to the DC port. The disadvantage of this topology consists in the DC link voltage being the sum of the DC port voltage and the power decoupling capacitor voltage. That translates in a poor DC utilization ratio and FOM.

Zhong *et.al.* [3]

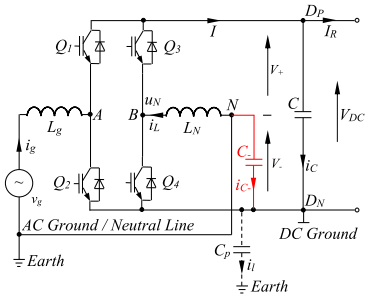


Figure 2.4: Zhong *et.al.* [3]

The so called Beijing topology, shown in Fig.2.4, was introduced by Zhong *et.al.* in [3]. The topology uses a full bridge to control grid voltage, and a power decoupling capacitor connected between one of the bridge arms and the negative terminal of the DC link. This topology has the advantage of requiring a small number of active devices, however the presence of the power decoupling capacitor poses significant constraints on the DC link voltage, to avoid overmodulation. For this reason, the FOM and the DC utilization ratio are very low. Another disadvantage of this topology is that the current flowing in the bridge arm connected to the capacitor is significantly high, both in RMS and peak value, reducing the overall efficiency.

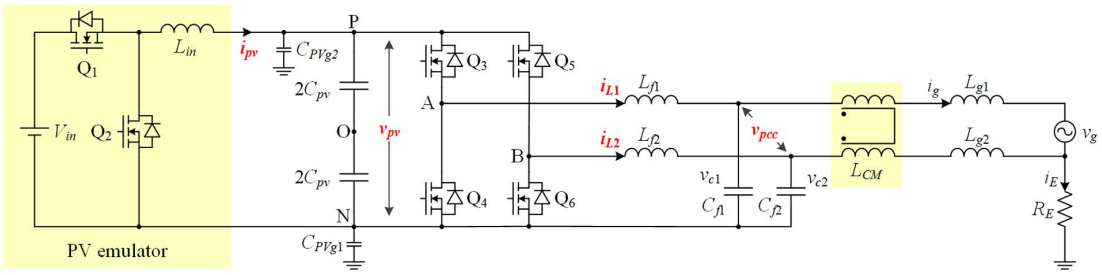


Figure 2.5: Tang *et.al.* [4]

Tang *et.al.* [4]

The topology introduced by Tang *et.al.* in [4], similarly to the Beijing converter, is constituted by a full bridge whose differential voltage is used to control grid current. In this case, however, two power decoupling capacitors are used, connected between each bridge arm and the negative DC link terminal. This topology has the advantage of having a small number of devices, moreover, the power decoupling capacitors offer a good filtering action both for common and for differential mode currents. However, due to the voltage constraints imposed by the AC port, the utilization of the capacitors is not ideal, leading to low DC voltage utilization and low FOM. The same topology was introduced by Vasquez *et.al.* in [42], and its control is further discussed in [43].

Tang *et.al.* [5]

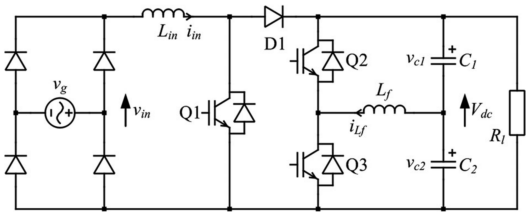


Figure 2.6: Tang *et.al.* [5]

The topology introduced by Tang *et.al.* in [5], is a PFC with an additional power decoupling cell, formed by Q2, Q3, Lf and two equal capacitors, C1 and C2, as shown in Fig.2.6. The peculiarity of this topology is that the same capacitors that provide power ripple decoupling are connected in series and also

work as DC capacitor, absorbing the switching frequency ripple current. The energy stored in the two capacitor is controlled by changing the voltage applied to the midpoint of the two. The configuration that corresponds to the maximum stored energy is found when one capacitor is completely charged and the other completely discharged, while the minimum stored energy is stored when the midpoint voltage is equal to $V_{DC}/2$, *i.e.*, when the voltage is equally shared between the two capacitors. The disadvantage of this topology consists in the suboptimal energy utilization of the capacitors, due to the fact that one capacitor is charging while the other is discharging.

Xia *et.al.* [6]

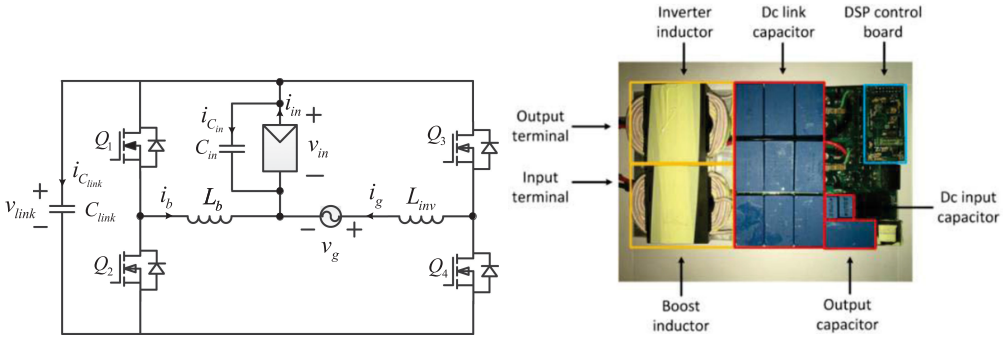


Figure 2.7: Xia *et.al.* [6]

The topology introduced by Xia *et.al.* in [6] has the advantage of being a double-grounded converter, that is, both the negative DC port connection and one of the AC port connection are connected to the same node. This has the advantage of solving the problem of leakage currents, for this reason, this topology is indicated for use in PV systems. The disadvantage is an extremely low DC utilization ratio, that translates in additional switching losses, and the need for big filtering inductors (shown in Fig.2.7b).

2.5 Conclusions

In this chapter, a literature review of the state-of-the art regarding single phase grid front-ends is presented, with particular focus on the ripple power decoupling capability of various solutions.

Active ripple power decoupling capability and good leakage current filtering are identified as important feature for the development of better converters, that manage to achieve significantly higher power density with the reduction of the required DC link capacitance and, in case of PV systems, have the possibility to use a transformer-less configuration, reducing costs and losses and improving reliability. Moreover, the use of LCL filters in the AC side of the converter is shown to be particularly beneficial for reducing the size of the AC current filter.

For these reasons, the proposed topologies introduced in Chapters 5 and 6 are capable of active power decoupling and make use of LCL filters on the AC side. Before introducing the topologies, a more in depth analysis of ripple power decoupling and leakage current filtering is discussed in the following Chapters.

A theoretical approach to the leakage current problem in transformer-less PV systems is addressed in detail in Chapter 4.

The next chapter is dedicated to an analytical study of ripple power in single phase systems.

Chapter 3

Ripple power decoupling in single-phase converters

A single phase AC-DC converter can be defined as an apparatus that exchanges electrical power between a DC and a single phase AC port. Since the power coming from DC sources (PV, eolic or batteries) is constant, while the power exchanged through a single phase AC connection is pulsating, the converter has to be able to store energy, via one or more energy storage elements, in order to provide power decoupling, since the power exchanged through its two port is not equal in every instant, as shown in fig.3.1.

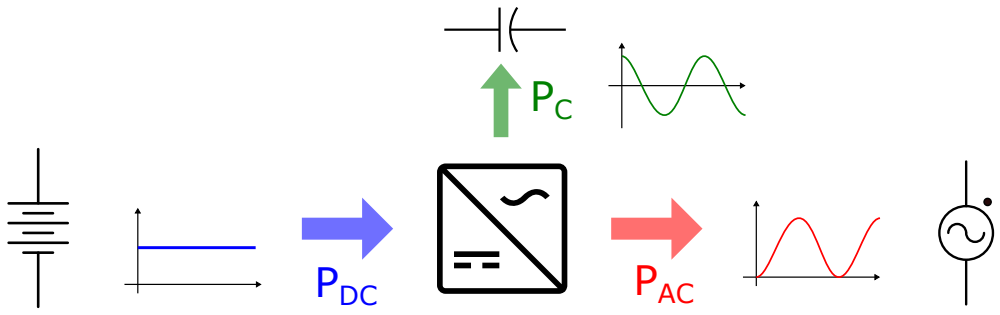


Figure 3.1: Basic power flow in Single-Phase converters

In this chapter, an analysis of the power balance of a generic AC-DC single phase converter is introduced in section 3.1. Using that analysis, the voltage waveform that has to be applied to one or more power decoupling capacitors in order to achieve power decoupling is achieved, in section 3.2. Section 3.3 contains

an analysis of the currents flowing through the ports of a single phase AC-DC converter using a ripple port, that is useful for the description of the proposed topologies introduced in the following chapters.

3.1 Ripple power

When internal losses are neglected, the ideal energy balance of any converter can be expressed as in (3.1), where $E(t)$ is energy stored in the converter over time, t_0 is an arbitrary initial instant of time, and $P_{in}(t)$, $P_{out}(t)$ are the instantaneous power flows in and out of the converter.

$$E(t) - E(t_0) = \int_{t_0}^{t} [P_{in}(t^*) - P_{out}(t^*)]\, dt^* \tag{3.1}$$

Considering an ideal single-phase converter, its basic power flow diagram can be illustrated as shown in Fig. 3.1, assuming that the power entering the DC port is constant and equal to P_{DC}, while at AC side the converter operates with ideal sinusoidal quantities and arbitrary power factor. By neglecting the internal losses the difference between the instantaneous powers flowing in and out the converter can be then calculated as follows:

$$V_{AC}(t) = \sqrt{2} V_{AC,RMS} \sin(\omega t) \tag{3.2}$$

$$I_{AC}(t) = \frac{\sqrt{2}}{V_{AC,RMS}} \Big[P \sin(\omega t) - Q \cos(\omega t) \Big] \tag{3.3}$$

$$P_{out} = V_{AC}(t)\, I_{AC}(t) = P\,[1 - \cos(2\omega t)] - Q \sin(2\omega t) \tag{3.4}$$

$$P_R(t) = P_{in}(t) - P_{out}(t) = P \cos(2\omega t) + Q \sin(2\omega t) \tag{3.5}$$

Where $V_{AC,RMS}$ is the RMS value of the AC converter voltage, P and Q are the active and reactive power injected from the converter into the grid, and $\omega = 2\pi f$ where f is the AC frequency.

Substituting in (3.1), the resulting energy is:

$$E(t) - E(t_0) = \int_{t_0}^{t} [P\, \cos(2\omega t^*) + Q\, \sin(2\omega t^*)]\, dt^* \tag{3.6}$$

The minimum energy storage capability E_R of the converter can be calculated by solving the integral in 3.6:

$$E_R = \max\Big(E(t) - E(t_0)\Big) = \frac{\sqrt{P^2 + Q^2}}{\omega} \tag{3.7}$$

Since the net power flow entering the converter calculated in (3.5) is a periodic function at double the AC frequency, when t_0 is chosen equal to 0, according to (3.2), $E(t_0)$ represents the energy stored in the reactive elements at any instant when the AC port voltage is zero.

The energy stored in reactive elements is a function of the voltages applied across capacitors and currents flowing through inductors. For simplicity, the converter is assumed to be designed such that the energy stored in small size capacitors and inductors aimed to filter high-frequency harmonics is negligible, so that only *nc* power ripple decoupling capacitors and/or *nl* power ripple decoupling inductors can be taken into account in the main power balance. The total stored energy may then be expresses as follows, provided that all reactive elements can be considered constant and time invariant:

$$E(t) = \frac{1}{2}\sum_{i}^{nc} C_i V_i^2(t) + \frac{1}{2}\sum_{j}^{nl} L_j I_j^2(t) \tag{3.8}$$

By substituting (3.8) in (3.6), assuming $t_0 = 0$ and solving the integral, it is possible to obtain a relation between voltages in power decoupling capacitors and currents in power decoupling inductors that shall be ideally verified at any instant of time if ideal power decoupling is achieved. It is important to note that the resulting expression in (3.9) holds true without making any assumption on the specific converter topology under study, and has therefore general validity in single-phase converters.

$$\frac{1}{2}\sum_{i}^{nc} C_i\big[V_i^2(t) - V_{i0}^2\big] + \frac{1}{2}\sum_{j}^{nl} L_j\big[I_j^2(t) - I_{j0}^2\big] = \frac{1}{2\omega}\left\{P\sin(2\omega t) + Q\Big[1 - \cos(2\omega t)\Big]\right\} \tag{3.9}$$

Where V_{i0} are the voltages of each power decoupling capacitor, and I_{j0} are the currents of each power decoupling inductor, at $t = t_0$.

3.2 Energy storage in capacitors

In order to size a capacitor, the values of maximum voltage, maximum rms current and, obviously, capacitance must be determined, considering that the power decoupling component has to exchange a power equal to the opposite of the ripple power.

3.2.1 DC-link connected capacitors

Applying a variable voltage to the capacitor, the energy that can be exchanged is equal to:

$$E_R = \frac{1}{2} C \left(V_{max}^2 - V_{min}^2\right)$$

In the case of dc-link connected capacitors it is useful to obtain energy in terms of voltage ripple:

$$E_R = \frac{1}{2} C \left[\left(V_{DC} + \frac{\Delta V}{2}\right)^2 - \left(V_{DC} - \frac{\Delta V}{2}\right)^2\right] = \tag{3.10}$$

$$= C\, V_{DC} \Delta V = \tag{3.11}$$

$$= C\, V_{DC}^2 \frac{V_{ripple_max,\%}}{100} \tag{3.12}$$

Thus, capacitance must be equal or greater to:

$$C = \frac{100\, E_R}{V_{DC}^2\, V_{ripple_max,\%}} = \frac{100\, \sqrt{P^2 + Q^2}}{\omega\, V_{DC}^2\, V_{ripple_max,\%}} \tag{3.13}$$

Since voltage ripple in DC-bus is usually required to be small, it can be neglected to calculate current flowing in the capacitor:

$$I(t) \simeq -\frac{P_R(t)}{V_{DC}} = -\frac{\sqrt{P^2 + Q^2}\ \sin\left(2\omega t + \theta\right)}{V_{DC}} \tag{3.14}$$

Being the current sinusoidal, it is immediate to achieve its rms value:

$$I_{rms} = \frac{1}{\sqrt{2}} \frac{\sqrt{P^2 + Q^2}}{V_{DC}} \tag{3.15}$$

While this solution is simple to implement, since it does not need any kind of additional components and control architecture, it should be noted that it is not good in terms of energy density, since only a small quota of the energy stored in the capacitor contributes in power decoupling. Moreover, in order to keep the ripple low, a high value of capacitance must be used, typically restricting the choice to electrolytic capacitors, which have well-known problems in terms of lifespan and reliability [7].

3.2.2 Ripple port

To maximize energy density it is advisable to control voltage applied to the capacitor independently from dc-bus, in order to apply larger ripple voltages. To do so, an auxiliary circuit, called *ripple port*, has to be introduced, as shown in figure 3.2. The concept of ripple port was introduced by Krein *et.al.* in [7] and has since been widely adopted [27, 28, 43–45].

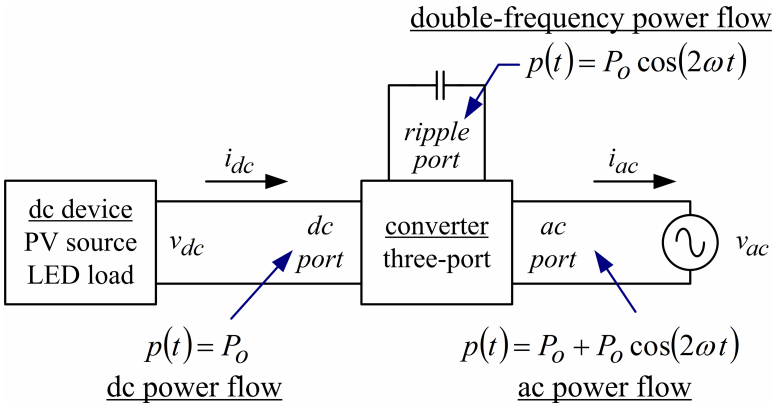


Figure 3.2: Ripple port (Krein *et al* [7])

In this case the value of capacitance required, given a maximum and a minimum voltage v_{max}, v_{min} can be calculated as:

$$C = \frac{2\ E_R}{(v_{max}^2 - v_{min}^2)} \tag{3.16}$$

Since capacitor voltage is not approximately constant as in the previous case, in

order to calculate it as function of time, given the required instantaneous power $P_R(t)$, this equation must be solved:

$$E(t) - E_0 = -\int_0^t P_R(t^*)dt^* \tag{3.17}$$

Where:

- $E(t)$ is the energy stored in the capacitor(s) over time;
- E_0 is the energy stored in the capacitor(s) at t=0;
- $P_R(t)$ is the ripple power.

Since $P_R(t)$ is known, its integral can be calculated as:

$$-\int_0^t P_R(t^*)dt^* = -\int_0^t P_R \sin(2\omega t^* + \theta)dt^* = \frac{P_R}{2\omega}\left[\cos(2\omega t + \theta) - \cos(\theta)\right] \tag{3.18}$$

Assuming to have one single capacitor, its energy can be calculated as a function of its voltage over time:

$$E = \frac{1}{2}Cv(t)^2 \tag{3.19}$$

$$E_0 = \frac{1}{2}Cv_0^2 \tag{3.20}$$

Substituting in eq.3.17:

$$\frac{1}{2}Cv(t)^2 - \frac{1}{2}Cv_0^2 = \frac{P_R}{2\omega}\left[\cos(2\omega t + \theta) - \cos(\theta)\right] \tag{3.21}$$

Thus:

$$v(t) = \sqrt{\frac{P_R}{C\omega}\left[\cos(2\omega t + \theta) - \cos(\theta)\right] + v_0^2} \tag{3.22}$$

The sign of voltage is, obviously, unimportant.

It should be noted that this equation can be solved only for certain values of v_0 (in order to have a positive number under the root operator). The minimum instantaneous value of v(t) is:

$$v_{min} = \sqrt{\frac{P_R}{C\omega}\left[-1-\cos(\theta)\right] + v_0^2} \tag{3.23}$$

Thus, the minimum value of v_0, that corresponds to a null minimum instantaneous voltage, can be calculated as follows:

$$v_{0,min} = \sqrt{\frac{P_R}{C\omega}\left(1+\cos\theta\right)} \tag{3.24}$$

Current can now be achieved both using the constitutive relation of capacitor (deriving voltage over time and multiplying by C) or simply dividing instantaneous power by voltage:

$$i(t) = \frac{-P_R \sin(2\omega\, t+\theta)}{\sqrt{\frac{P_R}{C\omega}\left[\cos(2\omega t+\theta)-\cos(\theta)\right] + v_0^2}} \tag{3.25}$$

In case of unity power factor operation ($P_R = P$ and $\theta = -\frac{\pi}{2}$):

$$v(t) = \sqrt{\frac{P_R}{C\omega}\,\sin(2\omega t) + v_0^2} \tag{3.26}$$

$$i(t) = \frac{P_R \cos(2\omega\, t)}{\sqrt{\frac{P_R}{C\omega}\,\sin(2\omega t) + v_0^2}} \tag{3.27}$$

As can be seen from (3.23) and (3.25), choosing a low value of v_0 reflects in a lower maximum voltage, thus, a low v_0 enables the use of the smallest possible capacitor given the maximum voltage and the magnitude of power ripple; however it involves higher values of RMS current. On the other hand, using high values of v_0 results in sinusoidal-like waveforms of current and ripple voltage, eventually resolving to those found in DC-link connected capacitors.

Those equations can simply be adapted in case of the use of multiple capacitors, each one controlled by a different voltage. In order to do so, however, additional equations must be provided to solve the system.

3.3 Destructive interference

Having calculated the waveform of voltage and currents of the power decoupling capacitor in (3.23) and (3.25), the analytic expression of all the waveforms of the steady-state voltage and current flowing through the AC, DC and ripple port of a generic single phase AC-DC converter are known.

This section discusses a method for reducing the current stress in the switching devices and magnetic components of single-phase AC/DC converters, by exploiting the destructive interference occurring between some spectral components of the currents flowing through the converter ports. This can profitably be exploited by adopting topological configurations that generate such destructive interference; and constitutes the principle around which the proposed topologies described in Chapters 5 and 6 were conceived.

As described in section 3.2.2, if the ripple port is considered external to the converter, a generic single phase AC/DC converter exchanges power between three electrical ports: the AC port, the DC port and the ripple port.

Since the current flowing in the AC port is a sinusoid at grid frequency, the current flowing in the DC port is DC, and the current flowing in the ripple port has a fundamental frequency that is double the AC frequency, it follows that no destructive interference is possible, since there are no spectral components at the same frequency. However, if the AC current is rectified by a rectifier/unfolder bridge, operating at grid frequency, the resulting rectified/unfolded AC current has both a DC component and a fundamental frequency at double the grid frequency.

It is shown that it is possible to exploit the destructive interference between the spectrum components at the same frequency of the currents, obtaining beneficial results, both in terms of reduced peak currents and reduced RMS current stress on the converter components.

3.3.1 Fourier analysis of currents

From circuit analysis it is well known [46] that the RMS of a generic signal can be calculated knowing the magnitudes of its spectral components, achieved using the Fourier series transform:

$$RMS(f) = \sqrt{\frac{1}{T}\int_0^T f(t)^2 dt} = \sqrt{c_0^2 + \frac{1}{2}\sum_i c_i^2} \tag{3.28}$$

Considering the linearity of the Fourier transform, it follows that the RMS of the sum of two signals having different spectral components is equal to the root of the sum of the squares of the RMS of each signal.

For this reason, if the spectra of the two currents have components at the same frequency, the RMS of the sum can increase or decrease depending on the phase between the interfering components, that is, if the interference is constructive or destructive.

Fourier series of converter port currents

In this subsection, the fundamental components of the currents flowing through the ports of a generic converter are obtained using the Fourier series transform.

Assuming the voltages of the converter port to be independent with respect to the power, it follows that all the obtained currents are linear with the exchanged power P; for this reason, they are normalized and the result is indicated as A/kW.

The Fourier series of a rectified sine wave is:

$$x(t) = A\big|\sin(2\pi f t)\big| \;=\; \frac{2A}{\pi} - \frac{4A}{\pi}\sum_{k=1}^{\infty}\frac{\cos\big(k2\pi f t\big)}{4k^2-1} \tag{3.29}$$

Thus:

$$|I_{AC}(t)|_0 = \frac{2}{\pi}\frac{\sqrt{2}P}{V_{AC,RMS}} \qquad \Rightarrow \qquad \frac{|I_{AC}|_0}{P} = 3.91\frac{A}{kW} \tag{3.30}$$

$$|I_{AC}(t)|_1 = -\frac{4}{3\pi}\frac{\sqrt{2}P}{V_{AC,RMS}}\cos(2\pi\, 2ft) \quad \Rightarrow \quad \frac{RMS(|I_{AC}|_1)}{P} = 3.69\frac{A}{kW} \tag{3.31}$$

The resulting RMS currents as function of the transferred power P are calculated considering a RMS grid voltage of 230V.

Assuming the DC bias V_0 to be high compared to the amplitude of the voltage ripple, the dependence of the capacitor voltage on P is neglected. The ripple port current can thus be obtained as follows.

$$I_C(t) = \frac{P_R(t)}{V_C(t)} \simeq \frac{P_R(t)}{V_0} \tag{3.32}$$

$$I_C(t) \simeq \frac{P}{V_0}\cos(2\pi\, 2f) \qquad \Rightarrow \qquad \frac{I_{C\,1,RMS}}{P} = \sqrt{2}\frac{1e3}{V_0}\frac{A}{kW} \tag{3.33}$$

$$I_{DC}(t) = \frac{P}{V_{DC}} \qquad \Rightarrow \qquad \frac{I_{DC}}{P} = \frac{1e3}{V_{DC}}\frac{A}{kW} \tag{3.34}$$

3.3.2 Interference

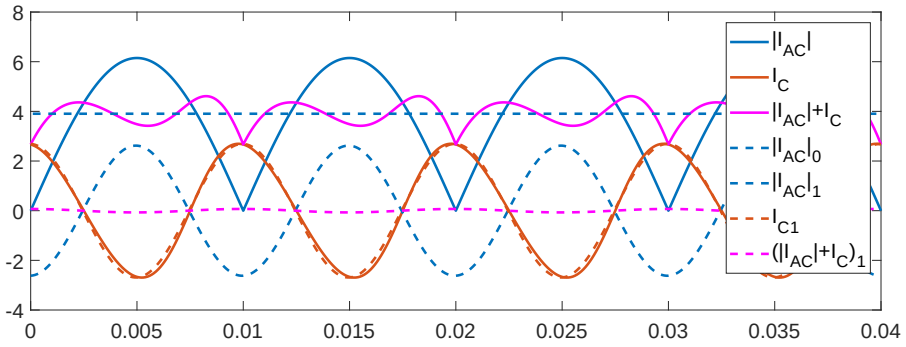
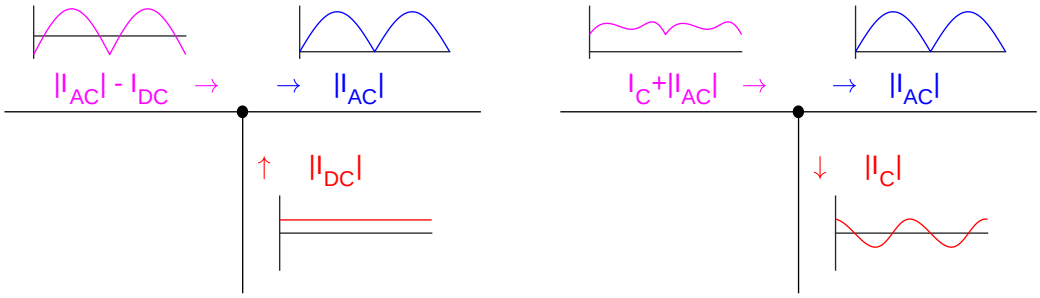


Figure 3.3: Fundamental components of $|I_{AC}(t)|$ and $I_C(t)$: cancellation of the AC components in $|I_{AC}| + I_C$ ($P = 1kW$, $V_0 = 375V$, $V_{DC} = 450V$)

A possible strategy to increase the efficiency of the converter is to adopt a topology that exploits a destructive interference between the current flowing through the ports of the converter, in order to reduce the RMS applied on the switching devices.

Since the 100Hz component of the capacitor current is almost opposite in phase with the 100Hz component of rectified grid current, the interference between them is destructive if they are added: figure 3.3 shows the rectified grid current $|I_{AC}|$, capacitor current I_C and their sum.



(a) DC component reduction (b) 100Hz component reduction

Figure 3.4: Topological configurations that achieve destructive interference

The maximum destructive interference is obtained if the two components have the same magnitude, leading to a complete cancellation:

$$\frac{P}{V_0} \simeq \frac{4}{3\pi}\frac{\sqrt{2}P}{V_{AC,RMS}} \qquad \Rightarrow \qquad V_0 = \frac{3\pi}{4\sqrt{2}}V_{AC,RMS} \simeq 383V \tag{3.35}$$

The RMS of the resulting current can be obtained as follows:

$$\mathbf{RMS}\Big(|I_{AC}| + I_C\Big) = \mathbf{RMS}\Big(|I_{AC}| - |I_{AC}|_1\Big) = \tag{3.36}$$

$$= \sqrt{\mathbf{RMS}\Big(I_{AC}\Big)^2 - \mathbf{RMS}\Big(|I_{AC}|_1\Big)^2} = \tag{3.37}$$

$$= \sqrt{\left(\frac{P}{V_{AC,RMS}}\right)^2 - \left(\frac{4}{3\pi}\frac{P}{V_{AC,RMS}}\right)^2} = \tag{3.38}$$

$$= \frac{P}{V_{AC,RMS}}\sqrt{1 - \left(\frac{4}{3\pi}\right)^2} = \tag{3.39}$$

$$\simeq 0.906\ \mathbf{RMS}\Big(I_{AC}\Big) \tag{3.40}$$

In order to achieve destructive interference between the DC components of the rectified AC current and the DC port current, they have to be connected as shown in Fig.3.4a. In the same way, in order to achieve destructive interference between the fundamental component of the rectified grid current and the ripple port current, the connection has to be made as in Fig.3.4b.

3.4 Conclusions

In the present Chapter, an analytical study of ripple power in single phase systems was discussed.

The possibility of exploiting a destructive interference between the currents flowing through the ports of a generic single-phase AC-DC converter was investigated. It was shown that reduction of the double frequency current components can only be achieved if the rectified/unfolded grid current is considered.

The configuration shown in figure 3.4b is exploited in the proposed topologies introduced in Chapters 5 and 6.

In the following Chapter, a theoretical approach to the leakage current problem in transformer-less PV systems is addressed.

Chapter 4

Leakage currents in PV applications

Traditionally, AC to DC power converter for PV systems make use of a transformer in the power-conversion stage. The presence of a transformer has several advantages, such as galvanic isolation between the DC and AC ports of the converter, which is often mandatory; and voltage gain capability, that enables the use of a small number of series-connected PV modules without the need for a voltage boost stage.

In some countries, galvanic isolation between the AC grid and the panels is not mandatory, consequently, the use of transformer-less topologies is of interest. This is because, despite lacking the advantages previously described, the use of a transformer involves the necessity for an additional stage in the converter, increasing costs and losses and reducing reliability [47].

One of the most challenging problems faced by transformer-less converters is the presence of leakage currents. Since PV modules have a large stray capacitance to ground, and the neutral conductor of the grid is grounded, if a high frequency voltage is applied between the grid and the PV modules currents can circulate, causing losses and EMI noise. [48]

In the following section the leakage currents are defined and a circuital model useful to calculate their magnitude is described. Moreover, several solution exist-

ing in the literature, useful to reduce leakage currents in transformer-less single-phase PV systems are discussed.

4.1 Analysis

The spectral components of common mode currents can be classified in three components:

- a grid-frequency component ($50 - 60Hz$);
- a switching frequency component (often called leakage current) ($10^4 \div 10^5 Hz$);
- high-frequency components ($> 1MHz$ in case of Si devices, $> 10MHz$ for wide band-gap devices).

Grid-frequency components are usually low in magnitude, especially in the case of low-power low-voltage systems, because of the high impedance of stray PV capacitance at grid frequency; since the impedance of the stray capacitors at these frequencies is such that the current is negligible. However, in bigger systems, the growing of stray capacitance due to the larger number of panels can significantly increase those currents, especially if the AC voltage is high.

The high-frequency components are generated by the high dV/dt inherent in the commutation of the switching devices. The spectra of these components vary depending on the type of active devices used, *i.e.* wide band-gap devices operating in hard switching tend to have an high dV/dt in terms of magnitude, with a spectrum of frequencies of 10-100MHz, while Si devices exhibit a lower dV/dt and a longer turn on and turn off period. In order to filter these components a common mode filter can be used. This filter can have a reduced size, due to the high frequency of the signal, however care must be taken when choosing the components to make sure of their correct behaviour in the required frequency range. These design considerations are common to all grid-connected converters [23].

The switching frequency common mode current components, commonly referred as leakage currents, are excited by the common mode voltage present between the output of the inverter (generally a full bridge) and the DC port of the inverter, that can be connected to a string of PV panels either directly or through a boost stage. Because of the relatively high stray capacitance occurring between the active components of the PV panel and the outer structure of the panel itself, that must be grounded by law, leakage currents can reach very high levels if left unfiltered.

Since high frequency components are simple to filter, and in low-voltage systems grid frequency components are usually small, special attention is given to the switching frequency components, because their magnitude can severely impact the size of the EMI filter, and may reduce the efficiency and reliability of the inverter.

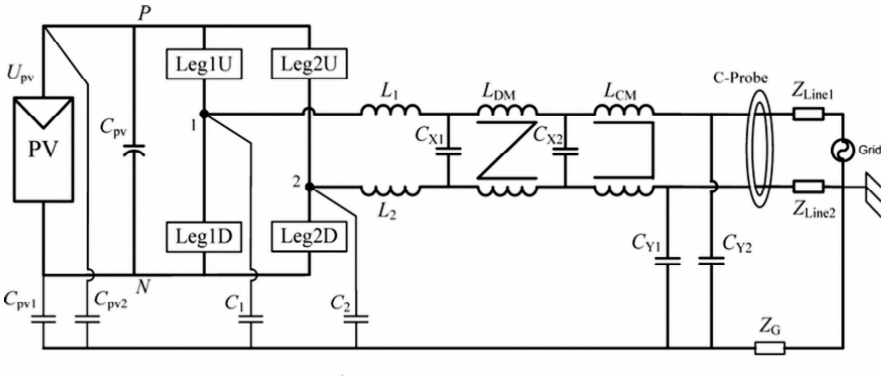


Figure 4.1: Common-mode current circuit (Xiao and Xie [8])

Circuital model

A circuital model for a generic converter including the stray capacitance and the commonly used output common mode and differential mode filters is shown in fig.4.1. The currents flowing from the PV modules stray capacitance can circulate through the grid, via the ground impedance Zg. Common mode reduction capacitors C_{Y1} and C_{Y2} are usually included in the EMI filter, and act as a current divider to reduce the quota of leakage current flowing through the PV panels that

circulates through the grid.

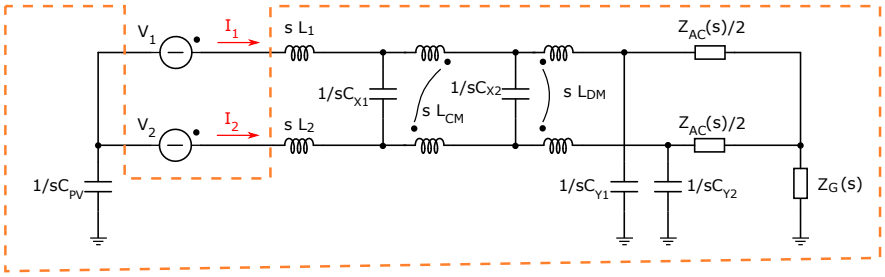


Figure 4.2: Equivalent two-port model for the circuit shown in Fig.4.1

It is important to take into account the parasitics of the various components, for this reason the resulting circuit model can be particularly complex. Assuming linearity, Laplace transform can be used to solve the circuit.

The circuit shown in fig.4.2 is the equivalent circuit for the topology shown in 4.1, useful to analyse the switching frequency component of the leakage current. The DC and AC voltage sources are removed, as their spectra do not include any switching frequency components, and the stray capacitors C_1 and C_2 are neglected, due to their high impedance at switching frequency.

Capacitors C_1 and C_2 model the stray capacitance between the mid-point of the inverter arms and ground, due to the presence of the heatsink. C_1 and C_2 are directly connected to the noise source, for this reason the currents flowing through them is often quite high in amplitude. Despite this, due to their small size, the spectral content of those currents is limited to high frequency components, and this justifies neglecting them in the leakage current model, that refers to the switching-frequency component only.

Common mode separation

If the passive elements connected to the terminal 1 and 2 of the circuit shown in fig.4.1 are balanced, it is possible to calculate the common mode and the differential mode of the currents separately. This can be proven by applying multi-port network analysis to the circuit. Considering a two port network, and the associated voltage inputs $V_1(s)$ and $V_1(s)$ and the corresponding currents $I_1(s)$ and $I_1(s)$, indicated by the dotted line in fig.4.2, and applying the following

transformation:

$$\begin{vmatrix} V_{DM}(s) \\ V_{CM}(s) \end{vmatrix} = K_V \begin{vmatrix} V_{1N}(s) \\ V_{2N(s)} \end{vmatrix} \qquad K_V = \begin{bmatrix} 1/2 & 1/2 \\ 1 & -1 \end{bmatrix} \tag{4.1}$$

$$\begin{vmatrix} I_{DM}(s) \\ I_{CM}(s) \end{vmatrix} = K_I \begin{vmatrix} I_{1N}(s) \\ I_{2N(s)} \end{vmatrix} \qquad K_I = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \tag{4.2}$$

$$\begin{vmatrix} I_{1N}(s) \\ I_{2N}(s) \end{vmatrix} = [Y] \begin{vmatrix} V_{1N}(s) \\ V_{2N}(s) \end{vmatrix} \Rightarrow \tag{4.3}$$

$$\Rightarrow [K_I] \begin{vmatrix} I_{1N}(s) \\ I_{2N}(s) \end{vmatrix} = [K_I][Y][K_V]^{-1} \left([K_V] \begin{vmatrix} V_{1N}(s) \\ V_{2N}(s) \end{vmatrix} \right) \Rightarrow \tag{4.4}$$

$$\Rightarrow \begin{vmatrix} I_{CM}(s) \\ I_{DM}(s) \end{vmatrix} = [K_I][Y][K_V]^{-1} \begin{vmatrix} V_{CM}(s) \\ V_{DM}(s) \end{vmatrix} \tag{4.5}$$

If the circuit is balanced, that is, if Y_{11} is equal to Y_{22}, the matrix $[K_I][Y][K_V]^{-1}$ is diagonal:

$$[K_I][Y][K_V]^{-1} = \begin{bmatrix} Y_{CM} & 0 \\ 0 & Y_{DM} \end{bmatrix} \tag{4.6}$$

Unbalanced circuit

In case of unbalanced circuit, calculating the common and differential mode voltages is not useful, since the common mode current is dependent on both. In order to calculate the common mode current, the complete circuit has to be solved. Solving the circuit, assuming linearity, results in the following equation:

$$i_{CM}(s) = \frac{V_{1N}(s)}{Z_1(s)} + \frac{V_{2N}(s)}{Z_2(s)} \tag{4.7}$$

The impedances $Z_1(s)$ and $Z_2(s)$ depend on the passive filters, while $V_{1N}(s)$ and $V_{2N}(s)$ depend on the chosen modulation strategy and the choice of the topology.

Considerations about resonance

The circuit contains both inductive and capacitive elements, for this reason, resonance does occur at certain frequencies. Since the grid impedance and ground

impedance can vary significantly depending on whether the grid is strong or weak, and stray capacitance of the PV panels can also vary depending on the PV model and also on the weather, the resonating frequency can vary.

For this reason, care must be taken in the design of the CM filter, to avoid resonance occurring at switching frequency, or at close multiples; and the real component of the impedance, that is constituted by the resistive components of the ground impedance and the stray resistors in the filtering inductors of the converter, has to be taken into account.

4.2 Leakage currents mitigation strategies

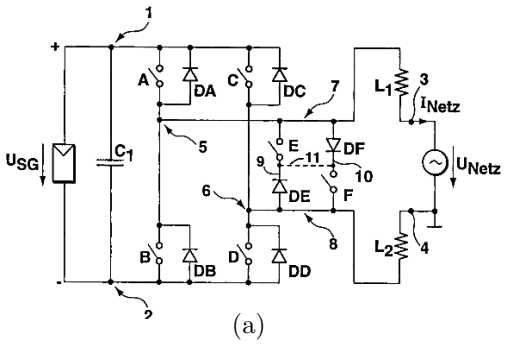
The known methods used to mitigate leakage currents can be divided in two main categories: the use of a modulation technique, usually with a modification of the converter topology, that allows to break the conduction path between the AC and the DC side of the converter, and the double-grounded topologies, where one terminal of the PV panel is grounded. Another strategy worth mentioning is exploited by the topologies that make use of the same capacitor that provides power ripple cancellation for common mode current filtering.

4.2.1 Conduction path break

One well-known technique to reduce leakage currents consist in breaking the conduction path between the PV panels and the grid during the free-wheeling period of the AC filtering inductor. That can be achieved in different ways, some of which are illustrated in fig.4.3.

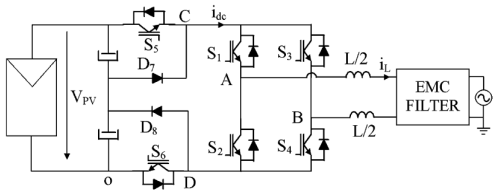
Breaking the connection between the AC and the DC port of the converter during the free-wheeling period is useful to reduce common mode voltage, as shown in fig.4.4, where a traditional inverter is compared with a heric inverter.

The disadvantage of this kind of solutions consists in the need for additional active components, and in some case a consistent reduction of efficiency, due to the increased number of devices in the conduction path, especially in [51], where



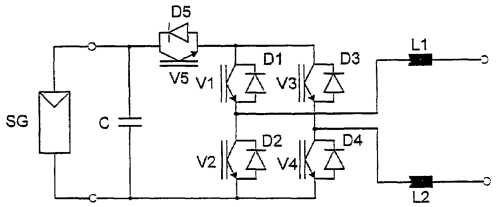
(a)

Heric topology (2003) [49]



(b)

Gonzalez (2007) *et.al.* [50]



(c)

H5 topology (2008) [51]

Figure 4.3: Common mode voltage reduction

an active device is placed between the inverter and the DC bus capacitor.

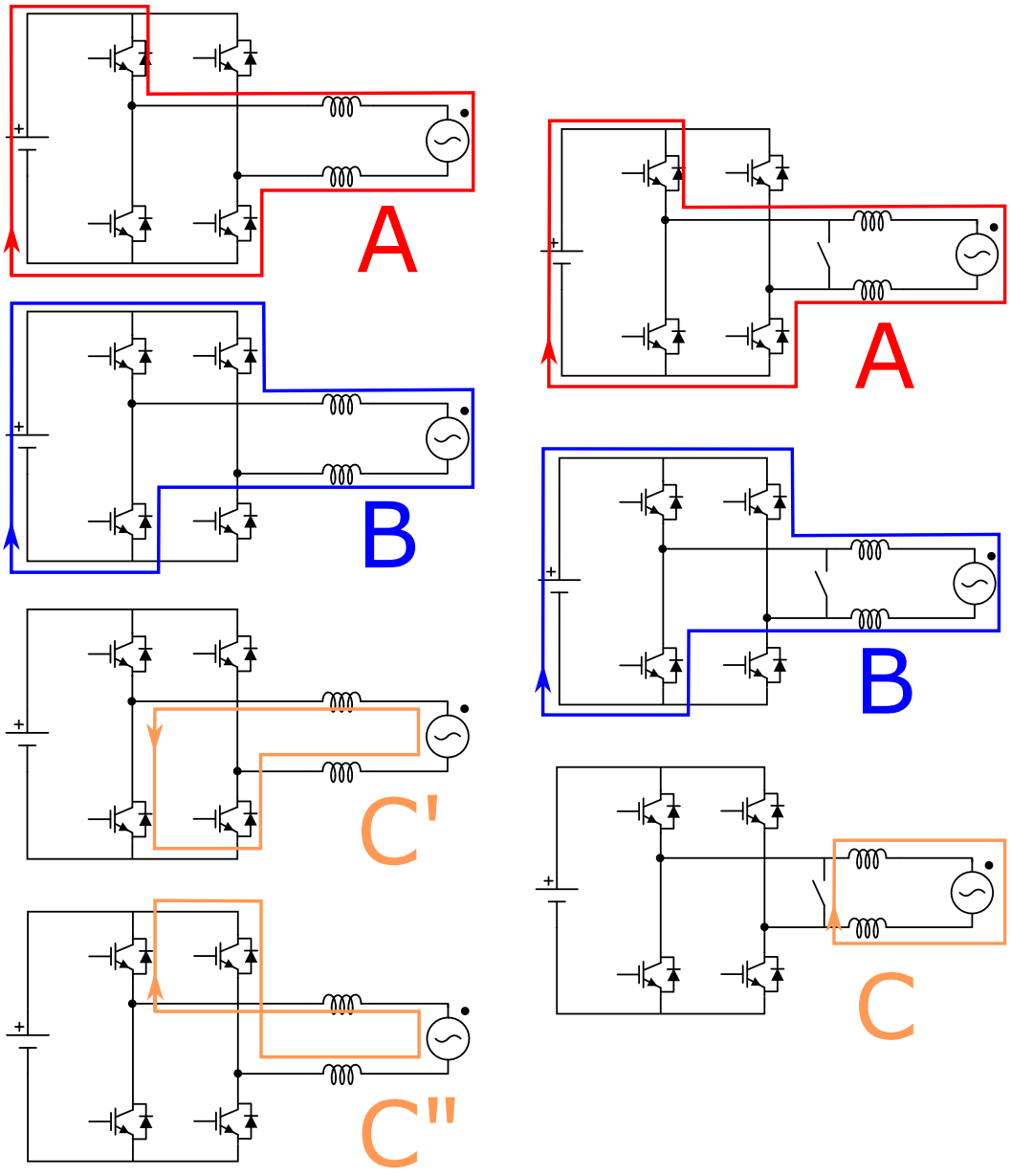
4.2.2 Doubly-grounded converters

Another possibility is making use of topologies that involve a double grounded connection, that is, topologies where one terminal of the PV panel (usually the negative) is grounded.

The main disadvantage of these solutions is the low DC utilization ratio of the converter, defined as the ratio between the DC bus voltage applied to the AC front-end and the peak AC voltage.

For example, in the topology introduced Xia *et.al.* [6], shown in Fig.4.5, the voltage V_{link} is around 900V, with a rated AC peak voltage of 340V (240V$_{RMS}$), resulting in a DC utilization ratio of 48.5%; while in the topology introduced Roy *et.al.* [9], shown in Fig.4.6, the voltage v_{dc2} applied to the AC full bridge has an amplitude of about 400V, for a rated AC peak voltage of about 170V (120V$_{RMS}$), which results in a DC utilization ratio of 42.5%.

A low DC utilization ratio is undesirable, since it translates in higher switching



(a) Generic inverter (b) Heric inverter

Figure 4.4: Operating states: comparison

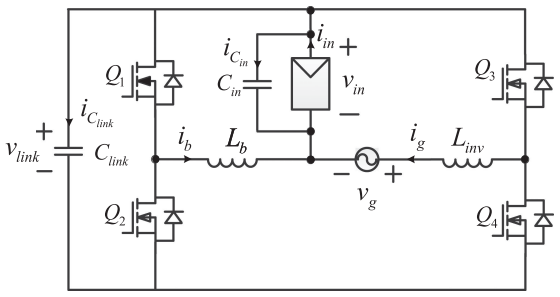


Figure 4.5: Double grounded converters: Xia *et.al.* (2017) [6]

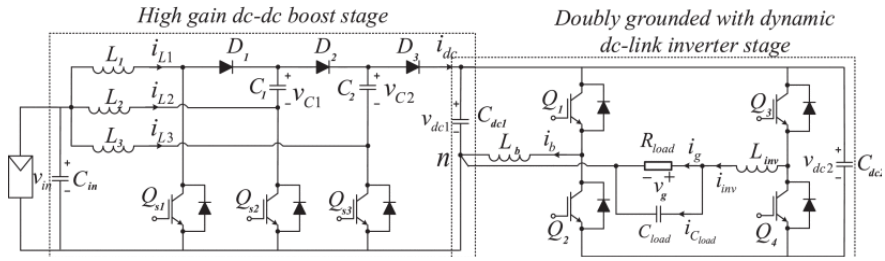


Figure 4.6: Double grounded converters: Roy *et.al.* (2019) [9]

losses in the active devices due to the increased voltage stress on the devices, and either in higher ripple currents or the need for bigger filtering inductors.

4.2.3 Other strategies

Tang *et.al.*

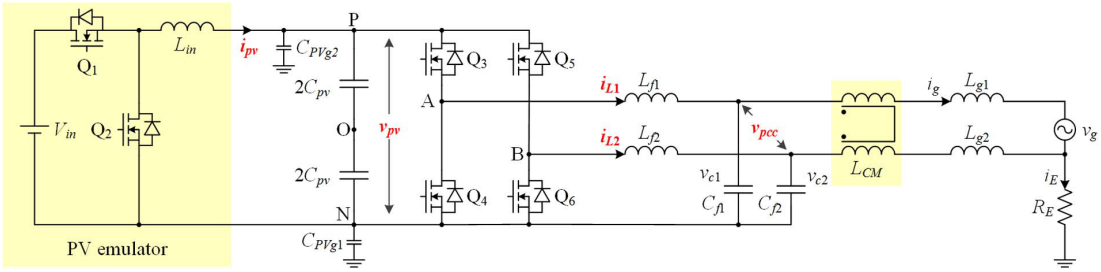


Figure 4.7: Tang *et.al* [4]

The topology shown in fig.4.7, introduced in [4], makes use of two big capacitors, indicated as C_{f1} and C_{f2}, which work both as energy storage components for the pulsating power elimination and as filters, both for differential and, with the help of the choke L_{CM}, common mode current ripple. This solution has the big advantage of requiring a small number of active devices, improving reliability and reducing costs. The disadvantages are an increased current stress on the switching devices, due to the additional current flowing in the capacitors, and the requirement of big capacitors for power decoupling, due to the additional constraints on their voltage waveform. This translates in lower power density and low DC voltage utilization.

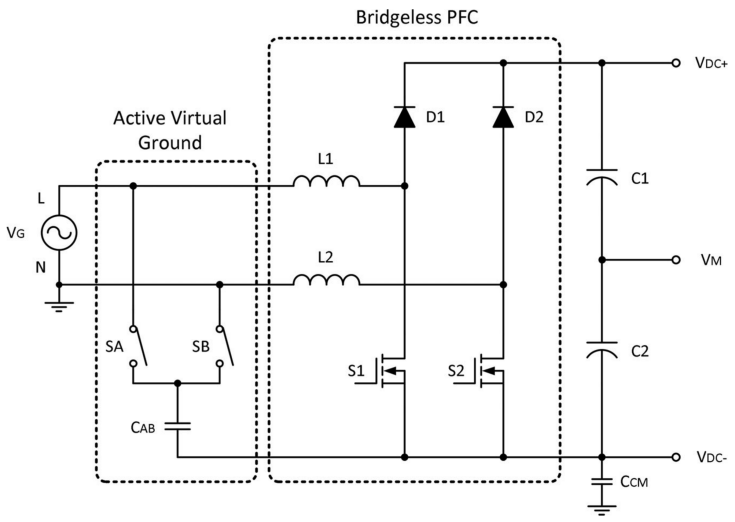


Figure 4.8: Active virtual ground [10]

Active virtual ground

The "Active virtual ground" topology, shown in fig.4.8, obtains attenuation of switching frequency common mode by exploiting an additional capacitor C_{AB}, that is alternatively connected to one of the AC port connections via the two switches S_A and S_B.

During the positive half-cycle of the grid, the capacitor C_{AB} is connected to the line (L) connection of the AC port, the switch S_2 is always closed and the AC current is modulated by S_1. During the negative cycle, C_{AB} is connected to the neutral (N) and the current is modulated by S_2, while S_1 is closed. It follows that, neglecting the ground impedance and the line impedance, C_{AB} is in parallel with the stray capacitor C_{CM}, thus acting as current divider and reducing the CM current injected in the grid.

Compared to the previous solution, this topology provides good leakage currents filtering using a much smaller capacitor, however, pulsating power elimination is not achieved, because control on the voltage ripple of the capacitor is lost.

4.3 Conclusions

In this Chapter, the issue of leakage currents in transformerless PV systems were discussed in detail. Several strategies to tackle this problem, available in literature, were considered.

In the following two Chapters, two novel topologies are introduced, the second of which has inherent leakage current filtering capabilities.

Chapter 5

Proposed topology: Double Full Bridge Converter

In this chapter, a topology for a single phase AC-DC converters, named "Double Full Bridge converter", is introduced and analysed.

This topology is intended for use as grid front-end, able to interface a DC microgrid, a PV panel system and-or a battery storage system to a single-phase AC connection.

The advantages are a reduced current stress in the devices operated at high frequency, active ripple power decoupling with good energy utilization of the power decoupling capacitor, and the possibility to use a reduced number of switches in case of unidirectional power flow.

The drawbacks of this topology are an high number of active devices, involving a increased cost, and the presence of a synchronous rectifier/unfolder stage, causing additional power losses and thus reduced efficiency.

The design of the passive component is discussed, and a control structure is described and validated with time-domain simulations. Extensive experimental results were recorded, and are exposed in chapter 9.

This chapter is structured as follows. Section 5.1 describes the proposed topology, explaining its operating principles and proposing a design method for the power decoupling capacitor and for the other passive components; section 5.2 de-

scribes the proposed control scheme, and finally section 5.3 shows the simulation results.

5.1 Theory of operation

As the name suggests, the proposed topology is formed by two full bridges, one switched at high-frequency, and one at grid frequency, as shown in figure 5.1. The low frequency full bridge (LFB) is operated at each zero crossing of the grid voltage, so that the steady-state value of the voltage applied to the filtering capacitor C_{AB}, situated on the pseudo-DC side of the LFB, is always positive and equal to the rectified grid voltage. In other words, the LFB is operated as an unfolder-rectifier bridge.

The AC-side of the LFB can be directly connected to the grid, however, for better current filtering and improved stability of the PLL [52], an additional filtering inductor L_{AC} can be used.

The inductors L_A and L_B are placed on the AC-side of the HFB in order to filter its output currents I_A and I_B. The power decoupling capacitor C_{PD} is connected between one arm and the negative DC terminal of the high-frequency switched full bridge (HFB), while C_{AB} is connected between its two arms. The steady-state voltage applied to C_{AB} is thus equal to the differential voltage modulated by the HFB.

5.1.1 Steady state analysis

In order to analyse the behaviour of the converter, the steady-state waveforms of the current and voltage modulated by the HFB (I_A, I_B and V_A, V_B) are considered.

The steady-state value of V_A is equal to the voltage applied to the power decoupling capacitor C_{PD}. Since the power ripple exchanged by the capacitor C_{AB} can be neglected due to its small size, only one capacitor is used for power decoupling, and its the voltage waveform $V_A(t)$ can be derived directly from

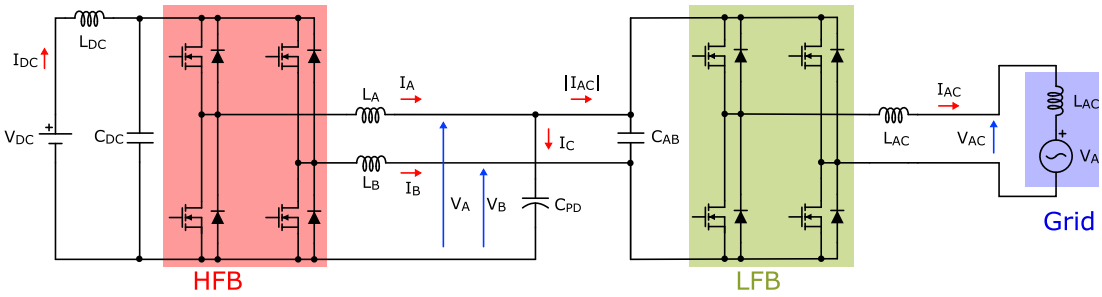
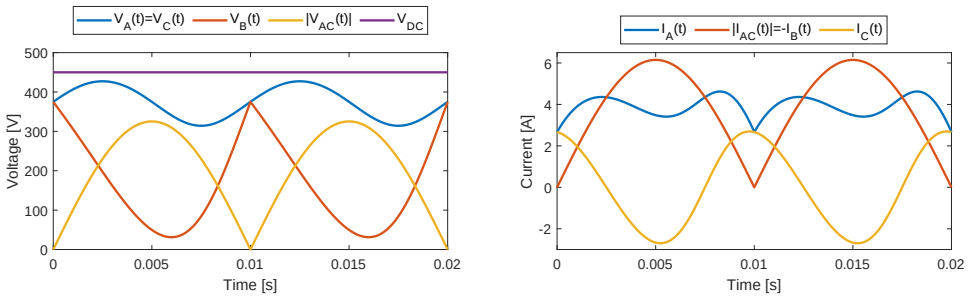


Figure 5.1: Dual Full-Bridge topology



(a) (b)

Figure 5.2: Voltage and current waveforms ($V_{DC} = 450V, P = 1kW, C = 76\mu F$)

eq.3.22. In this case, only active power is considered.

$$\begin{cases} V_A(t) = V_C(t) = \sqrt{\frac{P}{\omega C}\sin 2\omega t + V_0^2} \\ V_B(t) = V_C(t) - |V_{AC}(t)| \end{cases} \tag{5.1}$$

The steady-state waveform of I_A is equal to the sum of the rectified-unfolded grid current and the current flowing out of the capacitor:

$$\begin{cases} I_A(t) = |I_{AC}(t)| + I_C(t) = \sqrt{2}\frac{P}{V_{AC,RMS}}|\sin \omega t| + \frac{P\cos 2\omega t}{\sqrt{\frac{P}{\omega C}\sin 2\omega t + V_0^2}} \\ I_B(t) = -|I_{AC}(t)| \end{cases} \tag{5.2}$$

Both currents are periodical with a period equal to half grid period.

The first harmonic component of the capacitor current is similar in magnitude to the first harmonic of rectified grid current, and almost opposite in phase. Since the high-frequency bridge arm current I_A is the sum of the two, the result is that the current waveform has an high DC component and low AC ripple, leading to lower RMS and thus reduced losses. For example, using the same parameters as in figure 5.2, the RMS value of grid current and $I_{B,RMS}$ is 4.35 A, $I_{A,RMS}$ is 3.95 A and the RMS current of the capacitor is 1.86 A.

Rated power	P	1	kW
DC voltage	V_{DC}	450	V
AC voltage	V_{AC}	230	V_{RMS}
Power decoupling capacitor	C_{PD}	76	μF
C_{PD} DC offset voltage	V_0	375	V
Switching frequency	f	50	kHz
HFB filtering inductors	L_A	275	μH
	L_B	375	μH
AC filter	C_{AB}	1	μF
	L_{AC}	100	μH
DC filter	L_{DC}	500	μH
	C_{DC}	1	μF

Table 5.1: Double full bridge topology: Circuit parameters

5.1.2 Design of the power decoupling capacitor

Given the steady-state voltage waveforms shown in (5.1), it follows that, to avoid over-modulation, the instantaneous voltage across the power decoupling capacitor C_{PD} must be always lower than the DC voltage and always higher than the absolute value of grid voltage:

$$V_{AC}|\sin\omega t| < \sqrt{\frac{P}{\omega C_{PD}}\sin 2\omega t + V_0^2} < V_{DC} \tag{5.3}$$

It can be observed that since the voltage ripple across the capacitor is constrained by the DC-link voltage, choosing a higher voltage for the DC link leads to a higher energy utilization of the capacitor, i.e. the capacitor operates closer to the rated voltage. As a consequence, the capacitor will be smaller in size for a given nominal power of the converter. The choice of the rated DC link voltage is thus a compromise between the energy utilization of the power decoupling capacitor R_{E_C} and the voltage utilization ratio of the converter R_V, which are defined as follows:

V_{DC}	C_{MIN}	R_V	R_{E_C}
$400V$	$79\mu F$	81%	51%
$450V$	$48\mu F$	72%	65%
$500V$	$35\mu F$	65%	73%
$550V$	$27\mu F$	59%	79%
$600V$	$21\mu F$	54%	83%

Table 5.2: Power decoupling capacitor sizing

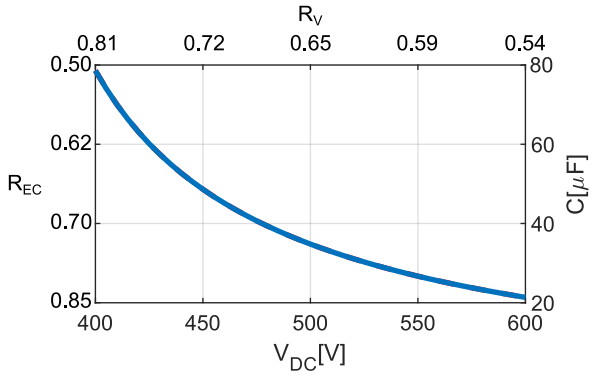


Figure 5.3: Power decoupling capacitor sizing

$$R_{E_C} = \frac{E_{C,MAX} - E_{C,MIN}}{E_{C,MAX}} = \frac{V_{C,MAX}^2 - V_{C,MIN}^2}{V_{C,MAX}^2} \qquad R_V = \frac{V_{AC,peak}}{V_{DC}} \tag{5.4}$$

The minimum value of capacitance that respects the constraints of (5.3) for different DC voltage levels can be numerically calculated [53], and are shown in Table 5.2, considering a nominal power of 1kW, AC line frequency of 50 Hz and voltage amplitude of $230V_{RMS}$. The values of capacitance reported in the table are the minimum values that respect the constraints in (5.3). Fig.5.3 shows on the x axis the DC voltage and the voltage ratio R_V, and on the y axis the minimum capacitance and the energy utilization ratio R_{E_C}.

The rated capacitance of the chosen power decoupling capacitor should be significantly higher than the theoretical minimum value, in order to take into account the capacitor tolerance and the effect of ageing on the capacitance, and to guarantee the correct behaviour of the converter both during transients and in case of a possible deviation of the AC and/or DC voltage amplitudes from their

nominal values.

A DC link voltage of 450V was chosen, being a good compromise between energy utilization ratio and voltage utilization ratio, which in this case is 72%. The corresponding minimum capacitance required for a rated power of 1kW is $48\mu F$. According to the need for a higher capacitor discussed in the previous paragraph, a capacitor of $76\mu F$ was chosen. The corresponding energy utilization ratio is about 46%.

5.1.3 Design of the high frequency filters

The discussion presented so far referred to the waveshaping of voltages and currents in the converter averaged over a switching period. This is because the ripple compensation deals with low frequency components and the the analysis can, in first approximation, neglect the high frequency switching components. However, the design of the filter inductors L_A, L_B and of the filter capacitor C_{AB} must be based on those harmonics.

The design of the inductors is based on the fact that both L_A and L_B are connected between the one leg of the HFB and two equivalent voltage sources represented by different combinations of the voltages across C_{AB} and C_{PD}. In the assumption of both capacitors having negligible voltage ripple, the voltage across each filter inductor $L_i, i = A, B$ can be calculated, knowing the duty cycle $d_i, i = A, B$ of each leg of the HFB, the switching frequency f and the dc-link voltage V_{DC}. The duty cycles are defined as the ratio between the period during which the upper switch of each leg is closed and the switching period. The resulting ripple current is a triangular wave with a peak-to-peak amplitude of:

$$\Delta I_i = \frac{V_{DC}}{f L_i} d_i (1 - d_i) \tag{5.5}$$

Fig.5.4 shows the ripple current envelope flowing in the HFB arms, calculated using the steady-state voltages expressed in (5.1) to calculate the duty cycles d_i, an inductor L_A equal to $275\mu H$ and L_B equal to $375\mu H$. With this specific choice of L_A and L_B, the absolute value of the peak current in both arms, that

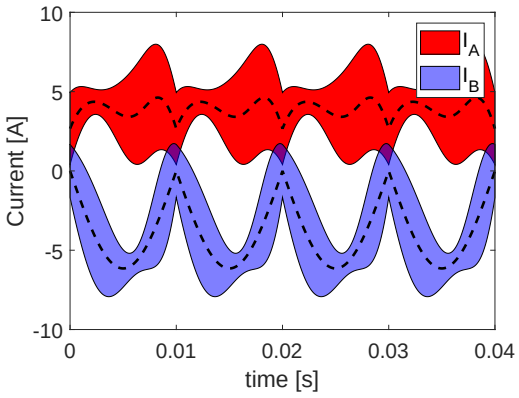


Figure 5.4: Ripple current envelopes on HFB arms: $f = 50kHz$, $L_A = 275\mu H$, $L_B = 375\mu H$, $P = 1kW$

is the sum of the triangular switching ripple component and the low-frequency component as calculated in (5.2), is the roughly the same and equal to about $8A$ at nominal power. A low peak current is an advantage since it allows the use of inductors having a low saturating current, reducing the size and cost of the magnetic components.

Finally, the design of the capacitor C_{AB} is based on a consideration about the operation of the LFB. Since the bridge uses simple MOSFETs with antiparallel diodes, it can only accept positive voltages at its DC terminals. In the proposed topology, the DC voltage of the LFB corresponds to the voltage across C_{AB}, that has a low frequency component equal to the rectified AC voltage $V_{AC}(t)$. If the voltage at the DC input of the LFB changes sign, the antiparallel diodes in the bridge start to conduct. If that happens, the current I_B starts flowing in the capacitor C_{PD} and the control of grid current would be lost.

The low-frequency component of the voltage applied to C_{AB}, equal to $|V_{AC}| = V_A - V_B$ as defined in (5.1), is always positive. However, the voltage ripple generated by the switching components of the current I_B can drive the voltage negative in the intervals where the low frequency component of the modulated voltage $|V_{AC}|$ is close to zero, around the zero crossing of grid voltage. In those intervals, diode conduction may occur. Therefore, the value of C_{AB} is chosen in order to reduce its voltage ripple to acceptable magnitudes.

Assuming all the high-frequency ripple of I_B to flow in capacitor C_{AB}, the peak-to-peak amplitude of the resulting voltage ripple can be calculated as follows:

$$\Delta V_{C_{AB}} = \frac{1}{4}\frac{\Delta I_B}{f C_{AB}} \tag{5.6}$$

In this case ΔI_B is calculated from (5.5), using the duty-cycle applied at the zero crossing of grid voltage, that is V_0/V_{DC}. The peak-to-peak value of such current is $2.1A$. Choosing a C_{AB} equal to $1\mu F$ results in a peak-to-peak ripple voltage at the zero-crossing of grid voltage equal to about 10V. Such value is low enough not to cause any noticeable distortion on grid current, as shown later in the experimental results.

On the DC side of the converter, the LC filter formed by L_{DC} and C_{DC} is sized to remove the high-frequency ripple from the DC current. Choosing $C_{DC} = 1\mu F$ and $L_{DC} = 500\mu H$ results in a cutoff frequency of about $10kHz$, which is sufficient to remove the switching frequency components on I_{DC}. The choice of using a a large inductor and a relatively small DC link capacitor is made on purpose, in order to highlight the correct behaviour of the active power ripple decoupling of the converter, since the contribution of the DC link capacitor in the compensation of the power ripple at twice the grid frequency is in this case negligible.

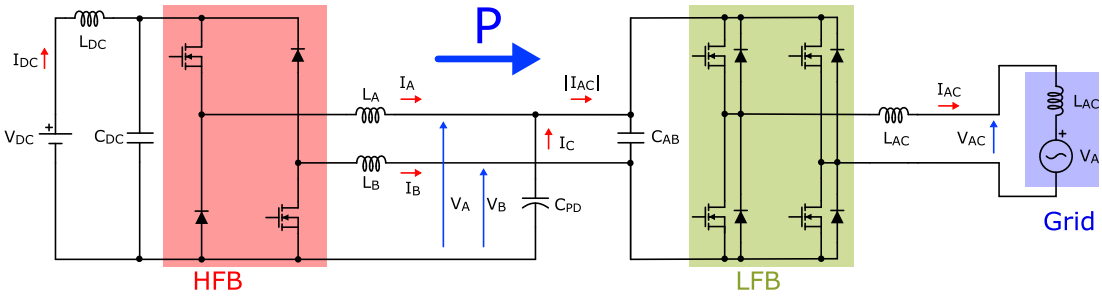
5.1.4 Unidirectional power

If, as first approximation, the voltage ripple on the power decoupling capacitor is neglected, it follows that the currents I_A and I_B are linearly dependent on power, as shown in (5.7).

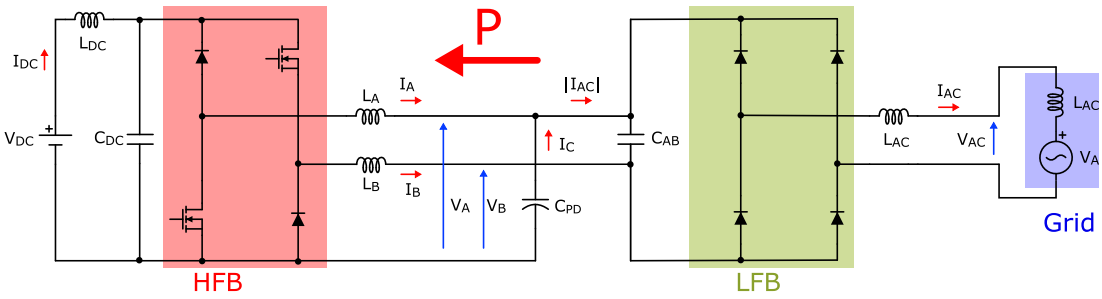
$$I_A(t) = I_{AC}(t) + I_C(t) = \sqrt{2}\frac{P}{V_{AC,RMS}}|\sin(\omega t)| + \frac{P\cos(2\omega t)}{\sqrt{\frac{P}{\omega C}\sin 2\omega t + V_0^2}} \tag{5.7}$$

$$\simeq P\left[\frac{\sqrt{2}}{V_{AC,RMS}}|\sin(\omega t)| + \frac{\cos(2\omega t)}{V_0}\right] \tag{5.8}$$

$$\frac{\sqrt{2}}{V_{AC,RMS}}|\sin(\omega t)| + \frac{\cos(2\omega t)}{V_0} > 0 \quad \Rightarrow \quad \sqrt{2}\frac{V_0}{V_{AC,RMS}} > -\frac{\cos(2\omega t)}{|\sin(\omega t)|} \tag{5.9}$$



(a) AD-DC converter (unfolder)



(b) DC-AC converter (rectifier, only two active devices)

Figure 5.5: Unidirectional power topologies

It is easy to see that the condition in 5.9 is verified with an ample margin, since V_0 is chosen to be 400V, while $V_{AC,RMS}$ is 230V, so their ratio is higher than 1. It can be proven by numerical calculations that the condition is verified even if the capacitor voltage ripple is not neglected.

The current I_A always has the same sign as the power P, while I_B has an opposite sign. Since unidirectional current is achieved if unidirectional power is required, it is possible to reduce the number of active devices, especially in case of rectifier operation, as shown in fig.5.5.

Although these solutions are potentially more reliable and inexpensive compared to the bidirectional topology having all the active components, they exhibit a lower efficiency, due to the higher conduction losses on the diodes, and therefore are suitable for low nominal powers, or in applications where cost and reliability are more important than efficiency.

5.1.5 Power losses analysis

A numerical estimation of the converter losses was performed, using Matlab-Simulink and PLECS.

The losses occurring in the DFBC can be divided in the following components:

- Switching losses in the HFB switches;
- Conduction losses in the HFB switches;
- Conduction losses in the LFB switches;
- Winding and core losses in the filtering inductors L_A and L_B.

Switching losses

Switching losses in the HFB switches are calculated based on the method exposed in [54]:

$$E_{ON} = \frac{1}{2} U_{DD} I_{Don} \left[t_r + \frac{C_{rss}(0) + C_{rss}(U_{DD})}{2} R_g \frac{U_{DD}}{U_{dr} - U_{plateau}} \right] + Q_{RR} U_{DD} \tag{5.10}$$

$$E_{OFF} = \frac{1}{2} U_{DD} I_{Don} \left[t_f + \frac{C_{rss}(0) + C_{rss}(U_{DD})}{2} R_g \frac{U_{DD}}{U_{plateau}} \right] \tag{5.11}$$

where:

- C_{rss} is the equivalent gate-source capacitance;
- R_g and U_{dr} are the gate resistor and the gate driver power supply voltage;
- U_{DD} and I_{Don} are the instantaneous voltage and current prior to the switching action;
- Q_{RR} is the reverse recovery charge of the diode.

$$P_{SW} = \sum_k (E_{ON} + E_{OFF}) f_{sw} \tag{5.12}$$

The parameters used for calculating losses are extracted from the datasheet of the devices, that are SiC MOSFETs (C3M0120090J by Cree/Wolfspeed) for the HFB and Si MOSFETs (IPB65R110CFD by Infineon) for the LFB.

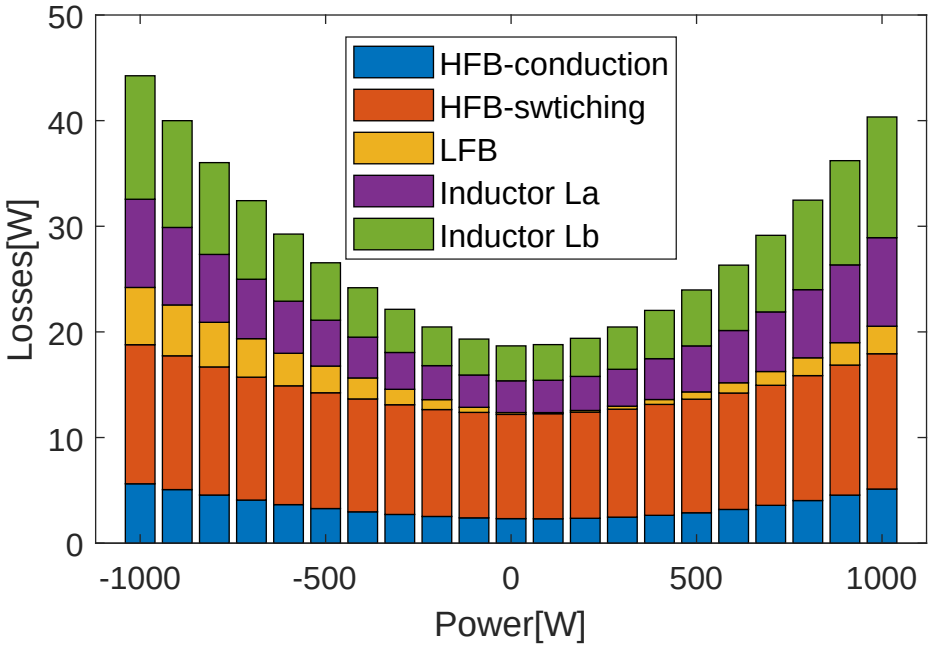


Figure 5.6: Power losses distribution

Conduction losses

Conduction losses in both the HFB and the LFB active devices are calculated considering the $R_{DS,ON}$ of the mosfets and both the threshold voltage and equivalent resistance of the diode, taken from the datasheet.

The losses occurring in the DC link capacitor and in other passives were neglected.

Conduction losses occurring in the windings of the filtering inductors L_A, L_B, and L_{FG} are calculated neglecting skin effect. In order to reduce the losses due to skin effect, the windings were manufactured using five small section magnetic wires in parallel instead of a single thicker wire.

Results

The calculated power losses distribution for different power levels is shown in Fig.5.6. The results indicate an efficiency at nominal power of about 96% in inverter mode and 94% in rectifier mode.

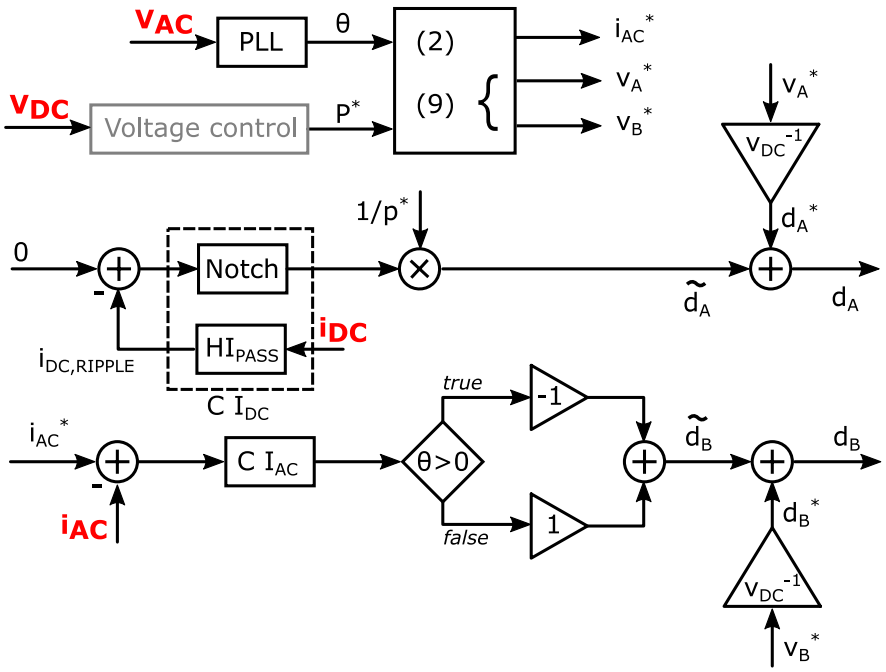


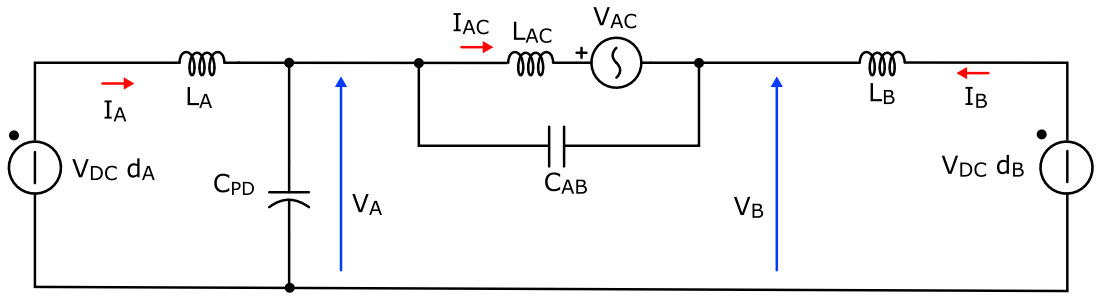
Figure 5.7: Control structure. Measured signals are written in red.

5.2 Control

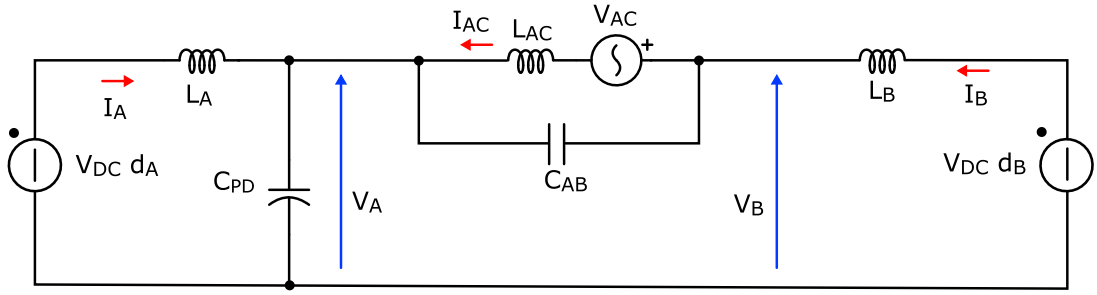
The control architecture is designed with the aim of minimizing complexity. The control is able to achieve an effective control of the AC current, in order to follow a required AC power reference P^*, and at the same time apply a closed loop compensation on the DC current ripple.

The control system is modelled as a MIMO with two inputs, the duty cycles d_A and d_B of the two legs of the HFB, and two outputs, the AC current i_{AC} and the ripple component of the DC current $i_{DC,RIPPLE}$. The control of the converter can be split so that one PWM bridge leg can be used to control the voltage V_A across the power ripple decoupling capacitor, while the other leg controls the grid current according to the desired P, independently. This is made possible by the size of the power decoupling capacitor C_{PD}, that prevents the action of the first bridge leg to quickly affect the AC grid current, thus effectively decoupling the control structure.

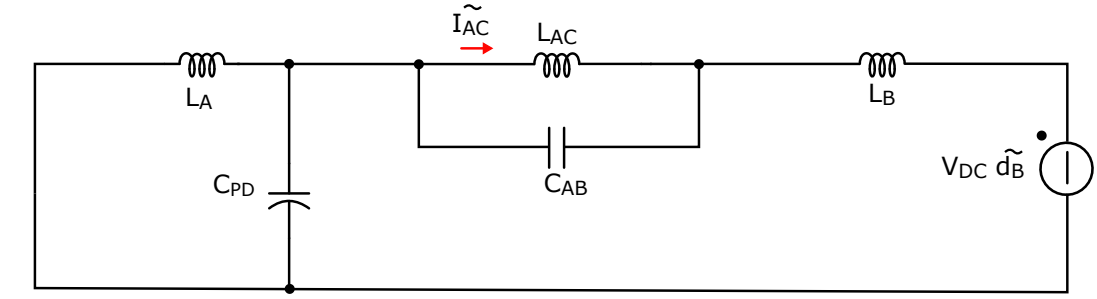
The control architecture is shown in Fig. 5.7. In this case, the reference power P^* is an input, however, depending on the application, it can be the output of an outer control loop that controls the DC voltage V_{DC}, such as, for example,



(a) Large signal model, mode A



(b) Large signal model, mode B



(c) Small signal model

Figure 5.8: AC current control models

an MPPT controller if the proposed converter is used as grid interface for solar power systems.

Since the steady-state waveforms of the voltages V_A^* and V_B^* are known analytically from the operating point according to (5.1), their values are added as *feed-forward* terms to the output of the AC and DC controllers. The implementation of the *feed forward* of V_B is particularly helpful for the provision of the high-frequency components of its waveform.

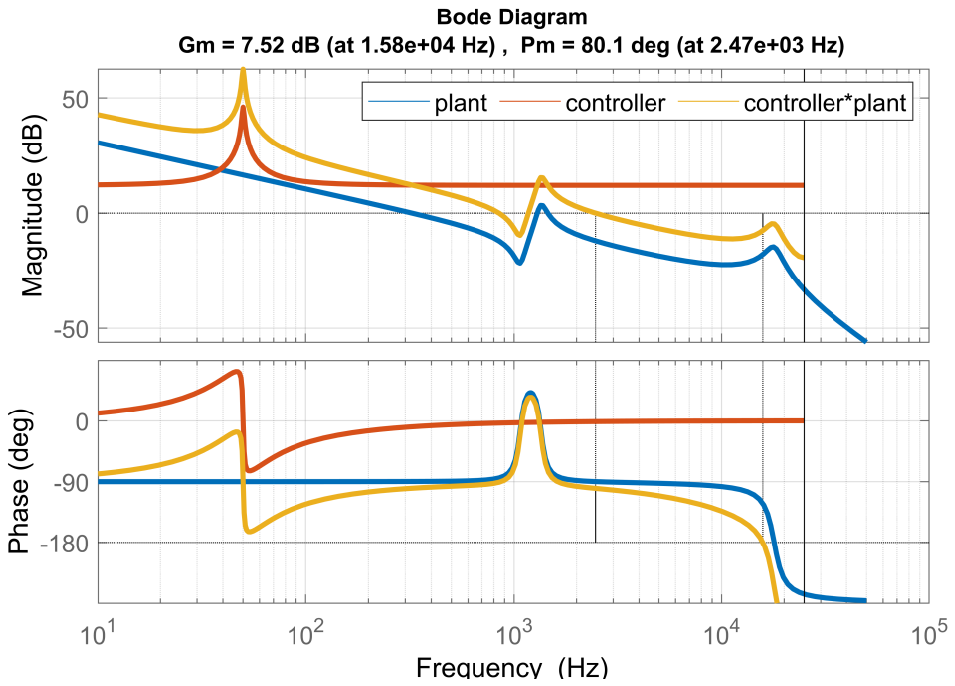


Figure 5.9: Bode plot, I_{AC} control

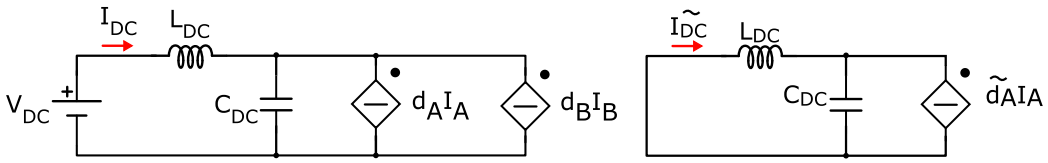
5.2.1 AC current control

As described in Section 5.1, as far as the AC current control is concerned, the converter operates in two different modes according to the state of the LFB. The large signal equivalent circuits for each mode are shown in Fig. 5.8a and 5.8b.

In both modes, from a small signal perspective, the action of the high frequency component of the voltage $V_{DC}\, d_A$ on the grid current is neglected, because of the filtering action of C_{PD}.

The transfer function is the same for the two modes, with the exception of the sign. The state of the system is identified by the currents I_{AC} and I_B flowing in the inductors L_{AC} and L_B and the voltage V_{AB} applied across the capacitor C_{AB}. Since the transition between each mode happens at the zero-crossing of the converter AC voltage V_{AC} and in the assumption of unity power factor operation, I_{AC}, I_B and V_{AB} are all close to zero during the transition. For this reason, the state of the system is not affected by the mode change.

Assuming to correct the sign of the AC current controller output by inverting it during mode A, the resulting equivalent circuit, valid in both modes, is shown



(a) Large signal model (b) Small signal model

Figure 5.10: DC ripple current control models

in Fig. 5.8c, where $\tilde{d_B}$ is the small signal component of the duty-cycle of leg B. The system is thus similar to a generic voltage source converter connected to the grid via a LCL filter, with an additional double pole and zero pair due to the presence of C_{PD} and L_A. The transfer function of the plant is the following:

$$\frac{\tilde{I_{AC}}}{\tilde{d_B}} = \frac{1}{s(L_B + L_{AC})} \frac{s^2/\omega_Z^2 + 1}{(s^2/\omega_{P1}^2 + 1)(s^2/\omega_{P2}^2 + 1)} \tag{5.13}$$

Where:

$$\omega_{Z1} = (C_{PD} L_A)^{-0.5} \qquad f_{Z1} = \frac{\omega_{Z2}}{2\pi} \simeq 1.07kHz \tag{5.14}$$

$$\omega_{P1} = \left(C_{PD} \frac{L_A(L_B + L_{AC})}{L_A + L_B + L_{AC}} \right)^{-0.5} \qquad f_{P1} = \frac{\omega_{P1}}{2\pi} \simeq 1.35kHz \tag{5.15}$$

$$\omega_{P2} = \left(C_{AB} \frac{L_B L_{AC}}{L_B + L_{AC}} \right)^{-0.5} \qquad f_{P2} = \frac{\omega_{P2}}{2\pi} \simeq 18kHz \tag{5.16}$$

The chosen current controller is a PR resonating at grid frequency. The controller is able to damp the resonant pole at $1.35kHz$, while the damping of the resonant pole at $18kHz$ is passive. Sufficient passive damping is obtained without excessive power losses thanks to the non-linear dissipative behaviour of the magnetic components, that show a higher equivalent series resistance at high frequencies. The bode plot of the plant and the proposed controller is shown in Fig.5.9.

5.2.2 DC ripple current control

Assuming the DC filter to completely filter out the switching frequency components, the DC current I_{DC} is approximated to:

$$I_{DC} \approx \frac{1}{s^2/\omega_{DC}^2 + 1} (d_A I_A + d_B I_B) \tag{5.17}$$

where $\omega_{DC} = (L_{DC}\, C_{DC})^{-0.5} \simeq 4.5kHz$.

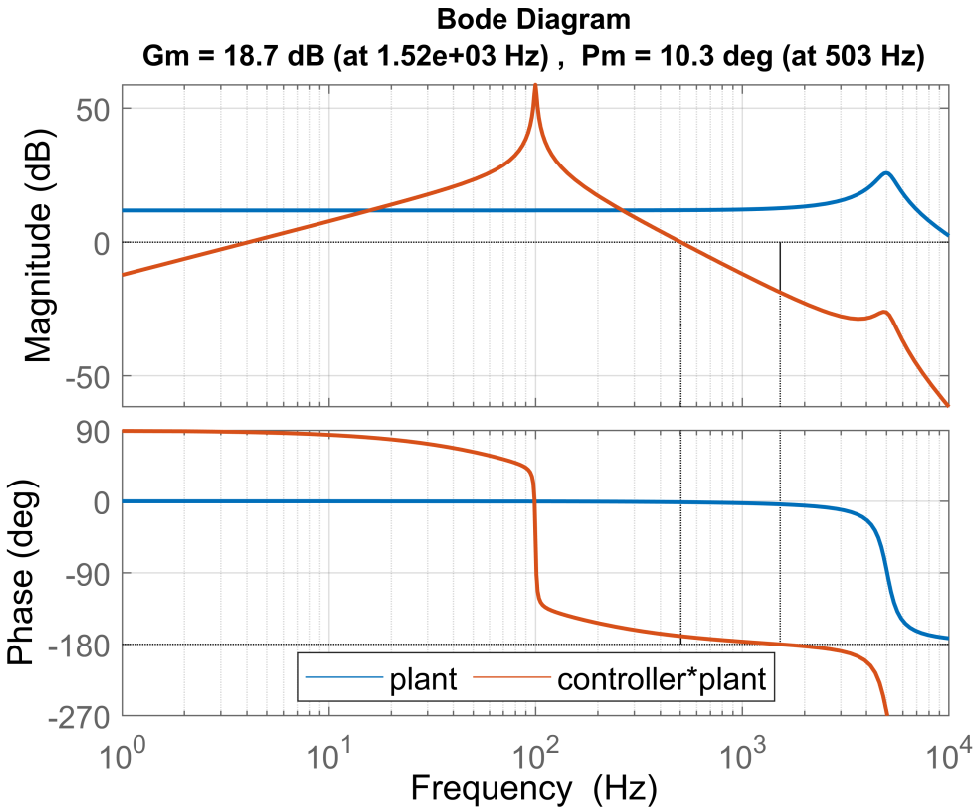


Figure 5.11: Bode plot of I_{DC} plant and controller

Since the mean value of the current I_A at nominal power is 3.9A and varies linearly with the power P, the small signal transfer function for $\tilde{I_{DC}}$ is:

$$\frac{\tilde{I_{DC}}}{\tilde{d_A}} = 3.9\, p^* \, \frac{1}{s^2/\omega_{DC}^2 + 1} \tag{5.18}$$

Where p^* is the reference power expressed in per units.

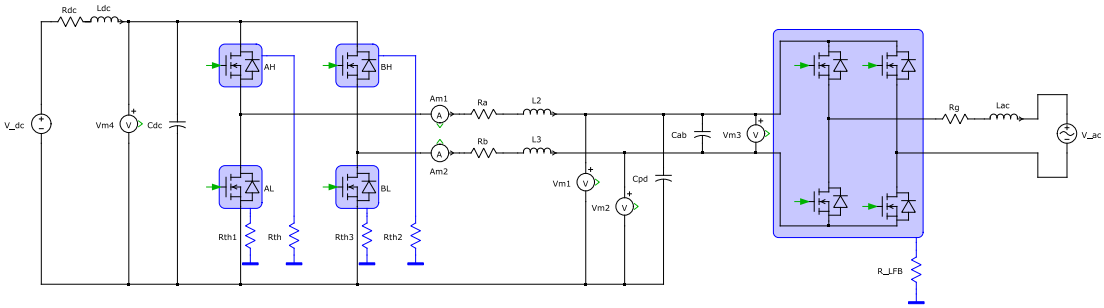
Assuming to control the DC current ripple by acting on the duty-cycle d_A, and neglecting the action of the DC filter, the DC control system can be modelled as in Fig.5.10. The target of the controller is to set to zero the ripple components of I_{DC} so that the current pulsation at twice the grid frequency is removed from the DC-link in closed loop. Therefore, a high-pass filter cascaded with a notch tuned at 100Hz is used for the DC current ripple controller. The transfer function of the controller is the following:

$$C_{I_{DC}}(s) = 0.01 \frac{s}{s/(2\pi 100) + 1} \frac{1}{s^2/(2\pi 100)^2 + 1} \tag{5.19}$$

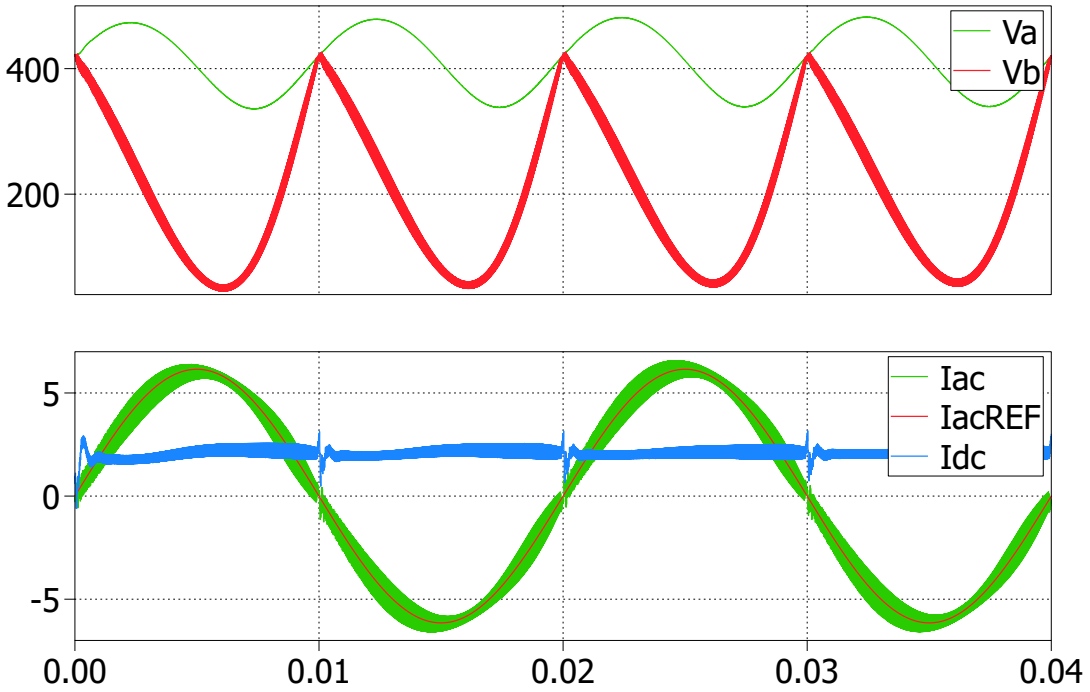
Since the current I_A is not constant, the gain of the DC ripple current control loop changes significantly over time and a good gain margin of the controller is

required. The proposed controller has a gain margin of 18.7dB, with a cut-off frequency of 500Hz, as shown in Fig. 5.11.

5.3 Simulation results



(a) Model



(b) Results, P_{REF}=1kW

Figure 5.12: DFBC: PLECS simulation

In order to test the control algorithm and to calculate power losses, a time-domain simulation of the proposed topology was made using Matlab-Simulink together with the PLECS toolbox.

The simulation proves the correct behaviour of the control system.

5.4 Comparison with state-of-the-art topologies

In this Section, the performances of the DFBC are compared with those of the state-of-the-art topologies discussed in Chapter 2.

As can be seen in the comparison table 5.3, the DFBC proves to be an interesting solution as topology for single phase AC-DC converter, both in terms of FOM and on DC utilization ratio.

The presence of the unfolder-rectifier bridge constitutes a drawback of this topology, compared to other solutions that do not make use of it, both for the additional cost and reduced reliability due to the higher number of active devices, and in terms of reduced efficiency, due to the conduction losses in the bridge, especially in case of rectifier mode, if synchronous rectification is not applied. On the other hand, the destructive interference exploited in this topology translates in reduced conduction losses in the power decoupling capacitor arm of the HFB.

The efficiency of the DFBC is acceptable if compared with the other topologies of table 5.3, however, efficiency is highly dependent on several design parameters, such as the switching frequency, the choice of the switching devices, the core material used for the filtering inductors; for this reason, comparing different topologies in terms of efficiency is not particularly significant. Conversely, the FOM is particularly significant since it derives from voltage constraints on the power decoupling capacitor that are inherent in the topology.

	Nominal Power $[kW]$	Number of devices	DC port voltage $[V]$	DC bus voltage $[V]$	AC port voltage $[V_{RMS}]$	Frequency $[Hz]$	Power dec. Capacitance $[\mu F]$	Efficiency %	DC util. ratio %	FOM %
Wang *et.al.* [1]	15	6	540	540	150	233	200	93	39	35(100)*
Breazeale*et.al.* [2]	1	6	200-550	700	240	60	2·102	97	48	11
Xia *et.al.* [6]	1	4	200-475	950	120	60	45	96	18	13
Zhong *et.al.* [3]	1	4	400	400	110	50	30	92	39	13
Tang *et.al.* [5]	1	3+5diodes	380	380	110	60	2·90	93	41	40
Tang *et.al.* [4]	.5	4	250	250	110	60	2·60	96	62	35
DFBC	1	4+4 slow	450	450	230	50	76	95	72	42

Table 5.3: Comparison between state-of-the-art single phase topologies and DFBC

5.5 Conclusions

In this chapter, a topology, named Double Full Bridge Converter (DFBC) was introduced and described. A design procedure for its passive components is included, together with a control structure and losses analysis. The correct behaviour of the control system is confirmed by time-domain simulations.

In order to validate the simulation results, an experimental setup was built. The description of the hardware implementation of the topology and the experimental results are presented in Section 9.2.

In the next chapter, another proposed topology for a single phase grid front-end is presented.

Chapter 6

Proposed topology: Jumping Capacitor Converter

In this chapter, an AC-DC converter topology, named "Jumping Capacitor Converter" (JCC), is introduced and analysed.

As for the DFBC, this topology is intended for use as grid front-end, able to interface a DC microgrid, a PV panel system and-or a battery storage system to a single-phase AC connection.

A destructive interference involving the power decoupling capacitor current and the rectified grid current is exploited here as well, as in the DFBC, however, this topology does not include a low-frequency full bridge, requiring only two low-frequency switches instead of four.

This topology has the capability of providing a good filtering of leakage currents, requiring a small or no additional common mode filter; for this reason, it is suitable to use as grid front-end for transformerless PV systems.

A design procedure for the passive component is discussed, and the common mode currents filtering capability inherent in the topology is discussed. Control structure is described and validated with time-domain simulations. Extensive experimental results are recorded, and are shown in chapter 9.

This chapter is structured as follows. Section 6.1 describes the proposed topology, explaining its operating principles and proposing a design method for

the power decoupling capacitor and for the other passive components; section 6.2 analyses the behaviour of the topology in terms of common mode current filtering; section 6.3 describes the proposed control scheme, and finally section 6.4 shows the simulation results.

6.1 Theory of operation

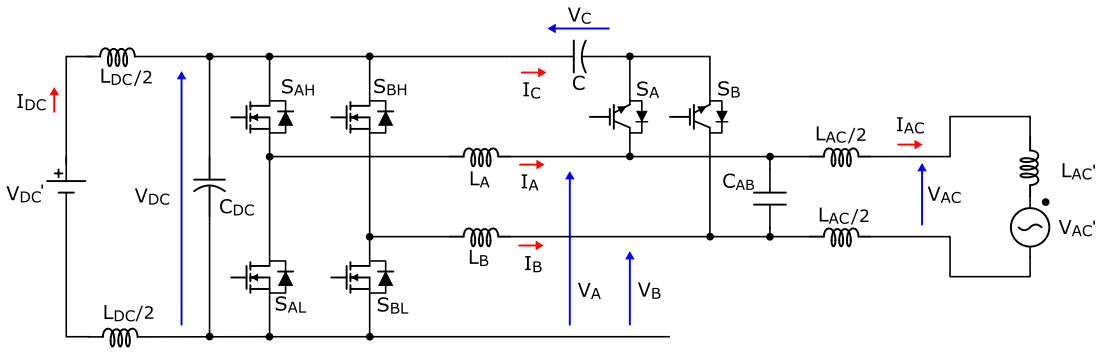


Figure 6.1: Proposed topology

The JCC is depicted in Fig.6.1: it consists of one H-bridge, formed by S_{AH}, S_{AL}, S_{BH} and S_{BL}, a DC filter including L_{DC} and C_{DC}, an AC filter formed by L_{AC} and C_{AB}, inductors L_A and L_B, the power decoupling capacitor C and two additional active switches S_A and S_B. The switches in the H-bridge are modulated at high frequency, while the additional two switches are soft switched at the grid frequency.

The DC port of the converter is connected to the terminals of the H-bridge as in a standard H-bridge DC/AC converter. One terminal of the power decoupling capacitor C is connected to the positive DC rail of the bridge, while the other is alternatively connected to one of the two inductors L_A, L_B, by the action of S_A and S_B.

Two operating modes are defined, as shown in figure 6.2, according to the state of the switches S_A and S_B. In both operating modes, the voltage applied to the converter side of the AC filter is the differential voltage modulated by the H-bridge, that is used to control grid current. Since the power decoupling capacitor branch is alternatively connected between the positive DC link and one of the

Rated power	P	1	kW
DC voltage	V_{DC}	450	V
AC voltage	V_{AC}	240	V_{RMS}
	f_{AC}	50	Hz
Power decoupling capacitor	C	76	μF
C_{PD} DC offset voltage	V_0	385	V
Switching frequency	f	100	kHz
Filtering inductors	L_A, L_B	130	μH
AC filter	C_{AB}	2	μF
	L_{AC}	300	μH
DC filter	L_{DC}	10	μH
	C_{DC}	10	μF

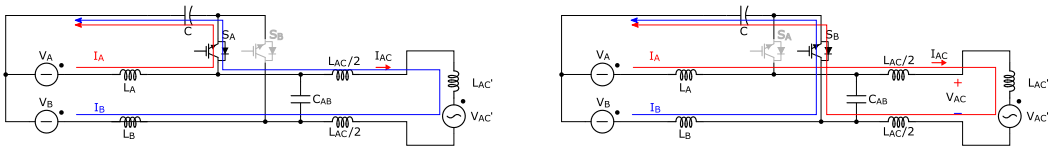
Table 6.1: JCC Circuit parameters

modulated output of the H-bridge, its voltage can be controlled independently from the voltage applied to the grid. By applying an opportune voltage waveform to the power decoupling capacitor, as explained in section 6.1.1, the capacitor is able to provide a ripple power that cancels out the 100Hz power pulsation inherent in the single phase AC connection, effectively eliminating the 100Hz DC current ripple, without the need for a big DC link capacitor.

6.1.1 Steady state analysis

In order to illustrate the steady state operation of the JCC, the ideal average steady-state waveforms of the significant currents and voltages are discussed, neglecting the switching frequency ripple.

The energy storage function required to decouple the ideal power flows sought at DC and AC ports is accomplished by the capacitor C. The other reactive elements in the circuit are designed to filter switching harmonics and store a negligible amount of energy. Assuming ideal AC port quantities, *i.e.* sinusoidal voltage and current at unity power factor, the ideal voltage waveform $V_{PD}(t)$



(a) Mode A: S_A on, S_B off, $V_{AC} < 0$ (b) Mode B: S_A off, S_B on, $V_{AC} > 0$

Figure 6.2: Operating modes

across C and its current $I_{PD}(t)$ in order to obtain ripple power cancellation, can be derived from the basic AC/DC power balance and are shown in (6.1).

$$V_{PD}(t) = \sqrt{\frac{P}{\omega C}\sin 2\omega t + V_0^2} \qquad I_{PD}(t) = \frac{P\cos 2\omega t}{\sqrt{\frac{P}{\omega C}\sin 2\omega t + V_0^2}} \tag{6.1}$$

Where P is the active power, ω is the AC pulsation, and V_0 is an arbitrary DC offset applied to the decoupling capacitor, as shown in [53].

The switches S_A and S_B change state at each zero crossing of the AC voltage, as shown in Fig.6.2:

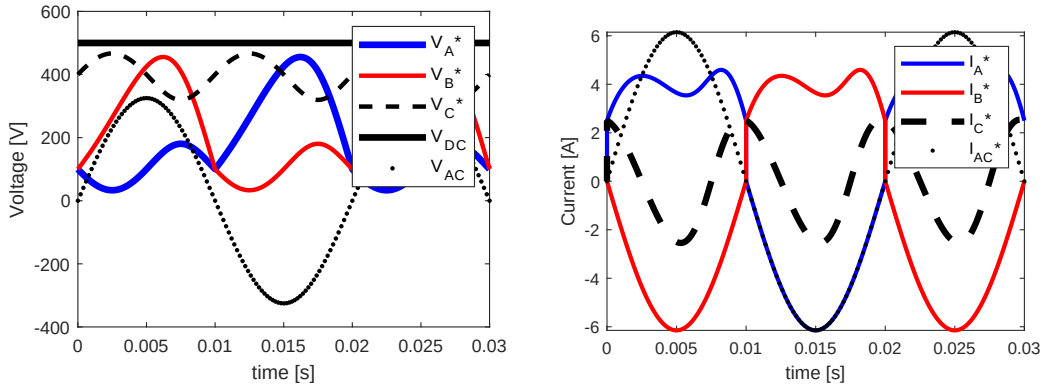
$$\begin{cases} V_{AC} \leq 0 & \text{MODE A: } S_A \text{ closed, } S_B \text{ open} \\ V_{AC} > 0 & \text{MODE B: } S_A \text{ open, } S_B \text{ closed} \end{cases} \tag{6.2}$$

The state of S_A and S_B is selected so that the negative terminal of the power decoupling capacitor C is always connected to the node having the lower voltage with respect to the DC bus.

In order to drive the voltage across C to the one needed for power decoupling, the ideal voltages V_A^* and V_B^* modulated by the half bridges formed respectively by S_{AH} and S_{AL}, S_{BH} and S_{BL} must be the following, where the action of S_A and S_B is taken into account:

$$V_A^*(t) = \begin{cases} V_{DC} - V_{PD}(t) & V_{AC} \leq 0 \\ V_{DC} - V_{PD}(t) + V_{AC}(t) & V_{AC} > 0 \end{cases} \tag{6.3}$$

$$V_B^*(t) = \begin{cases} V_{DC} - V_{PD}(t) - V_{AC}(t) & V_{AC} \leq 0 \\ V_{DC} - V_{PD}(t) & V_{AC} > 0 \end{cases} \tag{6.4}$$



(a) Steady state voltages

(b) Steady state currents

Figure 6.3: Steady-state voltages and current waveforms ($V_{DC} = 500V$, $P = 1kW$, $C = 55\mu F$)

Depending on the state of S_A and S_B, the steady-state waveform of the current flowing in the bridge arm is equal either to the grid current I_{AC}, or to the sum of I_{AC} and I_{PD}:

$$I_A^*(t) = \begin{cases} I_{AC}(t) - I_{PD}(t) & V_{AC} \leq 0 \\ I_{AC}(t) & V_{AC} > 0 \end{cases} \tag{6.5}$$

$$I_B^*(t) = \begin{cases} -I_{AC}(t) & V_{AC} \leq 0 \\ -I_{AC}(t) - I_{PD} & V_{AC} > 0 \end{cases} \tag{6.6}$$

$$I_C^*(t) = -I_A^*(t) - I_B^*(t) = I_{PD}(t) \tag{6.7}$$

Both voltages and currents are periodical with a period equal to the AC grid period. The steady state values are shown, for a specific operating point, in Fig.6.3.

Since S_A and S_B are operated at the zero crossing of the grid voltage, it follows that in case of unity power factor, the current flowing in the bridge arms is equal to ether the grid current I_{AC} or the current I_X, defined in (6.8).

$$I_X(t) = \begin{cases} -I_{AC}(t) - I_{PD}(t) & V_{AC} > 0 \\ I_{AC}(t) - I_{PD}(t) & V_{AC} \leq 0 \end{cases} = -\frac{P\cos 2\omega t}{\sqrt{\frac{P}{\omega C}\sin 2\omega t + V_0^2}} - \sqrt{2}\frac{P}{V_{AC,RMS}}|\sin \omega t| \tag{6.8}$$

From the Fourier series of the power decoupling capacitor current in Fig. 6.3 it can be seen that the first harmonic component of I_C is similar in magnitude to the first harmonic of the rectified grid current, and almost opposite in phase. For this reason, the sum of the two results in a current waveform that has an high DC component and low AC ripple, reducing the RMS value. For example, using the same parameters as in Fig.6.3, the RMS value of grid current is 4.35 A, while the RMS of $I_X(t)$ is 3.95 A. Since the current flowing in the bridge arms is equal to $I_{AC}(t)$ in one semi-period and to $I_X(t)$ in the other, it follows that its RMS across the entire period is slightly lower than the RMS of grid current alone (4.15 A).

This result is particularly relevant, considering the fact that, in other existing topologies where the control of the voltage of one or more power decoupling capacitors is achieved using the same bridge that controls grid current, the RMS current flowing in the bridge arms is often significantly higher than the RMS of the grid current [3, 4].

6.1.2 Power decoupling capacitor sizing

The power decoupling capacitor voltage constraints are the same as the DFBC, consequently, the design of the capacitor is subjected to the same considerations described in the previous chapter.

As for the previous topology, a DC link voltage of 450V was chosen, having a voltage utilization ratio of 72%. The corresponding minimum capacitance required for a rated power of 1kW is $48\mu F$. A capacitor of $76\mu F$ was chosen. The corresponding energy utilization ratio is 46%.

6.2 Leakage currents

As described in chapter 3, if the converter is used to interface PV systems with the grid, leakage current occur, because of the presence of stray capacitance between the PV active elements and its chassis, which is connected to ground.

The equivalent circuit for the resulting common mode currents is shown in fig.6.4.

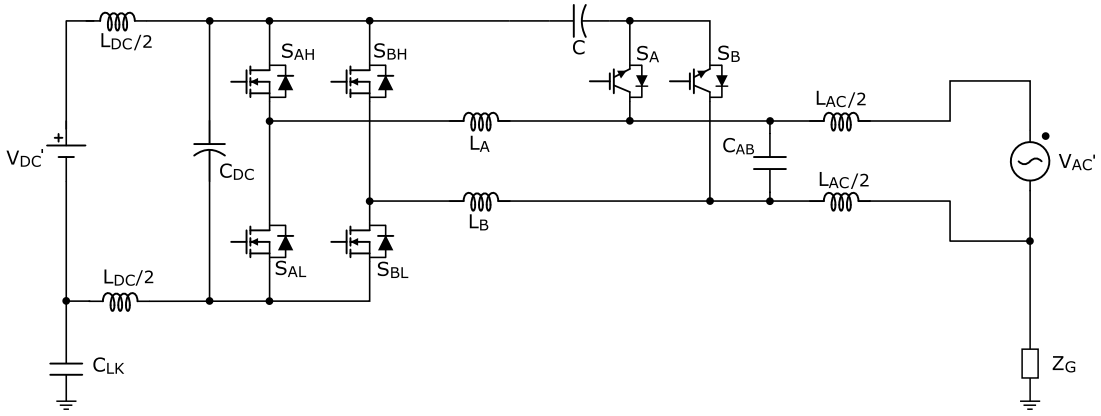
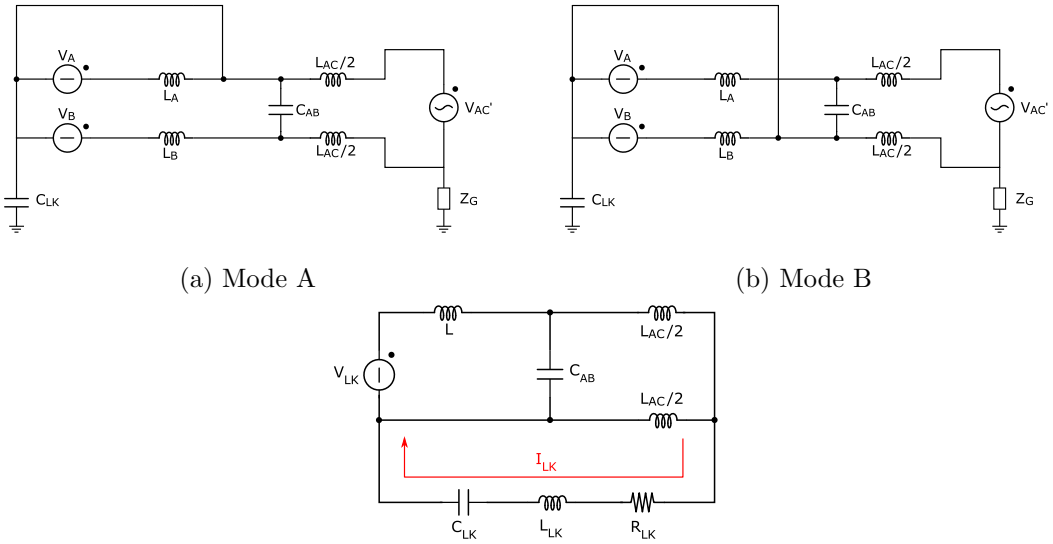


Figure 6.4: Leakage currents circuit model

Because of the size of the power decoupling capacitor, it can be considered as a short circuit at switching frequency, therefore, neglecting the stray resistance of the switches S_A and S_B, the equivalent circuit for common mode currents can be reduced, for both operating modes, to the one shown in fig.6.5.

$$V_{LK}(t) = \begin{cases} V_B(t) & V_{AC} \leq 0 \\ V_A(t) & V_{AC} > 0 \end{cases} \tag{6.9}$$

The transfer function in $\frac{I_{LK}(s)}{V_{LK}(s)}$ is obtained in reference to the equivalent circuit shown in Fig.6.5c. The magnitude of $\frac{I_{LK}}{V_{LK}}$, is about -80dBS at 100kHz. This value is obtained choosing L_A, $L_B = 130\mu H$, and C_{AB} equal to $2\mu F$, while the ground resistance is 5Ω. The bode plot of the transfer function, for different values of capacitance C_{LK}, is shown in fig.6.6.



(a) Mode A

(b) Mode B

(c) Equivalent circuit, valid for both modes

Figure 6.5: Leakage currents equivalent circuits

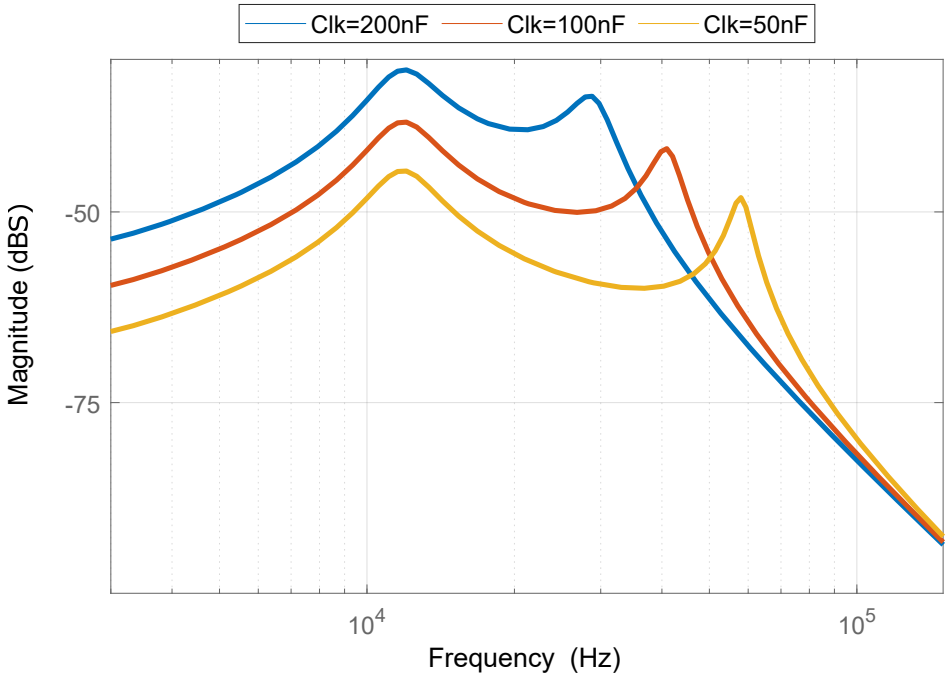


Figure 6.6: Common mode current impedance

6.3 Control

The control architecture is shown in Fig.6.7. The main difference in comparison to the control structure of the DFBC is the change that occurs during mode transitions, where the output of the controllers is alternated between the two legs of the full bridge.

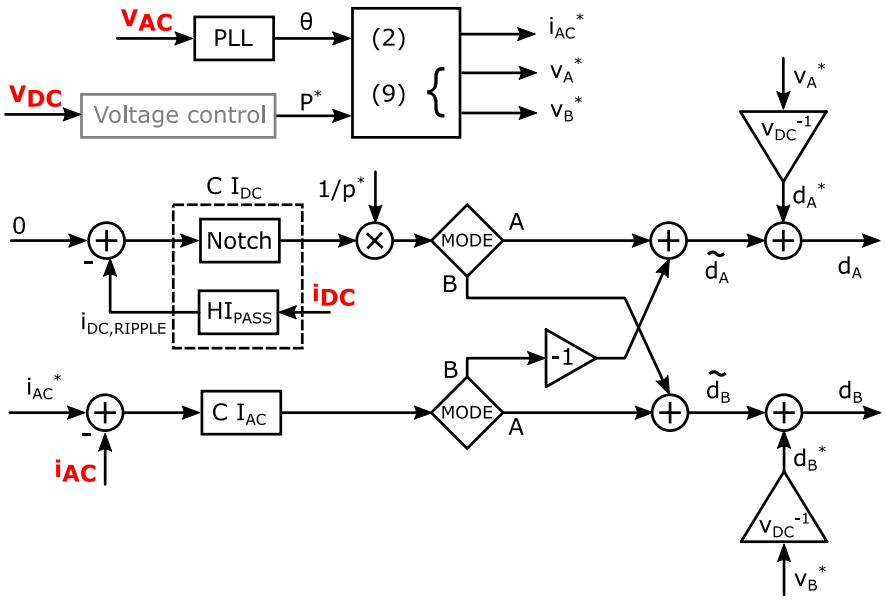


Figure 6.7: Control structure. Measured signals are written in red.

6.3.1 AC current control

As described in Section 6.1, the converter operates in two different modes according to the state of the switches S_A and S_B.

The large signal equivalent circuits for each mode are shown in Fig. 6.8a and 6.8b. The transfer function is the same for the two modes, with the exception of the sign, in the same way as for the DFBC.

$$\frac{\tilde{I_{AC}}}{\tilde{d_B}} = -\frac{1}{s(L+L_{AC})}\frac{s^2/\omega_Z^2+1}{(s^2/\omega_{P1}^2+1)(s^2/\omega_{P2}^2+1)} \qquad MODE\ A \qquad (6.10)$$

$$\frac{\tilde{I_{AC}}}{\tilde{d_A}} = \frac{1}{s(L+L_{AC})}\frac{s^2/\omega_Z^2+1}{(s^2/\omega_{P1}^2+1)(s^2/\omega_{P2}^2+1)} \qquad MODE\ B \qquad (6.11)$$

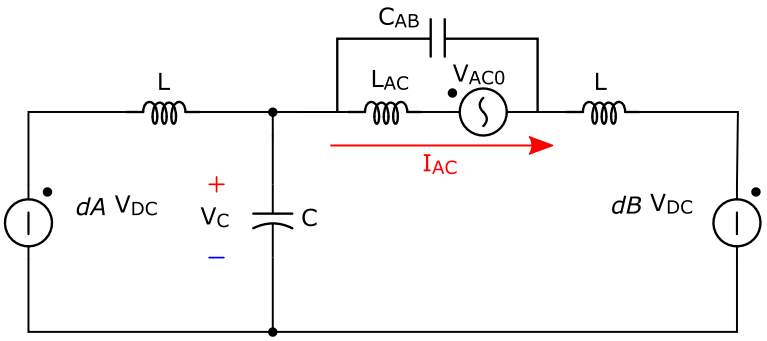
Where:

$$\omega_{Z1} = (CL)^{-0.5} \qquad f_{Z1} = \frac{\omega_{Z2}}{2\pi} \simeq 1.60\,kHz \qquad (6.12)$$

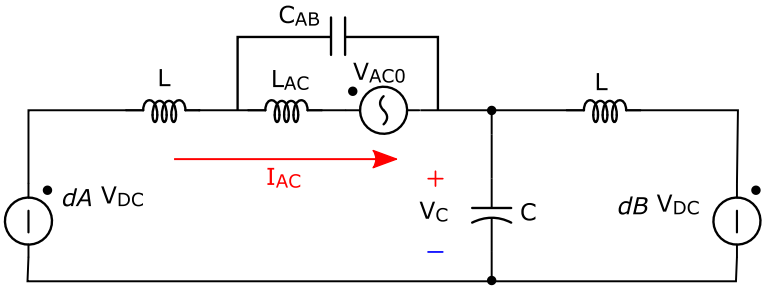
$$\omega_{P1} = \left(C\,\frac{L(L+L_{AC})}{2\,L+L_{AC}}\right)^{-0.5} \qquad f_{P1} = \frac{\omega_{P1}}{2\pi} \simeq 11.5\,kHz \qquad (6.13)$$

$$\omega_{P2} = \left(C_{AB}\frac{L\,L_{AC}}{L+L_{AC}}\right)^{-0.5} \qquad f_{P2} = \frac{\omega_{P2}}{2\pi} \simeq 74.2\,kHz \qquad (6.14)$$

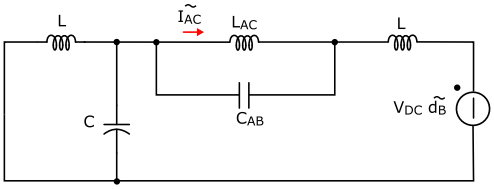
The chosen current controller is a PR resonating at grid frequency. The controller is able to damp the resonant poles at $11.5kHz$, while the damping of



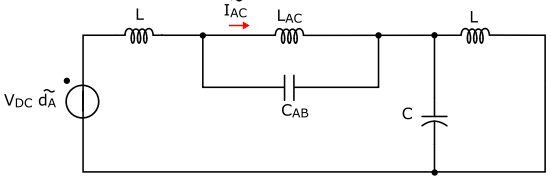
(a) Large signal model, mode A



(b) Large signal model, mode B



(c) Small signal model, mode A



(d) Small signal model, mode B

Figure 6.8: AC current control models

the resonant poles at $74.2kHz$ is passive, due to the AC losses in the inductors. The bode plot of the system and controller is shown in fig.6.9.

6.3.2 DC ripple current control

Neglecting the switching frequency components, the DC current I_{DC} is approximated to:

$$I_{DC} \approx \frac{1}{s^2/\omega_{DC}^2 + 1}(d_A I_A + d_B I_B) \tag{6.15}$$

The corresponding large signal equivalent circuit is shown in fig.6.10a. Since the AC current is controlled by the duty cycle d_B during mode A and d_A during mode B, the control the DC current is operated using d_A during mode A and d_B during mode B.

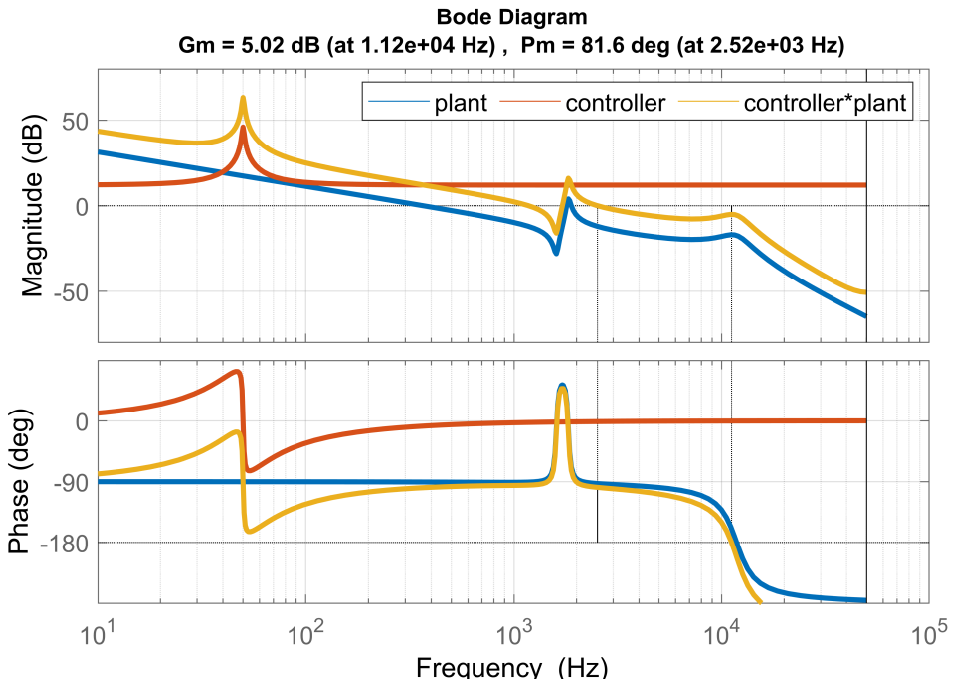


Figure 6.9: Bode plot, I_{AC} control

By operating the control in this way, it follows that the current flowing in the leg that controls I_DC in both modes is I_X, defined in (6.8).

Since the mean value of the current I_X at nominal power is 3.9A and changes linearly with the power P, the small signal transfer function for $\tilde{I_{DC}}$ is approximated as:

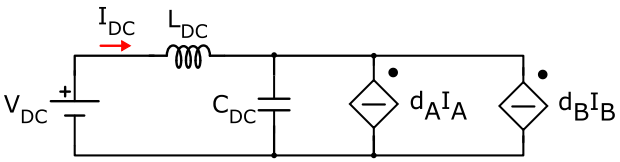
$$\frac{\tilde{I_{DC}}(s)}{\tilde{d_X}(s)} = I_X(s)\,\frac{1}{s^2/\omega_{DC}^2+1} \simeq 3.9\,p^*\,\frac{1}{s^2/\omega_{DC}^2+1} \tag{6.16}$$

Where p^* is the reference power expressed in per units.

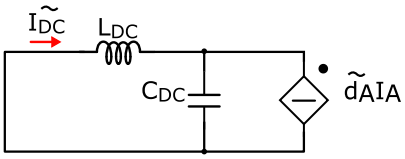
Assuming to control the DC current ripple by acting on the duty-cycle d_X, and neglecting the action of the DC filter, the DC control system can be modelled as in Fig.6.10. The target of the controller is to set to zero the ripple components of I_{DC} so that the current pulsation at twice the grid frequency is removed from the DC-link. Therefore, a high-pass filter cascaded with a notch tuned at 100Hz is used for the DC current ripple controller. The transfer function of the controller is the following:

$$C_{I_{DC}}(s) = 0.01\frac{s}{s/(2\pi 100)+1}\,\frac{1}{s^2/(2\pi 100)^2+1} \tag{6.17}$$

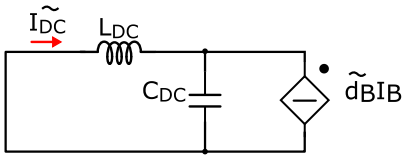
The controller is the same as the one used in the DFBC.



(a) Large signal model



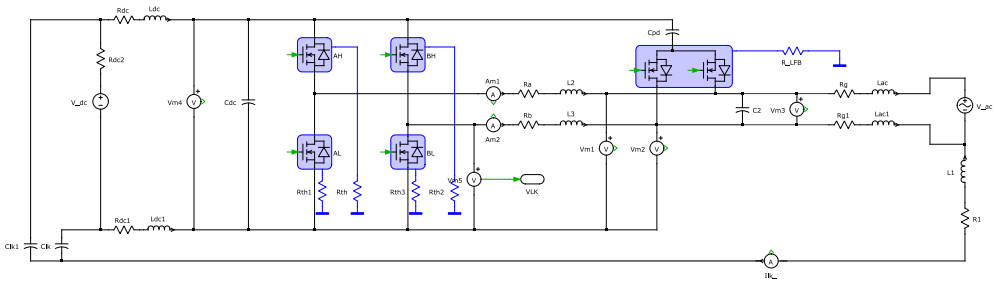
(b) Small signal model, mode A



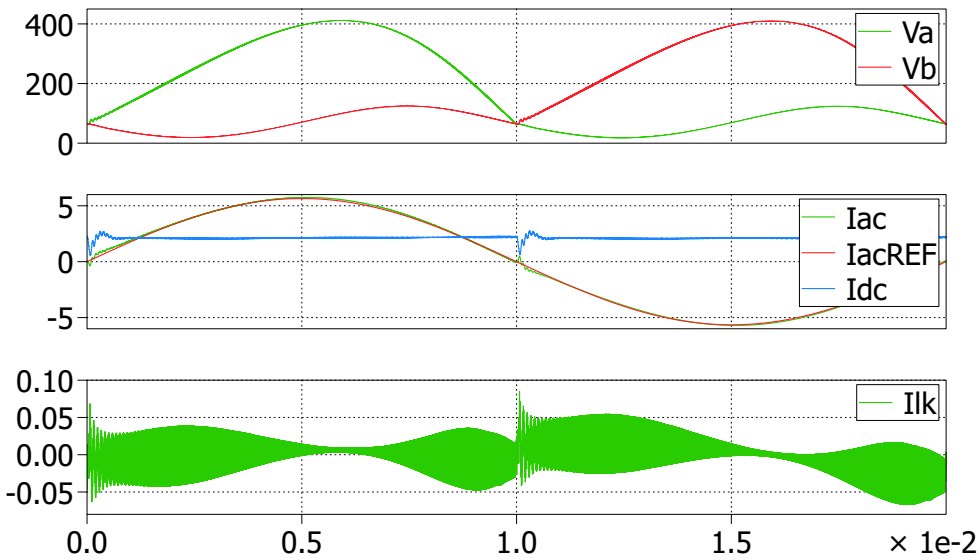
(c) Small signal model, mode B

Figure 6.10: DC ripple current control models

6.4 Simulation results



(a) Model



(b) Results

Figure 6.11: DFBC: PLECS simulation

In order to test the control algorithm and to calculate power losses, a time-

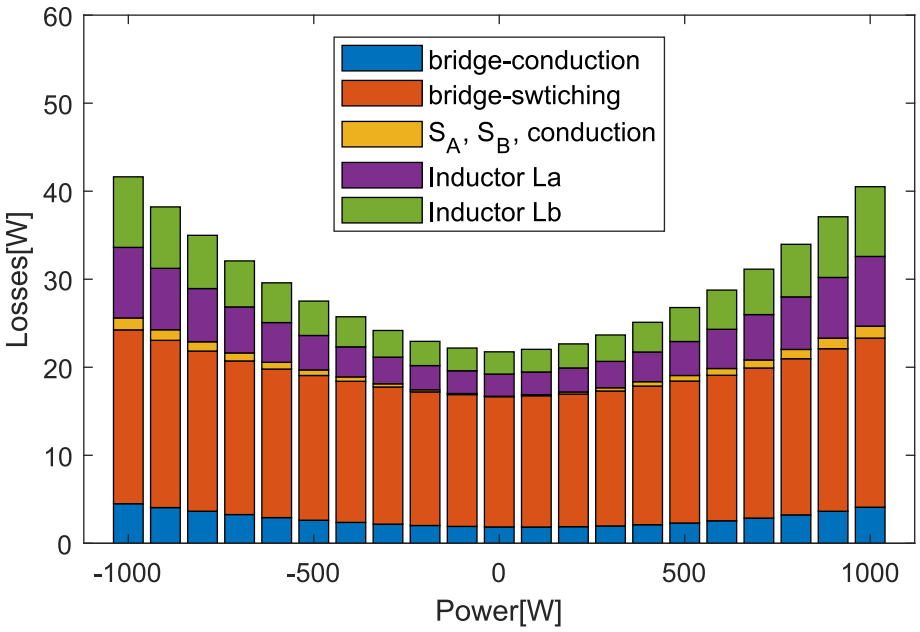


Figure 6.12: Power losses distribution

domain simulation of the proposed topology was made using Matlab-Simulink together with the PLECS toolbox.

The simulation proves the correct behaviour of the control system.

The leakage current I_{LK} has a RMS value over the AC period of 28.8 mA_{RMS}.

A power losses analysis was carried on using the same methods described in the previous chapter. In order to achieve a good filtering of the common mode currents, the passive filters were slightly oversized compared to the DFBC, especially the filtering inductors L_A and L_B. This involves a reduction of the ripple component of the currents, both in the active devices, in the DC link capacitors as well as in capacitor C and C_{AB}, and in the filtering inductors themselves. For this reason, conduction losses in the active devices and in the inductors are reduced. Due to the hard switching operation, switching losses in the bridge devices are relatively high.

6.5 Comparison with state-of-the-art topologies and DFBC

As can be seen from the comparison table 6.2, the two topologies share the same DC utilization ratio and FOM.

This happens because the current waveforms and the duty cycles in the full bridge operated at high frequency of the DFBC are the essentially the same as the ones of the full bridge of the JCC, with the difference that in the DFBC one arm is always connected to the power decoupling capacitor and the other to the AC port, while in the JCC their operation is swapped at each zero crossing of the AC voltage. In these terms, the two topologies can be seen as two different ways to implement the same concept of destructive interference between the rectified AC current and the capacitor current, exposed in Chapter 3.

Since the considerations about the comparison between the JCC and the other state-of-the-art are the same as the DFBC, discussed in the previous Chapter, in this section the focus is the comparison between the JCC and the DFBC.

The obvious difference between the two are the number of devices, the JCC having two "slow" switching devices and the DFBC four. Moreover, the current flowing in the slow devices of the JCC has a lower RMS and peak value, being the power decoupling capacitor current and not the AC current, which is higher.

On the other hand, the DFBC offers the possibility of reducing the size of the inductor L_A, connected to the power decoupling capacitor, with respect to L_B. This is because in the DFBC L_A filters the ripple current flowing in the capacitor, while L_B filters the current flowing in the AC port, that must have a small ripple to comply with the norms. In addition to that, the DFBC, as opposed to the JCC, has the capability of being able to operate with a reduced number of active devices if unidirectional power flow is required.

For these reasons, the DFBC seems better suitable for use in case of unidirectional power transfer, especially in rectifier mode, if low costs are required, while, if the power transfer has to be bidirectional, or if efficiency is key, the JCC is

preferable.

	Nominal Power $[kW]$	Number of devices	DC port voltage $[V]$	DC bus voltage $[V]$	AC port voltage $[V_{RMS}]$	Frequency $[Hz]$	Power dec. Capacitance $[\mu F]$	Efficiency %	DC util. ratio %	FOM %
Wang *et.al.* [1]	15	6	540	540	150	233	200	93	39	35(100)*
Breazeale*et.al.* [2]	1	6	200-550	700	240	60	2·102	97	48	11
Xia *et.al.* [6]	1	4	200-475	950	120	60	45	96	18	13
Zhong *et.al.* [3]	1	4	400	400	110	50	30	92	39	13
Tang *et.al.* [5]	1	3+5diodes	380	380	110	60	2·90	93	41	40
Tang *et.al.* [4]	.5	4	250	250	110	60	2·60	96	62	35
DFBC	1	4+4 slow	450	450	230	50	76	95	72	42
JCC	1	4+2 slow	450	450	230	50	76	96	72	42

Table 6.2: Comparison between state-of-the-art single phase topologies, DFBC and JCC

6.6 Conclusions

In this chapter, a topology, named Jumping Capacitor Converter (JCC) was introduced and described. A design procedure for its passive components is included, together with a control structure and losses analysis. The correct behaviour of the control system is confirmed by time-domain simulations.

The topology provides inherent leakage currents filtering capability, as the capacitive network formed by C and C_{AB} have a string filtering action on the common mode currents. For this reason, this topology is suitable as grid front-end for transformerless PV systems, or in other applications where leakage currents are an issue.

In order to validate the simulation results, an experimental setup was built. The description of the hardware implementation of the topology and the experimental results are presented in Chapter 9.

In the next two Chapters, a new modulation technique is introduced, and applied to the JCC. Since the modulation can be applied to a large number of topologies, it is presented in a general form in the next Chapter, while its implementation on the JCC is detailed in Chapter 8.

Chapter 7

Extended Triangular Current Mode (eTCM)

The widespread use of fast switching wide band-gap devices is driving a drastic change in the design of power converters, because of their low switching losses. Switching frequencies can be increased, achieving higher power densities due to the smaller passives required. Soft switching techniques achieving zero current switching (ZCS) and/or zero voltage switching (ZVS), can be used to reduce switching losses and EMI emission [55]. In particular, ZVS appears to be particularly beneficial if applied to SiC or GaN mosfets [56]. For this reason, in recent times, a renewed interest in ZVS techniques is apparent [57–59].

Resonant converters exploit the resonance of one or more LC circuits in order to obtain soft switching, however soft switching operation is often restricted to a limited operating range [60]. Other soft switching strategies require additional active elements to operate, such as the auxiliary resonant commutated pole converter [61]. In this case, the drawbacks are the additional cost and complexity of the converter.

Triangular Current Mode (TCM) has the advantage of obtaining ZVS without requiring any additional component and without eccessive complications in control [57]. In this case, zero voltage switching is obtained by opportunely modulating the amplitude of the current ripple generated by the switching devices.

The drawback, here, is that a high ripple current leads to higher conduction losses in the devices, and, more importantly, in the inductors, where AC losses severely contribute to the total losses. This problem is particularly of interest if wide band-gap devices are used, as AC losses in the inductors tend to increase with frequency.

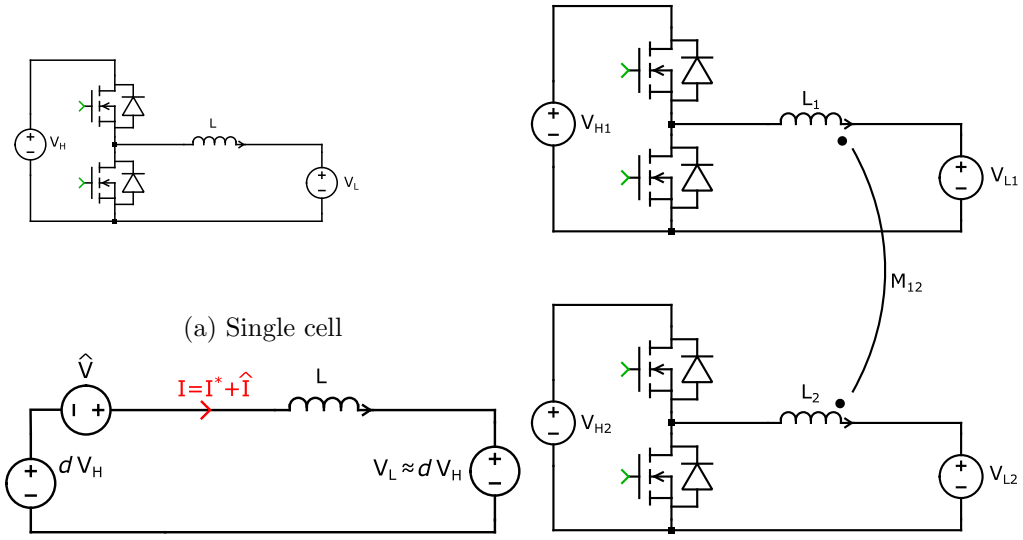
In order to reduce AC losses, several manifacturing techniques are available, such as using Litz cable to reduce skin effect in the copper, and use of core ferrite materials that exhibit low AC losses. Since these thechniques are expensive, a modulation technique able to obtain ZVS with smaller ripple currents compared to TCM is of interest.

In this chapter a new current mode, named "extended Triangular Current Mode" (eTCM) is introduced. This modulation, similarly to Triangular Current Mode (TCM) can be used to obtain ZVS, and generalized, that is, it can be applied to a large number of topologies. It is shown that eTCM can achieve ZVS at the price of a lower increase of the RMS and/or peak value of the ripple current compared to TCM.

In the first part of the chapter the modulation is introduced, then a design algorithm for the magnetic components is described; lastly, the performances of the modulation are compared with TCM.

7.1.1 Fundamental cell

In this chapter, the concept of fundamental cell is used. A fundamental cell is defined as an half bridge and a filtering inductor, connected between two voltage sources. To clearly illustrate the modulation techniques, the schematic of a fundamental cell is shown in Fig.7.1b. The current I flowing in the filtering inductor L is affected by the low voltage source V_L and the voltage modulated by the half bridge, which can be considered as the sum of a low frequency component, equal to the duty cycle times the high voltage ($d\,V_H$), and a zero-mean-value rectangular pulse train voltage $\hat{V}(t)$ at switching frequency. In the same way, the current $I(t)$ can be considered as the sum of a low frequency component I^*, and



(a) Single cell

(b) Single cell: equivalent circuit

(c) Mutually connected cells

Figure 7.1: Fundamental cell

a switching frequency zero-mean-value triangular current $\hat{I}(t)$:

$$I^* = \frac{1}{L}\int_0^t dV_H - V_L dt^* \qquad \hat{I}(t) = \frac{1}{L}\int_0^t \hat{V}(t^*)dt^* \tag{7.1}$$

where d is the duty-cycle, f is the switching frequency, and V_H is the high voltage. In general, d, f, V_H, V_L and consequently I^* can vary in time; however it is assumed that their variation is slow compared to the switching frequency; therefore, for better clarity, their time dependency is not explicitly indicated, as opposed to $\hat{I}(t)$ and $\hat{V}(t)$.

$\hat{V}_H(t)$ is defined, for each switching period T, as:

$$\hat{V}_H(t) = \begin{cases} V_H - V_L & t \in T_{ON} \\ -V_L & t \in T_{OFF} \end{cases} \tag{7.2}$$

where T_{ON} is the period during which the upper switch is closed, and T_{OFF} is the period during which the lower switch is closed.

7.1.2 Triangular Current Mode (TCM)

Triangular current mode was introduced in [57]. This modulation strategy allows to obtain zero voltage switching on the active devices of a half bridge, by ensuring that the instantaneous current flowing in the output inductor of the half bridge

is such that the stray capacitor of the switches are completely discharged prior to their turn on.

In order to illustrate this modulation, the equivalent circuit shown in Fig.7.1b is considered. The peak-to-peak amplitude of the ripple current $\hat{I}(t)$ can be achieved by solving the integral (7.1):

$$\Delta I = \left| \frac{1}{L} \int^{T_{ON}} \hat{V}(t^*) dt^* \right| = \left| \frac{1}{L} \int^{T_{OFF}} \hat{V}(t^*) dt^* \right| = \frac{V_H}{fL} d[1-d] \tag{7.3}$$

The instantaneous value of the ripple current at the turn on of the high switch is equal to $-\frac{1}{2}\Delta I$, while at the turn on of the low switch is $+\frac{1}{2}\Delta I$. If the ripple component of the current flowing in the output inductor is high enough, with respect to the steady-state component, the instantaneous current $I(t)$ is negative at the turn on of the high side switch and positive at the turn on of the the low side switch, achieving ZVS. The ZVS conditions are shown in (7.4).

$$\begin{cases} I(t_{ON}) = I^* - \hat{I}(t_{ON}) = I^* - \frac{1}{2}\Delta I < -I_{ZVS} \\ I(t_{OFF}) = I^* + \hat{I}(t_{OFF}) = I^* + \frac{1}{2}\Delta I > I_{ZVS} \end{cases} \tag{7.4}$$

where t_{ON} is the instant of time that corresponds to the turn on of the high switch, t_{OFF} is the instant of time that corresponds to the turn on of the low switch, and I_{ZVS} is the minimum current required for the resonant transition between the inductor and the stray capacitors of the active devices to discharge the capacitor of the switch that is going to be closed, thus obtaining ZVS, as discussed in [57, 62].

The maximum switching frequency that can be applied while still achieving ZVS in a generic instant of time t can be derived from (7.3) and (7.4), and is shown in (7.5).

$$f_{ZVS} \leq \frac{1}{2} V_{DC} \frac{d(1-d)}{L} \frac{1}{|I^*| + I_{ZVS}} \tag{7.5}$$

Since, in order to reduce the losses, it is desirable to reduce the ripple current, this maximum switching frequency is typically chosen when variable frequency modulation is used and ZVS is required [63].

From (7.4) follows that, in order to obtain ZVS, the peak value of the current has to be higher than double the low frequency component, causing high RMS losses in the fundamental cell. In order to deal with this problem, interleaving is proposed in [57]; however, interleaving comes with the disadvantages of a more complex structure, and usually higher costs [64].

7.1.3 extended Triangular Current Mode (eTCM)

The analysis exposed in the previous section can be extended for N fundamental cells, operating at the same switching frequency f, having a mutual coupling between their filtering inductors, as in Fig.7.1c.

In this case, the relation between the ripple components of voltages and currents can be studied using the impedance parameters of a multi-port network:

$$\begin{vmatrix} \hat{V}_1(t) \\ \vdots \\ \hat{V}_N(t) \end{vmatrix} = \frac{d}{dt}[\mathcal{L}] \begin{vmatrix} \hat{I}_1(t) \\ \vdots \\ \hat{I}_N(t) \end{vmatrix} \tag{7.6}$$

where $\hat{V}_1(t)$, $\hat{V}_N(t)$ and $\hat{I}_1(t)$, $\hat{I}_N(t)$ are the ripple components of voltages and currents of the bridge arms, and $\mathcal{L}$ is the inductance matrix defined as:

$$\mathcal{L} = \begin{bmatrix} L_{11} & \dots & L_{1N} \\ \vdots & \ddots & \vdots \\ L_{N1} & \dots & L_{NN} \end{bmatrix} \qquad L_{ij} = V_i \Big/ \frac{dI_j}{dt}\Big|_{V_k=0,\ k\neq i} \tag{7.7}$$

The inverse relation is:

$$\begin{vmatrix} \hat{I}_1(t) \\ \vdots \\ \hat{I}_N(t) \end{vmatrix} = \int_0^t [\Gamma] \begin{vmatrix} \hat{V}_1(t^*) \\ \vdots \\ \hat{V}_N(t^*) \end{vmatrix} dt^* \tag{7.8}$$

where Γ is the inverse inductance matrix, $\mathcal{L}^{-1}$.

(7.3) can be extended to N fundamental cells, whose inductors are mutually coupled. In this case, the current ripple $\hat{I}_i(t)$ flowing thorugh each output inductor L_i is equal to the sum of N triangular components $\hat{I}_{ij}(t)$ generated by the ripple

voltage modulated by each leg j. Their peak-to-peak amplitude ΔI_{ij} can be calculated as follows:

$$\Delta I_{ij} = \Gamma_{ij} \frac{V_{DC}}{f} d_j (1 - d_j) \tag{7.9}$$

The total ripple current $\hat{I}_i(t)$ has a piecewise waveform, and, being the sum of zero-mean-value triangular components, has zero mean. The peak-to-peak amplitude of the total ripple current can vary according to the phase shift between the modulation of the cells; in particular, the positive peak of $\hat{I}_i(t)$, $\hat{I}^+_{i,max}$, is equal to the sum of the positive peaks of its triangular components $\hat{I}_{ij}(t)$, if they are exactly in phase, while otherwise lower; in the same way, the negative peak of $\hat{I}_i(t)$, $\hat{I}^-_{i,min}$ is equal to the sum of the negative peaks of its triangular components $\hat{I}_{ij}(t)$, if they are in phase, while otherwise higher:

$$\hat{I}^+_{i,max} \leq +\frac{1}{2} \sum_j \Delta I_{ij} \qquad\qquad \hat{I}^-_{i,min} \geq -\frac{1}{2} \sum_j \Delta I_{ij} \tag{7.10}$$

Therefore, generally:

$$-\frac{1}{2} \sum_j \Delta I_{ij} \leq \hat{I}_i(t) \leq +\frac{1}{2} \sum_j \Delta I_{ij} \tag{7.11}$$

In eTCM, unlike TCM, the positive and negative peak value of the ripple current can be different in magnitude, depending on the duty cycles applied to each fundamental cell, the phase shift, and the inductance matrix $\mathcal{L}$.

From (7.4), it follows that a negative instantaneous current is required to achieve ZVS at the turn-on of the upper switch of a leg, while a positive current is required to achieve ZVS at the turn-on of the lower switch.

For this reason, if the low frequency component of the current, I^*, is positive, a higher negative ripple current $\hat{I}(t)$ is required to obtain ZVS on the upper switch, while ZVS on the lower switch is obtained even with low ripple. By opportune choice of the phase shift between the modulation of each leg, using eTCM it is possible to achieve an high negative peak value and a low positive peak value of the ripple current of one leg, thus potentially achieving ZVS with lower losses compared to TCM, where the positive and negative peak of the ripple current are always the same.

As this mode of operation of the converter is similar to TCM, extended for N mutually-coupled fundamental cells, this mode of operation is named *extended Triangular Current Mode* (eTCM).

Because of the presence of the mutual coupling, this modulation has similarities with the modulation techniques commonly used in Dual Active Bridge [65], such as trapezoidal current mode; however, the mutual coupling is used here in order to shape the ripple current to obtain ZVS with low ripple, and not to transfer power trough the magnetic coupling, that here is considered as a secondary effect.

7.2 Magnetics design for eTCM

The aim of the magnetics design is to size the magnetic components used with eTCM, in other words, to choose the elements of the matrix $\mathcal{L}$.

The target of the design of the magnetic components usually consists in finding a balance between the minimization of the ripple currents, in order to reduce the current stress in the switching devices and in the input-output filters, and the size and cost of the magnetic components. For example, considering a single fundamental cell, given a required maximum current I_{MAX}, the minimum inductance can be calculated as follows:

$$L_{MIN} = \frac{V_H}{f}\frac{1}{\hat{I}_{MAX}} = \frac{V_H}{f}\frac{1}{I_{MAX} - |I^*|} \tag{7.12}$$

The saturation current of the inductor has to be higher than the maximum current I_{MAX}. For this reason, the design of the inductor has to take into account the peak current applied to it. In order to compare two designs having different peak current and inductance values, in terms of size and cost of the magnetic component, it is chosen to consider the maximum magnetic energy E_L stored in the inductor, defined as:

$$E_L = \frac{1}{2} L I_{MAX}^2 \tag{7.13}$$

When more than one fundamental cell are considered, the cost and size of the magnetic components depend on the required inductances, the maximum currents

flowing in each winding and the mutual coupling between the windings. In order to compare different magnetic structures, the maximum magnetic energy can again be considered.

$$E_L = \mathbf{MAX}\left(\frac{1}{2}\begin{vmatrix} I_1(t) \\ \vdots \\ I_N(t) \end{vmatrix}' [\mathcal{L}] \begin{vmatrix} I_1(t) \\ \vdots \\ I_N(t) \end{vmatrix}\right), t \in T. \tag{7.14}$$

The inductance matrix $\mathcal{L}$ can be indicated as the product between a base inductance L and the normalized inductance matrix l:

$$\mathcal{L} = L\,l \qquad\qquad l = \begin{bmatrix} 1 & k_M\tau \\ k_M\tau & \tau^2 \end{bmatrix} (for N = 2) \tag{7.15}$$

The following algorithm define a design procedure for the inductance matrix $\mathcal{L}$, given the following constraints:

1. Fixed duty cycles
2. Fixed currents
3. Fixed switching frequency

In the following case, a fixed switching frequency of 100kHz is considered.

7.2.1 Magnetic design algorithm

In general, a converter can operate with currents and duty cycles that vary in time. In order to simplify the design, a converter operating with fixed duty cycles and currents is initially considered. The algorithm is tailored for the design of a system limited to two fundamental cells, however, it can be easily extended for N elements.

The following is the description of the algorithm for magnetic design.

Definition

The following algorithm is defined for the case of two fundamental cells, however, it can be easily extended for a generic number. In order to identify the cell

currents and voltages, letter are used (such as I_A, I_B, d_A, d_B) instead of numbers as it was done so far, in order to keep the notation consistent with what was used for the topologies DFBC and JCC.

Inputs:

- the duty cycles d_A, d_B;
- the low frequency components of the currents I_A^*, I_B^*;
- the DC-link voltage V_{DC};
- the switching frequency f
- the following additional constraints:
  - the maximum peak current $I_{PK,\,MAX}$;
  - the maximum RMS current $I_{RMS,\,MAX}$;
  - the minimum reverse current for obtaining ZVS I_{ZVS};

Outputs:

- the inductance matrix $\mathcal{L}$ (L, k_M, τ);
- the optimum phase shift δ;
- the maximum magnetic energy E_L

Implementation

The algorithm gets the best inductance matrix and phase shift by fixing k_M, τ and δ and calculating the minimum base inductance L that verifies the maximum current constraint, and the associated maximum magnetic energy E_L.

The process is repeated for every combination of k_M, τ and δ, and the solution having the minimum E_L is chosen.

The value of L is chosen in two steps: first, the constraints on current peak, RMS and ZVS are translated in constraints on the value of L (L_{MIN} and L_{MAX}), then, the optimum value is chosen inside those constraints.

For each step the normalized ripple current $\hat{i}$, defined as follows, is obtained, and used to calculate the base inductor L that respects the constraints.

$$\hat{i} = L\,\hat{I} \tag{7.16}$$

RMS constraint Since the low frequency and the ripple frequency components of the current have a different spectrum, the RMS of the total current can be calculated as:

$$I_{RMS} = \sqrt{RMS(I^*)^2 + RMS(\hat{I})^2} = \sqrt{RMS(I^*)^2 + \frac{1}{L^2}RMS(\hat{i})^2} < I_{RMS,\,MAX} \tag{7.17}$$

The minimum inductance L_{MIN} that verifies the RMS constraint is thus:

$$L > L_{MIN} = \sqrt{\frac{RMS(\hat{i})^2}{I_{RMS,\,MAX}^2 - RMS(I^*)^2}} \tag{7.18}$$

Peak current constraint

$$I < I_{MAX} \;\Rightarrow\; \left|\frac{\hat{i}}{L} + I^*\right| < I_{MAX} \Rightarrow \begin{cases} \frac{\hat{i}}{L} + I^* < I_{MAX} \\ \frac{\hat{i}}{L} + I^* > -I_{MAX} \end{cases} \Rightarrow \begin{cases} L > \frac{\hat{i}}{I_{MAX} - I^*} \\ L > \frac{-\hat{i}}{I_{MAX} + I^*} \end{cases} \tag{7.19}$$

As for the RMS constraint, the peak current constraint sets a constraint on the minimum size of the inductor.

ZVS constraint As previously stated, in order to achieve ZVS in each fundamental cell, the current has to verify the conditions (7.4):

$$\begin{cases} I_{ON} < -I_{ZVS} \\ I_{OFF} > I_{ZVS} \end{cases} \tag{7.20}$$

In TCM, the positive peak of the ripple current always occurs at the turn off of the upper device, and the negative peak at the turn on of the higher device, hence, the ZVS constraint translates in a upper bond to the value of L_{MAX}, as a very high ripple does not prevent ZVS. In eTCM, however, this is not always the case, as the effect of the mutual coupling can cause the ripple current to have an

opposite sign during the switching transition. For this reason, a lower bond on the value of L_{MIN} is also possible. According to the sign of the ripple and low frequency component of the current, the ZVS constraints on L are the following:

$$I_{ON} < -I_{ZVS} \Rightarrow L\,\hat{i_{ON}} + I^* < -I_{ZVS} \Rightarrow \begin{cases} L < \frac{-\hat{i_{ON}}}{I_{ZVS}+I^*} & I_{ZVS} + I^* > 0 \\ L > \frac{-\hat{i_{ON}}}{I_{ZVS}+I^*} & I_{ZVS} + I^* < 0 \\ \hat{i_{ON}} < 0 & I_{ZVS} + I^* = 0 \end{cases} \quad (7.21)$$

$$I_{OFF} > I_{ZVS} \Rightarrow L\,\hat{i_{OFF}} + I^* > I_{ZVS} \Rightarrow \begin{cases} L < \frac{\hat{i_{OFF}}}{I_{ZVS}-I^*} & I_{ZVS} - I^* > 0 \\ L > \frac{\hat{i_{OFF}}}{I_{ZVS}-I^*} & I_{ZVS} - I^* < 0 \\ \hat{i_{OFF}} > 0 & I_{ZVS} - I^* = 0 \end{cases} \quad (7.22)$$

Optimum solution Once the current constraints are translated to constraints for the inductor, the optimum solution for L that respect the constraints can be calculated. If the constraints are consistent, that is, if $L_{MAX} > L_{MIN}$, the algorithm identifies the best value of L that minimize the RMS current, the peak current or the magnetic energy.

The choice of the best value for L corresponds to the minimization of a cost function. The three cost functions that are implemented in the algorithm are the following:

- minimization of maximum RMS current;
- minimization of maximum peak current;
- minimization of maximum magnetic energy E_L.

If the minimum RMS or peak current is required, the solution is to the highest possible base inductor, that is, $L_{BEST} = L_{MAX}$, since L is inversely proportional to the amplitude of the ripple current component. If, instead, the minimum magnetic energy is required, the optimum solution does not correspond to the minimum L, and has to be numerically calculated.

7.2.2 Simulation results

Several simulations were made, in order to test the correct behaviour of the design algorithm. The analysis of the results lead to the following considerations:

- The results of the design algorithm are consistent with the well-known design practices in case of interleaving (same duty-cycle, same low-frequency current) (see Scenario 2).

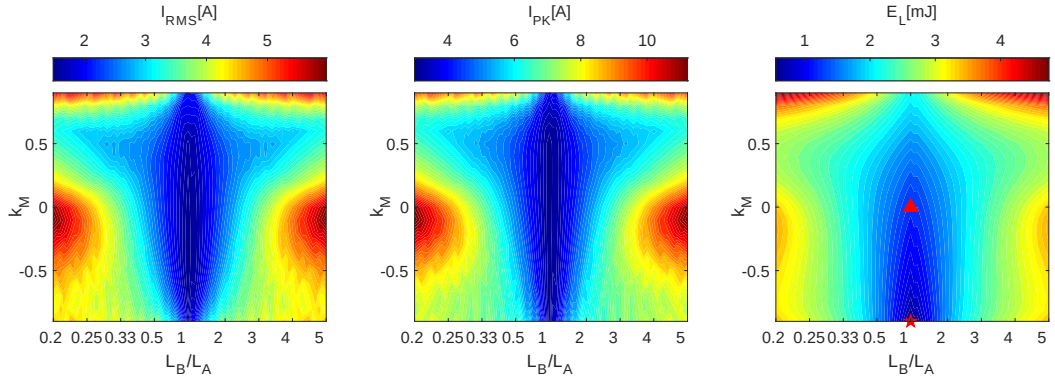
- The best solution in terms of reduction of the maximum magnetic energy E_L, in case of high low-frequency currents, consists in having a high mutual coupling coefficient between the inductors, in order to achieve the maximum flux cancellation. For example, in both Scenario 1 and Scenario 2, the chosen mutual coupling is the maximum negative coupling (-0.9), while in Scenario 3, for the same reason, the optimum coupling is positive.

- eTCM is able to extend the ZVS region, that is to say that, for some magnetic designs, ZVS can be obtained using eTCM but not using TCM. This is the case for Scenario 4, 5 and 6, where, due to a constraint set on the RMS and/or peak current of the currents, TCM is unable to achieve ZVS.

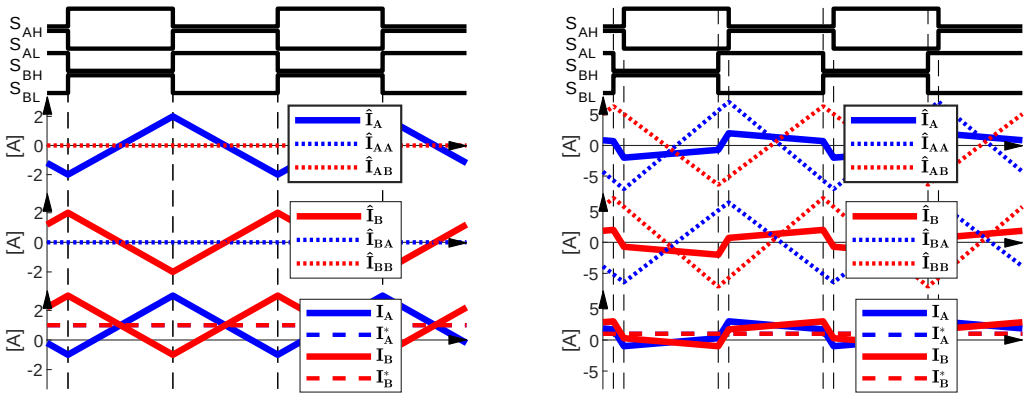
Scenario 1: Interleaving

Same duty cycles and currents ($d_A = d_B$, $I_A = I_B$), minimum E_L, $I^*_{ZVS} = 1A$.

PARAMETERS			RESULTS				L_{eTCM}		
f	100	kHz		TCM	eTCM		L_A	414	uH
V_H	450	V	E_L	1.266	0.556	mJ	L_B	414	uH
d_A	0.5		$I_{A,RMS}$	1.528	1.698	A	M	-373	uH
d_B	0.5		$I_{B,RMS}$	1.528	1.698	A	L_{TCM}		
I^*_B	1.0	A	$I_{A,MAX}$	3.000	3.000	A	L_A	281	uH
I^*_A	1.0	A	$I_{B,MAX}$	3.000	3.000	A	L_B	281	uH



(a) RMS current (b) Peak current (c) Magnetic energy



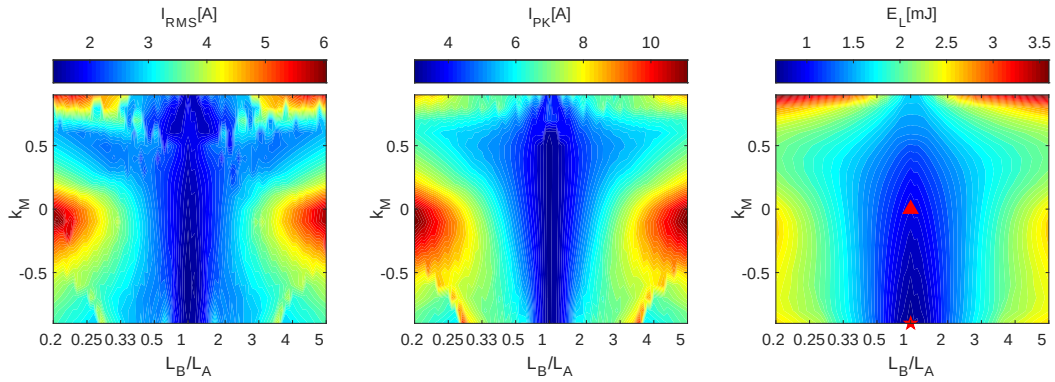
(d) Ripple current waveforms, TCM (e) Ripple current waveforms, eTCM

Figure 7.2: eTCM, fixed operating point

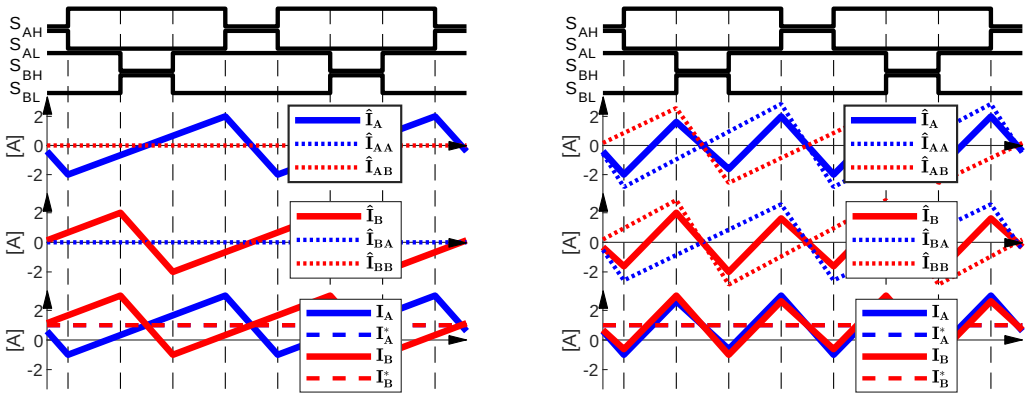
Scenario 2: Interleaving

Same duty cycles and currents ($d_A = d_B$, $I_A = I_B$), minimum E_L, $I^*_{ZVS} = 1A$.

PARAMETERS			RESULTS				L_{eTCM}		
f	100	kHz		TCM	eTCM		L_A	777	uH
V_H	450	V	E_L	0.961	0.667	mJ	L_B	777	uH
d_A	0.8		$I_{A,RMS}$	1.528	1.455	A	M	-699	uH
d_B	0.8		$I_{B,RMS}$	1.528	1.454	A	L_{TCM}		
I^*_B	1.0	A	$I_{A,MAX}$	3.000	3.000	A	L_A	211	uH
I^*_A	1.0	A	$I_{B,MAX}$	3.000	3.000	A	L_B	211	uH



(a) RMS current (b) Peak current (c) Magnetic energy



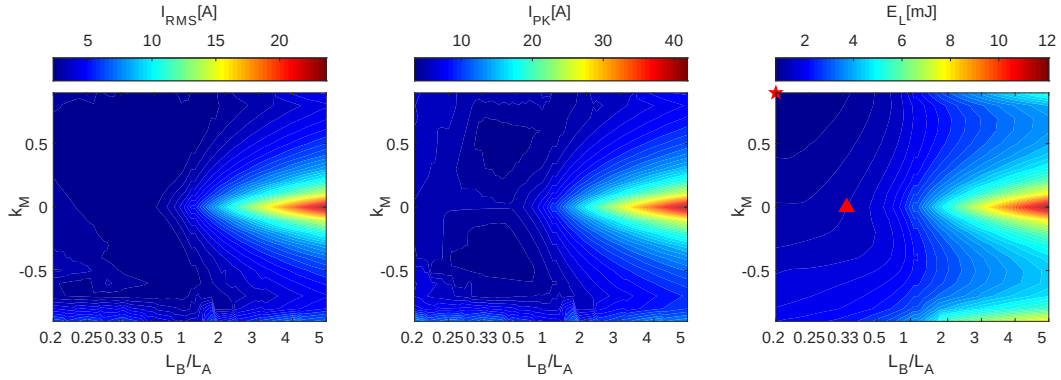
(d) Ripple current waveforms, TCM (e) Ripple current waveforms, eTCM

Figure 7.3: eTCM, fixed operating point

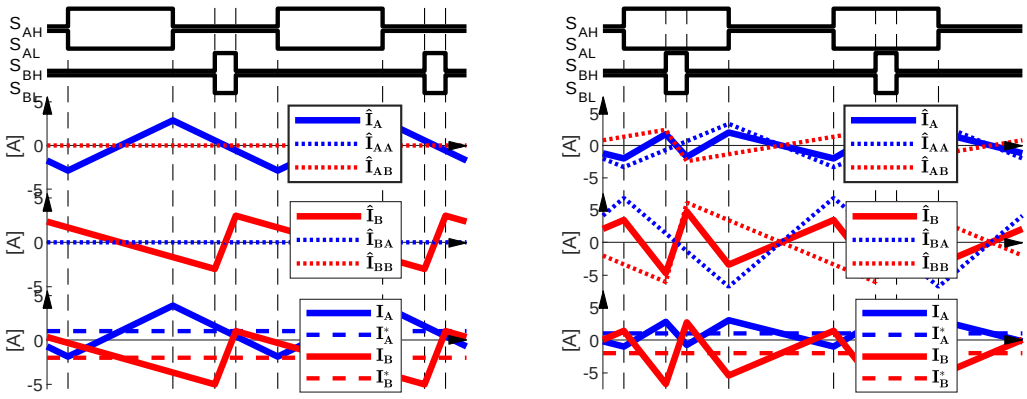
Scenario 3: Different current sign

Different current signs, minimum E_L, $I^*_{ZVS} = 1A$.

PARAMETERS			RESULTS				L_{eTCM}		
f	100	kHz		TCM	eTCM		L_A	884	uH
V_H	450	V	E_L	1.469	0.793	mJ	L_B	177	uH
d_A	0.5		$I_{A,RMS}$	1.937	1.498	A	M	356	uH
d_B	0.1		$I_{B,RMS}$	2.646	2.996	A	L_{TCM}		
I^*_B	-2.0	A	$I_{A,MAX}$	3.874	3.000	A	L_A	196	uH
I^*_A	1.0	A	$I_{B,MAX}$	5.000	6.678	A	L_B	67	uH



(a) RMS current (b) Peak current (c) Magnetic energy



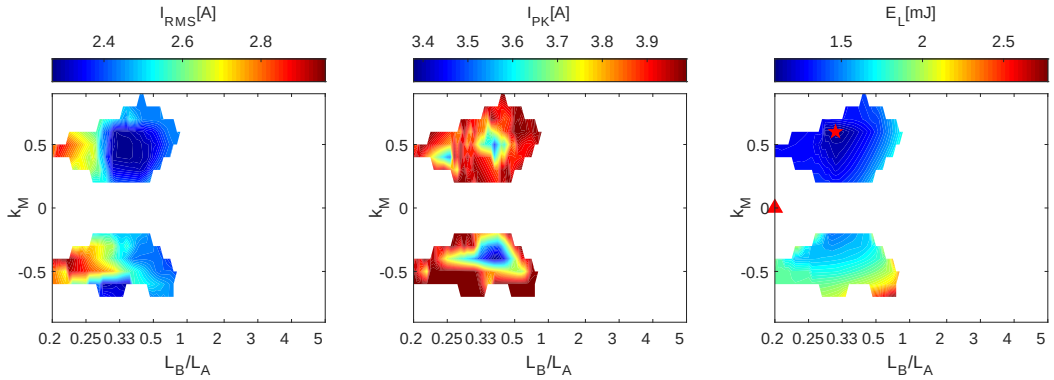
(d) Ripple current waveforms, TCM (e) Ripple current waveforms, eTCM

Figure 7.4: eTCM, fixed operating point

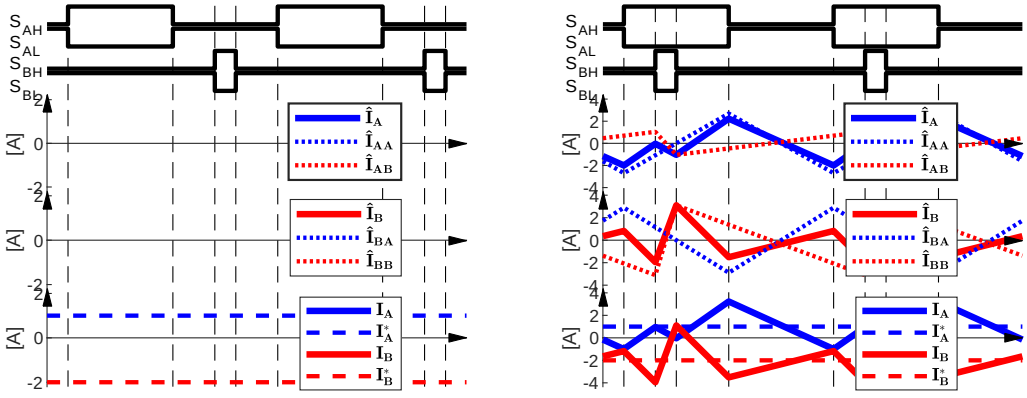
Scenario 4: Peak current limit

Different current signs, minimum E_L, $I^*_{ZVS} = 1A$, $I_{PK,MAX} = 4A$.

PARAMETERS			RESULTS				L_{eTCM}		
f	100	kHz		TCM	eTCM		L_A	326	uH
V_H	450	V	E_L	–	1.090	mJ	L_B	102	uH
d_A	0.5		$I_{A,RMS}$	–	1.518	A	M	109	uH
d_B	0.1		$I_{B,RMS}$	–	2.297	A	L_{TCM}		
I^*_B	−2.0	A	$I_{A,MAX}$	–	3.231	A	L_A	–	uH
I^*_A	1.0	A	$I_{B,MAX}$	–	3.947	A	L_B	–	uH



(a) RMS current (b) Peak current (c) Magnetic energy



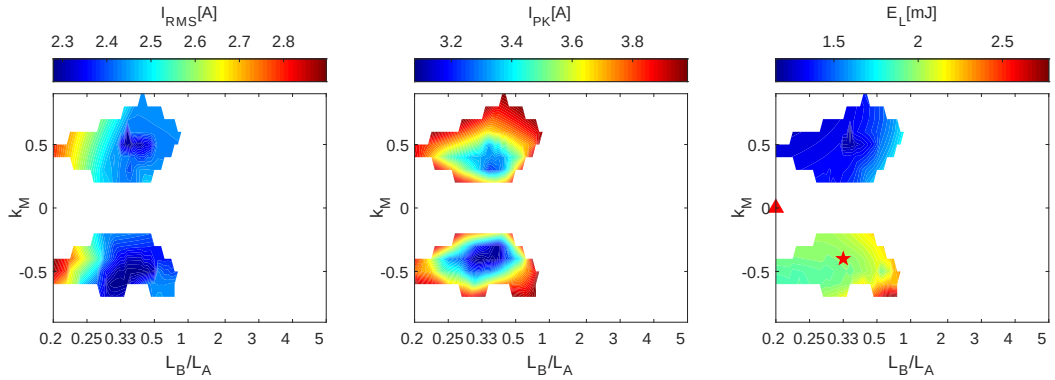
(d) Ripple current waveforms, TCM (e) Ripple current waveforms, eTCM

Figure 7.5: eTCM, fixed operating point

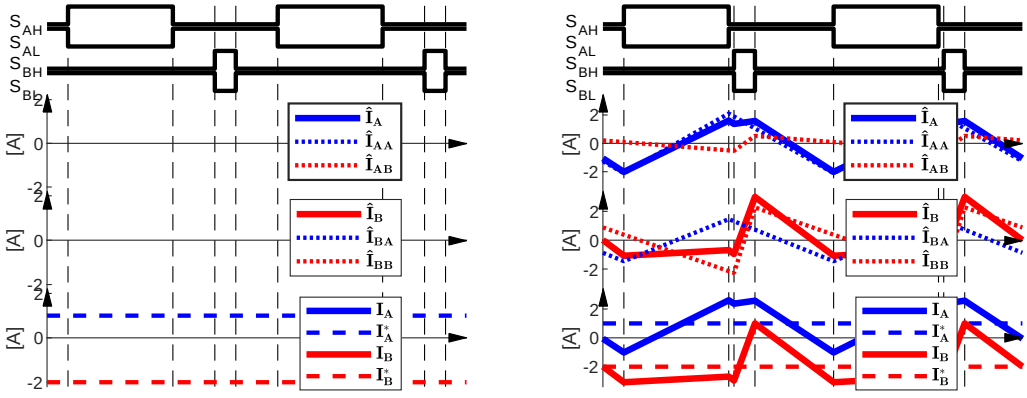
Scenario 5: Peak current limit

Different current signs, minimum current peak, $I^*_{ZVS} = 1A$, $I_{PK,MAX} = 4A$.

PARAMETERS			RESULTS				L_{eTCM}		
				TCM	eTCM		L_A	318	uH
f	100	kHz					L_B	106	uH
V_H	450	V	E_L	–	1.155	mJ	M	−74	uH
d_A	0.5		$I_{A,RMS}$	–	1.504	A	L_{TCM}		
d_B	0.1		$I_{B,RMS}$	–	2.348	A			
I^*_B	−2.0	A	$I_{A,MAX}$	–	2.608	A	L_A	–	uH
I^*_A	1.0	A	$I_{B,MAX}$	–	3.079	A	L_B	–	uH



(a) RMS current (b) Peak current (c) Magnetic energy



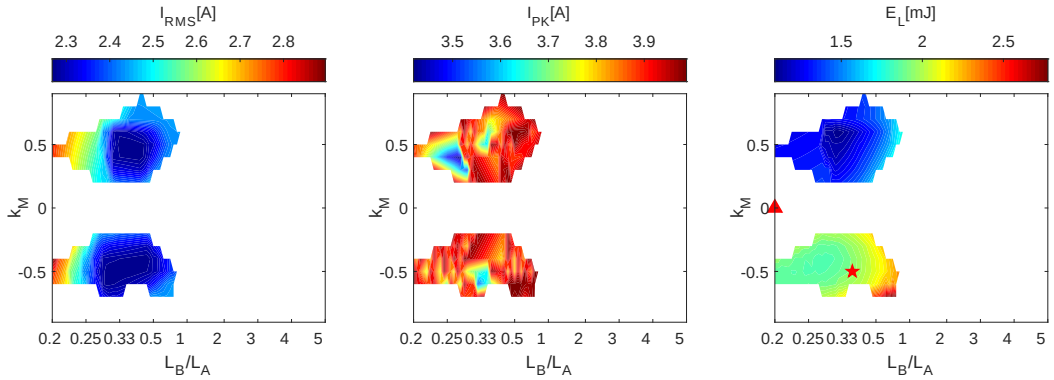
(d) Ripple current waveforms, TCM (e) Ripple current waveforms, eTCM

Figure 7.6: eTCM, fixed operating point

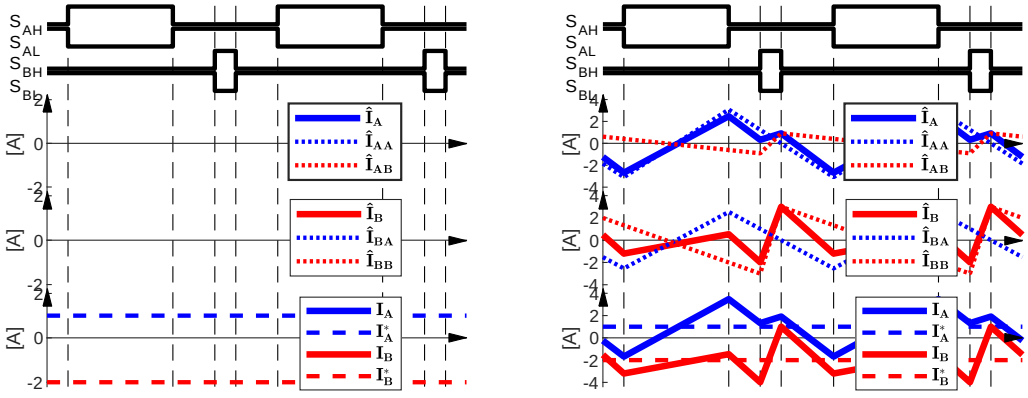
Scenario 6: RMS current limit

Different current signs, minimum current RMS, $I^*_{ZVS} = 1A$, $I_{PK,MAX} = 4A$.

PARAMETERS			RESULTS				L_{eTCM}		
				TCM	eTCM		L_A	243	uH
f	100	kHz	E_L	–	1.090	mJ	L_B	90	uH
V_H	450	V	$I_{A,RMS}$	–	1.724	A	M	-74	uH
d_A	0.5		$I_{B,RMS}$	–	2.268	A	L_{TCM}		
d_B	0.1		$I_{A,MAX}$	–	3.478	A	L_A	–	uH
I^*_B	-2.0	A	$I_{B,MAX}$	–	3.986	A	L_B	–	uH
I^*_A	1.0	A							



(a) RMS current (b) Peak current (c) Magnetic energy



(d) Ripple current waveforms, TCM (e) Ripple current waveforms, eTCM

Figure 7.7: eTCM, fixed operating point

7.3 Variable operating point

The eTCM current mode can be obtained even if the duty cycles and low frequency current components are variable in time, which is the case for AC-DC converters.

The main difference between variable and fixed operating point is that, in case of variable operating point, the design of the magnetic structure has to be a global optimum, that is, must minimize the chosen cost function over the entire operating range, which, in case of an AC-DC converter, corresponds to one AC period.

For a given magnetic structure, the target of variable operating point eTCM modulation is to find the best phase shift δ and switching frequency f for each switching interval.

To find the best δ and f, a useful simplification is to consider each switching interval separately, under the assumption of their influence on each other being negligible. This is not necessarily true for phase shift, as a jump in phase shift translates in a step variation of the low frequency component of the current.

This is in apparent contradiction with the definition of ripple current component as defined in section 7.1.1, that has the property of having zero mean value; however zero mean value is the consequence of an opportune choice of the integration constant. In reality, the integration constant for each switching period is fixed by the continuity of the current.

Taking in to account the effect of the phase shift of each switching period on all the others would severely complicate the problem, therefore, the interaction is assumed being negligible. This assumption is reasonable if the phase variations between one switching interval and the next are small.

Given the hypothesis of slow variation of phase, the optimum phase shift and switching frequency for each switching interval can be solved by applying the same algorithm used for fixed operating point to each switching interval.

To choose the best magnetic structure, instead, all the different operating points have to be taken into account. To do so, a simple solution is to apply the

eTCM algorithm to find the best phase shift and switching frequency for each switching interval, and use it to calculate the currents over the entire operating range. The currents peak values, RMS, and maximum magnetic energy can then be achieved, and used to compare different magnetic structures.

The design of the magnetic structure for variable operating point can thus be carried as follows: given the waveforms of the duty cycles and low frequency current components, a cost can be assigned for each magnetic structure, using the procedure described in the previous paragraph. The one having the lowest cost is then chosen.

7.4 Simplified extended Triangular Current Mode (SeTCM)

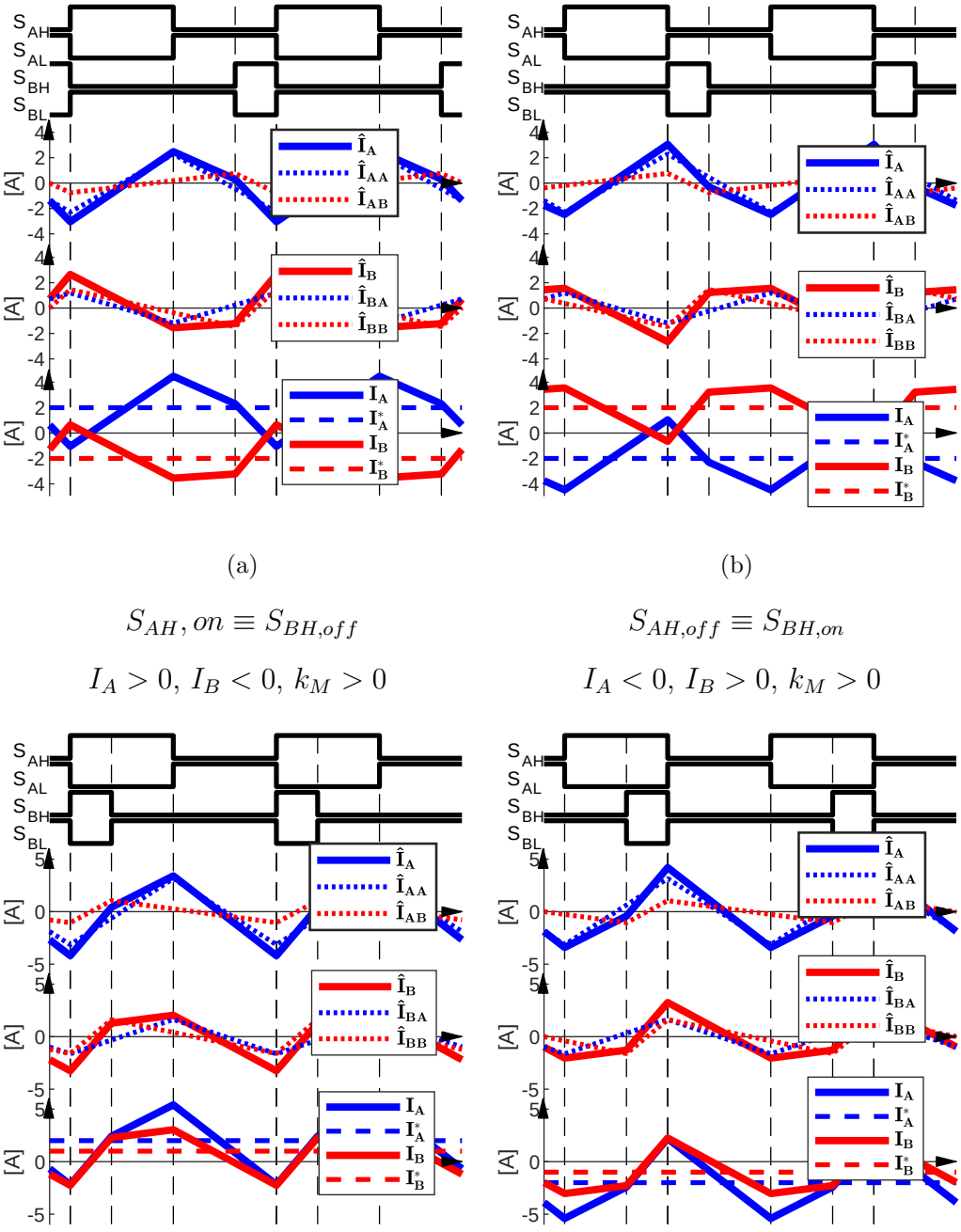
As can be seen in the previous section, finding the optimum phase shift and frequency can be computationally cumbersome, as they depend on both the duty cycles and the low frequency component, the constraints, and the chosen optimum function; and a closed form analytical solution is not easy to find.

In order to easily implement eTCM on a microcontroller, a simplified modulation is proposed.

The modulation, that considers two mutually coupled fundamental cells, consists in choosing the phase shift in order to achieve the maximum peak ripple at the switching instant when it is required to obtain ZVS, and choosing the maximum switching frequency that verifies the ZVS conditions.

In SeTCM, the phase shift is chosen according to the sign of the low frequency component of the currents in the two cells. The four different cases are shown in fig.7.8.

To illustrate the modulation, case A is considered (fig.7.8a). Assuming zero ripple, since I_A^* is positive and I_B^* is negative, ZVS is obtained for the turn on of S_{AL} and S_{BH}. To obtain ZVS for the turn on of S_{AH} and S_{BL} the ripple current has to be high enough to invert the sign of the current prior to the switching.



(a)

$S_{AH}, on \equiv S_{BH,off}$

$I_A > 0,\ I_B < 0,\ k_M > 0$

(b)

$S_{AH,off} \equiv S_{BH,on}$

$I_A < 0,\ I_B > 0,\ k_M > 0$

(c)

$S_{AH,on} \equiv S_{BH,on}$

$I_A > 0,\ I_B > 0,\ k_M < 0$

(d)

$S_{AH,off} \equiv S_{BH,off}$

$I_A < 0,\ I_B < 0,\ k_M < 0$

Figure 7.8: Simplified extended Triangular Current Mode (SeTCM)

The phase shift is chosen so that the turn on of S_{AH} and S_{BL} is coincident, hence the maximum peak of the ripple, that corresponds to the sum of the peak of the two triangular components $\hat{I}_{AA}(t)$ and $\hat{I}_{AB}(t)$, occurs during their commutation.

The minimum of $\hat{I}_{AA}(t)$, equal to $-\frac{1}{2}\Delta I_{AA}$, always corresponds to the turn on of S_{AH}. Assuming a positive coupling, Γ_{12} and Γ_{21} are negative, and the minimum of $\hat{I}_{AB}(t)$ corresponds to the turn on of S_{BL}. It follows that the minimum negative peak of the total ripple current $\hat{I}_A(t)$, $\hat{I}^-_{i,min}$ is obtained if the turn on of the leg A is synchronized with the turn off of the leg B, as shown in figure 7.8a. Since the duty-cycles d_A and d_B are independent, the turn on of leg B does not correspond to the turn off of leg A, therefore, the negative peaks of its components $\hat{I}_{AA}(t)$ and $\hat{I}_{AB}(t)$ are not in phase, and the maximum positive peak value of $\hat{I}_A$, $\hat{I}^+_{i,max}$ is lower than their sum:

$$\begin{cases} \hat{I}^-_{A,min} & = -\frac{1}{2}(\Delta I_{AA} + \Delta I_{AB}) \equiv \hat{I}_A(t_{AH,ON}) \\ \hat{I}^+_{A,max} & < +\frac{1}{2}(\Delta I_{AA} + \Delta I_{AB}) \end{cases} \tag{7.23}$$

This condition is particularly favourable, since the maximum amplitude of the ripple current is obtained when it is required to achieve ZVS, while, when ZVS is already obtained even without the contribution of ripple current, the ripple is lower. Since the matrix Γ must be symmetric, the same considerations apply in case of the current I_B: in this case, the positive ripple current is maximum at the turn-on of the low switch.

$$\begin{cases} \hat{I}^-_{B,min} & > -\frac{1}{2}(\Delta I_{BA} + \Delta I_{BB}) \\ \hat{I}^+_{B,max} & = +\frac{1}{2}(\Delta I_{BA} + \Delta I_{BB}) \equiv \hat{I}_B(t_{BL,ON}) \end{cases} \tag{7.24}$$

The instantaneous value of the current I_A at the turn-on of S_{AH} and of I_B at the turn-on of S_{BL} are the following:

$$I_A(t_{A,ON}) = I^*_A + \hat{I}_A(t_{A,ON}) = I^*_A - \frac{1}{2}\frac{V_{DC}}{f}\left[d_A(1-d_A)\Gamma_{1,1} + d_B(1-d_B)\Gamma_{1,2}\right] \tag{7.25}$$

$$I_B(t_{B,OFF}) = I^*_B + \frac{1}{2}\frac{V_{DC}}{f}\left[d_A(1-d_A)\Gamma_{2,1} + d_B(1-d_B)\Gamma_{2,2}\right] \tag{7.26}$$

It is thus sufficient to design the magnetics and to choose the switching frequency f in order to obtain a negative $I_{A,ON}$ and a positive $I_{B,OFF}$ to verify ZVS in both legs.

Assuming the sign of the low frequency component to remain unchanged during the operation of the converter, the opportune synchronization of the turn on and turn off can easily be implemented in the PWM peripheral of a microcontroller, so that calculating the phase shift for each step is no longer required.

That leaves to the control the task of calculating only the frequency, if variable frequency is required. This can be obtained given the duty cycles and low frequency currents, by calculation or simply by using a look-up table.

$$\begin{cases} f_{ZVS,Aon} < \dfrac{1}{2}\dfrac{V_{DC}}{I_{ZVS}+I_A(t)^*}\left[d_A(1-d_A)\Gamma_{1,1}+d_B(1-d_B)\Gamma_{1,2}\right] & \text{(7.27a)} \\ f_{ZVS,Boff} < \dfrac{1}{2}\dfrac{V_{DC}}{I_{ZVS}-I_B(t)^*}\left[d_A(1-d_A)\Gamma_{2,1}+d_B(1-d_B)\Gamma_{2,2}\right] & \text{(7.27b)} \end{cases}$$

If the chosen switching frequency verifies (7.27a), S_{AH} turns on in ZVS conditions, while S_{BL} turns on in ZVS if (7.27b) is verified. The switching frequency that achieves ZVS conditions in both legs with the lowest current ripple is the minimum of the two.

It should be noted that the use of SeTCM is not limited to the case in which the sign of the low frequency currents never changes: for example, if, during the operation of the converter, the sign of both I_A^* and I_B^* is inverted, it is sufficient to reconfigure the PWM modulator for case B.

7.4.1 Comparison between TCM, eTCM and SeTCM

Since SeTCM reduces the degrees of freedom of the system, by fixing the phase shift, it follows that its performances are reduced compared to eTCM. In particular, eTCM offers better performances when the ZVS condition is easily met, that is, when the product between the maximum switching frequency and the inductance L is small; while the performances of eTMC and SeTCM are similar in the opposite condition (that is, if the inductance is relatively high).

TCM offers the possibility of choosing a different switching frequency for each fundamental cell. As consequence, TCM performances can be better in some cases, in terms of lower current flowing in the filtering inductor. However, for the

same reason, the RMS and peak current in all the components that are affected by the sum of the currents of the cells, such as, for example, a common DC link capacitor, are much higher, both in terms of RMS and peak value.

An example of this is shown in the next section, where TCM, eTCM and SeTCM are applied to the JCC topology.

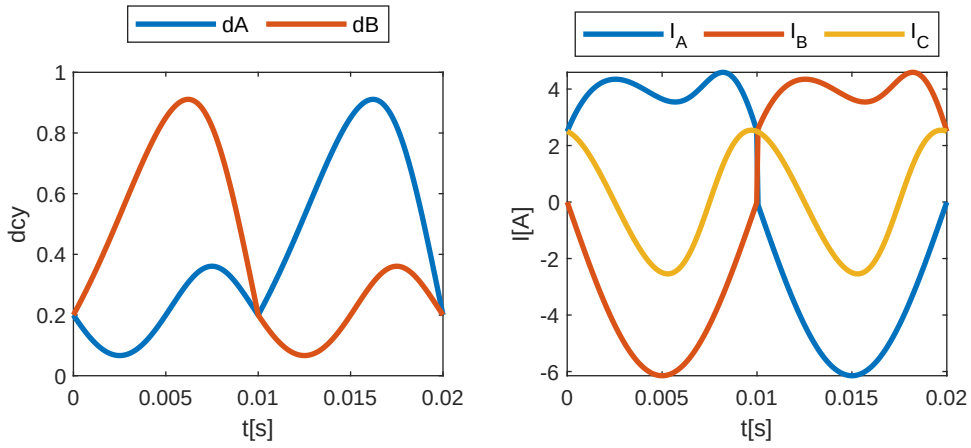
7.5 Design example: application to JCC

In order to compare the performances of the proposed modulations and design method, TCM, eTCM and SeTCM are applied to the JCC converter, where steady-state conditions are assumed, as shown in Fig.7.9. It is also assumed that the voltage drop on the capacitive network formed by C_{AB} and C is negligible at switching frequency. The range for the switching frequency is assumed to span between 50kHz and 150kHz.

The design procedure was taken forward choosing minimum RMS, using the algorithm described in section 7.2.1, where, given a magnetic structure, for each switching instant the duty cycles and low frequency current component are given as input and the best switching frequency and phase are calculated, independently from the others, as explained in section 7.3. The same algorithm was used for SeTCM, by limiting the choice of phase shift to the single value indicated by SeTCM, according to the sign of the low frequency current component.

The envelopes of the currents obtained with the three different modulation methods are shown in fig.7.10, where are plotted, from top to bottom, the currents I_A and I_B, the current flowing in the capacitor I_C, which is the sum of the two, and the DC link current I_{DC}.

The TCM has poor performances in this application, especially at fixed swtiching frequency. This happens because in some moments of the AC period, the duty cycle is very close to the boundaries when the low frequency current flowing in the output inductor is high, while in other moments the current is low when the duty cycle is close to 0.5. As can be seen in (7.5), in the first case a small inductor is required to obtain enough current ripple to achieve ZVS, while in the second case



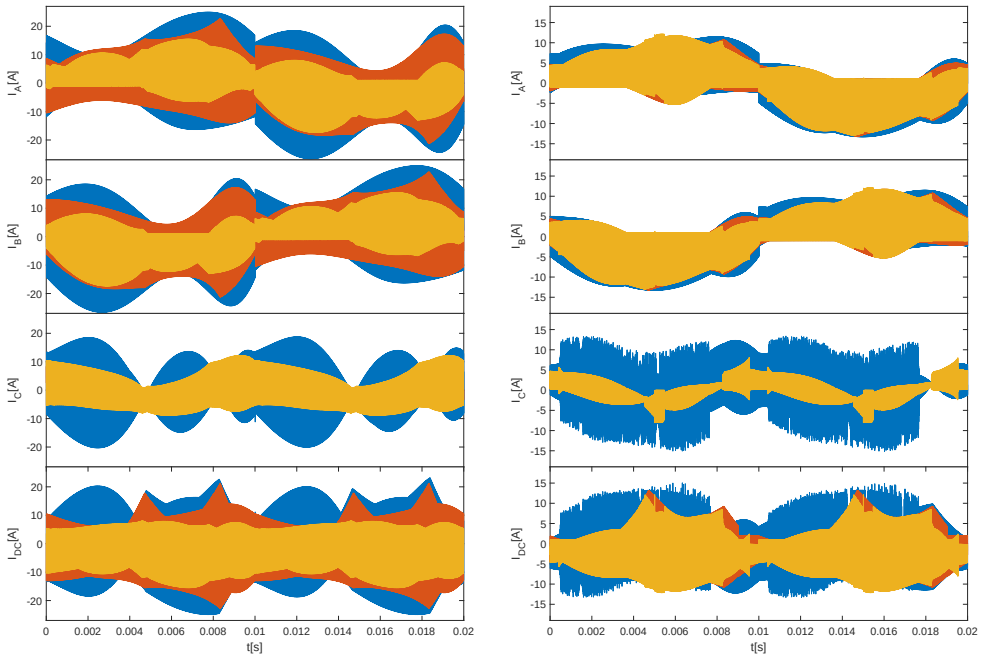
(a) (b)

Figure 7.9: JCC converter: low frequency steady state duty cycles and currents

the ripple current is sufficient even with a bigger inductor. Since the inductor is chosen in order to obtain ZVS over the entire period, it follows that the ripple current in case of fixed frequency TCM is often much bigger than required, as can be seen in table 7.1.

With its ability to choose the best phase shift for every switching period, the eTCM achieves significantly better performances in terms of lower current RMS and peak, since it manages, with the same magnetic circuit, to modulate the amplitude of the ripple current so that it is close to the minimum required for ZVS. SeTCM achieves intermediate performances.

In case of variable switching frequency, the performance of the three modulation techniques are similar in terms of I_A and I_B RMS and peak value, however, both eTCM and SeTCM generate a much lower ripple current in the power decoupling capacitor and the DC link capacitor, improving efficiency. This happens because the two arms are modulated at different frequencies, as explained in the previous section. On the other hand, the size of the required magnetics is slightly lower for TCM, as shown in table 7.1. In this scenario, the performances of eTCM ans SeTCM are similar, even if eTCM achieves a lower peak current in the power decoupling capacitor and operates at lower switching frequency, as shown in Fig.7.11b.

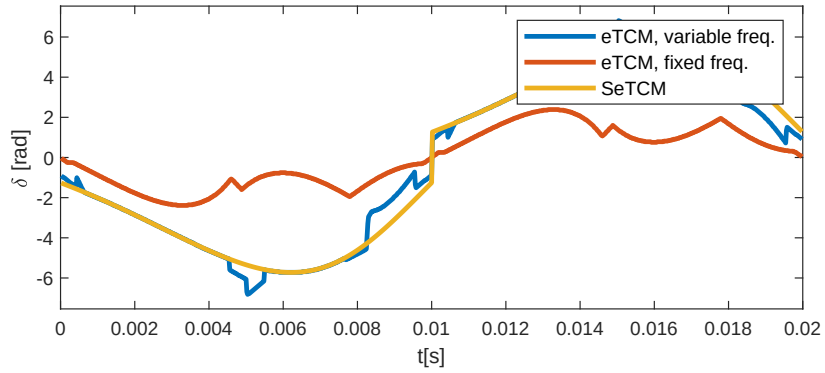


(a) Fixed frequency (b) Variable frequency

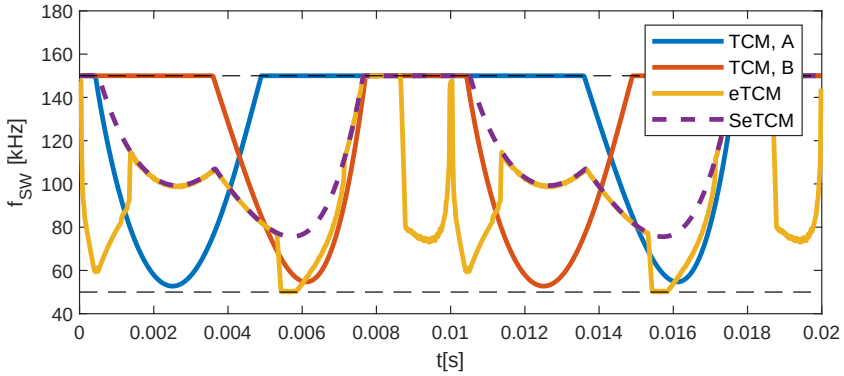
Figure 7.10: Variable operating point eTCM: application to JCC

			$\mathbf{I_A, I_B}$		$\mathbf{I_C}$		$\mathbf{L_A, L_B}$	$\mathbf{L_C}$	$\mathbf{E_L}$
			RMS	Peak	RMS	Peak			
fixed	frequency	TCM	10.1 A	26.6 A	7.4 A	20.3 A	$55\mu H$	–	46.1 mJ
		eTCM	5.9 A	17.4 A	4.9 A	12.2 A	$60\mu H$	$70\mu H$	26.0 mJ
		SeTCM	8.5 A	22.7 A	3.2 A	8.7 A	$60\mu H$	$70\mu H$	36.9 mJ
variable	frequency	TCM	5.5 A	13.3 A	5.1 A	15.2 A	$55\mu H$	–	11.4 mJ
		eTCM	5.3 A	13.2 A	2.2 A	4.4 A	$60\mu H$	$70\mu H$	13.3 mJ
		SeTCM	5.4 A	13.3 A	2.2 A	8.7 A	$60\mu H$	$70\mu H$	14.6 mJ

Table 7.1: Modulations comparison



(a) Optimum phase shift



(b) Optimum switching frequency

Figure 7.11: Results of eTCM algorithm

Chapter 8

Practical implementation of SeTCM on JCC

In this chapter, the SeTCM modulation, introduced in 7.4, is applied to the Jumping Capacitor Converter.

The steady state duty cycles and current waveforms of the JCC were used as application example in the previous chapter, however, only the theoretical steady state waveforms of the ripple current were calculated. This chapter describes the steps that must be taken in order to apply the SeTCM to the real converter, taking into account the implementation of the control structure, of the modulator, operating at variable frequency, and at the same time the implementation of the phase shift control.

A detailed description of the implementation of SeTCM in the DSP is included. It is shown that the variable phase shift of SeTCM can be easily implemented by opportune configuration of the PWM peripheral of the DSP, obtaining the required modulation without making use of additional CPU time.

8.1 Application of SeTCM to JCC

As shown in the previous chapter, SeTCM offers similar performances in terms of ripple current peak and RMS compared to eTCM. Because of its reduced complexity compared to eTCM, SeTCM is chosen to be implemented on the

JCC.

The SeTCM can be applied to the JCC, considering two fundamental cells: the one formed by S_{AH}, S_{AL} and L_A, and the one formed by S_{BH}, S_{BL} and L_B. In order to do so, the requirements to apply variable operating point eTCM, described in the previous chapter, must be met. The requirements are the following:

- the influence of the ripple component of the currents on the high and the low side voltage source of the two fundamental cells is negligible, in other words, the voltage ripple must be small compared to the high side voltage;
- the phase shift has slow variation in time.

The two fundamental cells have the same high voltage source, constituted by C_{DC}, and different low voltage sources, constituted by the network of C and C_{AB}. In order to meet the first requirement it is sufficient, in the design stage, to size the capacitor C_{AB} in order to limit the voltage ripple, knowing the amplitude of the current ripple.

In SeTCM the phase shift is tied to the duty cycles, for this reason, the second requirement is obtained if the duty cycles are slowly changing. Since the steady-state duty cycles are slowly changing, the slow variation of phase is verified if the control effort is limited.

In addition to that, the magnetic circuit has to be modified, in order to obtain mutual coupling between L_A and L_B. The inductor L_C (see Fig.8.1), has the effect of introducing a mutual action of the ripple voltage generated on each half bridge on both currents I_A and I_B, as required by eTCM. The current flowing through L_C is the sum of I_A and I_B; for this reason, the effect of L_C is similar to that of a positive mutual coupling between the inductors L_A and L_B (in other words, introducing an ideal common mode choke with zero leakage inductance and mutual equal to L_C results in the same inductance matrix $\mathcal{L}$).

The presence of L_C modifies the dynamic behaviour of the system, hence, the control system has to be tuned accordingly, taking also into account the variable switching frequency modulation. Moreover, the voltage drop on L_C translates in

a common mode voltage applied to the AC port; for this reason, the AC and DC filter must be modified.

In summary, in order to apply eTCM to the JCC, the JCC has to be modified, in terms of:

- topology, with the insertion of the additional inductor L_C;
- design of the input and output filters, due to the worse performances in terms of higher common mode noise;
- control structure, able to operate with variable switching frequency.

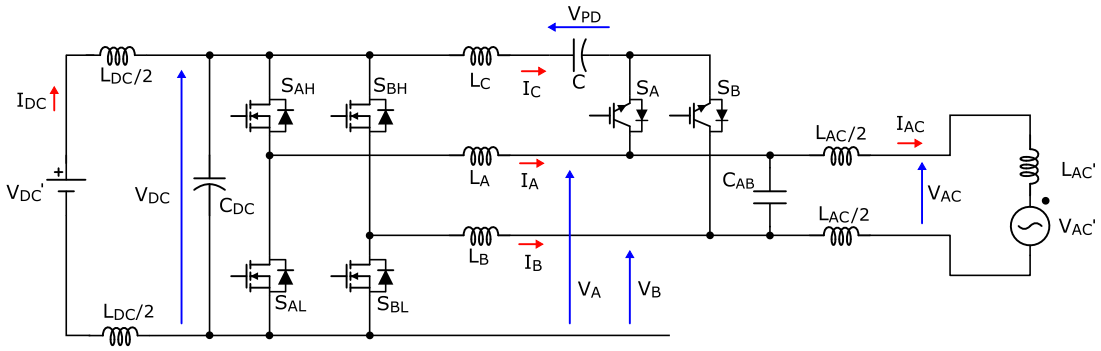


Figure 8.1: JCC modified for eTCM

With reference to Fig.8.1, assuming $L_A = L_B = L$, the inductance matrix is:

$$\mathcal{L} = \begin{bmatrix} L + L_C & L_C \\ L_C & L + L_C \end{bmatrix} \quad \Gamma = \mathcal{L}^{-1} = \frac{1}{L(L + 2\,L_C)} \begin{bmatrix} L + L_C & -L_C \\ -L_C & L + L_C \end{bmatrix} \tag{8.1}$$

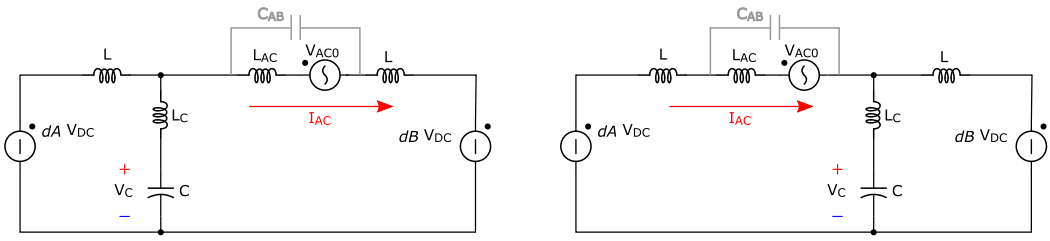
In order for C_{AB} to behave like a voltage source, its value is chosen so that the resonant frequency introduced by it is significantly lower than the switching frequency. A capacitance of $1\mu F$ is used, resulting in a resonating frequency $f_{C_{AB}}$ of $15.86kHz$, as calculated in (8.2), which is lower than the minimum switching frequency ($50kHz$).

$$L_{AB,eq} = L_{AC}//(L_C + L_A//L_B) \quad f_{C_{AB}} = \frac{1}{2\pi}(C_{AB}L_{AB,eq})^{-1/2} = 15.86kHz \tag{8.2}$$

Rated power	P	1	kW
DC voltage	V_{DC}	500	V
AC voltage	V_{AC}	240	V_{RMS}
	f_{AC}	50	Hz
Power decoupling capacitor	C	80	μF
C DC offset voltage	V_0	400	V
Switching frequency	f	50-150	kHz
Filtering inductors	L_A, L_B	60	μH
	L_C	70	μH
AC filter	C_{AB}	1	μF
	L_{AC}	1000	μH
DC filter	L_{DC}	10	μH
	C_{DC}	10	μF

Table 8.1: JCC modified for eTCM: Circuit parameters

8.2 Control



(a) Mode A (b) Mode B

Figure 8.2: Small signal model

The proposed control method is able to follow a grid current reference and mitigate the dc-link current ripple. This control solution is suitable to be used as inner loop for a cascade control system, making possible the use of a slow outer loop for DC voltage control.

A null grid inductance is considered here as worst case scenario, so that the equivalent grid inductor is equal to L_{AC} (see figure 8.1). The equivalent small

signal circuit for each mode of operation is shown in figure 8.2.

The transfer functions of the system for each operating mode are:

MODE A:

$$i_{AC}(s) = \frac{V_{DC}}{sL_{EQ}(s^2/\omega_P^2+1)}\Big[(s^2/\omega_{Z1}^2+1)d_A - (s^2/\omega_{Z2}^2+1)d_B\Big] \tag{8.3}$$

$$v_C(s) = \frac{V_{DC}}{s^2/\omega_P^2+1}(k_1 d_A + k_2 d_B) \tag{8.4}$$

MODE B:

$$i_{AC}(s) = \frac{V_{DC}}{sL_{EQ}(s^2/\omega_P^2+1)}\Big[(s^2/\omega_{Z2}^2+1)d_A - (s^2/\omega_{Z1}^2+1)d_B\Big] \tag{8.5}$$

$$v_C(s) = \frac{V_{DC}}{s^2/\omega_P^2+1}(k_2 d_A + k_1 d_B) \tag{8.6}$$

where:

$$L_{EQ} = L_{AC} + 2L \qquad \omega_P = \frac{1}{\sqrt{C[L_C + \frac{L(L+L_{AC})}{2L+L_{AC}}]}} \tag{8.7}$$

$$k_1 = \frac{L_{AC}+L}{L_{AC}+2L} \qquad \omega_{Z1} = \frac{1}{\sqrt{C(L_C+L_{AC}+L)}} \tag{8.8}$$

$$k_2 = \frac{L}{L_{AC}+2L} \qquad \omega_{Z2} = \frac{1}{\sqrt{CL_C}} \tag{8.9}$$

The system is a MIMO with two inputs, the duty cycles d_A and d_B, and two outputs, i_{AC} and v_C. In order to decouple the system, a decoupling matrix is used. Using the decoupling matrix $\mathcal{K}_A$ in mode A and $\mathcal{K}_B$ in mode B, as defined in (8.10), the same transfer functions are obtained in both modes of operation.

$$\begin{vmatrix} dA \\ dB \end{vmatrix} = \Big[\mathcal{K}\Big] \cdot \begin{vmatrix} u_{AC} \\ u_{DC} \end{vmatrix} \tag{8.10}$$

$$\mathcal{K}_A = \begin{bmatrix} \frac{k_1}{k_1+k_2} & 1 \\ -\frac{k_2}{k_1+k_2} & 1 \end{bmatrix} \simeq \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \quad \mathcal{K}_B = \begin{bmatrix} \frac{k_2}{k_1+k_2} & 1 \\ -\frac{k_1}{k_1+k_2} & 1 \end{bmatrix} \simeq \begin{bmatrix} 0 & 1 \\ -1 & 1 \end{bmatrix} \tag{8.11}$$

The resulting transfer functions are:

$$i_{AC}(s) = \frac{V_{DC}}{sL_{EQ}(s)(s^2/\omega_P^2+1)}\Big\{\Big[1 + s^2\Big(\frac{k_1}{\omega_{Z2}^2} + \frac{k_2}{\omega_{Z1}^2}\Big)/(k_1+k_2)\Big]u_{AC}(s) + \tag{8.12}$$

$$+ s^2\Big(\frac{1}{\omega_{Z1}^2} - \frac{1}{\omega_{Z2}^2}\Big)u_{DC}(s)\Big\} \tag{8.13}$$

$$v_C(s) = \frac{1}{s^2/\omega_P^2+1}u_{DC}(s) \tag{8.14}$$

Because of the power balance, a change in the power decoupling capacitor voltage V_C causes a change in the I_{DC} current. The system can be linearised as follows:

$$P_{DC} = P_C + P_{AC} \;\Rightarrow\; V_{DC}(I^*_{DC} + i_{DC}) = C(V^*_C + v_C)\frac{d}{dt}(V^*_C + v_C) + P_{AC} = \tag{8.15}$$

$$\simeq CV^*_C\frac{d}{dt}(V^*_C + v_C) + P_{AC} \tag{8.16}$$

where I^*_{DC} and V^*_C are the low frequency components of DC current and capacitor voltage. The steady state components of power erase each other, leaving:

$$V_{DC}i_{DC} = CV^*_C\frac{d}{dt}v_C \qquad \Rightarrow \qquad i_{DC}(s) = \frac{V^*_C(s)}{V_{DC}} * \frac{sC}{s^2/\omega_P^2 + 1}u_{DC}(s) \tag{8.17}$$

8.2.1 AC current controller

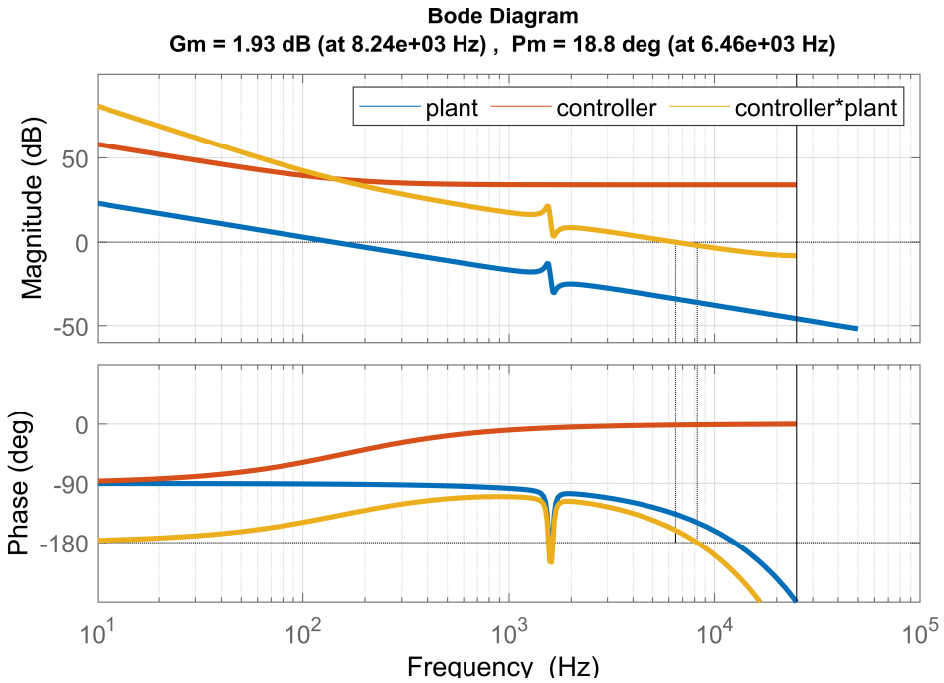


Figure 8.3: SeTCM on JCC - Bode blot of current controller

The AC current controller is designed given the transfer function (8.13), where the influence of U_{DC} is neglected. A PI controller is chosen, for its simplicity.

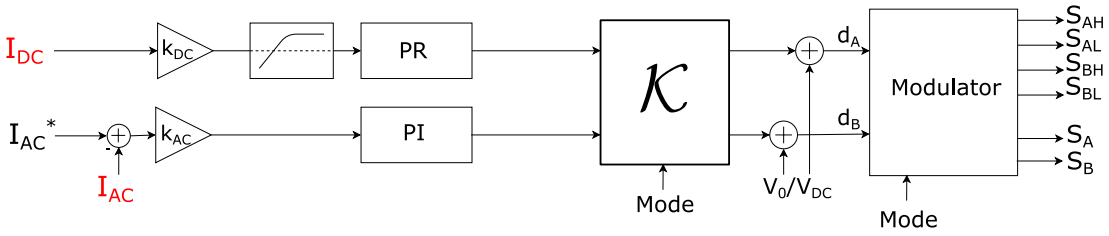


Figure 8.4: Control structure. Measured signals are written in red.

8.2.2 DC current controller

The chosen DC current controller is the same used for the JCC topology with normal modulation, as described in Chapter 6.

8.2.3 Control structure

The introduction of the inductor L_C complicates the control of the system because it introduces a coupling. However, if the AC filter inductor L_{AC} is sufficiently big compared to L, the term $\frac{k_1}{k_1+k_2}$ is close to 1 and $\frac{k_2}{k_1+k_2}$ is around 0. In this case, the control structure is very similar to the one described in chapter 6, for both the AC and the DC controllers. The only difference consists in a opportune tuning of the AC controller, due to the different size of the passives, especially the AC filter inductor.

8.3 Implementation in DSP

8.3.1 Control algorithm

The proposed control structure was applied in a DSP. The implementation of the controller is complicated by the choice of operating the PWM modulator at variable switching frequency. In order to simplify the implementation, it is chosen to operate the controller at a fixed switching frequency equal to 50kHz.

This translates in a variable delay in the control chain. Since the PWM frequency varies in a range spanning from 50 to 150kHz, it follows that the maximum delay happens when the PWM frequency is at is lowest, and is equal to the sum

of the control delay and the PWM period.

The worst case scenario thus corresponds to a time delay of $40\mu s$. Since the effect of a time delay is a reduction of the phase margin at high frequencies, it follows that, if the system is stable at the maximum delay, it is also stable for smaller delays.

8.3.2 Configuration of the modulator

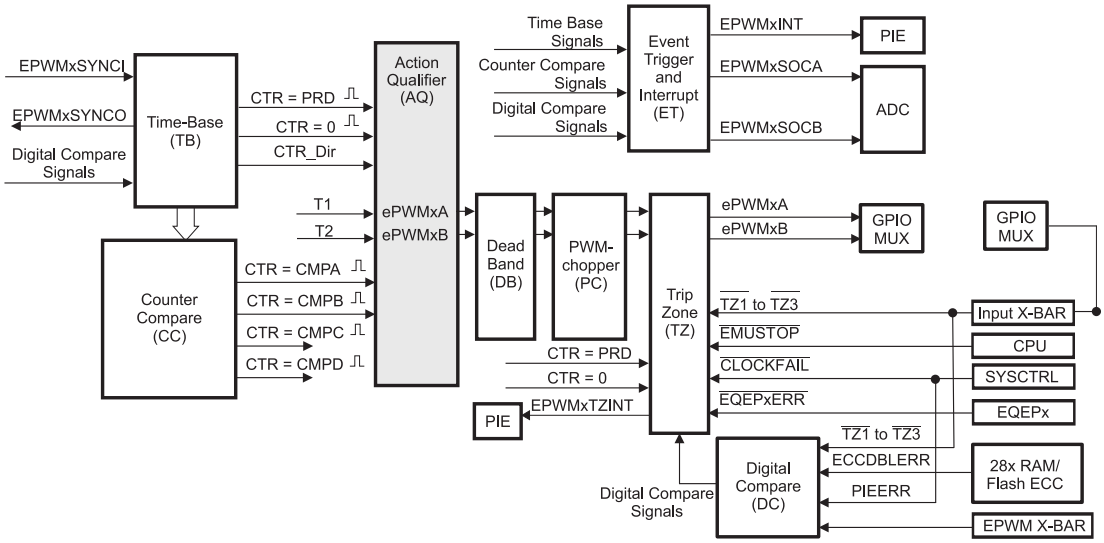


Figure 8.5: Internal configuration of C2000 ePWM block [11]

The main advantage of the SeTCM modulation lay in its simplicity of implementation in the microcontroller. In this section, the implementation of SeTCM on a C2000 DSP is described. The implementation makes use of an opportune configuration on the PWM peripheral included in the DSP in order to achieve the required phase shift with minimal CPU overhead or intervention.

The TMS320F28377S by Texas Instruments is equipped with 24 PWM modulators, each of which is structured as shown in Fig.8.5, and is composed by the following submodules:

- Time-Base module (TB), where the PWM carrier wave is generated, and flags are assigned in case of the carrier reaching its limits.
- Counter Compare (CC), where the carrier is compared with up to four different thresholds, and flags are assigned accordingly.

- Action Qualifier (AQ), where up to two control signals ePWMxA and ePWMxB are set or cleared according to the flags coming from the TB and CC.

- Dead Band module (DB), where the two PWM output are defined according to the state of ePWMxA and ePWMxB.

Other submodules, responsible for the trips and the generation of interrupts are not used for SeTCM and are not discussed here.

Two PWM channels are used, one for each leg of the JCC full bridge. The Time-Base module of both are configured to generate a triangular carrier, incrementing from zero to a value PRD that determines the switching period. The carriers of the two modules are synchronized, so that the carrier of the two modules is the same. One threshold of the comparator, CMPA, is set in the CC submodule of both channels to define the duty cycles.

The AQ module is configured to set the ePMWxA signal so that it corresponds to the PWM signal applied to the top device of the leg (neglecting the dead-time). The generation of the appropriate complementary signal for the low device, and the implementation of the dead time is taken care by the DB submodule. The output of the AQ is set or cleared according to the flag set by the TB module when the carrier is zero, or the one set by the CC module when the carrier is equal to the threshold CMPA. The configuration it changed every AC half-period, as defined in Tab.8.2.

		Carrier = 0	Carrier = CMPA	definition of CMPA
Mode A	Channel A	SET	CLEAR	CMPA=PRD*dcyA
	Channel B	CLEAR	SET	CMPA=PRD*(1-dcyB)
Mode B	Channel A	CLEAR	SET	CMPA=PRD*(1-dcyA)
	Channel B	SET	CLEAR	CMPA=PRD*dcyB

Table 8.2: Action Qualifier settings for SeTCM

Using the carrier reset to change the state of the PWM outputs ensures the

synchronization of the switching action required by the SeTCM, since the carriers of the two channels are synchronized.

The only operation that has to be carried over by the CPU are setting the period register of the TB and the comparators of the CC to obtain the required duty cycles and switching frequencies, while the correct phase shift between the two legs is taken care by the peripheral.

In order to change the switching frequency, the reference value of the period for each switching cycle is stored in a look-up table. During each iteration of the control loop, the CPU updates the period register of the PWM peripheral.

8.4 Conclusion

In this Chapter, a practical implementation of the SeTCM current mode was described, describing the steps that have to be taken in order to implement it, that are a modified magnetic structure that introduces a mutual action between the fundamental cells, and a different implementation of the PWM modulation. In addition to that, the control of the converter needs to take into account the alteration in the magnetic structure, and has to be modified accordingly.

The main challenge of applying the proposed technique to an existing topology constitute in the increased complexity of the control, due to the introduction of the dependency between the ripple currents, while the implementation of the modulation proves to be relatively easy, as it can be obtained simply by an opportune configuration of the PWM peripheral of a DSP.

In the next chapter, the hardware setup used to get experimental validation for the topologies proposed in this thesis is described, and the obtained experimental results are exposed.

Chapter 9

Experimental results

This Chapter contains the experimental results for the two proposed topologies presented in Chapter 5 and 6. In order to test the novel topologies, a reconfigurable experimental setup was designed, built and tested.

In the first section, the hardware setup is described. In the following sections, the experimental results for the DFBC, the JCC and the application of SeTCM on JCC are discussed.

9.1 Reconfigurable hardware setup

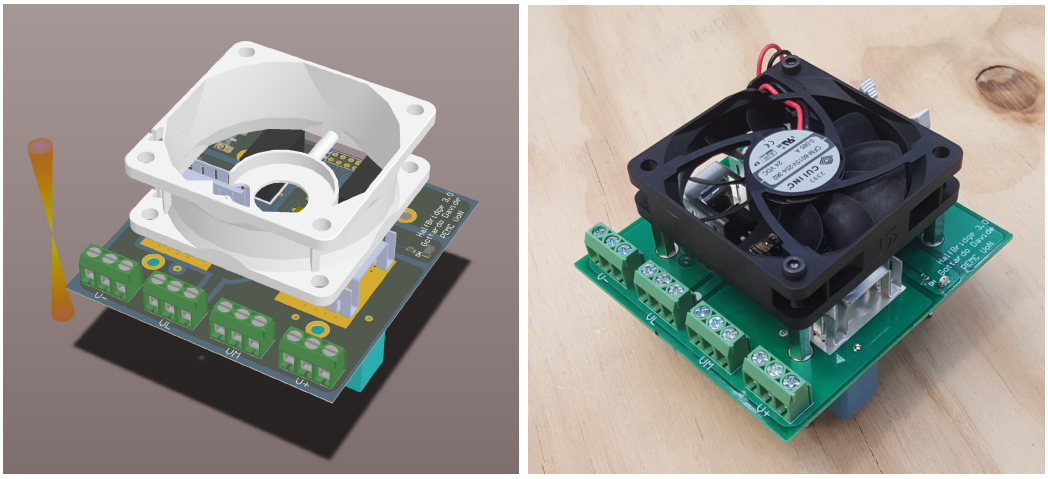
The experimental setup is formed by six galvanically-isolated half bridge modules, and a control board.

The topologies to be validated and tested are implemented by opportune connections between the half bridge modules, and by the introduction of the required passive components.

9.1.1 Half bridge modules

Each module hosts the two active devices, the gate drivers and the gate drive power supplies.

Figure 9.1 shows both the 3D render (a) of the experimental half bridge module and a photograph (b), highlighting the input and output connections, the fan



(a) (b)

Figure 9.1: Experimental setup: Half bridge module

and heatsink. The active devices are mounted on the surface of the PCB directly underneath the fan.

Heat removal is achieved with the use of aluminium heatsinks, soldered directly on the drain connection situated on the bottom of the active devices.

The soldering area on the PCB for the power transistors was designed to be compatible with both D^2PAK and $TO\,263\,7$ packages, in order to be able to be adapted to a large number of active devices.

The schematic of the half bridge module and its gate drivers is shown in Fig.9.2.

The chosen gate drivers (1EDI60N12AF by Infineon [66]) are powered by a bipolar voltage and have a separate connection for the charging and the discharging resistor of the gate.

Each module has four power connections: the DC positive and negative terminal, marked as V+ and V-, the midpoint of the half bridge VL, and the midpoint VM of the DC link capacitor, which is formed by two film capacitors connected in series. One additional low LSR capacitor is placed in parallel with the DC link.

The control signals, transmitted via a flat cable, are the two complementary PWM signals that control the gate driver, and one enable line. The power supply

for the logic side of the gate driver is also provided by the same flat cable, while the power for the two isolated gate drive supplies and the fan is provided by a separate connector.

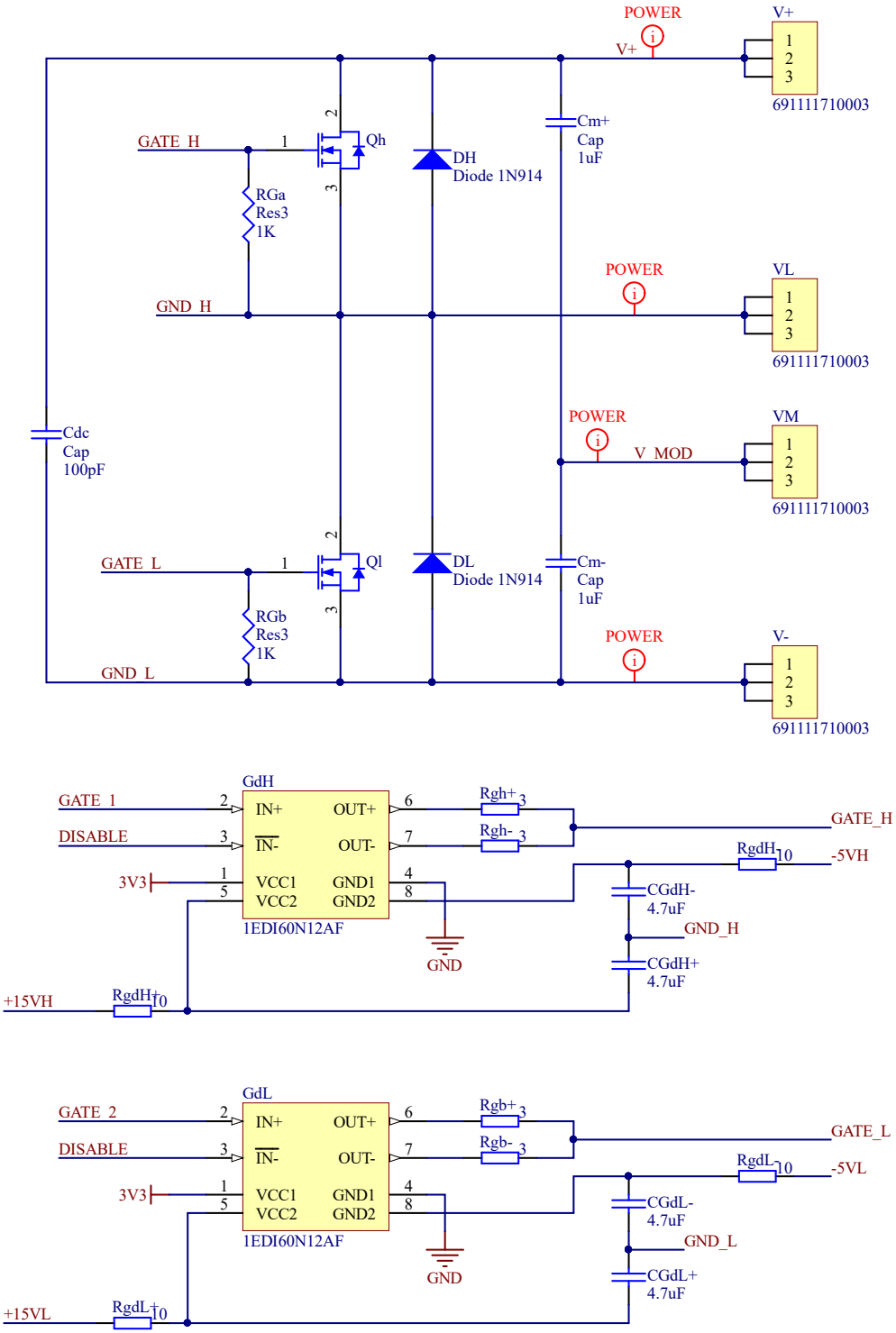


Figure 9.2: Half bridge module: schematic

9.1.2 Control board

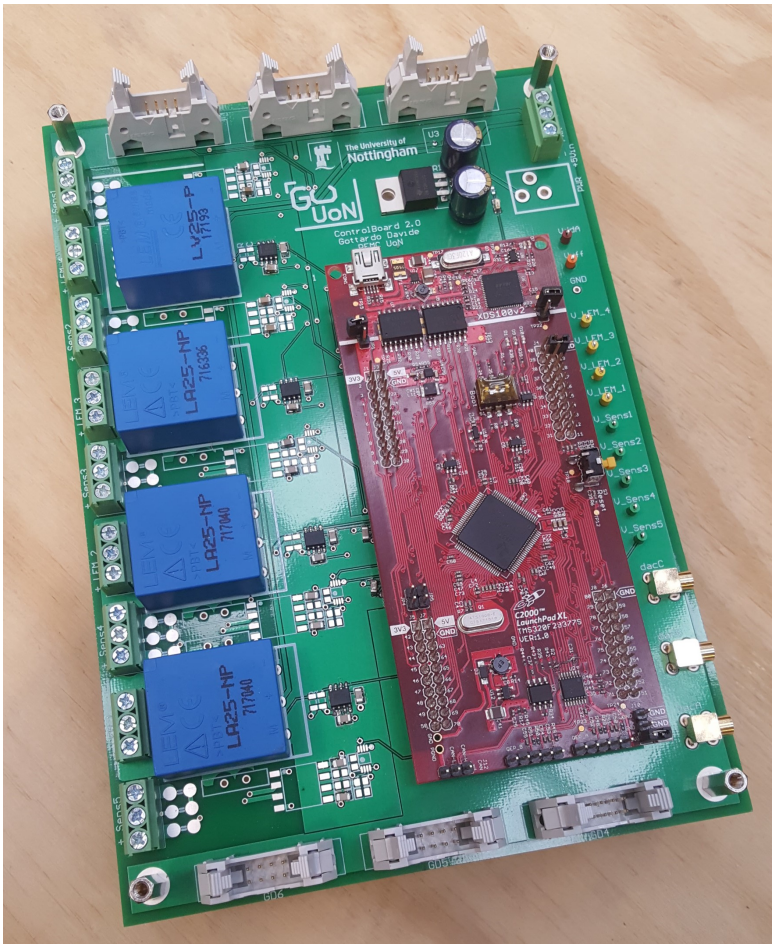


Figure 9.3: Experimental setup: Control board

The control board shown in fig.9.3 hosts a TI launchpad evaluation board, equipped with a C2000 MCU, the TMS320F28377S. The evaluation board contains a programmer-debugger, that can be used to control the converter with a PC.

The control board hosts six flat cable connectors to drive the half bridge modules, and nine sensor inputs that can be configured to be used as voltmeter or ammeter. Five inputs are constituted by an isolated analog voltage transducer, that can be connected to a voltage divider to use for reading voltages or to shunt resistors for current reading. The other four sensors are based on closed loop hall effect based transducers. The analog output of each voltmeter and ammeter is modified by an analog conditioning circuit and applied to the ADC inputs of the

MCU.

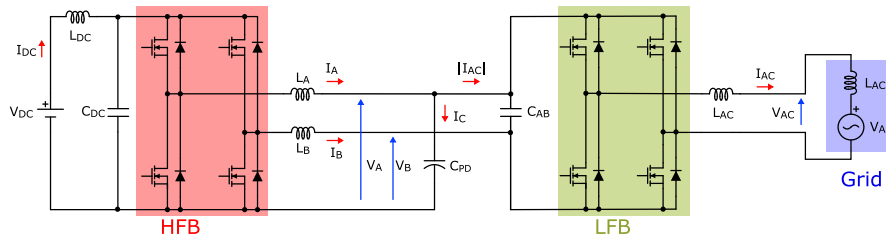
The TMS320F27377S includes three independent DAC channels, that are routed to three DBC connectors. They can be used, for example, to send real-time waveforms from the MCU to an oscilloscope, and/or to provide a triggering signal.

9.2 DFBC prototype

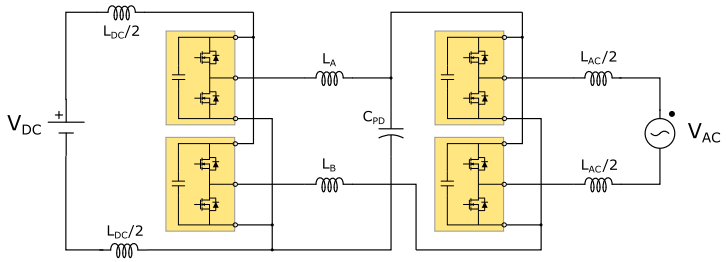
In this section, the experimental results for the DFBC are described.

A prototype of the DFBC topology was built using the experimental setup described in the previous section. To do so, four half bridge modules were used, two for the high frequency bridge and two for the low frequency bridge. To complete the topology, the following passives are added:

- the AC and DC inductors L_{AC}, L_{DC};
- the high frequency filtering inductors L_A and L_B;
- the power decoupling capacitor C_{PD};



(a)



(b)

Figure 9.4: DFBC implementation using the reconfigurable hardware setup

Figure 9.4 illustrates how the four half-bridge modules, together with the other passive components, are connected to obtain the required topology.

Since the main claim of the topology is its ability to obtain active ripple power decoupling, a small DC link capacitor was chosen, so that its influence on the 100Hz ripple component is negligible. For this reason, no additional DC capacitor is added, and the resulting DC link capacitance is equal to $1\mu F$, which corresponds to the parallel connection of the DC capacitors of the two half bridge modules used for the HFB.

In the same way, the filtering capacitor C_{AB} is constituted by the two DC link capacitors of the modules used for the LFB.

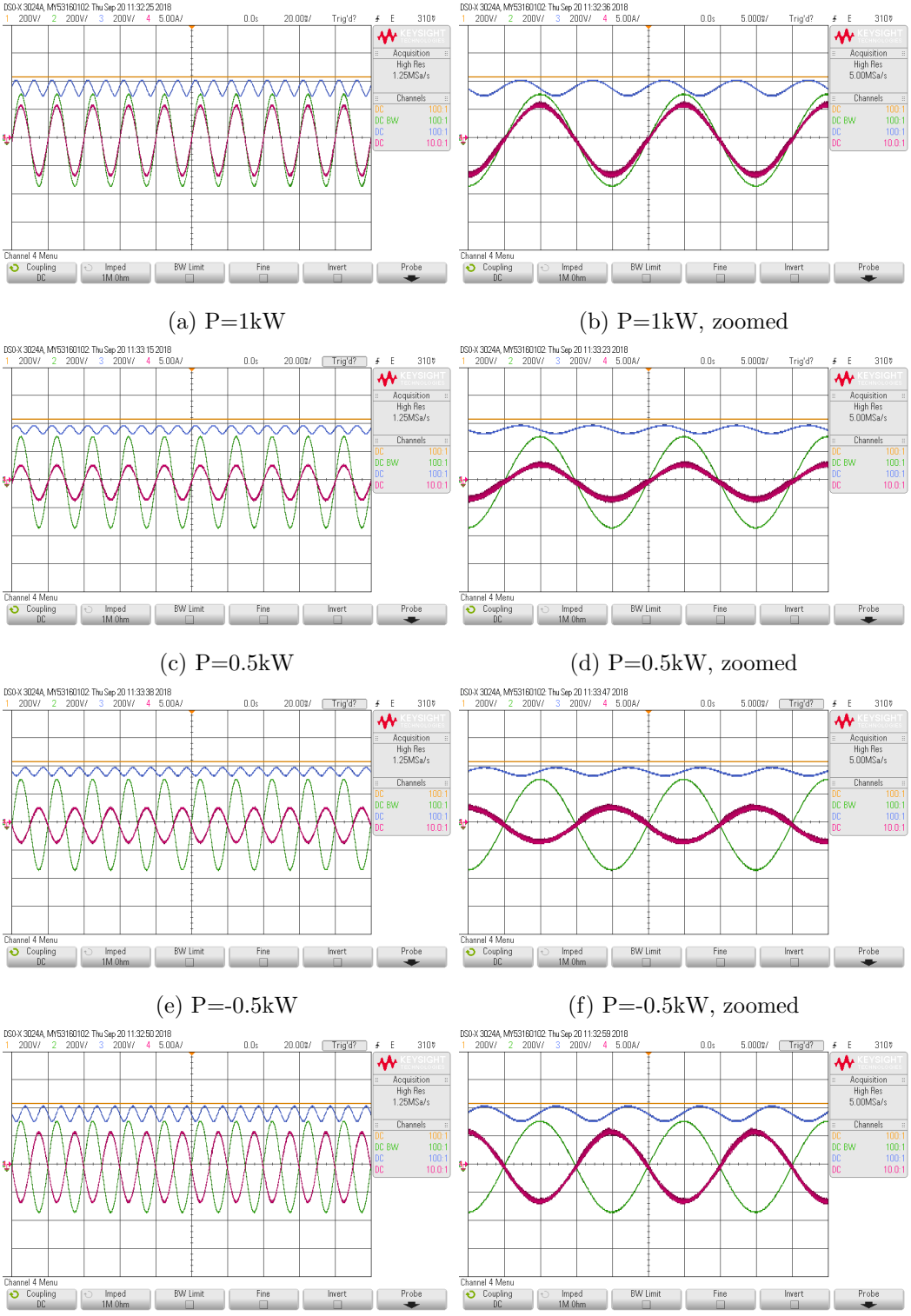
9.2.1 Experimental results: Steady-state

In order to validate the calculation shown in Chapter 5, regarding the steady-state waveform of voltage and current relative to the DFBC, a series of experimental waveforms were captured at different operating points of the converter.

The voltage and the current waveforms of the converter ports, where the power decoupling capacitor is intended as ripple port of the converter, are shown respectively in figures 9.5 and 9.6.

In each case, the power decoupling function is operating correctly, as can be seen by the waveforms of the DC current and of the power decoupling capacitor voltaqe. The grid voltage and current are in phase for positive current and 180 out of phase for negative current.

Figure 9.7 show the current waveforms of the currents I_A and I_B. Both currents are unidirectional, and the reduced amplitue of I_B due to the destructive interference between the capacitor current and the rectified AC current is visible.



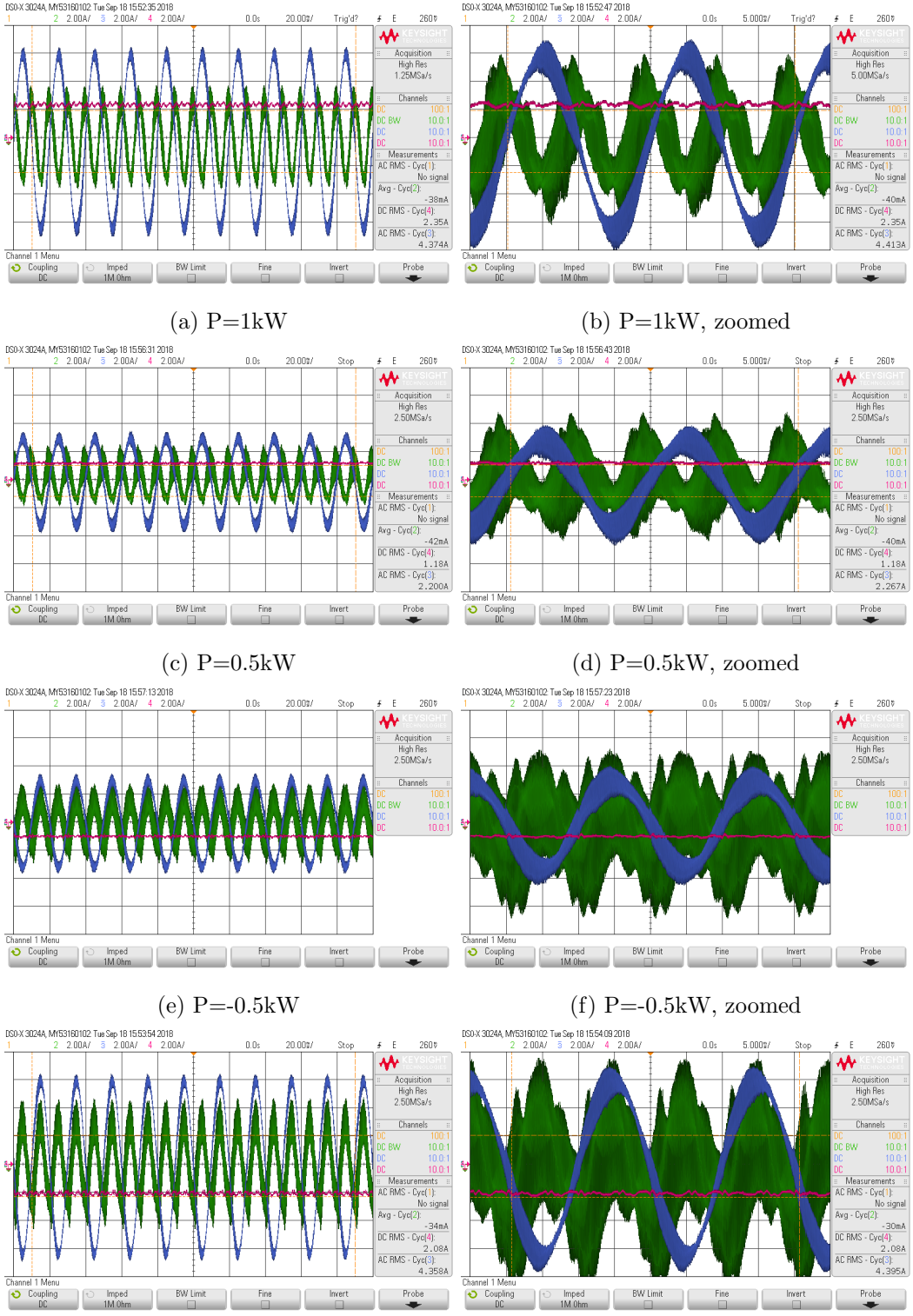
(a) P=1kW (b) P=1kW, zoomed

(c) P=0.5kW (d) P=0.5kW, zoomed

(e) P=-0.5kW (f) P=-0.5kW, zoomed

(g) P=-1kW (h) P=-1kW, zoomed

Figure 9.5: DFBC, steady state voltages: V_{DC} (yellow, 200V/div), V_{AC} (green, 200V/-div), V_C (blue, 200V/div), I_{AC} (red, 5A/div)



(a) P=1kW (b) P=1kW, zoomed

(c) P=0.5kW (d) P=0.5kW, zoomed

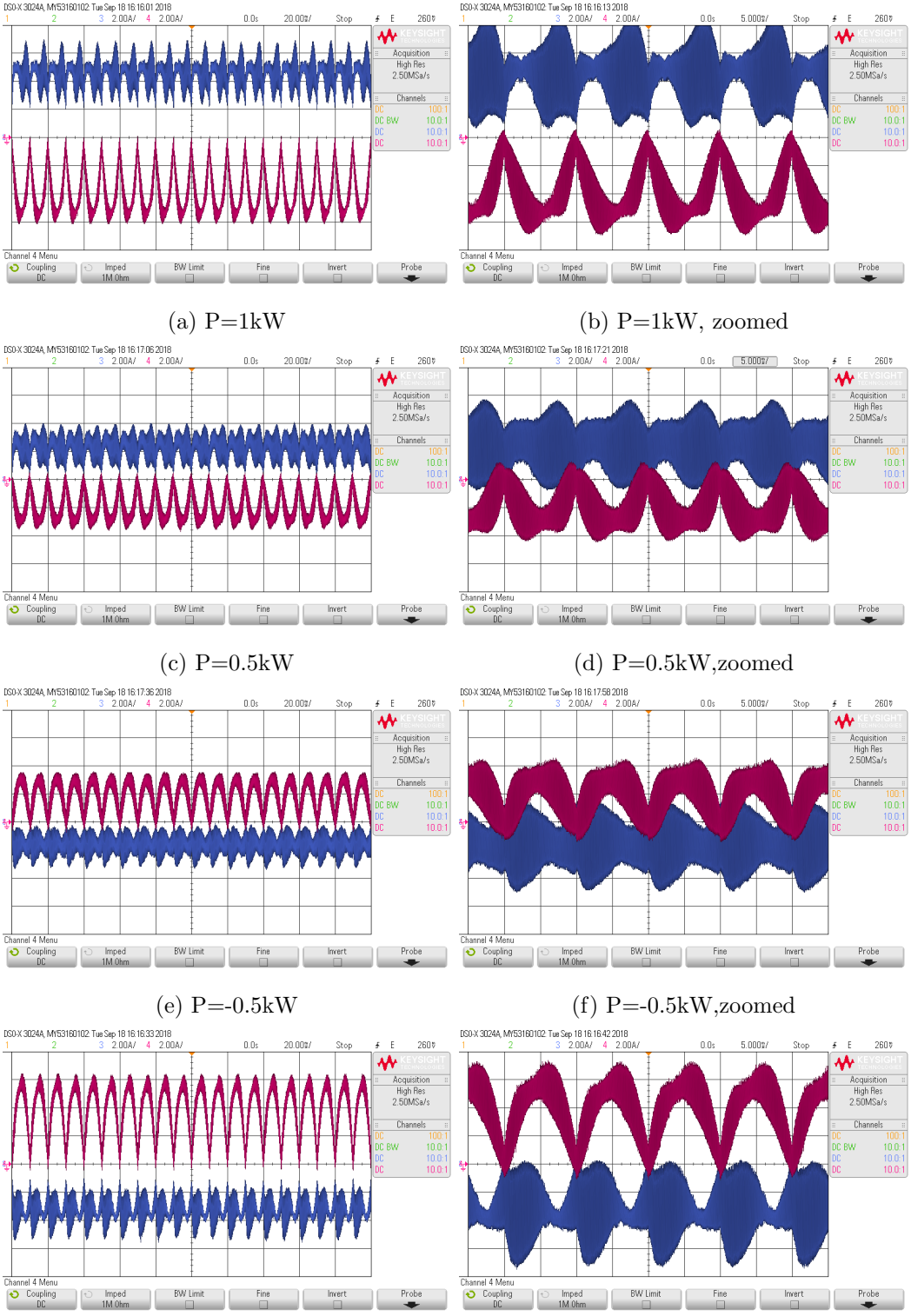
(e) P=-0.5kW (f) P=-0.5kW, zoomed

(g) P=-1kW (h) P=-1kW, zoomed

Figure 9.6: DFBC, steady state currents: I_C (green, 2A/div), I_{AC} (blue, 2A/div), I_{DC} (red, 2A/div)

9.2.2 Experimental results: Transient

The correct behaviour of the control system during transients is validated by applying a step change on the reference power.



(a) P=1kW (b) P=1kW, zoomed

(c) P=0.5kW (d) P=0.5kW,zoomed

(e) P=-0.5kW (f) P=-0.5kW,zoomed

(g) P=-1kW (h) P=-1kW

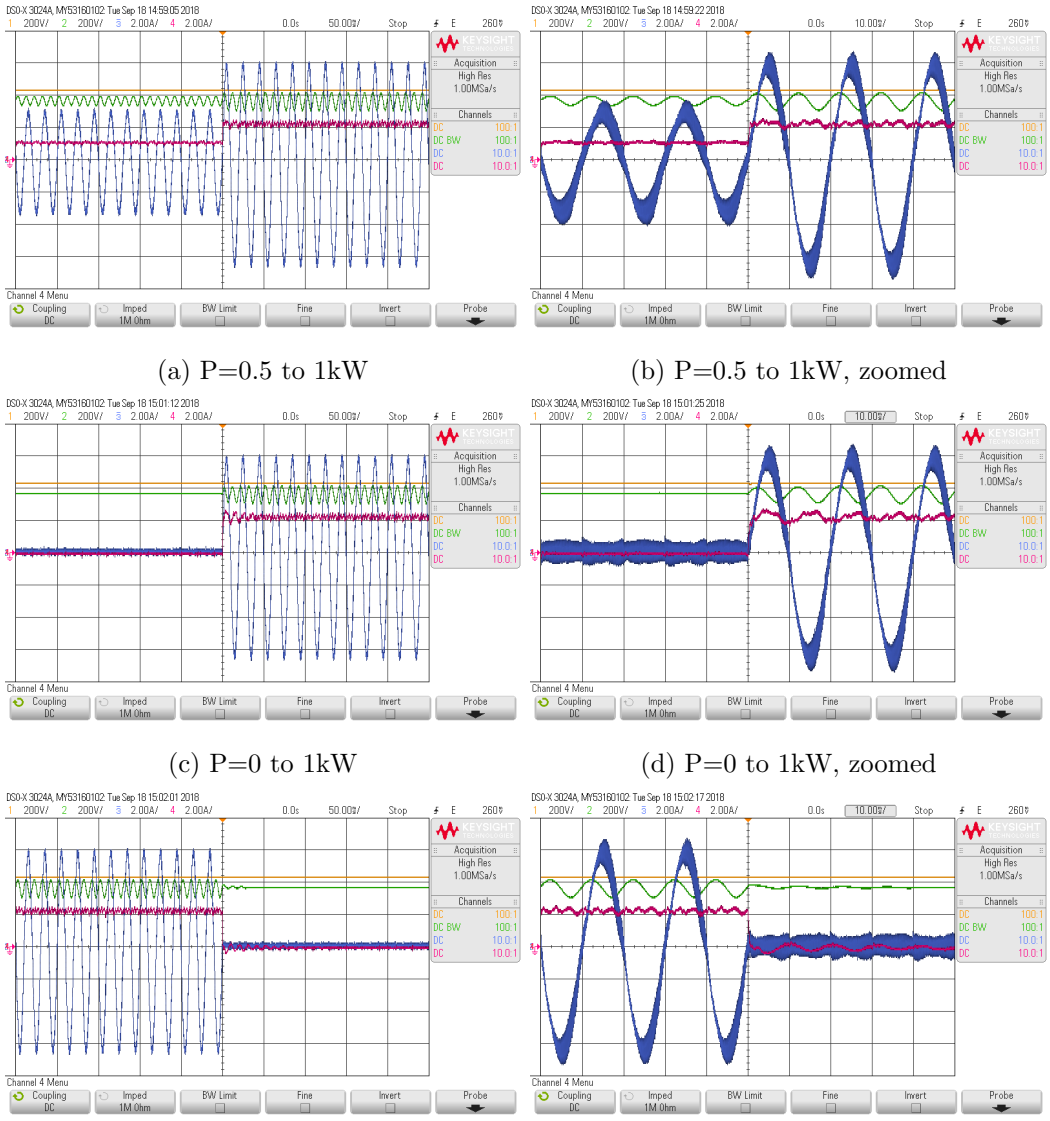
Figure 9.7: DFBC, steady state currents: I_A (blue, 2A/div), I_B (red, 2A/div)

The following oscilloscope screenshots show the waveforms of the DC voltage, power decoupling capacitor voltage, and AC current and voltage.

Several step transitions in the reference power were applied, and the oscillo-

scope screenshots of the waveforms of DC voltage, power decoupling capacitor voltage, and AC current and voltage were captured. The reference power is always positive in figure 9.8, that is, power is injected from the DC source to the grid; it is negative in Fig.9.9, while in Fig.9.10 power inversion is applied.

The control system of the converter is able to deal with significant step variations in the reference power, without stability issues and without distortion on the AC and DC currents.



(a) P=0.5 to 1kW

(b) P=0.5 to 1kW, zoomed

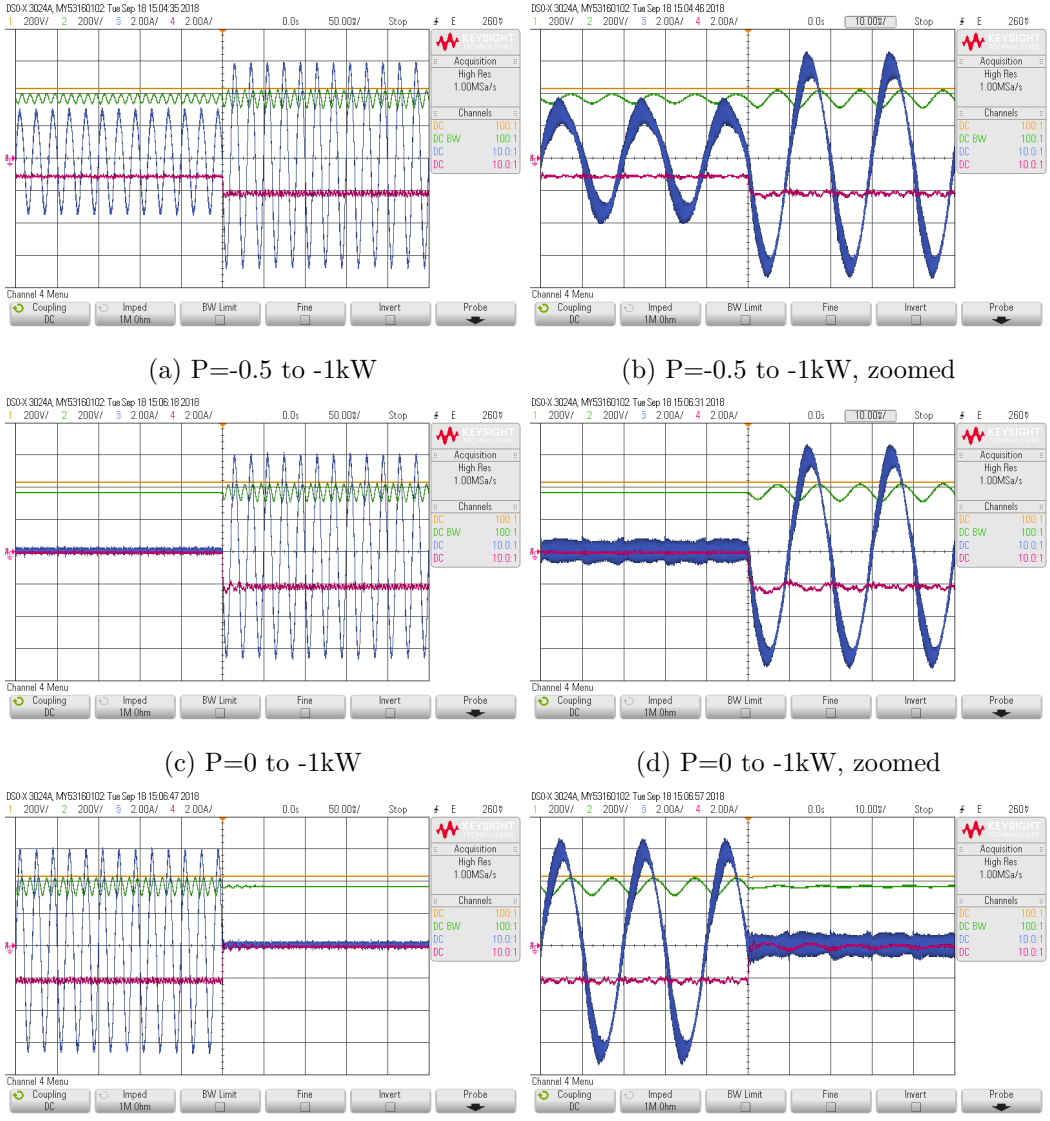
(c) P=0 to 1kW

(d) P=0 to 1kW, zoomed

(e) P=1kW to 0

(f) P=1kW to 0, zoomed

Figure 9.8: DFBC, transient, positive power: V_{DC} (yellow, 200V/div), V_C (green, 200V/div), I_{AC} (blue, 2A/div), I_{DC} (red, 2A/div)



(a) P=-0.5 to -1kW

(b) P=-0.5 to -1kW, zoomed

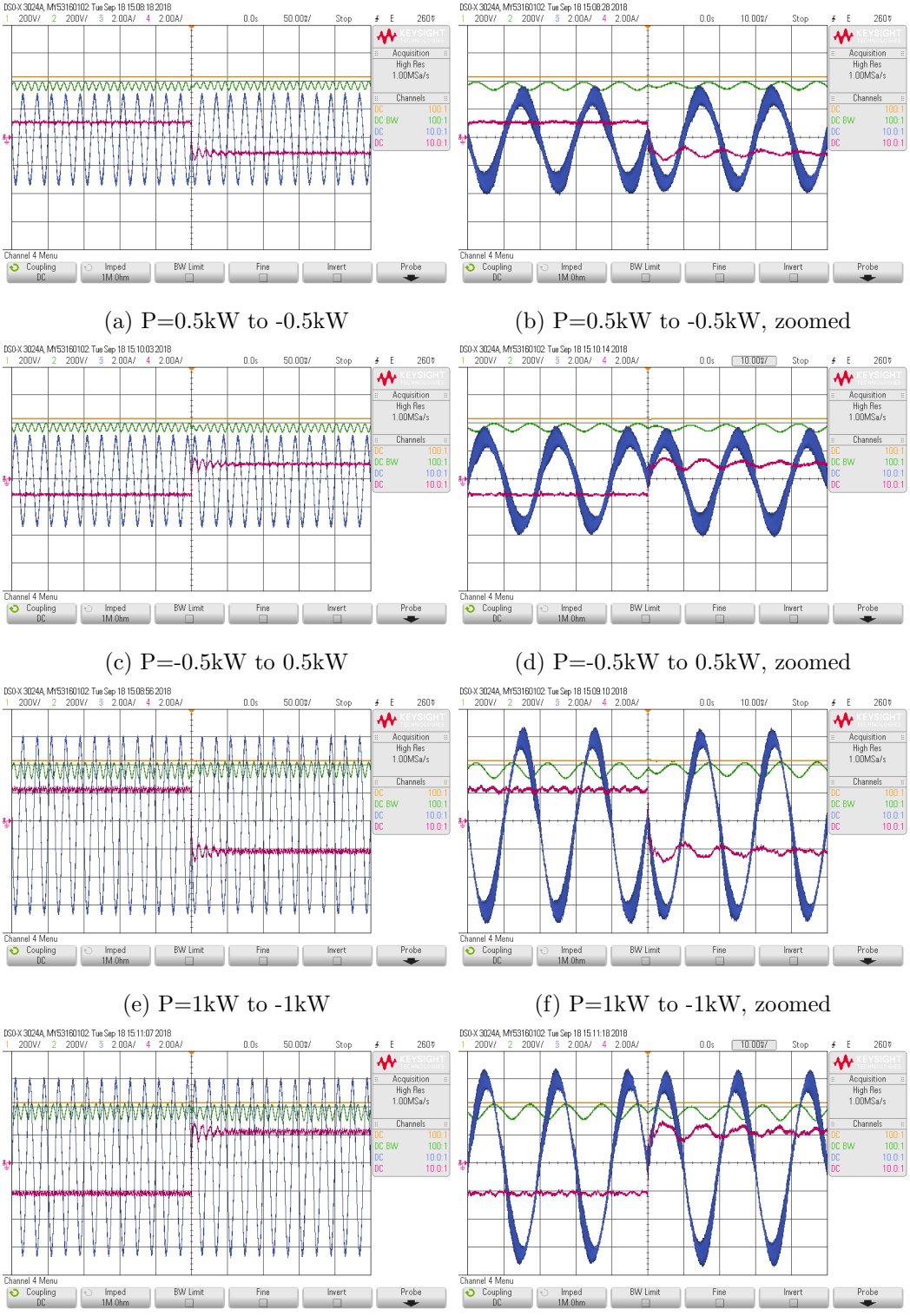
(c) P=0 to -1kW

(d) P=0 to -1kW, zoomed

(e) P=-1kW to 0

(f) P=-1kW to 0, zoomed

Figure 9.9: DFBC, transient, negative power: V_{DC} (yellow, 200V/div), V_C (green, 200V/div), I_{AC} (blue, 2A/div), I_{DC} (red, 2A/div)



(a) P=0.5kW to -0.5kW

(b) P=0.5kW to -0.5kW, zoomed

(c) P=-0.5kW to 0.5kW

(d) P=-0.5kW to 0.5kW, zoomed

(e) P=1kW to -1kW

(f) P=1kW to -1kW, zoomed

(g) P=-1kW to 1kW

(h) P=-1kW to 1kW, zoomed

Figure 9.10: DFBC, transient, power inversion: V_{DC} (yellow, 200V/div), V_C (green, 200V/div), I_{AC} (blue, 2A/div), I_{DC} (red, 2A/div)

9.3 JCC prototype

In this section, the experimental results for the JCC are described.

As for the DFBC, a prototype of the JCC topology was built using the same experimental setup. Four half bridge modules were used, two for the high frequency half bridges and two for the low frequency switches. In the same way as the DFBC topology, the prototype makes use of wide band-gap devices SiC MOSFETs (C3M0120090J by Cree/Wolfspeed) for the high frequency half bridges and Si MOSFETs (IPB65R110CFD by Infineon) for the slow switches.

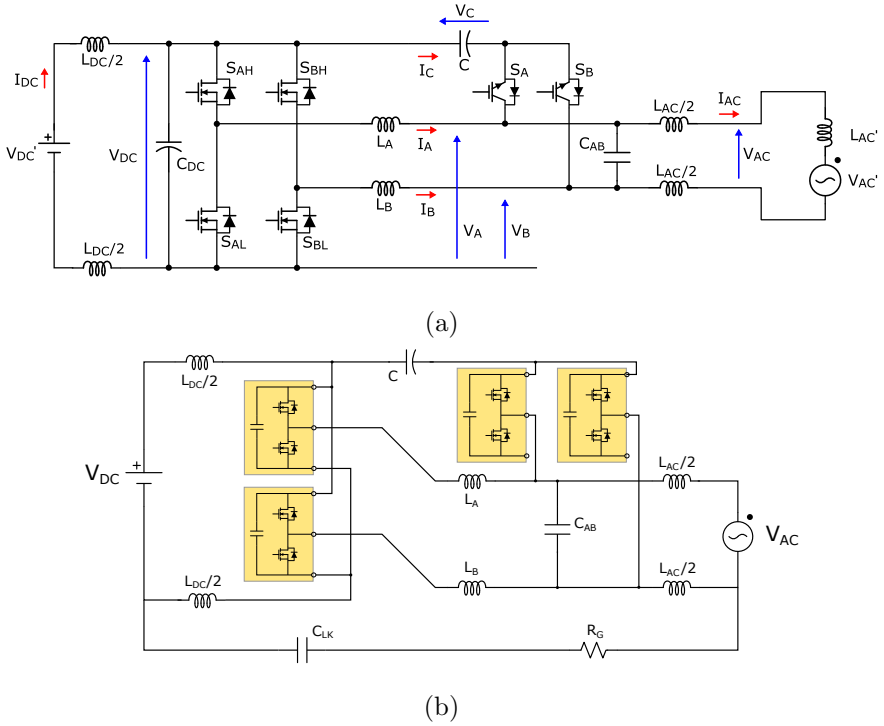


Figure 9.11: JCC implementation using the reconfigurable hardware setup

To complete the topology, the following passive components are added:

- the AC and DC inductors L_{AC}, L_{DC};
- the high frequency filtering inductors L_A and L_B;
- the power decoupling capacitor C;

In addition to that, an additional circuit constituting the path for leakage current was added. The circuit is made by a capacitor of $200nF$ and a resistor of 5Ω

connected in series, simulating the ground impedance and the stray capacitance of the PV panels.

Figure 9.11 illustrates how the four half-bridge modules, together with the other passive components, are connected to obtain the required topology. The negative terminal of the power decoupling capacitor is connected to each terminal of the capacitor C_{AB} via two half bridge modules, where only the top device is operated, wile the other is always left open.

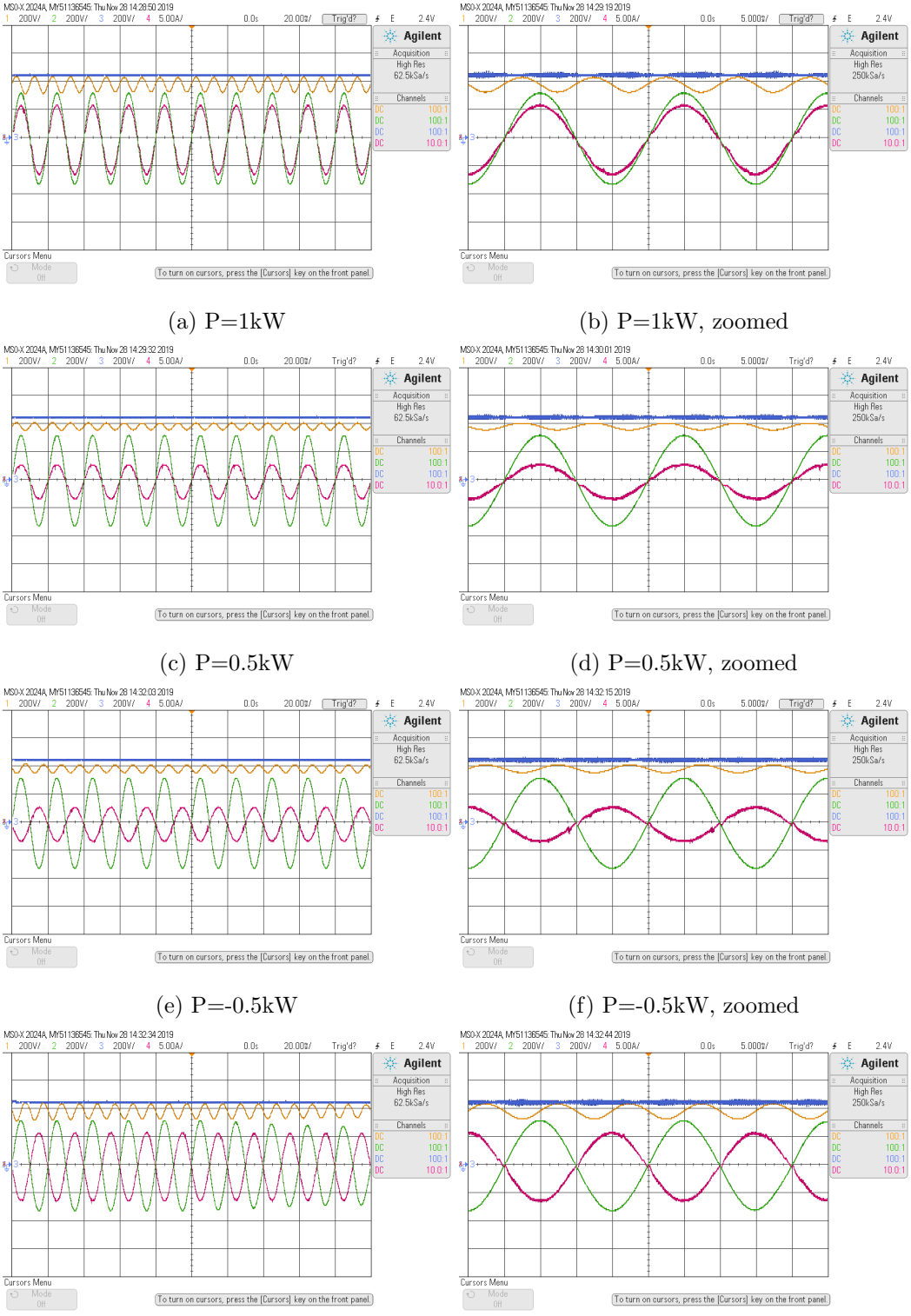
9.3.1 Experimental results: Steady-state

In this section, a series of experimental waveforms for the steady state operation of the JCC prototype at different power levels, (1, 0.5, -0.5 and -1kW) are shown.

Figures 9.12 and 9.13 show, respectively, the voltage and the current waveforms of the converter ports, where the power decoupling capacitor is intended as ripple port of the converter, as described in Chapter 3. In each case, the ripple on the capacitor voltage can be seen and shows that the power decoupling function is operating correctly. It can also be seen that the grid voltage and current are in phase for positive current and 180 out of phase for negative current.

It can be clearly seen that the power decoupling is working, since the AC current and voltage are sinusoidal while the DC voltage and current are smooth. The current waveform of the power decoupling capacitor is in good accord with the expected one, as calculated in Chapter 6.

Figure 9.14 show the current waveforms of the currents I_A and I_B. The reduction of the current peak value, due to the destructive interference between the power decoupling capacitor current and the AC current is clearly noticeable.



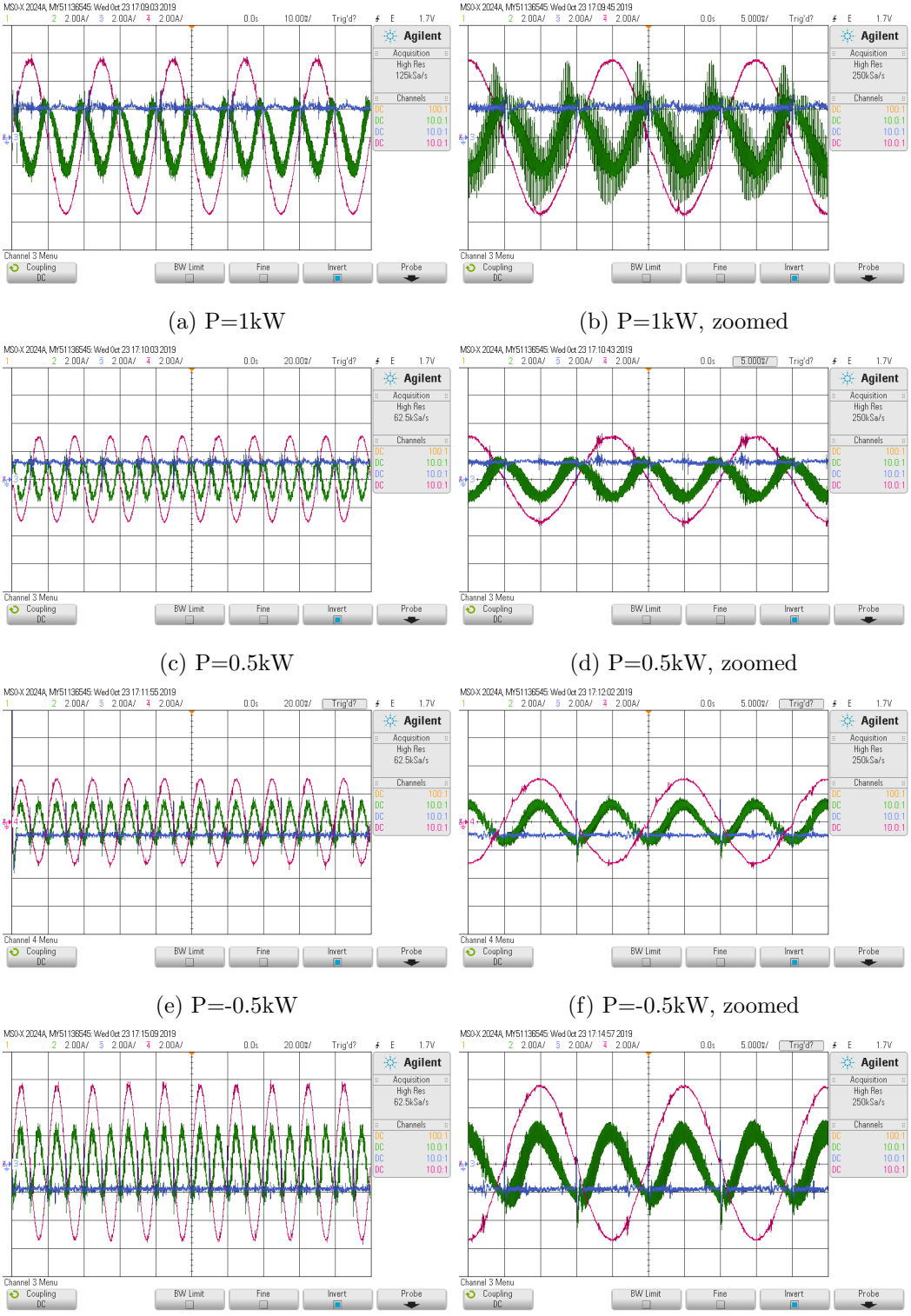
(a) P=1kW (b) P=1kW, zoomed

(c) P=0.5kW (d) P=0.5kW, zoomed

(e) P=-0.5kW (f) P=-0.5kW, zoomed

(g) P=-1kW (h) P=-1kW, zoomed

Figure 9.12: JCC, steady state voltages: V_C (yellow, 200V/div), V_{AC} (green, 200V/div), V_{DC} (blue, 200V/div), I_{AC} (red, 5A/div)



(a) P=1kW (b) P=1kW, zoomed

(c) P=0.5kW (d) P=0.5kW, zoomed

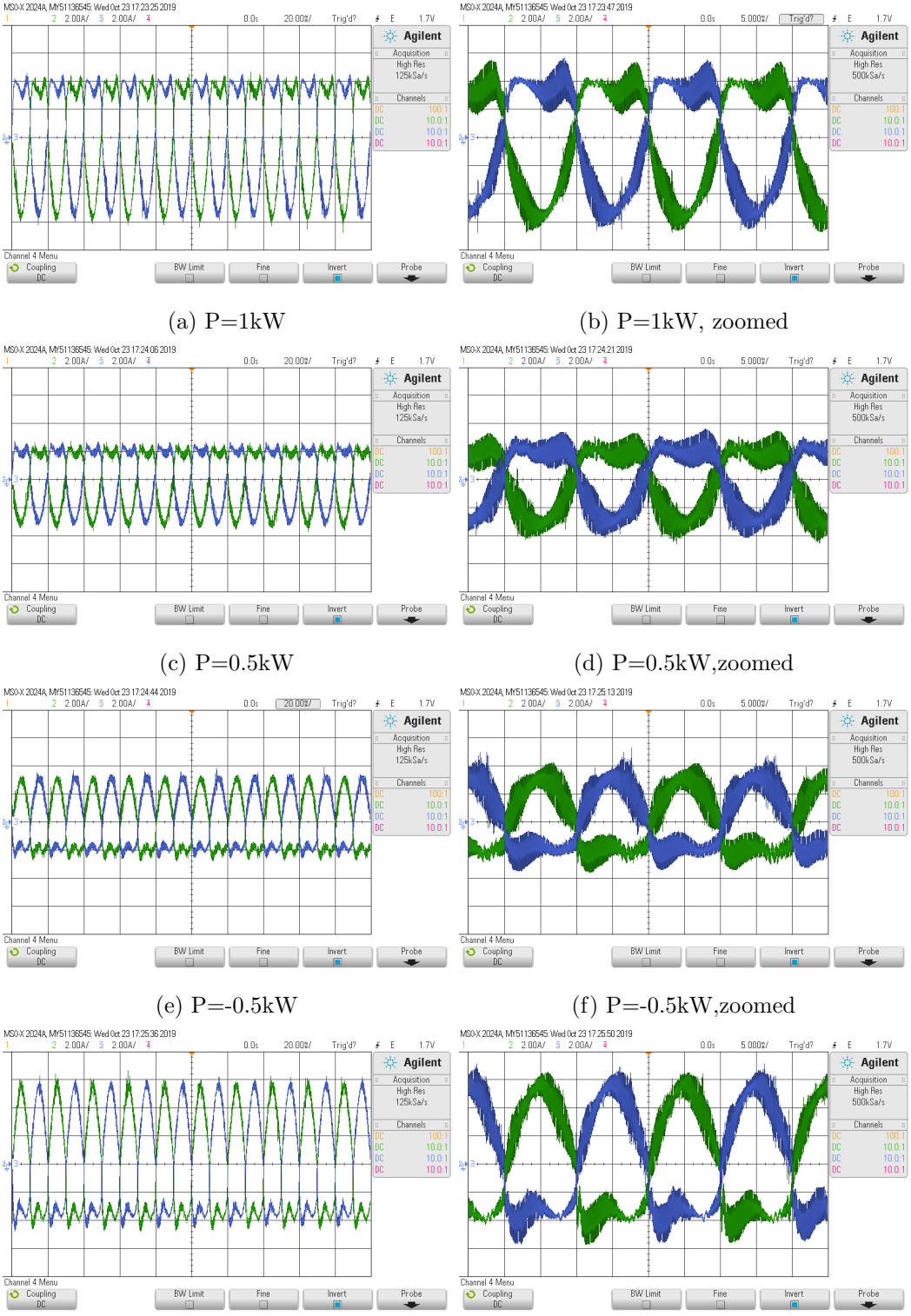
(e) P=-0.5kW (f) P=-0.5kW, zoomed

(g) P=-1kW (h) P=-1kW, zoomed

Figure 9.13: JCC, steady state currents: I_C (green , 2A/div), I_{DC} (blue , 2A/div), I_{AC} (red , 2A/div)

9.3.2 Experimental results: Transient

In order to assess the correct behaviour of the control system during transients, several step changes of the reference power were applied.



(a) P=1kW (b) P=1kW, zoomed

(c) P=0.5kW (d) P=0.5kW,zoomed

(e) P=-0.5kW (f) P=-0.5kW,zoomed

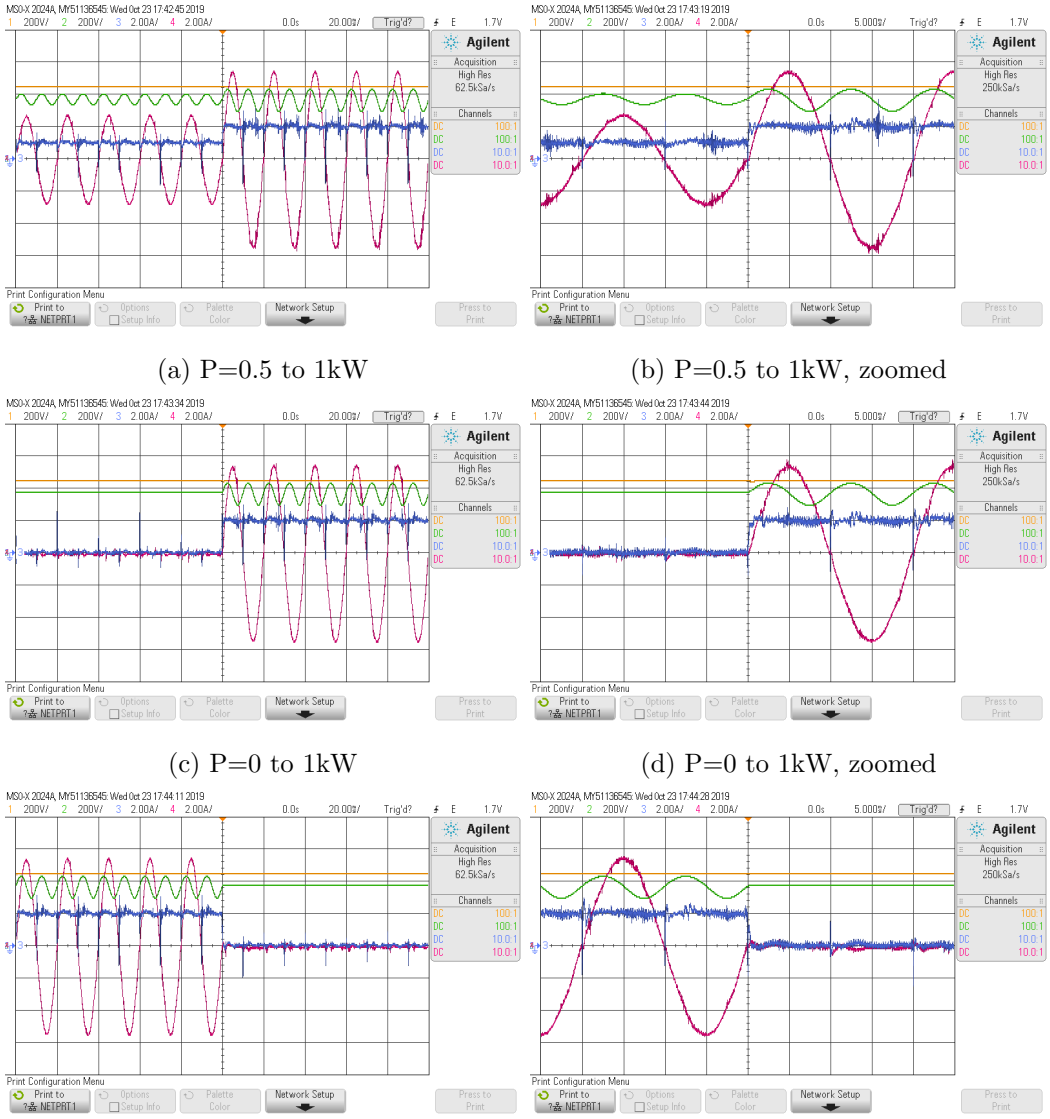
(g) P=-1kW (h) P=-1kW

Figure 9.14: JCC, steady state currents: I_A (blue , 2A/div), I_B (green , 2A/div)

In the scenarios shown in figure 9.15, the reference power is always positive, that is, power is injected from the DC source to the grid; in Fig.9.16 negative, while in Fig.9.17 a power inversion is applied.

In each figure are included the waveforms of the DC voltage, power decoupling capacitor voltage, and AC current and voltage.

The results show that the control system of the converter is able to deal with a significant step in the reference power, without hitting the voltage constraints of the power decoupling capacitor and without significant distortion on the AC and DC currents.



(a) P=0.5 to 1kW

(b) P=0.5 to 1kW, zoomed

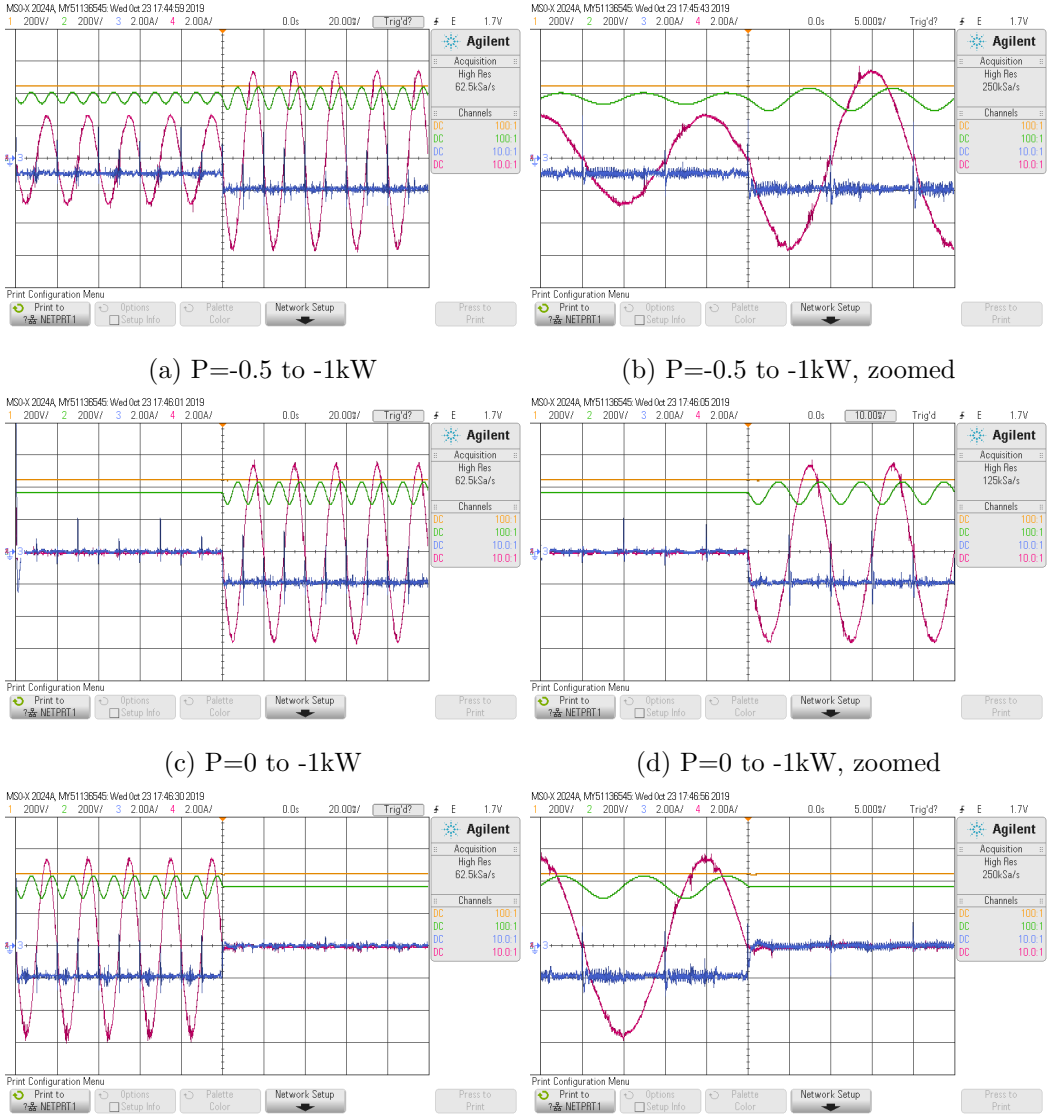
(c) P=0 to 1kW

(d) P=0 to 1kW, zoomed

(e) P=1kW to 0

(f) P=1kW to 0, zoomed

Figure 9.15: JCC, transient, positive power: V_{DC} (yellow, 200V/div), V_C (green, 200V/div), I_{AC} (blue, 2A/div), I_{DC} (red, 2A/div)



(a) P=-0.5 to -1kW

(b) P=-0.5 to -1kW, zoomed

(c) P=0 to -1kW

(d) P=0 to -1kW, zoomed

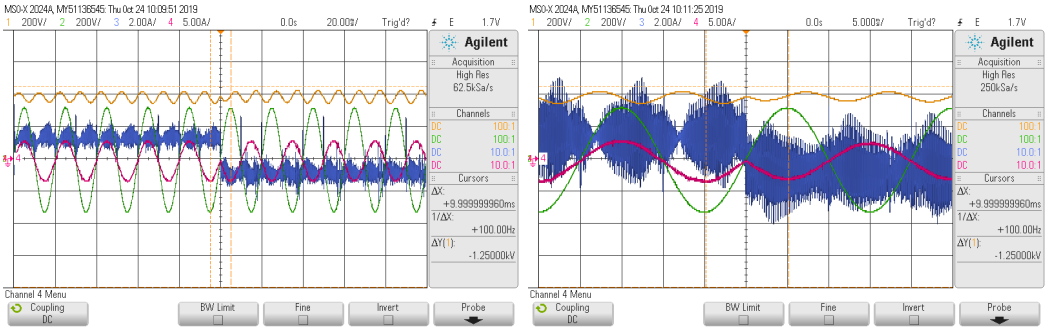
(e) P=-1kW to 0

(f) P=-1kW to 0, zoomed

Figure 9.16: JCC, transient, negative power: V_{DC} (yellow, 200V/div), V_C (green, 200V/div), I_{AC} (blue, 2A/div), I_{DC} (red, 2A/div)

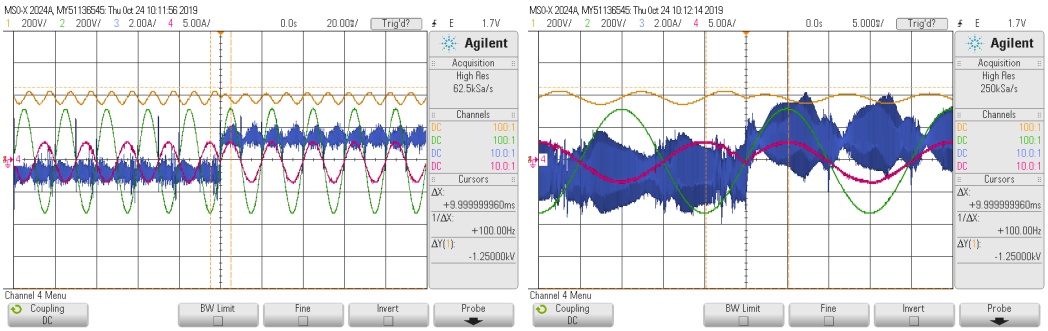
9.3.3 Experimental results: Leakage current

As can be seen from the waveform shown in fig.9.18, the leakage voltage V_{LK} has a very small ripple at switching frequency, resulting in small leakage currents without the need for additional filtering, although additional small leakage filters might be needed depending on the norms. The peak-to-peak amplitude of the common mode current is about 40mA, with a measured RMS of 34mA.



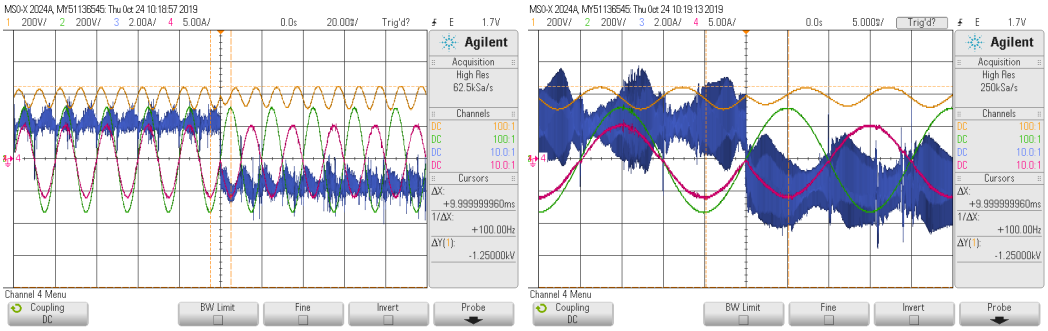
(a) P=0.5kW to -0.5kW

(b) P=0.5kW to -0.5kW, zoomed



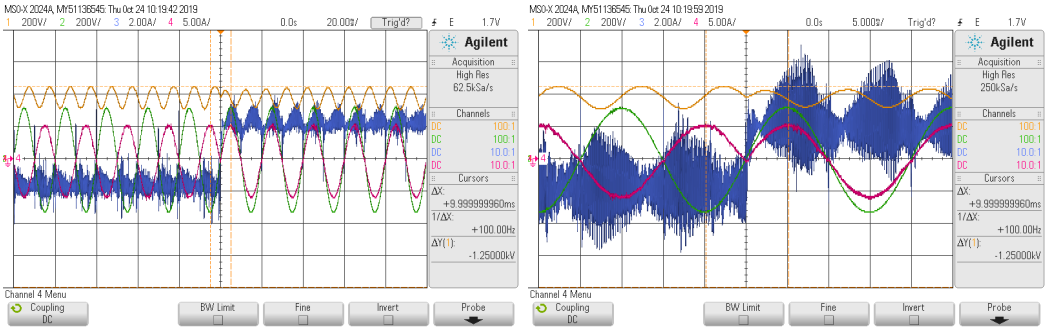
(c) P=-0.5kW to 0.5kW

(d) P=-0.5kW to 0.5kW, zoomed



(e) P=1kW to -1kW

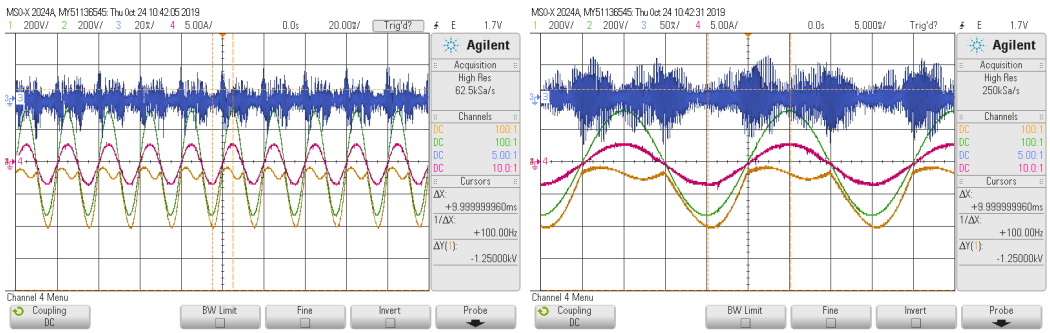
(f) P=1kW to -1kW, zoomed



(g) P=-1kW to 1kW

(h) P=-1kW to 1kW, zoomed

Figure 9.17: JCC, transient, power inversion: V_{DC} (yellow, 200V/div), V_C (green, 200V/div), I_{AC} (blue, 2A/div), I_{DC} (red, 2A/div)



(a) Leakage current (b) Leakage current, zoomed

Figure 9.18: JCC, Leakage current: V_{LK} (yellow, 200V/div), V_{AC} (green, 200V/div), I_{LK} (blue, 20mA/div), I_{AC} (red, 5A/div)

9.4 SeTCM on JCC

In the current section, the experimental results concerning the application the SeTCM modulation in the JCC topology, as described in Chapter 8, are presented.

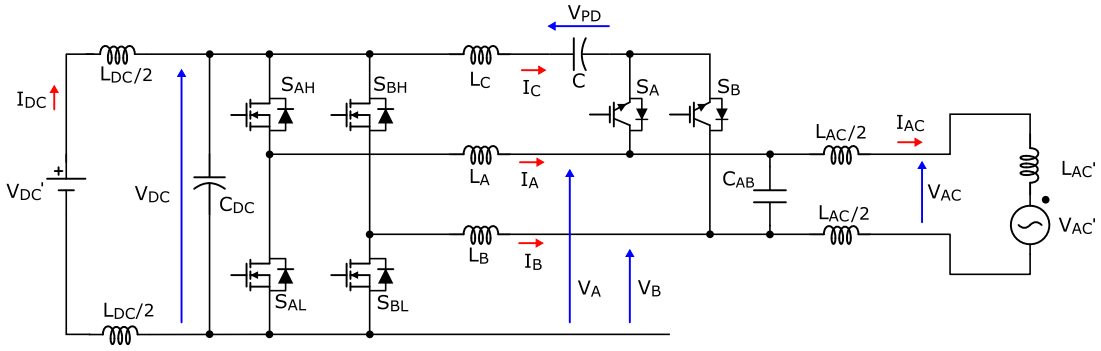


Figure 9.19: JCC modified for eTCM

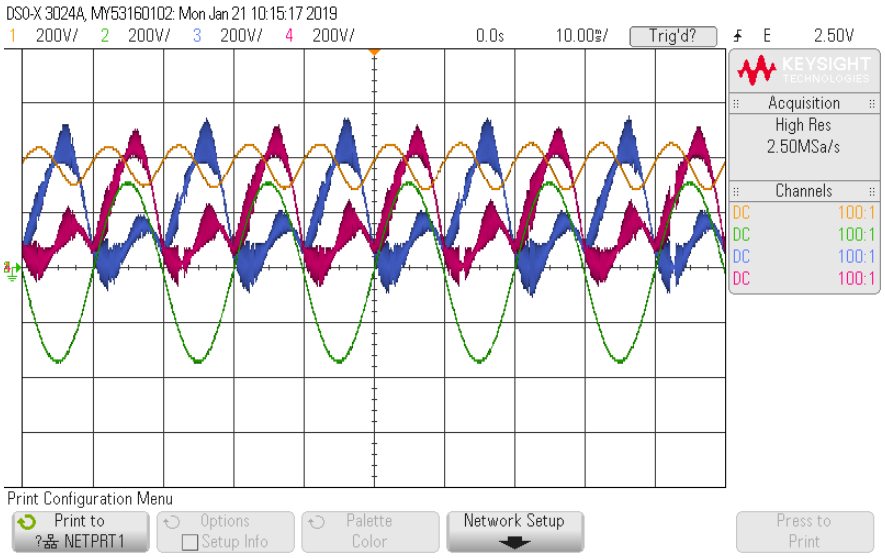
The hardware setup used is the same as the one described in the previous section, with the modifications discussed in Chapter 8. In order to apply the variable frequency SeTCM to the topology, inductor L_C was added, and L_A and L_B replaced so that their value corresponds to the one calculated in the SeTCM magnetic design. In addition to that, bigger inductors were used for the AC and DC filters, in order to deal with the additional common mode voltage inherent in the choice of the magnetic structure. The other components were reused, the only additional modification being the software programmed on the DSP.

9.4.1 Experimental results: Steady state

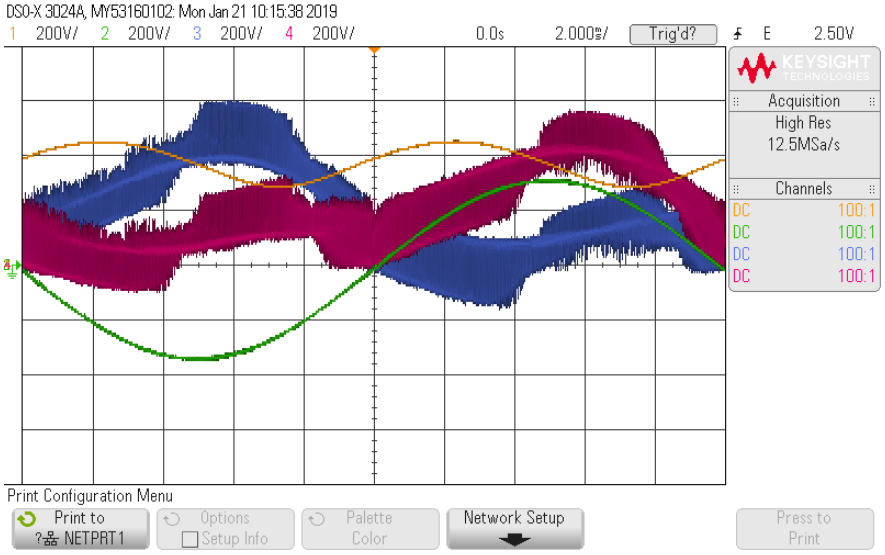
In contrast with the experimental results taken in the previous section, the aim of the following results is not to assess the low frequency component of voltage and currents, but on their switching frequency ripple component, influenced by the SeTCM modulation. For this reason, only one operating point of the converter is considered, that is a reference power set to 1kW, corresponding to the nominal power of the converter.

The steady state voltages defined in Fig.9.19, which are the power decoupling capacitor voltage, the AC port voltage, and the voltages V_A and V_B, are shown in Fig.9.20. In contrast with the implementation of the topology shown in the previous section, a significant high frequency voltage ripple appears on both the modulated voltages. This voltage ripple corresponds to the voltage applied to the inductor L_C.

Fig.9.21 shows the steady state current waveform of the AC and DC port, and the currents I_A and I_B. The experimental current waveforms are in good accord with the expected ones, as described in the previous chapter.



(a)



(b)

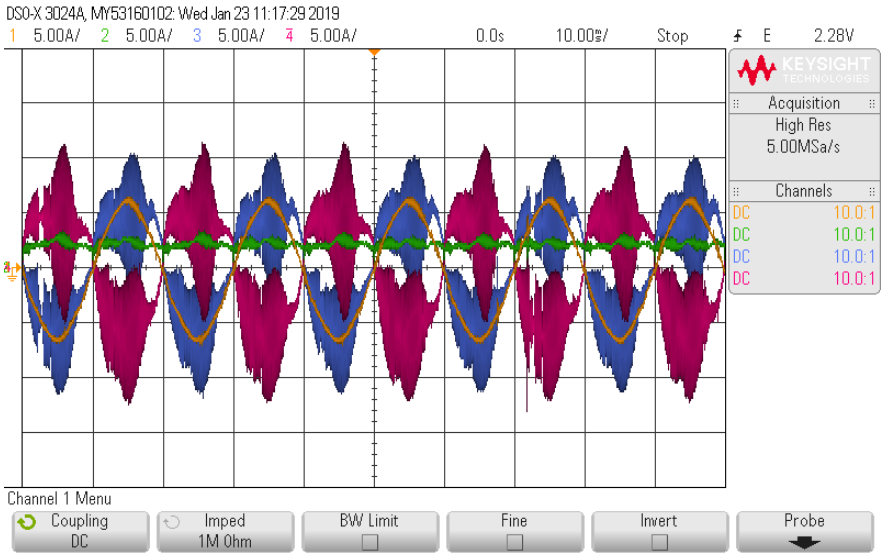
Figure 9.20: SeTCM on JCC: Voltages waveform - V_{PD} (yellow, 200V/div), V_{AC} (green, 200V/div), V_A (blue, 200V/div), V_B (red, 200V/div)

9.4.2 Experimental results: Zero Voltage Switching

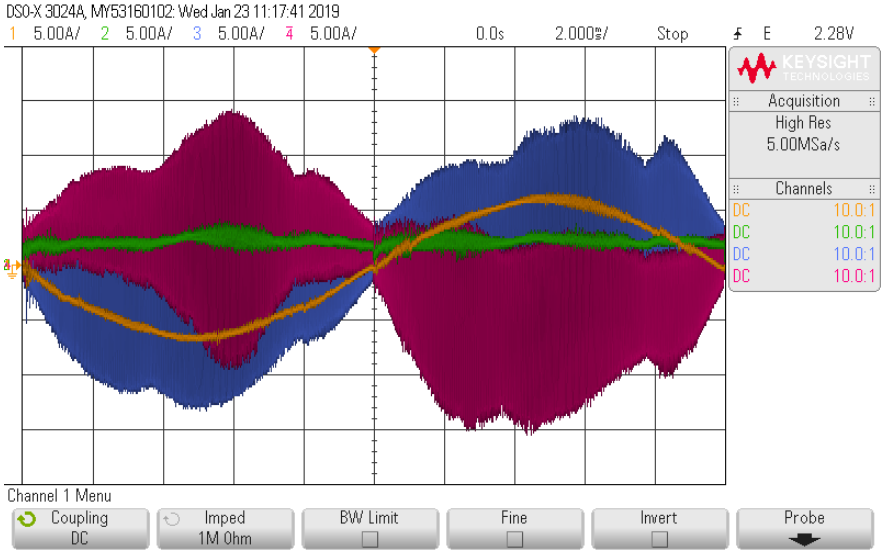
In figures 9.22, 9.23 and 9.24, the waveforms of the voltage modulated by the two half bridges are shown, together with the currents I_A and I_B.

The time axis is magnified in the scope screenshots shown in Fig.9.22 and 9.23 in order to verify the correct inversion of sign of the current prior to the switching, required for ZVS.

Fig.9.24 shows the voltage waveforms measured in the midpoint of the two



(a)



(b)

Figure 9.21: SeTCM on JCC: Currents waveform - I_{AC} (yellow, 5A/div), I_{DC} (green, 5A/div), I_A (blue, 5A/div), I_B (red, 5A/div)

half bridges formed respectively by S_{AH}, S_{AL} and S_{BH}, S_{BL}, and the currents I_A and I_B. The slow dV/dt of the switching typical of ZVS is identifiable. The readings of the currents are heavily affected by switching noise, probably due to the use of hall effect probes instead of Rogowsky coils. The use of Rogowsky coils was avoided, since an accurate reading of the DC component of the current is necessary for ensuring the change of sign.

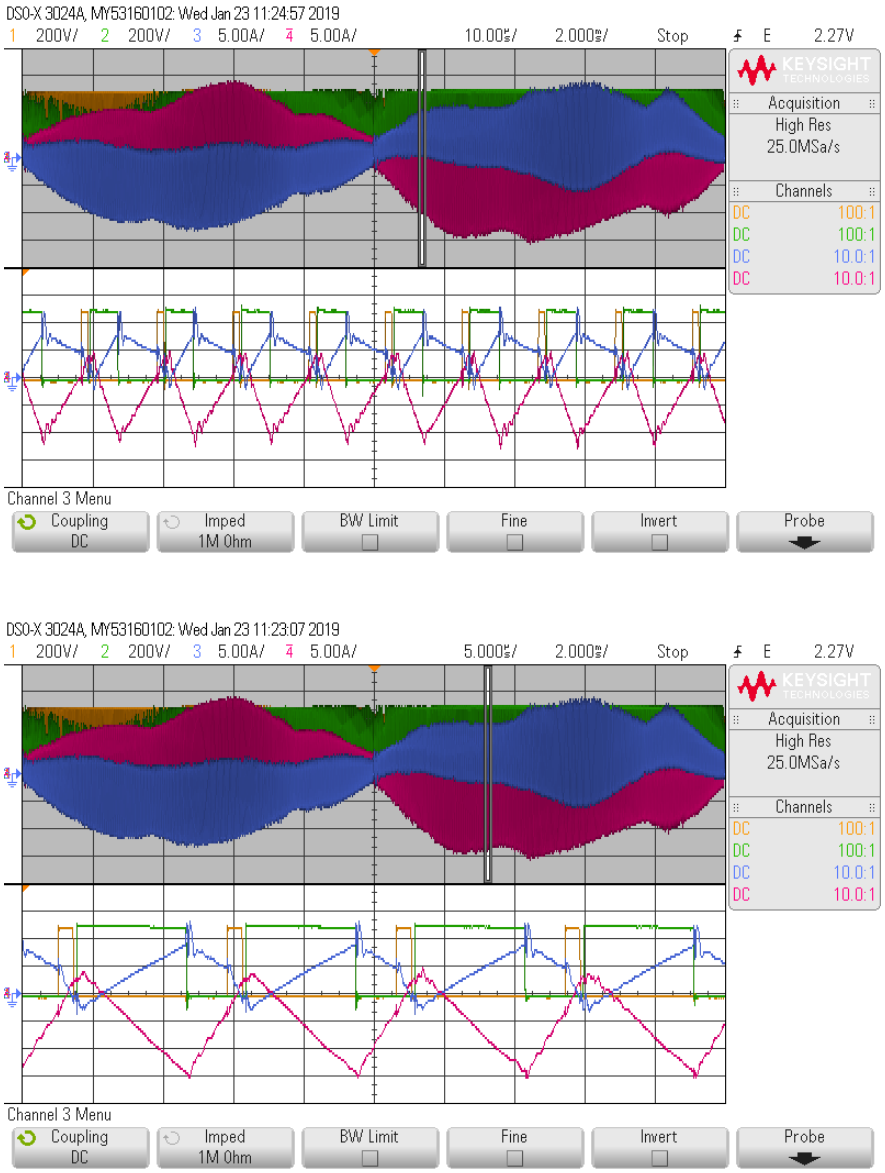


Figure 9.22: SeTCM on JCC: Voltages waveform, zoomed - V_A (yellow, 200V/div), V_B (green, 200V/div), I_A (blue, 5A/div), I_B (red, 5A/div)

9.4.3 Experimental results: Transient

In order to test the control algorithm a load transient from no power to 1kW injected in the grid was executed. The results are shown in Fig.9.25, where the DC and AC port currents, the DC link voltage and the power decoupling capacitor voltage waveforms are shown. As expected, the behaviour of the control structure is significantly worse than the one of the original topology presented in Chapter 6, as can be seen by the higher ripple in both the DC and the AC current, however the controller is stable and the converter operates as expected. The additional

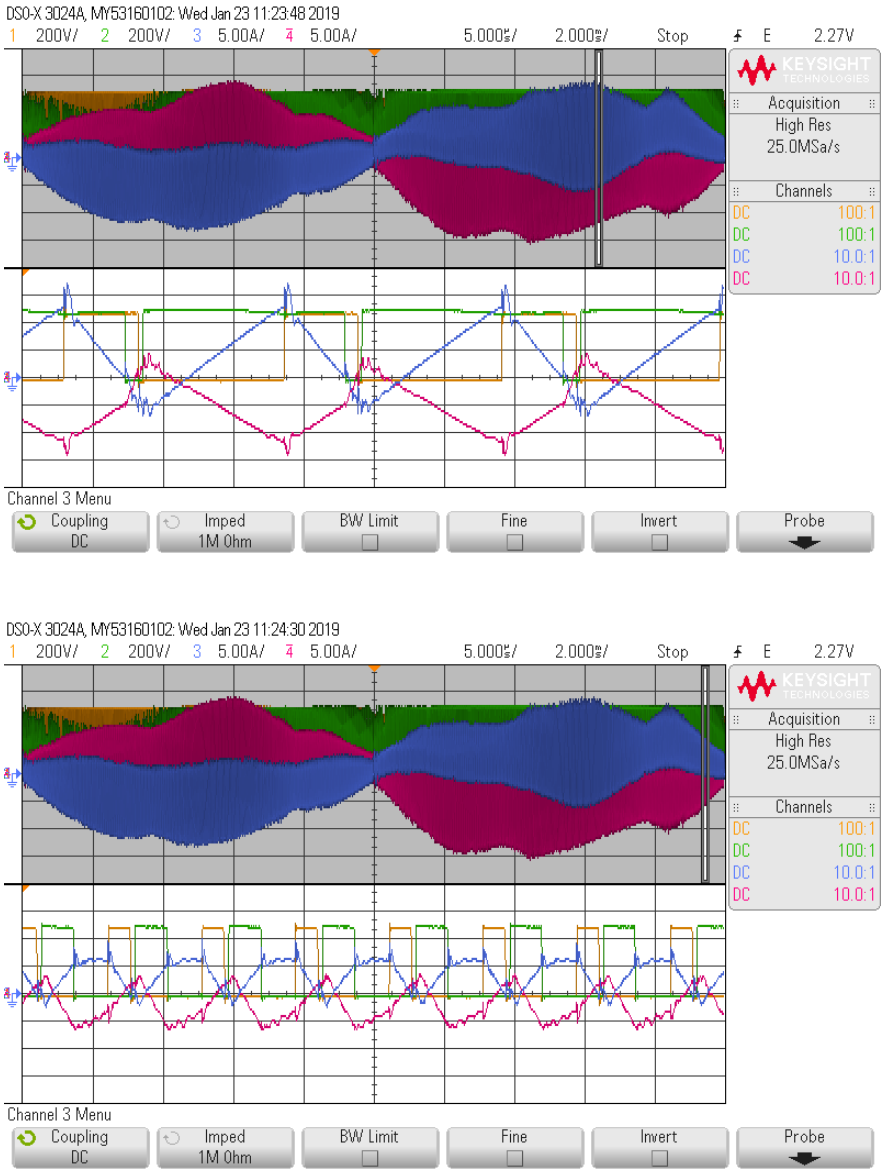


Figure 9.23: SeTCM on JCC: Currents waveform, zoomed (cont.) - V_A (yellow, 200V/-div), V_B (green, 200V/div), I_A (blue, 5A/div), I_B (red, 5A/div)

ripple on the currents can be explained by the higher common mode noise applied to the AC terminals, due to the voltage ripple shown in Fig.9.20.

9.4.4 Experimental results: Efficiency

The measured efficiency amounts to 93.3% at nominal power and 90.5 at half load. The lower efficiency is likely to be the cause of the inductors operating close to the saturation region, resulting in losses that are higher than the turn-on

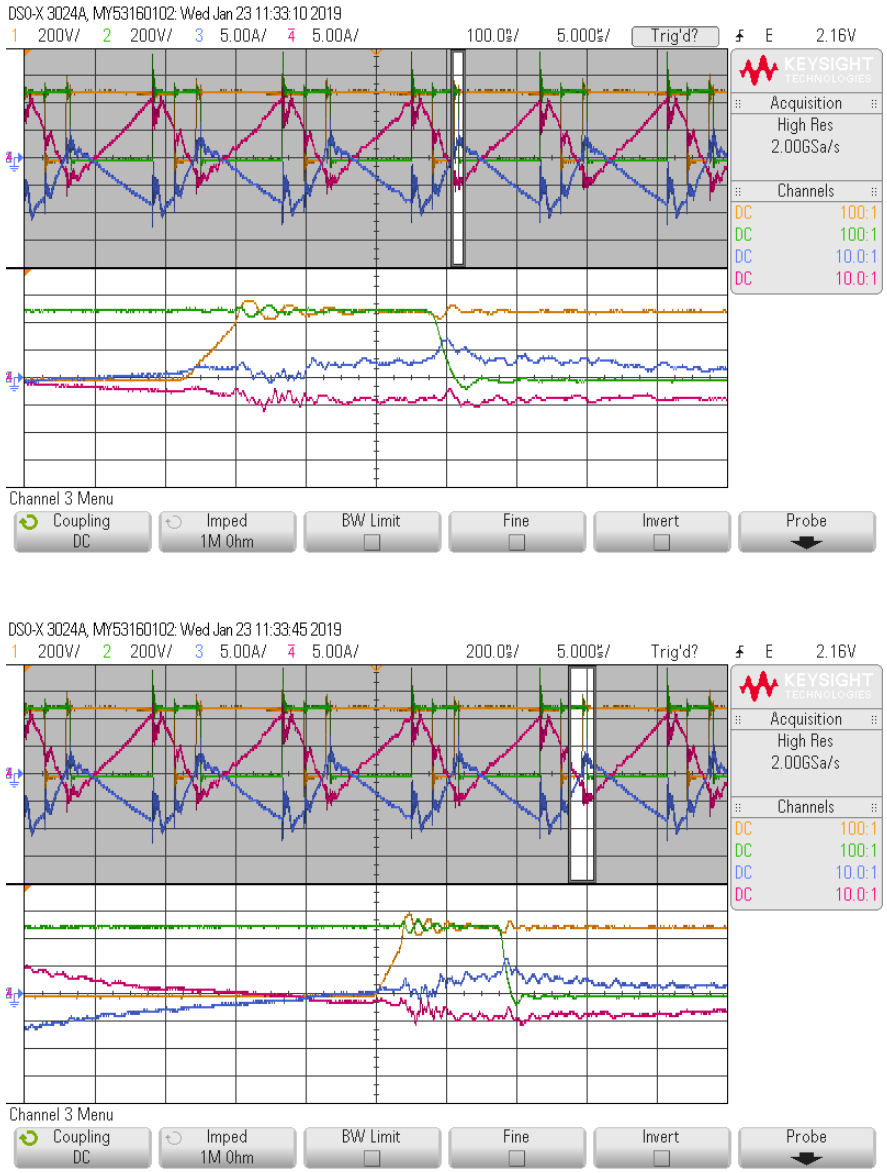


Figure 9.24: SeTCM on JCC: ZVS - V_A (yellow, 200V/div), V_B (green, 200V/div), I_A (blue, 5A/div), I_B (red, 5A/div)

losses of the active devices, that are removed.

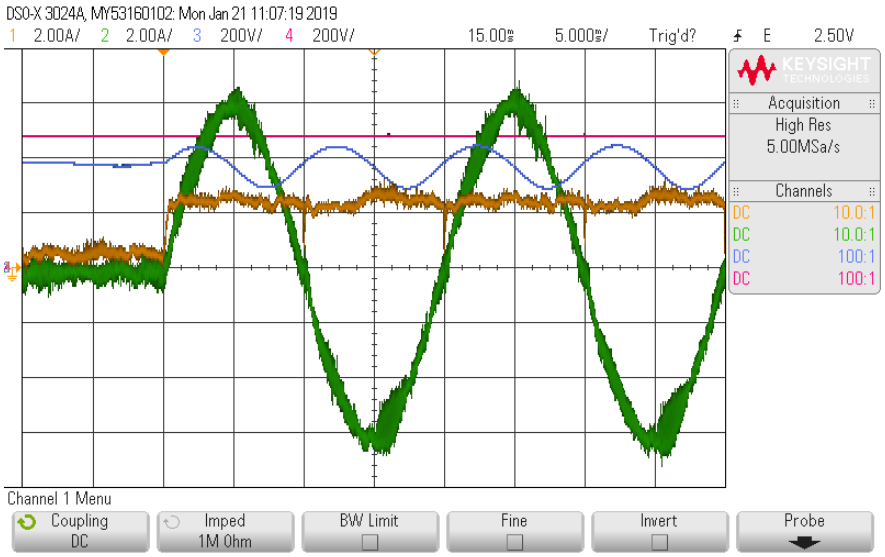


Figure 9.25: SeTCM on JCC: Transient behaviour - I_{DC} (yellow, 2A/div), I_{AC} (green, 2A/div), V_{PD} (blue, 200V/div), V_{DC} (red, 5A/div)

9.5 Conclusions

In this Chapter, the physical setup used to obtain experimental data is described, following with the exposition of the results relative to the DFBC and JCC topologies, and the implementation of SeTCM on the JCC.

Being the setup reconfigurable, the same hardware was used in all the experiments. The way in which the half-bridge modules are connected to obtain the required topologies is described.

Both the steady-state behaviour at various load point and several transients are shown, proving the power decoupling capability of the topologies and the good performances of the control system.

In case of the SeTCM, several zoomed-in voltage and current waveforms were captured, in order to assess the ZVS switching condition. Based on the results, it appears that the SeTCM modulation is able to achieve ZVS across the entire grid period, as claimed.

Chapter 10

Conclusions

This research project focused on the analysis of the state of the art of single phase grid-connected converters, specifically addressing those used in energy storage systems and photovoltaic systems; with the aim of developing novel converter topologies having improved efficiency, smaller size and/or minor costs.

One of the main reliability issues in single phase converters arises from the use of electrolytic capacitors, as energy buffer, to compensate for the power pulsation, which is present in single phase connections. Electrolytic capacitor have well known reliability problems due to ageing, which make their use problematic, especially in PV systems, that have a life expectancy of up to 20 years. In order to overcome this problem, film capacitors can be used; however, film capacitor are, for the same capacitance and nominal voltage, more expensive and exhibit a much lower energy density. For this reason, it is common practice to make use of auxiliary circuits able to control the voltage applied to the power decoupling capacitor, instead of connecting it to the DC link. This solution makes possible to use a much smaller capacitance, with the disadvantage of reducing the efficiency and increasing costs.

Passive components are used as filters to interface the converter with its AC and DC electrical port. The size of the required passive components is chiefly determined by the switching frequency, decreasing as the switching frequency increase. Increasing switching frequency, however, comes with the disadvantage

of higher losses in the magnetic components, due to increased losses in the core and in the winding, and in the switches themselves. To reduce losses on the active devices, wide-band gap devices can be used, in conjunction with soft switching techniques.

In case of PV systems, the stray capacitance in the panels generates a ground loop for common-mode currents to flow through. This is an issue for transformerless converters, that in general require additional common mode filters to comply with the quality standards for grid connection.

Following the analysis of the main issues concerning singe phase converters, two new topologies, the Double Full Bridge Converter (DFBC) and the Jumping Capacitor Converter (JCC), were introduced. Both topologies address the problem of active power decoupling, where the power decoupling section is operated by the same full bridge that controls grid current. Film capacitors can thus be used, without negative effects on the overall efficiency of the converter.

Both the DFBC and the JCC are based on the concept of destructive interference exposed in Chapter 3, where the rectified grid current and the power decoupling capacitor current are added achieving lower RMS and peak value. In DFBC this is obtained by rectifying the grid current via a rectifier/unfolder bridge operating at grid frequency, while in JCC it is obtained by alternatively connecting the power decoupling capacitor to the legs of the full bridge that drives grid current by the use of two additional devices.

An analysis of the leakage current was applied on the JCC. It is shown that, due to the characteristics of the topology, leakage currents are small even without the use of an additional common mode filter.

In order to validate the proposed topologies, a multipurpose reconfigurable test rig was build. The rig is composed of six galvanically isolated half-bridge modules, and a control board hosting current and voltage sensors and a microcontroller.

The two proposed topologies were compared with existing state of the art solutions, and proved to be competitive, in terms of high DC utilization ratio

and good energy utilization of the power decoupling capacitor.

In order to extend the ZVS operating region of the proposed topologies, a new current mode, the extended Triangular Current mode, was introduced. While this current mode can be applied to the proposed topologies, it is formulated in a general way, and can be applied (with some minor modifications) to any topology. A design algorithm for the sizing of the magnetic components, associated with the use of eTCM, is proposed.

By adding additional degrees of freedom on the frequency and phase shift of the modulated PWM waveforms, and adding a mutual coupling between the filtering inductors of the fundamental cells that has an influence on the control, the implementation of eTCM poses additional challenges to the control of the topologies on which it is applied. To mitigate the challenge, the Simplified extended Triangular Current Mode (SeTCM) was introduced. This modulation has the advantage of limiting the degrees of freedom that can be controlled to the switching frequency alone, while the phase shift can be directly implemented in the modulator, at the cost of reduced performances if compared with eTCM.

The application of the SeTCM on the JCC is described, with a focus on the magnetic design, and its consequence on the control of the converter. The control was successfully implemented in the microcontroller, programmed in C. Using SeTCM, ZVS is achieved on all the active switches during the entire AC grid period, for every operating point of the converter.

In order to control the switching frequency for SeTCM, a look-up table was used, where a different PWM period is used according to the instant in the grid period. A similar approach can be used if eTCM is chosen, with the addition of another lookup table to set the variable phase shift, however, in case of eTCM the experimental validation was not taken forward, hence, a detailed description of the control for eTCM is not included in this work.

In conclusion, the proposed topologies and modulation techniques are aimed to the development of better single phase AC-DC converters, in terms of reduced size of the passive components and improved reliability thanks to the active ripple

decoupling, better efficiency thanks to the destructive interference, and lower EMI thanks to leakage current rejection and/or ZVS operation.

10.1 Achievements

The main achievements of this PhD project can be summarized as follow:

- Introduction of two novel topologies the Double Full Bridge Converter (DFBC) and the Jumping Capacitor Converter (JCC).
- Description of the design procedure and control method for both topologies.
- Introduction of a novel current mode, named extended Triangular Current Mode (eTCM).
- Development of a design method of the magnetic components used for eTCM.
- Implementation of the SeTCM control in a microcontroller.

10.2 Future work

As a further development of this research, the following points are identified as promising for future work:

- The hardware tests on both topologies were applied on a multi-purpose rig, constituted by galvanically isolated half bridge modules. Better performances in terms of higher efficiency are likely to be obtained if a dedicated prototype is developed for each topology.
- The eTCM sizing algorithm is able to completely reconstruct the current waveform, both in its low frequency and high frequency ripple components. With this information, it is possible to calculate not only the RMS and peak value of the current, but also a detailed estimation of the losses, in both the magnetics and the active devices, including switching losses. It is

thus possible to find the optimum switching frequency and phase shift that result in the maximum overall efficiency of the converter.

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