

PhD Thesis

Open Circuit Fault Detection and Diagnosis on Matrix Converter Systems

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Abstract

Matrix converters have received continued research attention as a result of their possibility of higher power density, controllable input power factor, and removal of DC-Link component. However due to the numerous semiconductor power switches used in such circuits there is a high possibility of switch failures.

This thesis considers both the direct matrix converter (DMC) topology and the indirect matrix converter (IMC) topology. The DMC and IMC system behaviour under an open circuit switch fault condition is investigated and given in detail with the aim of contributing more expert knowledge to a fault diagnosis method for a DMC or IMC system. The expert knowledge can effectively avoid false diagnosis in DMC and IMC systems. Several expert-knowledge-based fault diagnosis methods are developed in this thesis to diagnose open circuit switch faults in DMC system and IMC system with finite-control-set model-predictive-control (FCS-MPC) strategy or space vector modulation (SVM) strategy. An experimental prototype of the DMC has been built to validate the proposed fault diagnosis methods.

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Chapter 1

Introduction

1.1 Motivation

The matrix converter (MC) topology can realize direct AC to AC power conversion with minimal requirements for passive components [2]. It comprises of a matrix of bidirectional switches which connect the output lines direct to the input lines. The MC topology has advantages such as a compact power circuit, the possibility of higher power density [3], controllable input power factor [4, 5], and removal of DC-Link component [6]. Without the bulky DC-Link component, the MC topology is an alternative to the traditional back-to-back PWM converter topology in volume and weight critical applications such as aerospace. The size of the inductance-capacitance input filter of the MCs needs to be properly designed to maximize the power density. However, removal of the DC-Link components also means that any power pulsations at the MC output will also be present at the MC input. Therefore, the MC topology is more suited to constant power loads application than to pulsed loads applications [2]. The MC topology is very suitable for applications such as induction machines and permanent-magnet synchronous machines sinusoidal motor drives.

It has been shown that 21% of the failures of the voltage sourced converters are caused by semiconductor faults[1]. Another industry survey claims

that the failure of the power devices counts for 38% of the total faults in the variable speed AC drives[7]. Since the MC topology is composed of semiconductor switches and has no DC-Link components in the power circuit, so the reliability of the semiconductor switches is a big concern for the application of the matrix converter. Usually, there are three ways to improve the reliability of a power electronic system. These three ways are prognosis, condition monitoring, and diagnosis respectively. The prognosis assesses the current health level of a component, and predicts the health of the component at some point in the future [8]. The prognosis is a very challenging task because it needs good failure modeling of the components. Condition monitoring is used to measure the condition of a component in real-time, and appropriate action will be taken if it drifts away from the healthy condition. The condition monitoring technique requires sensing and signal processing techniques as well as knowledge of power device failure mechanisms, which will increase the hardware complexity and cost. The diagnosis is to identify the root cause of a fault, given that a fault has occurred. Diagnosis techniques are still a cost-effective way to improve power electronic system reliability because it requires less or even no additional hardware complexity compared to condition monitoring techniques.

It is inevitable that a fault may occur during the matrix converter (MC) system lifetime. A semiconductor switch can either fail to an short circuit fault or an open circuit fault. Most of the short circuit switch fault detection and diagnosis methods are hardware circuit based rather than software based. This is because the time interval between the fault initiation and failure is too small to implement a software based detection method [9]. When an open circuit switch fault occurs, the MC may not suffer catastrophic failure. However, if the open circuit switch fault can not be detected, diagnosed, and isolated in time, accumulated over-voltage stress on the power switches will cause further damage to the MC system. This thesis will focus on the open circuit switch faults in the MC system.

Fast and reliable fault diagnosis methods are essential to minimize any

hazard from over-voltage or over-current conditions. The fault detection and diagnosis methods in power electronics proposed in the literature can be divided into two categories: the signal processing-based [10] and the analytical model-based methods [11, 12, 13, 14, 15, 16].

In [10], a Fast Furrier Transformation (FFT) is used to analyze the spectral components in the output current, but this method cannot locate the fault to the exact bidirectional switch because the spectral components caused by each faulty device in one output phase are similar. Considering the analytical model-based fault diagnosis methods, in [11], the matrix converter output voltage is captured by three additional voltage sensors and used for fault detection purpose, which can locate the fault to a particular output phase rather than to one bidirectional switch. The work presented in [12] improves the output error voltage method by implementing nine modulated error voltages to locate the fault to one switch. In [13], a MC fault diagnosis method is proposed which relies on the reduction of the MC output currents. However, the use of output currents will slow down the fault detection process. In [14], a fault detection method based on the clamp circuit capacitor current measurement is proposed. An additional current sensor is used in this method and the fault detection process is slowed down by the integration of the clamp circuit current. [15] proposes a fault diagnosis method which relocates the three output current sensors ahead of the clamp circuit to directly measure the matrix converter output currents within three different zero vectors. However, the zero vectors duty-cycle are extremely small and hard to capture at high modulation ratios.

The motivation of this thesis is to develop open-circuit-switch fault diagnosis methods for matrix converter systems with high precision and high speed.

1.2 Contribution

Three open circuit fault diagnosis methods for MC systems are proposed and explored in the research described this thesis.

1.2.1 Open Circuit Fault Diagnosis for Direct Matrix Converters with Finite Control Set Model Predictive Control Strategies

This fault diagnosis method is for direct matrix converters (DMC) using a finite control set model predictive control (FCS-MPC) strategy. The proposed method has been validated experimentally. The three output current sensors are located ahead of the clamp circuit to measure the matrix converter output current directly. In addition, current recirculating information is contributed to the fault detection system to avoid false-diagnosis. The proposed method can locate an open-circuit switch fault in one sampling period, which significantly improves the speed and the precision of the fault detection and diagnosis progress compared with the method in [16]. In addition, the proposed fault diagnosis method is applicable within the whole range of modulation indexes, compared with the presented method in [15], which can only be applied at a low modulation index.

1.2.2 Open Circuit Fault Diagnosis for Direct Matrix Converter with Space Vector Modulation Strategies

The second proposed fault diagnosis method is for DMC using space vector modulation (SVM) strategies. The proposed method has been validated experimentally. In this method, an over-sampling technique is applied to sample the DMC output current. The current sampling frequency is 16 times higher than the SVM modulation frequency. The reason to use over-sampling technique is because there is more than one switching state change in each modulation period.

1.2.3 Open Circuit Fault Diagnosis for Indirect Matrix Converter with Finite Control Set Model Predictive Control Strategies

The third proposed is an error-voltage-based fault diagnosis method for indirect matrix converters (IMC) using a FCS-MPC strategy. If the inverter stage of the IMC occurs as an open-circuit fault, the faulty switch can be located within one sampling period by using the output error voltages and the switching state information. The error voltage is acquired by comparing the reference output voltages and the estimated output voltages. When the rectifier stage of the IMC occurs as an open-circuit fault, two additional voltage sensors will be used to measure the fictitious DC-Link voltage of the IMC. Combining the information of rectifier stage switching states and the DC-Link voltages allows the faulty switch to be identified within one sampling period.

1.3 Thesis Structure

The thesis is structured as follows.

Chapter 2 introduces the basic concepts of the matrix converter topologies, including the direct matrix converter (DMC) topology and the indirect matrix converter (IMC) topology. General operation principles of the matrix converter topologies are described mathematically to shown how the switches of the matrix converters act. The DMC topology consists of a switch matrix, an input filter and a clamp circuit. The IMC topology consists of a fictitious rectifier stage and inverter stage, an input filter and a clamp circuit. Since there are no freewheeling devices in the DMC topology, a commutation strategy is required to avoid input short circuit and output open circuit. The output-current-direction based four step commutation strategy is commonly used for the commutation process.

Chapter 3 introduces the causes of open circuit faults in matrix converter systems. Firstly, the failure mechanisms of open circuit faults in matrix converter systems are described in detail. Then a condition monitoring technique is introduced both at the device level and at the system level. Finally, the previous proposed fault detection and diagnosis methods for matrix converter systems is reviewed.

Chapter 4 introduces the SVM strategy for the direct matrix converter, and the FCS-MPC strategy on the direct and indirect matrix converter systems. The SVM algorithm and the FCS-MPC algorithm are discussed in detail in this chapter.

Chapter 5 introduces three different single switch open circuit fault detection and diagnosis methods for matrix converter systems. The first diagnosis method is for the DMC system with a FCS-MPC strategy. The second diagnosis method is for the DMC system with a SVM strategy. The third diagnosis method is for the IMC system with a FCS-MPC strategy. Moreover, the bidirectional switch open circuit fault behaviour analysis for both the direct matrix converter and the indirect matrix converter are discussed in detail at the beginning of this chapter.

Chapter 6 presents the simulation results of the DMC system with FCS-MPC strategy, the DMC system with SVM strategy, and the IMC system with FCS-MPC strategy respectively. The simulation results prove the feasibility of the proposed fault detection and diagnosis methods.

Chapter 7 introduces the experimental implementation of the laboratory prototype direct matrix converter for the open circuit switch fault detection and diagnosis. The direct matrix converter power circuit comprises of the power devices, the gate drive circuit, the input filter, the current direction detection circuit and the voltage measurement circuits. The clamp circuit is implemented independently from the matrix converter power circuit in order to place the clamp circuit after the output current sensors for fault detection

and diagnosis purposes. The high bandwidth current sensor design has been described in detail. The specially designed high bandwidth current sensor can achieve current oversampling for fault detection and diagnosis purpose. The hardware control platform implementation of the direct matrix converter system has been achieved using a high performance DSP and FPGA. The fault detection method is implemented in the DSP to achieve real-time fault detection and diagnosis.

Chapter 8 presents the experimental results for the direct matrix converter. All the experimental data presented in this chapter is captured by the DSP-FPGA control platform. This means that the fault detection and diagnosis algorithm proposed in the previous chapter can be implemented into the DSP-FPGA control platform. This will guarantee that the fault detection and diagnosis algorithm can do real-time fault detection and diagnosis for the direct matrix converter system.

Chapter 9 concludes the thesis.

Chapter 2

Matrix Converter Topologies

2.1 Introduction

A matrix converter (MC) is a power converter topology with advantages such as the potential for a compact power circuit[3], controllable input power factor [4, 5], and no large passive DC-Link components [6]. Therefore, research attention has focused on the matrix converter topology for many applications in systems such as the more electric aircraft. Compared to the AC-AC power converter topologies with DC-Link components such as the well known PWM Back-to-Back converter [17, 18], the main advantage of the MCs is the lack of DC-Link components. This is because the use of electrolytic capacitors can be a major cause of lower than ideal converter reliability and lifetime [1].

The direct matrix converter (DMC) is a matrix of bidirectional switches that connect each converter output phase to each supply line [6]. Many modulation strategies for the DMC have been proposed in the literature. The Venturini modulation method proposed in [6] is based on a low frequency modulation matrix which describes the low frequency behaviour of the DMC currents and voltages. The space vector modulation (SVM) method was first proposed in [6] and further developed [19] to become a very efficient mathematical approach for DMC modulation by using the duty-cycle space vector concept. Recently, model predictive control (MPC) has become popular due to the advantages such as fast dynamic response as well as it being relatively

easy to include the non-linearity and constraints of the system [20, 21, 22].

The indirect matrix converter (IMC)[23] is an alternative structure to the DMC. The IMC is also known as the two stage matrix converter and maintains the same input-output performance as the DMC. The IMC contains a current source rectifier (CSR) and a voltage source inverter connected directly by a so-called fictitious DC-Link. The IMC topology simplifies the modulation analysis due to its two stage nature. The IMC also has the potential to reduce the number of controlled semiconductor devices in the source rectifier bridge depending on the power flow requirement [24].

This chapter first introduces the fundamentals of the DMC and the IMC topologies. Then the MC structure will be presented with more detail of the bidirectional switch, the clamp circuit and the input filter. Since there is no freewheeling device in the MCs, a clamp circuit is required to protect the MC against over-voltage damage. A clamp circuit will provide a current circulating path for the inductive load currents to avoid inductive load open-circuit voltages. For good performance the MC also must have an input filter to minimize the high frequency components in the input currents. Finally, the bidirectional switch commutation techniques are presented.

2.2 Direct Matrix Converter Topology

The direct matrix converter topology is shown in Figure 2.1. The direct matrix converter system is composed of an input filter, a switch matrix of nine bidirectional switches and a clamp circuit. The input filter attenuates the switching frequency harmonics in the input currents. The semiconductor switch matrix connects the AC input directly to the three phase output load. The clamp circuit of the direct matrix converter includes 12 fast recovery diodes and a capacitor.

Each output phase of the direct matrix converter is connected to the three phase input voltage source by three bidirectional switches. In total of nine bidirectional switches are used in the 3×3 direct matrix converter topology. The relation between the output voltages and input voltages of the DMC is shown in Equation 2.1. It can be seen from the Equation 2.1 that the

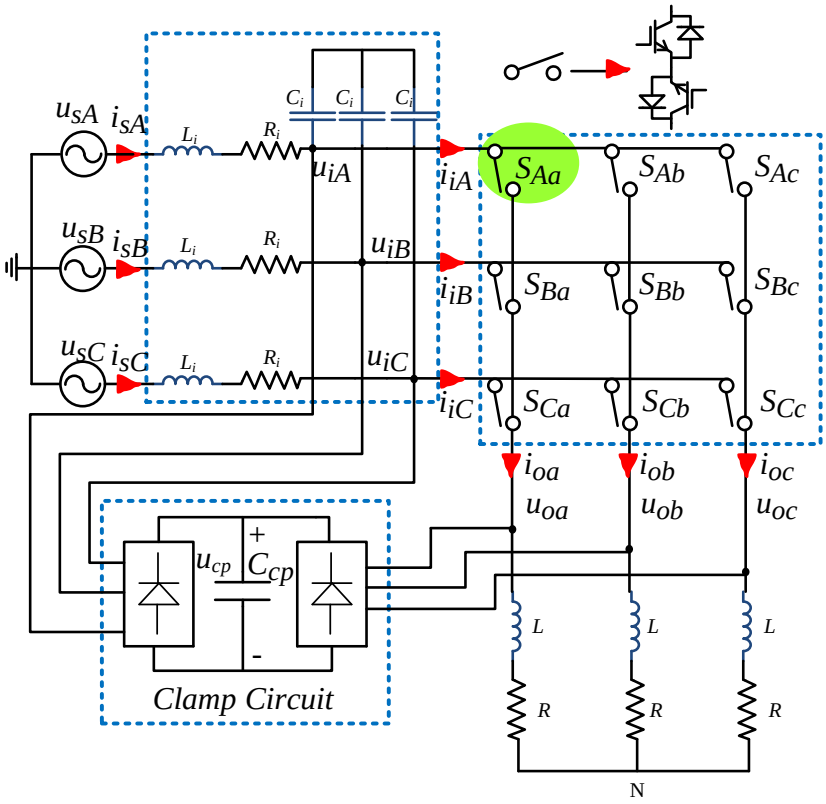


Figure 2.1: Direct matrix converter topology

output voltages are the function of the switching state matrix and the input voltages. The relation between the input currents and the output currents of the DMC is shown in Equation 2.2. It can be seen from the equation 2.2 that the input currents are the function of the switching state matrix and the output currents.

$$\begin{bmatrix} u_{oa} \\ u_{ob} \\ u_{oc} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \cdot \begin{bmatrix} u_{sA} \\ u_{sB} \\ u_{sC} \end{bmatrix} \tag{2.1}$$

$$\begin{bmatrix} i_{iA} \\ i_{iB} \\ i_{iC} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \cdot \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} \tag{2.2}$$

Where $S_{jk}(j = A, B, C; k = a, b, c.)$ represents the switching state of each bidirectional switch. $S_{jk} = 0$ means that the switch S_{jk} is off and $S_{jk} = 1$ means that the switch S_{jk} is on.

In order to control output voltages and the input currents of the DMC, the bidirectional switches have to be turned on or off at given times. During the normal operation of the DMC, the input terminals should not be short circuited because the current is fed by a voltage source. On the other hand, an output phase of the DMC must never be open circuited due to the inductive nature of the load. Therefore, the duty cycles of the nine bidirectional switches have to satisfy the conditions as presented in Equation 2.3.

$$\begin{aligned} 0 \leq m_{jk} \leq 1,\ j = A, B, C,\ k = a, b, c. \\ m_{Aa} + m_{Ba} + m_{Ca} = 1 \\ m_{Ab} + m_{Bb} + m_{Cb} = 1 \\ m_{Ac} + m_{Bc} + m_{Cc} = 1 \end{aligned} \tag{2.3}$$

Where $m_{jk}(j = A, B, C; k = a, b, c.)$ means the duty cycle of each bidirectional switch.

2.3 Indirect Matrix Converter Topology

The indirect matrix converter topology is shown in Figure 2.2. The indirect matrix converter is composed of a current source rectifier stage and a voltage source inverter stage connected by a fictitious DC-Link. The rectifier stage consists of six bidirectional switches, and the inverter stage consists of six unidirectional switches with freewheeling diodes. The clamp circuit is composed of a diode and a capacitor and connected to the fictitious DC-Link of

the indirect matrix converter. The purpose of the clamp circuit is to provide a current recirculating path when a semiconductor switch suffers from an open circuit fault or when the converter is turned off unexpectedly.

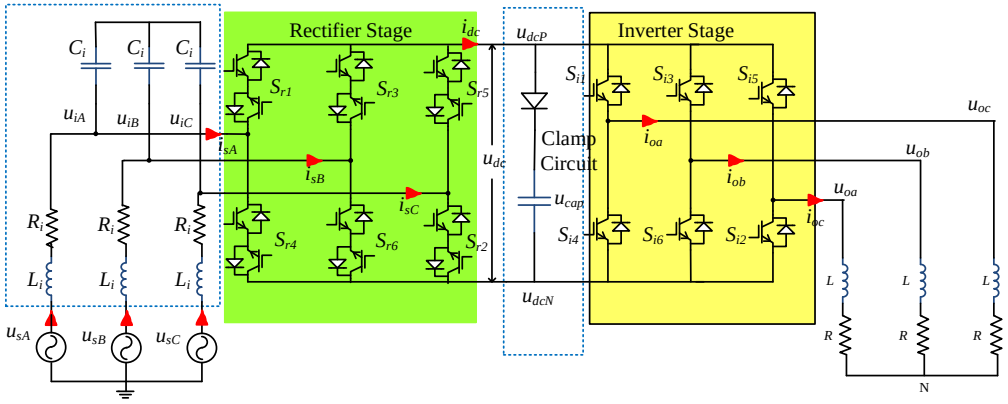


Figure 2.2: Indirect matrix converter topology

The indirect matrix converter topology approach can simplify the concept of the control algorithm in comparison with the direct matrix converter approach [25]. The indirect matrix converter topology is divided into two stages. In this approach to modulation, the rectifier stage and the inverter stage are considered separately. The fictitious DC-Link voltage is comprised of the switched input voltages, and the fictitious DC-Link current is composed of switched the output currents. The input voltage vector $\vec{u_s}$, input current vector $\vec{i_s}$, output voltage vector $\vec{u_o}$ and output current vector $\vec{i_o}$ are shown in Equation 2.4. the output voltage vector $\vec{u_o}$ is referenced to the load neutral point.

$$\begin{aligned} \vec{u_s} &= [u_{iA}, u_{iB}, u_{iC}]^T \\ \vec{i_s} &= [i_{iA}, i_{iB}, i_{iC}]^T \\ \vec{u_o} &= [u_{oa}, u_{ob}, u_{oc}]^T \\ \vec{i_o} &= [i_{oa}, i_{ob}, i_{oc}]^T \end{aligned} \tag{2.4}$$

For the rectifier stage, the fictitious DC-Link voltage u_{dc} is acquired as

a function of the input voltages vector $\vec{u_s}$; the rectifier stage switch states are as shown in Equation 2.5. The input current vector $\vec{i_s}$ are obtained as a function of the fictitious DC-Link current $\vec{i_{dc}}$ and the rectifier stage switch states, as shown in Equation 2.6.

$$u_{dc} = [S_{r1} - S_{r4} \quad S_{r3} - S_{r6} \quad S_{r5} - S_{r2}]\vec{u_s} \tag{2.5}$$

$$\vec{i_s} = \begin{bmatrix} S_{r1} - S_{r4} \\ S_{r3} - S_{r6} \\ S_{r5} - S_{r2} \end{bmatrix} i_{dc} \tag{2.6}$$

For the inverter stage, the output voltage vector $\vec{u_o}$ can be derived as a function of the fictitious DC-Link voltage u_{dc} and the inverter stage switch states, as shown in Equation 2.7. The fictitious DC-Link current i_{dc} is a function of the output current vector $\vec{i_o}$ and the inverter stage switch states, as shown in Equation 2.8.

$$\vec{u_o} = \begin{bmatrix} S_{i1} - S_{i4} \\ S_{i3} - S_{i6} \\ S_{i5} - S_{i2} \end{bmatrix} u_{dc} \tag{2.7}$$

$$i_{dc} = [S_{i1} \quad S_{i3} \quad S_{i5}]\vec{i_o} \tag{2.8}$$

2.4 Matrix Converter Structure

In this section the MC structure will be presented in more detail. The MC has to have an input filter to minimize the high frequency components in the input currents. The switching matrix itself consists of bi-directional switches and there is an over-voltage clamp circuit as descried above.

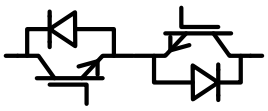


Figure 2.3: Common emitter bidirectional switch

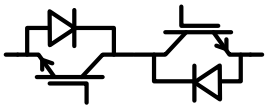


Figure 2.4: Common collector bidirectional switch

2.4.1 Bidirectional Switches

Bidirectional switches are required by the matrix converter to block voltage and control the conduction of current in both directions [3]. However, there is no single semiconductor device currently available, which can satisfy these requirements. Therefore, the bidirectional switch has to be constructed using discrete power power semiconductor devices. There are two arrangements commonly used to create a bidirectional switch, the common emitter arrangement and the common collector arrangements.

The common emitter bidirectional switch arrangement comprises of two controllable devices, such as IGBTs, and two uncontrollable devices, such as diodes, as shown in Figure 2.3. The diodes provide the reverse blocking capability. When designing the gate drive circuit, the common emitter point is regarded as a local ground for each gate drive circuit. Therefore, the DMC requires nine isolated power supplies and the IMC requires six isolated power supplies when using common emitter switch arrangement [14].

The common collector bidirectional switch arrangement also consists of two IGBTs and two diodes, as shown in Figure 2.4. The advantage of this arrangement is that the number of isolated power supplies is possible to reduce from nine to six for the DMC topology [3]. However, this arrangement is often not feasible in a large practical system due to the stray inductance between bi-directional switches[3].

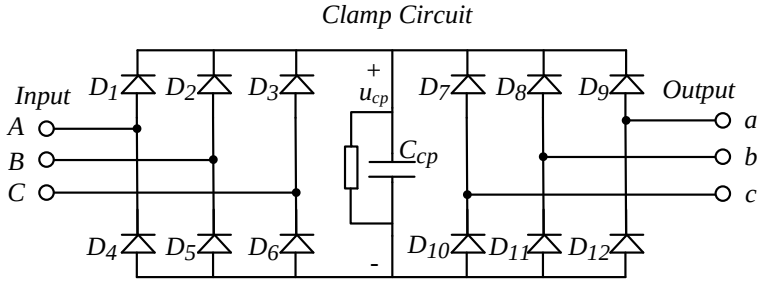


Figure 2.5: Clamp circuit of DMC

2.4.2 Clamp Circuit

Since there are no free-wheeling devices in the DMC, a clamp circuit must be added to protect the DMCs from over-voltage when an open-circuit fault occurs or when the converter is turned off. If these over voltages are not clamped, they could destroy the power semiconductor devices [26]. A typical clamp circuit is shown in Figure 2.5. The clamp circuit is connected between the three phase input supply and the load terminals of the converter. The clamp circuit consists of two fast-recovery diode rectifier bridges, a clamp capacitor and a dissipation resistor. During an open circuit switch fault, the reactive energy stored in the load inductance is transferred to the clamp capacitor and can then be dissipated in the resistor.

The clamp circuit configuration for the IMCs is shown in Figure 2.6. The IMC clamp circuit consist of a single clamp capacitor and a single diode connected between the fictitious rectifier stage and the inverter stage [27]. The IMC clamp circuit does not usually operate under healthy operating condition. Under an output over-voltage fault condition all the switches will be turned off immediately. The fictitious inverter stage freewheeling diodes will provide a current recirculating path to safely remove the energy stored in the inductance of a load [28].

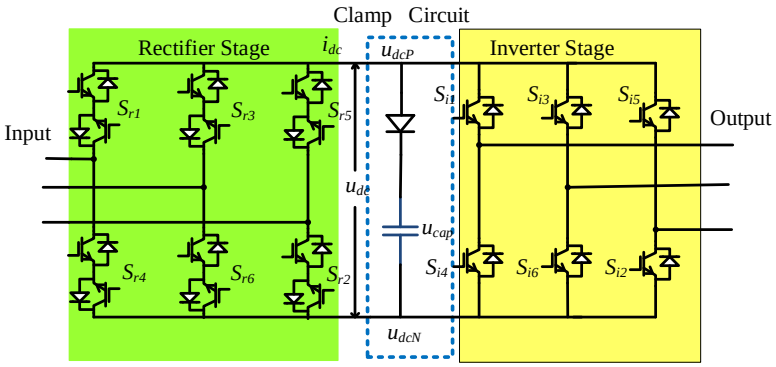


Figure 2.6: Clamp circuit of IMC

2.4.3 Input Filter

In order to ensure input current quality as well as to mitigate the input voltage distortion the MC must have an input filter to minimize the high frequency components in the input currents. The input filter can also help to reduce the electromagnetic interferences (EMI) requirements [29]. One commonly used input filter configuration is shown in Figure 2.7. This LC configuration of the input filter is recommended considering the size and cost efficiency [30]. The size of the reactive components in the LC filter are decided by the switching frequency of the matrix converter [31] and the input power quality requirements. A damping resistor is recommended in parallel with the filtering inductance to improve the system stability [32].

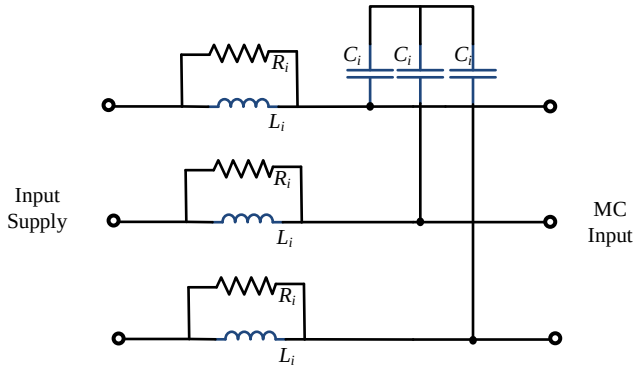


Figure 2.7: Input filter of MC

2.5 Bidirectional Switch Commutation Techniques

Due to the lack of a free-wheeling diodes in the DMC topology, a commutation strategy is required to avoid input short circuits and output open circuits when commutating current between any two bidirectional switches. Several commutation methods have been proposed in the literature [3]. They are categorized as current-direction-based commutation and relative-voltage-magnitude-based commutation. The relative-voltage-magnitude-based commutation requires accurate measurement of the input voltage relative magnitudes. The current-direction-based commutation includes two step commutation and four step commutation. The commonly used solution is the more reliable output-current-direction based four-step current commutation strategy.

There are two gate drive signals for each bidirectional switch. Take bidirectional switch S_{Aa} for example as shown in Figure 2.1, the gate drive signal S_{AaF} controls the forward IGBT and S_{AaR} controls the reverse IGBT of the bidirectional switch. In order to explain the four-step commutation clearly, a simplified two-input-phase to one-output-phase matrix converter with two bidirectional switches is used as an example, as shown in Figure 2.8. When the output current direction is positive, the four gate drive signals for the two

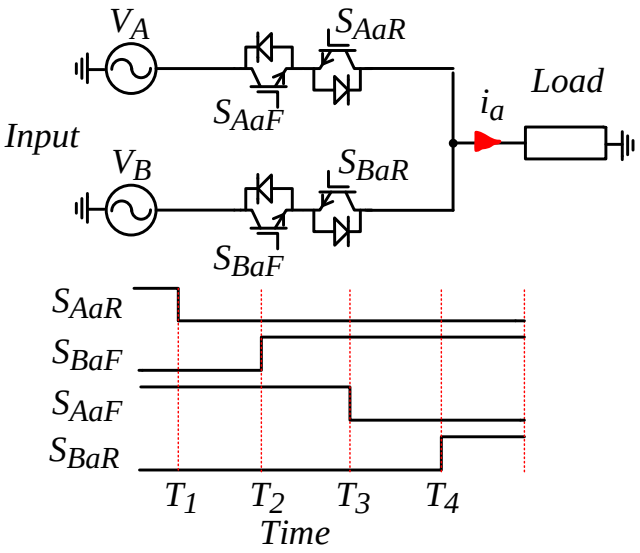


Figure 2.8: Output-current-direction based four step commutation with positive direction current

bidirectional switches act, as shown in Figure 2.8. Before the commutation starts, the bidirectional switch S_{Aa} is conducting. Both S_{AaF} and S_{AaR} are on. When the commutation occurs, the first step is to turn off S_{AaR} because it is not conducting at the time. The second step is to turn on S_{BaF} to provide a current path in the bidirectional switch S_{Ba} due to the positive output current direction. The third step is to turn off the S_{AaF} to commutate the current from bidirectional switch S_{Aa} to S_{Ba}. The final step is to turn on the S_{BaR} to complete the commutation sequence.

When the output current direction is negative as shown in Figure 2.9, the four gate drive signals for the two bidirectional switches act as shown in figure 2.9. Before the commutation happening, the bidirectional switch S_{Aa} is conducting. Both S_{AaF} and S_{AaR} are 1. When the commutation occurs, the first step is to turn off the S_{AaF} because it is not conducting at the moment. The second step is to turn on the S_{BaR} to provide the current path in the bidirectional switch S_{Ba} due to the negative output current direction. The third step is to turn off the S_{AaR} to commutate the current from bidirectional

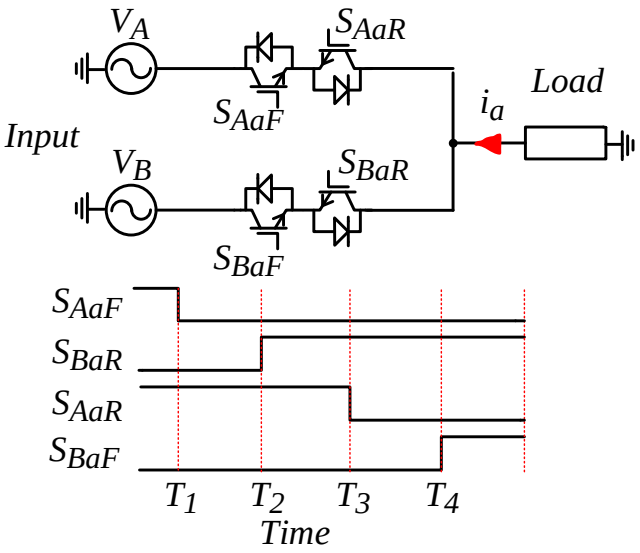


Figure 2.9: Output current direction based four step commutation with negative direction current

switch S_{Aa} to S_{Ba}. The fourth step is to turn on the S_{BaF} to complete the commutation sequence.

2.6 Summary

This chapter introduces the basic concepts of the matrix converter topologies, including the direct matrix converter (DMC) topology and the indirect matrix converter (IMC) topology. General operation principles of the matrix converter topologies are described mathematically to shown how the the switches of the matrix converters act. The DMC topology is constructed by a switch matrix, an input filter and a clamp circuit. The IMC topology consists of a fictitious rectifier stage and inverter stage, an input filter and a clamp circuit. Since there is no freewheeling device in the DMC topology, a commutation strategy is required to avoid input short circuit and output open circuit. The output-current-direction based four step commutation strategy is commonly used for the commutation process.

Chapter 3

Matrix Converters Failure Mechanisms and Fault Diagnosis

3.1 Introduction

The matrix converters are composed of semiconductor switches and have no DC-Link component in the power circuit. So the reliability of the semiconductor switches is a big concern for the application of the matrix converters. Usually, a semiconductor switch can either occur an open circuit fault or a short circuit fault. Ideally, an open circuit switch fault means there is no current flowing in the switch when the switch is turned on, and a short circuit switch fault means there is no voltage drop across the switch when the switch is turned off.

An open circuit switch fault may occur due to the bond-wire lift-off or gate driver fault. An open circuit switch fault in the matrix converter will cause over-voltage stress in the semiconductor switch. If the open circuit switch fault can not be detected and located quickly enough, a catastrophic failure may occur eventually. A short circuit switch fault in the matrix converter may occur due to the gate driver fault or avalanche breakdown. It is more difficult to deal with a short circuit fault compared to an open circuit

fault, because the time between the fault initiation and failure is much more smaller in short circuit faults than in open circuit faults. Therefore, most of the IGBT short circuit fault detection and protection methods are hardware-circuit based rather than algorithm based [9].

Usually, there are three ways to improve the reliability of a power electronic system. These three ways are condition monitoring, diagnosis, and prognosis respectively. Condition monitoring measures the condition of a component in real-time, and appropriate action is taken if it drifts away from the healthy condition. Diagnosis is identifying the root cause of a fault, given that a fault has occurred. Prognosis assesses the current health level of a component, and predicts the health of the component at some point in the future [8]. Prognosis is a very challenging task because it needs reliability modeling of the components. The condition monitoring technique requires sensing and signal processing techniques as well as the knowledge of power device failure mechanisms, which will increase the hardware complexity and cost. Therefore, diagnosis techniques are still a cost-effective way to improve the power electronic system reliability because they require less or even no hardware complexity compared to condition monitoring techniques.

This chapter will focus on the open circuit faults in the matrix converters. Firstly, the failure mechanisms of open circuit faults in the matrix converter system will be described in detail. Then the condition monitoring technique will be introduced. Finally, the previous proposed fault detection and diagnosis methods in both direct matrix converter and indirect matrix converter systems will be reviewed.

3.2 Open Circuit Faults Mechanisms in Matrix Converter Systems

An open circuit fault in the matrix converter system is usually caused either by a power device failure or by a gate driver fault. When the fault is caused by a power device failure, the power device reliability issues become a big concern. Therefore, this section will describe the reliability issues and the

failure mechanisms of power devices as well as the gate driver fault mechanisms.

3.2.1 Power Devices Reliability Issues

Reliability is defined as the ability of an item to perform required function under stated conditions for a certain period of time, which is often measured by probability of failure, frequency of failure, or in terms of availability [33]. The availability is defined as the ratio of the total time a functional unit is capable of being used during a given interval to the length of the internal. Power electronics reliability have been a significant concern since the beginning of the power electronics applications. The good news is that the power devices reliability has been dramatically improved in recent years [34]. For instance, the failure rate of the insulated gate bipolar transistor (IGBT) power module has fallen from 1000 failures in time (FITs) in year 1995 to 20 FITs in year 2000, where $1FIT = 1 * 10^{-9}$ failures per device-hour [35]. However, the reliability issues of power devices is always a big concern in safety-critical applications such as more electric aircraft (MEA) electrical power system (EPS) [36]. For example, 21% of the failures of the voltage sourced converters are caused by the semiconductor faults as shown in Figure 3.1 [1]. Another industry survey claims that the failure of the power devices count for 38% of the total faults in the variable speed AC drive area [7]. The results of these surveys indicate that the power devices reliability is still an important focus in industry as well as in research.

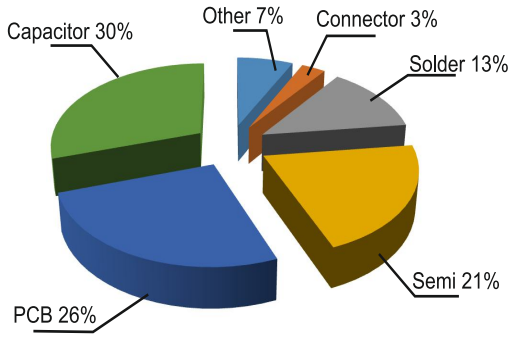


Figure 3.1: Failure distribution in power electronics [1]

3.2.2 Power Devices Failure Mechanisms

The failure mechanisms of the power devices have been well researched in literature [37, 38, 39, 40, 41, 42, 43, 44, 45]. Knowledge of power device failure mechanisms is necessary before doing fault detection and diagnosis on the power devices. This is because the failure mechanisms will decide what kind of fault will occur inside a power device. For example, the failure mechanisms of the open circuit switch fault are different from the failure mechanisms of the short circuit switch fault. Different types of power devices also have different types of failure mechanisms. So the fault detection and diagnosis strategy on power electronics should be developed based on specific application conditions.

There are two different types of failure mechanisms of power devices. They are extrinsic failure mechanisms and intrinsic failure mechanisms respectively. The extrinsic failure mechanisms are due to the weaknesses in design and manufacturing process. The intrinsic failure mechanisms are caused by the time-dependent degradation of device characteristics during useful lifetime. This section will ignore the weaknesses in design and manufacturing process and focus on the intrinsic failure mechanisms because the components and constituent materials are used close to their physical limits.

The intrinsic failure mechanisms include the sudden catastrophic failures and wear-out failures. Sudden catastrophic failures can occur due to many factors such as over-voltage leading to dielectric breakdown, over-current

leading to overheating and destruction, over-temperature, and cosmic rays radiation effects. The sudden catastrophic failures are unpredictable. The wear-out failures are caused by the build-up of damage and gradual degradation such as over-temperature, which eventually will lead to catastrophic failure. Wear-out degradation mechanisms have no externally observable change in performance or gradual decline in performance with time until the catastrophic failure occurs. The wear-out mechanisms are usually predictable.

Take the insulated gate bipolar transistor (IGBT) for example, the cross-sectional view of an IGBT is shown in Figure 3.2. The power module consists of the wire bonds, the solder joints, the semiconductor devices, the ceramic substrate, the heat spreader(base plate) and the bus-bars. The IGBT power module wear-out mechanisms include the wire-bond lift-off, cracking of die-attach solder, cracking and delamination of the substrate-to-base-plate mountdown solder, and the delamination and fracture of ceramic substrates [46].

Wire-bond lift-off is caused by thermal-mechanical stresses due to the coefficient of thermal expansion (CTE) mismatch between the aluminum wire and the silicon. This CTE mismatch will cause fatigue cracking at the bond interface. The cracking of die-attach solder is caused by creep and thermal-mechanical fatigue. Cracking and delamination of the substrate-to-base-plate mountdown solder is also caused by thermal-mechanical fatigue due to CTE mismatch between the involved layers. The delamination and fracture of ceramic substrates is also due to the CTE mismatch [46].

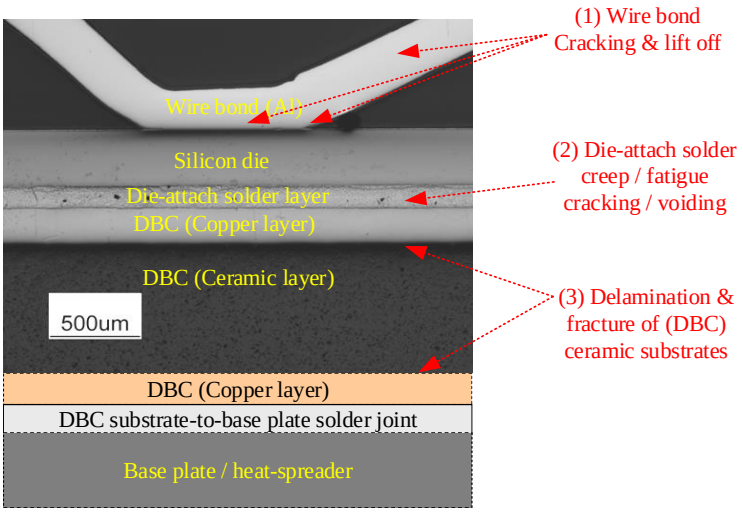


Figure 3.2: Cross-sectional view of an IGBT

3.2.3 Gate Driver Fault Mechanism

A gate driver fault may cause an open circuit switch fault or a short circuit switch fault even though a semiconductor switch is in healthy condition. This gate driver fault mechanism is called gate-misfiring. If a semiconductor switch is supposed to turn off but the gate driver outputs a turn-on signal, it may cause a short circuit switch fault. If a semiconductor switch is supposed to turn on but the gate driver outputs a turn-off signal, it may cause an open circuit switch fault. In most cases, the gate-misfiring is intermittent in nature [9]. Therefore, real-time monitoring is essential especially in safety critical applications such as more electric aircraft (MEA) electrical power system (EPS).

3.3 Power Electronics Condition Monitoring Methods

In order to guarantee the reliability of a power electronic system during operation and prevent a catastrophic failure from occurring, a condition moni-

toring scheme can be implemented either at the device level or at the system level. Device level condition monitoring means that additional sensing units are implemented to measure some specific device parameters which indicate the degradation of the device. The measured device parameters include the on-stage voltage, the temperature, and the gate drive signal. System level condition monitoring means that the device condition can be indirectly monitored by only using some specific system parameters. This is because the power electronic system response will be affected by the degradation of a power device.

3.3.1 On-State Voltage-Based Condition Monitoring

A sensing unit can be implemented into a device power module to periodically monitor the on-state voltage (voltage between collector and emitter V_{CE} when switching on) and current of the device. The on-state voltage and current of the device are sampled simultaneously. A on-state voltage look-up table is saved for a range of given current values. For a given current value, the simultaneously measured on-state voltage will be compared with the one in the look-up table to monitor the health condition of the device. This method can be used to detect the bond wire lift-off failure [47, 48, 49, 50, 51].

3.3.2 Temperature-Based condition monitoring

Additional temperature sensors can be located inside a device power module as well as on the heat sink to measure the device temperature over a period of time [52]. The temperature data is saved together with the corresponding load current. Then the recorded data is used to calculated the thermal resistance of the power module at different locations. The aim of the condition monitoring is achieved when the thermal resistance is changing [53, 54, 47, 55, 56, 57, 58, 59].

3.3.3 Gate-Signal-Based Condition Monitoring

The gate-signal-based condition monitoring is based on the gate voltage waveform during turn-on process. This is because the gate charge distribution is affected by the degradation of the power device. However, the gate-signal-based condition monitoring technique requires very high sampling resolution of the voltage sensing unit in order to capture the Miller Plateau. Therefore, this technique will greatly increase the hardware complexity and the cost [60].

3.3.4 System Level Condition Monitoring Methods

Theoretically, the system response will be affected by the degradation of a power device. So monitoring the power device condition on the system level is possible by knowing the system characteristics [61, 50]. When monitoring the power device condition at the system level, no additional sensing unit is required by each power device. Instead, only system level signals such as output voltages and/or output currents are required to detect the degradation of a power device if the system behaviour under degradation conditions is known. Therefore, the system level condition monitoring methods have the advantage that minimum additional sensing units and hardware complexity is required.

In order to successfully implement the condition monitoring methods on system level, the following three requirements should be satisfied [8].
1) The system characteristic change under specific failure mode condition must be known.
2) Advanced signal sensing and processing techniques might be required such as over-sampling techniques.
3) High-frequency noise attenuation is necessary for advanced signal sensing and processing techniques.

As mentioned before, condition monitoring is measuring the condition of a component in real-time, and taking appropriate action if it drifts away from a healthy condition. Diagnosis is identifying the root cause of a fault, given that a fault has occurred. So a real-time fault detection and diagnosis system is the

combination of system level condition monitoring techniques and diagnosis techniques. In the next section, a literature review on fault detection and diagnosis methods in a matrix converter system will be presented.

3.4 Open Circuit Fault Detection and Diagnosis in Matrix Converter Systems

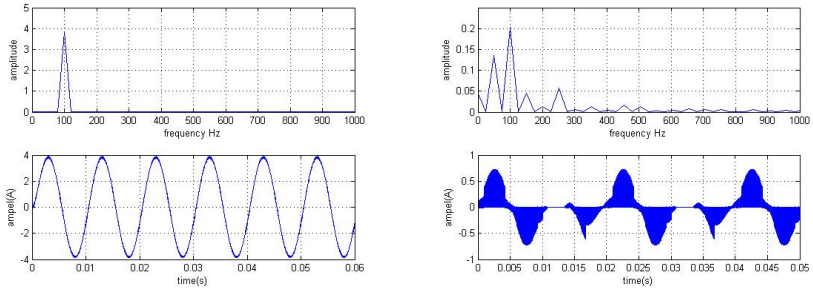
It is inevitable that an open circuit fault will occur during a matrix converter (MC) system lifetime. In order to continue operation, fast and reliable fault diagnosis methods are essential to minimize the hazard of over-voltage or over-current conditions. The fault detection and diagnosis methods in matrix converter systems can be mainly divided into two categories: the signal processing based diagnosis and the analytical model based methods. In this section, these two categories of fault detection and diagnosis methods will be described in detail.

3.4.1 MC Signal Processing Based Diagnosis

The signal processing based diagnosis analyzes the characteristics of the sampled signals, such as the spectral components of the current. Characteristic changes of the sampled signals can indicate that a fault is occurring.

MC Current Spectral Components Based Diagnosis

Current spectral components based diagnosis has been proposed in literature [10]. This method analyzes the output current spectral components by using Fast Fourier Transformation (FFT) analysis. Supposed that the fundamental component of the input current frequency is $50Hz$ and the fundamental component of the output current frequency is $100Hz$. Therefore, the spectral components of output current will include other faulty-related component frequency, besides the fundamental component of the output current. Output-phase-a current spectral components on healthy and open-circuit operation are shown below respectively in figure 3.3 to prove the theory mentioned



(a) Current spectra of the output phase a when in normal operation

(b) Current spectra of the output phase a when Sw_{Ac} open-circuit

Figure 3.3: Current spectra of matrix converter during normal and open-circuit condition

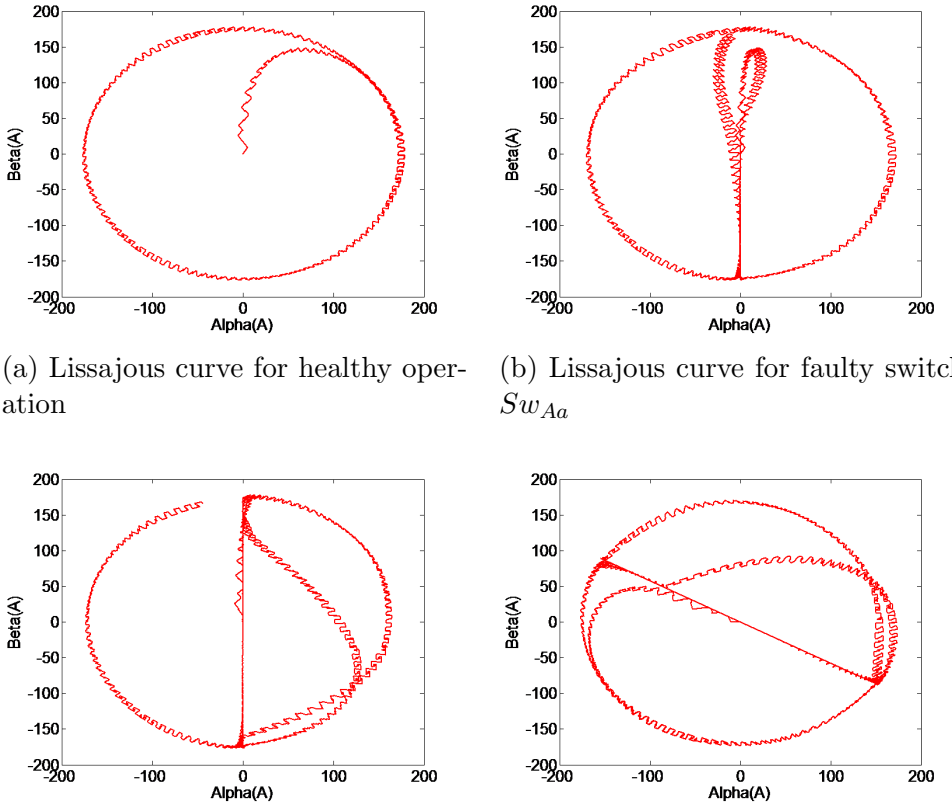
above. Another similar diagnosis method is proposed in [62] to analyze the current spectral components by using Discrete Wavelet Transform (DWT). The main drawback of this spectral component based method is that it cannot locate down to the single bidirectional switch which is open-circuit. It can only detect the faulty phase because the spectral components of each single faulty switch in one output phase are similar to each other.

MC Current Park Vector Based Diagnosis

Park Vector method is based on the alpha-beta transformation that transforms the three phase output current into two phase alpha-beta frame. This approach based on computer-aided monitoring of the three-phase supply current Park Vector, and the fault diagnosis scheme is based on identifying unique signature patterns in the figures obtained. Recently, some literature [63, 64] uses the Park Vector to detect and diagnose fault in matrix converters.

The Lissajous curve is a circle with fixed frequency on healthy operation. When in faulty condition, other frequency components are added and the Lissajous curve shape changes due to the fault. Therefore, the fault can be detected and diagnosed after minimum one complete output cycle, which slows down the fault detection speed. Although the instantaneous frequency

method [65] could reduce the detection time, it can only detect a fault rather than diagnose it. Additional information such as switch state should also be considered to locate the fault down to any single bidirectional switch. In addition, this method also needs to consider the value of the duty-cycle to ensure that the faulty switch is the predominant switch in one switch period. This Park vector method is also used to detect and diagnose fault for sparse matrix converters based on similar theory [64]. The Lissajous curve of the matrix converter output current Park vector during healthy and open-circuit operation is presented in figure 3.4.



(a) Lissajous curve for healthy operation

(b) Lissajous curve for faulty switch Sw_{Aa}

(c) Lissajous curve for faulty switch Sw_{Ba}

(d) Lissajous curve for faulty switch Sw_{Ca}

Figure 3.4: Lissajous curve of the matrix converter output current Park vector during healthy and open-circuit operation

3.4.2 MC Analytical Model Based Diagnosis

The analytical model based diagnosis requires the mathematical model of the matrix converter system to do fault detection and diagnosis. Usually, the switch matrix model of the matrix converter system is utilized to help locate the fault. System level signals such as the MC output voltage, the MC clamp circuit capacitor current, or the MC output current will also be sampled for diagnosis purpose.

MC Output Voltage Based Diagnosis

The idea of the MC output voltage based method is to compare the actual output voltage with the reference voltage value already known by the analytical model. The voltage signal based fault detection and diagnosis scheme was first used for matrix converters in [11]. It is based on the indirect matrix converter low frequency analytical model, which consists of an assumed rectifier and inverter connected with a virtual DC-Link. This method compares the actual output three phase voltages with estimated reference values to get three phase error voltages, which can be used for fault detection and diagnosis.

The matrix converter three phase output voltages can be estimated by calculating the transfer matrix times the input voltages. The estimated voltage is expressed in equation 3.1. Where $\bar{V}_{outa}$, $\bar{V}_{outb}$, and $\bar{V}_{outc}$ are the estimated output phase voltages. The error voltages are the difference between the actual voltage value and the estimated voltage value and can be expressed in equation 3.2.

$$\begin{bmatrix} \bar{V}_{outa} \\ \bar{V}_{outb} \\ \bar{V}_{outc} \end{bmatrix} = \begin{bmatrix} Sw_{Aa} & Sw_{Ba} & Sw_{Ca} \\ Sw_{Ab} & Sw_{Bb} & Sw_{Cb} \\ Sw_{Ac} & Sw_{Bc} & Sw_{Cc} \end{bmatrix} \cdot \begin{bmatrix} V_{inA} \\ V_{inB} \\ V_{inC} \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} V^{err}_{outa} \\ V^{err}_{outb} \\ V^{err}_{outc} \end{bmatrix} = \begin{bmatrix} V_{outa} - \bar{V}_{outa} \\ V_{outb} - \bar{V}_{outb} \\ V_{outc} - \bar{V}_{outc} \end{bmatrix} \tag{3.2}$$

These three output error voltages can only locate the fault on each phase, not on each bidirectional switch. In order to diagnose which bidirectional switch is open-circuit, input current-output voltage sector combination information is needed. Under normal operation, the output error voltages should be extremely small, but the error voltage will increase obviously if an open-circuit fault occurs. Therefore, this phenomenon can help to detect and diagnose open-circuit fault. In addition, since voltage sensor is susceptible to noise, therefore integration of the error voltage is needed to improve the noise immunity.

One obvious disadvantage of this method is that three additional output voltage sensors are needed, which is not usually available in traditional motor drive systems. This will increase the system complexity and decrease the reliability. Moreover, the integration of the error voltage will slow down the detection speed. In addition, the detection speed will become very slow if the output frequency is close to input frequency, because it will take a long time to get the information of the combination of the input-output-sectors.

In order to overcome the disadvantage mentioned above, more error signals should be generated to locate the fault down to each bidirectional. Therefore, papers [12, 66, 67] improved this method by using the switching function of each bidirectional switch of the matrix converter to modulate nine Modulated Error Voltage (MEV) signals. The procedure to calculate the nine MEV signals is expressed in equation 3.3.

$$\begin{bmatrix} \varepsilon_{Aa} & \varepsilon_{Ba} & \varepsilon_{Ca} \\ \varepsilon_{Ab} & \varepsilon_{Bb} & \varepsilon_{Cb} \\ \varepsilon_{Ac} & \varepsilon_{Bc} & \varepsilon_{Cc} \end{bmatrix} = \begin{bmatrix} V_{outa} - \bar{V}_{outa} & 0 & 0 \\ 0 & V_{outb} - \bar{V}_{outb} & 0 \\ 0 & 0 & V_{outc} - \bar{V}_{outc} \end{bmatrix} \cdot \begin{bmatrix} Sw_{Aa} & Sw_{Ba} & Sw_{Ca} \\ Sw_{Ab} & Sw_{Bb} & Sw_{Cb} \\ Sw_{Ac} & Sw_{Bc} & Sw_{Cc} \end{bmatrix} \tag{3.3}$$

This MEV method is an analytical method because the reference voltage value can be calculated in real-time by using a low frequency modulation matrix (LFMM) mathematical model. Since there are delays in matrix converter system such as IGBTs switching on and off time delay, and the respond time delay of the voltage transducers (Hall effect sensors), so only after a certain delay time the output error voltage should be evaluated to detect the fault. In addition, the error voltage signals should also be integrated to avoid noise issues. When the valid output voltages are measured after a delay time and nine MEVs are calculated, an open-circuit fault can be diagnosed and located on each bidirectional switch. Again, the added voltage sensors are sensitive to noise and will increase the system complexity.

Other literature also proposed the similar output error voltage based and nine MEV based fault detection method [68, 69, 70, 71]. Paper [68] proposes an open circuit fault diagnosis method for the direct matrix converter with model predictive control (MPC) strategy. This method estimates the output voltage errors by using the output load model. The method proposed in [69, 70] compares the measured output voltage signals with reference input voltage signals, and then combines the switching state information to generate error signals. A hysteresis detector is used to evaluate these error signals. If the error signals reach certain limit value, a fault can be detected. However, the added voltage sensors is sensitive to noise and will increase the system complexity. In [71], an open circuit fault diagnosis method is proposed based on the indirect matrix converter (IMC) topology with space vector modulation (SVM) strategy. The proposed fault diagnosis method requires additional voltage sensors to measure the IMC output voltages as well as the fictitious DC-Link voltage. Again, this method requires additional hardware complexity.

MC Clamp Circuit Capacitor Current Based Diagnosis

One fault detection and diagnosis method using clamp circuit current is proposed in [72, 14]. This method uses an additional current sensor to measure the current passing through the capacitors in the clamp circuit. The sensor

placement is shown in figure 3.5. The matrix converter current clamp system is presented in the figure 3.5 below. If an open-circuit fault happens in the matrix converter, the load current will flow through the clamp circuit instead. Therefore, the current flowing through the capacitor of the clamp circuit is measured to modulate nine current errors. The nine current errors can be expressed in equation 3.4. Where i_j means the output phase currents, S_{jkf} means the forward switch and S_{jkr} means the reverse switch. Furthermore, this method integrates nine current errors in order to provide noise immunity as well as prevent incorrect faulty device diagnosis. However, the additional current sensor increases the drive system complexity, which will decrease the system reliability. Moreover, the integration of the current errors will slow down the diagnosis speed.

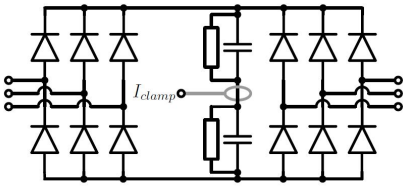


Figure 3.5: Clamp circuit current sensor placement

$$e_{jk} = \begin{cases} i_{clamp}S_{jkf} - ||i_j| - i_{clamp}|S_{jkf} & i_j > 0 \\ i_{clamp}S_{jkr} - ||i_j| - i_{clamp}|S_{jkr} & i_j < 0 \end{cases} \tag{3.4}$$

Another method is proposed in the literature [73] to overcome the disadvantage mentioned above. Three traditional current sensors are connected close to the converter and the clamp circuit are connected closed to the load. The current sensor location change enables the clamp circuit current measurement without an additional current sensor. Therefore, the clamp circuit can be reconstructed with some minor mathematical manipulations. The clamp circuit can be expressed in equation 3.5.

$$\begin{aligned} \sum_{n=1}^{3} i_{load}(n) &= \sum_{n=1}^{3} (i_{out}(n) + i_{clamp}(n)) \\ \sum_{n=1}^{3} i_{out}(n) &= -\sum_{n=1}^{3} i_{clamp}(n) \end{aligned} \tag{3.5}$$

Using the information of the reconstructed clamp circuit current along with three output current, the open-circuit fault can be diagnosed on each bidirectional switch when sampling current within all three zero vectors. However, the experiment results only show the fault location on each phase rather than each bidirectional switch. Another disadvantage is that this method only works well when the load current is flowing and the faulty switch is the predominant switch. If there is little load current flowing, the reconstructed clamp circuit current will be zero and the fault cannot be detected.

MC Output Current Based Diagnosis

Paper [15] proposes a fault diagnosis method which relocates the three output current sensors ahead of the clamp circuit to directly measure the matrix converter output current within three different zero vectors. The space vector modulation (SVM) technique is used in this method. However, the zero vectors duty-cycle are extremely small and hard to capture in high modulation ratio occasions. A similar fault diagnosis method is proposed in [16], relying on the load currents decreasing to zero. The model predictive control (MPC) technique is applied in this method. However, waiting for load current to decrease to zero will slow down the fault diagnosis process.

The main advantage of the proposed fault diagnosis methods in [15, 16] is that it requires no load model or additional sensor. However, the limitation of this method is that there is not enough expert knowledge about how current circulates in the matrix converter during a fault period, to guarantee the fault diagnosis system to make correct diagnosis about which switch is open-circuit. For instance, if the open-circuit load current flows through the clamp circuit and matrix converter and back to load, the common mode current will

exist in the matrix converter and may cancel the current in the healthy phase such as output phase b. Therefore, the output phase b current will be zero and the fault diagnosis system will assume output phase b as open circuit. This wrong detection can be solved if more expert knowledge, such as how current circulating in clamp circuit and in matrix converter, is added into the fault diagnosis system.

3.5 Summary

This chapter introduces the open circuit faults in the matrix converter systems. Firstly, the failure mechanisms of open circuit faults in the matrix converter system is described in detail. Then the condition monitoring technique is introduced both on the device level and on the system level. Finally, the previous proposed fault detection and diagnosis methods in the matrix converter systems is reviewed.

This chapter focuses on the open circuit fault in the matrix converter system. The open circuit fault can either be caused by the power device failure or by the gate drive circuit failure. There are three ways to improve the reliability of a matrix converter system and mitigate the damage caused by the open circuit fault. These three ways are prognosis, condition monitoring, and diagnosis respectively. The prognosis is a very challenging task because it needs the reliability modeling of the components. The condition monitoring technique requires sensing and signal processing techniques as well as the knowledge of power device failure mechanisms, which will increase the hardware complexity and cost. The real-time fault diagnosis technique is the combination of the system level condition monitoring technique and the diagnosis technique. Therefore, the diagnosis technique is still a cost-effective way to improve the matrix converter system reliability because it require less or even no hardware complexity comparing to condition monitoring technique.

Fault diagnosis technique requires the expert knowledge of the system behaviour under a fault condition. For example, the fault diagnosis in a direct matrix converter system with finite-control-set model-predictive-control (FCS-MPC) strategy does not require over-sampling technique because there

is only one fixed switching state during each modulation period. However, for the space vector modulation (SVM) strategy and the modulated model-predictive-control (M2PC) strategy, the over-sampling technique may be required because the switching state during each modulation period is changing. Therefore, the fault diagnosis algorithm design highly depends on the characteristics of the matrix converter system, including the topology, the control strategy and so on.

Chapter 4

Matrix Converter System Modulation and Control

4.1 Introduction

This chapter will introduce commonly used modulation techniques for which the fault diagnosis techniques described later will be required to be able to use. This chapter introduces the Space Vector Modulation (SVM) strategy and the Finite-Control-Set Model Predictive Control (FCS-MPC) strategy for the direct matrix converter (DMC) system. In addition, this chapter also introduces the Finite-Control-Set Model Predictive Control (FCS-MPC) strategy for the indirect matrix converter (IMC) system. Moreover, the faulty behaviour analysis under an bidirectional switch open circuit fault in both the direct and indirect matrix converter systems is presented in the chapter.

4.2 Space Vector Modulation for Direct Matrix Converters

This section will introduce the Space Vector Modulation (SVM) strategy applied to the direct matrix converter system. The SVM strategy applies specific switching vectors for a pre-calculated time with a specific switching sequence during each modulation period. The demand output voltage and

input current vectors can be synthesized by applying each specific switching vector with a specific duty cycle.

4.2.1 SVM switching vectors

The valid switching vectors for a direct matrix converter are shown in Table 4.1. There are a total of 21 valid switching vectors. These 21 valid switching vectors are grouped into two different categories. Those that interconnect all of the output phases to the same input phase are called zero vectors. The rest of the 18 switching vectors which connect two output phases to the same input phase and the remaining output phase to another input phase are called active vectors. Where α_o is the angle of the output voltage vector and β_i represents the angle of the input current vector.

Table 4.1: Valid SVM switching vectors for direct matrix converter as shown in Figure 2.1

Switching configuration	Switches On	u_o	α_o	i_i	β_i
$+1$	$S_{Aa}\ S_{Bb}\ S_{Bc}$	$2/3u_{AB}$	0	$2/\sqrt{3}i_a$	$-\pi/6$
-1	$S_{Ba}\ S_{Ab}\ S_{Ac}$	$-2/3u_{AB}$	0	$-2/\sqrt{3}i_a$	$-\pi/6$
$+2$	$S_{Ba}\ S_{Cb}\ S_{Cc}$	$2/3u_{BC}$	0	$2/\sqrt{3}i_a$	$\pi/2$
-2	$S_{Ca}\ S_{Bb}\ S_{Bc}$	$-2/3u_{BC}$	0	$-2/\sqrt{3}i_a$	$\pi/2$
$+3$	$S_{Ca}\ S_{Ab}\ S_{Ac}$	$2/3u_{CA}$	0	$2/\sqrt{3}i_a$	$7\pi/6$
-3	$S_{Aa}\ S_{Cb}\ S_{Cc}$	$-2/3u_{CA}$	0	$-2/\sqrt{3}i_a$	$7\pi/6$
$+4$	$S_{Ba}\ S_{Ab}\ S_{Bc}$	$2/3u_{AB}$	$2\pi/3$	$2/\sqrt{3}i_b$	$-\pi/6$
-4	$S_{Aa}\ S_{Bb}\ S_{Ac}$	$-2/3u_{AB}$	$2\pi/3$	$-2/\sqrt{3}i_b$	$-\pi/6$
$+5$	$S_{Ca}\ S_{Bb}\ S_{Cc}$	$2/3u_{BC}$	$2\pi/3$	$2/\sqrt{3}i_b$	$\pi/2$
-5	$S_{Ba}\ S_{Cb}\ S_{Bc}$	$-2/3u_{BC}$	$2\pi/3$	$-2/\sqrt{3}i_b$	$\pi/2$
$+6$	$S_{Aa}\ S_{Cb}\ S_{Ac}$	$2/3u_{CA}$	$2\pi/3$	$2/\sqrt{3}i_b$	$7\pi/6$
-6	$S_{Ca}\ S_{Ab}\ S_{Cc}$	$-2/3u_{CA}$	$2\pi/3$	$-2/\sqrt{3}i_b$	$7\pi/6$
$+7$	$S_{Ba}\ S_{Bb}\ S_{Ac}$	$2/3u_{AB}$	$4\pi/3$	$2/\sqrt{3}i_c$	$-\pi/6$
-7	$S_{Aa}\ S_{Ab}\ S_{Bc}$	$-2/3u_{AB}$	$4\pi/3$	$-2/\sqrt{3}i_c$	$-\pi/6$
$+8$	$S_{Ca}\ S_{Cb}\ S_{Bc}$	$2/3u_{BC}$	$4\pi/3$	$2/\sqrt{3}i_c$	$\pi/2$
-8	$S_{Ba}\ S_{Bb}\ S_{Cc}$	$-2/3u_{BC}$	$4\pi/3$	$-2/\sqrt{3}i_c$	$\pi/2$
$+9$	$S_{Aa}\ S_{Ab}\ S_{Cc}$	$2/3u_{CA}$	$4\pi/3$	$2/\sqrt{3}i_c$	$7\pi/6$
-9	$S_{Ca}\ S_{Cb}\ S_{Ac}$	$-2/3u_{CA}$	$4\pi/3$	$-2/\sqrt{3}i_c$	$7\pi/6$
0_A	$S_{Aa}\ S_{Ab}\ S_{Ac}$	0	$-$	0	$-$
0_B	$S_{Ba}\ S_{Bb}\ S_{Bc}$	0	$-$	0	$-$
0_C	$S_{Ca}\ S_{Cb}\ S_{Cc}$	0	$-$	0	$-$

According to the value of α_o and β_i in Table 4.1, it can be seen that the active vectors can divide the input and output $\alpha - \beta$ coordinates into six sectors. The output line-to-neutral voltage sectors together with the numbered vectors which produce output in the relevant directions are presented in Figure 4.1. The input line current sectors together with the numbered vectors which create the vector directions are shown in Figure 4.2.

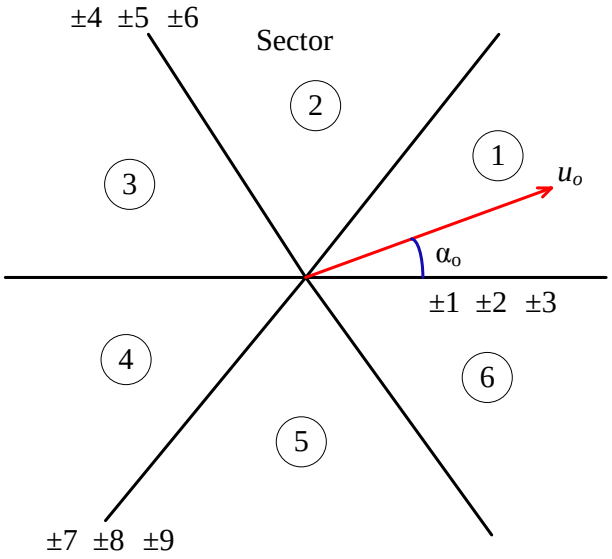


Figure 4.1: Output line-to-neutral voltage sectors

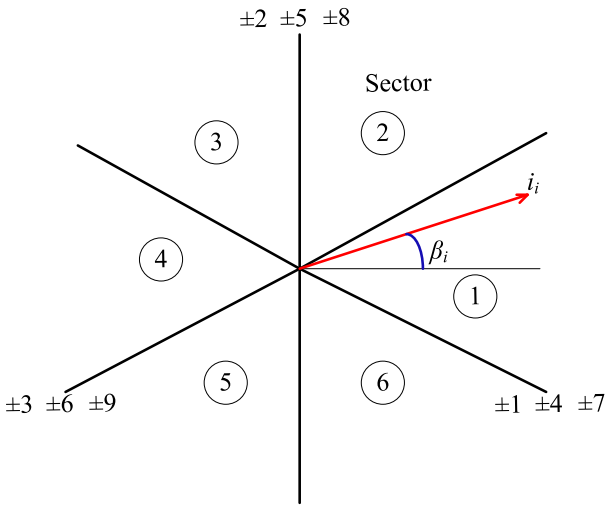


Figure 4.2: Input line current sectors

The input line current space vector can be derived from the output currents. The input current vector $\vec{i_i}$ and the output voltage line-to-neutral space vector $\vec{u_o}$ are given in equation 4.1. Taking the -6 active-vector as an example, the input currents are given by $i_A = i_b$, $i_B = 0$, and $i_C = i_a + i_c = -i_b$. Substituting these values into equation 4.1 and calculating the synthesized input current vector, the -6 space vector can be obtained as $-2/\sqrt{3}i_b$.

$$\begin{aligned} \vec{i_i} &= 2/3 * (i_a + i_b * e^{j2\pi/3} + i_c * e^{j4\pi/3}) \\ \vec{u_o} &= 2/3 * (v_{AO} + v_{BO} * e^{j2\pi/3} + v_{CO} * e^{j4\pi/3}) \end{aligned} \tag{4.1}$$

The output line-to-neutral voltage vector can be derived from the the input voltages as shown in Figure 4.3. Taking +1 active vector for instance, for the line-to-neutral case $V_{Out-a} = 2/3(V_{AB})$, $V_{Out-b} = -1/3(V_{AB})$, $V_{Out-c} = -1/3(V_{AB})$, the synthesized output line-to-neutral voltage vector can be calculated out as $2/3(V_{AB})$ by equation 4.1.

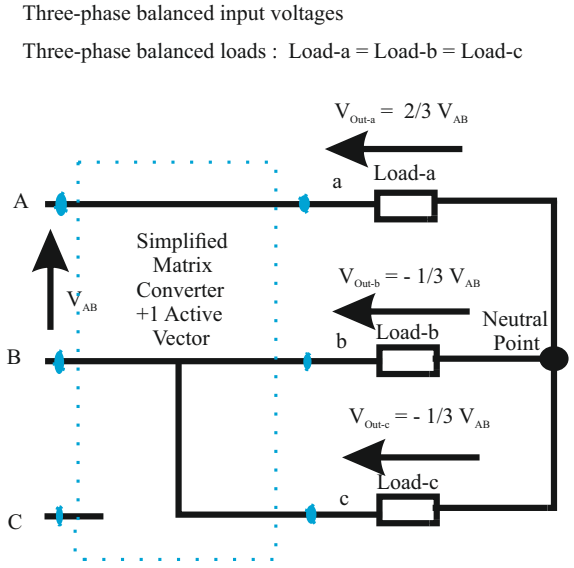


Figure 4.3: Output voltage space vectors representation

4.2.2 Direct Matrix Converter SVM Strategy Switching Sequence

The SVM strategy usually selects both the active vectors and the zero vectors to synthesize the reference vector. The knowledge about which vectors to apply, the sequence of the applied vectors and the duty cycle is required to be decided by the SVM algorithm. This section discusses three SVM strategy switching sequences. There are: SVM with three zero vectors per sequence (3-Zero-SVM); SVM with two zero vectors per sequence (2-Zero-SVM); and SVM with one zero vector per sequence (1-Zero-SVM).

The 3-Zero-SVM switching sequence is shown in Figure 4.4. The 2-Zero-SVM switching sequence is shown in Figure 4.5. The 1-Zero-SVM switching sequence is shown in Figure 4.6. The 1-zero-SVM has the potential of lower switching loss due to less number of switching in each PWM period compared to 3-Zero-SVM and 2-Zero-SVM. However, the 1-zero-SVM has the potential of higher switching harmonics compared to 3-Zero-SVM and 2-Zero-SVM. In terms of fault diagnosis, the 1-zero-SVM will be a better choice because it will make the fault diagnosis algorithm easier to locate the faulty switch.

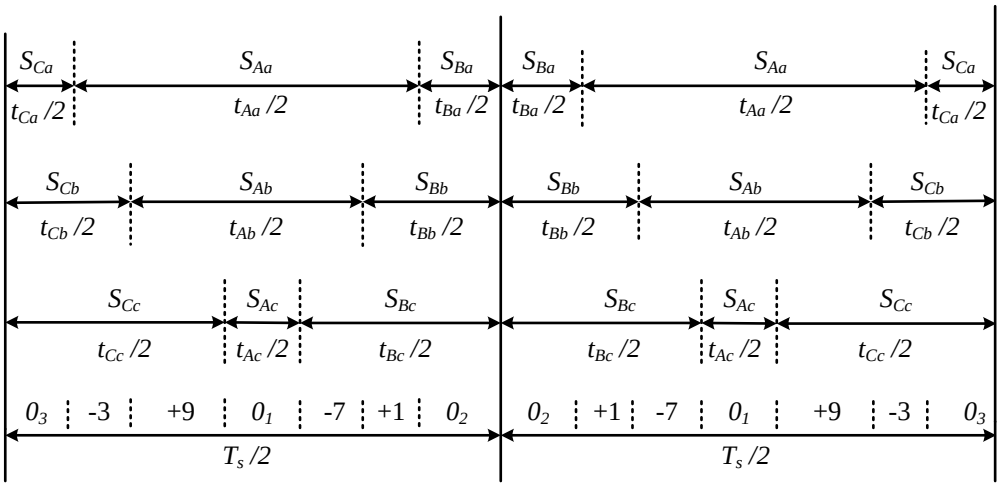


Figure 4.4: The 3-Zero-SVM switching sequence

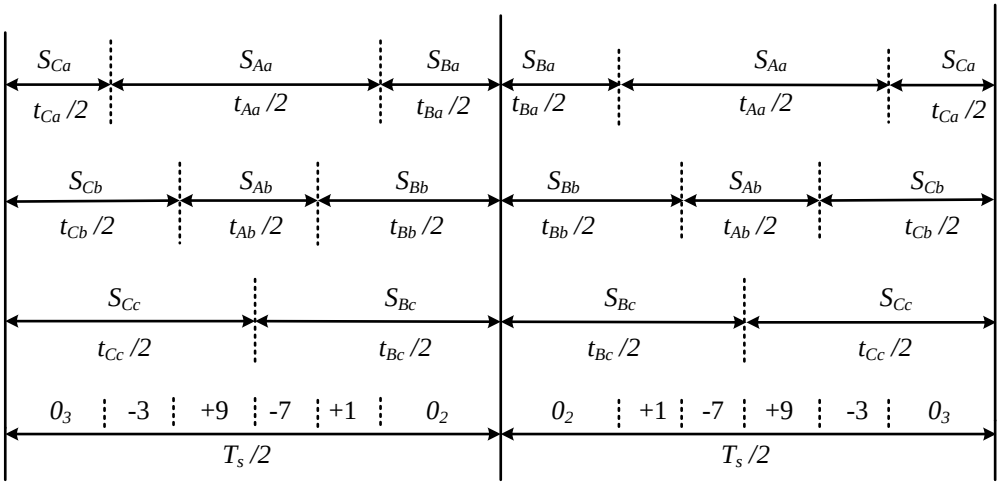


Figure 4.5: The 2-Zero-SVM switching sequence

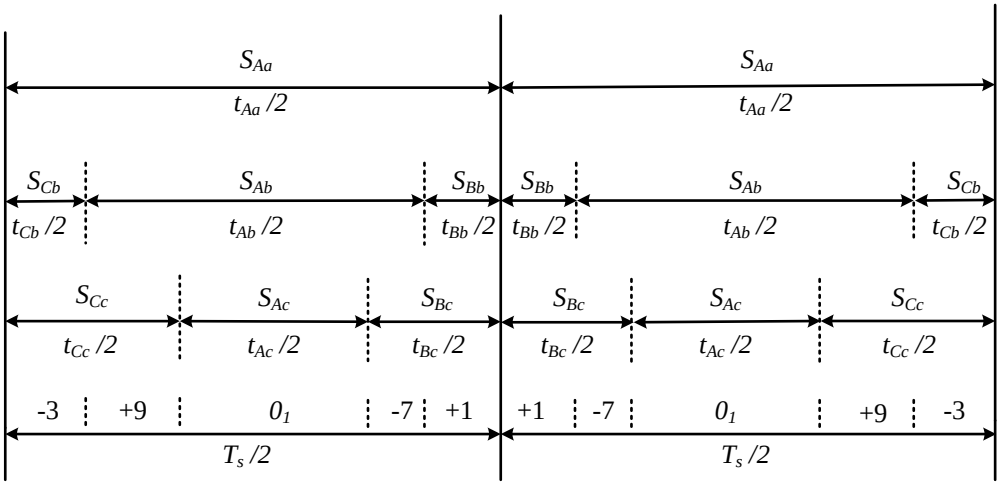


Figure 4.6: The 1-Zero-SVM switching sequence

4.2.3 Direct Matrix Converter SVM Strategy Duty Cycle Calculation

This section discusses how to calculate the duty cycle of each applied vector. Assume that now the input-output sector combination is 1-1. Define $\bar{\alpha_o} = \alpha_o - \pi/6$. $\bar{\alpha_o}$ is the angle between the output reference voltage and the bisecting line of each output voltage sector. From Figure 4.7, the output reference voltage vector V_0 can be divided into two vectors as presented in V_{01} and V_{02}.

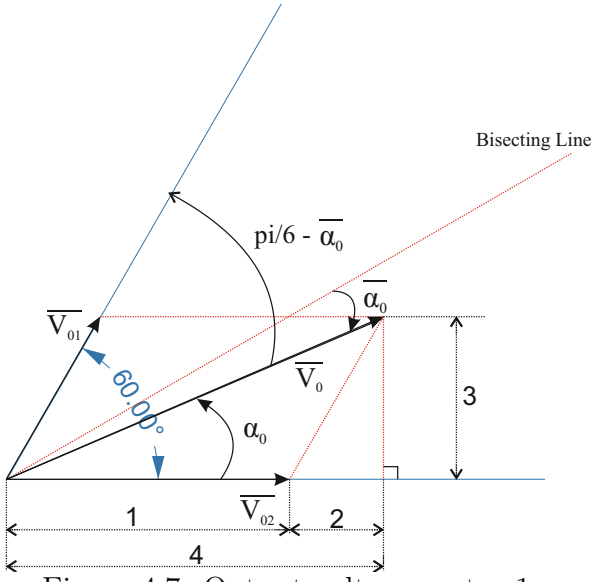


Figure 4.7: Output voltage vector 1

From the figure 4.7, we calculate the length of 1,2,3, and 4 as shown from Equation 4.2 to 4.5.

$$\text{length}_4 = |V_o| * \cos(\alpha_o) = |V_o| * \cos(\bar{\alpha_o} + \pi/6) \tag{4.2}$$

$$\text{length}_3 = |V_o| * \sin(\alpha_o) = |V_o| * \sin(\bar{\alpha_o} + \pi/6) \tag{4.3}$$

$$\text{length}_2 = \text{length}_3/\sqrt{3} = (1/\sqrt{3}) * |V_o| * \sin(\bar{\alpha_o} + \pi/6) \tag{4.4}$$

$$\begin{aligned} \text{length}_1 &= \text{length}_4 - \text{length}_2 \\ &= |V_o| * \cos(\bar{\alpha_o} + \pi/6) - (1/\sqrt{3}) * |V_o| * \sin(\bar{\alpha_o} + \pi/6) \end{aligned} \tag{4.5}$$

Therefore, $\overline{V}_{o2}$ equals to the value of $length_1$:

$$\overline{V}_{o2} = \sqrt{1 + 1/3} * |V_o| * \sin(\bar{\alpha_o} + \pi/6 + \tan^{-1}(-\sqrt{3})) \tag{4.6}$$

Where $\tan^{-1}(-\sqrt{3})$ equals to $2 * \pi/3$. After some manipulation, $\bar{V_{o2}}$ is shown in Equation 4.7.

$$\overline{V}_{o2} = \sqrt{1 + 1/3} * |V_o| * \cos(\overline{\alpha}_o + \pi/3) \tag{4.7}$$

$\overline{V}_{o1}$ is shown in equation 4.8.

$$\overline{V}_{o1} = 2 * \text{length}_2 = 2 * (1/\sqrt{3}) * |V_o| * \sin(\overline{\alpha}_o + \pi/6) \tag{4.8}$$

After some manipulations, $\overline{V}_{o1}$ can be expressed in Equation 4.9.

$$\overline{V}_{o1} = 2 * \text{length}_2 = 2 * (1/\sqrt{3}) * |V_o| * \cos(\overline{\alpha}_o - \pi/3) \tag{4.9}$$

According to the literature written by Casadei [19], two equations can be written with reference to the output voltage vector as expressed in Equation 4.10. Assume that now the input-output sector combination is 1-1.

$$\begin{aligned} \overline{V}_{o1} &= \overline{V}_{o1}^{I} * \delta^{I} + \overline{V}_{o}^{II} * \delta^{II} \\ &= 2 * (1/\sqrt{3}) * |V_o| * \cos(\bar{\alpha_o} - \pi/3) * e^{j\pi/3} \\ \overline{V}_{o2} &= \overline{V}_{o1}^{III} * \delta^{III} + \overline{V}_{o}^{IV} * \delta^{IV} \\ &= 2 * (1/\sqrt{3}) * |V_o| * \cos(\bar{\alpha_o} + \pi/3) \end{aligned} \tag{4.10}$$

There is a $e^{j\pi/3}$ in $\bar{V_{o1}}$ because the angle of vector $\bar{V_{o1}}$ is $\pi/3$ as shown in Figure 4.7. The angle of vector $\overline{V}_{o2}$ is 0 as shown in Figure 4.7, so there is no angle term in $\overline{V}_{o2}$. When considering all the 6 output voltage sectors, the

Equation 4.10 can be generalized in equation 4.11. Where K_v is the output voltage sector number.

$$\begin{aligned} \overline{V}_{o1} &= \overline{V}_o^I * \delta^I + \overline{V}_o^{II} * \delta^{II} \\ &= 2 * (1/\sqrt{3}) * |V_o| * \cos(\bar{\alpha_o} - \pi/3) * e^{j[(K_v-1)\pi/3+\pi/3]} \\ \overline{V}_{o2} &= \overline{V}_o^{III} * \delta^{III} + \overline{V}_o^{IV} * \delta^{IV} \\ &= 2 * (1/\sqrt{3}) * |V_o| * \cos(\bar{\alpha_o} + \pi/3) * e^{j[(K_v-1)\pi/3]} \end{aligned} \tag{4.11}$$

Since the output voltage sector is 1, so two of the four selected active vectors are expressed in Equation 4.13:

$$\begin{aligned} \overline{V}_o^I &= (2/3) * V_{31} * e^{j*4*\pi/3} \\ \overline{V}_o^{II} &= (2/3) * V_{12} * e^{j*4*\pi/3} \end{aligned} \tag{4.12}$$

Then we calculate the V_{31} and V_{12} expressed in Equation 4.13 and 4.14:

$$\begin{aligned} V_{31} &= V_3 - V_1 \\ &= V_i * \cos(\alpha_i - 4 * \pi/3) - V_i * \cos(\alpha_i) \\ &= V_i * (-2 * \sin(\alpha_i - 2 * \pi/3) * \sin(-2 * \pi/3)) \\ &= \sqrt{3} * V_i * \sin(\alpha_i - 2 * \pi/3) \end{aligned} \tag{4.13}$$

$$\begin{aligned} V_{12} &= V_1 - V_2 \\ &= V_i * \cos(\alpha_i) - V_i * \cos(\alpha_i - 2 * \pi/3) \\ &= V_i * (-2 * \sin(\alpha_i - \pi/3) * \sin(\pi/3)) \\ &= -\sqrt{3} * V_i * \sin(\alpha_i - \pi/3) \end{aligned} \tag{4.14}$$

Therefore, $\overline{V}_o^I$ and $\overline{V}_o^{II}$ can be expressed in equation 4.15.

$$\begin{aligned} \overline{V}_o^I &= (2/3) * \sqrt{3} * V_i * \sin(\alpha_i - 2 * \pi/3) * e^{j*4*\pi/3} \\ \overline{V}_o^{II} &= (2/3) * (-\sqrt{3} * V_i * \sin(\alpha_i - \pi/3)) * e^{j*4*\pi/3} \end{aligned} \tag{4.15}$$

Then substitute Equation 4.15 into Equation 4.10. After some manipulation, one of the equations about duty cycle δ^I and δ^{II} can be obtained in Equation 4.16. Where q is the modulation depth V_{out}/V_{in}

$$\cos(\alpha_i - 7\pi/6) * \delta^I - \cos(\alpha_i - 5\pi/6) * \delta^{II} = -q * \cos(\bar{\alpha_o} - \pi/3) \tag{4.16}$$

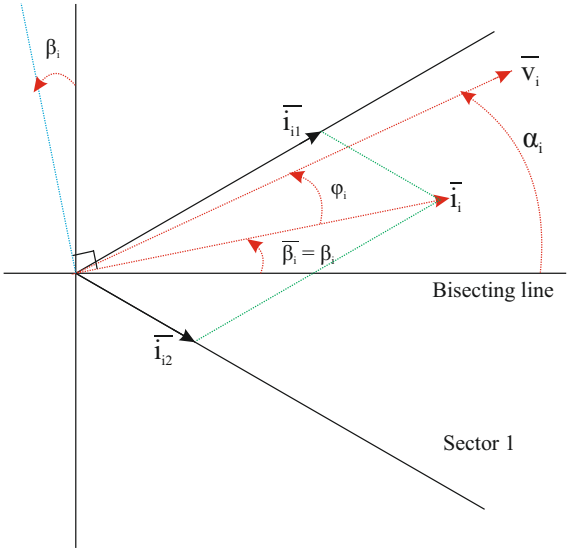


Figure 4.8: Input current vector 1

Next, try to get the other equation about duty cycle δ^I and δ^{II} , in order to solve these two active duty cycles. The input currents sector 1 is shown in figure 4.8. It can be seen from Figure 4.8 that φ_i is the input power factor angle, α_i is the input voltage vector angle, β_i is the input current vector angle, $\bar{\beta_i}$ is the angle between the input current vector and the bisecting line of each input current sector. In the input current sector 1, $\bar{\beta_i} = \beta_i$. The sum

of the two active current vectors +9 and +7 must be in the same direction as the input current vector. Also, the sum of two active current vectors +3 and +1 must be in the same direction as the input current vector. According to this, another two equations can be acquired to solve the active duty cycles. These two equations are expressed in Equation 4.17. Where K_i is the input current sector number. One thing important is that two vectors use dot product.

$$\begin{aligned}(\bar{i}_i^{I} * \delta^{I} + \bar{i}_i^{II} * \delta^{II}) \cdot je^{j\bar{\beta}_i} e^{j(K_i-1)\pi/3} = 0 \\ (\bar{i}_i^{III} * \delta^{III} + \bar{i}_i^{IV} * \delta^{IV}) \cdot je^{j\bar{\beta}_i} e^{j(K_i-1)\pi/3} = 0\end{aligned} \tag{4.17}$$

From Table 4.1, it can be see that two of four active current vectors are expressed in equation 4.18.

$$\begin{aligned}\bar{i}_i^{I} &= (2/\sqrt{3}) * i_c * e^{j7\pi/6} \\ \bar{i}_i^{II} &= (2/\sqrt{3}) * i_c * e^{-j\pi/6}\end{aligned} \tag{4.18}$$

Since in the input sector 1, we substitute Equation 4.18 into Equation 4.17, we can obtain Equation 4.19.

$$\begin{aligned}(e^{j7\pi/6} * \delta^{I} + e^{-j\pi/6} * \delta^{II}) \cdot e^{j\bar{\beta}_i + \pi/2} = 0 \\ \delta^{I} * (e^{j7\pi/6} \cdot e^{j\bar{\beta}_i + \pi/2}) + \delta^{II} * (e^{j-\pi/6} \cdot e^{j\bar{\beta}_i + \pi/2}) = 0 \\ \delta^{I} * (e^{j7\pi/6} \cdot e^{j\bar{\beta}_i + \pi/2}) = \delta^{I} * \cos(7\pi/6 - \bar{\beta}_i - \pi/2) = -\delta^{I} * \cos(\bar{\beta}_i + \pi/3) \\ \delta^{II} * (e^{j-\pi/6} \cdot e^{j\bar{\beta}_i + \pi/2}) = \delta^{II} * \cos(-\pi/6 - \bar{\beta}_i - \pi/2) = -\delta^{II} * \cos(\bar{\beta}_i - \pi/3) \\ -\delta^{I} * \cos(\bar{\beta}_i + \pi/3) - \delta^{II} * \cos(\bar{\beta}_i - \pi/3) = 0 \\ \delta^{II} = \frac{-\delta^{I} * \cos(\bar{\beta}_i + \pi/3)}{\cos(\bar{\beta}_i - \pi/3)}\end{aligned} \tag{4.19}$$

After calculating out the δ^{II} using δ^{I}, then substitute δ^{II} into equation 4.16, duty cycle δ^{I} can be calculated as shown in Equation 4.20.

$$\cos(\alpha_i - 7\pi/6) * \delta^I - \cos(\alpha_i - 5\pi/6) * (\frac{-\delta^I * \cos(\bar{\beta}_i + \pi/3)}{\cos(\bar{\beta}_i - \pi/3)}) = -q * \cos(\bar{\alpha_o} - \pi/3) \tag{4.20}$$

After some manipulation, duty cycle δ^I is calculated out in input-output sector combination 1-1 and expressed in Equation 4.21.

$$\delta^I = \frac{2}{\sqrt{3}} * q * \frac{\cos(\bar{\alpha_o} - \pi/3) * \cos(\bar{\beta}_i - \pi/3)}{\cos(\varphi_i)} \tag{4.21}$$

Finally, all the four active vector duty cycles are calculated out when considering 36 the input and output sector combination conditions. The duty cycles are presented in equation 4.22. Where K_v is the output voltage sector number and K_i is the input current sector number.

$$\begin{aligned}
\delta^I &= (-1)^{K_v+K_i} \frac{2}{\sqrt{3}} * q * \frac{\cos(\bar{\alpha_o} - \pi/3) * \cos(\bar{\beta}_i - \pi/3)}{\cos(\varphi_i)} \\
\delta^{II} &= (-1)^{K_v+K_i+1} \frac{2}{\sqrt{3}} * q * \frac{\cos(\bar{\alpha_o} - \pi/3) * \cos(\bar{\beta}_i + \pi/3)}{\cos(\varphi_i)} \\
\delta^{III} &= (-1)^{K_v+K_i+1} \frac{2}{\sqrt{3}} * q * \frac{\cos(\bar{\alpha_o} + \pi/3) * \cos(\bar{\beta}_i - \pi/3)}{cos(\varphi_i)} \\
\delta^{IV} &= (-1)^{K_v+K_i} \frac{2}{\sqrt{3}} * q * \frac{\cos(\bar{\alpha_o} + \pi/3) * \cos(\bar{\beta}_i + \pi/3)}{\cos(\varphi_i)}
\end{aligned} \tag{4.22}$$

4.3 Model Predictive Control for Direct Matrix Converters

This section will introduce the Finite Control Set Model predictive Control (FCS-MPC) strategy applied to the direct matrix converter system. In order to implement the FCS-MPC strategy onto the direct matrix converter system, a discrete-time model of the direct matrix converter is required. In addition, the discrete-time models of the input filter and the output load is required by the FCS-MPC strategy to predict the discrete-time variables in the direct matrix converter system such as the input voltages, source currents

and output currents.

4.3.1 Direct Matrix Converter Model

The direct matrix converter is comprised of nine bidirectional switches as shown in Figure 4.9. The switch state matrix M is shown in Equation 4.23. $S_{jk}(j = A, B, C; k = a, b, c.)$ represents the switching state of each bidirectional switch. $S_{jk} = 0$ means the switch S_{jk} is off and $S_{jk} = 1$ means the switch S_{jk} is on. The output voltage of the direct matrix converter is the function of the switch state matrix and the input voltage of the direct matrix converter as shown in Equation 4.24. The input current of the direct matrix converter is the function of the switch state matrix and the output current of the direct matrix converter as shown in Equation 4.25.

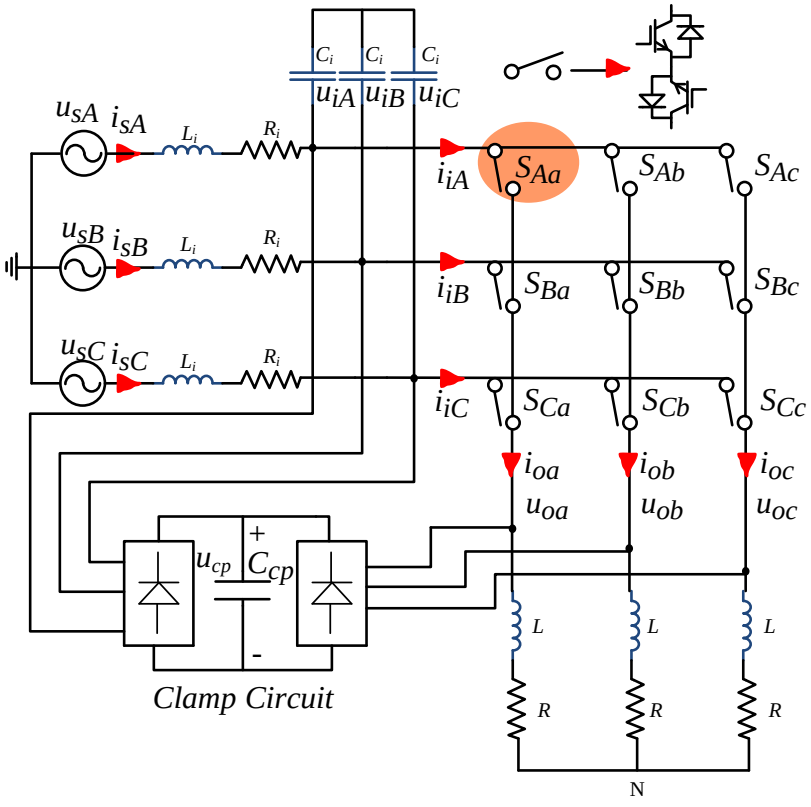


Figure 4.9: Direct matrix converter topology

$$\left[M\right] = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \tag{4.23}$$

$$\begin{bmatrix} u_{oa} \\ u_{ob} \\ u_{oc} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \cdot \begin{bmatrix} u_{iA} \\ u_{iB} \\ u_{iC} \end{bmatrix} \tag{4.24}$$

$$\begin{bmatrix} i_{iA} \\ i_{iB} \\ i_{iC} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \cdot \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} \tag{4.25}$$

During the normal operation of the direct matrix converter, the input terminals of the DMC should not be short circuited because it is fed by a voltage source. At the same time, an output phase of the DMC must never be open circuited due to the nature of inductive load. Therefore, the switch states of the nine bidirectional switches at any instant time have to satisfy the condition as presented in Equation 4.26.

$$\begin{aligned} 0 \leq m_{jk} \leq 1,\ j = A, B, C,\ k = a, b, c. \\ S_{Aa} + S_{Ba} + S_{Ca} = 1 \\ S_{Ab} + S_{Bb} + S_{Cb} = 1 \\ S_{Ac} + S_{Bc} + S_{Cc} = 1 \end{aligned} \tag{4.26}$$

Where $S_{jk}(j = A, B, C; k = a, b, c.)$ stands for the switch state of each bidirectional switch. $S_{jk} = 0$ means the switch S_{jk} is off and $S_{jk} = 1$ means the switch S_{jk} is on. Therefore, in total of 27 valid switching states satisfy the operating requirement of the direct matrix converter. The 27 valid switching states are listed in the Table 4.2.

Table 4.2: Valid switching states for the DMC with FCS-MPC strategy

	Switching configuration	Switches On
Active Vectors	$+1$	$S_{Aa}\ S_{Bb}\ S_{Bc}$
	-1	$S_{Ba}\ S_{Ab}\ S_{Ac}$
	$+2$	$S_{Ba}\ S_{Cb}\ S_{Cc}$
	-2	$S_{Ca}\ S_{Bb}\ S_{Bc}$
	$+3$	$S_{Ca}\ S_{Ab}\ S_{Ac}$
	-3	$S_{Aa}\ S_{Cb}\ S_{Cc}$
	$+4$	$S_{Ba}\ S_{Ab}\ S_{Bc}$
	-4	$S_{Aa}\ S_{Bb}\ S_{Ac}$
	$+5$	$S_{Ca}\ S_{Bb}\ S_{Cc}$
	-5	$S_{Ba}\ S_{Cb}\ S_{Bc}$
	$+6$	$S_{Aa}\ S_{Cb}\ S_{Ac}$
	-6	$S_{Ca}\ S_{Ab}\ S_{Cc}$
	$+7$	$S_{Ba}\ S_{Bb}\ S_{Ac}$
	-7	$S_{Aa}\ S_{Ab}\ S_{Bc}$
	$+8$	$S_{Ca}\ S_{Cb}\ S_{Bc}$
	-8	$S_{Ba}\ S_{Bb}\ S_{Cc}$
	$+9$	$S_{Aa}\ S_{Ab}\ S_{Cc}$
	-9	$S_{Ca}\ S_{Cb}\ S_{Ac}$
Zero Vectors	0_A	$S_{Aa}\ S_{Ab}\ S_{Ac}$
	0_B	$S_{Ba}\ S_{Bb}\ S_{Bc}$
	0_C	$S_{Ca}\ S_{Cb}\ S_{Cc}$
Rotating Vectors	$--$	$S_{Aa}\ S_{Bb}\ S_{Cc}$
	$--$	$S_{Aa}\ S_{Cb}\ S_{Bc}$
	$--$	$S_{Ba}\ S_{Ab}\ S_{Cc}$
	$--$	$S_{Ba}\ S_{Cb}\ S_{Ac}$
	$--$	$S_{Ca}\ S_{Ab}\ S_{Bc}$
	$--$	$S_{Ca}\ S_{Bb}\ S_{Ac}$

4.3.2 Input Filter Model

The input filter being discussed in this section is the LCR filter as shown in the Figure 4.9. The time-continuous model of the LCR input filter can be described by Equation 4.27.

$$\begin{aligned} L_i \frac{di_s}{dt} &= u_s - u_i - R_i i_s \\ C_i \frac{du_i}{dt} &= i_s - i_i \end{aligned} \tag{4.27}$$

Where L_i, C_i and R_i are the input filter inductance, capacitance and resistance respectively. Where u_s is the input source voltage, u_i is the direct matrix converter input voltage, and i_s is the source current. The state-space description of the input filter time-continuous model is shown in Equation 4.28.

$$\begin{bmatrix} \frac{du_i}{dt} \\ \frac{di_s}{dt} \end{bmatrix} = A \begin{bmatrix} u_i \\ i_s \end{bmatrix} + B \begin{bmatrix} u_s \\ i_i \end{bmatrix} \tag{4.28}$$

Where A and B are presented in Equation 4.29.

$$A = \begin{bmatrix} 0 & \frac{1}{C_i} \\ -\frac{1}{L_i} & -\frac{R_i}{L_i} \end{bmatrix} \qquad B = \begin{bmatrix} 0 & -\frac{1}{C_i} \\ \frac{1}{L_i} & 0 \end{bmatrix} \tag{4.29}$$

A discrete time of model of the input filter can be obtained by discretizing the time-continuous model as shown in 4.28. The input filter discrete model is shown in Equation 4.30.

$$\begin{bmatrix} u_i^{k+1} \\ i_s^{k+1} \end{bmatrix} = G \begin{bmatrix} u_i^k \\ i_s^k \end{bmatrix} + H \begin{bmatrix} u_s^k \\ i_i^k \end{bmatrix} \tag{4.30}$$

Where G and H are presented in Equation 4.31.

$$\begin{aligned} G &= e^{AT_s} \\ H &= A^{-1}(G-I)B \end{aligned} \tag{4.31}$$

By substituting Equation 4.31 into Equation 4.30, the input voltage of the direct matrix converter and the input source current can be predicted at the next sampling time point T_s^{k+1}. The predicted input voltage value of the direct matrix converter is shown in Equation 4.32. The predicted input source current value is shown in Equation 4.33. $D1 - D4$ and $E1 - E4$ are the coefficients made up to facilitate getting Equation 4.30 from Equation 4.31.

$$u_i^{k+1} = D_1 u_s^k + D_2 u_i^k + D_3 i_s^k + D_4 i_i^k \tag{4.32}$$

$$i_s^{k+1} = E_1 u_s^k + E_2 u_i^k + E_3 i_s^k + E_4 i_i^k \tag{4.33}$$

4.3.3 Output Load Model

The output load being discussed in this section is a three phase resistance-inductive load as shown in Figure 4.9. The time-continuous model of the resistance-inductive load can be described by Equation 4.34.

$$L\frac{di_o}{dt} = u_o - Ri_o \tag{4.34}$$

Where L is the load inductance and R is the load resistance. Where i_o is the load current and u_o is the output voltage. When taking sampling time T_s into consideration, the load current i_o can be discretized by a forward Euler approximation as shown in the Equation 4.35. By substituting Equation 4.36 into Equation 4.35, the output current of the direct matrix converter at the

next sampling point T_s^{k+1} time point can be predicted.

$$i_o^{k+1} = F_1 i_o^k + F_2 u_o^k \tag{4.35}$$

The F_1 and F_2 are shown in Equation 4.36.

$$\begin{aligned} F_1 &= 1 - \frac{T_s R}{L} \\ F_2 &= \frac{T_s}{L} \end{aligned} \tag{4.36}$$

4.3.4 FCS-MPC Strategy

The FCS-MPC strategy enables the controlled variables to achieve the corresponding reference at the end of each sampling time period T_s by predicting the controlled variables two steps ahead within one sampling time period T_s. The time diagram of the FCS-MPC algorithm is presented in Figure 4.10. The FCS-MPC algorithm computes the controlled variables such as the output current i_o and the input current i_s at T_s^{k+2} time point. The output current i_o^{k+2} and the input current i_s^{k+2} are calculated for every one of the 27 possible switching states. The switching state which can generate the minimum error between the predicted variable value and the reference variable will be selected as the output switching state during the next sampling period T_s.

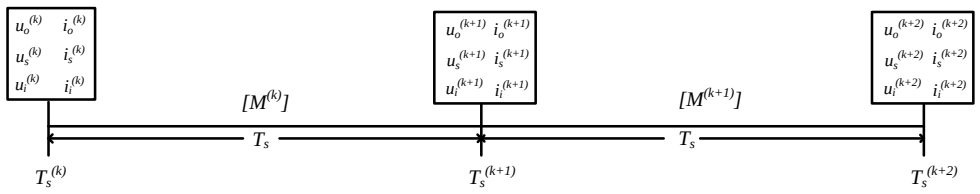


Figure 4.10: The time diagram of the FCS-MPC algorithm

The output current of the direct matrix converter i_o^k, the input voltage

u_i^k of the direct matrix converter, the input source voltage u_s^k, and the input source current i_s^k are sampled by the sensors at sampling point T_s^k. The switching state matrix $[M^k]$ represents the output states of the nine bidirectional switches. The output switching states $[M^k]$ will last for one sampling period T_s from time point T_s^k to time point T_s^{k+1}. The variables for FCS-MPC algorithm at time point T_s^k are presented in Equation 4.37.

$$\begin{cases} u_o^k = [M^k] \cdot u_i^k \\ i_o^k = \text{Sampled by sensor} \\ u_i^k = \text{Sampled by sensor} \\ u_s^k = \text{Sampled by sensor} \\ i_s^k = \text{Sampled by sensor} \\ i_i^k = [M^k] \cdot i_o^k \end{cases} \tag{4.37}$$

The output current of the direct matrix converter i_o^{k+1} can be computed by the discrete-time output resistance-inductance load model as shown in Equation 4.35. The input voltage u_i^{k+1} of the direct matrix converter and the input source current i_s^{k+1} can be predicted by the discrete-time input filter model as shown in Equation 4.32 and Equation 4.33. Therefore, the variables for FCS-MPC algorithm at time point T_s^{k+1} are presented in Equation 4.38.

$$\begin{cases} u_o^{k+1} = [M^{k+1}] \cdot u_i^{k+1} \\ i_o^{k+1} = F_1 \cdot u_o^k + F_2 \cdot i_o^k \\ u_i^{k+1} = E_1 \cdot u_s^k + E_2 \cdot u_i^k + E_3 \cdot i_s^k + E_4 \cdot i_i^k \\ u_s^{k+1} = u_s^k \\ i_s^{k+1} = D_1 \cdot u_s^k + D_2 \cdot u_i^k + D_3 \cdot i_s^k + D_4 \cdot i_i^k \\ i_i^{k+1} = [M^{k+1}] \cdot i_o^{k+1} \end{cases} \tag{4.38}$$

Next, the FCS-MPC algorithm will compute the output current i_o^{k+2} and the input current i_s^{k+2} for every one of the 27 possible switching states as shown in the Table 4.2. By substituting the Equation 4.38 into Equation 4.32 4.33 4.36, the output current i_o^{k+2} and the input current i_s^{k+2} can be

obtained as shown in Equations 4.39 and 4.40.

$$\begin{aligned} i_o^{k+2} = F_1 \cdot [M^{k+1}] \cdot u_i^{k+1} \\ +F_1 \cdot F_2 \cdot [M^k] \cdot u_i^k \\ +F_2 \cdot F_2 \cdot i_o^k \end{aligned} \tag{4.39}$$

$$\begin{aligned} i_s^{k+2} = (D_1 + D_2 \cdot E_1 + D_3 \cdot D1)u_s^k \\ +(D_2 \cdot E_2 + D_3 \cdot D_2)u_i^k \\ +(D_2 \cdot E_3 + D_3 \cdot D_3)i_s^k \\ +(D_2 \cdot E_4 + D_3 \cdot D_4)i_i^k \\ +D_4 \cdot F_1 \cdot [M^{k+1}] \cdot u_o^k \\ +D_4 \cdot F_2 \cdot [M^{k+1}] \cdot i_o^k \end{aligned} \tag{4.40}$$

The three phase source voltages u_s are shown in Equation 4.41. Where U_{sm} is the amplitude of the source voltage, and Φ is the angle of the source voltage vector $\vec{u_s}$ which can be derived from u_{sa}, u_{sb} and u_{sc}. The three phase reference output currents i_o^* is shown in Equation 4.42, where θ is the reference output current angle. The three phase reference source currents i_s^* are shown in Equation 4.43. This section considers the input power factor to be 1 so the displacement angle ψ between source voltage u_s and source current i_s is 0. Where I_{sm}^* is the amplitude of the reference source current i_s^*.

$$\begin{aligned} u_{sa} &= U_{sm}\cos(\Phi) \\ u_{sb} &= U_{sm}\cos(\Phi - \frac{2}{3}\pi) \\ u_{sc} &= U_{sm}\cos(\Phi + \frac{2}{3}\pi) \end{aligned} \tag{4.41}$$

$$\begin{aligned} i_{oa}^{*} &= I_{om}^{*}\cos(\theta) \\ i_{ob}^{*} &= I_{om}^{*}\cos(\theta - \frac{2}{3}\pi) \\ i_{oc}^{*} &= I_{om}^{*}\cos(\theta + \frac{2}{3}\pi) \end{aligned} \tag{4.42}$$

$$\begin{aligned} i_{sa}^{*} &= I_{sm}^{*}\cos(\Phi) \\ i_{sb}^{*} &= I_{sm}^{*}\cos(\Phi - \frac{2}{3}\pi) \\ i_{sc}^{*} &= I_{sm}^{*}\cos(\Phi + \frac{2}{3}\pi) \end{aligned} \tag{4.43}$$

The amplitude of the reference source current I_{sm}^{*} can be derived by the active power flow of the direct matrix converter. The input active power P_{in} can be calculated by Equation 4.44. The output active power P_{out} can be calculated by Equation 4.45. The η is the efficiency of the direct matrix converter and can be calculated by Equation 4.46.

$$P_{in} = \frac{3}{2}(U_{sm}I_{sm}\cos(\psi) - {I_{sm}^{*}}^{2}R_{i}) \tag{4.44}$$

$$P_{out} = \frac{3}{2}{I_{om}^{*}}^{2}R \tag{4.45}$$

$$\eta = \frac{P_{out}}{P_{in}} \tag{4.46}$$

According to Equation 4.45 4.44 4.46, the amplitude of the reference source current I_{sm}^{*} can be calculated by Equation 4.47.

$$I_{sm}^{*} = \frac{-\eta U_{sm} \pm \sqrt{(\eta U_{sm})^2 - 4\eta R_i {I_{om}^{*}}^2 R}}{-2\eta R_i} \tag{4.47}$$

4.3.5 FCS-MPC Algorithm Cost Function

The three phase voltage and current vectors are transformed by using an $\alpha - \beta$ linear transformation as shown in Equation 4.48. Where $[V_a\ V_b\ V_c]^T$ is the three phase voltage or three phase current vector, and $[V_\alpha\ V_\beta]^T$ is the $\alpha - \beta$ coordinate vector.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.48}$$

In FCS-MPC algorithm, the cost function is a function that the algorithm wants to minimize. This is often represented as the difference between the demand and the algorithm's output. The cost function of the FCS-MPC can be defined in different format depending on the control priority of the controlled variables. One way to define the cost function of the FCS-MPC for the direct matrix converter is based on errors of the output current $i_{o\alpha\beta}$ and the source current $i_{s\alpha\beta}$. The err_o is the error between the real output current value $i_{o\alpha\beta}$ and the reference output current value $i_{o\alpha\beta}^{*}$. The err_s is the error between the real input source current value $i_{s\alpha\beta}$ and the reference source current value $i_{s\alpha\beta}^{*}$. The error err_o is calculated by Equation 4.49 and err_s is calculated by Equation 4.50.

$$err_o = i_{o\alpha\beta}^{*} - i_{o\alpha\beta} \tag{4.49}$$

$$err_s = i_{s\alpha\beta}^{*} - i_{s\alpha\beta} \tag{4.50}$$

The cost function g of the FCS-MPC algorithm is defined by Equation 4.51. The weighting factor λ in the cost function g is empirically tuned according to [74].

$$g = err_o + \lambda \cdot err_s \tag{4.51}$$

At the beginning, the weighting factor λ is set to 0, The output load current will be given priority at the cost of highly distorted input source current. Next, the weighting factor λ is tuned in order to achieve unity input power factor. At the same time, the output current needs to maintain good performance. Finally, The cost functions of all the 27 possible switching states will be calculated during each sampling period T_s. The 27 possible switching states will generate 27 cost function values $g^{k+2}[i]$ at the time point T_s^{k+2}. The switching state $[M^{k+1}]$ which has the minimum $g^{k+2}[i]$ will be chosen during the next sampling period as shown in Equation 4.52.

$$g[M^{k+1}] = \min\{g^{k+2}[i]\}, \qquad i = 1, 2, ..., 27. \tag{4.52}$$

4.4 Model Predictive Control for Indirect Matrix Converters

The indirect matrix converter is comprised of a rectifier stage and an inverter stage as well as a fictitious DC-Link as shown in Figure 4.11. The rectifier stage switching state matrix $M_{rectifier}$ is shown in Equation 4.53. $S_{rj}(j = 1, 2, ..., 6.)$ means the switching state of the rectifier switches. The inverter stage switching state matrix $M_{inverter}$ is shown in Equation 4.54. $S_{ij}(j = 1, 2, ..., 6.)$ means the switching state of the inverter switches. $S_{rj} = 0$ means the switch S_{rj} is off and $S_{rj} = 1$ means the switch S_{rj} is on. The same rule applies on the inverter switches.

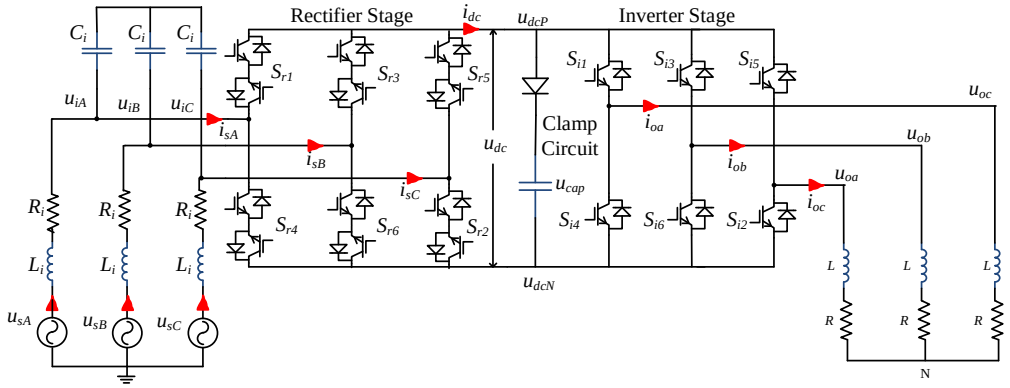


Figure 4.11: Indirect matrix converter topology

$$\left[M_{rectifier}\right] = \begin{bmatrix} S_{r1} & S_{r3} & S_{r5} \\ S_{r4} & S_{r6} & S_{r2} \end{bmatrix} \tag{4.53}$$

$$\left[M_{inverter}\right] = \begin{bmatrix} S_{i1} & S_{i3} & S_{i5} \\ S_{i4} & S_{i6} & S_{i2} \end{bmatrix} \tag{4.54}$$

4.4.1 Indirect Matrix Converter Model

For the rectifier stage, The fictitious DC-Link voltage u_{dc} is acquired as a function of the input voltages u_s and the rectifier stage switching states as shown in Equation 4.55. The input current i_s is obtained as a function of the fictitious DC-Link current i_{dc} and the rectifier stage switching states as shown in Equation 4.56.

$$u_{dc} = [S_{r1} - S_{r4} \quad S_{r3} - S_{r6} \quad S_{r5} - S_{r2}]u_s \tag{4.55}$$

$$i_s = \begin{bmatrix} S_{r1} - S_{r4} \\ S_{r3} - S_{r6} \\ S_{r5} - S_{r2} \end{bmatrix} i_{dc} \tag{4.56}$$

For the inverter stage, the output voltage u_o is acquired as a function of the fictitious Dc-Link voltage u_{dc} and the inverter stage switching states as shown in Equation 4.57. The fictitious DC-Link current i_{dc} is obtained as a function of the output current i_o and the inverter stage switching states as shown in Equation 4.58.

$$u_o = \begin{bmatrix} S_{i1} - S_{i4} \\ S_{i3} - S_{i6} \\ S_{i5} - S_{i2} \end{bmatrix} u_{dc} \tag{4.57}$$

$$i_{dc} = [S_{i1} \quad S_{i3} \quad S_{i5}] i_o \tag{4.58}$$

4.4.2 Input Filter Model

The input filter being discussed in this section is the LCR filter as shown in the Figure 4.11. The input filter discrete time model in the indirect matrix converter is exactly the same as the one in the direct matrix converter as shown in Equation 4.59. Where G and H are presented in Equation 4.60.

$$\begin{bmatrix} u_i^{k+1} \\ i_s^{k+1} \end{bmatrix} = G \begin{bmatrix} u_i^k \\ i_s^k \end{bmatrix} + H \begin{bmatrix} u_s^k \\ i_i^k \end{bmatrix} \tag{4.59}$$

$$\begin{aligned} G &= e^{AT_s} \\ H &= A^{-1}(G - I)B \end{aligned} \tag{4.60}$$

By substituting Equation 4.60 into Equation 4.59, the input voltage of the indirect matrix converter and the input source current can be predicted at the next sampling time point T_s^{k+1}. The predicted input voltage value of the indirect matrix converter is shown in Equation 4.61. The predicted input source current value is shown in Equation 4.62.

$$u_i^{k+1} = D_1 u_s^k + D_2 u_i^k + D_3 i_s^k + D_4 i_i^k \tag{4.61}$$

$$i_s^{k+1} = E_1 u_s^k + E_2 u_i^k + E_3 i_s^k + E_4 i_i^k \tag{4.62}$$

4.4.3 Output Load Model

The output load being discussed in this section is a three phase resistance-inductive load as shown in Figure 4.11. The output load discrete time model in the indirect matrix converter is exactly the same as the one in the direct matrix converter as shown in Equation 4.63. The F_1 and F_2 are shown in Equation 4.64.

$$i_o^{k+1} = F_1 i_o^k + F_2 u_o^k \tag{4.63}$$

$$\begin{aligned} F_1 &= 1 - \frac{T_s R}{L} \\ F_2 &= \frac{T_s}{L} \end{aligned} \tag{4.64}$$

4.4.4 FCS-MPC Strategy

The time diagram of the FCS-MPC algorithm is presented in Figure 4.12. It can be seen from the time diagram that the indirect matrix converter FCS-MPC algorithm is very similar to that of the direct matrix converter FCS-MPC algorithm. The slight difference in the indirect matrix converter system is that the fictitious DC-Link voltage u_{dc} and current i_{dc} have to be calculated by the FCS-MPC algorithm.

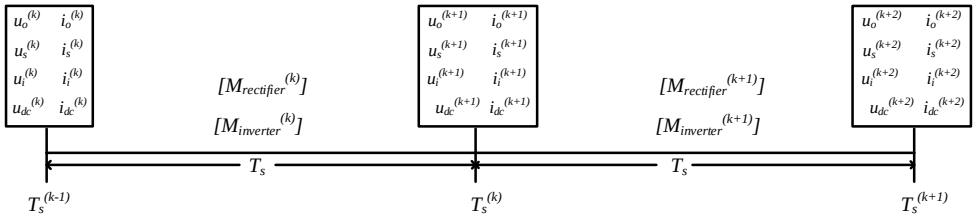


Figure 4.12: The time diagram of the FCS-MPC algorithm

The fictitious DC-Link voltage ${u_{dc}}^k$ at sampling point ${T_s}^k$ is calculated by Equation 4.65. The fictitious DC-Link current ${i_{dc}}^k$ at sampling point ${T_s}^k$ is calculated by Equation 4.66. The fictitious DC-Link voltage ${u_{dc}}^{k+1}$ at sampling point ${T_s}^{k+1}$ is calculated by Equation 4.67. The fictitious DC-Link current ${i_{dc}}^{k+1}$ at sampling point ${T_s}^{k+1}$ is calculated by Equation 4.68.

$$ {u_{dc}}^k = [{M_{rectifier}}^k]{u_s}^k \tag{4.65} $$

$$ {i_{dc}}^k = [{M_{inverter}}^k]{i_o}^k \tag{4.66} $$

$$ {u_{dc}}^{k+1} = [{M_{rectifier}}^{k+1}]{u_s}^{k+1} \tag{4.67} $$

$$ {i_{dc}}^{k+1} = [{M_{inverter}}^{k+1}]{i_o}^{k+1} \tag{4.68} $$

The switching state $[M_{rectifier}]$ and the corresponding input current i_i and the DC-Link voltage u_{dc} for the fictitious rectifier stage in the indirect matrix converter is shown in Table 4.3.

Table 4.3: Switching states in the fictitious rectifier stage

	S_{r1}	S_{r2}	S_{r3}	S_{r4}	S_{r5}	S_{r6}	i_{iA}	i_{iB}	i_{iC}	u_{dc}
1	1	1	0	0	0	0	i_{dc}	0	$-i_{dc}$	u_{AC}
2	0	1	1	0	0	0	0	i_{dc}	$-i_{dc}$	u_{BC}
3	0	0	1	1	0	0	$-i_{dc}$	i_{dc}	0	$-u_{AB}$
4	0	0	0	1	1	0	$-i_{dc}$	0	i_{dc}	$-u_{AC}$
5	0	0	0	0	1	1	0	$-i_{dc}$	i_{dc}	$-u_{BC}$
6	1	0	0	0	0	1	i_{dc}	$-i_{dc}$	0	$-u_{BC}$
7	1	0	0	1	0	0	0	0	0	0
8	0	1	0	0	1	0	0	0	0	0
9	0	0	1	0	0	1	0	0	0	0

The switching state $[M_{inverter}]$ and the corresponding line-to-line output voltage u_{ojk} and the DC-Link current i_{dc} for the fictitious inverter stage in the indirect matrix converter is shown in Table 4.4.

Table 4.4: Switching states in the fictitious inverter stage

	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}	u_{oab}	u_{obc}	u_{oca}	i_{dc}
1	1	1	0	0	0	1	u_{dc}	0	$-u_{dc}$	i_{oa}
2	1	1	1	0	0	0	0	u_{dc}	$-u_{dc}$	$i_{oa}+i_{ob}$
3	0	1	1	1	0	0	$-u_{dc}$	u_{dc}	0	i_{ob}
4	0	0	1	1	1	0	$-u_{dc}$	0	u_{dc}	$i_{ob}+i_{oc}$
5	0	0	0	1	1	1	0	$-u_{dc}$	u_{dc}	i_{oc}
6	1	0	0	0	1	1	u_{dc}	$-u_{dc}$	0	$i_{oa}+i_{oc}$
7	1	0	1	0	1	0	0	0	0	0
8	0	1	0	1	0	1	0	0	0	0

From the Table 4.3 and 4.4, it can be seen that there are 9 different switching states in the rectifier stage and there are 8 different switching stages in the inverter stage. However, the output voltage of the rectifier stage has to be positive all the time in order to maintain DC voltage at the fictitious DC-Link. Therefore, at any instant time, only 3 different switching states are qualified to select at the rectifier stage. Considering this restriction, only 24 switching states are qualified to select for the indirect matrix converter system.

4.4.5 Comparison between SVM and FCS-MPC

One advantage of the SVM algorithm is that the switching frequency is fixed, so it is easier to design a filter for SVM algorithm than the FCS-MPC algorithm because the switching frequency of FCS-MPC is not fixed. The applied switching state in each FCS-MPC sampling period is decided only by the cost function. Therefore, there is no fixed switching frequency in FCS-MPC. Another advantage of the SVM algorithm is that it requires less number of DSP instructions than the FCS-MPC algorithm. This is because FCS-MPC algorithm has to calculate the cost-function for each possible switching states and then select the optimum one. However, one disadvantage of the SVM algorithm is that the duty cycle concept is more difficult to understand than the FCS-MPC algorithm [75].

The advantage of the FCS-MPC algorithm is that the duty cycle concept is very easy to understand. However, the disadvantage of the FCS-MPC algorithm is that it is sensitive to the input filter and output load parameters, causing the selection of weighting factor used in the FCS-MPC algorithm time-consuming [75]. The aim of the comparison between FCS-MPC and SVM is to show the advantages and weakness clearly, which could be a helpful guidance when selecting a suitable modulation or control strategy in a specific application.

4.5 Summary

This Chapter introduces the SVM strategy on the direct matrix converter system, and the FCS-MPC strategy on the direct and indirect matrix converter systems. The SVM algorithm and the FCS-MPC algorithm are discussed in detail in this chapter.

Chapter 5

Fault Detection and Diagnosis Strategies in Matrix Converter Systems

5.1 Introduction

This chapter introduces single switch open circuit fault detection and diagnosis strategies applied to the direct and indirect matrix converter systems. These fault detection and diagnosis algorithms are developed based on the fault behaviour analysis discussed in the beginning of this chapter.

The fault detection and diagnosis algorithm will monitor the matrix converter system in real time by using sensors such as voltage sensors and current sensors. The speed and the precision of the fault detection and diagnosis algorithm depends on the precision and the location of the sensors. Taking the current sensor for example, the bandwidth of the current sensor should be designed to be able to detect the current change as soon as possible. Meanwhile, the bandwidth should not be designed too high because more noise will be sampled by a high bandwidth current sensor.

The location of the sensors is also very important for the fault detection and diagnosis algorithm. The voltage and current behaviour will be different in different system locations under an open circuit switch fault. Therefore,

the location of the sensors is essential for the fault detection and diagnosis system to capture the open circuit switch faulty behaviour fast and precisely.

When designing a fault detection and diagnosis system, the designer should avoid to add too much hardware complexity such as using too many additional sensors to monitor the system behaviour. An ideal direct matrix converter fault detection and diagnosis system should successfully detect and locate an open circuit switch fault with minimized number of additional sensors.

The direct matrix converter fault detection and diagnosis strategy proposed in this chapter will use no additional hardware sensor. For the indirect matrix converter system, the proposed fault detection and diagnosis strategy in this chapter will use two additional voltage sensors due to the two-stage operation nature of the indirect matrix converter system.

5.2 Open Circuit Fault behaviour Analysis for Direct Matrix Converters

If bidirectional switch open circuit fault occurs in the direct matrix converter, the faulty phase current will first recirculate in the clamp circuit. The current recirculating path is decided by three factors. The three factors are the direction and amplitude of faulty phase current, the input source voltages and the switching states, respectively. The following section will investigate the open circuit fault behaviour for direct matrix converter by giving a detailed mathematical model.

5.2.1 Mathematical Model of Open Circuit Fault behaviour for Direct Matrix Converters

In order to develop a detailed mathematical model of the open circuit fault behaviour for direct matrix converters, the DMC system current, voltage and switch state variables are defined as shown in Fig 5.1. The red arrows defines the positive direction of the corresponding current variables. In order

to simplify the mathematical model, the RLC input filter is not considered.

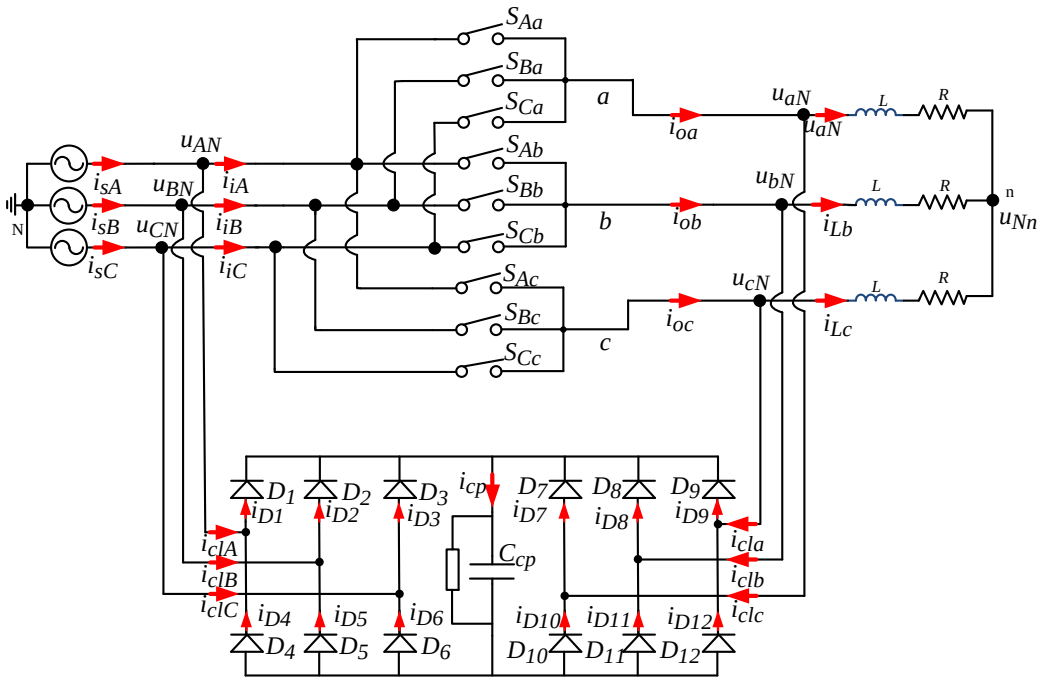


Figure 5.1: DMC open circuit fault behaviour model variables

The source currents i_{sABC}, DMC input currents i_{iABC} and clamp circuit input currents i_{clABC} satisfy the KCL rule as shown in equation 5.1.

$$\begin{aligned} i_{sA} &= i_{iA} + i_{clA} \\ i_{sB} &= i_{iB} + i_{clB} \\ i_{sC} &= i_{iC} + i_{clC} \end{aligned} \tag{5.1}$$

The DMC output currents i_{oabc}, load currents i_{Labc} and clamp circuit outputput currents i_{clabc} satisfy the KCL rule as shown in equation 5.2.

$$\begin{aligned} i_{oa} &= i_{La} + i_{cla} \\ i_{ob} &= i_{Lb} + i_{clb} \\ i_{oc} &= i_{Lc} + i_{clc} \end{aligned} \tag{5.2}$$

The three phase balanced R-L load model can be described in equation 5.3.

$$\begin{aligned} L\frac{di_{La}}{dt} + i_{La} \cdot R &= u_{aN} - u_{nN} \\ L\frac{di_{Lb}}{dt} + i_{Lb} \cdot R &= u_{bN} - u_{nN} \\ L\frac{di_{Lc}}{dt} + i_{Lc} \cdot R &= u_{cN} - u_{nN} \end{aligned} \tag{5.3}$$

The DMC switch model can be described in equation 5.4.

$$\begin{aligned} u_{abc} &= [S_{jk}]u_{ABC} \\ i_{ABC} &= [S_{jk}]^T i_{abc} \\ j &= A, B, C \\ k &= a, b, c \end{aligned} \tag{5.4}$$

The clamp circuit model can be described by the diode state matrix M_{clamp} as shown in equation 5.5. $D_i = 0$ means the corresponding diode is not conducting and $D_i = 1$ means the corresponding diode is conducting.

$$M_{clamp} = \begin{bmatrix} D_1 & D_2 & D_3 & D_7 & D_8 & D_9 \\ D_4 & D_5 & D_6 & D_{10} & D_{11} & D_{12} \end{bmatrix} \tag{5.5}$$

The sign function $sgn()$ is used in order to get the direction of the currents.

When DMC output phase a occurs an open circuit fault, diode state D_7 can be described in equation 5.6, and diode state D_{10} can be described in equation 5.7.

$$D_7 = \begin{cases} sgn(i_{cla}) & i_{cla} > 0 \\ 1 + sgn(i_{cla}) & i_{cla} < 0 \end{cases} \tag{5.6}$$

$$D_{10} = \begin{cases} -sgn(i_{cla}) & i_{cla} < 0 \\ 1 - sgn(i_{cla}) & i_{cla} > 0 \end{cases} \tag{5.7}$$

When DMC output phase b occurs an open circuit fault, diode state D_8 can be described in equation 5.8, and diode state D_{11} can be described in equation 5.9.

$$D_8 = \begin{cases} sgn(i_{clb}) & i_{clb} > 0 \\ 1 + sgn(i_{clb}) & i_{clb} < 0 \end{cases} \tag{5.8}$$

$$D_{11} = \begin{cases} -sgn(i_{clb}) & i_{clb} < 0 \\ 1 - sgn(i_{clb}) & i_{clb} > 0 \end{cases} \tag{5.9}$$

When DMC output phase c occurs an open circuit fault, diode state D_9 can be described in equation 5.10, and diode state D_{12} can be described in equation 5.11.

$$D_9 = \begin{cases} sgn(i_{clc}) & i_{clc} > 0 \\ 1 + sgn(i_{clc}) & i_{clc} < 0 \end{cases} \tag{5.10}$$

$$D_{12} = \begin{cases} -sgn(i_{clc}) & i_{clc} < 0 \\ 1 - sgn(i_{clc}) & i_{clc} > 0 \end{cases} \tag{5.11}$$

The clamp circuit upper six diodes state matrix Cl_{upper} is described in equation 5.12 and the bottom six diodes state matrix Cl_{bottom} is described in equation 5.13.

$$Cl_{upper} = \begin{bmatrix} D_1 & D_2 & D_3 & D_7 & D_8 & D_9 \end{bmatrix} \tag{5.12}$$

$$Cl_{bottom} = \begin{bmatrix} D_4 & D_5 & D_6 & D_{10} & D_{11} & D_{12} \end{bmatrix} \tag{5.13}$$

There are 3 situations for the diodes state matrix Cl_{upper} and 3 situations for the diodes state matrix Cl_{bottom}.These 6 situations are described in equation 5.14.

$$\begin{aligned}
\{D_1\ D_2\ D_3\ D_7\ D_8\ D_9\} &= \{0\ 0\ 0\ 1\ 0\ 0\} \\
\{D_1\ D_2\ D_3\ D_7\ D_8\ D_9\} &= \{0\ 0\ 0\ 0\ 1\ 0\} \\
\{D_1\ D_2\ D_3\ D_7\ D_8\ D_9\} &= \{0\ 0\ 0\ 0\ 0\ 1\} \\
\{D_4\ D_5\ D_6\ D_{10}\ D_{11}\ D_{12}\} &= \{0\ 0\ 0\ 1\ 0\ 0\} \\
\{D_4\ D_5\ D_6\ D_{10}\ D_{11}\ D_{12}\} &= \{0\ 0\ 0\ 0\ 1\ 0\} \\
\{D_4\ D_5\ D_6\ D_{10}\ D_{11}\ D_{12}\} &= \{0\ 0\ 0\ 0\ 0\ 1\}
\end{aligned} \tag{5.14}$$

When $\{D_1\ D_2\ D_3\ D_7\ D_8\ D_9\} = \{0\ 0\ 0\ 1\ 0\ 0\}$, we need to calculate the bottom six diodes state matrix Cl_{bottom}, which is $\{D_4\ D_5\ D_6\ D_{11}\ D_{12}\}$. The diode state D_{10} is not in the matrix Cl_{bottom} because $D_7 = 1$.

The switch voltage drop factor is ignored in order to simplify the analysis. The switch voltage drop factor will be considered at the end of this section. By ignoring the switch voltage drop, it can be seen that $u_{abc} = \{S_{jk}\}u_{ABC}$.

$D_7 = 1$ means that clamp circuit diode D_7 is conducting, so the diodes state matrix Cl_{bottom} can be described in equation 5.15.

$$\{D_4\ D_5\ D_6\ D_{11}\ D_{12}\} = \begin{cases} \{1\ 0\ 0\ S_{Ab}\ S_{Ac}\} & if\ min(u_A, u_B, u_C) = u_A \\ \{0\ 1\ 0\ S_{Bb}\ S_{Bc}\} & if\ min(u_A, u_B, u_C) = u_B \\ \{0\ 0\ 1\ S_{Cb}\ S_{Cc}\} & if\ min(u_A, u_B, u_C) = u_C \end{cases} \tag{5.15}$$

When $\{D_1\ D_2\ D_3\ D_7\ D_8\ D_9\} = \{0\ 0\ 0\ 0\ 1\ 0\}$, we need to calculate the bottom six diodes state matrix Cl_{bottom}, which is $\{D_4\ D_5\ D_6\ D_{10}\ D_{12}\}$. The diode state D_{11} is not in the matrix Cl_{bottom} because $D_8 = 1$.

$D_8 = 1$ means that clamp circuit diode D_8 is conducting, so the diodes state matrix Cl_{bottom} can be described in equation 5.16.

$$\{D_4\ D_5\ D_6\ D_{10}\ D_{12}\} = \begin{cases} \{1\ 0\ 0\ S_{Aa}\ S_{Ac}\} & if\ min(u_A, u_B, u_C) = u_A \\ \{0\ 1\ 0\ S_{Ba}\ S_{Bc}\} & if\ min(u_A, u_B, u_C) = u_B \\ \{0\ 0\ 1\ S_{Ca}\ S_{Cc}\} & if\ min(u_A, u_B, u_C) = u_C \end{cases} \tag{5.16}$$

When $\{D_1\ D_2\ D_3\ D_7\ D_8\ D_9\} = \{0\ 0\ 0\ 0\ 0\ 1\}$, we need to calculate the bottom six diodes state matrix Cl_{bottom}, which is $\{D_4\ D_5\ D_6\ D_{10}\ D_{11}\}$. The diode state D_{12} is not in the matrix Cl_{bottom} because $D_9 = 1$.

$D_9 = 1$ means that clamp circuit diode D_9 is conducting, so the diodes state matrix Cl_{bottom} can be described in equation 5.17.

$$\{D_4\ D_5\ D_6\ D_{10}\ D_{11}\} = \begin{cases} \{1\ 0\ 0\ S_{Aa}\ S_{Ab}\} & if\ min(u_A, u_B, u_C) = u_A \\ \{0\ 1\ 0\ S_{Ba}\ S_{Bb}\} & if\ min(u_A, u_B, u_C) = u_B \\ \{0\ 0\ 1\ S_{Ca}\ S_{Cb}\} & if\ min(u_A, u_B, u_C) = u_C \end{cases} \tag{5.17}$$

When $\{D_4\ D_5\ D_6\ D_{10}\ D_{11}\ D_{12}\} = \{0\ 0\ 0\ 1\ 0\ 0\}$, we need to calculate the upper six diodes state matrix Cl_{upper}, which is $\{D_1\ D_2\ D_3\ D_8\ D_9\}$. The diode state D_7 is not in the matrix Cl_{upper} because $D_{10} = 1$.

$D_{10} = 1$ means that clamp circuit diode D_{10} is conducting, so the diodes state matrix Cl_{upper} can be described in equation 5.18.

$$\{D_1\ D_2\ D_3\ D_8\ D_9\} = \begin{cases} \{1\ 0\ 0\ S_{Ab}\ S_{Ac}\} & if\ min(u_A, u_B, u_C) = u_A \\ \{0\ 1\ 0\ S_{Bb}\ S_{Bc}\} & if\ min(u_A, u_B, u_C) = u_B \\ \{0\ 0\ 1\ S_{Cb}\ S_{Cc}\} & if\ min(u_A, u_B, u_C) = u_C \end{cases} \tag{5.18}$$

When $\{D_4\ D_5\ D_6\ D_{10}\ D_{11}\ D_{12}\} = \{0\ 0\ 0\ 0\ 1\ 0\}$, we need to calculate the upper six diodes state matrix Cl_{upper}, which is $\{D_1\ D_2\ D_3\ D_7\ D_9\}$. The diode state D_8 is not in the matrix Cl_{upper} because $D_{11} = 1$.

$D_{11} = 1$ means that clamp circuit diode D_{11} is conducting, so the diodes state matrix Cl_{upper} can be described in equation 5.19.

$$\{D_1\ D_2\ D_3\ D_7\ D_9\} = \begin{cases} \{1\ 0\ 0\ S_{Aa}\ S_{Ac}\} & if\ min(u_A, u_B, u_C) = u_A \\ \{0\ 1\ 0\ S_{Ba}\ S_{Bc}\} & if\ min(u_A, u_B, u_C) = u_B \\ \{0\ 0\ 1\ S_{Ca}\ S_{Cc}\} & if\ min(u_A, u_B, u_C) = u_C \end{cases} \tag{5.19}$$

When $\{D_4\ D_5\ D_6\ D_{10}\ D_{11}\ D_{12}\} = \{0\ 0\ 0\ 0\ 0\ 1\}$, we need to calculate

the upper six diodes state matrix Cl_{upper}, which is $\{D_1\ D_2\ D_3\ D_7\ D_8\}$. The diode state D_9 is not in the matrix Cl_{upper} because $D_{12} = 1$.

$D_{12} = 1$ means that clamp circuit diode D_{12} is conducting, so the diodes state matrix Cl_{upper} can be described in equation 5.20.

$$\{D_1\ D_2\ D_3\ D_7\ D_8\} = \begin{cases} \{1\ 0\ 0\ S_{Aa}\ S_{Ab}\} & if\ min(u_A, u_B, u_C) = u_A \\ \{0\ 1\ 0\ S_{Ba}\ S_{Bb}\} & if\ min(u_A, u_B, u_C) = u_B \\ \{0\ 0\ 1\ S_{Ca}\ S_{Cb}\} & if\ min(u_A, u_B, u_C) = u_C \end{cases} \tag{5.20}$$

When considering the switch voltage drop, the voltage drop for 9 bidirecitonal switches can be represented by a switch voltage drop matrix $[V_{djk}]$ as shown in equation 5.21. We can assume a bidirectional switch has a constant voltage drop value V_{drop}. The direction of the voltage drop depends on the direction of the output current.

$$\Big[[V_{djk}]\Big] = V_{drop} \cdot \begin{bmatrix} sgn(i_a)S_{Aa} & sgn(i_b)S_{Ab} & sgn(i_c)S_{Ac} \\ sgn(i_a)S_{Ba} & sgn(i_b)S_{Bb} & sgn(i_c)S_{Bc} \\ sgn(i_a)S_{Ca} & sgn(i_b)S_{Cb} & sgn(i_c)S_{Cc} \end{bmatrix} \tag{5.21}$$

The switch voltage drop will not have an obvious influence on the clamp circuit model when the operating point voltage is big enough to ignore the switch voltage drop. The switch voltage drop will have an obvious influence on the clamp circuit model when the operating point voltage is low.

5.2.2 DMC Current Recirculating Analysis Under Single Switch Open Circuit Fault Condition

It is of significant importance to know how current will recirculate in the clamp circuit during an open circuit fault condition. The currents recirculating information is essential to improve the speed and precision of the output-current-based fault diagnosis methods, because the faulty output phase current will affect the currents of the healthy output phases by current recir-

culating and causes false-diagnosis in the fault diagnosis process eventually. According to the open circuit fault behaviour model developed in the previous section, when a bidirectional switch has an open circuit fault, the load current of the faulty output phase will recirculate through the clamp circuit. Then the recirculating current in the clamp circuit will either flow back to other phases of the load, or flow into the input source, DMC and then back to the load. The specific current recirculating path is decided by three factors. These three factors are the load current direction, the switching state, and the input voltages. There are two types of current recirculating paths that the faulty output phase load current can flow through. The type 1 current recirculating path means that the faulty output phase load current will flow through the clamp circuit, the input source, the DMC and finally flow back to other phases of the load. In a type 1 path, there are still currents flowing through the DMC output side. The type 2 current recirculating path means that the faulty output phase load current is the biggest absolute value among the three output load currents, and will flow through the clamp circuit and then flow back to other phases of the load directly. The key difference between type 1 path and type 2 path is the current difference of the healthy phases of the DMC output. Both of the currents of the healthy phases of the DMC output will not be zero in type 1 path. However, at least one current of the healthy phases of the DMC output will be zero in type 2 path.

5.2.3 Type 1 Current Recirculating Path

The type 1 current recirculating path under these specific conditions is shown in Fig 5.2. Type 1 current recirculating path includes the faulty phase of the load, the clamp circuit, the input source, the DMC and other phases of the load. Moreover, both of the currents of the healthy phases of the DMC output will not be zero in type 1 path. For instance, the bidirectional switch S_{Aa} occurs an open circuit fault at the time point t_k. The three phase input voltages at t_k are $u_{iA} = -48V$, $u_{iB} = +38V$ and $u_{iC} = +9V$, respectively. The faulty output phase current i_{oa} is flowing from the load, and the healthy output phases currents i_{ob} and i_{oc} are flowing into the load. The bidirectional

switches which are conducting at t_k are S_{Aa}, S_{Cb} and S_{Cc}, respectively. Under these conditions, the faulty output phase current i_{oa} will first flow into the clamp capacitor C_{cp} through diode D_7. Then the current will continue to flow through the diode D_4 because the diode D_4 is connecting to the most negative input voltage, as well as the nature of the diode bridge. Next, the current will continue to flow through the input voltage sources U_{sA}, U_{sC} and through the DMC due to the switching state condition. Finally, the current will flow back into the load phases b and c and create a complete current recirculating path for the faulty output phase current i_{oa}.

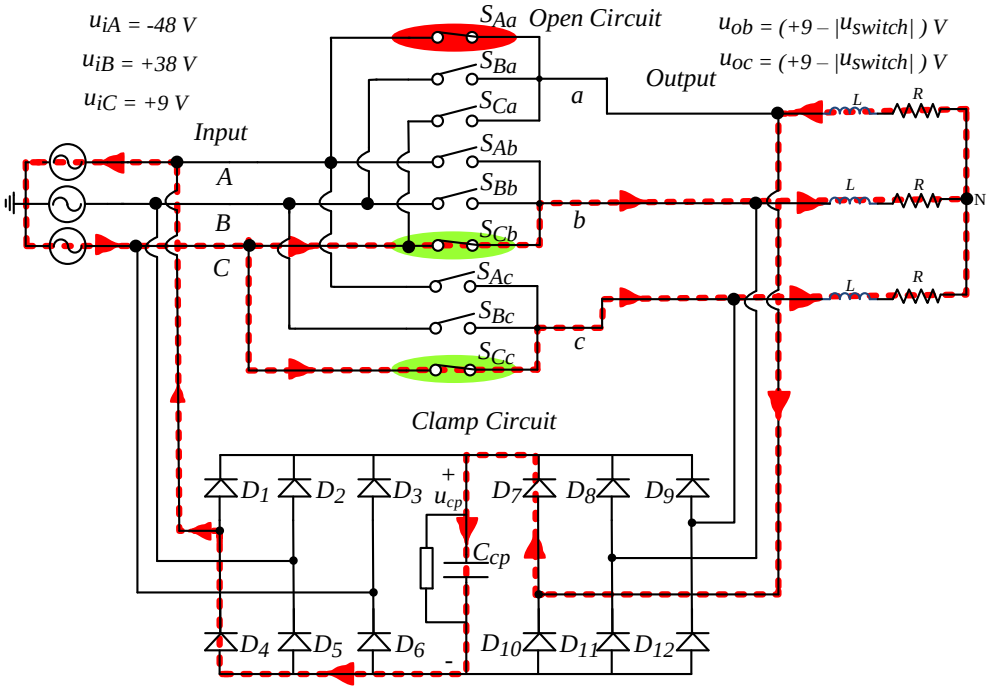


Figure 5.2: Type 1 current recirculating path

5.2.4 Type 2 Current Recirculating Path

The type 2 current recirculating path under these specific conditions is shown in Fig 5.3. Type 2 current recirculating path includes the faulty phase of the load, the clamp circuit, and other phases of the load. In addition, the faulty

output phase load current is the biggest absolute value among the three output load currents in type 2 path. Last but not least, at least one current of the healthy phases of the DMC output will be zero in type 2 path. For instance, the bidirectional switch S_{Aa} occurs an open circuit fault at the time point t_l. The three phase input voltages at t_l are $u_{iA} = -20V$, $u_{iB} = +48V$ and $u_{iC} = -28V$, respectively. The faulty output phase current i_{oa} is flowing into the converter, and the healthy output phases currents i_{ob} and i_{oc} are flowing into the load. The bidirectional switches which are conducting at t_k are S_{Aa}, S_{Cb} and S_{Bc}, respectively. Under these conditions, the faulty output phase current i_{oa} will first flow into the clamp capacitor C_{cp} through diode D_7. Then the current will be divided into two paths. One path will flow through diode D_6 and the other will flow through diode D_{11} because diode D_6 and diode D_{11} are connecting to the most negative voltage. Next, the current flowing from the diode D_{11} will flow into load phase b, and the current flowing from the diode D_6 will continue to flow through the input sources and the DMC and back to load phase c eventually. According to KCL law, i_{oa} equals to the sum of i_{ob} and i_{oc}. Due the reason that the absolute value of i_{oa} is the biggest among the three phase load current, so phase b load current will be supplied by part of the i_{oa} through clamp circuit diode D_{11}. Phase c load current will be supplied by the rest of the i_{oa} through clamp circuit dodie D_6 and bidirectional switch S_{Bc}. Since the load current i_{ob} is supplied by the faulty phase current i_{oa}, so there will be no current in the DMC output phase b.

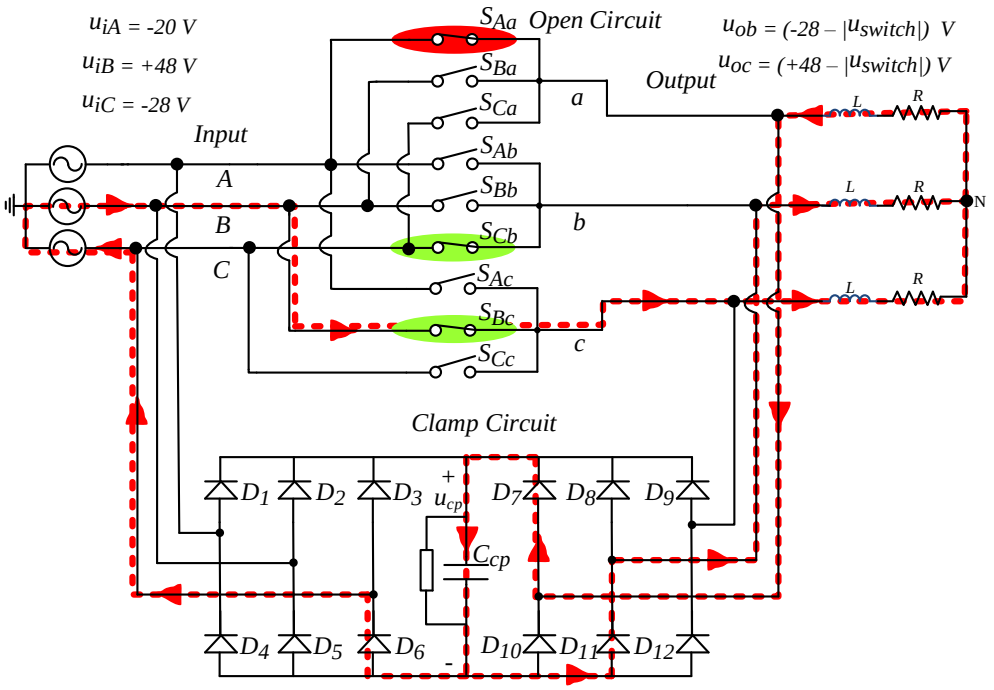


Figure 5.3: Type 2 current recirculating path

5.2.5 Comparison between Type 1 and Type 2 current recirculating paths

The comparison between type 1 and type 2 current recirculating paths are presented in TABLE 5.1. In conclusion, type 2 path will cause at least one healthy output phase current of the DMC to reduce to zero due to the influence of the faulty phase current, the input source voltages and the switching states. This information is very important for a fault diagnosis algorithm to aviod false-diagnosis.

Table 5.1: Comparison between type 1 and type 2 paths

	Type 1 *path*	*Type* 2 *path*
Is the faulty phase current the biggest absolute value?	No	Yes
Does the faulty phase DMC output current reduce to zero?	Yes	Yes
Does the healthy phase DMC output current reduce to zero?	No	Yes

5.2.6 False Diagnosis

In terms of the fault diagnosis method proposed in [15] that the output current sensors are located ahead of the clamp circuit to measure the DMC output current, if a output current sensor detects a zero current signal, the proposed fault diagnosis method will regard the corresponding DMC output phase as an open circuit phase. However, due to the influence of the faulty phase current recirculating, a healthy phase current sensor could detect a zero current signal, so the proposed fault diagnosis method will wrongly regard the corresponding healthy DMC output phase as an open circuit phase. This phenomenon is called false-diagnosis. A false-diagnosis will occur if there is a type 2 current recirculating path. Because the current sensor located in a healthy output phase of the DMC will detect a zero current, and a faulty flag will be generated indicating an open circuit fault occurring in the healthy output phase. Therefore, the current recirculating information presented in this chapter will avoid the false-diagnosis that occurs in [15].

5.2.7 Quantitative Analysis of the Relationship Between Fault Diagnosis Speed and Clamp Circuit Capacitor Design

The three phase input voltages are divided into six different sectors as shown in Fig 5.4. From Fig 5.4, it can be seen that DMC input voltage u_{iA} is the maximum value among the three input voltages in sector I and VI. u_{iB} is the maximum value among the three input voltages in sector II and III. u_{iC} is the maximum value among the three input voltages in sector IV and V. u_{iA} is the minimum value among the three input voltages in sector III and IV. u_{iB} is the minimum value among the three input voltages in sector V and VI. u_{iC} is the minimum value among the three input voltages in sector I and II.

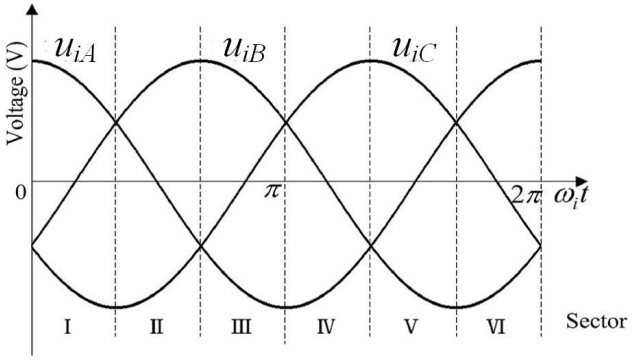


Figure 5.4: Input voltage sectors

Case 1

In case 1, the input voltage angle is entering the range of sectors VI and I. The load phase a reference current ${i_{La}}^*$ and the load phase a current i_{La} are positive. The sampling period is T_s. At the kth sampling period ${T_s}^k$, the controller attempts to minimize the difference between the load current i_{La} and its reference value i_{La} by setting $S_{Aa} = 1$. But the switch S_{Aa} is suffering an open circuit fault.

Therefore, The DMC output phase a is open circuited. The load phase a current i_{La} recirculates through the clamp circuit. The equivalent circuit is shown in Fig 5.5.

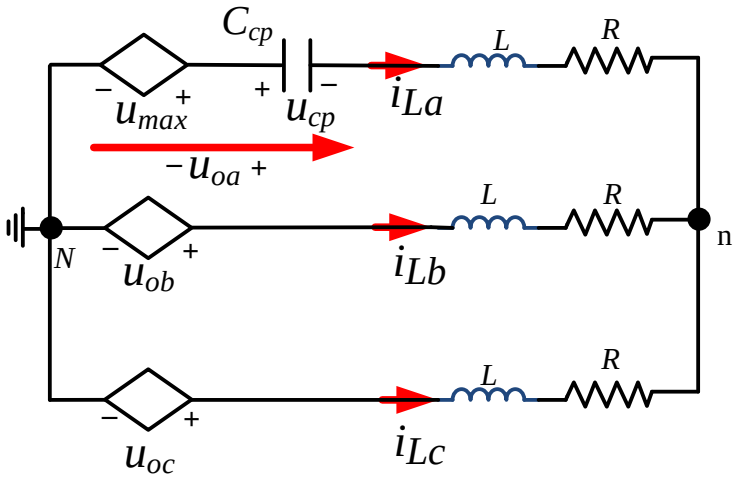


Figure 5.5: Equivalent circuit when i_{La} ¿ 0

The circuit model can be described in equations 5.22.

$$\begin{aligned} u_{oa} - R \cdot i_{La} - L\frac{di_{La}}{dt} &= u_{nN} \\ u_{ob} - R \cdot i_{Lb} - L\frac{di_{Lb}}{dt} &= u_{nN} \\ u_{oc} - R \cdot i_{Lc} - L\frac{di_{Lc}}{dt} &= u_{nN} \\ i_{La} + i_{Lb} + i_{Lc} &= 0 \end{aligned} \tag{5.22}$$

Where u_{nN} is the voltage between the load neutral point and the ground point of the power supply. The DMC output phase voltages can be described in equations 5.23.

$$u_{oa} = u_{max} - u_{cp}, \quad faulty, i_{La} > 0$$
$$\begin{bmatrix} u_{ob} \\ u_{oc} \end{bmatrix} = \begin{bmatrix} S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} u_{iA} \\ u_{iB} \\ u_{iC} \end{bmatrix} \tag{5.23}$$

Where U_{cp} indicates the capacitor voltage of the clamp circuit. Since the load phase a current charges the capacitor of the clamp circuit, U_{cp} is larger than the maximum input line to line voltage. The clamp circuit capacitor voltage can be described in equation 5.24.

$$\begin{aligned} u_{max} &= max(u_{iA}, u_{iB}, u_{iC}) \\ u_{min} &= min(u_{iA}, u_{iB}, u_{iC}) \\ u_{cp} &\geq u_{max} - u_{min} \end{aligned} \tag{5.24}$$

According to equations 5.22 and 5.23, the change rate of the load phase a current i_{La} can be described in equation 5.25.

$$\frac{di_{La}}{dt} = \frac{2u_{max} - 2u_{cp} - u_{ob} - u_{oc} - 3Ri_{La}}{3L} \tag{5.25}$$

According to equation 5.24, the following inequality 5.26 must be true.

$$\begin{aligned} u_{cp} &\geq u_{max} - u_{ob} \\ u_{cp} &\geq u_{max} - u_{oc} \end{aligned} \tag{5.26}$$

By substituting 5.26 into 5.25, it can be seen that the load phase a current change rate is negative as shown in inequality 5.27.

$$\frac{di_{La}}{dt} < 0, when\ i_{La} > 0. \tag{5.27}$$

The energy stored in the faulty phase load inductor can be described in equation 5.28.

$$E_L = \frac{1}{2} L {i_{La}}^2 \tag{5.28}$$

The change rate of the load inductor energy can be described in 5.29.

$$\frac{dE_L}{dt} = L i_{La} \frac{di_{La}}{dt} < 0 \tag{5.29}$$

Therefore, when the faulty switch satisfied $S_{Aa} = 1$, the amplitude of load phase a current decreases. By solving the first order ordinary differential equation (ODE) 5.25, the relationship between the load phase a current i_{La} and the time t is shown in equation 5.30.

$$i_{La(t)} = -(2u_{cp} - 2u_{max} + u_{ob} + u_{oc} - C1 \cdot e^{-3Rt})/3R \tag{5.30}$$

Where $C1$ is a constant depending on the initial value of $i_{La(t)}$.

Case 2

In case 2, the input voltage angle is entering the range of sectors VI and I. The load phase a reference current ${i_{La}}^*$ and the load phase a current i_{La} are negative.

Therefore, The DMC output phase a is open circuited. The load phase a current i_{La} recirculates through the clamp circuit. The equivalent circuit is shown in Fig 5.6.

The circuit model can be described in equations 5.22. The DMC output phase voltages can be described in equations 5.31.

$$\begin{gathered} u_{oa} = u_{min} + u_{cp}, \quad faulty, i_{La} < 0 \\ \begin{bmatrix} u_{ob} \\ u_{oc} \end{bmatrix} = \begin{bmatrix} S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} u_{iA} \\ u_{iB} \\ u_{iC} \end{bmatrix} \end{gathered} \tag{5.31}$$

According to equations 5.22 and 5.31, the change rate of the load phase a current i_{La} can be described in equation 5.32.

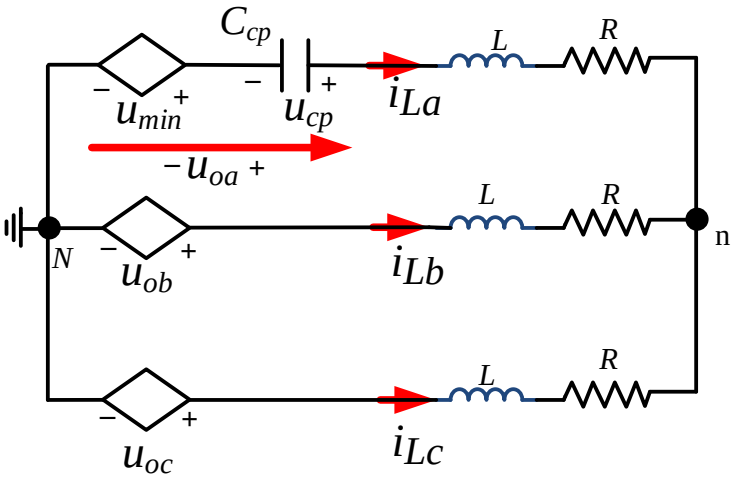


Figure 5.6: Equivalent circuit when i_{La} ¡ 0

$$\frac{di_{La}}{dt} = \frac{2u_{min} + 2u_{cp} - u_{ob} - u_{oc} - 3Ri_{La}}{3L} \tag{5.32}$$

By substituting 5.24 into 5.32, it can be seen that the load phase a current change rate is positive as shown in inequality 5.33.

$$\frac{di_{La}}{dt} > 0, when\ i_{La} < 0. \tag{5.33}$$

The change rate of the load inductor energy can be described in 5.34.

$$\frac{dE_L}{dt} = Li_{La}\frac{di_{La}}{dt} < 0 \tag{5.34}$$

Therefore, when the faulty switch satisfied $S_{Aa} = 1$, the amplitude of load phase a current decreases. By solving the first order ordinary differential equation (ODE) 5.32, the relationship between the load phase a current i_{La} and the time t is shown in equation 5.35.

$$i_{La(t)} = -(2u_b - 2u_{min} - 2u_{cp} + u_{oc} - C2 \cdot e^{-3Rt})/3R \tag{5.35}$$

Where $C2$ is a constant depending on the initial value of $i_{La(t)}$.

Clamp Circuit Capacitor Design

The clamp capacitor is a key element in the clamp circuit. The size of the clamp capacitor will decide how much energy could be stored in the clamp circuit. The maximum energy stored in the inductive load should be taken into consideration when selecting the size of the clamp capacitor.The equation of the maximum energy stored in a three phase resistance-inductance load can be described in Equation in 5.36 [76].

$$\begin{aligned} E_{RLload} &= \frac{1}{2} L_{load} ({i_a}^2 + {i_b}^2 + {i_c}^2) \\ &= \frac{3}{4} L_{load} {I_p}^2 \end{aligned} \tag{5.36}$$

Where E_{RLload} is the maximum energy stored in the resistance-inductance load. L_{load} is the inductance of the $R-L$ load. i_a, i_b and i_c are the three phase balanced load currents and I_p is the amplitude of the output phase current.

When an output open-circuit fault occurs, the maximum energy absorbed by the clamp capacitor can be expressed in Equation 5.37. Where E_{clamp} is the maximum energy absorbed by the clamp capacitor, C_{clamp} is the capacitance of the clamp circuit, V_{max} is the maximum acceptable clamp voltage related to the voltage rating of the power switches, V_{int} is the initial clamp voltage equal to the input line-to-line peak voltage.

$$E_{clamp} = \frac{1}{2} C_{clamp} ({V_{max}}^2 - {V_{int}}^2) \tag{5.37}$$

Due to the fact that the maximum energy stored in the resistance-inductance load must be lower than the energy absorbed by the clamp capacitor, so the capacitance of the clamp circuit can be calculated by Equation 5.38.

$$C_{clamp} > \frac{3}{2} \frac{L_{load} {I_p}^2}{{V_{max}}^2 - {V_{int}}^2} \tag{5.38}$$

Meanwhile, the required time for a correct fault diagnosis should also be considered when designing the clamp circuit capacitor.

If an open circuit fault can not be correctly detected unless all the energy stored in the load inductor has been transferred to the clamp circuit capacitor as shown in literature [16], the capacitance of the clamp circuit capacitor should be big enough to absorb all the energy stored in the faulty phase load inductor.

If an open circuit fault can be correctly detected within several sampling time periods as shown in literature [77], the capacitance of the clamp circuit capacitor can be designed relatively small because not the whole of the faulty phase load inductor energy will be transferred to the clamp circuit capacitor. This is because a fault tolerance strategy will be implemented into the DMC system once an open circuit fault can be correctly detected. Once the fault tolerance strategy is successfully implemented into the DMC system, the faulty switch may be isolated by using only the other two healthy bidirectional switches. In this way, only a relatively small amount of inductive load energy will be transferred to the clamp circuit capacitor, which will make the clamp circuit capacitor smaller than in literature [16].

Therefore, improving the speed of correct fault diagnosis can effectively reduce the size of the clamp circuit capacitor, which will make the DMC topology competitive especially in volume critical applications such as more electric aircraft.

5.2.8 Open Circuit Switch Fault Scenarios for Direct Matrix Converters

This thesis assumes the bidirectional switch is open circuited in both directions when an open circuit switch fault occurs. Nine open circuit switch fault scenarios are considered for direct matrix converters in this thesis as listed below.

1. Bidirectional switch S_{Aa} open circuit fault;
2. Bidirectional switch S_{Ab} open circuit fault;
3. Bidirectional switch S_{Ac} open circuit fault;

4. Bidirectional switch S_{Ba} open circuit fault;
5. Bidirectional switch S_{Bb} open circuit fault;
6. Bidirectional switch S_{Bc} open circuit fault;
7. Bidirectional switch S_{Ca} open circuit fault;
8. Bidirectional switch S_{Cb} open circuit fault;
9. Bidirectional switch S_{Cc} open circuit fault.

Due to the reason that the inputs of the direct matrix converter are three phase balanced sinusoidal waveforms, and the outputs of the direct matrix converter are usually three phase balanced RL-load or electrical machine, so each bidirectional switch switching waveform of the direct matrix converter should be the same but with different angle shift under ideal three phase balanced normal operations. Therefore, in this thesis simulation results and experimental results focus on bidirectional switch S_{Aa} open circuit fault. The fault diagnosis algorithms developed based on switch S_{Aa} open circuit fault can also be applied to the other eight bidirectional switches open circuit fault scenarios with no modification.

When one bidirectional switch fails open circuit, it could be either both IGBTs are open circuit or only one IGBT is open circuit. When only one IGBT fails open circuit, there could still be current circulating in the faulty switch depending on the current direction. This thesis assumes that both IGBTs of one bidirectional switch fail open circuit at the same time

5.3 Open Circuit Fault behaviour Analysis for Indirect Matrix Converters

There are different faulty scenarios at the system level of IMCs, including the input supply failure, rectifier stage failure and inverter stage failures. If there is an input supply open circuit failure and the IMC can run as normal, the output harmonics will increase and the output power will decrease. Since this thesis focuses on the semiconductor switch open circuit fault, the input supply failure will not be discussed in detail.

5.3.1 Inverter Stage Fault Operation

Since the rectifier stage and the inverter stage of the IMC are connected directly without any decoupling component, so if an open circuit fault occurs in the rectifier stage it will influence the behaviour of the inverter stage. Therefore, this section first analyzes the IMC inverter stage open circuit fault operation by assuming the rectifier stage is working normally. The inverter stage fault operation is shown in Figure 5.7.

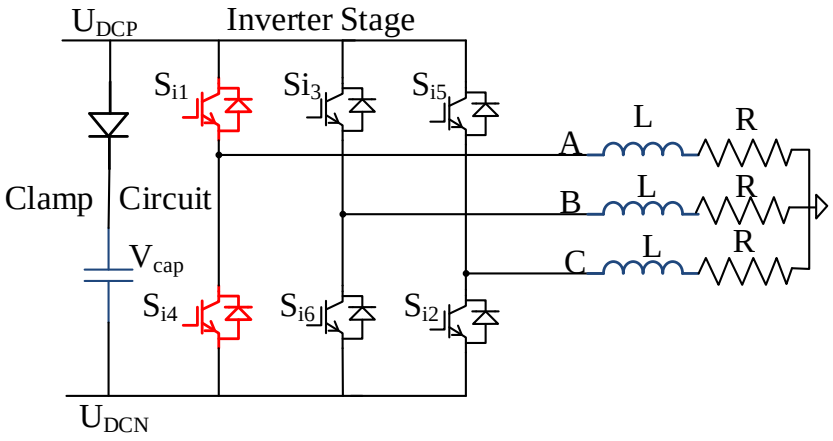


Figure 5.7: IMC inverter stage open-circuit fault operation

Assuming the sampling period is T_s, the switch S_{i1} is applied at the k^{th} sampling period ${T_s}^k$, and the switch S_{i1} is suffering an open-circuit fault. This will cause the actual switching state to be zero during the faulty period, which causes the desired output voltage values do not correspond to the real ones. To obtain the output line-to-line voltage without requiring additional voltage sensor, the load mathematical model is established in Equation 5.39. where u_N is the voltage drop between the power supply ground and the load neutral point. According to the load model, it can be seen that the actual output line-to-line voltage can be estimated if knowing the derivative part of the load current. The derivative part of the load current can be obtained by sampling the load current four times in one sampling period with equal time

gap at time points ${T_s}^k$, ${T_s}^{k+\frac{1}{4}}$, ${T_s}^{k+\frac{1}{2}}$ and ${T_s}^{k+\frac{3}{4}}$, respectively. Three sampled values at these four sampling points are used for estimating the line-to-line voltage.

$$\begin{aligned} u_{oA} - Ri_{oA} - L\frac{di_{oA}}{dt} &= u_N \\ u_{oB} - Ri_{oB} - L\frac{di_{oB}}{dt} &= u_N \\ u_{oC} - Ri_{oC} - L\frac{di_{oC}}{dt} &= u_N \\ i_{oA} + i_{oB} + i_{oC} &= 0 \end{aligned} \tag{5.39}$$

Assuming the output load current is expressed as in Equation 5.40:

$$f(t) = i_{oX}(t), X = A, B, C \tag{5.40}$$

According to Taylor's formula, the derivative part of the load current can be acquired by ignoring the higher order part as shown in Equation 5.41 [68].

$$f^{'}(kT_s + \frac{T_s}{2}) \approx \frac{2}{T_s} f(kT_s + \frac{3T_s}{4}) - \frac{2}{T_s} f(kT_s + \frac{T_s}{4}) \tag{5.41}$$

The actual output line-to-line voltages are estimated by substituting Equation 5.41 into Equation 5.39, as shown in Equation 5.42.

$$\begin{aligned} u_{oAB} \approx u_{oAB_{esti}} &= R{i_{oAB}}^{k+\frac{1}{2}} + \frac{2L}{T_s}({i_{oAB}}^{k+\frac{3}{4}} - {i_{oAB}}^{k+\frac{1}{4}}) \\ u_{oBC} \approx u_{oBC_{esti}} &= R{i_{oBC}}^{k+\frac{1}{2}} + \frac{2L}{T_s}({i_{oBC}}^{k+\frac{3}{4}} - {i_{oBC}}^{k+\frac{1}{4}}) \\ u_{oCA} \approx u_{oCA_{esti}} &= R{i_{oCA}}^{k+\frac{1}{2}} + \frac{2L}{T_s}({i_{oCA}}^{k+\frac{3}{4}} - {i_{oCA}}^{k+\frac{1}{4}}) \end{aligned} \tag{5.42}$$

Where :

$$
\begin{aligned}
{i_{oAB}}^{j} &= {i_{oA}}^{j} - {i_{oB}}^{j} \\
{i_{oBC}}^{j} &= {i_{oB}}^{j} - {i_{oC}}^{j} \\
{i_{oCA}}^{j} &= {i_{oC}}^{j} - {i_{oA}}^{j} \\
j = k + \frac{1}{4}, k + \frac{1}{2}, k + \frac{3}{4}&
\end{aligned}
\tag{5.43}
$$

Therefore, the actual output line-to-line voltages under faulty conditions can be estimated without additional voltage sensors. If an open-circuit fault occurs in the inverter stage, the estimated output line-to-line voltages will be different from the FCS-MPC predicted output line-to-line voltage, which can be used for IMC fault detection and diagnosis purpose.

5.3.2 Rectifier Stage Fault Operation

Designing a fault diagnosis method for the IMC is different from the DMC. This is because there are two stages and a fictitious DC-Link in the IMC. Therefore, additional sensors are necessary for IMC fault diagnosis because the rectifier stage and the inverter stage are not decoupled. If there is an open-circuit fault occurs in the rectifier stage, the fictitious DC-Link and the IMC output voltages will be influenced. Therefore, it is impossible to locate the open-circuit switch in the rectifier stage by using the estimated output line-to-line voltage only. In order to locate the faulty switch in the rectifier stage of the IMC, two additional voltage sensors are needed to measure the two fictitious DC-Link bus voltages U_{DCP} and U_{DCN} as shown in Fig 5.8.

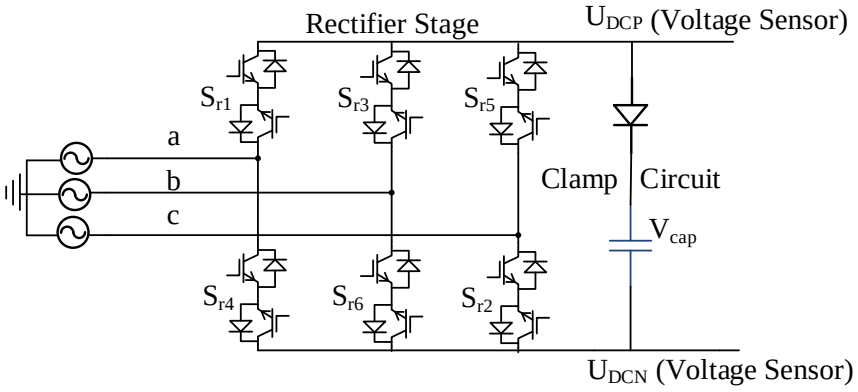


Figure 5.8: IMC rectifier stage open-circuit fault operation

Assuming S_{r1} is suffering an open-circuit fault, the clamp circuit diode will turn on and the fictitious DC-Link current i_{DC} will charge the clamp circuit capacitor. So the faulty voltage $U_{DCP-fault}$ of the positive DC-Link line will become dramatically more positive due to the application of the clamp circuit capacitor voltage. The faulty positive DC-Link voltage can be expressed in Equation 5.44.

$$\begin{aligned} U_{DCP-fault} &= U_{DCN} + U_{cap} \\ U_{DCN} &= \begin{bmatrix} v_{ia} & v_{ib} & v_{ic} \end{bmatrix} \begin{bmatrix} S_{r4} \\ S_{r6} \\ S_{r2} \end{bmatrix} \end{aligned} \tag{5.44}$$

Similarly, if S_{r4} is suffering an open-circuit fault, the clamp circuit diode will turn and the fictitious DC-Link current i_{DC} will charge the clamp circuit capacitor. So the faulty voltage $U_{DCN-fault}$ of the negative DC-Link line will become dramatically more negative due to the application of the clamp circuit capacitor voltage. The faulty negative DC-Link voltage can be expressed in Equation 5.45.

$$U_{DCN-fault} = U_{DCP} + U_{cap}$$
$$U_{DCP} = \begin{bmatrix} v_{ia} & v_{ib} & v_{ic} \end{bmatrix} \begin{bmatrix} S_{r1} \\ S_{r3} \\ S_{r5} \end{bmatrix} \tag{5.45}$$

5.4 Open Circuit Switch Fault Detection and Diagnosis Method for Direct Matrix Converter

The output current sensors of the direct matrix converter system can measure the output phase currents. Traditionally, three output current sensors are located beyond the clamp circuit to measure the output load phase current as shown in Figure 5.9. For this type of output current sensor location, an immediate change in the sampled current is not obvious because of the inductive load nature. Therefore, the speed of the fault detection and system diagnosis is not the optimum when using this location of the output current sensors.

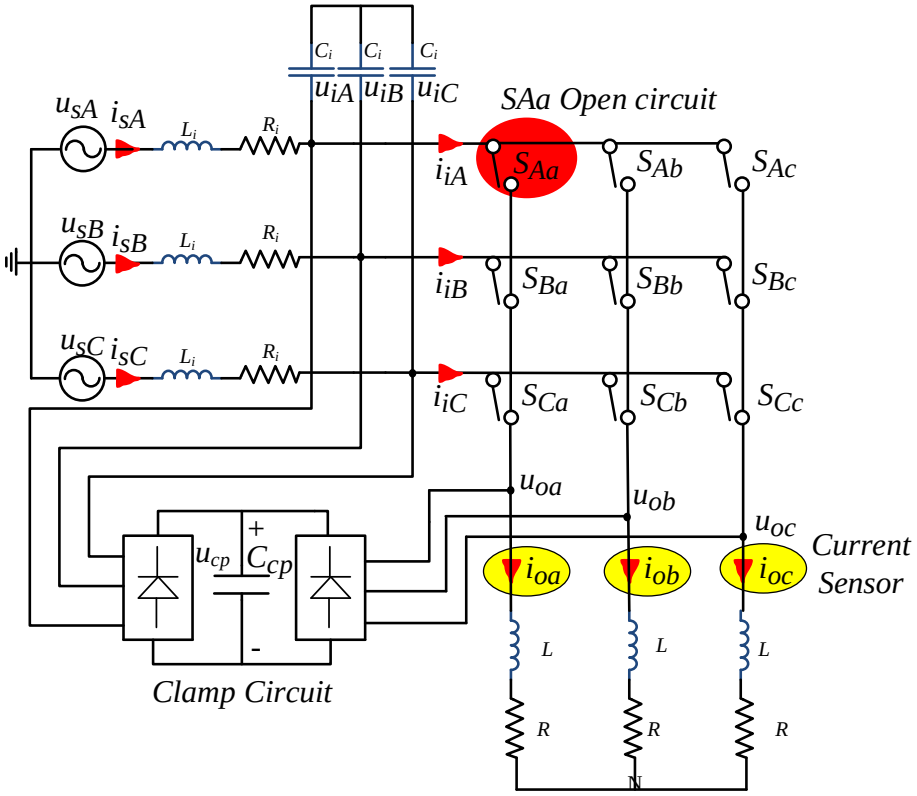


Figure 5.9: Output current sensors located behind the clamp circuit to measure the output load current

In this section, the three output current sensors are located ahead of the clamp circuit to measure the DMC output currents directly as shown in Figure 5.10. The advantage of the new sensor location is that once an open circuit switch fault occurs, the corresponding faulty-phase current sensor will measure a zero current immediately. For example, if the bidirectional switch S_{Aa} occurs an open circuit fault when the switch is supposed to be conducting, the current i_{oa} will become zero immediately because the phase A load current can not recirculate through the matrix converter anymore. Instead, the load current will recirculate through the clamp circuit which connected in parallel with the matrix converter. so the current sensor located at the new position will detect a zero current immediately after the conducting switch S_{Aa} occurs an open circuit fault. Therefore by using the new location for the output current sensors a faster fault detection and system diagnosis can be achieved.

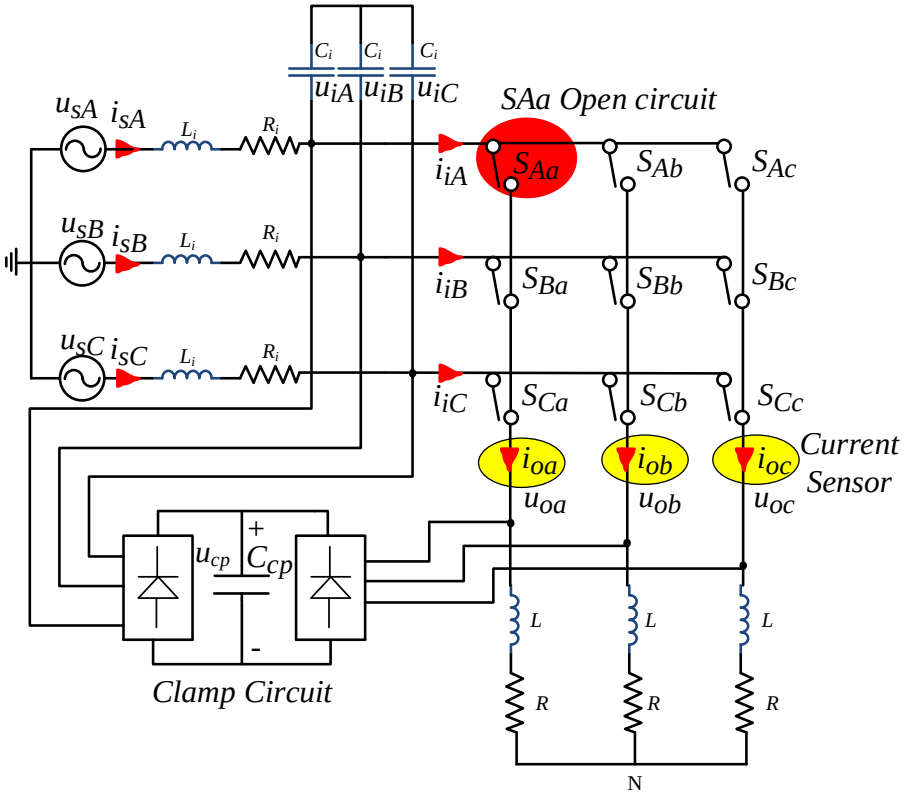


Figure 5.10: Output current sensors located ahead of the clamp circuit to measure the direct matrix converter output phase current

As mentioned before, the load currents will recirculate through the clamp circuit if the matrix converter output current is detected as zero as shown in Figure 5.11. When a zero current is detected by an output current sensor, the corresponding matrix converter output phase should be identified as an open-circuited faulty phase. Three variables F_a, F_b and F_c are defined to indicate the faulty possibility of the output phases A, B and C of the direct matrix converter respectively. The corresponding flags of F_a, F_b, F_c will be set to 1 or 0.5 to show the probability of the faulty phase. 1 means that the corresponding output phase must be the open-circuited faulty phase. 0.5 means the corresponding output phase might have an open circuit fault, but it is also possible that the corresponding output phase is a healthy phase. The possibility of the fault phase depends on which type of the current recirculating path is occurring. These three faulty flag values are the key to avoid false-diagnosis in a single switch faulty scenario. The reason 0.5 is needed is that the fault diagnosis algorithm can not set a 1 on any output phase in some scenarios. Then the fault diagnosis will suspect a possible faulty output phase. Figure 5.11 and Figure 5.12 show the potential path for the load currents when an open-circuited fault occurs.

Figure 5.11 shows that the currents of healthy phases b and c are not canceled by the faulty phase load current, because current sensors in output phase b and c can still detect a non-zero current. So in this case, the corresponding flags of F_a, F_b, F_c will be set to 1 or 0 and 0, respectively.

Figure 5.12 shows that the healthy output phase current is influenced by the actual open circuit faulty phase current by clamp circuit current recirculating because the current sensor in output phase b will detect a zero current. In this case, the flags F_a and F_b will be set to either 1 or 0.5. Then, the output currents amplitude information is required to decide the corresponding flag value. More details about the fault detection and diagnosis algorithm will be discussed next.

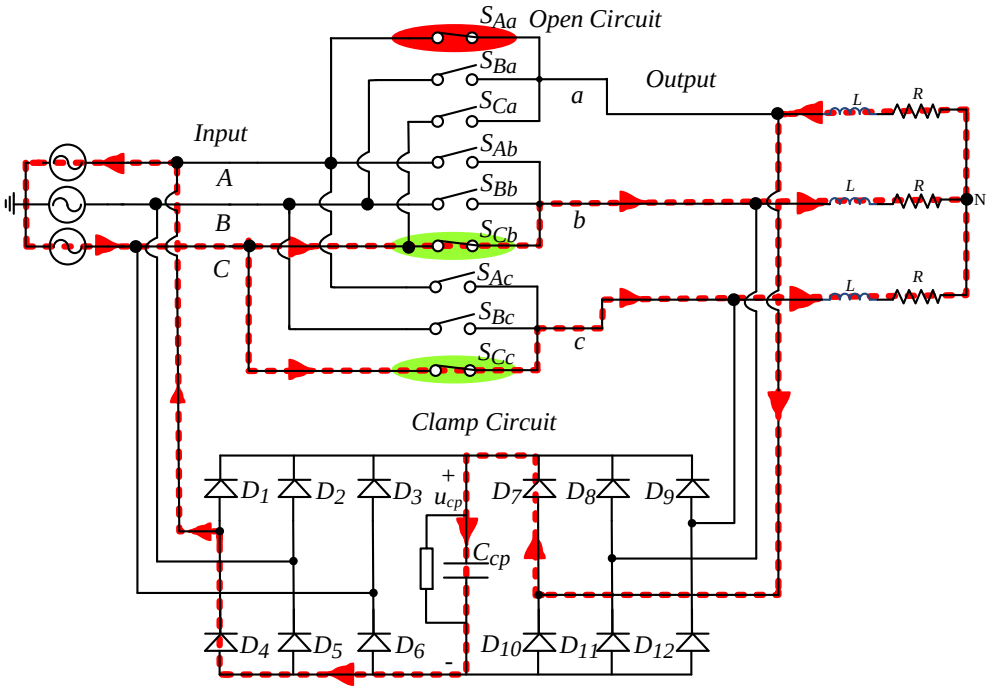


Figure 5.11: Type 1 faulty current recirculating path without healthy phase current cancellation

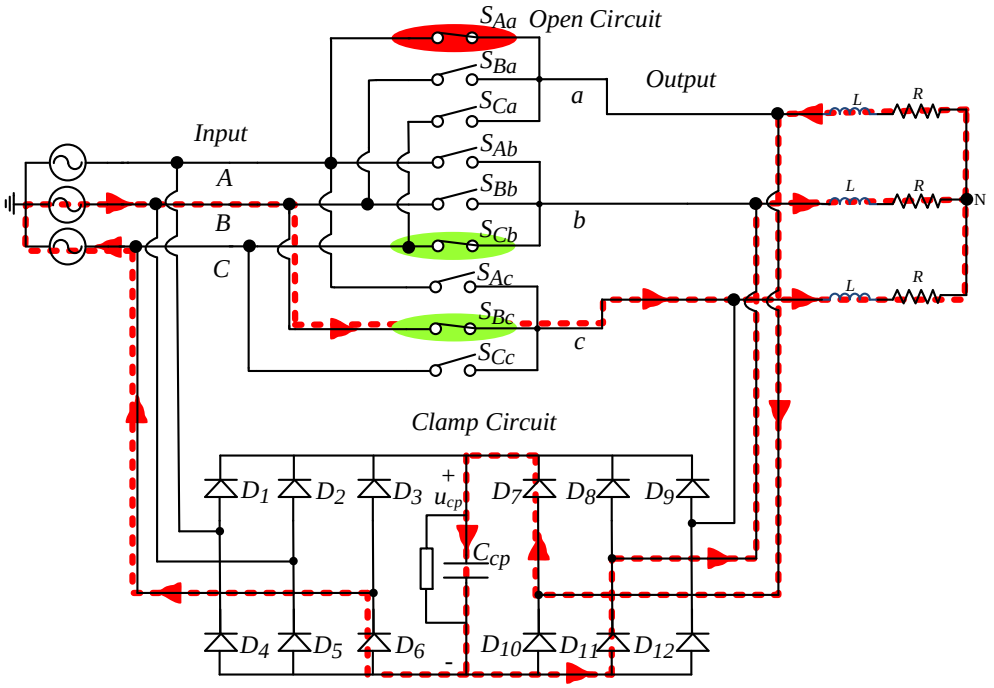


Figure 5.12: Type 2 faulty current recirculating path with healthy phase current cancellation

As mentioned in the above section, The faulty output phase current may recirculate through the clamp circuit and provide current supply for a healthy phase load current. So the recirculating current may cause the output current sensor detects a zero current. In order to avoid any false-diagnosis during the whole fault detection process, the clamp circuit current recirculating information is required for the fault detection algorithm. The three output phase currents of the direct matrix converter will be detected in every sampling period. The fault diagnosis algorithm flowcharts are shown in Figure 5.13, 5.14 and 5.15. The fault diagnosis algorithm for each output phase is exactly the same. ${i_{oa}}^k$, ${i_{ob}}^k$ and ${i_{oc}}^k$ mean the matrix converter three output phase currents during the sampling period ${T_s}^k$. ${i_{oa}}^{k-1}$, ${i_{ob}}^{k-1}$ and ${i_{oc}}^{k-1}$ mean the matrix converter three output phase currents during the sampling period ${T_s}^{k-1}$. $|{i_{oa}}^{k-1}|$, $|{i_{ob}}^{k-1}|$ and $|{i_{oc}}^{k-1}|$ mean the absolute value of the amplitude of the the matrix converter three output phase currents during the sampling period ${T_s}^{k-1}$. F_a, F_b and F_c indicate the faulty possibility flag of the output phases A, B and C of the direct matrix converter

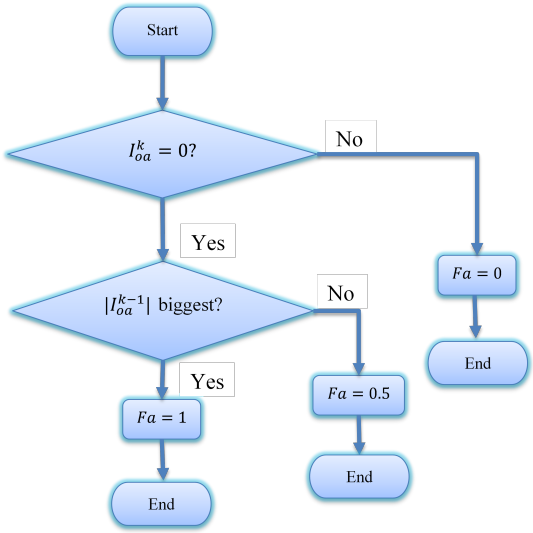


Figure 5.13: Flow chart of the fault detection for phase a

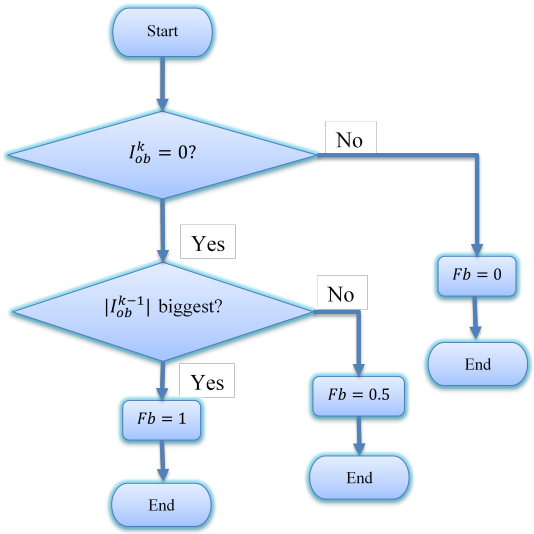


Figure 5.14: Flow chart of the fault detection for phase b

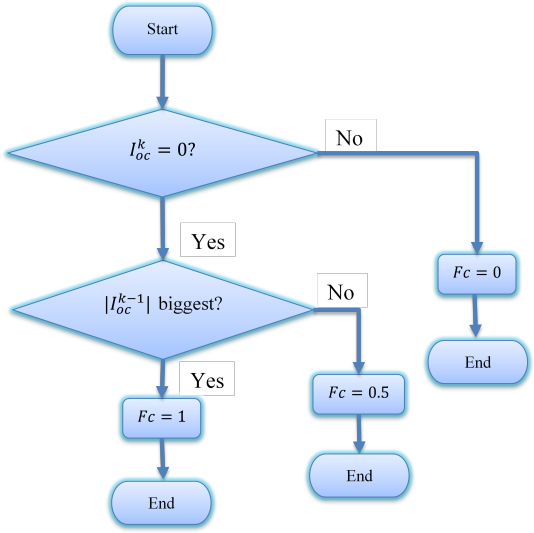


Figure 5.15: Flow chart of the fault detection for phase c

First, the output currents ${i_{oa}}^k$, ${i_{ob}}^k$ and ${i_{oc}}^k$ in the sampling period ${T_s}^k$ will be checked whether or not is zero. If the current is not zero, the fault detection algorithm will make a decision that there is no open circuit fault in the corresponding output phase and set the corresponding flag to 0. If the current is zero, then the fault detection algorithm will check whether or not the output currents ${i_{oa}}^{k-1}$, ${i_{ob}}^{k-1}$ and ${i_{oc}}^{k-1}$ in the sampling period ${T_s}^{k-1}$ is the biggest absolute value comparing the other two. If the output current is biggest absolute value, the fault detection algorithm will make a decision that the corresponding output phase is presenting an open circuit fault and set the corresponding flag to 1. If the output current is not the biggest absolute value, the fault detection algorithm will make a decision that the corresponding output phase might be presenting an open circuit fault and set the corresponding flag to 0.5.

Once the fault detection algorithm for each output phase has been completed, the switching state information of the sampling period ${T_s}^k$ will be used by the fault diagnosis algorithm to identify the specific bidirectional switch which is used in the faulty phase by solving Equation 5.46. Since this section focuses on single bidirectional switch open-circuited fault, the switch which has the highest possibility of being faulty will be identified as a faulty switch.

$$\begin{bmatrix} F_{Aa} & F_{Ba} & F_{Ca} \\ F_{Ab} & F_{Bb} & F_{Cb} \\ F_{Ac} & F_{Bc} & F_{Cc} \end{bmatrix} = \begin{bmatrix} F_a & 0 & 0 \\ 0 & F_b & 0 \\ 0 & 0 & F_c \end{bmatrix} \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \tag{5.46}$$

One drawback of the proposed method is that it will diagnose an open circuit fualt during the natural zero crossing. Therefore, at least two sampling periods are required to guarantee the currents are avoid the false triggering.

5.4.1 Open Circuit Switch Fault Detection and Diagnosis Method for Direct Matrix Converter with SVM Strategy

The fault detection and diagnosis algorithm requires the switching states information and the output current information in every modulation period. The 3-Zero-SVM switching sequence has 7 different switching states. The 2-Zero-SVM switching sequence has 6 different switching states. The 1-Zero-SVM switching sequence has 5 different switching states[78]. In order to reduce the complexity of the fault detection and diagnosis algorithm for the SVM strategy, the 1-Zero-SVM strategy is selected for the fault detection and diagnosis due to the least number of switching states.

In order to obtain the output current information of every switching state in one modulation period, the current over-sampling technique [79] is used as shown in Figure 5.16. Current over-sampling is a technique that using DSP/FPGA control platform and the ADC sampling circuit to sample the current signal many times in one sampling period. The number of samples in one sampling period depends on the specific application. In this matrix converter fault diagnosis application with $12.5kHz$ modulation frequency, the direct matrix converter output current can be sampled 16 times per modulation period. It means the current sample frequency is $200kHz$. By using the current over-sampling technique, the output current information in most switching states can be obtained within one modulation period. However, the current distortion during the switching commutation transient state and the high frequency noise captured by the high bandwidth current sensor will limit the precision of this over-sampling technique in practical application. In this thesis, the current over-sampling technique is used to detect the open circuit fault. The experimental results about the current over-sampling is presented in Chapter 8.

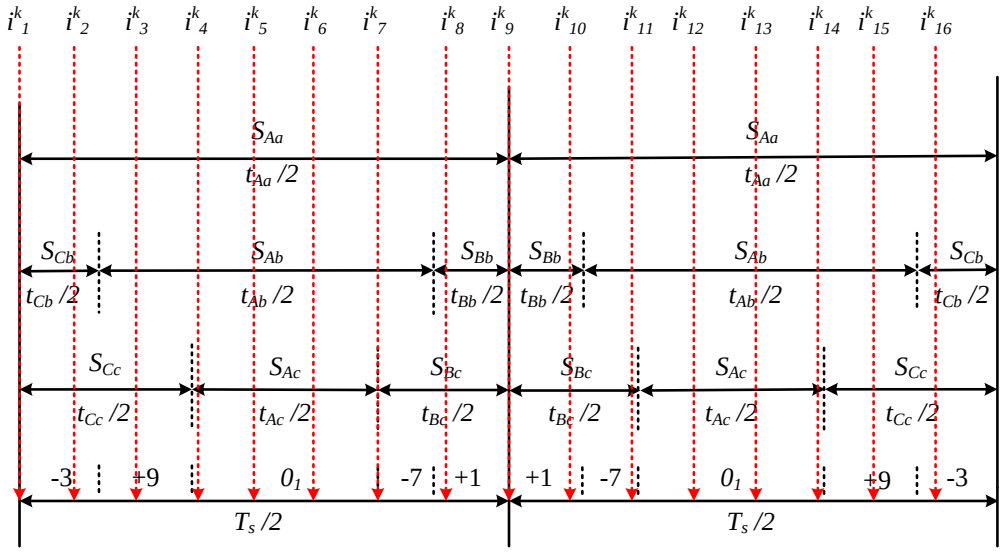


Figure 5.16: Output current over-sampling technique for SVM strategy

After obtaining the output current information and the corresponding switching state information within every modulation period, the fault detection and diagnosis algorithm can locate the faulty bidirectional switch following the flow charts as shown in Figure 5.13 5.14 5.15 and Equation 5.46.

The advantage for doing fault detection and diagnosis with SVM strategy is that the switching frequency is fixed. The fixed switching frequency will make it easier to design the filter for the direct matrix converter system with SVM strategy than with finite-control-set model-predictive-control(FCS-MPC) strategy, because the switching frequency is uncertain in FCS-MPC strategy. Another advantage for doing fault detection and diagnosis with SVM strategy is that the SVM algorithm computation amount is lower than the FCS-MPC algorithm. The computation amount is the total number of instructions required to be executed in the DSP control platform. More instructions are required to be executed in the FCS-MPC strategy than in the SVM strategy, because the FCS-MPC strategy calculates the cost function 27 times as discussed in Chapter 4.

5.4.2 Open Circuit Switch Fault Detection and Diagnosis Method for Direct Matrix Converter with FCS-MPC Strategy

As discussed in Chapter 4, the FCS-MPC strategy only apply one switching state during one sampling period. This characteristic will guarantee that the current sensor will not capture any current distortion caused by the switching commutation transient state. The current sampling technique for the FCS-MPC strategy is shown in Figure 5.17. It can be seen from figure 5.17 that only one sample of the voltage and current signals are required to execute the FCS-MPC strategy as well as the fault diagnosis algorithm because only one fixed switching state is applied during one sampling period.

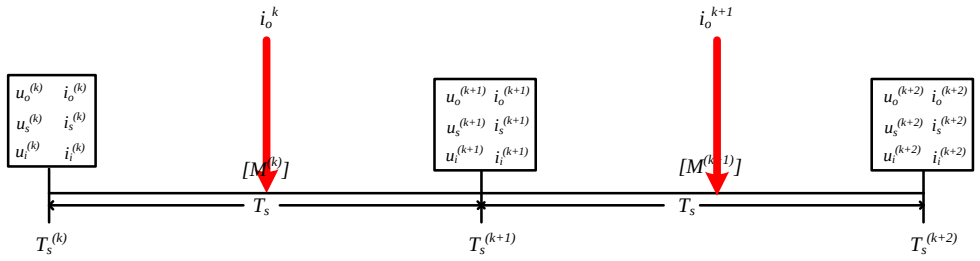


Figure 5.17: Output current sampling technique for FCS-MPC strategy

With the output current information and the corresponding switching state information within every sampling period, the fault detection and diagnosis algorithm can locate the faulty bidirectional switch by following the flow charts in Figure 5.13, 5.14 and 5.15 and solving Equation 5.46.

The advantage for doing fault detection and diagnosis with FCS-MPC strategy is that there is only one fixed switching state within one sampling period. So only one current sample is required within one sampling period. This current sensing requirement will allow relatively low bandwidth of the output current sensor. The low bandwidth of the output current sensor could potentially reduce the hardware cost.

5.5 Open Circuit Switch Fault Detection and Diagnosis Method for Indirect Matrix Converter with Model Predictive Control Strategy

The indirect matrix converter system is shown in Figure 5.18. The switching state information of the rectifier and inverter stages will be used for indirect matrix converter FCS-MPC fault detection purpose. Because the switching state will keep constant during one entire sampling period, which will help to locate the open-circuit switch. This section focuses on the single unidirectional switch open circuit fault in the fictitious inverter stage and the single bidirectional switch open circuit fault in the fictitious rectifier stage.

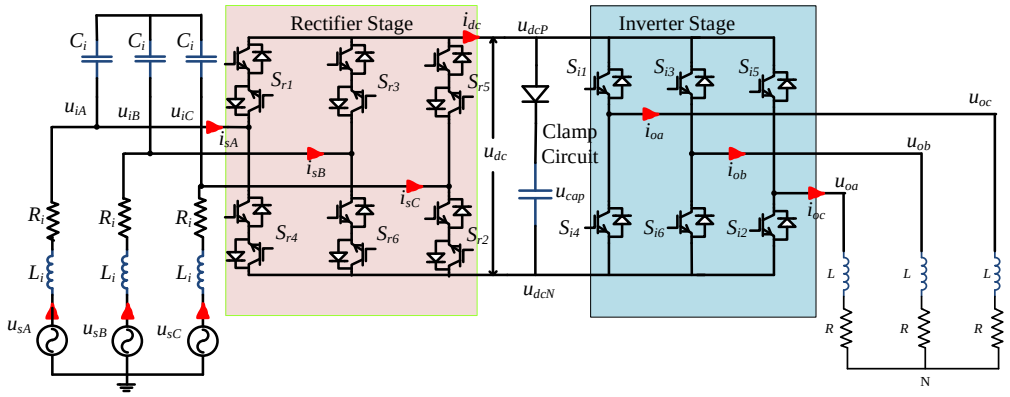


Figure 5.18: Indirect matrix converter system

5.5.1 Inverter Stage Fault Detection

The inverter stage fault operation is shown in Figure 5.19. This section assumes that the fictitious rectifier stage switches are healthy and there is a single unidirectional switch open circuit fault in the fictitious inverter stage.

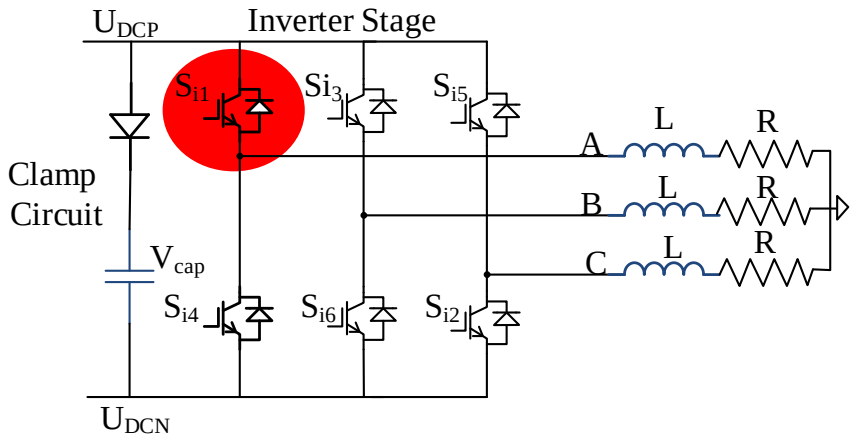


Figure 5.19: IMC inverter stage open-circuit fault operation

Assuming the sampling period is T_s, the switch S_{i1} is applied at the k^{th} sampling period ${T_s}^k$, and the switch S_{i1} is suffering an open-circuit fault. This will cause the actual switching state to be zero during the faulty period, which causes the desired values do not correspond to the real ones. To obtain the output line-to-line voltage without requiring additional voltage sensor, the load mathematical model is established in Equation 5.47. where u_N is the voltage drop between the power supply ground and the load neutral point. According to the load model, it can be seen that the actual output line-to-line voltage can be estimated if knowing the derivative part of the load current. The derivative part of the load current can be obtained by sampling the load current four times in one sampling period with equal time gap at time points ${T_s}^k$, ${T_s}^{k+\frac{1}{4}}$, ${T_s}^{k+\frac{1}{2}}$ and ${T_s}^{k+\frac{3}{4}}$, respectively. Three sampled values at these four sampling points are used for estimating the line-to-line voltage.

$$\begin{aligned} u_{oA} - Ri_{oA} - L\frac{di_{oA}}{dt} &= u_N \\ u_{oB} - Ri_{oB} - L\frac{di_{oB}}{dt} &= u_N \\ u_{oC} - Ri_{oC} - L\frac{di_{oC}}{dt} &= u_N \\ i_{oA} + i_{oB} + i_{oC} &= 0 \end{aligned} \tag{5.47}$$

Assuming the output load current is expressed as in Equation 5.48:

$$f(t) = i_{oX}(t), X = A, B, C \tag{5.48}$$

According to Taylor's formula, the derivative part of the load current can be acquired by ignoring the higher order part as shown in Equation 5.49 [68].

$$f^{'}(kT_s + \frac{T_s}{2}) \approx \frac{2}{T_s} f(kT_s + \frac{3T_s}{4}) - \frac{2}{T_s} f(kT_s + \frac{T_s}{4}) \tag{5.49}$$

The actual output line-to-line voltages are estimated by substituting Equation 5.41 into Equation 5.47, as shown in Equation 5.50.

$$\begin{aligned} u_{oAB} \approx u_{oAB_{esti}} &= R{i_{oAB}}^{k+\frac{1}{2}} + \frac{2L}{T_s}({i_{oAB}}^{k+\frac{3}{4}} - {i_{oAB}}^{k+\frac{1}{4}}) \\ u_{oBC} \approx u_{oBC_{esti}} &= R{i_{oBC}}^{k+\frac{1}{2}} + \frac{2L}{T_s}({i_{oBC}}^{k+\frac{3}{4}} - {i_{oBC}}^{k+\frac{1}{4}}) \\ u_{oCA} \approx u_{oCA_{esti}} &= R{i_{oCA}}^{k+\frac{1}{2}} + \frac{2L}{T_s}({i_{oCA}}^{k+\frac{3}{4}} - {i_{oCA}}^{k+\frac{1}{4}}) \end{aligned} \tag{5.50}$$

Where :

$$
\begin{aligned}
{i_{oAB}}^j &= {i_{oA}}^j - {i_{oB}}^j \\
{i_{oBC}}^j &= {i_{oB}}^j - {i_{oC}}^j \\
{i_{oCA}}^j &= {i_{oC}}^j - {i_{oA}}^j \\
j = k + \frac{1}{4}, k + \frac{1}{2}, k + \frac{3}{4}&
\end{aligned}
\tag{5.51}
$$

Therefore, the actual output line-to-line voltages under faulty conditions can be estimated without additional voltage sensors. If an open-circuit fault occurs in the inverter stage, the estimated output line-to-line voltages will be different from the FCS-MPC predicted output line-to-line voltages, which can be used for IMC fault detection and diagnosis purpose. The voltage errors between the estimated output line-to-line voltages and the FCS-MPC predicted output line-to-line voltages are ε_{AB}, ε_{BC}, and ε_{CA} respectively. The voltage errors ε_{AB}, ε_{BC}, and ε_{CA} will be used to identify the faulty output phase as shown in Table 5.2. All the three voltage errors will be smaller than the predefined threshold value ε_{th} in normal operation. Once the faulty output phase is identified, the corresponding flag F_X (F_A, F_B, F_C) will be set to 1. Then the faulty switch of the inverter stage can be identified by using switching states information as shown in Equation 5.52.

Table 5.2: Inverter stage faulty phase identification

	Normal operation	Phase-A fault	Phase-B fault	Phase-C fault
$\lvert\varepsilon_{AB}\rvert$	$< \varepsilon_{th}$	$> \varepsilon_{th}$	$> \varepsilon_{th}$	$< \varepsilon_{th}$
$\lvert\varepsilon_{BC}\rvert$	$< \varepsilon_{th}$	$< \varepsilon_{th}$	$> \varepsilon_{th}$	$> \varepsilon_{th}$
$\lvert\varepsilon_{CA}\rvert$	$< \varepsilon_{th}$	$> \varepsilon_{th}$	$< \varepsilon_{th}$	$> \varepsilon_{th}$

$$
\begin{bmatrix} F_{i1} & F_{i3} & F_{i5} \\ F_{i4} & F_{i6} & F_{i2} \end{bmatrix} = \begin{bmatrix} S_{i1} & S_{i3} & S_{i5} \\ S_{i4} & S_{i6} & S_{i2} \end{bmatrix} \begin{bmatrix} F_A & 0 & 0 \\ 0 & F_B & 0 \\ 0 & 0 & F_C \end{bmatrix} \tag{5.52}
$$

5.5.2 Rectifier Stage Fault Detection

This section assumes that the fictitious inverter stage switches are healthy and there is a single bidirectional switch open circuit fault in the fictitious rectifier stage. When an open-circuit fault occurs in the rectifier stage, the information of error output voltages and switching states will not be enough for fault detection and diagnosis. Therefore, two additional voltage sensors are implemented to measure the positive and negative buses voltages of the fictitious DC-Link as shown in Figure 5.20. The DC-Link voltage U_{DCP} and U_{DCN} will be used to identify whether the top switch or the bottom switch of the rectifier stage are open-circuited as shown in Table 5.3. The voltage U_{DCP} is the voltage difference between the DC-Link positive line and the input source neutral point. The voltage U_{DCN} is the voltage difference between the DC-Link negative line and the input source neutral point. If the DC-Link buses voltage error $|U_{DCP} - U_{DCP}{}^*|$ or $|U_{DCN} - U_{DCN}{}^*|$ is bigger than a predefined threshold value U_{th}, the corresponding flag $F_Y(F_P, F_N)$ will be set to 1 to indicate an open-circuit fault in the rectifier stage. Then the faulty switch of the rectifier stage can be identified by using switching states information as shown in equation 5.53.

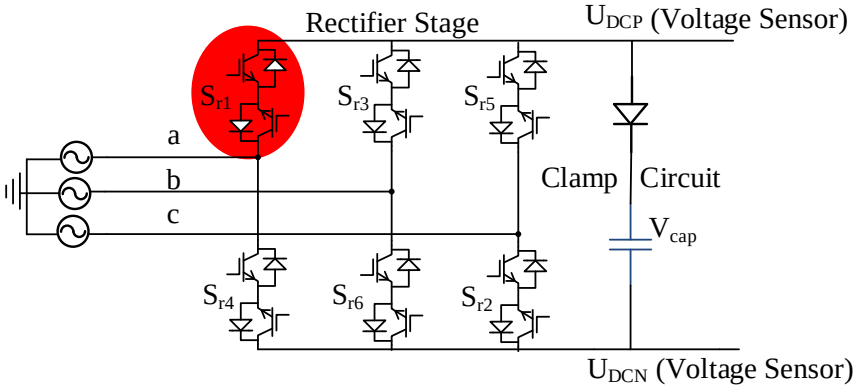


Figure 5.20: Rectifier stage of the indirect matrix converter system

Table 5.3: Rectifier stage faulty phase identification

	Normal opeartion	Top Switch fault	Bottom Switch fault
$\lvert U_{DCP} - {U_{DCP}}^* \rvert$	$< U_{th}$	$> U_{th}$	$< U_{th}$
$\lvert U_{DCN} - {U_{DCN}}^* \rvert$	$< U_{th}$	$< U_{th}$	$> U_{th}$

$$\begin{bmatrix} F_{r1} & F_{r3} & F_{r5} \\ F_{r4} & F_{r6} & F_{r2} \end{bmatrix} = \begin{bmatrix} F_P & 0 \\ 0 & F_N \end{bmatrix} \begin{bmatrix} S_{r1} & S_{r3} & S_{r5} \\ S_{r4} & S_{r6} & S_{r2} \end{bmatrix} \tag{5.53}$$

5.6 Summary

This chapter first introduces fault behaviour analysis under a bidirectional switch open circuit fault for both the direct and indirect matrix converter systems. Then three different single switch open circuit fault detection and diagnosis methods on matrix converter systems are proposed.

This chapter proposes a fault detection and diagnosis algorithm for the direct matrix converter system with SVM strategy. The advantage for doing fault detection and diagnosis with SVM strategy is that the switching frequency is fixed. The fixed switching frequency will make it easier to design the filter for the direct matrix converter system with SVM strategy than with FCS-MPC strategy, because the switching frequency is uncertain in FCS-MPC strategy. Another advantage for doing fault detection and diagnosis with SVM strategy is that the SVM algorithm computation burden is lower than the FCS-MPC algorithm. This advantage will reduce the control cost for SVM strategy compared to the FCS-MPC strategy.

This chapter also proposes a fault detection and diagnosis algorithm for the direct matrix converter system with the FCS-MPC strategy. The advantage of fault detection and diagnosis with the FCS-MPC strategy is that there is only one fixed switching state within one sampling period. So only one current sample is required within one sampling period. This current sensing requirement will allow a relatively low bandwidth for the output current sensor. The low bandwidth of the output current sensor could potentially

reduce the hardware cost.

Finally the chapter also proposes a fault detection and diagnosis algorithm for the indirect matrix converter system with FCS-MPC strategy. The advantage for using indirect matrix converter topology is that it will reduce the control complexity compared to the direct matrix converter. The control for the rectifier stage and the inverter stage is easier than the control of a direct matrix converter.

Chapter 6

Matrix Converter System Simulation Study and Results

6.1 Introduction

The purpose of the simulation study presented in this chapter is to analyze the behaviour of the direct matrix converter (DMC) and indirect matrix converter (IMC) under open circuit fault conditions. The fault diagnosis methods for the DMC presented in chapter 5 use the DMC output current signals to diagnose an open circuit switch fault. Therefore, it is important to know how the DMC output currents will recirculate in the clamp circuit when a bi-directional switch suffers from an open circuit fault. The fault diagnosis method for the IMC presented in chapter 5 uses the IMC voltage error signals to diagnose an open circuit switch fault. So knowing how the voltage signals will behave under an open circuit switch fault is necessary to locate the faulty switch.

This chapter presents the simulation results for both the DMC and the IMC systems using simulation software tools such as SYNOPSYS SABER and MATLAB/SIMULINK. The SYNOPSYS SABER is chosen to simulate the DMC output current recirculating behaviour in the clamp circuit when a bi-directional switch suffers from an open circuit fault. The advantage of using SYNOPSYS SABER is that device models are more accurate com-

pared to that in MATLAB/SIMULINK. The disadvantage of SYNOPSYS SABER is that the simulation time is longer than MATLAB/SIMULINK. The direct matrix converter system with the Space Vector Modulation (SVM) was also simulated with SYNOPSYS SABER. The direct matrix converter system with Finite-Control-Set Model Predictive Control (FCS-MPC) was simulated with the MATLAB/SIMULINK software. The indirect matrix converter system with the FCS-MPC strategy was also simulated with the MATLAB/SIMULINK software.

Fault behaviour analysis must has to be done first before designing a fault diagnosis method. So SYNOPSYS SABER was used at the beginning stage to investigate how the faulty phase current will recirculate through the clamp circuit in a DMC because SYNOPSYS SABER has very precise device model libraries. SVM strategy was implemented in the SYNOPSYS SABER DMC model. After the fault behaviour analysis is fully investigated, a FCS-MPC strategy was implemented in the MATLAB/SIMULINK model to reduce the simulation time because the device model libraries in MATLAB/SIMULINK is much simpler than those in SYNOPSYS SABER.

6.2 Direct Matrix Converter System Simulation and Results

6.2.1 Direct Matrix Converter System Simulation with Space Vector Modulation Strategy

The direct matrix converter system with the Space Vector Modulation (SVM) strategy has been simulated using the SYNOPSYS SABER software. The block diagram of the simulation model is shown in Figure 6.1. The simulation parameters for the direct matrix converter system are listed in Table 6.1. The three output current sensors are located ahead of the clamp circuit to measure the output currents of the direct matrix converter alone, as presented in the previous chapter. In order to eliminate the control influence on the fault diagnosis algorithm, open loop control is used throughout the simulation.

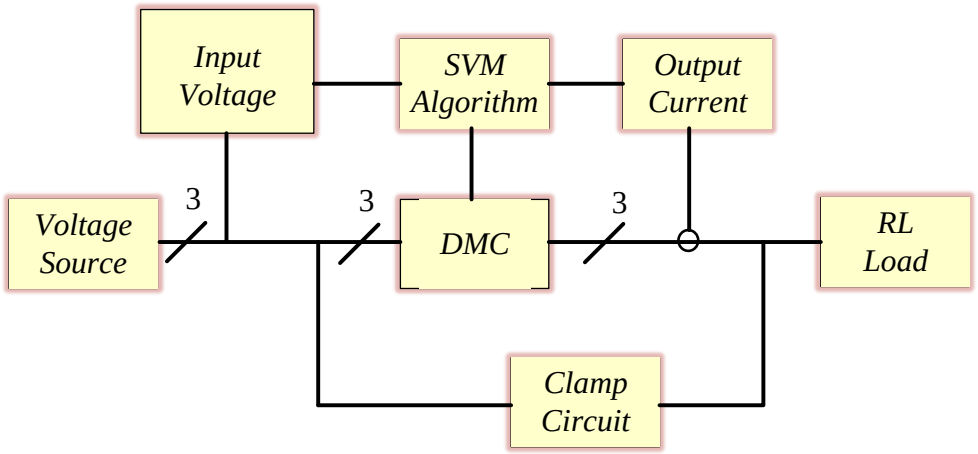


Figure 6.1: Direct matrix converter simulation block diagram with SVM strategy

Table 6.1: The simulation parameters of the direct matrix converter system with SVM strategy

Variables	Description	Value
U_{sm}	Amplitude AC Phase Voltage	$45[V]$
R_{load}	Load Resistor	$2.8[\Omega]$
L_{load}	Load Inductor	$17[mH]$
T_{sample}	Sampling Time	$80[\mu s]$
q	Modulation Index	0.5
I_{out}	Output Current Amplitude	$2.5[A]$
f_{out}	Output Current Frequency	$60[Hz]$

The direct matrix converter system with a clamp circuit is shown in the Figure 6.2. It can be seen from Figure 6.2 that there are three current sensors to measure the output three phase currents of the direct matrix converter. The clamp circuit comprises of 12 fast recovery diodes, D_1 to D_{12}, as shown in the Figure 6.2. The diodes current flowing through the corresponding diodes is indicated by i_{D1} to i_{D12}, as shown in the Figure 6.2.

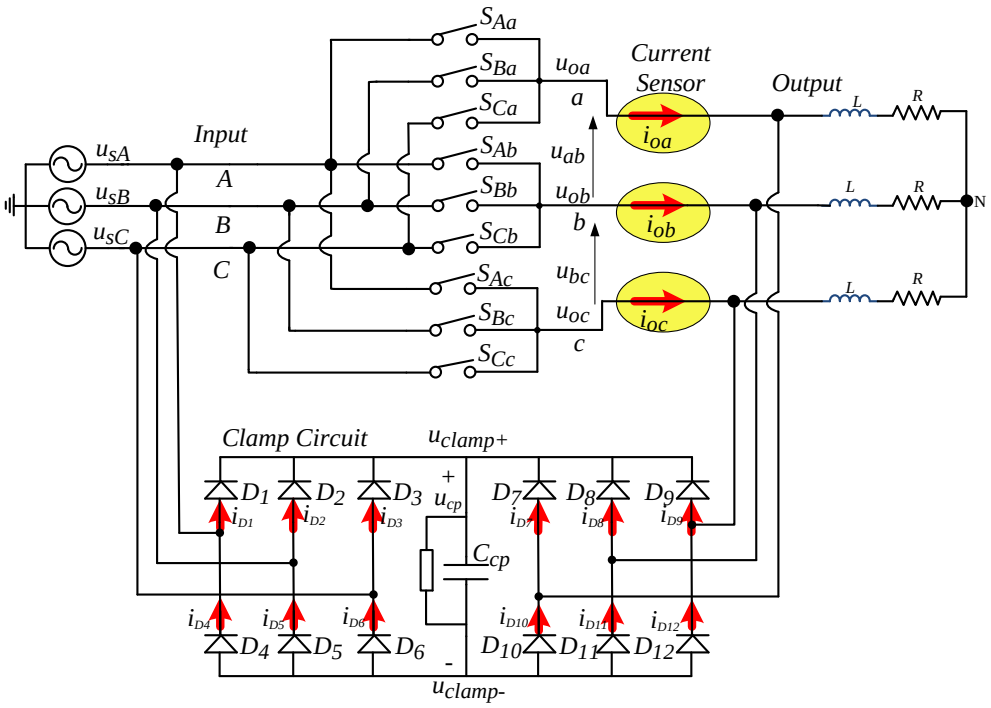


Figure 6.2: Direct matrix converter system with a clamp circuit

Normal Operation with SVM strategy

Under normal operating conditions with the SVM strategy, the input phase voltages u_s of the direct matrix converter system are as shown in Figure 6.3. The amplitude of u_s is set at $45V$ in order to be consistent with the experimental parameters. The frequency of the input voltage frequency is $50Hz$.

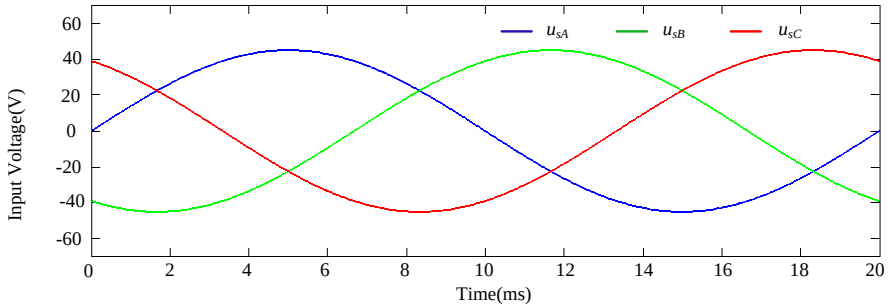


Figure 6.3: Direct matrix converter input source phase voltages with SVM strategy

The output phase voltage u_{oa} of the DMC with the SVM strategy is shown in Figure 6.4. It can be seen from Figure 6.4 that the output phase voltage u_{oa} is a piecewise waveform. This is because output phase a is connected to the input phases A, B and C by three bidirectional switches. For example, if the switch S_{Aa} is on, the output phase a will be connected to input phase A. If the switch S_{Ba} is on, the output phase a will be connected to input phase B. If the switch S_{Ca} is on, the output phase a will be connected to input phase C. A small voltage drop or increase in the output phase voltage u_{oa} can also been seen from Figure 6.4. This depends on the the direction of output current i_a and the voltage drop of the devices used in bi-directional switches.

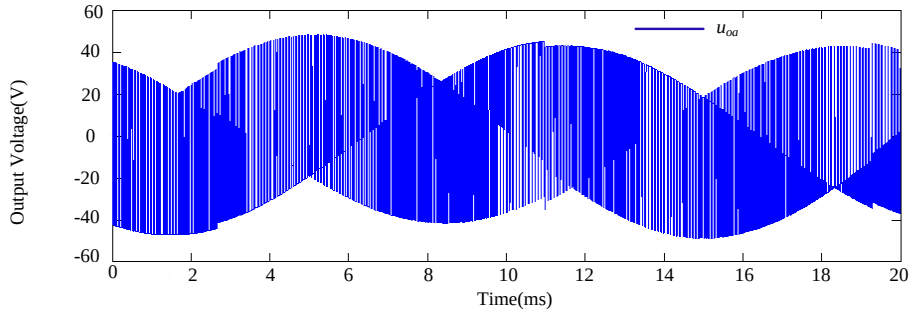


Figure 6.4: Direct matrix converter output phase voltage u_{oa} with SVM strategy

The output phase voltages u_{ob} and u_{oc} of the DMC with the SVM strategy

are shown in Figure 6.5 and Figure 6.6.

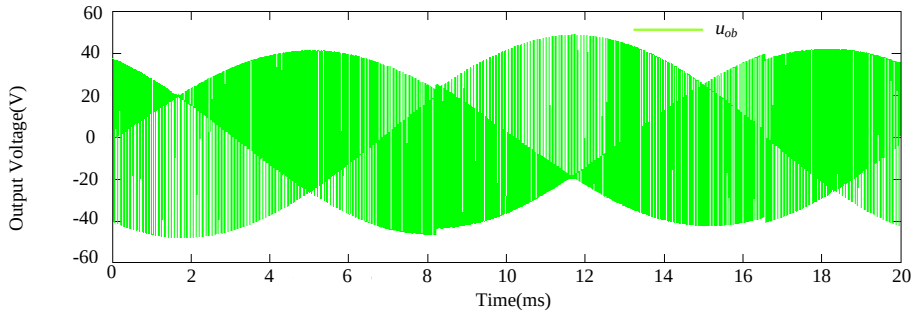


Figure 6.5: Direct matrix converter output phase voltage u_{ob} with SVM strategy

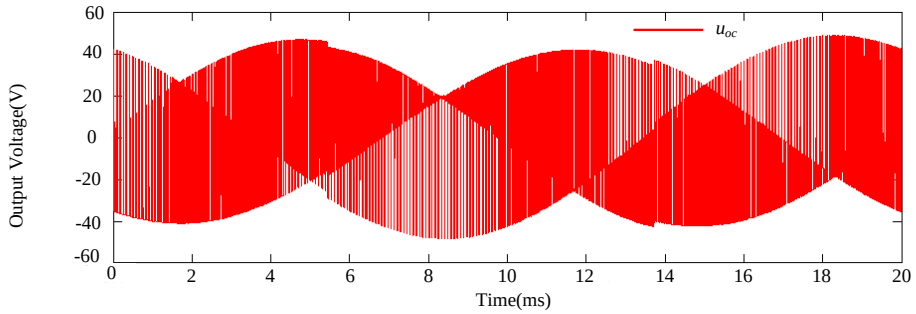


Figure 6.6: Direct matrix converter output phase voltage u_{oc} with SVM strategy

The three phase output currents i_o of the direct matrix converter are shown in Figure 6.7. The amplitude of i_o is modulated at $2.5A$ in order to be consistent with the experimental parameter presented in Chapter 8. The frequency of i_o is $60Hz$. The output currents are not ideal sinusoidal waveforms because the simulation model includes the voltage drop of the bi-directional switches. The voltage drop across the DMC as well as the edge uncertainty effect mentioned in [80] leads to the output current distortion.

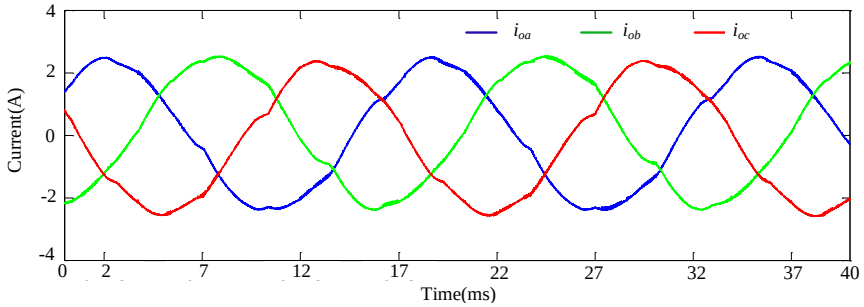


Figure 6.7: Direct matrix converter output currents with SVM strategy

Faulty Operation with SVM Strategy under A Switch S_{Aa} open circuit fault

Switch S_{Aa} is triggered to fail open circuited to show the output currents i_o behaviour under an open circuit fault condition. The output currents i_o of the direct matrix converter under an open circuit fault in switch S_{Aa} are shown in Figure 6.8. It can be seen from Figure 6.8 that switch S_{Aa} is triggered to fail open circuit at $1ms$. The three phase output currents become abnormal when the open circuit switch fault occurs.

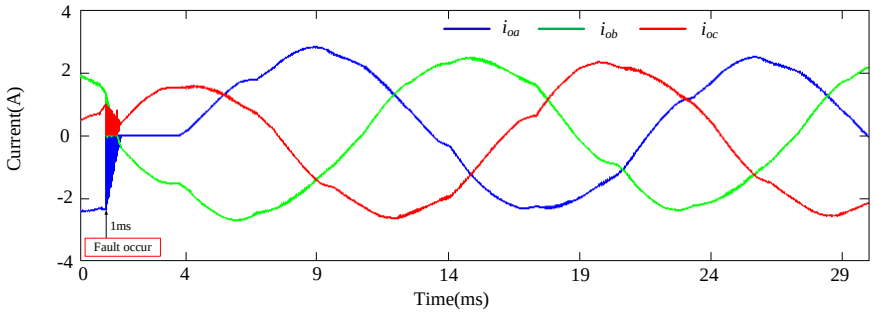


Figure 6.8: Direct matrix converter output currents i_o with SVM strategy under switch S_{Aa} open circuit condition

In order to see the behaviour of the output currents i_o clearly, the magnified output currents i_o of the direct matrix converter under an open circuit fault in switch S_{Aa} are shown in Figure 6.9. It can be seen from the Figure 6.9 that the output phase currents i_{oa}, i_{ob} and i_{oc} become zero when an open

circuit fault occurs at $0.175ms$. Then the output current i_{ob} becomes normal again at $0.183ms$. At $0.200ms$, output current i_{oc} becomes normal again. Therefore, the simulated output currents prove that the healthy phase output currents i_{ob} and i_{oc} will be influenced by faulty phase output current i_{oa} when switch S_{Aa} is suffering from an open circuit fault. When i_{ob} and i_{oc} become zero, a false diagnosis will occur if implementing the fault diagnosis method proposed in [15]. By implementing the fault diagnosis method proposed in chapter 5, a false diagnosis can be avoided.

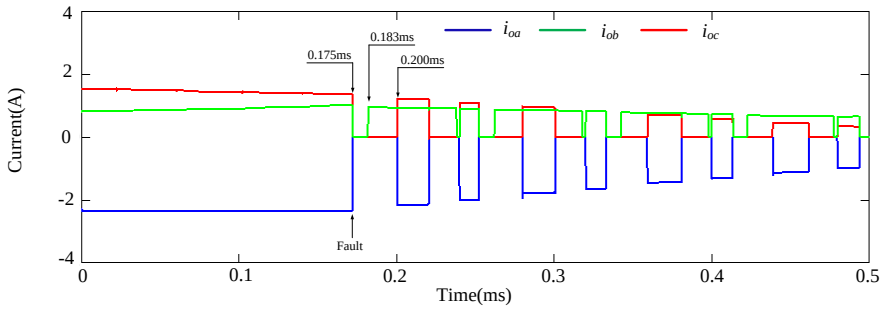


Figure 6.9: Direct matrix converter magnified output currents i_o with SVM strategy under switch S_{Aa} open circuit condition

The output current waveforms shown in Figure 6.9 can be further explained by analyzing the output current recirculating path through the clamp circuit. The current recirculating path through the clamp circuit can be derived by analyzing the currents flowing through the diodes of the clamp circuit. The currents flowing through the diodes are shown from Figure 6.10 to Figure 6.15.

The magnified clamp circuit diode currents i_{D1} and i_{D4} of the DMC with SVM strategy under an open circuit fault in switch S_{Aa} are shown in Figure 6.10. It can be seen from the Figure 6.10 that the diode current i_{D1} flowing through the diode D_1 is $0A$ from $0.175ms$ to $0.200ms$. The diode current i_{D4} flowing through the diode D_4 is $0A$ from $0.175ms$ to $0.183ms$. The diode current i_{D4} is around $0.95A$ from $0.183ms$ to $0.200ms$. Therefore, diode D_4 is conducting from $0.183ms$ to $0.200ms$ and diode D_1 is not conducting from $0.175ms$ to $0.200ms$.

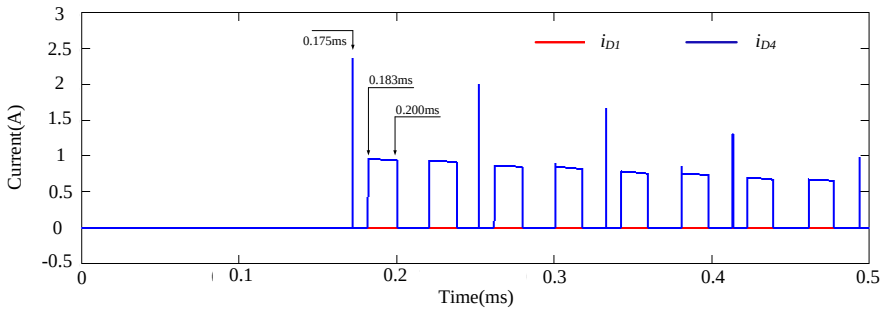


Figure 6.10: Direct matrix converter system magnified clamp circuit diode currents i_{D1} and i_{D4} with SVM strategy under switch S_{Aa} open circuit condition

The magnified clamp circuit diode currents i_{D2} and i_{D5} of the DMC with SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.11. It can be seen from the Figure 6.11 that the diode current i_{D2} flowing through the diode D_2 is $0A$ from $0.175ms$ to $0.200ms$. The diode current i_{D5} flowing through the diode D_5 is $0A$ from $0.175ms$ to $0.200ms$. Therefore, neither diode D_2 nor D_5 is conducting from $0.175ms$ to $0.200ms$.

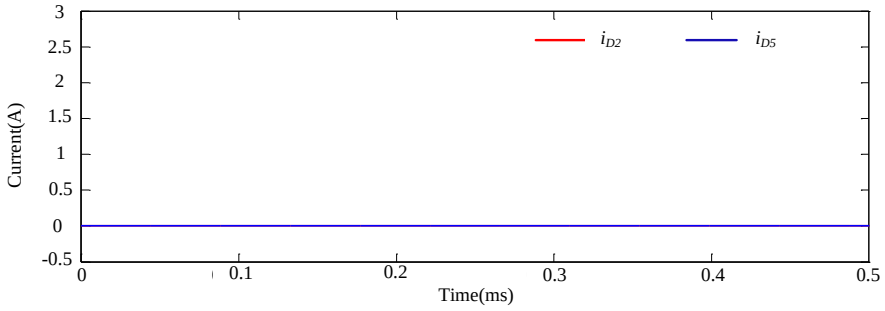


Figure 6.11: Direct matrix converter system magnified clamp circuit diode currents i_{D2} and i_{D5} with SVM strategy under switch S_{Aa} open circuit condition

The magnified clamp circuit diode currents i_{D3} and i_{D6} of the DMC with SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.12. It can be seen from the Figure 6.12 that the diode current i_{D3} flowing through the diode D_3 is $0A$ from $0.175ms$ to $0.200ms$. The diode current i_{D6}

flowing through the diode D_6 is $0A$ from $0.175ms$ to $0.200ms$. Therefore, neither diode D_3 nor D_6 is conducting from $0.175ms$ to $0.200ms$.

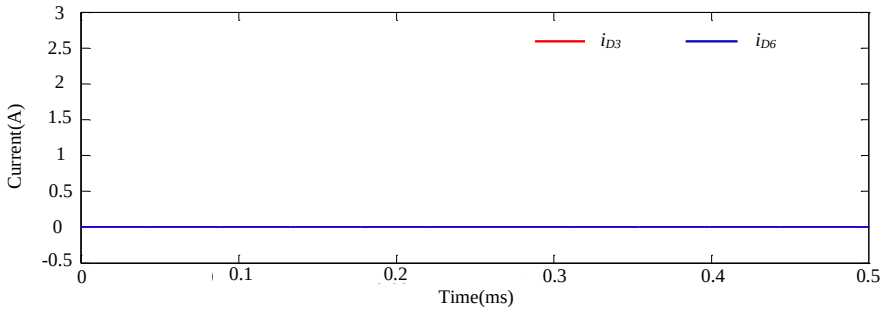


Figure 6.12: Direct matrix converter system magnified clamp circuit diode currents i_{D3} and i_{D6} with SVM strategy under switch S_{Aa} open circuit condition

The magnified clamp circuit diode currents i_{D7} and i_{D10} of the DMC with SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.13. It can be seen from the Figure 6.13 that the diode current i_{D7} flowing through the diode D_7 is around $2.2A$ from $0.175ms$ to $0.200ms$. The diode current i_{D10} flowing through the diode D_{10} is $0A$ from $0.175ms$ to $0.200ms$. Therefore, diode D_7 is conducting from $0.175ms$ to $0.200ms$ and diode D_{10} is not conducting from $0.175ms$ to $0.200ms$.

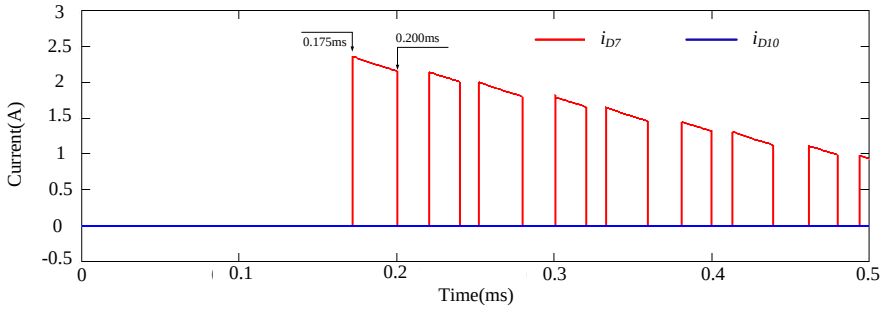


Figure 6.13: Direct matrix converter system magnified clamp circuit diode currents i_{D7} and i_{D10} with SVM strategy under switch S_{Aa} open circuit condition

The magnified clamp circuit diode currents i_{D8} and i_{D11} of the DMC with

SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.14. It can be seen from the Figure 6.14 that the diode current i_{D8} flowing through the diode D_8 is $0A$ from $0.175ms$ to $0.200ms$. The diode current i_{D11} flowing through the diode D_{11} is around $1.3A$ from $0.175ms$ to $0.200ms$. Therefore, diode D_{11} is conducting from $0.175ms$ to $0.200ms$ and diode D_8 is not conducting from $0.175ms$ to $0.200ms$.

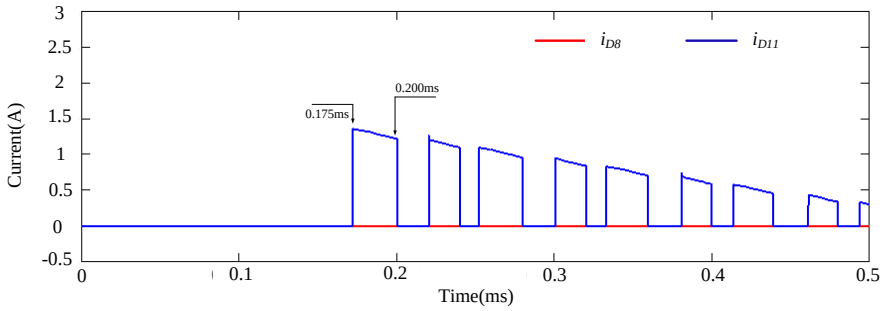


Figure 6.14: Direct matrix converter system magnified clamp circuit diode currents i_{D8} and i_{D11} with SVM strategy under switch S_{Aa} open circuit condition

The magnified clamp circuit diode currents i_{D9} and i_{D12} of the DMC with SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.15. It can be seen from the Figure 6.15 that the diode current i_{D9} flowing through the diode D_9 is $0A$ from $0.175ms$ to the time point $0.200ms$. The diode current i_{D12} flowing through the diode D_{12} is around $0.95A$ from $0.175ms$ to $0.183ms$. The diode current i_{D12} is $0A$ from $0.183ms$ to $0.200ms$. Therefore, diode D_{12} is conducting from $0.175ms$ to $0.183ms$ and diode D_{10} is not conducting from $0.175ms$ to $0.200ms$.

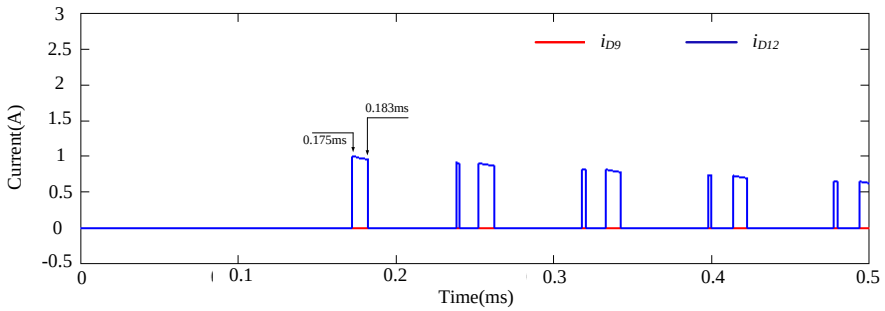


Figure 6.15: Direct matrix converter system magnified clamp circuit diode currents i_{D9} and i_{D12} with SVM strategy under switch S_{Aa} open circuit condition

According to the clamp circuit diode currents shown from Figure 6.10 to Figure 6.15, it can be seen that the faulty phase current i_{oa} will influence the healthy phase currents i_{ob} and i_{oc} by recirculating this current through the diode clamp circuit. Apart from the output currents, the current recirculating path in the diode clamp circuit also depends on the input and output voltages of the clamp circuit as discussed in section 5.2.2.

The magnified input voltages u_s of the direct matrix converter with SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.16. It can be seen from the Figure 6.16 that the input source voltage u_{sA} is $-39V$, u_{sB} is $-1V$ and u_{sC} is $+40V$ respectively when the switch S_{Aa} fails an open circuit. The input source voltages can be regarded as constant within one modulation period because the input frequency is usually $50Hz$ or $60Hz$, much lower than the modulation frequency which is around $10kHz$.

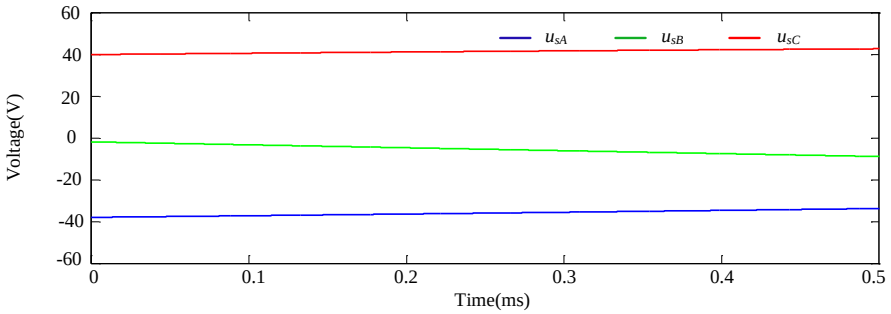


Figure 6.16: Direct matrix converter magnified input voltages u_s with SVM strategy under switch S_{Aa} open circuit condition

The magnified output phase voltage u_{oa} of the direct matrix converter with SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.17. It can be seen from the Figure 6.17 that the output phase voltage u_{oa} is $170V$ from $0.175ms$ to $0.200ms$. This means the faulty output phase voltage u_{oa} is clamped to the positive line of the clamp circuit from $0.175ms$ to $0.200ms$ because diode D_7 is conducting from $0.175ms$ to $0.200ms$.

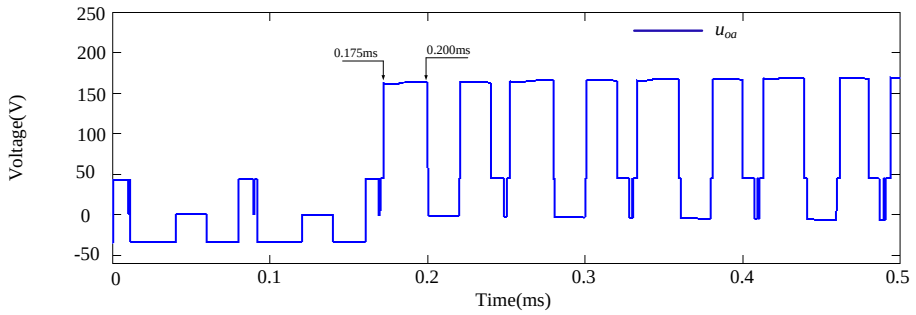


Figure 6.17: Direct matrix converter magnified output phase voltage u_{oa} with SVM strategy under switch S_{Aa} open circuit condition

The magnified output phase voltage u_{ob} of the direct matrix converter with SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.18. It can be seen from the Figure 6.18 that the output phase voltage u_{ob} is $-39V$ from $0.175ms$ to $0.200ms$. This means switch S_{Ab} turns on from $0.175ms$ to $0.200ms$ and connects the input phase A with the output phase b.

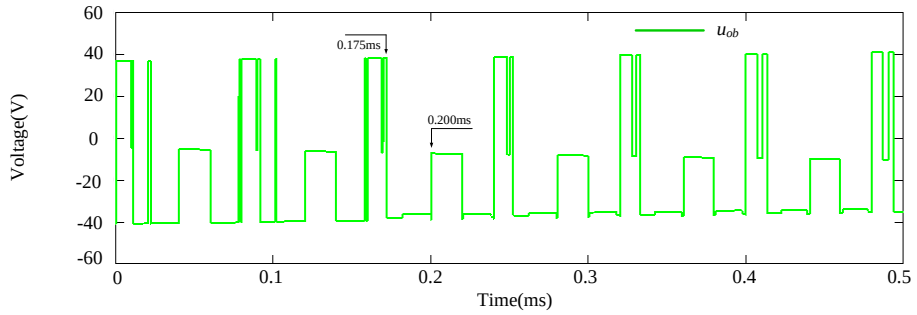


Figure 6.18: Direct matrix converter magnified output phase voltage u_{ob} with SVM strategy under switch S_{Aa} open circuit condition

The magnified output phase voltage u_{oc} of the direct matrix converter with SVM strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.19. It can be seen from the Figure 6.19 that the output phase voltage u_{oc} of the direct matrix converter is $-39V$ from $0.175ms$ to $0.183ms$. The output phase voltage u_{oc} is $+40V$ from $0.183ms$ to $0.200ms$. This means that switch S_{Ac} turns on from $0.175ms$ to $0.183ms$ and connects the input phase A with the output phase c. Switch S_{Cc} turns on from $0.183ms$ to $0.200ms$ and connects the input phase C with the output phase c.

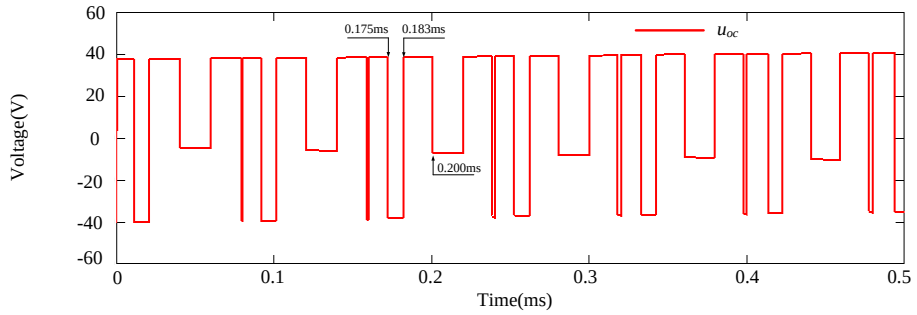


Figure 6.19: Direct matrix converter magnified output phase voltage u_{oc} with SVM strategy under switch S_{Aa} open circuit condition

In order to analyze the waveforms presented above, the clamp circuit diode current waveforms and their characteristics are summarized in Table 6.2. The input voltage, output voltage and clamp circuit voltage waveforms are summarized in Table 6.3.

Table 6.2: Faulty operation waveforms summary 1

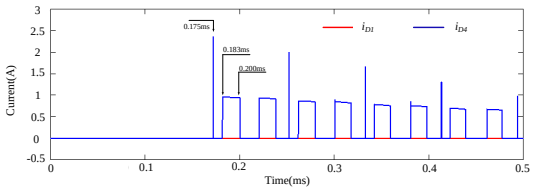
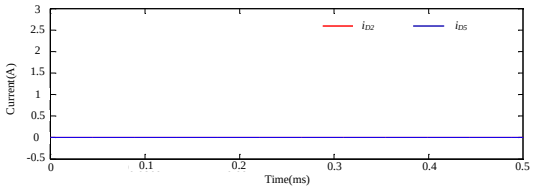
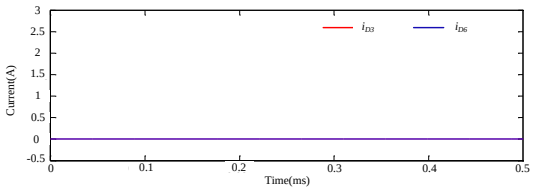
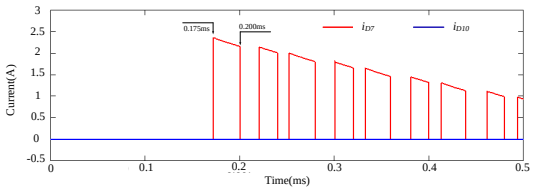
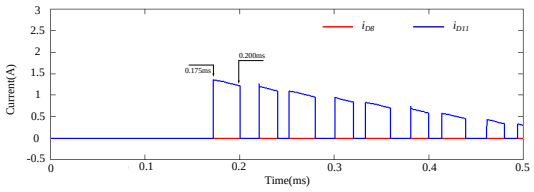
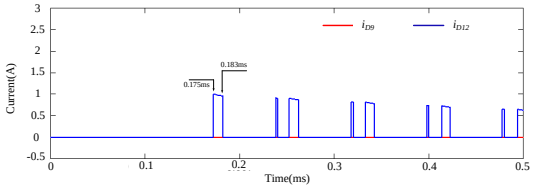
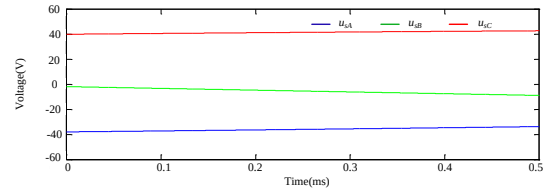
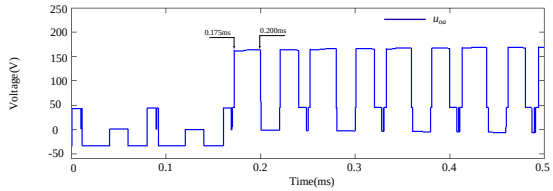
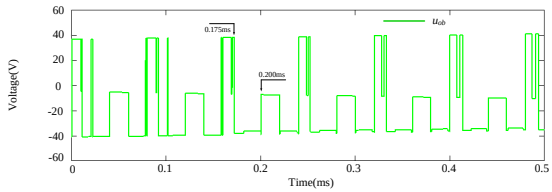
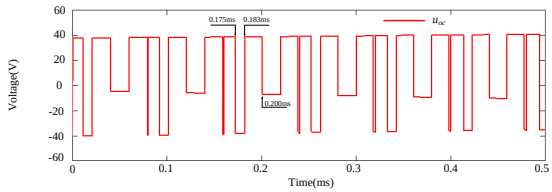
Waveforms	Characteristics
	• D_4 conducts from $0.183ms$ to $0.200ms$.
	• D_2 and D_5 conduct from $0.175ms$ to $0.200ms$.
	• D_3 and D_6 not conduct from $0.175ms$ to $0.200ms$.
	• D_7 conducts from $0.175ms$ to $0.200ms$.
	• D_{11} conducts from $0.175ms$ to $0.200ms$.
	• D_{12} conducts from $0.175ms$ to $0.183ms$.

Table 6.3: Faulty operation waveforms summary 2

Waveforms	Characteristics
	• $u_{sA} = -39V$,$u_{sB} = -1V$,$u_{sC} = +40V$.
	• u_{oa} is $170V$ from $0.175ms$ to $0.200ms$.
	• u_{ob} is $-39V$ from $0.175ms$ to $0.200ms$.
	• u_{oc} is $-39V$ from $0.175ms$ to $0.183ms$. • u_{oc} is $+40V$ from $0.183ms$ to $0.200ms$.

According to the waveforms shown above, the faulty phase current i_{oa} recirculating path under a switch S_{Aa} open circuit fault condition can be determined. From $0.175ms$ to $0.183ms$, the clamp circuit diodes D_7, D_{11} and D_{12} are conducting. Combining the information of the input voltage, the output current and the switching state from $0.175ms$ to $0.183ms$, it can be seen that the faulty phase current i_{oa} is recirculating, as shown in the Figure 6.20. This type of faulty phase current i_{oa} recirculating path can explain why the three phase output currents i_{oa}, i_{ob} and i_{oc} are all zero from $0.175ms$ to $0.183ms$. This is because in this type of current recirculating path, the amplitude of faulty phase current ${i_{oa}}^{k-1}$ at the modulation period ${T_s}^{k-1}$ is the largest absolute value among the three output currents. The switch S_{Aa} occurs open circuit fault at the beginning of the modulation period ${T_s}^{k}$ at $0.175ms$. Therefore, the faulty phase current i_{oa} can provide current for both the load phase b and the load phase c because ${i_{oa}}^{k-1}$ is the biggest absolute value.

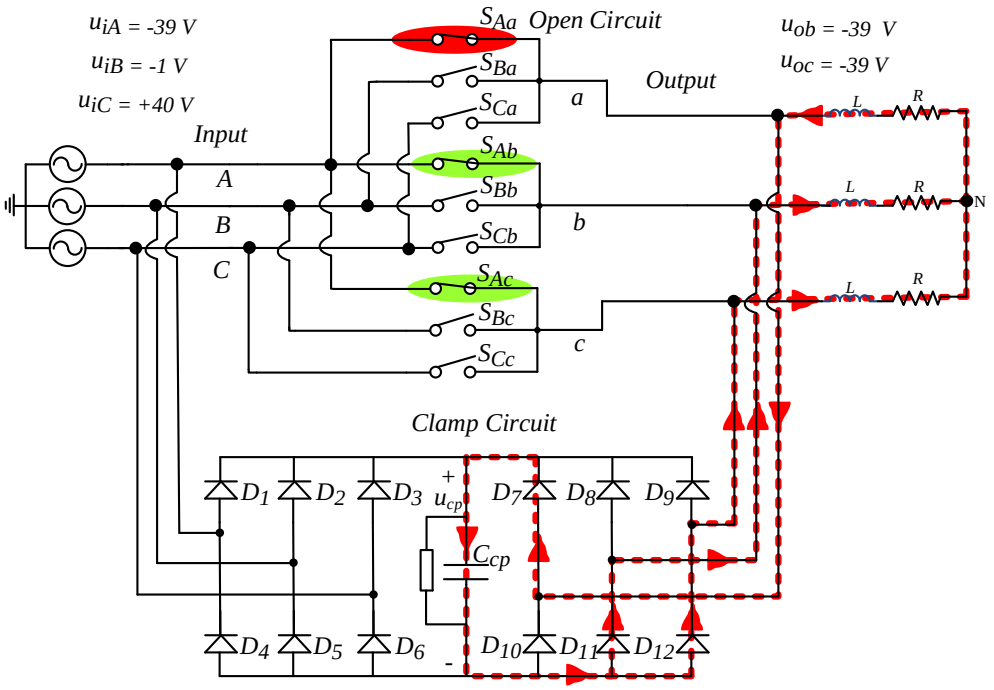


Figure 6.20: The faulty phase current i_{oa} recirculating path under the switch S_{Aa} open circuit fault condition from the time point $0.175ms$ to the time point $0.183ms$.

From time $0.183ms$ to $0.200ms$, the clamp circuit diodes D_4, D_7 and D_{11} are conducting. Combining the information of the input voltage, the output current and the switching state from $0.183ms$ to $0.200ms$, it can be seen that the faulty phase current i_{oa} is recirculating, as shown in the Figure 6.21. This type of faulty phase current i_{oa} recirculating path can explain why output current i_{oa} and i_{ob} are zero, but output current i_{oc} is not zero from $0.183ms$ to $0.200ms$. This is because in this type of current recirculating path, the amplitude of faulty phase current ${i_{oa}}^{k-1}$ at the modulation period ${T_s}^{k-1}$ is the biggest absolute value among the three output currents. Switch S_{Aa} is failing as an open circuit fault in the modulation period ${T_s}^{k}$ from $0.183ms$ to $0.200ms$. Therefore, the faulty phase current i_{oa} can provide current for load phase b because the clamp circuit diode D_{11} is conducting. However, the faulty phase current i_{oa} can not provide current for load phase c because

the clamp circuit diode D_4 is conducting.

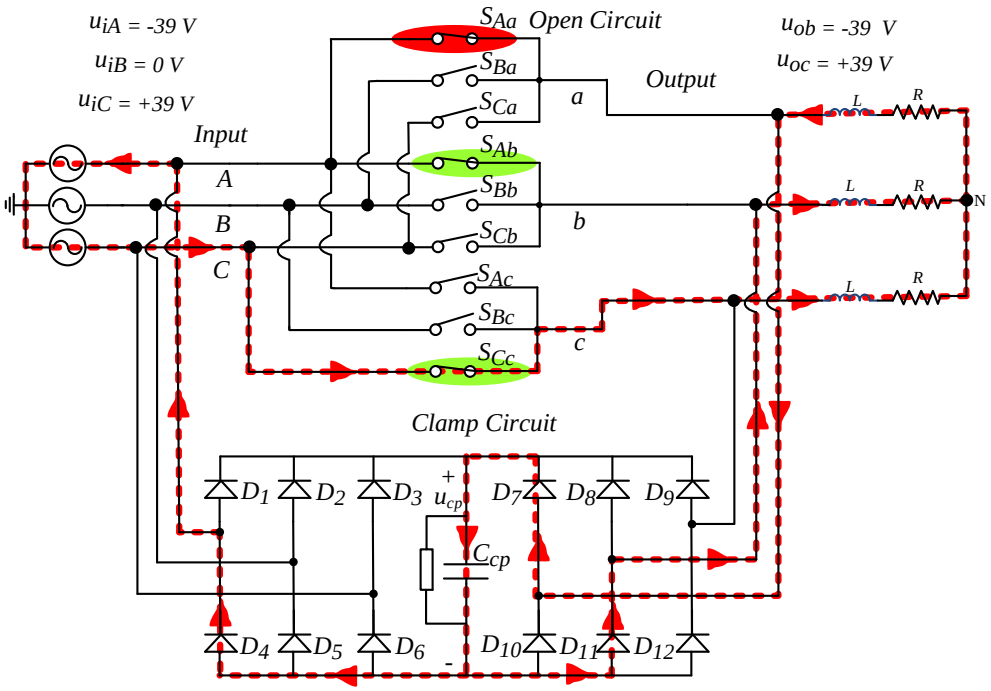


Figure 6.21: The faulty phase current i_{oa} recirculating path under the switch S_{Aa} open circuit fault condition from the time point $0.183ms$ to the time point $0.200ms$.

6.2.2 Direct Matrix Converter System Simulation with FCS-MPC Strategy

The direct matrix converter system with the FCS-MPC strategy has been simulated with MATLAB/SIMULINK software. The block diagram of the simulation model is shown in Figure 6.22. The simulation parameters of the direct matrix converter system with FCS-MPC strategy are listed in Table 6.4. The three output current sensors are located ahead of the clamp circuit to measure the output currents of the direct matrix converter.

As shown in Figure 6.22, the electronic parts modeling such as DMC and clamp circuit uses the SIMSCAPE library. The FCS-MPC algorithm

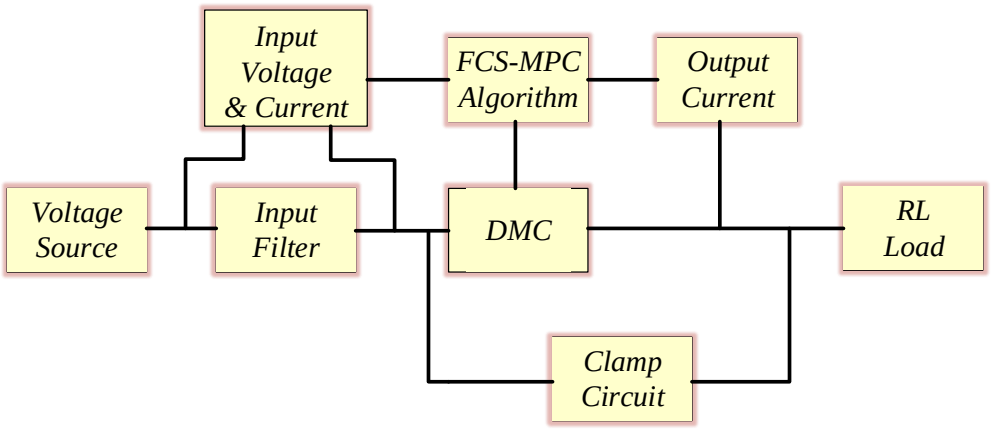


Figure 6.22: Direct matrix converter simulation block diagram with FCS-MPC strategy

is implemented in a S-Function block in the simulink model to realize the control purpose.

Table 6.4: The simulation parameters of the direct matrix converter system with FCS-MPC strategy

Variables	Description	Value
U_{sm}	Amplitude AC Phase Voltage	$50[V]$
L_f	Input Filter Inductor	$273[\mu H]$
C_f	Input Filter Capacitor	$72[\mu F]$
R_f	Input Filter Resistor	$0.08[\Omega]$
R_{load}	Load Resistor	$12[\Omega]$
L_{load}	Load Inductor	$17[mH]$
T_{sample}	Sampling Time	$100[\mu s]$
I_{out}	Output Current Amplitude	$2.5[A]$
f_{out}	Output Current Frequency	$60[Hz]$

Normal Operation with FCS-MPC strategy

Under normal operating condition with the FCS-MPC strategy, the input source three phase voltages u_s of the direct matrix converter system are shown in Figure 6.23. The amplitude of the u_s is set as $50V$ to be consistent with the experimental parameters. The frequency of the u_s is set as $50Hz$.

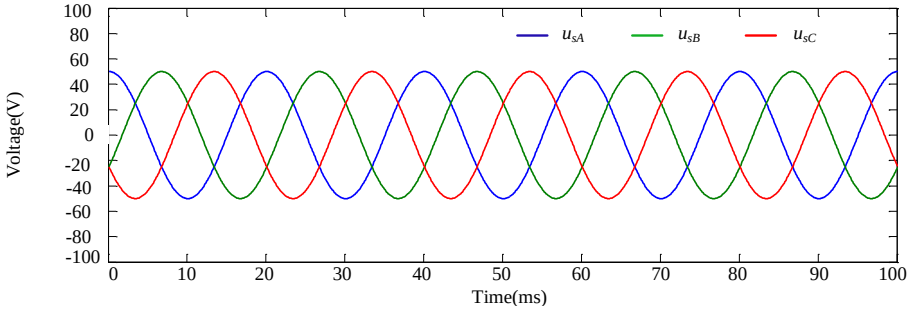


Figure 6.23: Direct matrix converter input source voltages with FCS-MPC strategy

The output three phase currents i_o of the direct matrix converter system is shown in Figure 6.24. The amplitude of the i_o is modulated at $2.5A$ to be consistent with the experimental parameters. The frequency of the i_o is set as $60Hz$.

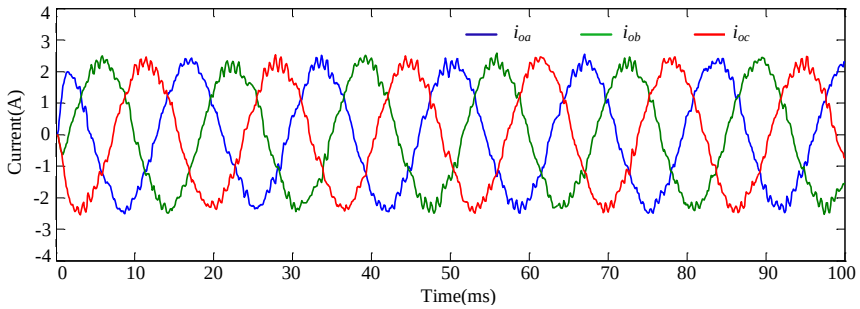


Figure 6.24: Direct matrix converter output currents with FCS-MPC strategy

The input source three phase currents i_s of the direct matrix converter with FCS-MPC strategy are shown in Figure 6.25. The applied FCS-MPC strategy use input current and output current as cost function factors. The input current and output current are coupled by the direct matrix converter. There is a trade-off between the input current quality and output current quality. In this theis, the weighting factor λ is set to 0.2, which gives the output currents priority over the input source currents. There is distortion in the input current waveform. This distortion adds noise into the DMC system, which helps to test the proposed fault diagnosis algorithm under noisy condition.

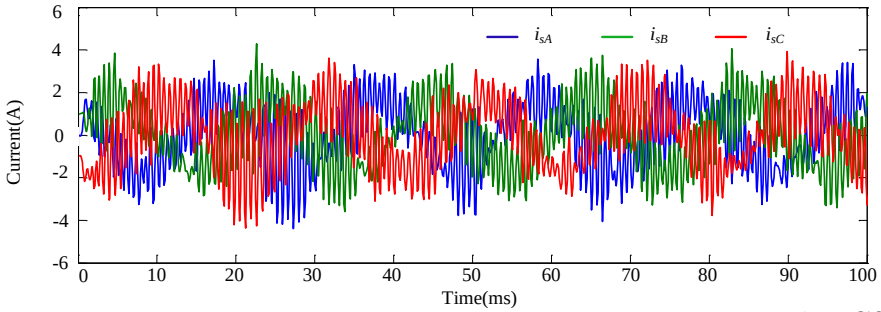


Figure 6.25: Direct matrix converter input source currents with FCS-MPC strategy

The output phase to phase voltage u_{oab} of the direct matrix converter system are shown in Figure 6.26. The output phase to phase voltage u_{obc}

of the direct matrix converter system with FCS-MPC strategy is shown in Figure 6.27. The output phase to phase voltage u_{oca} of the direct matrix converter system are shown in Figure 6.28.

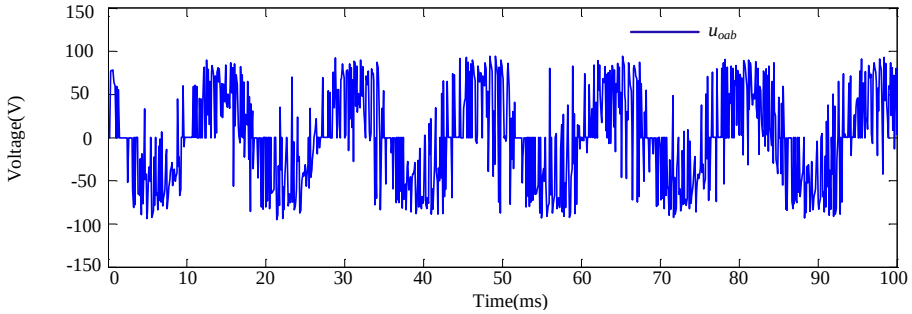


Figure 6.26: Direct matrix converter output phase to phase voltage u_{oab} with FCS-MPC strategy

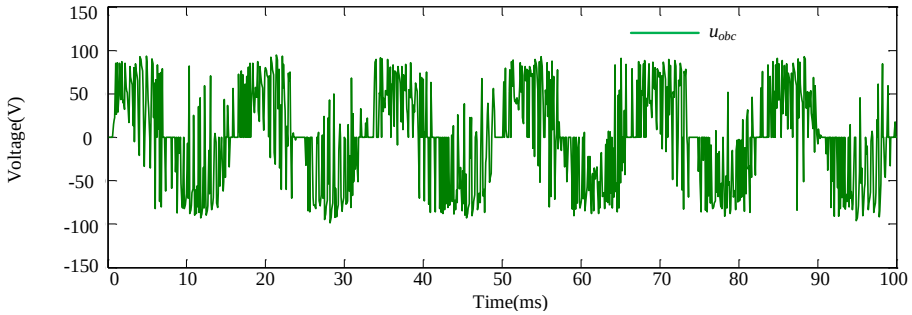


Figure 6.27: Direct matrix converter output phase to phase voltage u_{obc} with FCS-MPC strategy

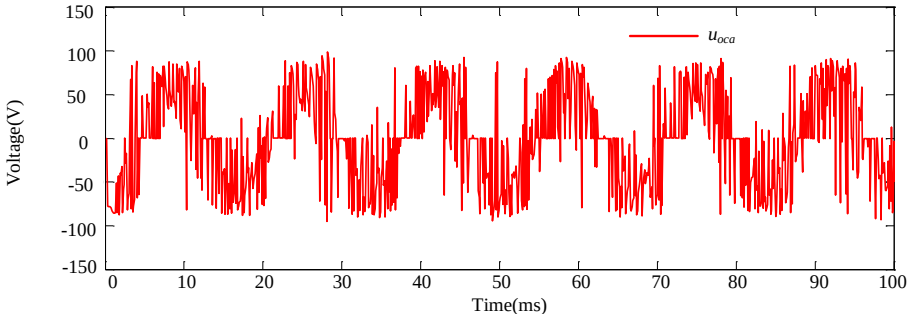


Figure 6.28: Direct matrix converter output phase to phase voltage u_{oca} with FCS-MPC strategy

Faulty Operation with FCS-MPC Strategy under Switch S_{Aa} open circuit fault

In order to analyze the open circuit fault behaviour of the DMC with a FCS-MPC strategy, a switch should be triggered to be open circuit for some time. The switch S_{Aa} is triggered to fail open circuit for $5ms$ in one output period to show the output currents i_o behaviour under an open circuit fault condition. The output currents i_o of the direct matrix converter system with FCS-MPC strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.29. The sampling time for this simulation is set as $100us$ in order to be consistent with the experimental parameters.

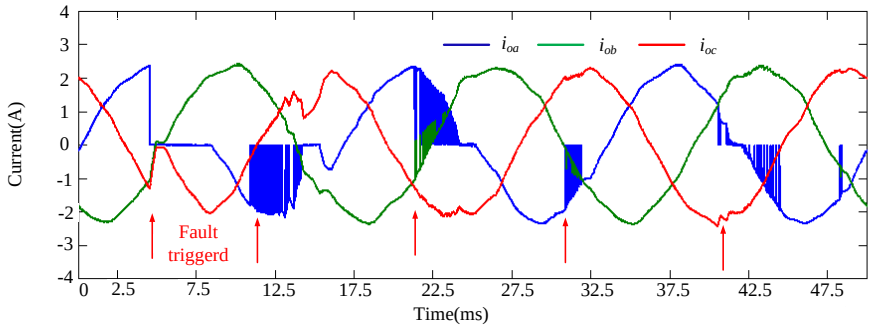


Figure 6.29: Direct matrix converter output currents i_o with FCS-MPC strategy under switch S_{Aa} open circuit condition with 100us sampling time

The magnified output currents i_o of the direct matrix converter using the

FCS-MPC strategy under an open circuit fault in switch S_{Aa} is shown in Figure 6.30.

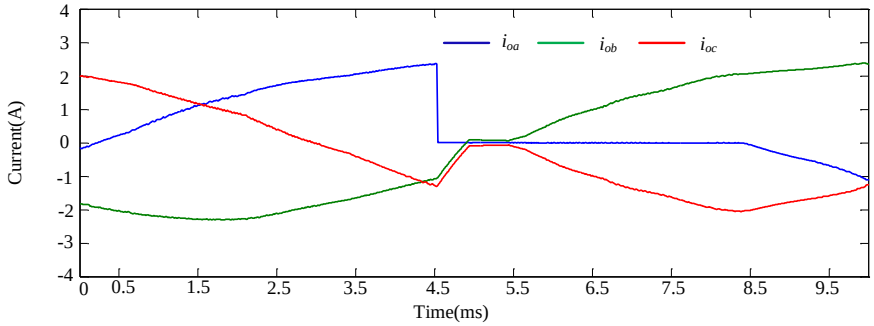


Figure 6.30: Direct matrix converter magnified output currents i_o with FCS-MPC strategy under switch S_{Aa} open circuit condition with 100us sampling time

The simulation results show that once bidirectional switch S_{Aa} fails open circuit, the faulty output phase current i_{oa} of the direct matrix converter will become zero as shown in Figure 6.30. In addition, the healthy output phase currents i_{ob} and i_{oc} could become zero as well because the faulty phase current recirculating in the clamp circuit will influence the healthy output phase current of the direct matrix converter.

6.3 Indirect Matrix Converter System Simulation and Results

The indirect matrix converter circuit is shown in the Figure 6.31. It can be seen from Figure 6.31 that the indirect matrix converter topology is composed of a matrix rectifier stage and an inverter stage. The rectifier stage and the inverter stage are connected by a fictitious DC-Link. The clamp circuit is comprised of a diode and a capacitor. This section will present the simulation results for the indirect matrix converter under normal operation conditions. This section will also present the simulation results of the indirect matrix converter under device switch open circuit fault operation conditions. The

indirect matrix converter system is simulated using MATLAB/SIMULINK.

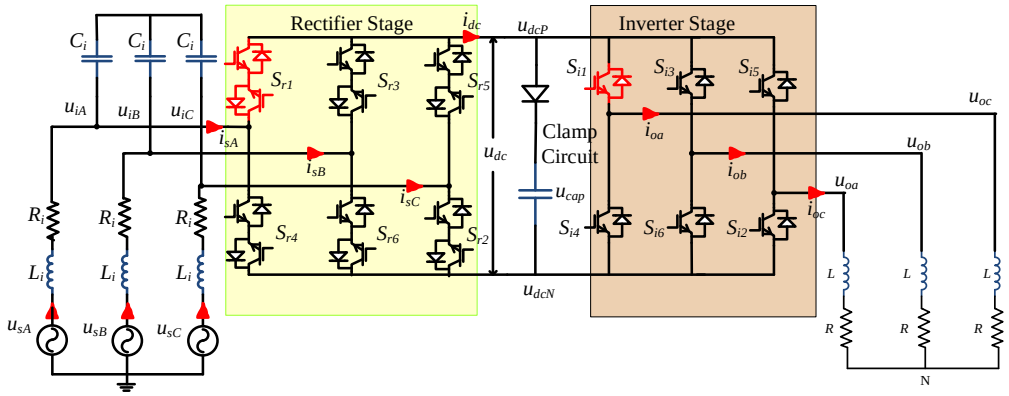


Figure 6.31: Indirect matrix converter system

6.3.1 Indirect Matrix Converter System Simulation with Model Predictive Control Strategy

The block diagram of the simulation model for the indirect matrix converter is shown in Figure 6.32. The simulation parameters for the indirect matrix converter system using FCS-MPC strategy are given in Table 6.5. There are two additional voltage sensors to measure the voltages u_{dcp} and u_{dcn} in order to do fault detection and diagnosis in the indirect matrix converter when an open circuit fault occurs in any device. u_{dcp} is the voltage between the DC-Link positive line and the input source neutral point. u_{dcn} is the voltage between the DC-Link negative line and the input source neutral point.

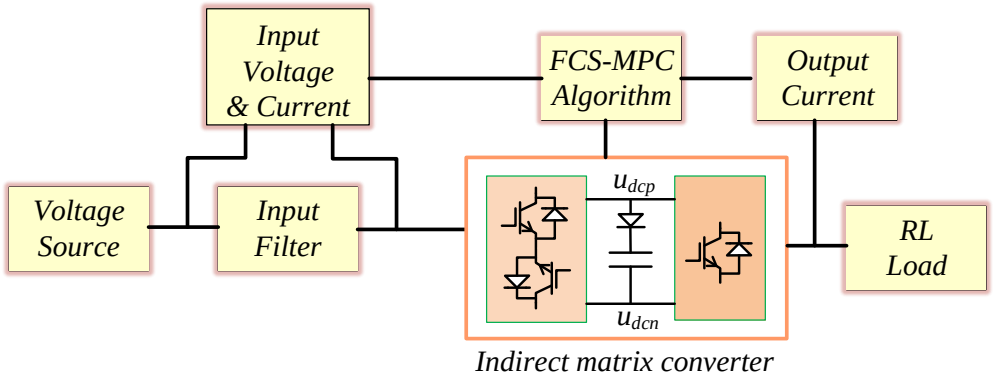


Figure 6.32: Indirect matrix converter output currents with FCS-MPC strategy

Table 6.5: The simulation parameters of the indirect matrix converter system with FCS-MPC strategy

Variables	Description	Value
U_{sm}	Amplitude AC Phase Voltage	$311[V]$
L_f	Input Filter Inductor	$400[\mu H]$
C_f	Input Filter Capacitor	$63[\mu F]$
R_f	Input Filter Resistor	$0.5[\Omega]$
R_{load}	Load Resistor	$10[\Omega]$
L_{load}	Load Inductor	$10[mH]$
T_{sample}	Sampling Time	$50[\mu s]$
I_{out}	Output Current Amplitude	$10[A]$
f_{out}	Output Current Frequency	$50[Hz]$
	Simulation Step	$1[us]$

If the fictitious inverter stage switch S_{i1} fails open circuit, the output current i_o of the indirect matrix converter is as shown in Figure 6.33. In this example, the amplitude of the output current is $10A$ before the open circuit switch fault occurs.

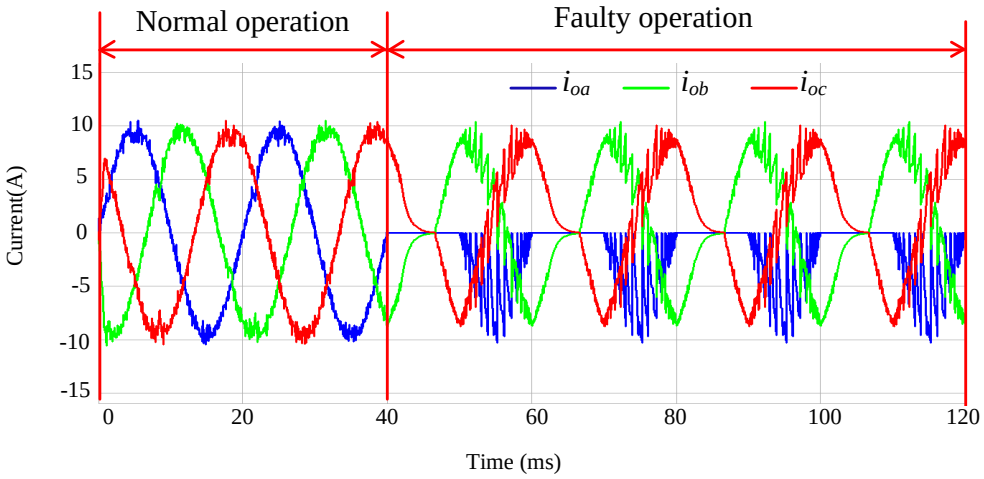


Figure 6.33: The output currents under S_{i1} fails open circuit

When the fictitious inverter stage switch S_{i1} fails open circuited, the fictitious DC-Link voltages u_{dcp} and u_{dcn} are as shown in Figure 6.34. It can be seen from the waveforms that the amplitude of the DC-Link voltages u_{dcp} and u_{dcn} do not change significantly.

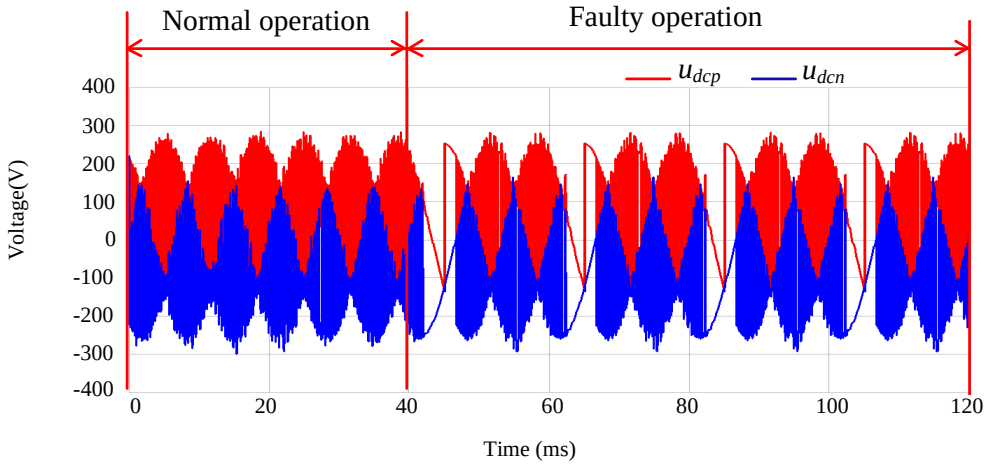


Figure 6.34: The fictitious DC-Link voltages under S_{i1} fails open circuit

The output error voltages ε_{ab}, ε_{bc} and ε_{ca} are the difference between the estimated output line-to-line voltages and the FCS-MPC algorithm predicted line-to-line output voltages. When the fictitious inverter stage switch S_{i1} fails open circuit, the output error voltages ε_{ab}, ε_{bc} and ε_{ca} are as shown in Figure 6.35. It can be seen from Figure 6.35 that the amplitude of the output error voltages increase significantly when the switch S_{i1} fails open circuit.

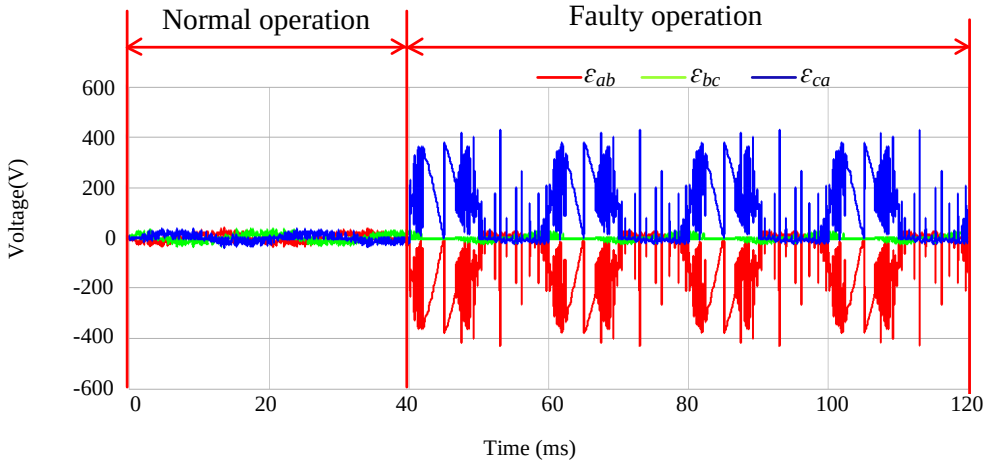


Figure 6.35: The output error voltages under S_{i1} fails open circuit

The magnified waveform of the output error voltages ε_{ab}, ε_{bc} and ε_{ca} are

shown in Figure 6.36 when the switch S_{i1} has an open circuit fault. The open circuit fault occurs at $40.0ms$. It can be seen from the Figure 6.36 that the amplitude of the output error voltages will exceed a defined threshold value within $100us$.

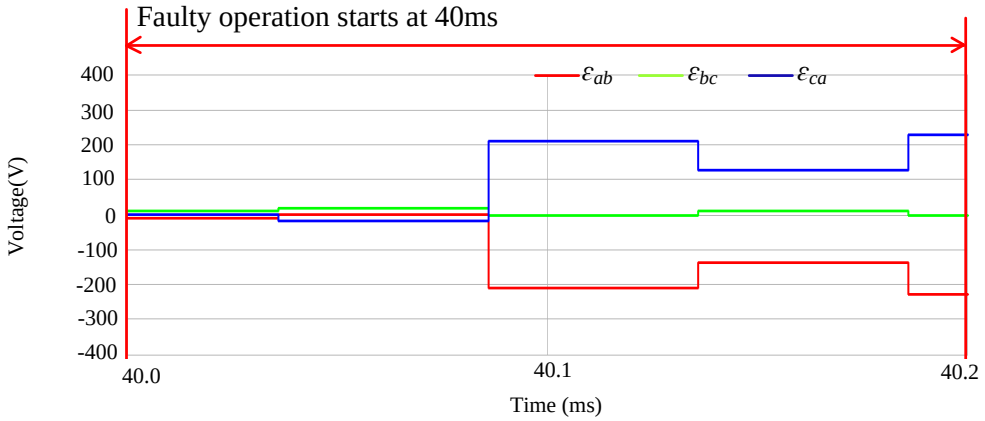


Figure 6.36: The magnified output error voltages under S_{i1} fails open circuit

Combined with the information of the DC-Link voltages u_{dcp} and u_{dcn}, it can be seen that the rectifier stage switches are healthy because the DC-Link voltages do not exceed the defined voltage threshold. Therefore, the output error voltages mean that an open circuit fault in the fictitious inverter stage can be detected within $100us$.

If the fictitious rectifier stage switch S_{r1} fails open circuit, the output currents under S_{r1} fails open circuit are shown in Figure 6.37. In this example, the switch S_{r1} fails open circuit fault at $57ms$.

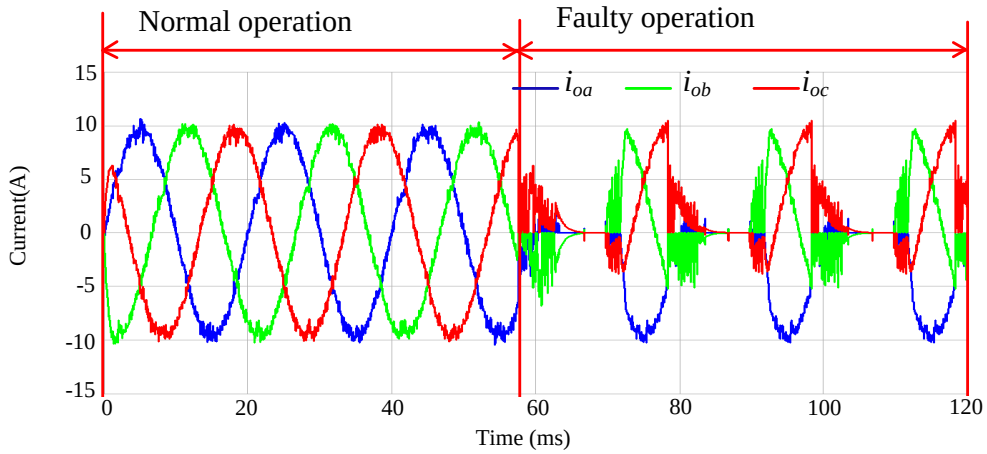


Figure 6.37: The output currents under S_{r1} fails open circuit

The output error voltages ε_{ab}, ε_{bc} and ε_{ca} are shown in Figure 6.38 for the case which the switch S_{r1} is open circuit. It can be seen from Figure 6.38 that the amplitude of the output error voltages increase significantly when switch S_{r1} fails open circuit. However, the DC-Link voltages u_{dcp} and u_{dcn} have to be considered before making the detection because the rectifier stage and the inverter stage are not decoupled in the indirect matrix converter circuit.

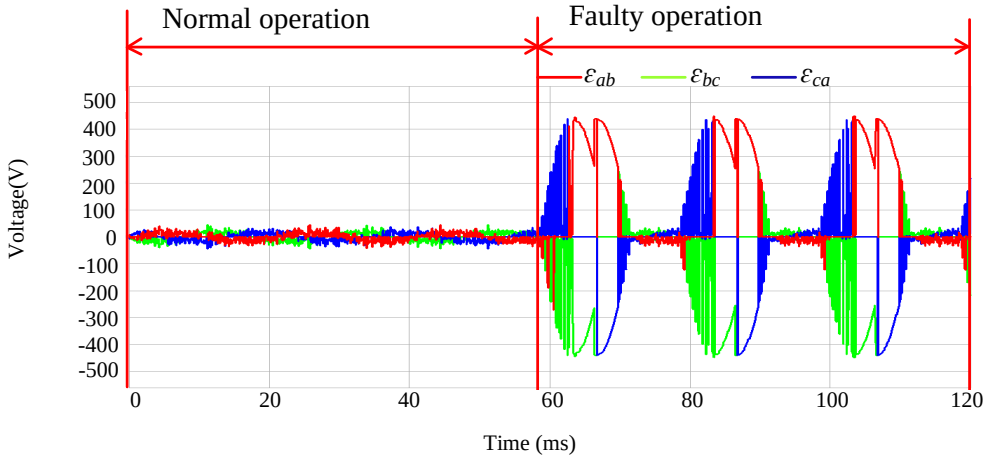


Figure 6.38: The output error voltages under S_{r1} fails open circuit

The fictitious DC-Link voltages u_{dcp} and u_{dcn} are shown in Figure 6.39

when switch S_{r1} fails open circuit. It can be seen from the waveforms that the amplitude of the DC-Link voltage u_{dcp} increases significantly after the switch S_{r1} fails open circuit, therefore allowing easy detection of the fault.

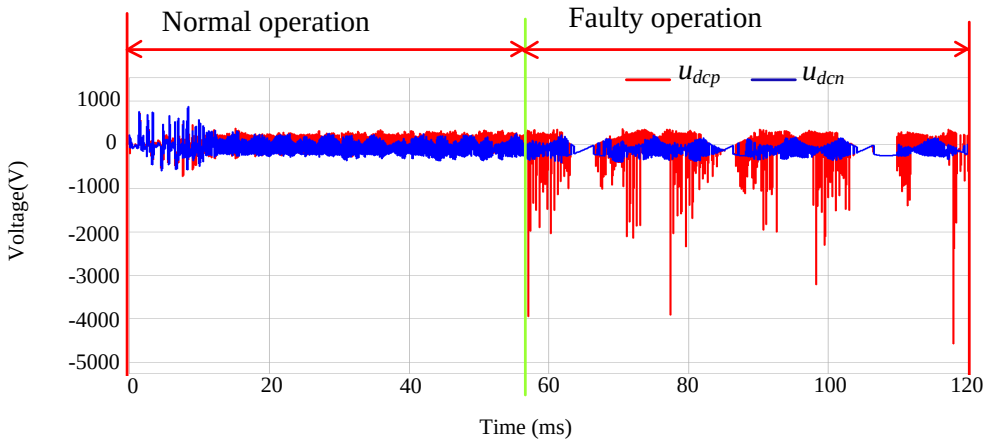


Figure 6.39: The fictitious DC-Link voltages under S_{r1} fails open circuit

The magnified fictitious DC-Link voltages u_{dcp} and u_{dcn} are shown in Figure 6.40 when the switch S_{r1} fails as an open circuit. In this example, the open circuit fault occurs at $57.0ms$. It can be seen from Figure 6.36 that the amplitude of the DC-Link positive line voltage u_{dcp} will exceed the defined voltage threshold value within $100us$.

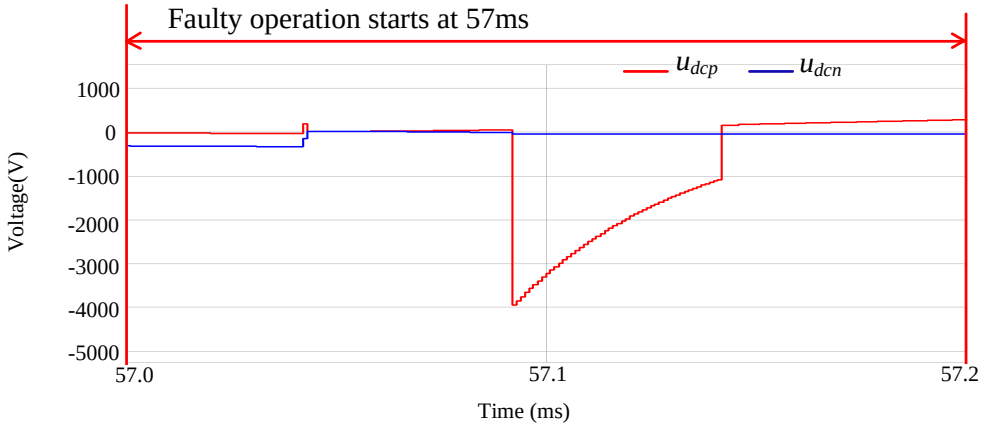


Figure 6.40: The magnified fictitious DC-Link voltages under S_{r1} fails open circuit

Combining with the information of the output error voltages, it can be seen that both the DC-Link voltages and the output error voltages exceed defined threshold value. This section focuses on a single switch open circuit fault, which can always be detected within $100us$.

6.4 Summary

This chapter presents the simulation results for the direct matrix converter system with SVM strategy. The simulation results for an bidirectional switch open circuit fault prove that the faulty output phase current recirculating path in the clamp circuit proposed in the previous chapter is viable. The simulation results also prove the feasibility of the proposed fault detection and diagnosis method proposed in the previous chapter.

This chapter also presents simulation results for the direct matrix converter system using the FCS-MPC strategy. The simulation results showing bidirectional switch open circuit fault prove the feasibility of the proposed fault detection and diagnosis method proposed in the previous chapter.

Finally, this chapter presents the simulation results for the indirect matrix converter system using the FCS-MPC strategy. The simulation results for bidirectional switch open circuit fault in the rectifier stage prove the feasi-

bility of the proposed fault detection and diagnosis method proposed in the previous chapter. The simulation results under an unidirectional switch open circuit fault in the inverter stage prove the feasibility of the proposed fault detection and diagnosis method also proposed in the previous chapter.

Chapter 7

Experimental Results

7.1 Introduction

This chapter presents the experimental results of the direct matrix converter system. All the experimental data presented in this chapter is captured by the DSP-FPGA control platform. This means that the fault detection and diagnosis algorithm proposed in the previous chapter can be implemented into the DSP-FPGA control platform. This will guarantee that the fault detection and diagnosis algorithm can do real-time fault detection and diagnosis for the direct matrix converter system.

7.2 Three Phase Direct Matrix Converter System with Model Predictive Control Strategy

In the experimental implementation, the Finite Control Set Model Predictive Control (FCS-MPC) strategy is used to control the DMC. The advantage of using FCS-MPC strategy is that there is only one fixed switching state applied in each sampling period, which will simplify the switching states capturing process in the DSP-FPGA control platform. The output current sensors are located ahead of the clamp circuit to measure the DMC output

currents directly as shown in Figure 7.1. The experimental parameters are presented in Table 7.1. The direct matrix converter system is shown in Figure 7.2.

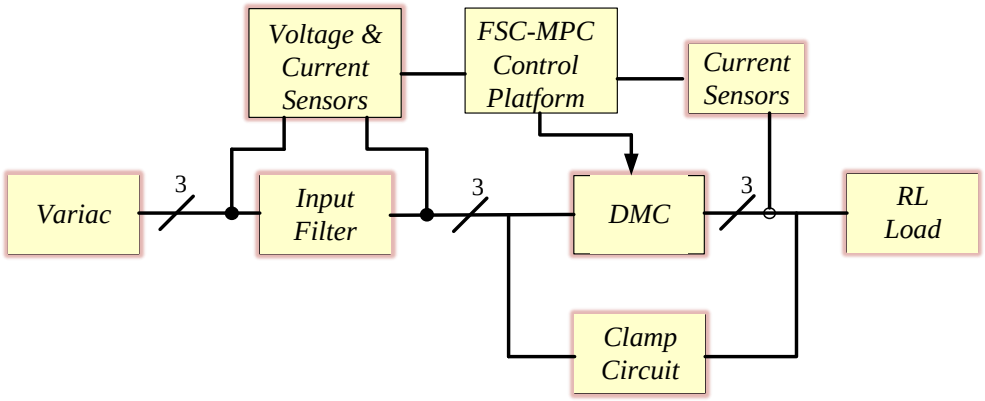


Figure 7.1: experimental rig set up diagram

Table 7.1: The experimental parameters of bench rig with FCS-MPC strategy

Variables	*Description*	*Value*
V_s	*Amplitude AC Phase Voltage*	$50[V]$
L_f	*Input Filter Inductor*	$273[\mu H]$
C_f	*Input Filter Capacitor*	$72[\mu F]$
R_f	*Input Filter Resistor*	$0.08[\Omega]$
R_{load}	*Load Resistor*	$12[\Omega]$
L_{load}	*Load Inductor*	$17[mH]$
T_{sample}	*Sampling Time*	$100[\mu s]$
I_{out}	*Output Current Amplitude*	$2.5[A]$
f_{out}	*Output Current Frequency*	$60[Hz]$

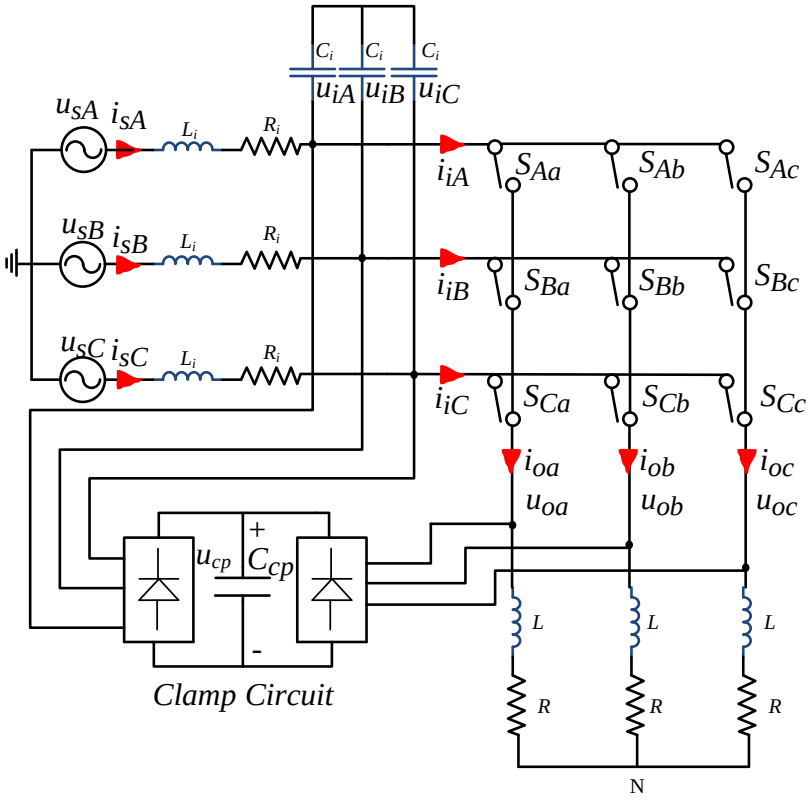


Figure 7.2: Direct matrix converter system operating under healthy operating condition

7.2.1 Healthy Operating Condition

Under healthy operating condition, the input source voltage amplitude V_s of the direct matrix converter system is $50V$. the three phase sinusoidal input source voltage u_s under normal operation is shown in Figure 7.3.

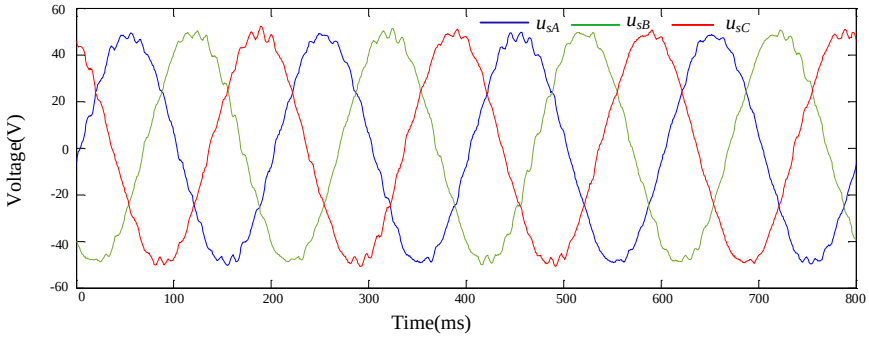


Figure 7.3: The normal operation input source voltage u_s of the direct matrix converter system with FCS-MPC strategy

Under healthy operating condition, the amplitude of the direct matrix converter input voltage u_i is $50V$. the input voltage u_i of the direct matrix converter under normal operation is shown in Figure 7.4.

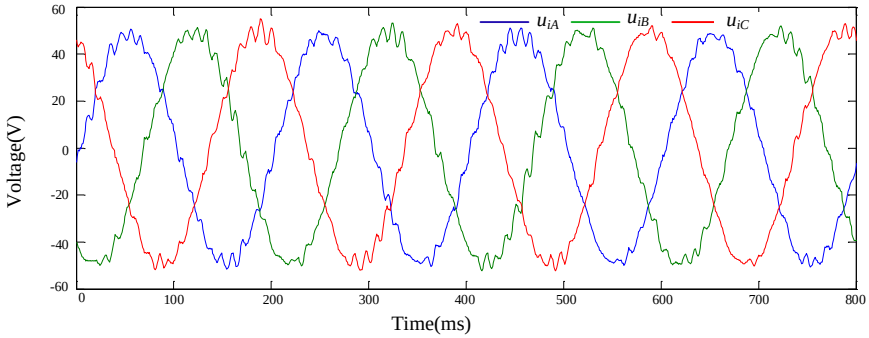


Figure 7.4: The normal operation input voltage u_i of the direct matrix converter system with FCS-MPC strategy

Under healthy operating condition, the amplitude of the direct matrix converter output current i_o is $2.5A$. the output current i_o of the direct matrix converter under normal operation is shown in Figure 7.5.

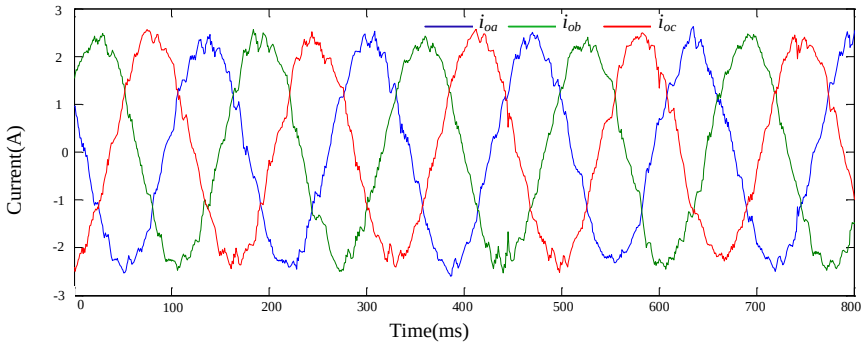


Figure 7.5: The normal operation output current i_o of the direct matrix converter system with FCS-MPC strategy

the input source current i_s of the direct matrix converter under normal operation is shown in Figure 7.6. The harmonic of the input source current is caused by the FCS-MPC control algorithm. The FCS-MPC control algorithm gives major priority to the output current rather than the input current. This is the reason why the harmonic of the input source current is high. Since the DMC system using the FCS-MPC control algorithm does not operate in ideal condition, quite amount of noise is introduced into the DMC system which can be seen from the input source current i_s waveform. One reason for this not ideal condition is that this thesis focus more on the fault diagnosis than on the control performance of the system. Another reason for this not ideal condition is that the feasibility of the proposed fault diagnosis method could be better tested under this not perfect and noisy condition, because the nature of the proposed fault diagnosis method is a threshold-value-based method, which is heavily depending on the noise level of the system. If the proposed fault diagnosis method can effectively locate the fault in this noisy condition, the performance of the proposed fault diagnosis method can be much better in a well-controlled and low-noise-level system.

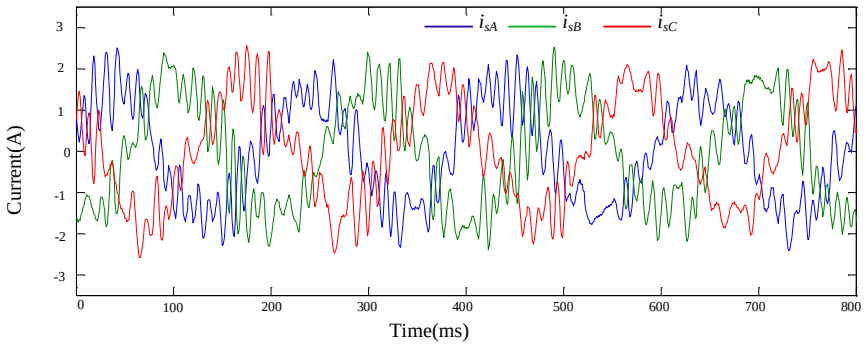


Figure 7.6: The normal operation input source current i_s of the direct matrix converter system with FCS-MPC strategy

7.2.2 Single Bidirectional Switch Open Circuit Fault Condition

In order to do fault detection and diagnosis experiment, a bidirectional switch has to be triggered to be open circuit for a certain amount of time and then set the switch back to be normal immediately after the triggering due to safety purpose. Since the direct matrix converter is a three phase balanced system, so each individual bidirectional switch is regarded as exactly the same as the others. In this section, the bidirectional switch S_{Aa} is triggered to be open circuit for $1ms$ and then set back to normal operation immediately for safety purpose. The direct matrix converter system under an open circuit fault condition is shown in Figure 7.7.

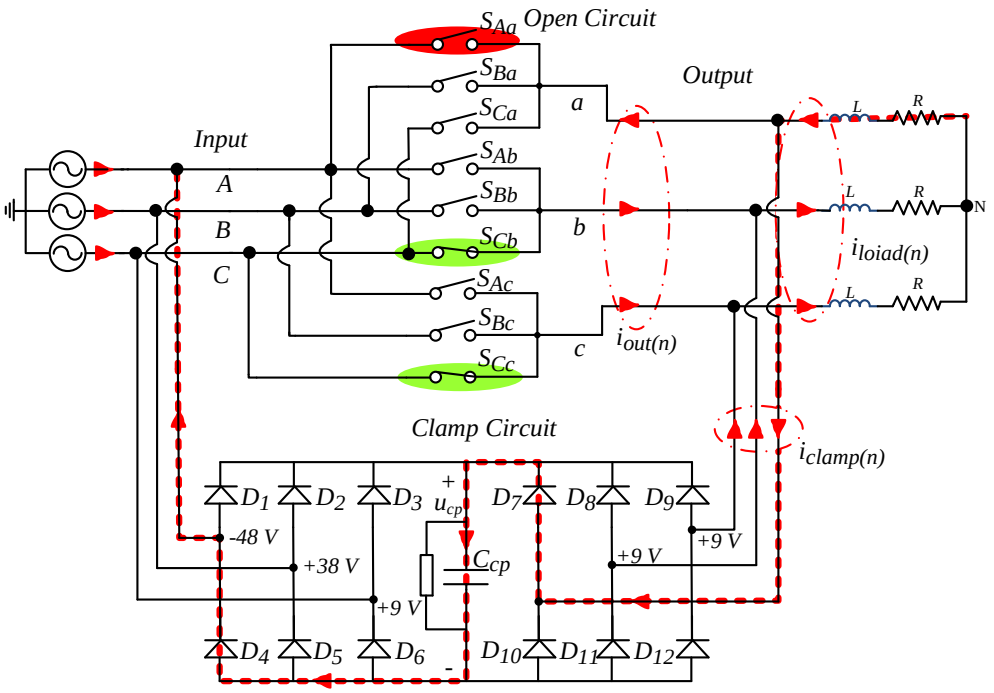


Figure 7.7: The direct matrix converter system under bidirectional switch S_{Aa} open circuit condition

Type 1 Path Results

The DMC output three phase currents i_{oa}, i_{ob}, and i_{oc} under the bidirectional switch S_{Aa} open circuit fault condition is shown in Figure 7.8. The magnified waveforms of the switching states, the DMC output currents, and the input voltages during the open circuit fault period is presented in Figure 7.9. The bidirectional switch S_{Aa} occurs an open circuit fault at $0.3ms$. The type 1 current recirculating path presented in Figure 7.10 occurs at $0.4ms$ as shown in Figure 7.9.The three phase input voltages at t_k are $u_{iA} = -48.0V$, $u_{iB} = +38.5V$ and $u_{iC} = +9.5V$, respectively. The faulty output phase current i_{oa} is flowing from the load, and the healthy output phases currents i_{ob} and i_{oc} are flowing into the load. The bidirectional switches which are conducting at t_k are S_{Aa}, S_{Cb} and S_{Cc}, respectively. From the experimental results it can be seen that there is current flowing in the DMC healthy output phases b and c.

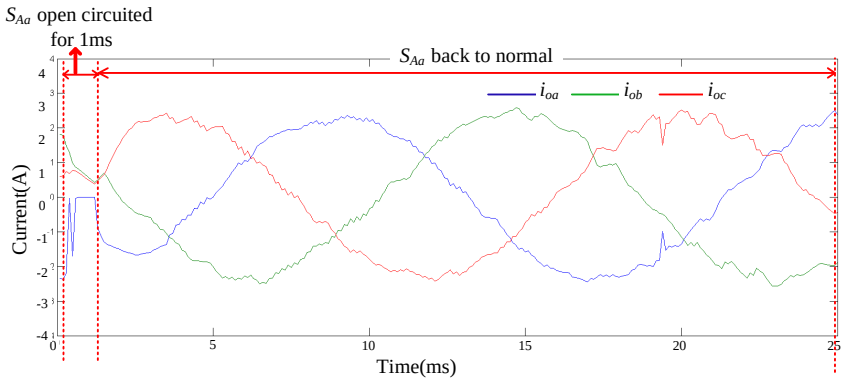


Figure 7.8: The DMC output currents under type 1 faulty phase current recirculating path occasion

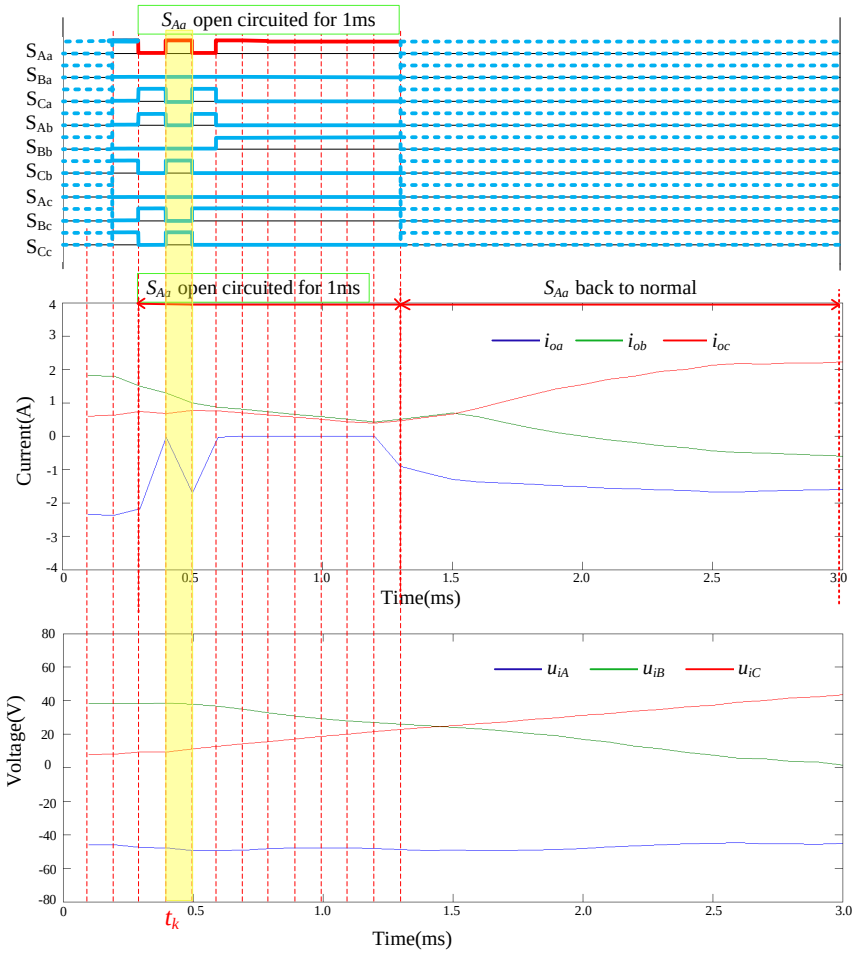


Figure 7.9: Magnified waveforms of the switching states, the output currents, and the input voltages of the DMC under type 1 faulty phase current recirculating path occasion

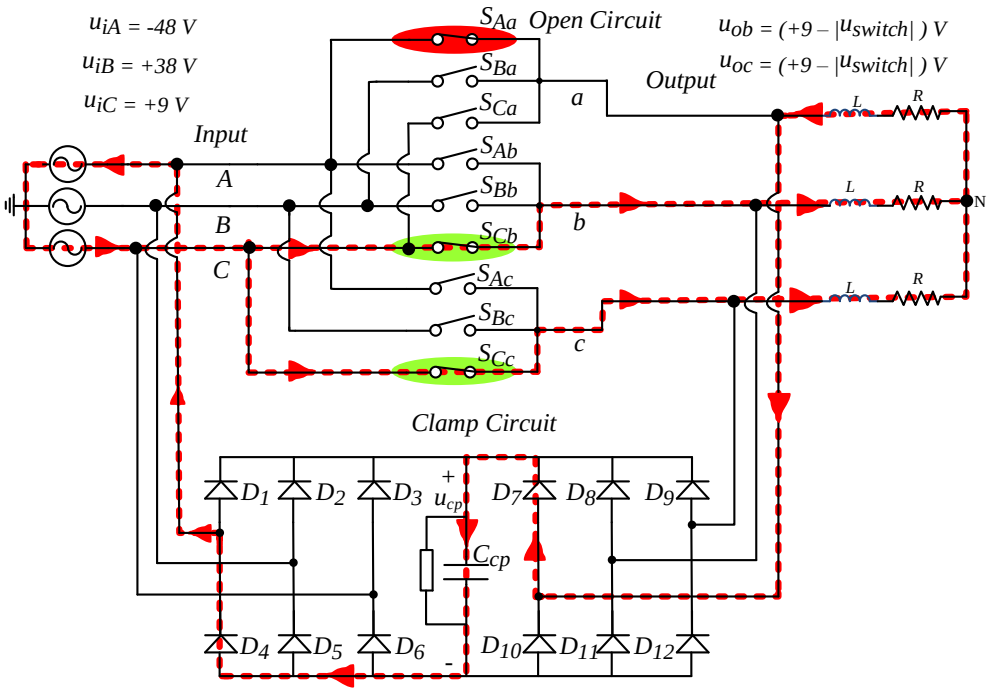


Figure 7.10: Magnified waveforms of the switching states, the output currents, and the input voltages of the DMC under type 1 faulty phase current recirculating path occasion

Type 2 Path Results

The DMC output three phase currents i_{oa}, i_{ob}, and i_{oc} under the bidirectional switch S_{Aa} open circuit fault condition is shown in Figure 7.11. The magnified waveforms of the switching states, the DMC output currents, and the input voltages during the open circuit fault period is presented in Figure 7.12. The bidirectional switch S_{Aa} occurs an open circuit fault at $0.3ms$. The type 2 current recirculating path presented in Figure 7.13 occurs at $0.4ms$ as shown in Figure 7.12. The three phase input voltages at t_l are $u_{iA} = -22.4V$, $u_{iB} = +48.4V$ and $u_{iC} = -26.0V$, respectively. The faulty output phase current i_{oa} is flowing from the load, and the healthy output phases currents i_{ob} and i_{oc} are flowing into the load. The bidirectional switches which are conducting at t_k are S_{Aa}, S_{Cb} and S_{Bc}, respectively. From the experimental

results it can be seen that there is no current flowing in the DMC healthy output phase b.

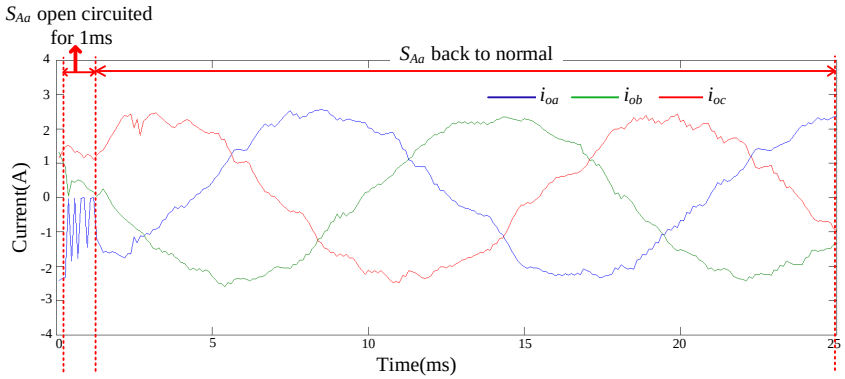


Figure 7.11: The DMC output currents under type 2 faulty phase current recirculating path occasion

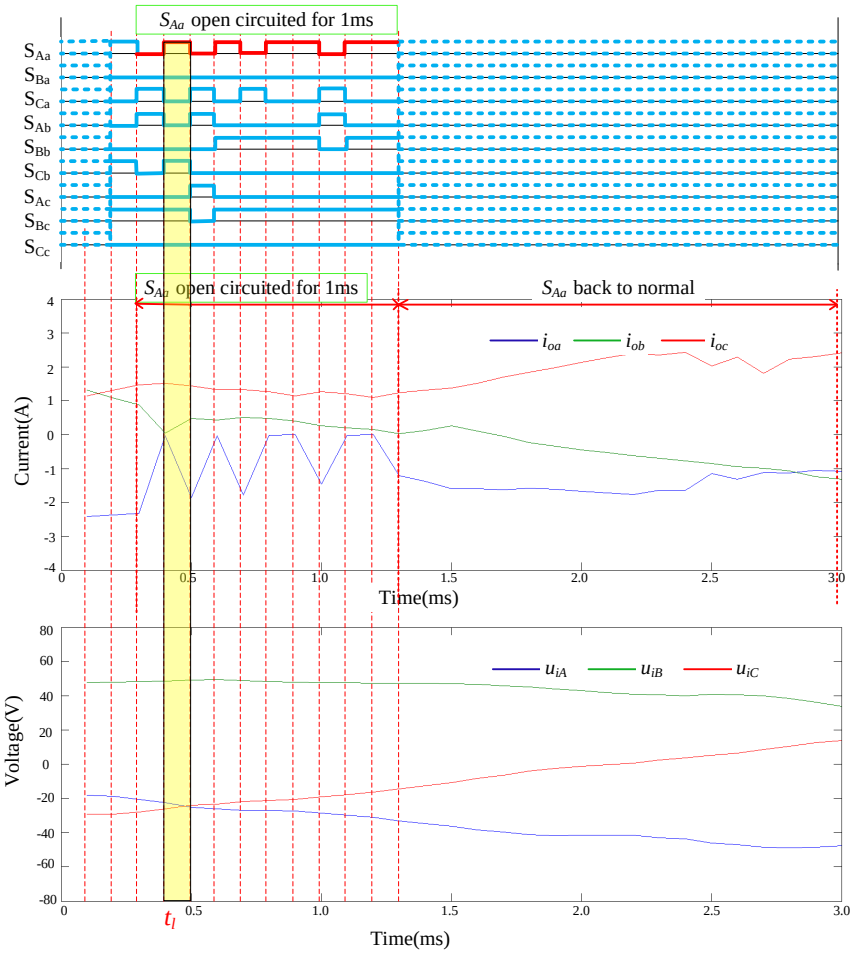


Figure 7.12: Magnified waveforms of the switching states, the output currents, and the input voltages of the DMC under type 2 faulty phase current recirculating path occasion

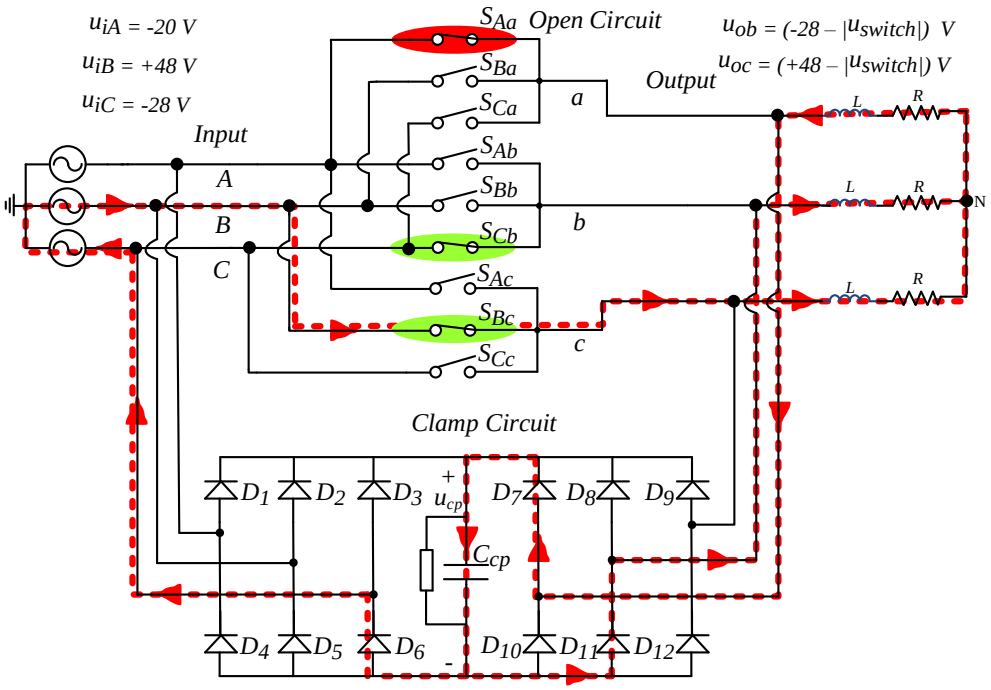


Figure 7.13: Magnified waveforms of the switching states, the output currents, and the input voltages of the DMC under type 2 faulty phase current recirculating path occasion

Fault Diagnosis Results

The results during the open-circuited period are magnified and shown in Fig. 7.14 and Fig. 7.15. It can be seen that the DMC output current i_{oa} drops to zero immediately when switch S_{Aa} is triggered to be open-circuited and keeps zero during the whole open-circuited period. So the open-circuited flag F_{Aa} is set to 1 by the proposed fault diagnosis system. If the absolute value of the open-circuited faulty output phase current is the biggest among the three output phase currents, The healthy output phases currents could be influenced by the faulty phase current to decrease to zero. This information is contributed to the proposed fault diagnosis system to avoid false-diagnosis. Since the absolute value of the current i_{oa} is the biggest among the three currents, so the current i_{ob} dropped to zero for two sampling periods. In

these two sampling periods, the open-circuited flag F_{Bc} is set to 0.5 respectively by the proposed fault diagnosis system by using the present switching state information, which are obtained directly from the FPGA card. Since this paper focuses on single-switch open-circuited fault occasion, so only the switch S_{Aa} with the highest faulty possibility is detected as open-circuited. The switch S_{Bc} is considered as healthy switch due to lower faulty possibility. Therefore, a false diagnosis can be avoided.

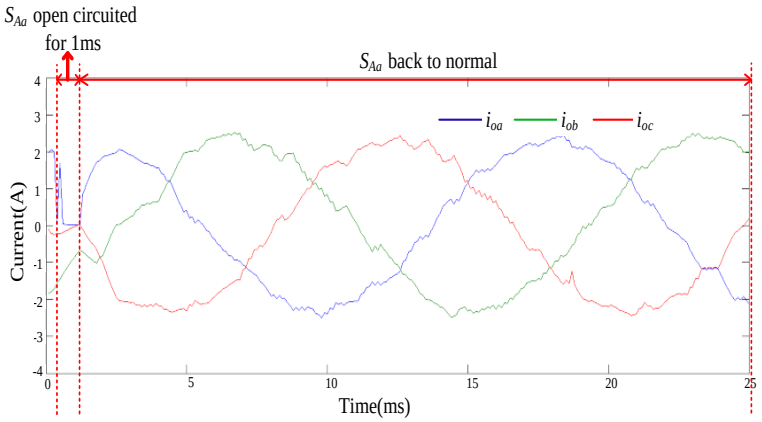


Figure 7.14: output currents under open circuit fault condition

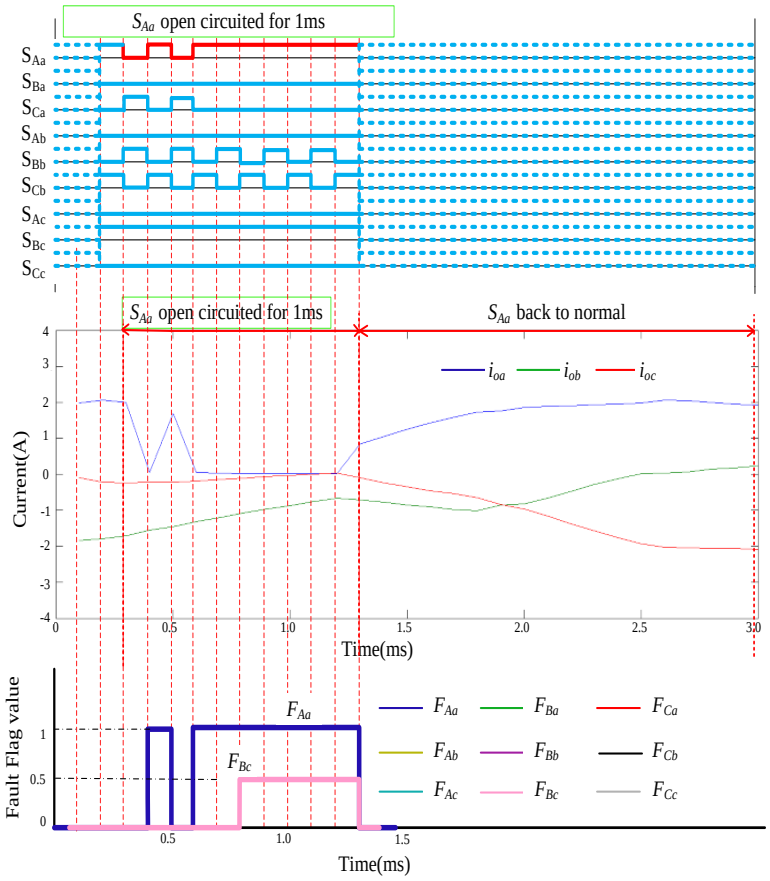


Figure 7.15: Magnified output currents under open circuit fault condition

One drawback of the proposed method is that it will diagnose an open-circuited fault during the natural zero crossing. Therefore, at least two sampling periods are needed to guarantee the currents are not experiencing natural zero crossing. The number of sampling periods needed also depends on the output frequency and amplitude. The lower the output frequency and the lower the amplitude, the more numbers of sampling periods are needed to avoid natural zero crossing.

7.2.3 Statistic Analysis of Fault Diagnosis Performance Under Random Noisy Condition

Under noisy condition, the fault diagnosis performance will be influenced because the nature of the proposed fault diagnosis method is based on threshold value selection. In reality, the output currents will almost never be exact zero because of the impact of noise. Therefore, a threshold value th and the three output phase faulty flag F_a, F_b, and F_c are defined as shown in equation 7.1.

$$\begin{aligned} &if\ i_{oa} < |th|, F_a = 0.5\ or\ 1; \\ &if\ i_{ob} < |th|, F_b = 0.5\ or\ 1; \\ &if\ i_{oc} < |th|, F_c = 0.5\ or\ 1; \end{aligned} \tag{7.1}$$

Where i_{oa}, i_{ob}, and i_{oc} are three phase DMC output currents.

In order to investigate the proposed fault diagnosis performance under random noisy condition, reasonable amount of open circuit faults are triggered randomly and the proposed fault diagnosis method is being applied on to diagnose the open circuit fault under different threshold value conditions. 11 sets of experimental results are selected to do the statistic analysis. The fault diagnosis method is being implemented by using MATLAB in order to diagnose the same open circuit fault with different threshold values including $th = 0.01$, $th = 0.02$, $th = 0.04$, and $th = 0.06$. Therefore, in total of 44 sets of fault diagnosis results are being investigated to do the statistic analysis. The 44 sets of fault diagnosis results can be found in the Appendix.

The outcome of the statistic analysis is shown in Fig 7.16. In Fig 7.16, S means the open circuit fault can be successfully detected, and F means the open circuit fault is failed to be detected. Cross symbol means the open circuit fault is successfully detected by detecting fault flag F_a being 1. Triangle symbol means the open circuit fault is successfully detected by detecting fault flag F_a being repeatable 0.5 for at least three continuous samples. Circle symbol means the open circuit fault is failed to be detected. The red line means the fault diagnosis performance when threshold value $th =$

0.01. The blue line means the fault diagnosis performance when threshold value $th = 0.02$. The green line means the fault diagnosis performance when threshold value $th = 0.04$. The yellow line means the fault diagnosis performance when threshold value $th = 0.06$.

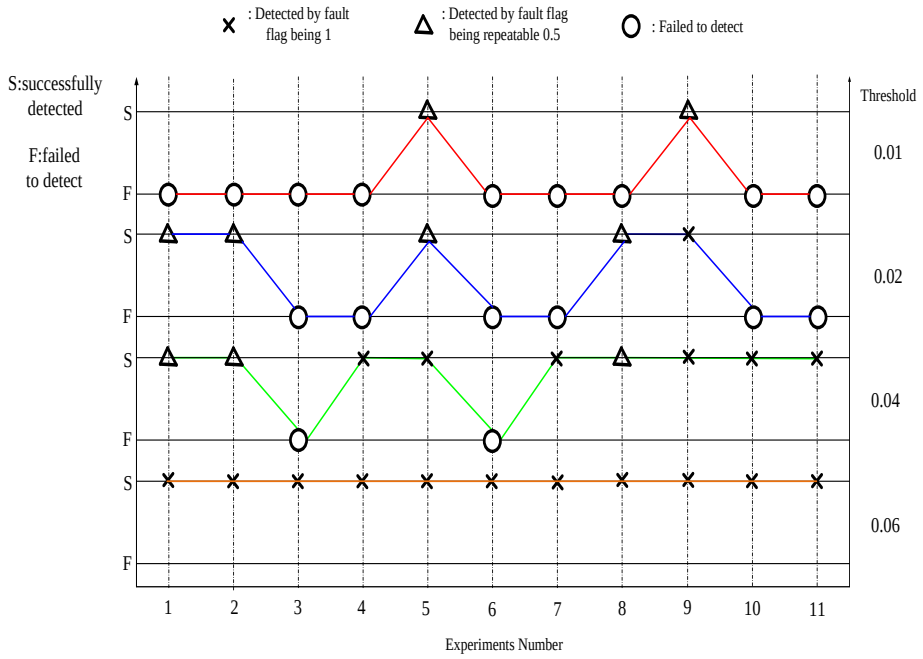


Figure 7.16: Proposed fault diagnosis method performance under different threshold value conditions

The probability of successful detection P_{sd} can be calculated under different threshold value conditions as shown in Fig 7.17. It can be seen from Fig 7.17 that when threshold value $th = 0.06$, the proposed fault diagnosis method can detect the open circuit fault 100% successfully under this specific DMC operating point. When a DMC system is operating in other operating points, the noise level would be different from the one experienced in this thesis. Therefore, the threshold value th should be adjusted accordingly depending on the DMC operating condition.

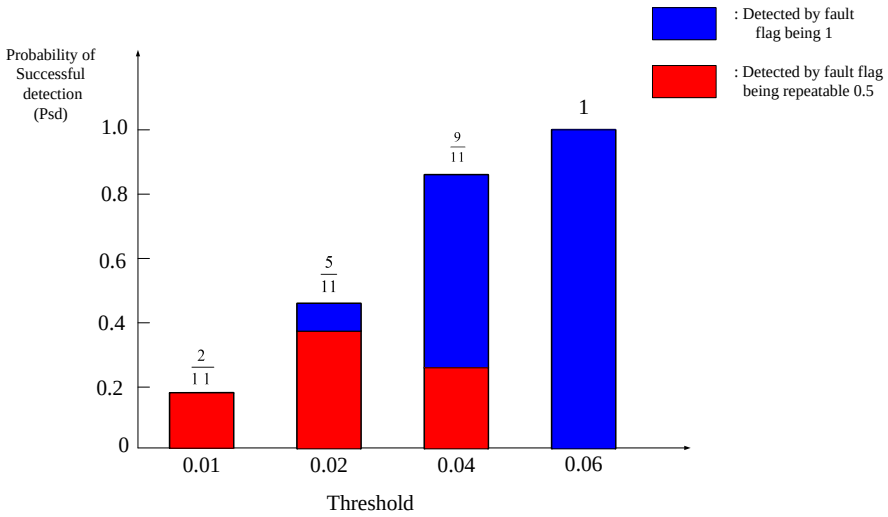


Figure 7.17: Probability of successful detection under different threshold value conditions

7.3 Three Phase Direct Matrix Converter System with Space Vector PWM Strategy

In the experimental implementation, the Space Vector Modulation (SVM) strategy is used to control the DMC. The advantage of using SVM strategy is that the SVM algorithm is simple and need less calculation than the FCS-MPC algorithm. Furthermore, the SVM strategy has a fixed switching frequency and therefore has fixed harmonic frequency. This characteristic makes it easier to design filter system for the SVM strategy. The output current sensors are located ahead of the clamp circuit to measure the DMC output currents directly as shown in Figure 7.18. The experimental parameters are presented in Table 7.2. The direct matrix converter system is shown in Figure 7.2. This section focuses on the open loop operation of the direct matrix converter system with SVM strategy.

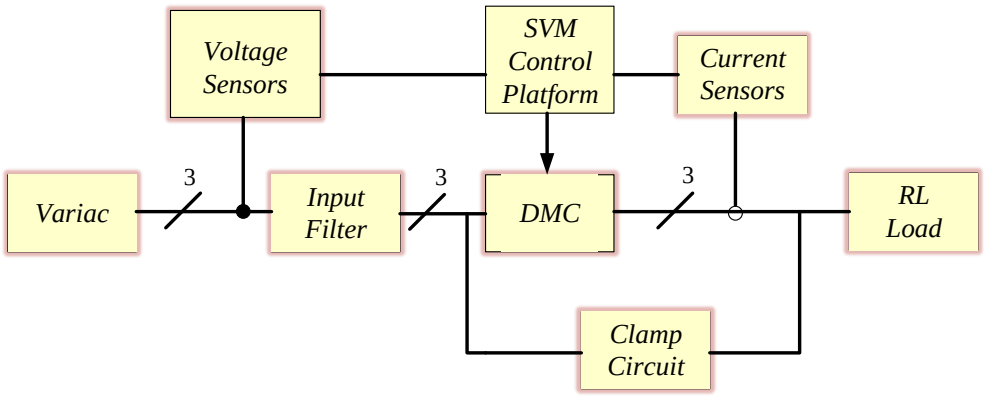


Figure 7.18: Experimental rig set up diagram with SVM strategy

Table 7.2: The experimental parameters of bench rig with SVM strategy

Variables	*Description*	*Value*
V_s	*Amplitude AC Phase Voltage*	$50[V]$
L_f	*Input Filter Inductor*	$273[\mu H]$
C_f	*Input Filter Capacitor*	$2[\mu F]$
R_f	*Input Filter Resistor*	$0.08[\Omega]$
R_{load}	*Load Resistor*	$2.8[\Omega]$
L_{load}	*Load Inductor*	$17[mH]$
f_m	*Modulation Frequency*	$12.5[kHz]$
I_{out}	*Output Current Amplitude*	$2[A]$
f_{out}	*Output Current Frequency*	$60[Hz]$

7.3.1 Healthy Operating Condition

Under healthy operating condition, the input source voltage amplitude u_s of the direct matrix converter system is $50V$. the three phase sinusoidal input source voltage u_s under normal operation is shown in Figure 7.19.

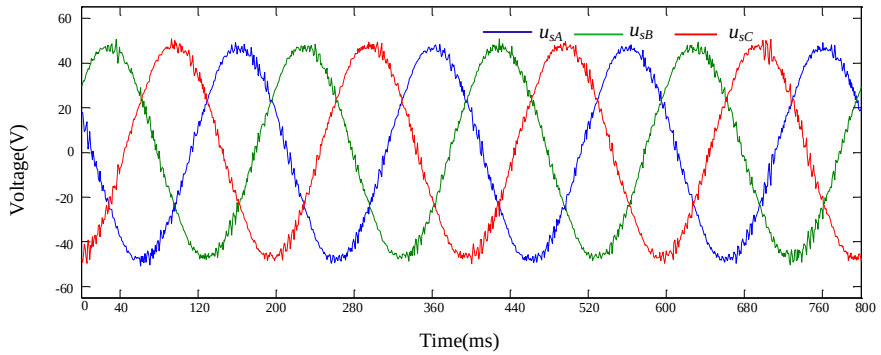


Figure 7.19: The normal operation input source voltage u_s of the direct matrix converter system with SVM strategy

Under healthy operating condition, the amplitude of the output current i_o of the direct matrix converter system is $2A$. The output current i_o of the direct matrix converter under normal operation is shown in Figure 7.20.

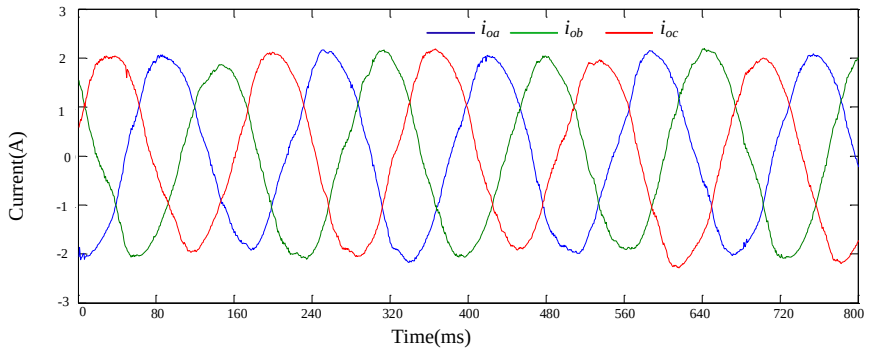


Figure 7.20: The normal operation output current i_o of the direct matrix converter system with SVM strategy

7.3.2 Single Bidirectional Switch Open Circuit Fault Condition

In this section, the bidirectional switch S_{Aa} is triggered to be open circuit for $1ms$ and then set back to normal operation immediately for safety purpose. The direct matrix converter system under an open circuit fault condition is shown in Figure 7.7. In the experiment, the 1-Zero-SVM switching sequence is applied because the 1-Zero-SVM switching sequence has less switching states than 2-Zero-SVM and 3-Zero-SVM. Reducing the switching states can reduce the complexity of the fault detection and the diagnosis algorithm. In order to capture the output current information of each switching state in one modulation period, an over-sampling technique is applied in this experiment. The output current sampling frequency is $200kHz$, which means the output current is sampled every $5us$. Since the modulation frequency is $12.5kHz$ in this experiment, so there are 16 output current samples in each modulation period as shown in Figure 7.21.

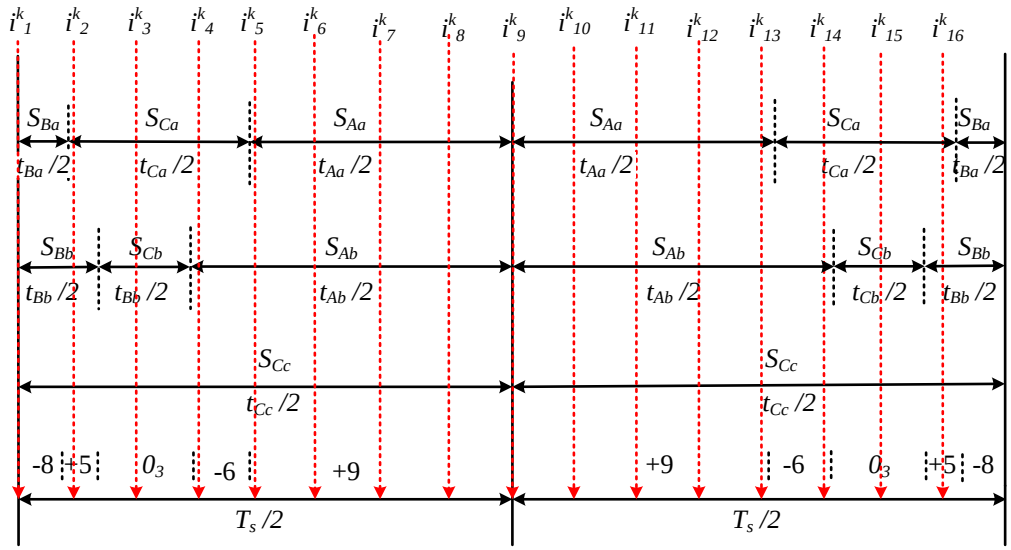


Figure 7.21: Output current over-sampling technique with $200kHz$ sampling frequency and $12.5kHz$ modulation frequency

There are 16 output current samples in each modulation period. The 16 samples of output phase a current i_{oa} of the direct matrix converter under

bidirectional switch S_{Aa} open circuit condition is shown in Figure 7.22. It can be seen from the Figure 7.22 that the over-sampling technique will capture some noise. This is because the sampling point may locate at the transient state of the switching commutation.

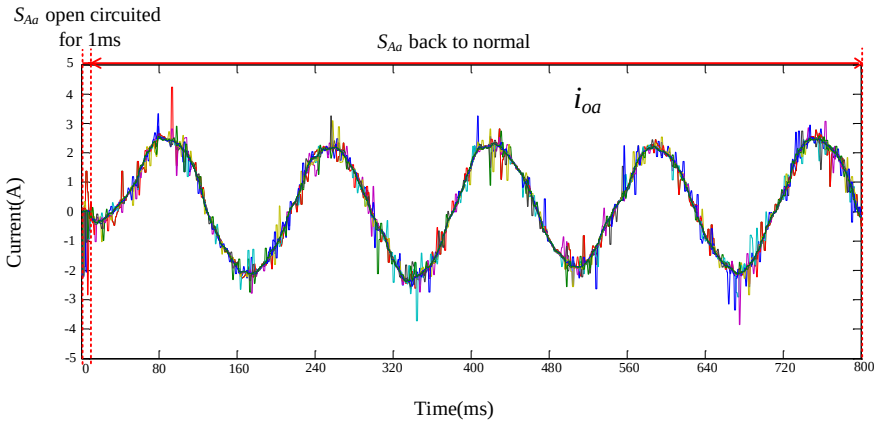


Figure 7.22: The output current i_{oa} of the direct matrix converter system with SVM strategy under bidirectional switch S_{Aa} open circuit condition

The 16 samples of output phase b current i_{ob} of the direct matrix converter under bidirectional switch S_{Aa} open circuit condition is shown in Figure 7.23. It can be seen from the Figure 7.23 that the over-sampling technique will capture some noise. This is because the sampling point may locate at the transient state of the switching commutation.

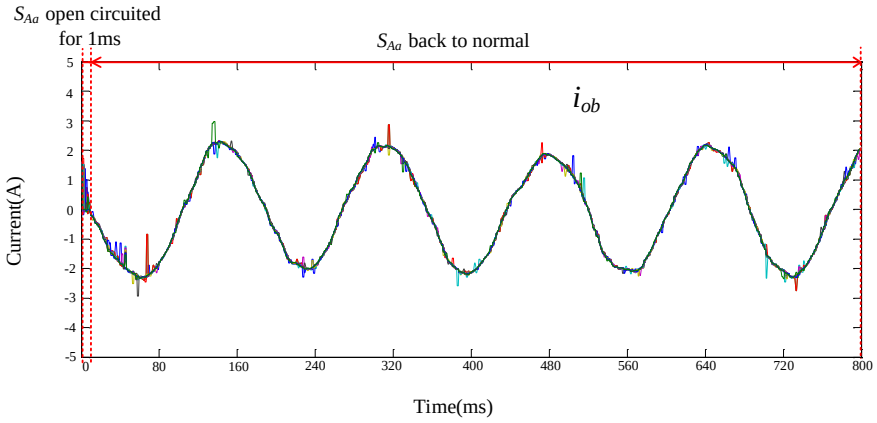


Figure 7.23: The output current i_{ob} of the direct matrix converter system with SVM strategy under bidirectional switch S_{Aa} open circuit condition

The 16 samples of output phase c current i_{oc} of the direct matrix converter under bidirectional switch S_{Aa} open circuit condition is shown in Figure 7.24. It can be seen from the Figure 7.24 that the over-sampling technique will capture some noise. This is because the sampling point may locate at the transient state of the switching commutation.

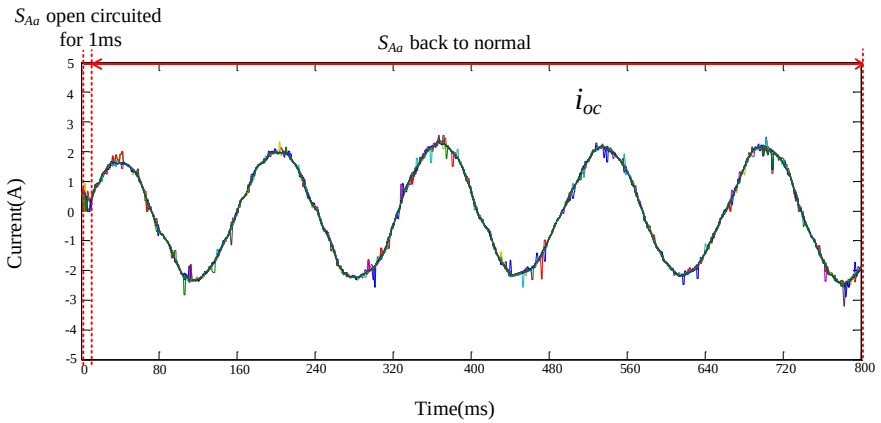


Figure 7.24: The output current i_{oc} of the direct matrix converter system with SVM strategy under bidirectional switch S_{Aa} open circuit condition

The magnified input source voltage u_s of the direct matrix converter under bidirectional switch S_{Aa} open circuit condition is shown in Figure 7.25.

Considering the input source voltage information and the switching state information together, the current recirculating path in the clamp circuit can be decided by the fault detection system to avoid false-diagnosis.

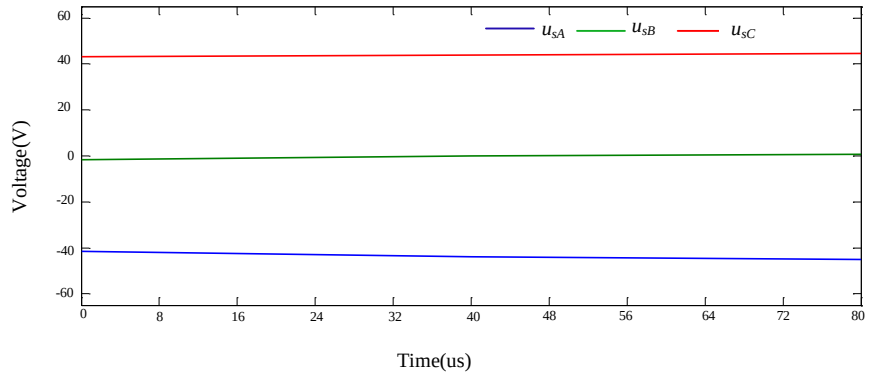


Figure 7.25: The magnified input source voltage u_s of the direct matrix converter system with SVM strategy under bidirectional switch S_{Aa} open circuit condition

The magnified sampling points of the output currents i_{oa}, i_{ob} and i_{oc} of the direct matrix converter under bidirectional switch S_{Aa} open circuit condition is shown in Figure 7.26, 7.27, and 7.28 respectively. There are 16 sampling points in one modulation period. This is the first modulation period after the switch S_{Aa} occurs open circuit fault. Considering the duty cycle of each vector, the input current sector and the output voltage sector combination information obtained from the DSP-FPGA platform, the switching sequence of this modulation period can be decided as shown in the Figure 7.26.

From Figure 7.26 it can be seen that the output phase a current i_{oa} becomes zero when the open circuit faulty switch S_{Aa} is applied in active vector $+9$. The output phase a current i_{oa} is not zero when the open circuit faulty switch S_{Aa} is not applied in vectors -8, $+5$, 0_3 and -6.

From Figure 7.27 it can be seen that output phase b current i_{ob} becomes zero when the open circuit faulty switch S_{Aa} is applied in active vector $+9$. This is because the faulty output phase current ${i_{oa}}^{k-1}$ at the previous modulation period ${T_s}^{k-1}$ is the biggest absolute value among the three output currents. So the faulty output phase current i_{oa} will recirculate through the

clamp circuit diode D_7 and D_{11} and go back to output load phase b. Therefore, the faulty output phase current i_{oa} will provide all the current required for output load phase b. This will cause the output current sensor located at the direct matrix converter output phase b detects zero current as shown in the Figure 7.27. The faulty output current i_{oa} recirculating path through the clamp circuit during vector +9 is shown in the Figure 7.29.

From Figure 7.28 it can be seen that the output phase c current i_{oc} flows as usual. This is because the switch S_{Cc} is conducting during vector +9. The bidirectional switch S_{Cc} connects the output phase c to the input source phase C. So the output phase voltage is $+42V$ regardless the switch voltage drop. The clamp circuit diode D_{12} will not conduct due to the clamp circuit characteristic. Therefore, the other part of the faulty output phase current i_{oa} will flow through clamp circuit Diode D_4 and go back to the direct matrix converter. So the output phase c current sensor will detect a non-zero current during vector +9 as shown in Figure 7.28.

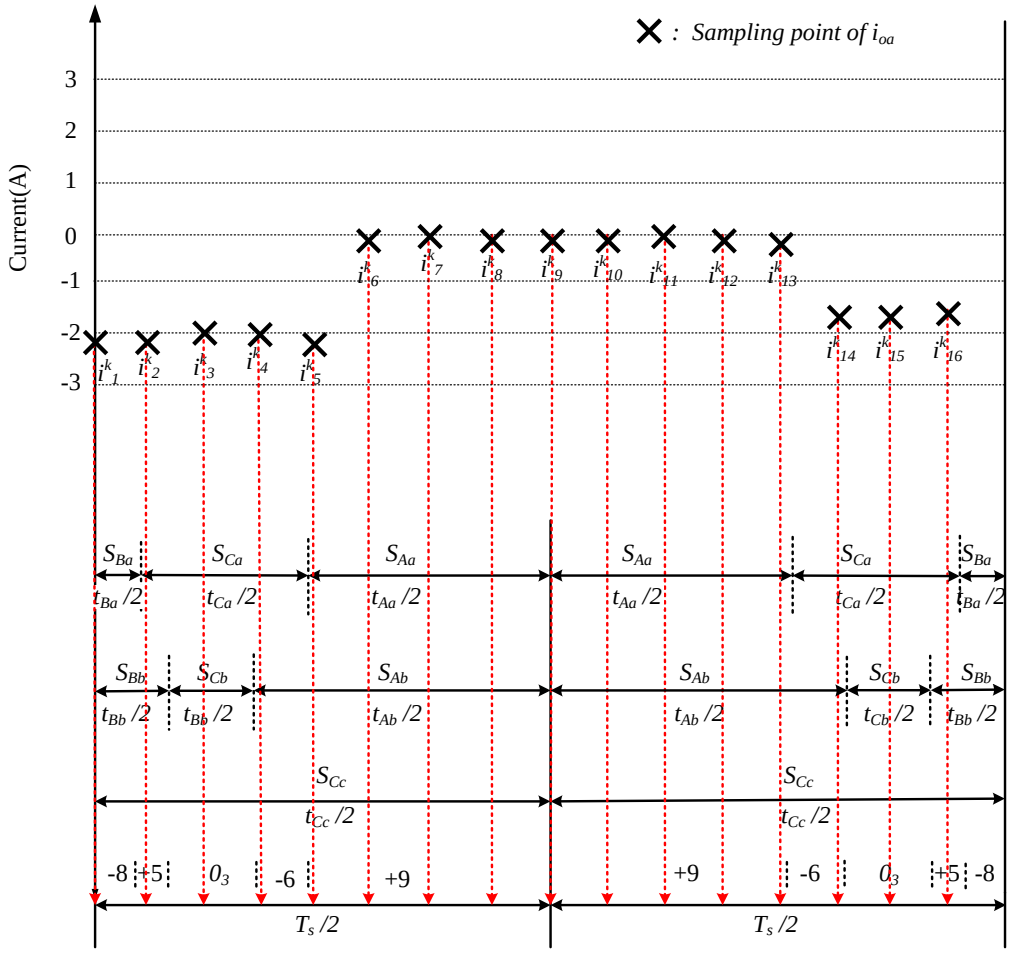


Figure 7.26: The magnified sampling points of the output current i_{oa} of the direct matrix converter system with SVM strategy under bidirectional switch S_{Aa} open circuit condition

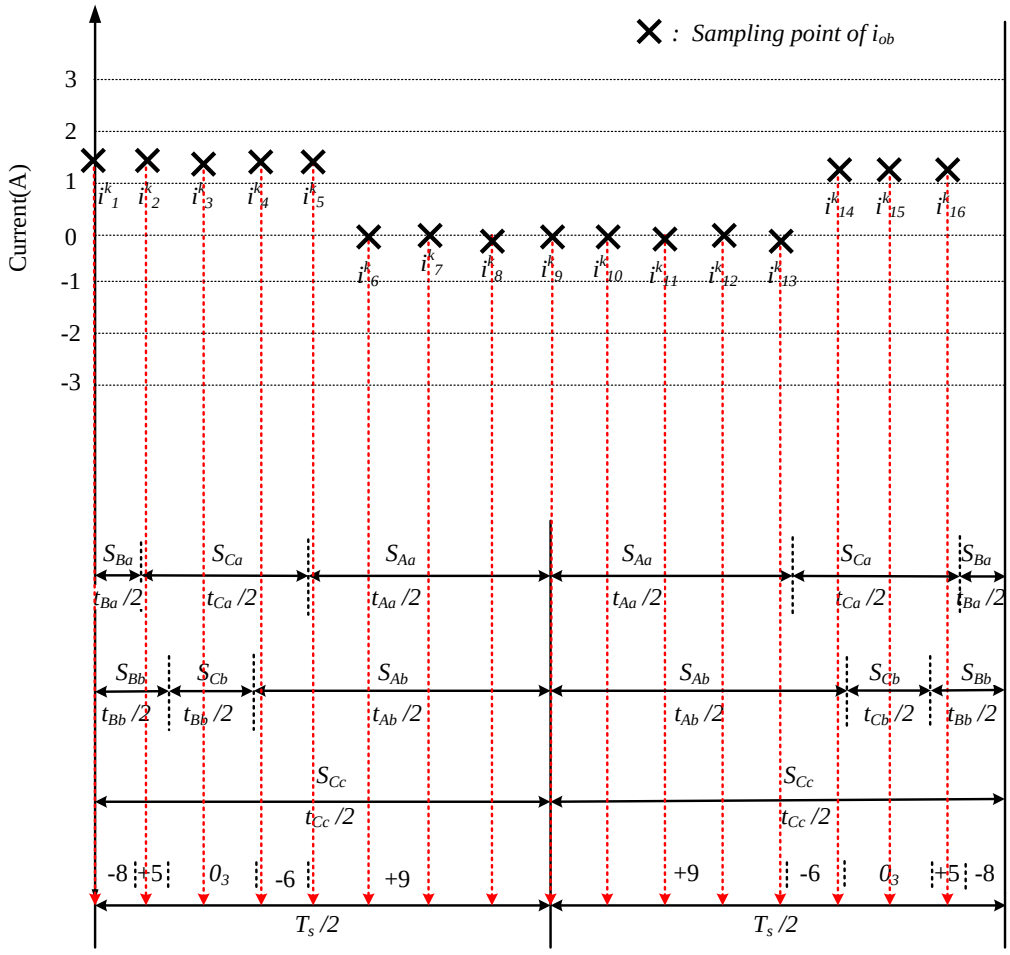


Figure 7.27: The magnified sampling points of the output current i_{ob} of the direct matrix converter system with SVM strategy under bidirectional switch S_{Aa} open circuit condition

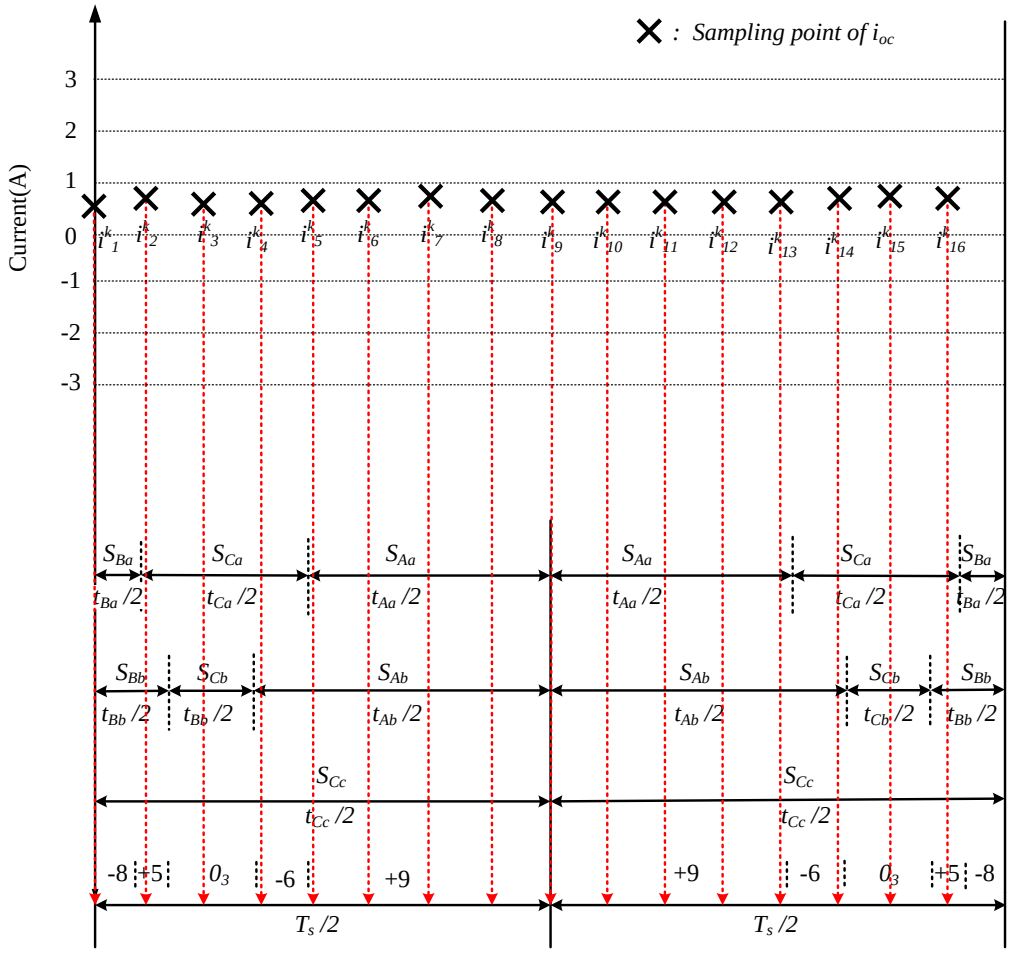


Figure 7.28: The magnified sampling points of the output current i_{oc} of the direct matrix converter system with SVM strategy under bidirectional switch S_{Aa} open circuit condition

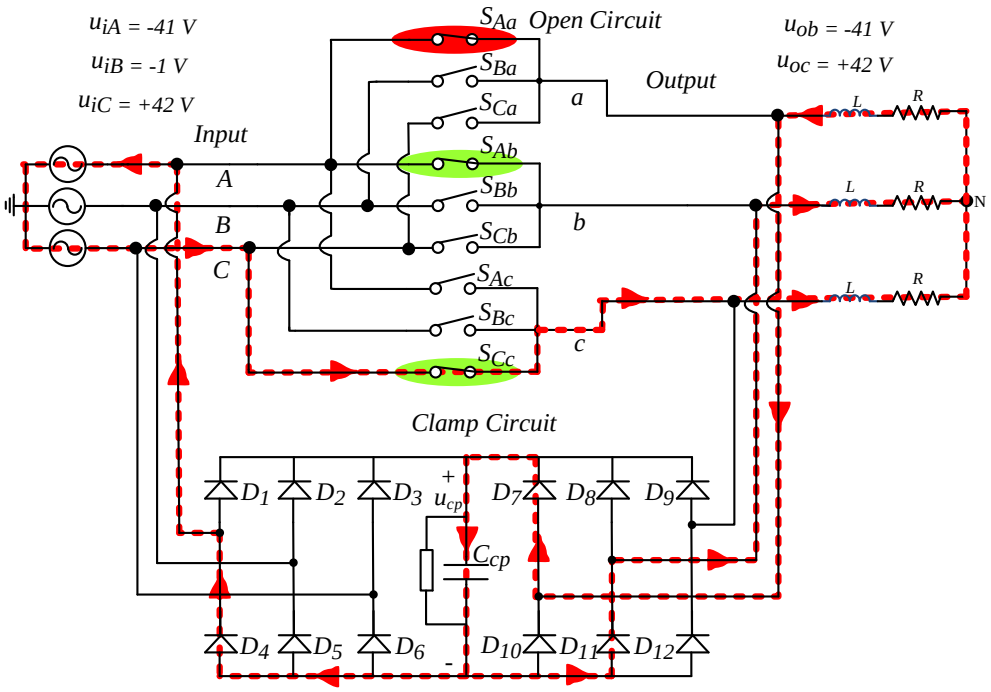


Figure 7.29: The faulty output current i_{oa} recirculating path through the clamp circuit during vector +9

7.4 Fault Detection and Diagnosis Methods Evaluation and Comparison

This section will evaluate and compare the Fault Detection and Diagnosis (FDD) methods and the control cost between the SVM strategy and the FCS-MPC strategy. The SVM strategy needs 0 input current sensor and the FCS-MPC strategy needs 2 input current sensors. The SVM strategy needs 3 output current sensors and the FCS-MPC strategy needs 3 output current sensors as well. The SVM strategy needs 2 input voltage sensors and the FCS-MPC strategy needs 4 input voltage sensors. Neither SVM strategy nor FCS-MPC strategy need any output voltage sensor. As for the FDD methods, the SVM strategy needs high bandwidth output current sensors such as $2MHz$ bandwidth because the over-sampling technique is applied.

Table 7.3: FDD Methods and Control Cost Evaluation and Comparison

	SVM	$FCS-MPC$
Input Current Sensor Number	0	2
Output Current Sensor Number	3	3
Input Voltage Sensor Number	2	4
Output Voltage Sensor Number	0	0
Output Current Sensor Bandwidth	*High*	*Low*
Control Algorithm Computation Amount	*Low*	*High*
FDD Algorithm Computation Amount	*High*	*Low*

The FCS-MPC strategy needs low bandwidth output current sensors such as $200kHz$ bandwidth because only one current sample is required within each sampling period. The SVM control algorithm computation amount is lower than the FCS-MPC algorithm. However, the SVM FDD algorithm computation amount is higher than the FCS-MPC algorithm. This is because there are at least 9 switching states within one SVM modulation period. In addition, there are much more output current samples within one SVM modulation period than the current sample within one FCS-MPC sampling period. The FDD algorithm need more computation to analyze the data obtained from the SVM system than from the FCS-MPC system.

7.5 Summary

This chapter presents the experimental results of the direct matrix converter system. All the experimental data presented in this chapter is captured by the DSP-FPGA control platform. This means that the fault detection and diagnosis algorithm proposed in the previous chapter can be implemented into the DSP-FPGA control platform. This will guarantee that the fault de-

tection and diagnosis algorithm can do real-time fault detection and diagnosis for the direct matrix converter system.

The proposed fault detection and diagnosis algorithm is experimentally implemented into the direct matrix converter system with FCS-MPC strategy. The advantage for doing fault detection and diagnosis with FCS-MPC strategy is that there is only one fixed switching state within one sampling period. So only one current sample is required within one sampling period. This current sensing requirement will allow relatively low bandwidth of the output current sensor. The low bandwidth of the output current sensor could potentially reduce the hardware cost.

The proposed fault detection and diagnosis algorithm is also experimentally implemented into the direct matrix converter system with SVM strategy. The advantage for doing fault detection and diagnosis with SVM strategy is that the switching frequency is fixed. The fixed switching frequency will make it easier to design the filter for the direct matrix converter system with SVM strategy than with FCS-MPC strategy. Because the switching frequency is uncertain in FCS-MPC strategy. Another advantage for doing fault detection and diagnosis with SVM strategy is that the SVM algorithm computation amount is lower than the FCS-MPC algorithm. This advantage will reduce the control cost for SVM strategy comparing with FCS-MPC strategy.

The speed and precision of the proposed fault diagnosis method require adjustment depending on the application condition. Ideally, if the output current frequency and amplitude are high, and the current sensors are well resisted to noise, and the derivative of the faulty output current exceeds the empirical threshold value, the open-circuited switch fault can be diagnosed within one sampling period. However, if the output current frequency or amplitude is low, the proposed method will diagnose an open-circuited fault during the natural zero crossing. Therefore, at least two sampling periods are required to guarantee the currents are not experiencing natural zero crossing. The lower the output frequency and amplitude, the more numbers of the sampling periods are required to avoid natural zero crossing. In addition, if the current sensors are not resistant to noise, more sampling periods are also required to inhibit the disturbance.

Chapter 8

Conclusion and Future Work

8.1 Conclusion

The matrix converter (MC) topology consists of a bidirectional switch matrix which connects the output direct to the input. The main advantage of the MC topology is the removal of DC-Link component, which makes the MC topology suitable for weight and volume critical conditions such as aerospace application. However, since the MC topology has more semiconductor switches than the traditional back-to-back PWM converter topology, the reliability of the semiconductors is always a big concern in the MC applications. It is inevitable that an open circuit switch fault will occur during the MC system lifetime. Therefore, it is of vital importance to diagnose the switch fault precisely and fast in order to prevent follow-on damage from the fault.

An effective open circuit fault diagnosis method requires the expert knowledge of the MC system behaviour under an open circuit switch fault. Therefore, this thesis has investigated both the open circuit fault MC system behaviour and the fault diagnosis methods for the MC system. Chapter 4 investigated the direct matrix converter (DMC) system behaviour under an open circuit fault condition with both the finite-control-set model-predictive-control (FCS-MPC) strategy and the space vector modulation (SVM) strat-

egy. In addition, the indirect matrix converter (IMC) system behaviour under the FCS-MPC strategy is also investigated in section 4.6. The expert knowledge of the open circuit fault system behaviour is then contributed to development of the fault diagnosis methods described in chapter 5. The MC system models are built and tested in simulation softwares such as SYNOPSYS SABER and MATLAB/SIMULINK. The simulation results are shown in chapter 6. The laboratory prototype of the DMC system for experimental test is described in chapter 7. The corresponding experimental waveform is presented in chapter 8 to prove the feasibility of the proposed fault diagnosis methods.

The three proposed open circuit fault diagnosis methods for the MC systems in chapter 5 are summarized as follows.

The first proposed fault diagnosis method is for direct matrix converter (DMC) with finite control set model predictive control (FCS-MPC) strategy. The three output current sensors are located ahead of the clamp circuit to measure the matrix converter output current directly. In addition, expert knowledge is contributed to the fault detection system to avoid false-diagnosis. Ideally the proposed method can locate an open-circuited switch fault in one sampling period. Moreover, the proposed fault diagnosis method is applicable within the whole range of modulation index from 0 to 0.866. The fault diagnosis algorithm is implemented into the DSP-FPGA control platform and can achieve real-time fault diagnosis. In this method, no additional sensing unit is implemented. All the signals required for the fault diagnosis system are also required for the normal operation of the DMC system. Moreover, no additional hardware complexity is implemented in this method. The bandwidth of the output current sensor is $200kHz$, a common LA55-P current transducer manufactured by LEM is enough for this application.

The second proposed fault diagnosis method is for DMC with space vector modulation (SVM) strategy. In this method, the over-sampling technique is

applied to sample the DMC output current. Three high bandwidth current sensors are required for this application. The high bandwidth current sensor comprises of a shunt resistor, an amplifier, an analog-to-digital converter (ADC), an isolator and differential transceivers. The current sampling frequency is 16 times higher than the SVM modulation frequency in this thesis. The reason to use over-sampling technique is because there are more than one switching state in each modulation period. The advantage for doing fault detection and diagnosis with SVM strategy is that the switching frequency is fixed. The fixed switching frequency will make it easier to design the filter for the direct matrix converter system with SVM strategy than with FCS-MPC strategy. Because the switching frequency is uncertain in FCS-MPC strategy. Another advantage for doing fault detection and diagnosis with SVM strategy is that the SVM algorithm computation amount is lower than the FCS-MPC algorithm.

The third proposed fault diagnosis method is for indirect matrix converter (IMC) with FCS-MPC strategy based on error voltage. If the inverter stage of the IMC occurs an open-circuit fault, the faulty switch can be located within one sampling period by using the output error voltages and the switching state information. The error voltage is acquired by comparing the reference output voltages and the estimated output voltages. When the rectifier stage of the IMC occurs an open-circuit fault, two additional voltages sensors will be used to measure the fictitious DC-Link voltages of the IMC. Combining the information of rectifier stage switching states and the DC-Link voltages, The faulty switch can be identified within one sampling period.

8.2 Future Work

There are a few points which can be investigated further in order to enhance the fault diagnosis performance of the MC systems.

1) The performance of the over-sampling current sensing system can be

improved by improving the immunity to noise.

2) A more advanced current sensing system can be developed by using scheduled-time sensing technique. The scheduled-time sensing technique can guarantee that the sampling point is located at the middle point of each switching state, which can effectively improve the immunity to noise.

3) A real time open circuit fault diagnosis implementation for the MC system with the SVM strategy can be developed in the future. Since the SVM strategy has 10 to 14 switching states in each modulation period, it is more difficult to capture the switching state information in real time in SVM strategy than in FCS-MPC strategy due to the limitation of the digital signal processor (DSP) technology.

4) In this thesis, only the direct matrix converter topology is experimentally implemented to test the feasibility of the proposed DMC fault diagnosis methods. The indirect matrix converter topology could also be experimentally constructed to test the validity of the proposed IMC fault diagnosis method.

5) In this thesis, only the resistance-inductance load is used to test the fault diagnosis methods for the MC systems. Future research could focus on the fault diagnosis in the MC inductive machine drive system and the MC permanent magnet synchronous machine (PMSM) drive system.

8.3 List of Publication

The work presented in this thesis has been published in the following journal and conference papers:

8.3.1 Journal Paper

1. J. Zhang, H. Dan, L. Empringham, L. de Lillo, and P. Wheeler,"Matrix Converter Open Circuit Fault behaviour Analysis and Diagnosis with a Model Predictive Control Strategy," IEEE Journal on Emerging and Selected Topics in Power Electronics.

8.3.2 Conference Papers

1. J. Zhang, L. Empringham, L. de Lillo, and P. Wheeler, "A Design Guide of Direct Matrix Converter Open Circuit Online Fault Diagnosis in Industrial Applications," Annual Conference of the IEEE Industrial Electronics Society (IECON) 2018, Accepted.

2. J. Zhang, H. Dan, L. Empringham, L. de Lillo, P. Wheeler, and M. Rivera, "Indirect Matrix Converter Open Circuit Fault Detection and Diagnosis with Model Predictive Control Strategy," Annual Southern Hemisphere Power Electronics Conference (SPEC) 2017.

3. J. Zhang, L. Empringham, L. de Lillo, P. Wheeler, and H. Dan, "Matrix Converter Open Circuit Fault Diagnosis with Asymmetric One Zero SVM," IEEE Energy Conversion Congress and Exposition (ECCE) 2017.

4. J. Zhang, C. Brunson, J. Bowden, L. de Lillo, and P. Wheeler, "Matrix Converter Open Circuit behaviour Analysis," Annual Conference of the IEEE Industrial Electronics Society (IECON) 2016.

5. M. Rivera, Z. Di, J. Zhang and P. Wheeler, "Indirect Predictive Control Strategy with Mitigation of Input Filter Resonances for a Direct Matrix Converter," The International Congress of Electric Engineering, Electronics and ICT (IEEE CHILECON) 2017.

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Chapter 9

Appendix

9.1 Simulation Schematics

Simulation works are done by MATLAB. Figure 9.1 shows the direct matrix converter system simulation schematic. Figure 9.2 shows the indirect matrix converter system simulation schematic.

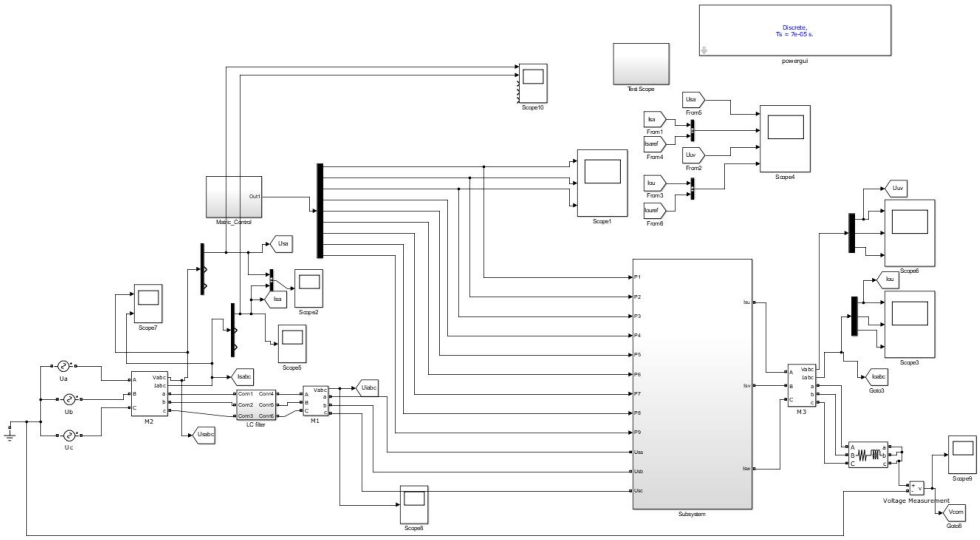


Figure 9.1: Direct matrix converter system MATLAB simulation schematic

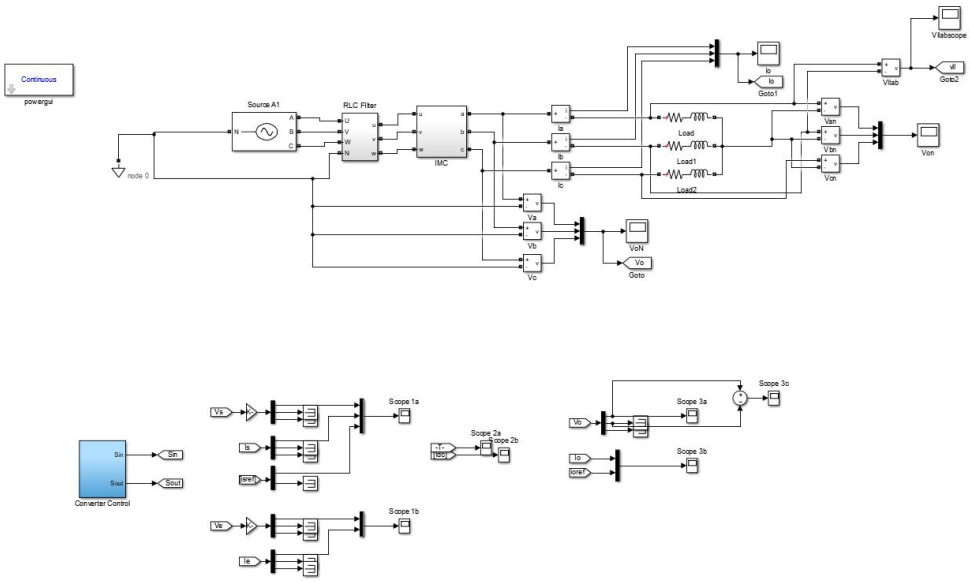


Figure 9.2: Indirect matrix converter system MATLAB simulation schematic

9.2 Direct Matrix Converter System Experimental Rig Set Up

In order to experimentally validate the effectiveness of the proposed fault detection and diagnosis methods in Chapter 5 for the direct matrix converter system, an experimental rig is set up for implementation. Figure 9.3 presents a functional block diagram of the direct matrix converter system structure when the FCS-MPC strategy is implemented. It can be seen from Figure 9.3 that the old current sensor is located behind the clamp circuit while the new current sensor is located ahead of the clamp circuit. The FCS-MPC DSP/FPGA control platform requires the input voltages, input currents as well as the matrix converter output currents to generate the gate drive signals. The gate drive circuits provide the isolation between the DSP/FPGA control platform and the matrix converter power module and drive the IGBTs on the matrix converter. Figure 9.4 presents a functional diagram of the direct matrix converter system structure when the SVM control strategy is implemented. The output current sensor is also located ahead of the clamp circuit. The SVM DSP/FPGA control platform requires the input voltages and the output currents to generate the gate drive signals.

There are two hardware implementation differences between the FCS-MPC strategy and the SVM strategy. The first difference is that the FCS-MPC strategy requires input current information but the SVM strategy does not. The second difference is that the FCS-MPC strategy requires low bandwidth current sensors but the SVM strategy requires high bandwidth current sensors for fault diagnosis algorithm.

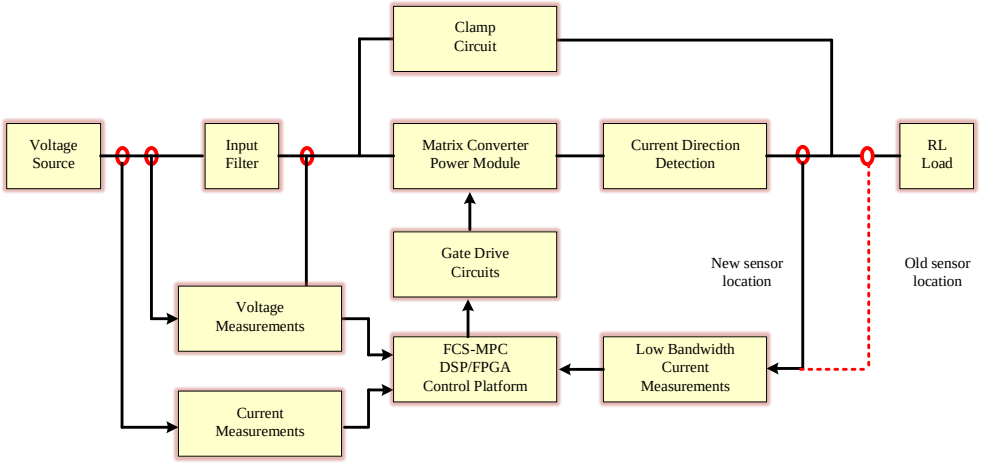


Figure 9.3: A functional block diagram of the direct matrix converter system structure with the FCS-MPC strategy

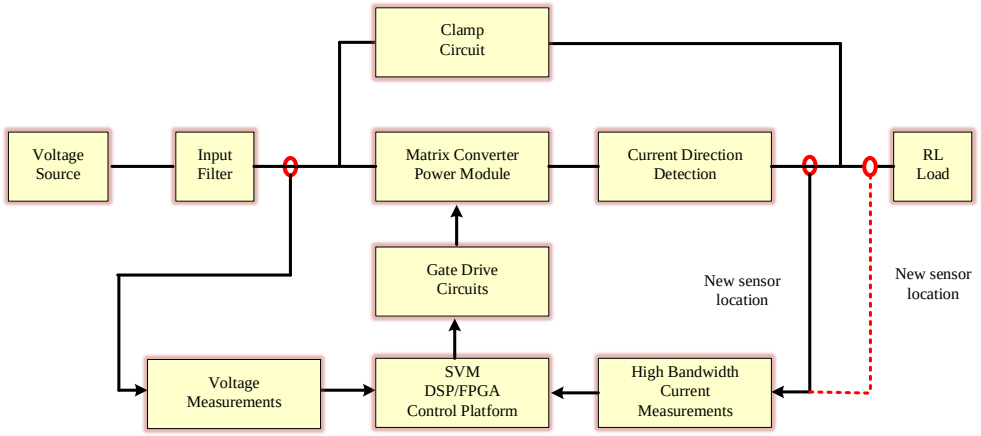


Figure 9.4: A functional diagram of the direct matrix converter system structure with the SVM strategy

In this chapter, the experimental prototype which is used to implement the direct matrix converter system is presented. The direct matrix converter experimental prototype consists of the power circuit with the gate drive circuit, the input filter and the current direction detection circuit. The design of this prototype has been developed by previous research work originated in the PEMC group. An independent clamp circuit is implemented in parallel with the direct matrix converter to protect the bidirectional switches from over-voltage damage. For the FCS-MPC direct matrix converter system, three low bandwidth output current sensors are implemented for fault detection and diagnosis purpose. For the SVM direct matrix converter system, three high bandwidth output current sensors are implemented for fault detection and diagnosis purpose. Finally, the direct matrix converter control platform for real time fault detection and diagnosis analysis is also described in this chapter. This control platform consists of a digital signal processor (DSP) and a field programmable gate array (FPGA) and more details will be given in section 7.2.5.

9.2.1 The Three Phase Direct Matrix Converter System Prototype

The three phase direct matrix converter system laboratory prototype is shown in Figure 9.5. This laboratory prototype comprises of the direct matrix converter power circuit, the control platform, the voltage and current measurement circuits, and the clamp circuit. It can be seen from Figure 9.5 that there are four output phases on the matrix converter power circuit. The fourth output phase is designed as a redundant phase for fault tolerant operation as seen in [81]. The experimental tests that have been done for this work use three output phases on the direct matrix converter for fault detection and diagnosis purpose. There are nine bidirectional switches on the power circuit. Each bidirectional switch consists of two IGBTs placed in a common emitter configuration. Each IGBT has an independent gate drive circuit. The current direction detection circuits are located at each output phase to provide the current direction sensing for the four step current com-

mutation of the bidirectional switches. Three $2uF$ input filter capacitors are implemented to attenuate the switching harmonics in the input currents. Each capacitor is connected between the two input phases.

The clamp circuit comprises of 12 ultra fast recovery diodes, two electrolytic capacitors and two bleed resistors. The clamp circuit is relocated in order to place the output current sensors ahead of the clamp circuit as shown in Figure 9.3 and 9.4. With this output current sensor location, the direct matrix converter output phase current will be measured instead of the output load current.

The measurement circuits include the input voltage and current measurement circuit, the low bandwidth output current measurement circuit, and the high bandwidth output current measurement circuit. When the direct matrix converter system is operating with the FCS-MPC control strategy, the low bandwidth output current measurement circuit will be used. When the direct matrix converter system is operating with the SVM control strategy, the high bandwidth output current measurement circuit will be used.

The control platform consists of a digital signal processor DSP card and a field programmable gate array (FPGA) card. The DSP/FPGA based control platform has been developed by the Power Electronic Machine and Control (PEMC) group at the University of Nottingham as a general purpose control platform. The control strategies are implemented on the DSP card and the FPGA generates the PWM signal. A host port interface (HPI) card is connected to the DSP card in order to read the real-time data from the DSP using MATLAB. A high bandwidth current sensor interface card is mounted on the FPGA card in order to obtain the output current data captured by the high bandwidth current sensor.

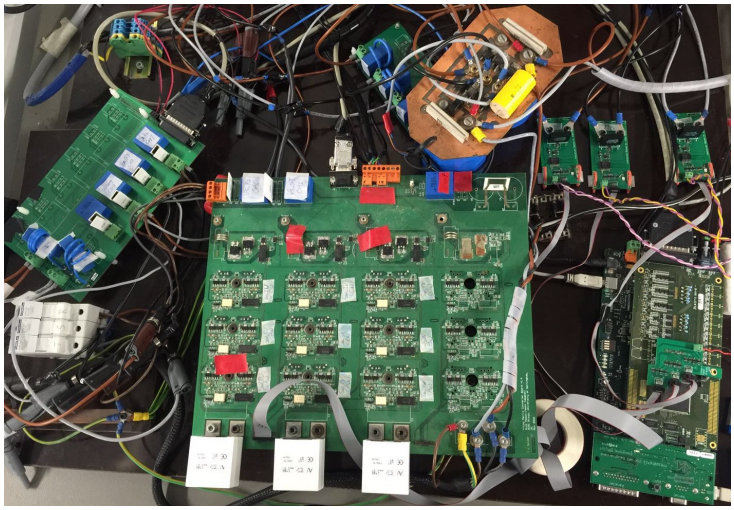


Figure 9.5: Direct matrix converter prototype

9.2.2 Power Circuit

A three phase direct matrix converter power circuit is required for the experimental validation of the proposed fault detection and diagnosis methods. The power circuit PCB of the direct matrix converter is shown in Figure 9.6. The simplified schematic diagram of the direct matrix converter power circuit is shown in Figure 9.7. There are nine SK60GM123 bidirectional switch modules in the laboratory prototype. The gate drive circuit are located at the top of the power circuit in order to minimize the distance between the gate drive circuit and the power switch. Therefore, the stray inductance can be effectively reduced by minimizing the distance between the gate drive circuit and the power switch. There are three $2\mu F$ polypropylene film capacitors MKPC4BS rated at $850V$ with 5% tolerance mounted on the power circuit. The input filter cut off frequency is designed to be lower than the switching frequency. In this experiment, the cut off frequency is designed to be around $3kHz$. The current direction detection circuit is located at each output phase of the direct matrix converter. There are two anti-paralleled Schottky diodes connected in series with each output phase. The anti-paralleled Schottky diodes are very effective when the output current is near the natural zero crossing point. This is because the Schottky diode voltage drop is bigger

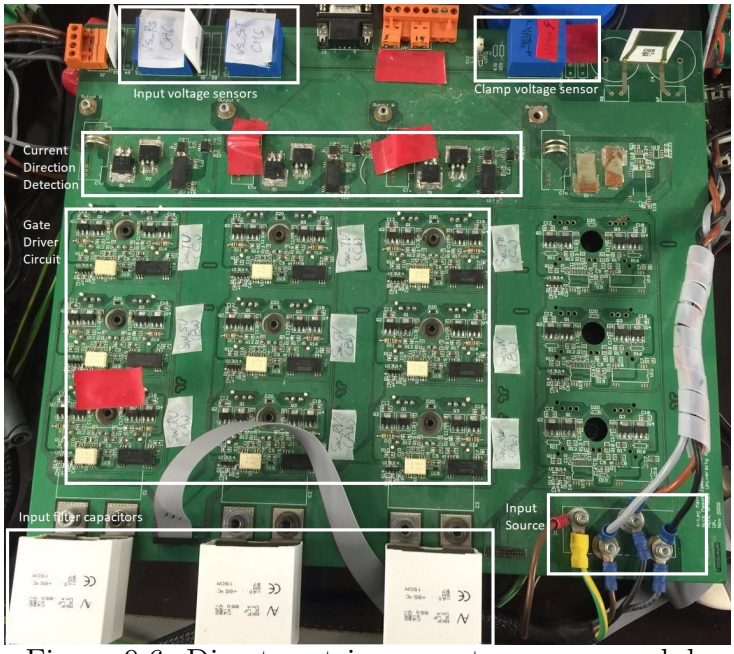


Figure 9.6: Direct matrix converter power module

comparing to a resistance shunt when the output current is near the natural zero crossing point. The input voltage measurement circuit is also mounted on the top left of the power circuit in order to measure the line-to-line input voltage.

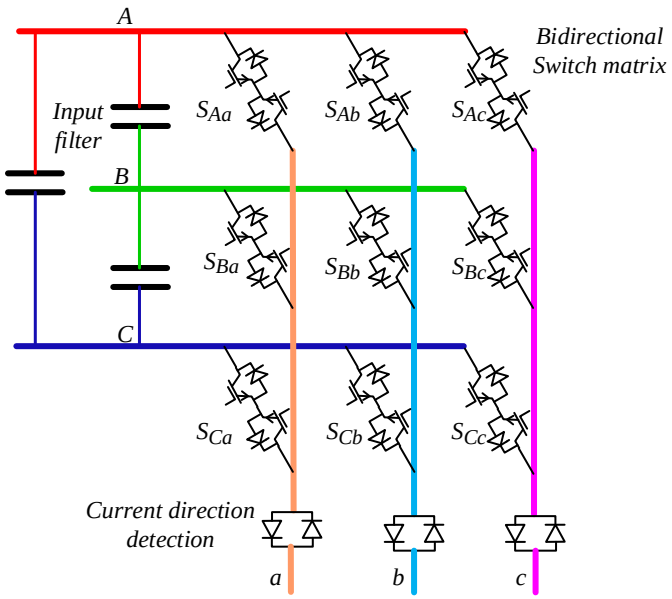


Figure 9.7: Schematic diagram of the direct matrix converter power circuit

Gate Drive Circuit

The gate drive circuit of the direct matrix converter is shown in Figure 9.8. The gate drive circuit comprises of the buffer, the opto-coupler, the push-pull amplifier and the isolated power supply. A structure diagram of the gate drive circuit for each bidirectional switch of the direct matrix converter is presented in Figure 9.9. The function of a gate drive circuit is to amplify the switching signals generated by the control platform in order to drive the IGBT module. There is a push-pull amplifier in the gate drive circuit to source the current when the switch is turned on and to sink the current when the switch is turned off. In addition, another function of the gate drive circuit is to provide electrical isolation between the low voltage platform and the high voltage power devices by using an isolated DC-DC converter and an opto-coupler. The opto-coupler will isolate signals between control platform buffers and the push-pull amplifiers.

The switch signals generated from the control platform are amplified by the gate drive circuit to drive the bidirectional switch. The function of the

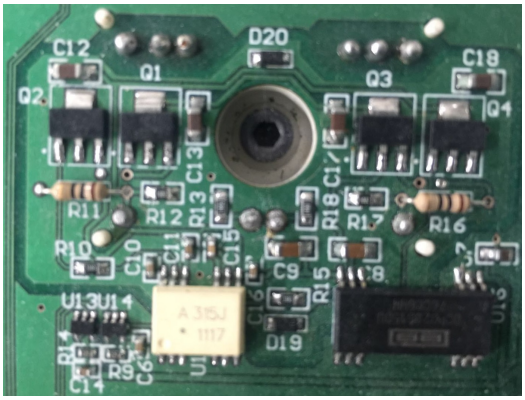


Figure 9.8: Direct matrix converter gate drive circuit

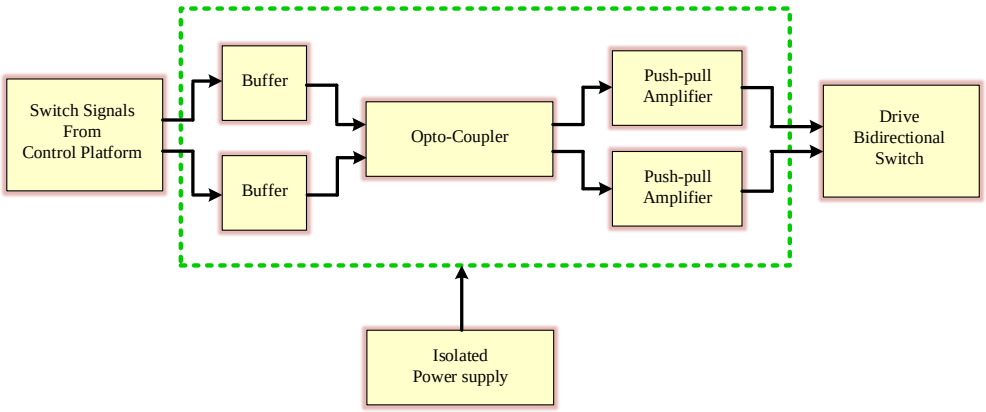


Figure 9.9: A diagram of the gate drive circuit for a bidirectional switch

buffer is to buffer each switch signal from the control platform. The function of the opto-coupler is to provide the electrical isolation between the low voltage control platform and the high voltage power circuit. The function of the push-pull amplifier is to provide the gate voltage and current when switch on or off an IGBT. The function of the isolated power supply is to generate isolated $\pm 15V$ voltage supply used for the output of the opto-coupler from a $5V$ DC supply.

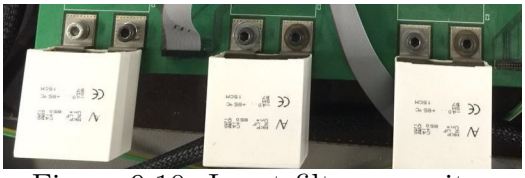


Figure 9.10: Input filter capacitor

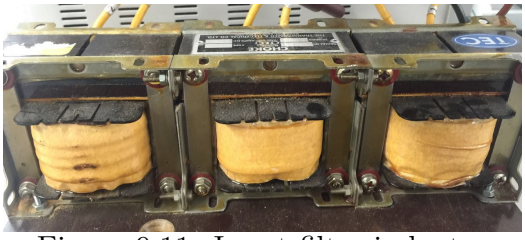


Figure 9.11: Input filter inductor

Input Filter

The function of the input filter is to attenuate the high frequency harmonics in the input currents. There are three polypropylene film capacitors MKPC4BS mounted between the input phases of the matrix converter. The $2\mu F$ polypropylene film capacitors MKPC4BS are rated at $850V$ voltage with a tolerance of 5%. The input filter capacitor of the direct matrix converter is shown in Figure 9.10.

The input filter inductor of the direct matrix converter is shown in Figure 9.11. The inductance of the inductor is $0.128mH$ due to the hardware availability in the laboratory. In addition, the inductance of the three phase AC Variac is also used as the input filter inductor for the laboratory prototype. The input filter cut off frequency is designed to be lower than the switching frequency. In this experiment, the cut off frequency is designed to be around $3kHz$.

Current Direction Detection Circuit

The current direction detection circuit of the direct matrix converter is used to detect the output current direction of the direct matrix converter. The output current direction information is essential for the four step current

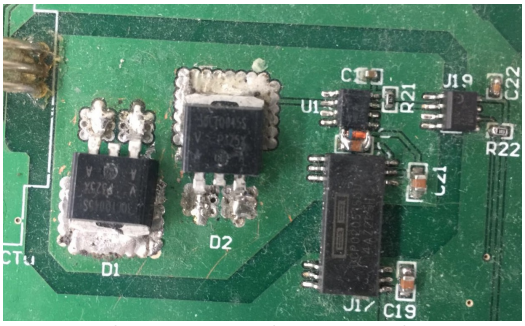


Figure 9.12: The current direction detection circuit

commutation strategy described in the previous chapter. The accurate detection of the output current direction will guarantee there is no input side short circuit or output side open circuit during a bidirectional switch commutation process. The current direction detection circuit of the direct matrix converter is shown in Figure 9.12.

The current direction detection circuit is composed of a pair of anti-paralleled Schottky diodes (30CTQ045S), a voltage comparator (LM311D), a high speed opto-coupler (HCPL-061N) and an isolated DC-DC converter (DCP020515). A diagram of the current direction detection circuit is shown in Figure 9.13. The function of the pair of anti-parallel Schottky diodes is to generate a voltage drop depending on the current i_{oa} direction. Using Schottky diode is a very high precision way to detect the output current direction because the voltage drop of the schottky diode is bigger than a resistance shunt when the current is near the natural zero crossing point. However, the schottky diode is not the most efficient option comparing to low resistance shunt. Therefore, the design of the current direction detection circuit depends on the specific application requirement. The function of the voltage comparator is to detect the direction of the voltage drop. The function of the high speed opto-coupler is to build electrical isolation between the power circuit and the control platform.

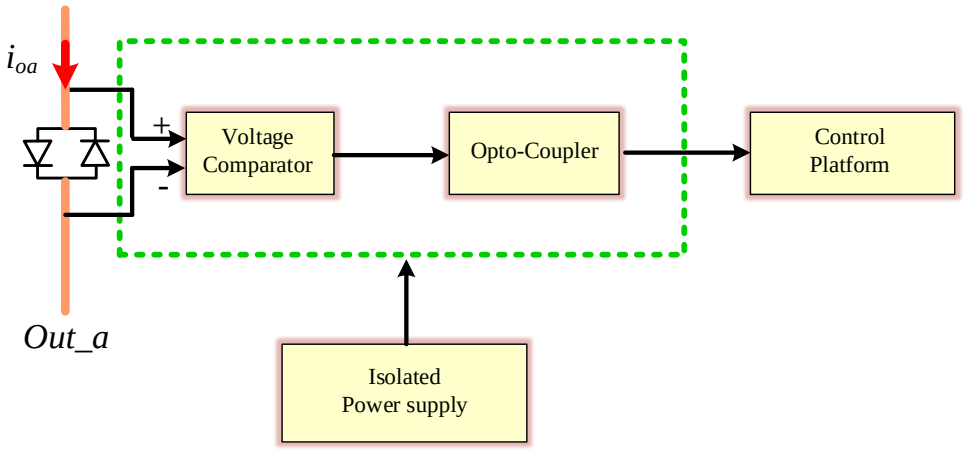


Figure 9.13: Diagram of the current direction detection circuit

Voltage Measurement Circuit

The voltage measurement circuit is placed on the top left of the power circuit to measure line-to-line input voltages required by the control stategy. The voltage transducer is Hall-effect LV25-P manufactured by LEM. This LV25-P voltage transducer can provide galvanic isolation between the power circuit and the control platform. The schematic diagram of the Hall-effect LV25-P voltage transducer is shown in the Figure 9.14. It can be seen from the Figure 9.14 that the voltage u_p to be measured is first converted to a current i_p at the primary side. Then the output signal of the voltage transducer is delivered by a output current i_M.

The LV25-P voltage transducer is set up as shown in Figure 9.14. i_p is the primary current generated by the measured voltage u_p, i_M is the secondary current and $i_M = 2.5i_p$ [82]. R_p is the external resistor and R_M is the measuring resistor. The external and measuring resistor values require to be decided in order to allow proper operation of the voltage transducer.

The value of the external resistor R_p can be calculated by Equation 9.1.The recommended range of i_p is from $-14mA$ to $+14mA$ [82]. Therefore, the external resistor R_p can be determined by ensuring primary current i_p is within that range.

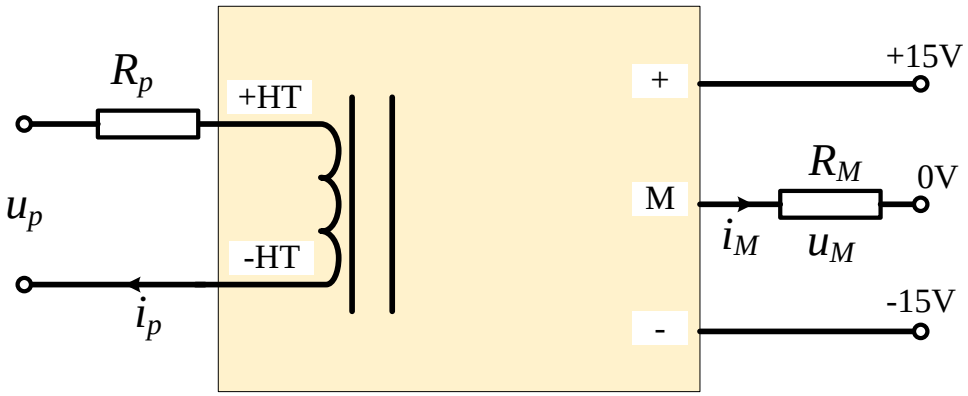


Figure 9.14: The schematic diagram of the LV25-P voltage transducer

$$\begin{aligned} \frac{1.2u_{p(max)}}{R_p} &< 14mA \\ R_p > \frac{1.2u_{p(max)}}{14mA} &= \frac{1.2 \times 50V}{14mA} = 4.29k\Omega \end{aligned} \tag{9.1}$$

Where $u_{p(max)}$ is the maximum possible value of u_p. Be noticed that a 20% safety margin is applied on the maximum voltage estimation. In this work a $40k\Omega$ resistor is used for R_p which will increase the safety margin bigger than 20%.

The value of the measuring resistor R_M is selected based on that u_M range. The maximum voltage range that can be measured across the measuring resistor is $\pm 5V$. Applying a voltage higher than $\pm 5V$ will saturate the A2D converter input. Due to the fact that $i_M = 2.5i_p$, the measuring resistor value can be calculated by Equation 9.2.

$$\begin{aligned} i_{M(max)}R_M = 2.5 \times \frac{1.2u_{p(max)}}{R_p}R_M &< 5V \\ R_M &< 1111\Omega \end{aligned} \tag{9.2}$$

In this work, a 190Ω resistor is used for R_M due to the hardware availability in the laboratory.



Figure 9.15: The clamp circuit

9.2.3 Clamp Circuit

The clamp circuit consists of 12 fast recovery diodes, the energy storage capacitors and the dissipated resistors. Since there is no DC-Link in the direct matrix converter topology, so a clamp circuit is required to protect the direct matrix converter switches from over-voltage damage. The function of the clamp circuit is to provide a path for the load current when there is an open circuit fault at the output load side of the direct matrix converter. The clamp circuit of the direct matrix converter is shown in Figure 9.15. Figure 9.16 shows the schematic diagram of the clamp circuit connected in parallel with the direct matrix converter.

It can be seen from Figure 9.15 that The 12 fast recovery diodes (RHRP30120) are mounted on the top of the clamp circuit to form a rectifier circuit. There are two $2200\mu F$, $400V$ electrolytic capacitors placed under the clamp circuit for mechanical reason. The $22k\Omega$ resistor is connected in parallel with the electrolytic capacitor in order to dissipate the energy stored in the electrolytic capacitor.

The clamp circuit will not work when the direct matrix converter is operating under healthy condition. When there is a fault such as an open circuit

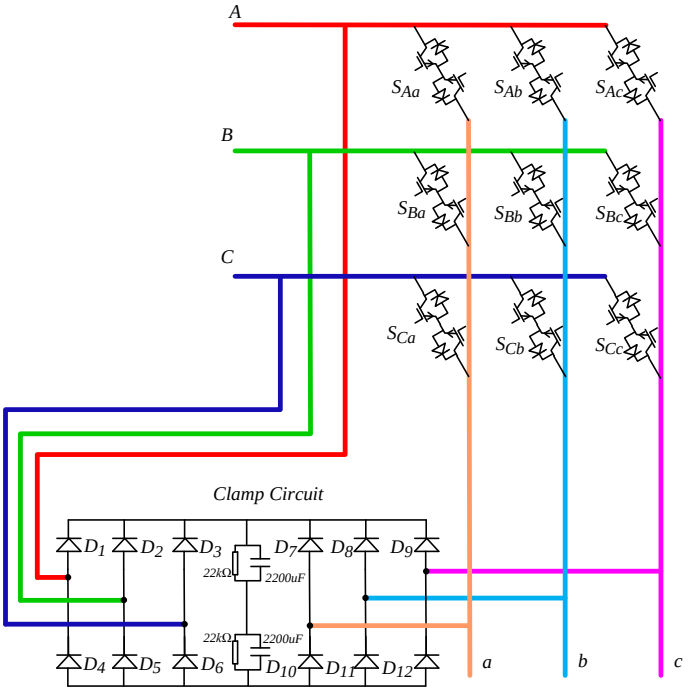


Figure 9.16: The schematic diagram of the clamp circuit

fault in the power switches or a commutation failure between bidirectional switches, the clamp circuit will provide a path for the output load current by using the fast recovery diodes as discussed in Chapter 5. The energy stored in the inductive load will be transferred to the clamp capacitor and then dissipated in the paralleled resistor.

The clamp capacitor is a key element in the clamp circuit. The size of the clamp capacitor will decide how much energy could be stored in the clamp circuit. The maximum energy stored in the inductive load should be taken into consideration when selecting the size of the clamp capacitor. The equation of the maximum energy stored in a three phase resistance-inductance load can be described in Equation in 9.3 [76].

$$\begin{aligned} E_{RLload} &= \frac{1}{2} L_{load} ({i_a}^2 + {i_b}^2 + {i_c}^2) \\ &= \frac{3}{4} L_{load} {I_p}^2 \end{aligned} \tag{9.3}$$

Where E_{RLload} is the maximum energy stored in the resistance-inductance load. L_{load} is the inductance of the $R-L$ load. i_a, i_b and i_c are the three phase balanced load currents and I_p is the amplitude of the output phase current.

When an output open-circuit fault occurs, the maximum energy absorbed by the clamp capacitor can be expressed in Equation 9.4. Where E_{clamp} is the maximum energy absorbed by the clamp capacitor, C_{clamp} is the capacitance of the clamp circuit, V_{max} is the maximum acceptable clamp voltage related to the voltage rating of the power switches, V_{int} is the initial clamp voltage equal to the input line-to-line peak voltage.

$$E_{clamp} = \frac{1}{2} C_{clamp} ({V_{max}}^2 - {V_{int}}^2) \tag{9.4}$$

Due to the fact that the maximum energy stored in the resistance-inductance load must be lower than the energy absorbed by the clamp capacitor, so the capacitance of the clamp circuit can be calculated by Equation 9.5.

$$C_{clamp} > \frac{3}{2} \frac{L_{load} {I_p}^2}{{V_{max}}^2 - {V_{int}}^2} \tag{9.5}$$

For the worst scenario, the acceptable clamp voltage rate is $800V$, The maximum IGBT current is $60A$ and the load inductance is $17mH$. After calculation, the clamp capacitor size is around $145\mu F$. In the experiment, the clamp capacitor of $1100\mu F$ is selected for safety purpose.

9.2.4 Low Bandwidth Current Sensor

Since only one sample is required for the voltage and current signals during one sampling period for the fault diagnosis algorithm with the finite-control-set model-predictive-control (FCS-MPC) strategy as discussed in Chapter 5, so low bandwidth current sensors with a bandwidth of $200kHz$ can satisfy the fault diagnosis requirement.

Three low bandwidth current transducers are used for the direct matrix converter FCS-MPC strategy fault detection and diagnosis. These three current transducers are Hall-effect sensors LA55-P manufactured by LEM and are connected as shown in Figure 9.17. The frequency bandwidth of the LA55-P current transducer is $200kHz$ [83]. The LA55-P current transducer can provide galvanic isolation between the power circuit and the control platform.

A schematic diagram of the low bandwidth current measurement circuit

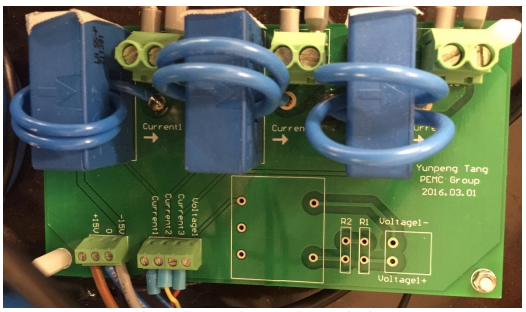


Figure 9.17: The low bandwidth current sensor

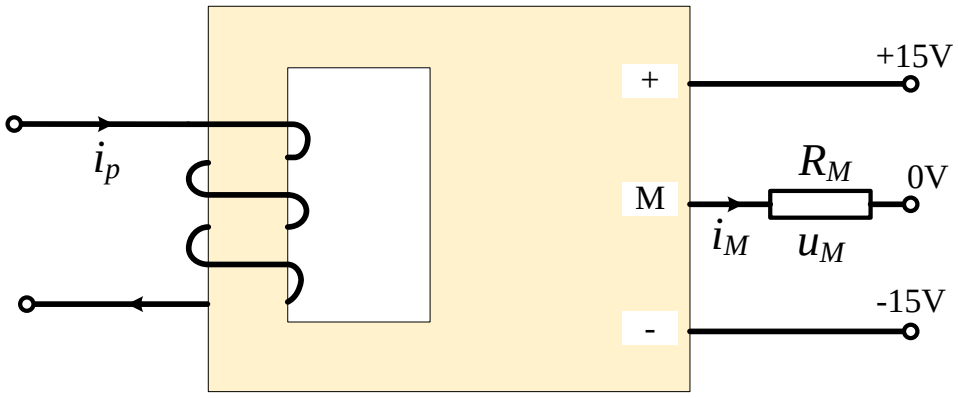


Figure 9.18: The schematic diagram of the low bandwidth current sensor measurement circuit

used for measuring the direct matrix converter output phase current is shown in Figure 9.18. The two primary side terminals of the current transducer are connected in series with one direct matrix converter output phase. The measured current in the primary side will generate a secondary current in the secondary side of the current transducer with a conversion ratio of $1:1000$. Then the secondary current of the transducer will flow through a measurement resistor R_M. The maximum voltage range across the measurement resistor is $\pm 5V$. Applying a voltage higher than this range will saturate the input of the A2D converter. Due to the fact that $i_p = 1000 i_M$, so the value of the measurement resistor R_M can be determined by Equation 9.6.

$$\begin{aligned} u_M = i_M R_M < 5V \\ R_M < \frac{5V}{i_{M(max)}} = \frac{5V}{10mA} = 500\Omega \end{aligned} \tag{9.6}$$

In this work, a 190Ω resistor is used for the measurement resistor R_M due to the hardware availability in the laboratory.

9.2.5 High Bandwidth Current Sensor

When implementing fault diagnosis algorithm with space vector modulation (SVM) strategy, more than one samples are required during each sampling period. For example, there are 10 switching states in one modulation period with One-Zero-SVM as discussed Chapter 5.

Due to the fact that there are four active vectors and at least one zero vector are applied in each modulation period, a high bandwidth current sensor is required to monitor the output current at each applied vector. When the SVM modulation frequency is set to be $12.5kHz$, the bandwidth of the current sensor should be higher than $1MHz$ in order to detect the rising and falling edges of the faulty current. This is because each switching vector is forced to apply for at least $1us$ by the DSP/FPGA control platform.

To achieve high bandwidth of the current sensor, a shunt resistor is implemented. The high bandwidth current sensor comprises of a shunt resistor, an amplifier, an analog-to-digital converter (ADC), an isolator and differential transceivers. A schematic diagram of the high bandwidth current sensor is shown in Figure 9.19. A shunt resistor is connected in series with the direct matrix converter output phase to generate a voltage drop V_s when a current i_{oa} flows through it. Then, the generated voltage drop V_s will be amplified and level shifted by the amplifier in order to satisfy the input requirement of the ADC. The $SDATA$ in Figure 9.19 means the serial digital signal generated by the ADC. The $CLOCK$ means the clock signal of the ADC. The CS signal is the chip select signal of the ADC.

Next, the ADC will start converting from analog signal to digital signal and send the digital signal $SDATA$ to the control platform via an isolator and transceivers after conversion. Meanwhile, the control platform will send clock signal $CLOCK$ and chip select signal CS to the ADC via transceivers and an isolator in order to control the output of the ADC. The three high bandwidth current transducers used for the direct matrix converter SVM strategy fault detection and diagnosis are shown in Figure 9.20. A more detailed description of each element in the high bandwidth current sensor is given in the following section.

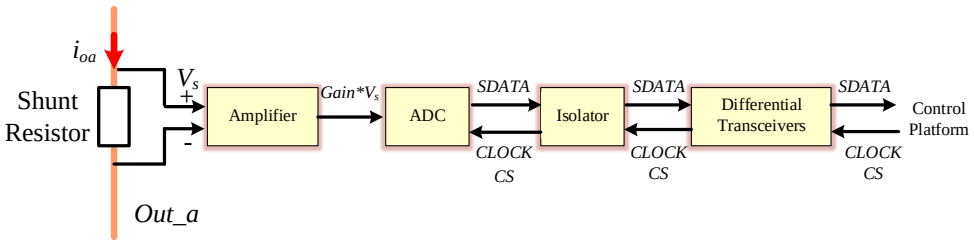


Figure 9.19: The schematic diagram of the high bandwidth current sensor

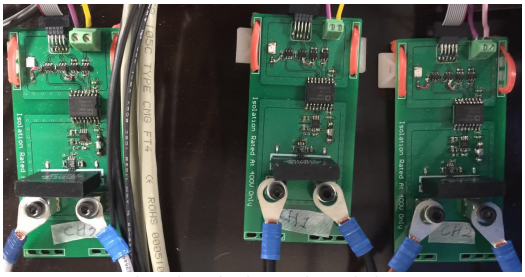


Figure 9.20: The high bandwidth current sensor

Shunt Resistor

In this work, the CS3FR050E shunt with kelvin terminals is used as the shunt resistor. The shunt resistance is 0.05Ω and the tolerance of the shunt resistor is 1%. A voltage drop V_s across the shunt will be measured when a current flows through the shunt resistor. The shunt schematic is shown in Figure 9.21. It can be seen from the schematic that two of the shunt terminals are connected in series with the direct matrix converter output phase. Another two terminals are connected to the input of the amplifier which will be described next.

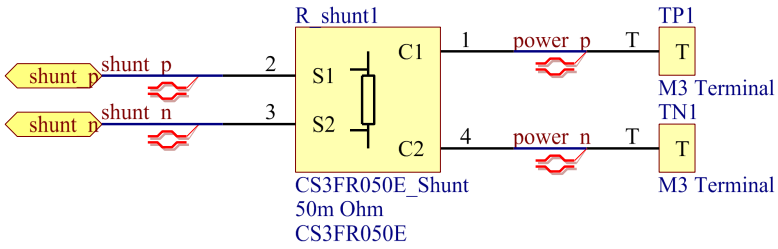


Figure 9.21: Schematic of Shunt

Amplifier

The amplifier used in this work is the LT1999-10 bidirectional current sense amplifier. The bandwidth of the amplifier is $2MHz$ at the $-3dB$ point. The gain of the amplifier is $10V/V$. The gain of the amplifier is chosen based on the shunt resistance value. If accuracy is of greater importance than efficiency in the experiment, the highest valued shunt resistor is recommended to use together with the lowest valued gain amplifier. If efficiency is of greater importance than accuracy, the lowest valued shunt resistor is recommended to use together with the highest valued gain amplifier. In this work, the accuracy factor is more important than th efficiency factor, so the highest valued 0.05Ω shunt resistor is used together with the amplifier with the lowest valued gain of 10. The amplifier schematic is shown in Figure 9.22. It can be seen from the Figure 9.22 that the VCC is decoupled from the GND by a $0.1\mu F$ and a $4.7\mu F$ capacitors. A $10pF$ capacitor is used to prevent dv/dt edges on the input from coupling to the floating shutdown pin $SHDN$. The amplifier output pin is connected to a RC low pass filter whose cut-off frequency is $33MHz$. The resistance of the RC low pass filter is set to 470Ω and the capacitance of the RC low pass filter is set to $10pF$.

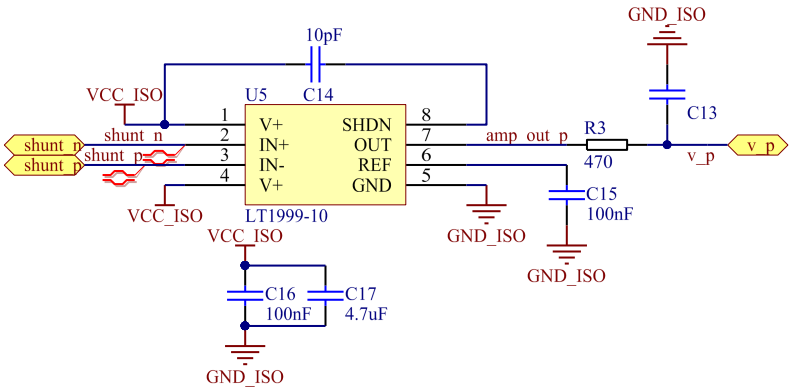


Figure 9.22: Schematic of operational amplifier

Analog to Digital Converter (ADC)

The analog to digital converter (ADC) used in this work is the AD7451 12-bit ADC with $1Msps$ throughput rate as shown in Figure 9.23.. The track-and-hold (T/H) amplifier in the AD7451 ADC can handle input frequencies up to $3.5MHz$. It can be seen from the Figure 9.23 that the input pin 7 is the ADC clock input and the ADC clock is set to $10MHz$ in this work. The input pin 5 is the chip select signal CS and it is active low. The ADC output data is transferred to the control platform with Serial Peripheral Interface (SPI) through pin 6.

The timing diagram of the ADC AD7451 is shown in Figure 9.24. It can be seen from the Figure 9.24 that the chip select signal CS initiates the conversion process and frames the data transfer. The falling edge of the chip select signal CS will take the serial data bus out of the three-state. Then the analog input is sampled and the conversion is initiated. The analog-to-digital conversion requires 16 clock cycles to finish. The ADC input clock signal controls the transfer of data during conversion. The output serial data bits are clocked out on the falling edge of the clock signal. The data stream of the AD7451 comprises of four leading zeros, followed by 12 bits of conversion data as shown in the Figure 9.24.

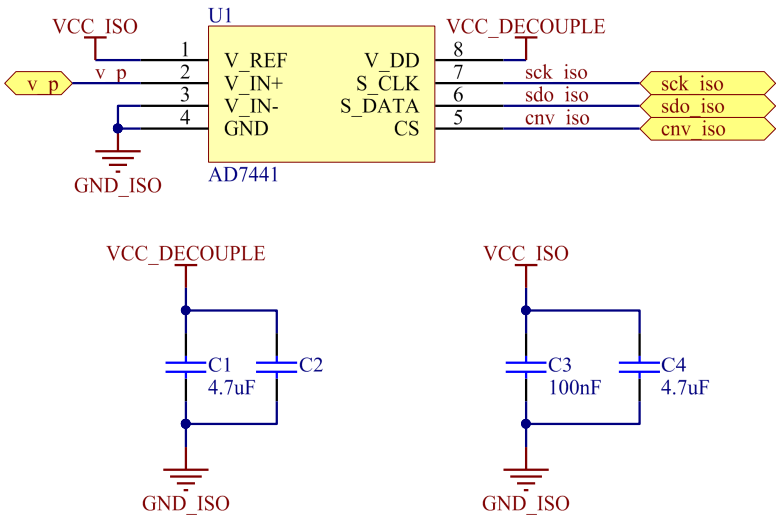


Figure 9.23: Schematic of adc

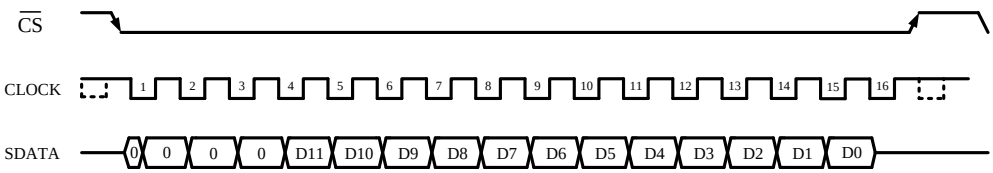


Figure 9.24: Timing diagram of adc

Isolator

The isolator used in this work is the ADuM5402 quad-channel isolator with integrated DC-to-DC converter. The function of the isolator is to provide galvanic isolation between the power circuit and the control platform. The schematic of the isolator is shown in Figure 9.25. It can be seen from Figure 9.25 that the pin 16 of the ADuM5402 will provide an isolated voltage source which will supply the ADC and amplifier as mentioned before. There are four signal isolation channels in the ADuM5402 at a maximum data rate of $25Mbps$. Channel A is for the ADC clock signal and Channel B is for the chip select signal. Channel C is for the ADC output serial data signal and Channel D is for the ADC clock echo signal. The function of the ADC clock echo signal is to overcome the isolator to isolator time jitter problem. This is because even from the same batch the isolator to isolator time jitter is varying from $50ns$ to $100ns$, which will cause the outputs of each isolator can not be clocked-in at exactly the same time. However, the channel to channel jitter of a single isolator is varying only from $5ns$ to $10ns$. Therefore, the SPI clock of the ADC is fed-back across the isolation barrier as the clock echo signal in order to overcome the isolator to isolator time jitter issue.

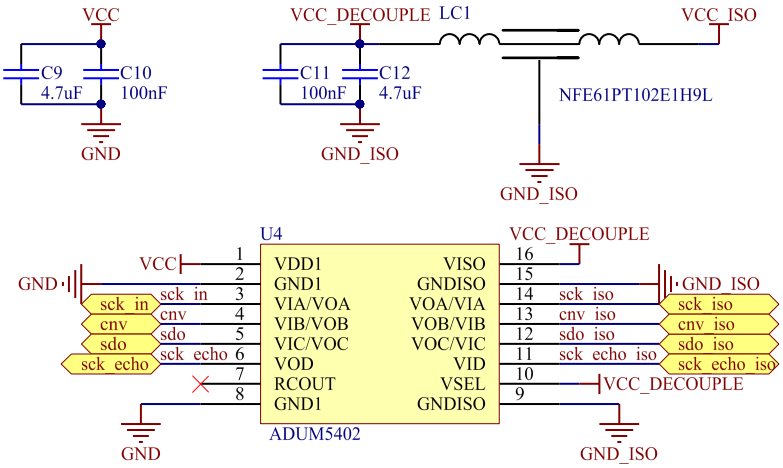


Figure 9.25: Schematic of isolator

transceivers

The transceivers used in this work are for RS-485 and RS-422 communication. The transmitter used in this work is the MAX3295 RS-485/RS-422 transmitter which can operate at data rates up to $20Mbps$. The receiver used in this work is the MAX3281E RS-485/RS-422 receiver which can operate at data rates up to $52Mbps$. The schematic of the transceivers is shown in Figure 9.26. The signals such as ADC clock signal, ADC chip select signal, and ADC serial output data signal are flow through the transceivers with high noise immunity due to the nature of the differential signals in the RS-485 communication.

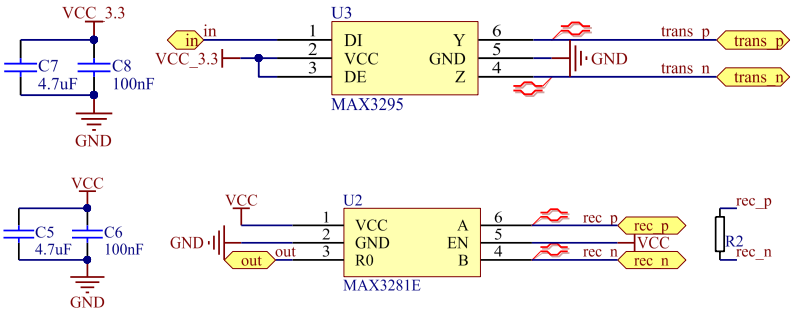


Figure 9.26: Schematic of tranceiver

9.2.6 Matrix Converter Control Platform

This section introduces the hardware implementation of the direct matrix converter control platform as shown in Figure 9.27. The diagram of the overall implementation of the direct matrix converter control system is shown in Figure 9.28. The matrix converter control platform consists of a digital signal processor (DSP) card, a field programmable gate array (FPGA) card, a host port interface (HPI) daughter card and a high bandwidth current sensor interface card. The main function of the DSP card is to calculate the control algorithm of the direct matrix converter. The main function of the FPGA card is to generate the PWM gate drive signal. The function of the HPI daughter card is to realize bidirectional data transmission between the host PC and the DSP card without interfering the normal operation of the DSP card. The function of the high bandwidth current sensor interface card is to provide bidirectional data transmission between the FGPA card and the high bandwidth current sensor.

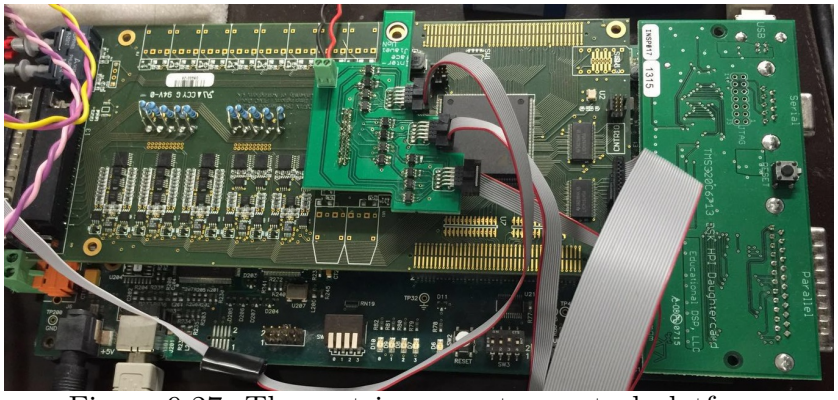


Figure 9.27: The matrix converter control platform

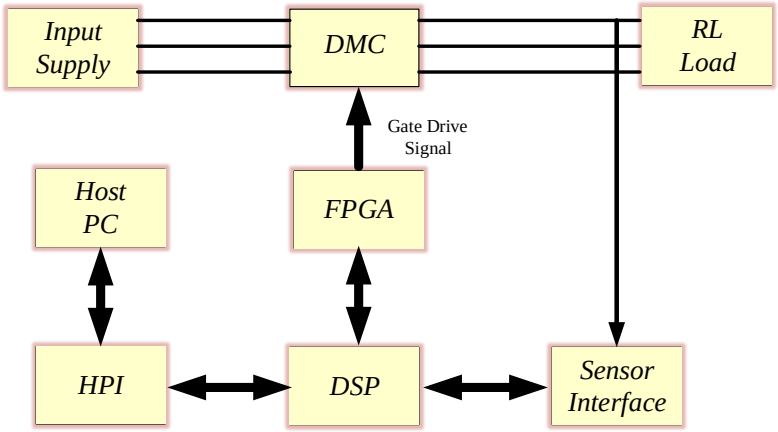


Figure 9.28: Overall direct matrix converter control system implementaiton

Digital Signal Processor (DSP) Card

The DSP development board with a high-performance Texas Instruments TMS320C6713 floating-point digital signal processor is shown in Figure 9.29. The clock frequency of the DSP is $225MHz$. In this work, the SVM algorithm and the FCS-MPC algorithm are executed in the DSP respectively. For the FCS-MPC algorithm, it is executed at every interrupt interval of $100\mu s$. For the SVM algorithm, it is executed at every interrupt interval of $80\mu s$. In addition, the fault detection and diagnosis algorithm is implemented in the DSP card in order to achieve real-time fault detection and diagnosis.

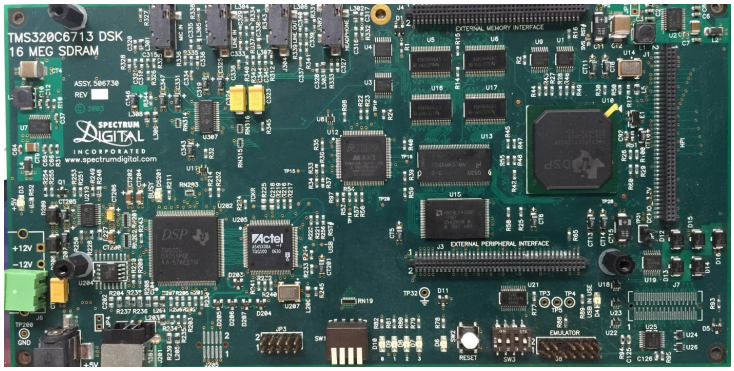


Figure 9.29: The digital signal processor card

Field Programmable Gate Array (FPGA) Card

The FPGA card shown in Figure 9.30 is designed and developed by the PEMC group of the University of Nottingham [84]. A high performance Actel ProASIC3 FPGA is implemented in this flexible and versatile FPGA card in order to interface with the TMS320C6713 DSP to control the direct matrix converter. There are ten 12-bit analog-to-digital conversion channels on the FPGA card for control purpose [81]. The switch signals generated by the FPGA card are transmitted to the gate drive circuits through the specific output pins.

Several versions of the FPGA firmware have been previously developed with reference to specific application requirements. In this work the FPGA card is developed in order to realize oversampling fault detection and diagnosis in the direct matrix converter system. One function of the newly developed FPGA cores is to provide an interface between the high bandwidth current sensor and the FGPA card. Another function of the FGPA cores is to reconfigure the switch signal output pins in order to generate an open circuit switch fault. In addition, one more function of the FPGA cores is to feedback the switching state to the DSP during each interrupt interval for fault detection and diagnosis purpose.

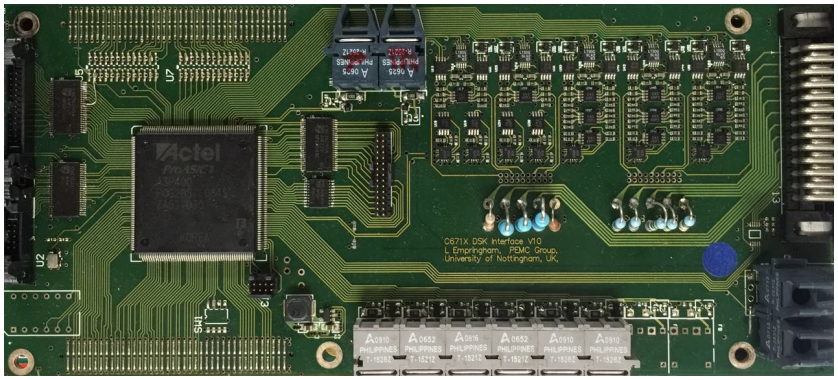


Figure 9.30: The field programmable gate array card

Host Port Interface (HPI) Daughter Card

The Educational DSP DSK6713HPI daughter card is shown in Figure 9.31. Through the HPI daughter card, an external host PC can directly read the entire DSP memory space without interfering the normal operation of the DSP. In addition, an external host PC can also modify the variables in the DSP in order to trigger an open circuit switch fault at the proper time-point. A host program in MATLAB has been developed to provide the data visualization ability as well as the state trigger ability. The HPI daughter card can capture data from the DSP memory and plot the data in the MATLAB. In addition, the HPI daughter card can modify the variables in the DSP to trigger a switch fault through the developed MATLAB graphical user interface (GUI).

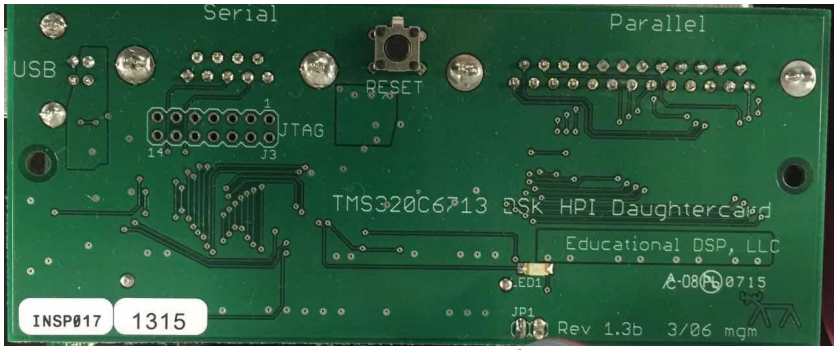


Figure 9.31: The host port interface daughter card

The Interface Card for The High Bandwidth Current Sensor

The interface card for the high bandwidth current sensor is shown in Figure 9.32. The function of the interface card is to provide bidirectional data transmission between the FPGA card and the high bandwidth current sensor. The interface card consists of six MAX3295 transmitters and six MAX3281E receivers. The six MAX3295 transmitters provide the signal channels for the ADC clock signal and chip select signal. The six MAX3281E receivers provide the signal channels for the serial data output signal and the clock echo signal.

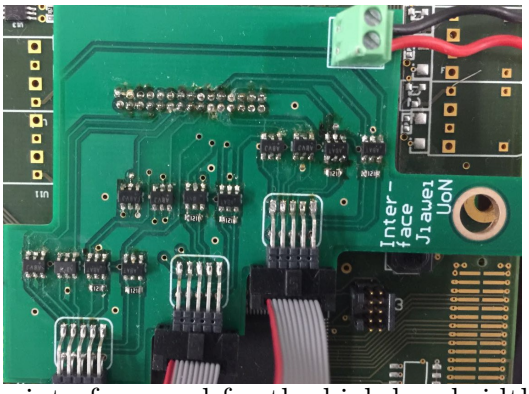


Figure 9.32: The interface card for the high bandwidth current sensor

Author contribution to the experimental rig

The original contribution in the experimental rig setting up including current sensor design, current sensor interface design, experimental rig build up and fault diangosis algorithm development.

9.3 Experimental Fault Diagnosis Results for Statistic Analysis Purpose

In total of 44 sets of fault diagnosis results are being investigated to do the statistic analysis. There are shown from Fig 9.33 to Fig 9.75.

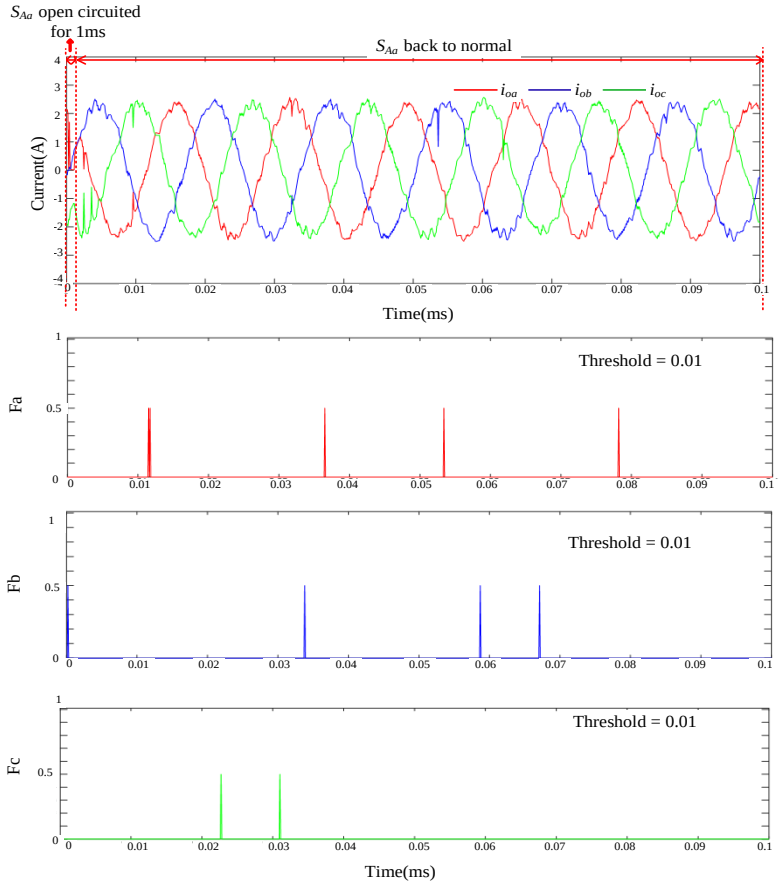


Figure 9.33: Fault diagnosis on experiment number 1, threshold value $th = 0.01$

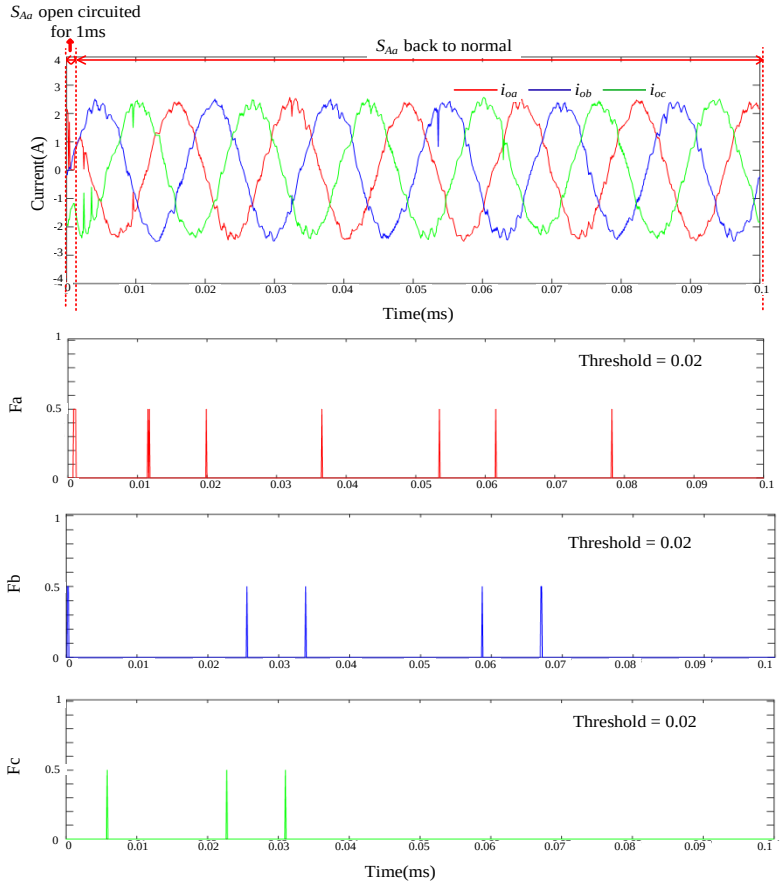


Figure 9.34: Fault diagnosis on experiment number 1, threshold value $th = 0.02$

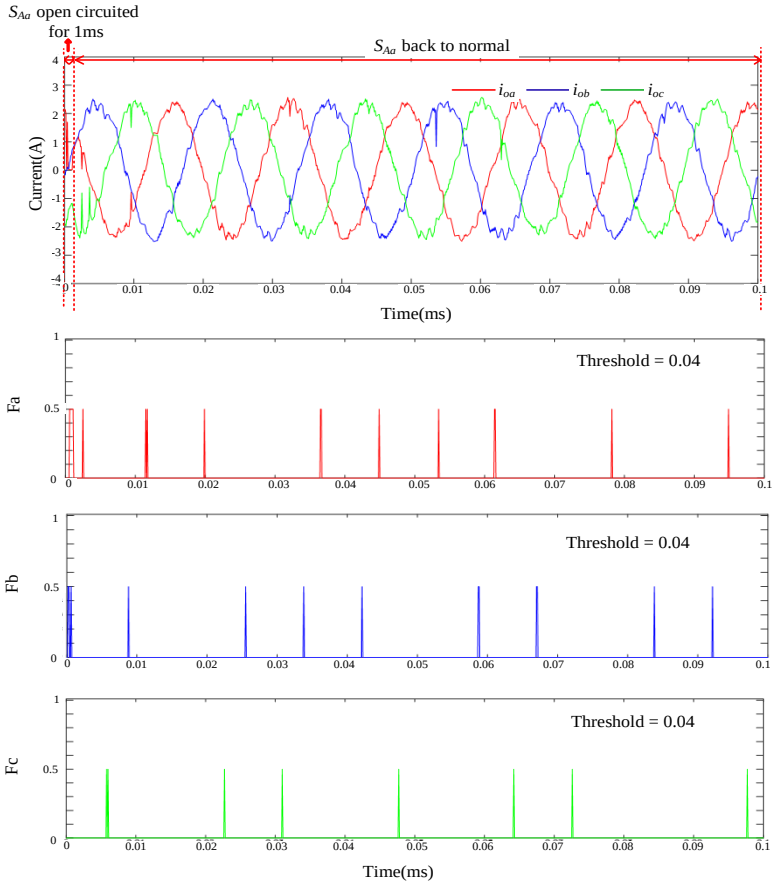


Figure 9.35: Fault diagnosis on experiment number 1, threshold value $th = 0.04$

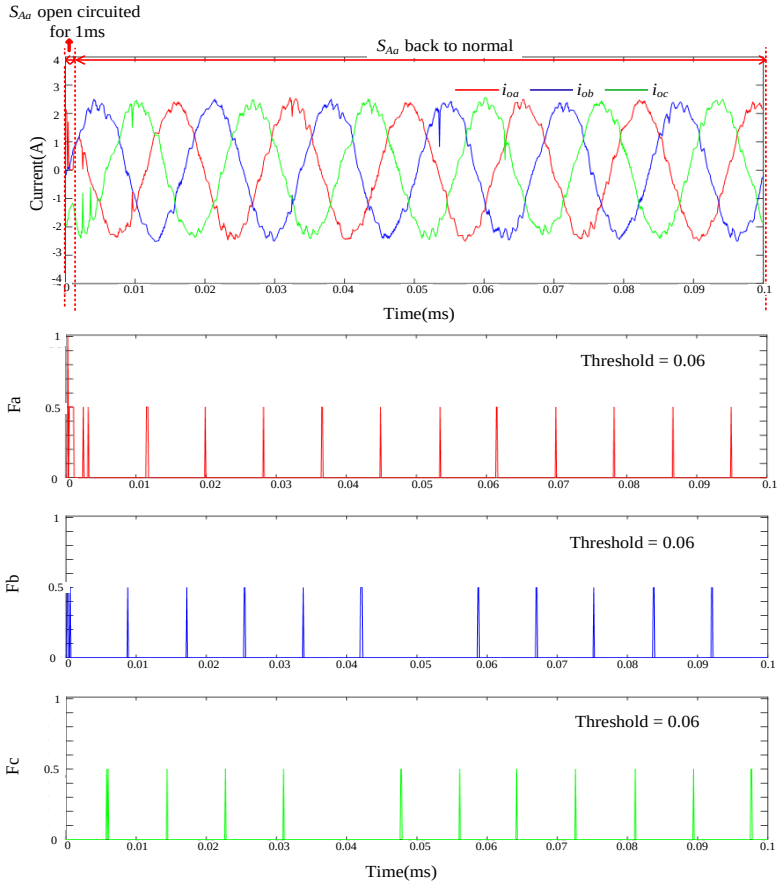


Figure 9.36: Fault diagnosis on experiment number 1, threshold value $th = 0.06$

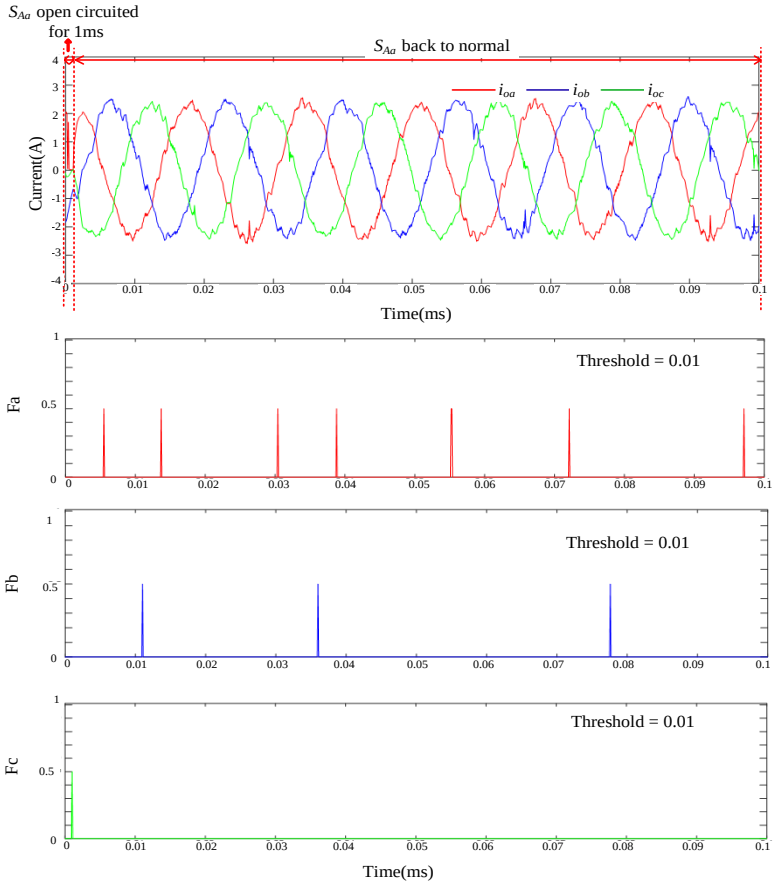


Figure 9.37: Fault diagnosis on experiment number 2, threshold value $th = 0.01$

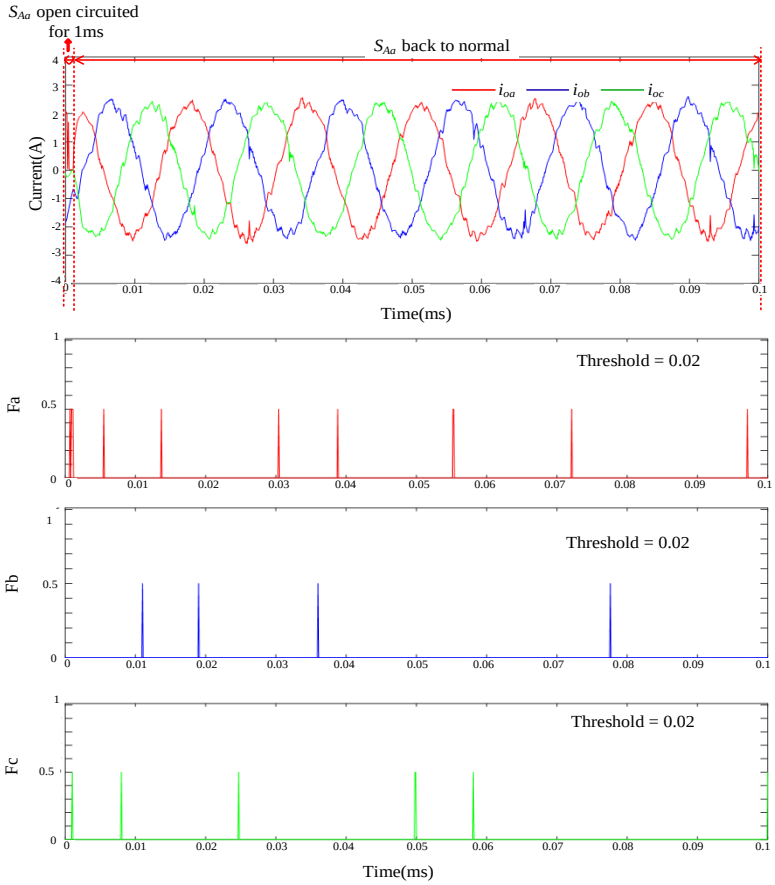


Figure 9.38: Fault diagnosis on experiment number 2, threshold value $th = 0.02$

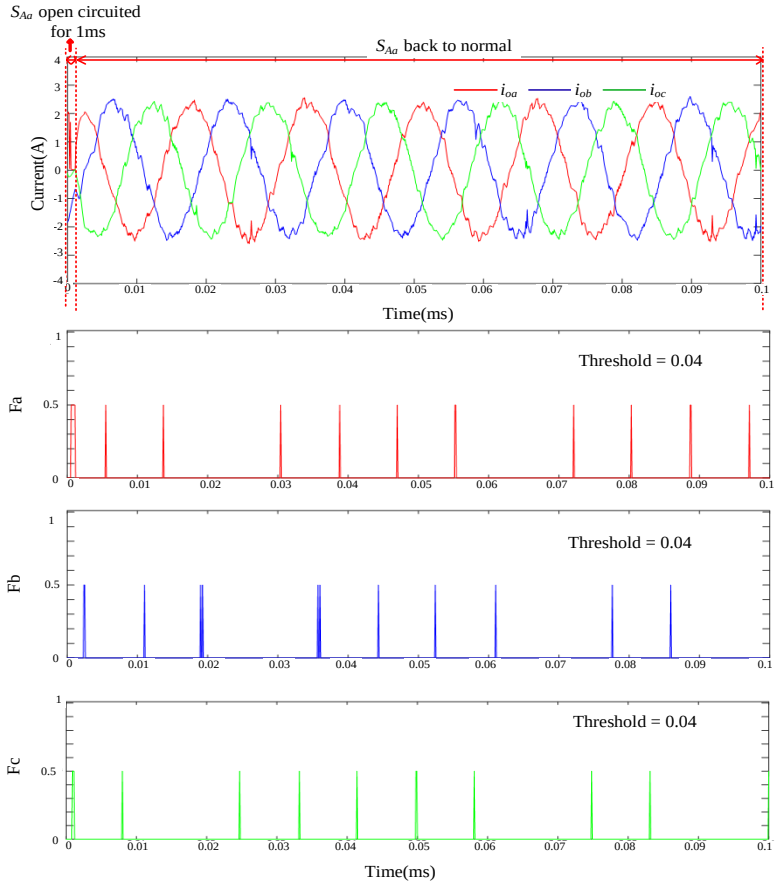


Figure 9.39: Fault diagnosis on experiment number 2, threshold value $th = 0.04$

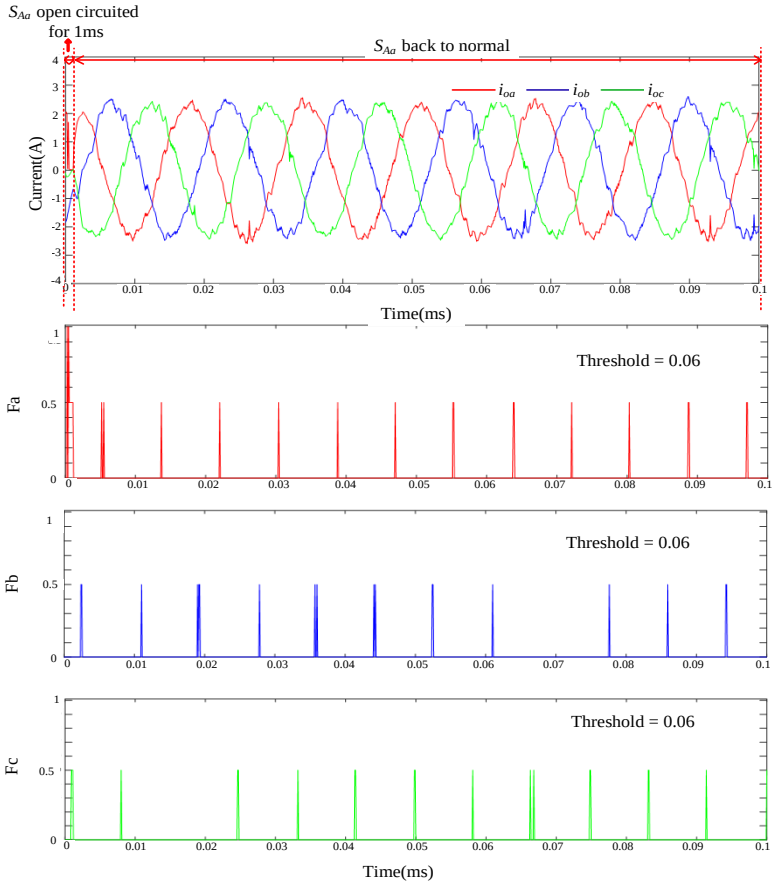


Figure 9.40: Fault diagnosis on experiment number 2, threshold value $th = 0.06$

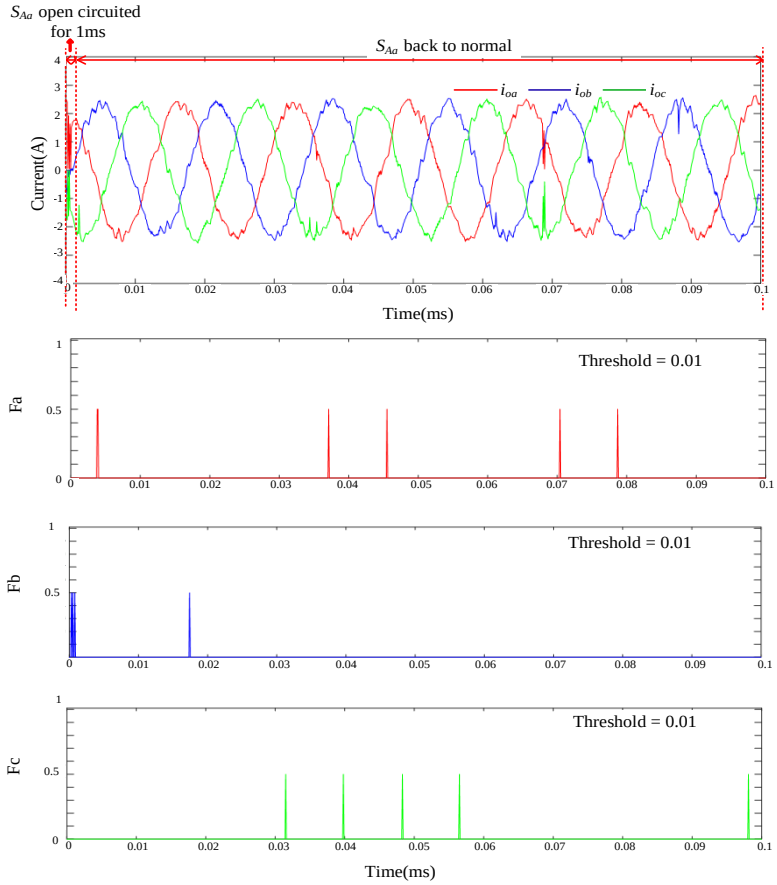


Figure 9.41: Fault diagnosis on experiment number 3, threshold value $th = 0.01$

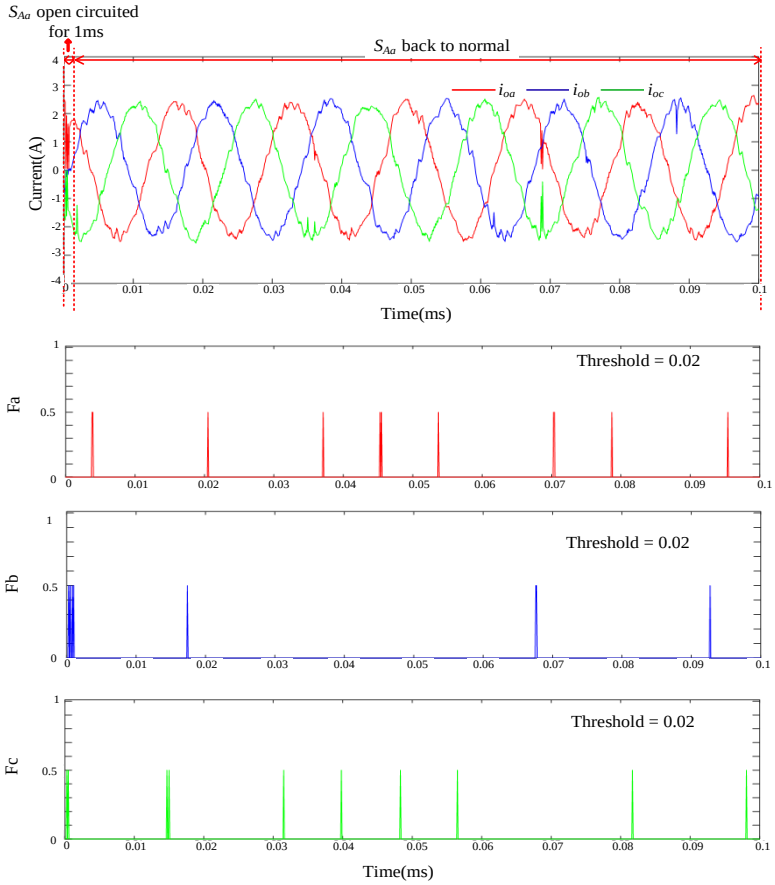


Figure 9.42: Fault diagnosis on experiment number 3, threshold value $th = 0.02$

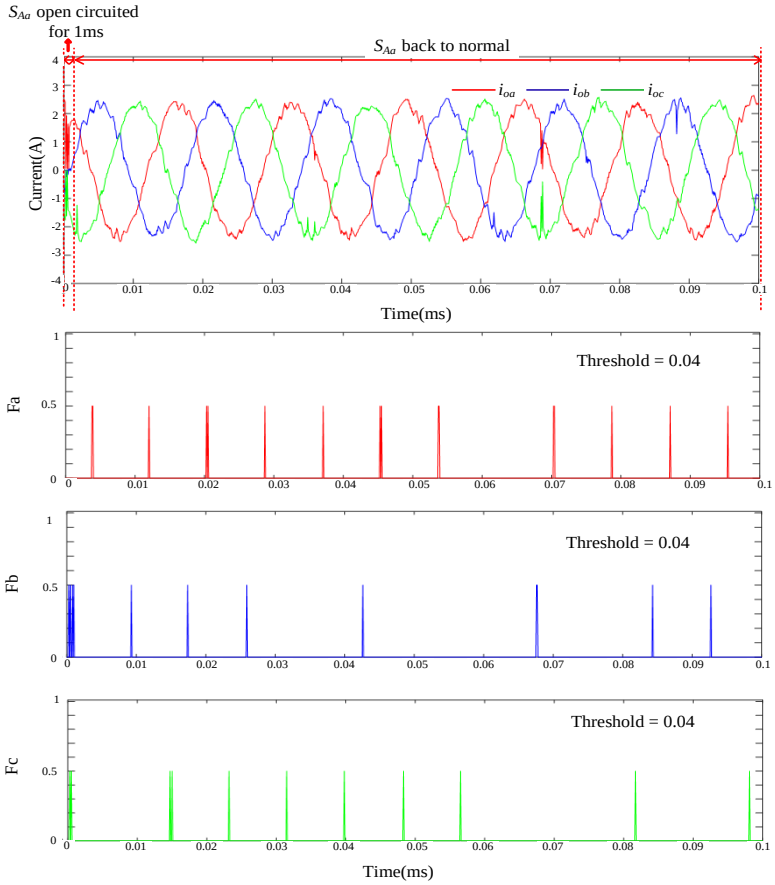


Figure 9.43: Fault diagnosis on experiment number 3, threshold value $th = 0.04$

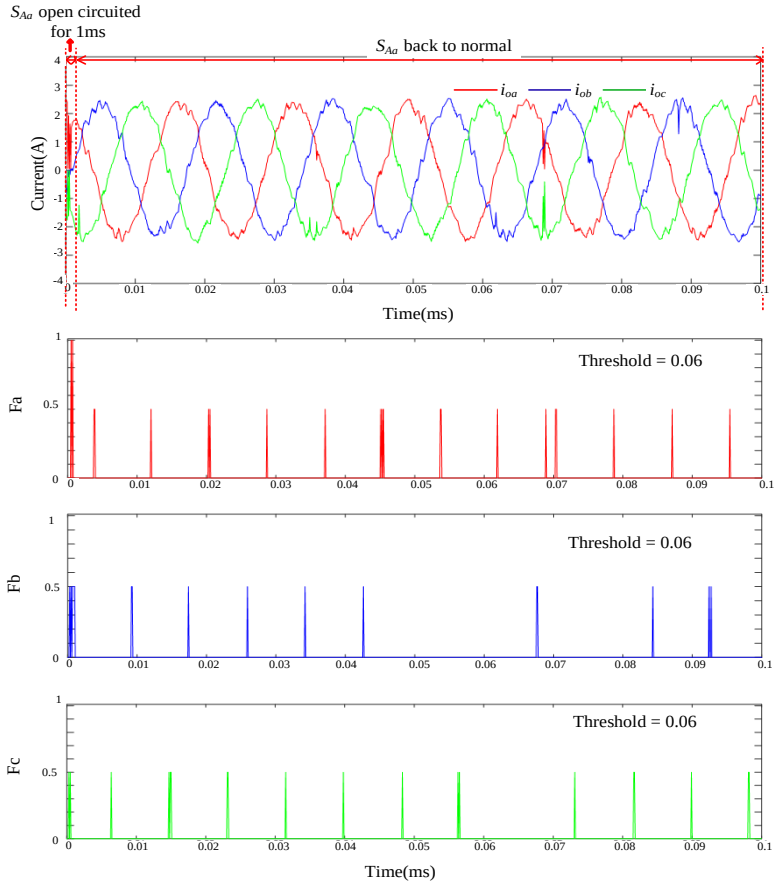


Figure 9.44: Fault diagnosis on experiment number 3, threshold value $th = 0.06$

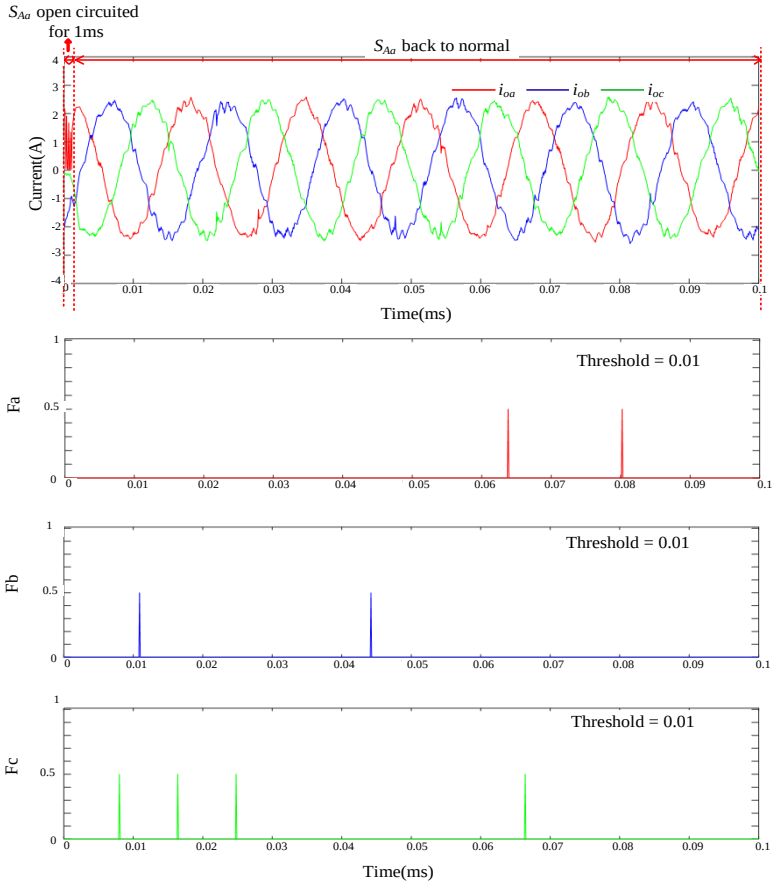


Figure 9.45: Fault diagnosis on experiment number 4, threshold value $th = 0.01$

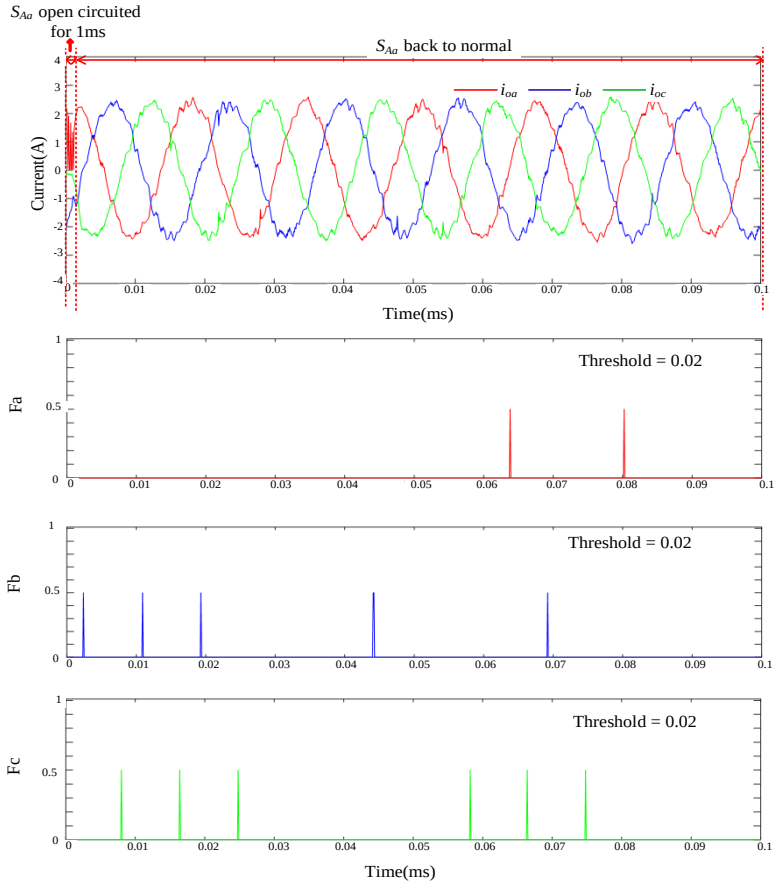


Figure 9.46: Fault diagnosis on experiment number 4, threshold value $th = 0.02$

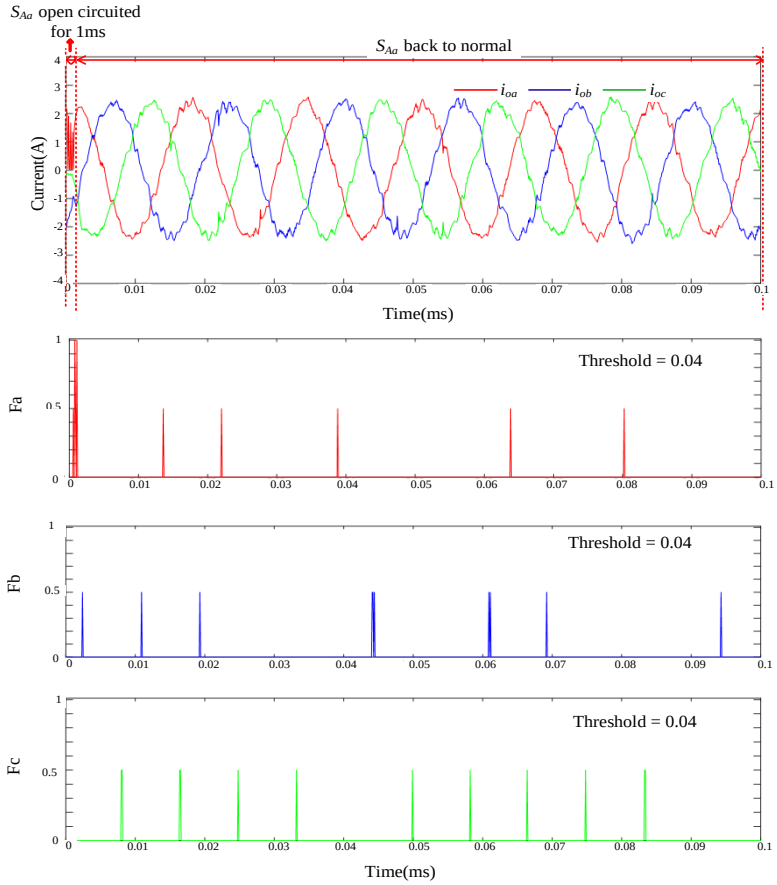


Figure 9.47: Fault diagnosis on experiment number 4, threshold value $th = 0.04$

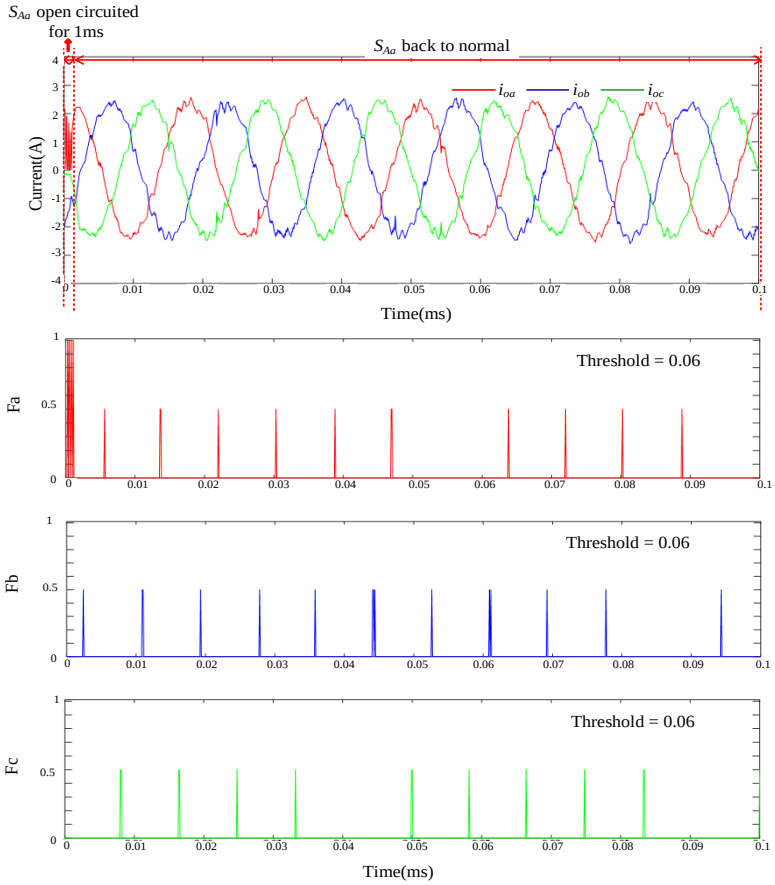


Figure 9.48: Fault diagnosis on experiment number 4, threshold value $th = 0.06$

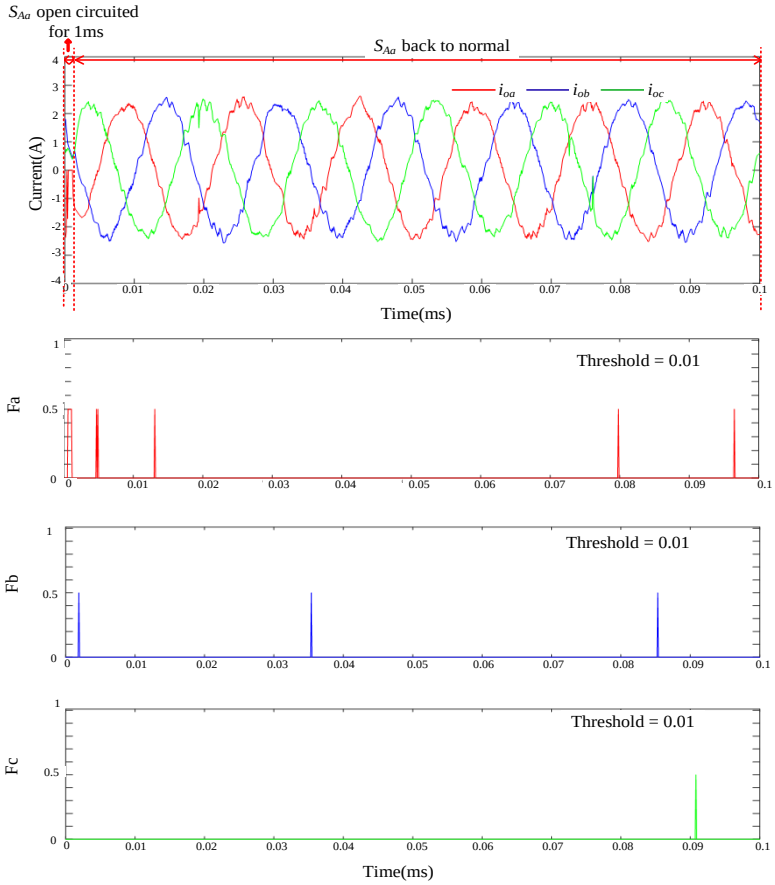


Figure 9.49: Fault diagnosis on experiment number 5, threshold value $th = 0.01$

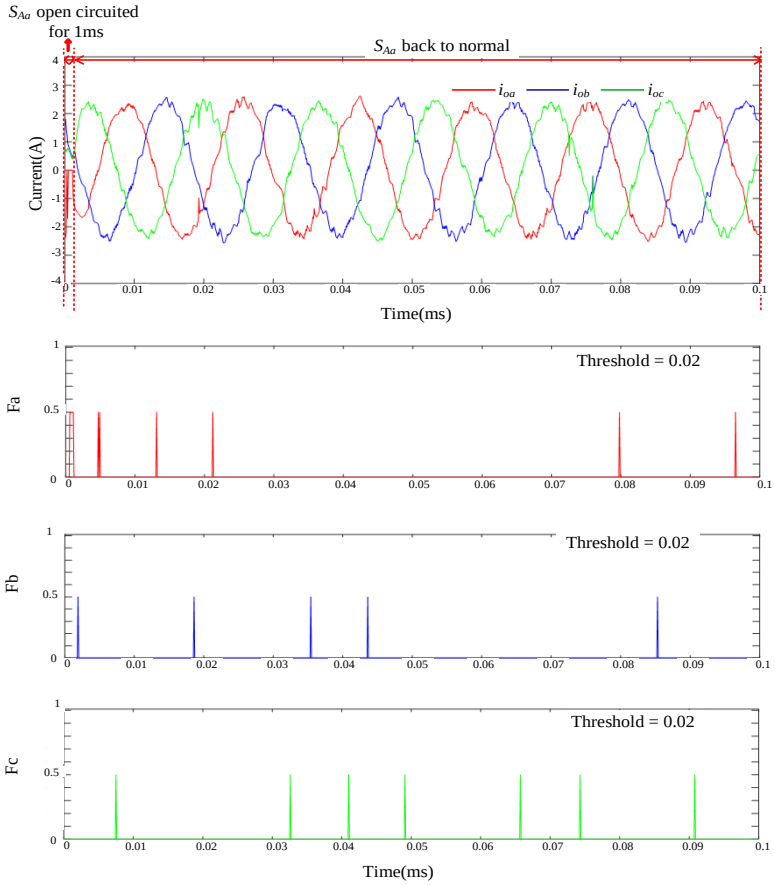


Figure 9.50: Fault diagnosis on experiment number 5, threshold value $th = 0.02$

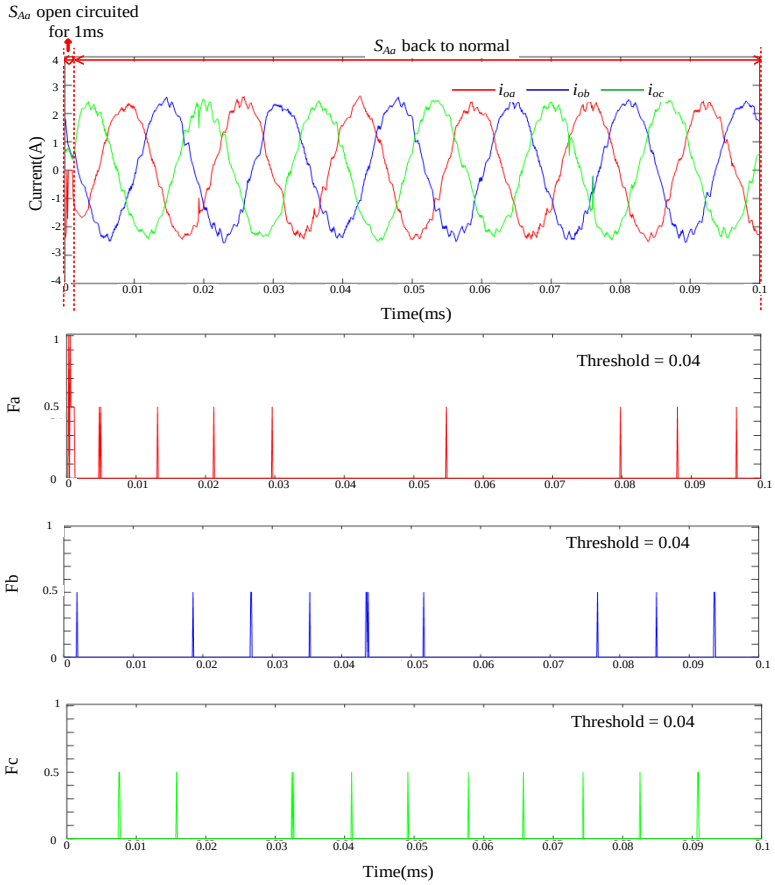


Figure 9.51: Fault diagnosis on experiment number 5, threshold value $th = 0.04$

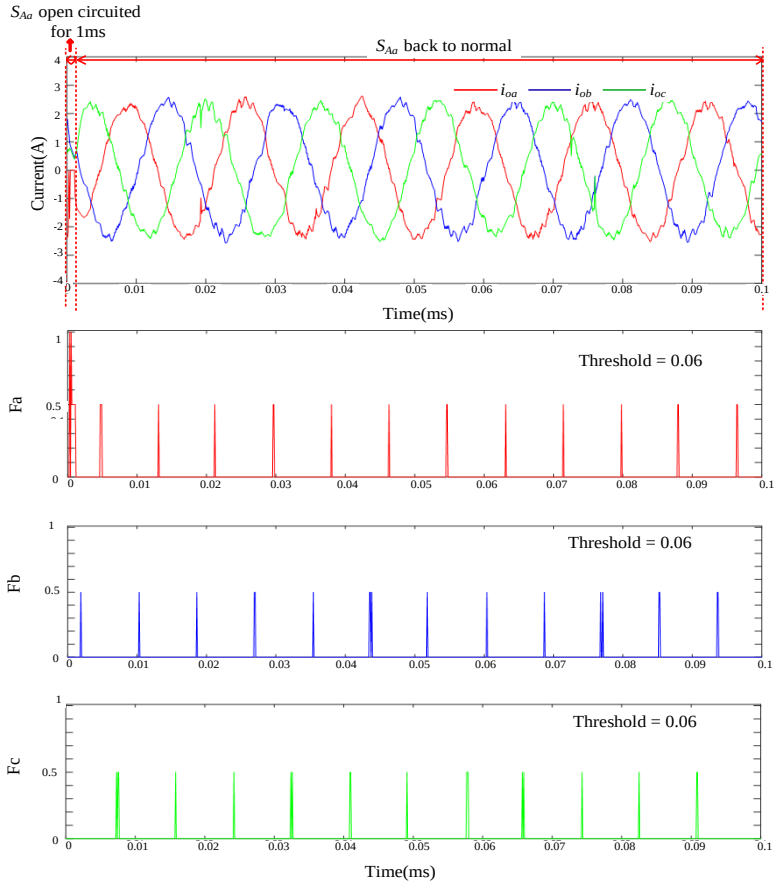


Figure 9.52: Fault diagnosis on experiment number 5, threshold value $th = 0.06$

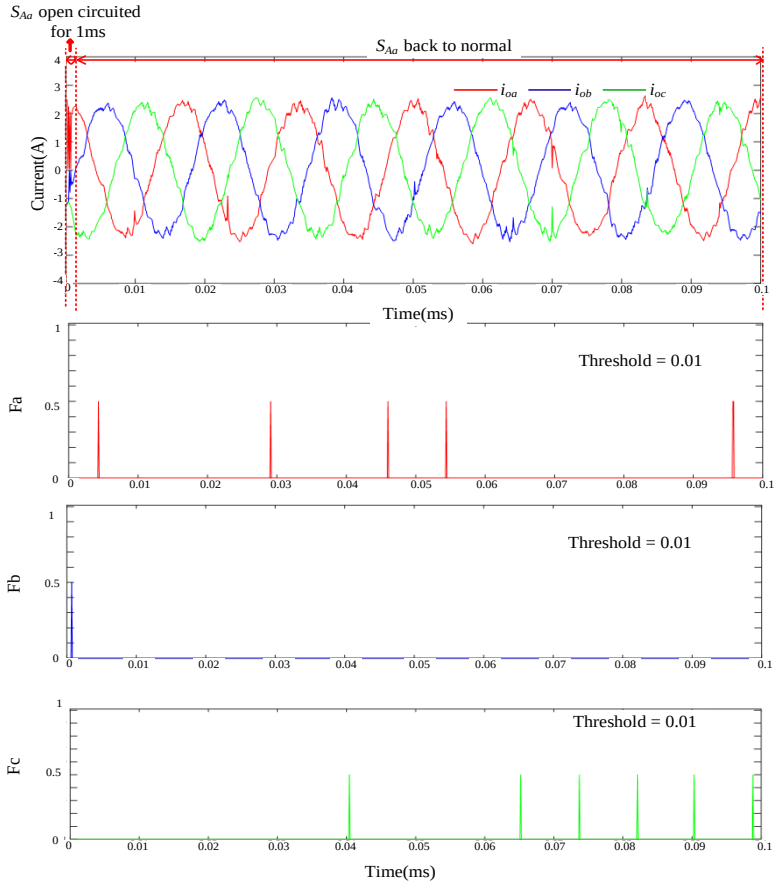


Figure 9.53: Fault diagnosis on experiment number 6, threshold value $th = 0.01$

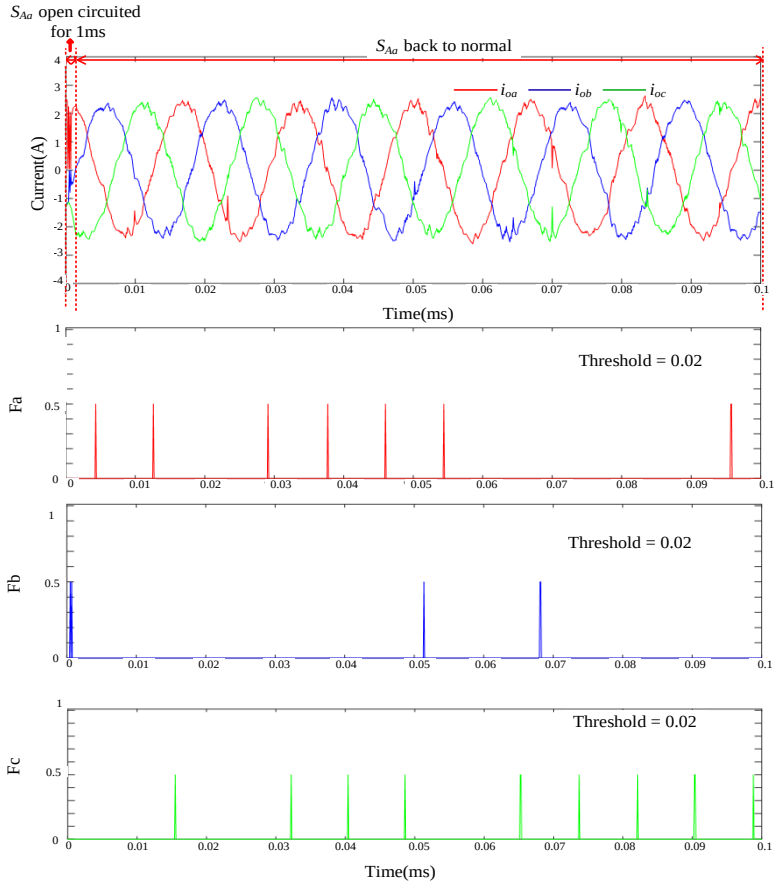


Figure 9.54: Fault diagnosis on experiment number 6, threshold value $th = 0.02$

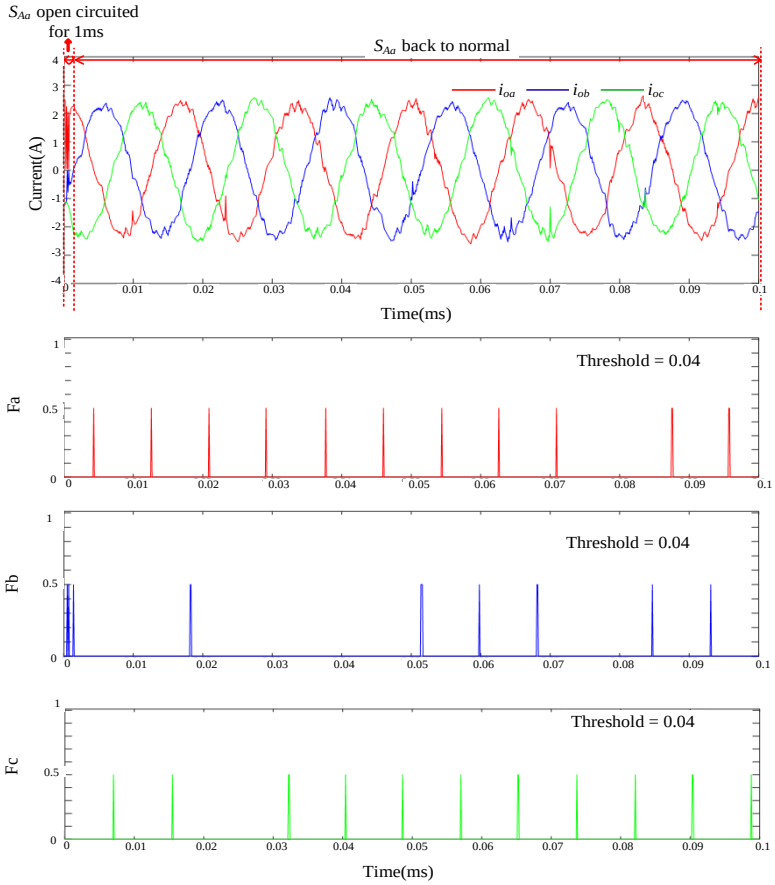


Figure 9.55: Fault diagnosis on experiment number 6, threshold value $th = 0.04$

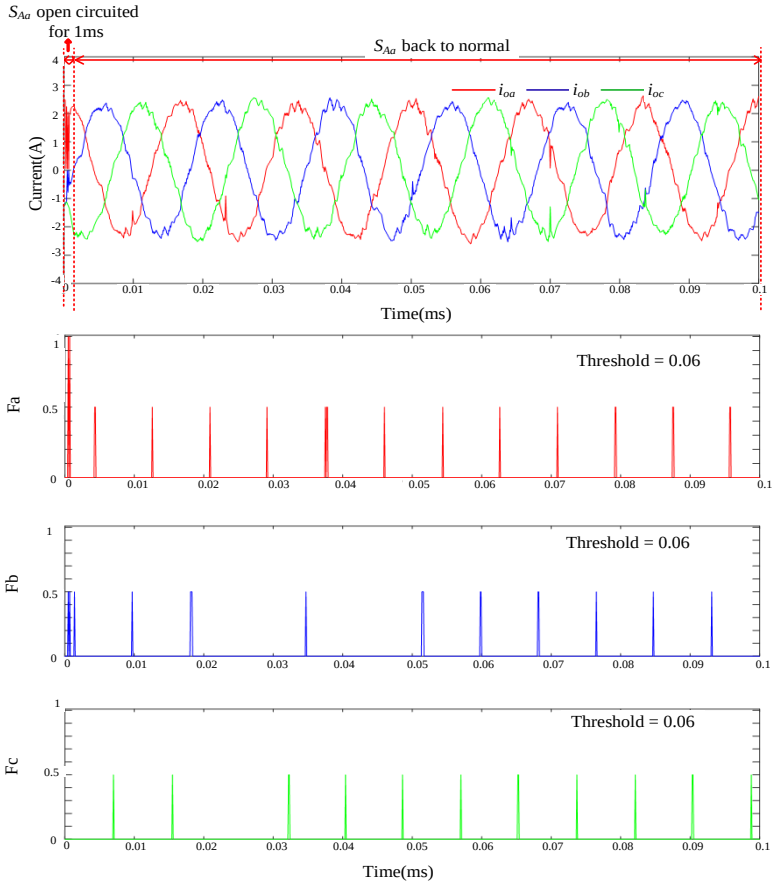


Figure 9.56: Fault diagnosis on experiment number 6, threshold value $th = 0.06$

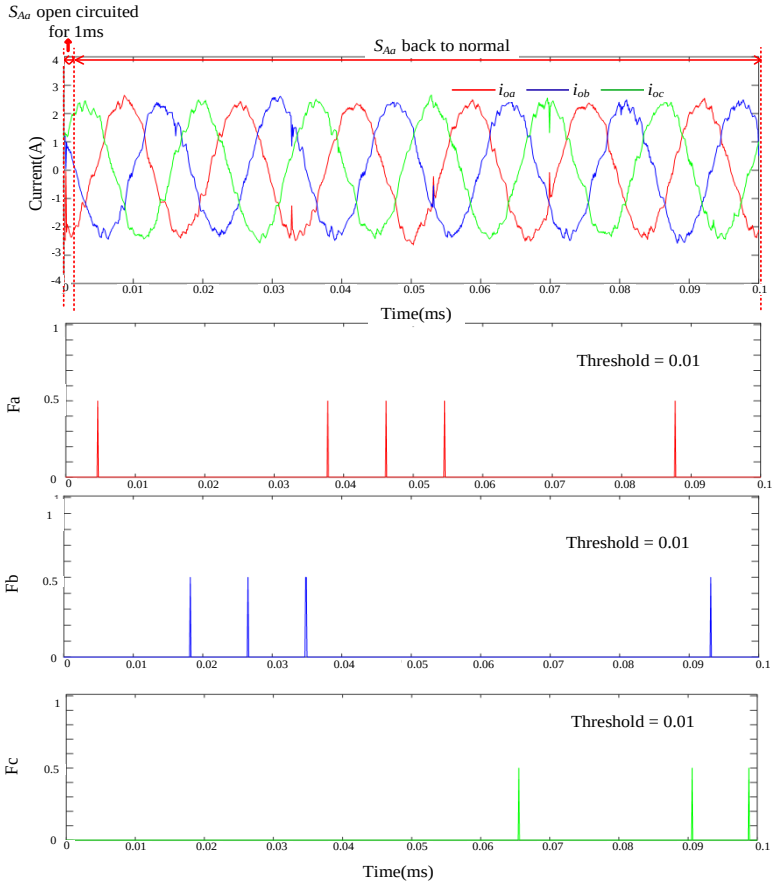


Figure 9.57: Fault diagnosis on experiment number 7, threshold value $th = 0.01$

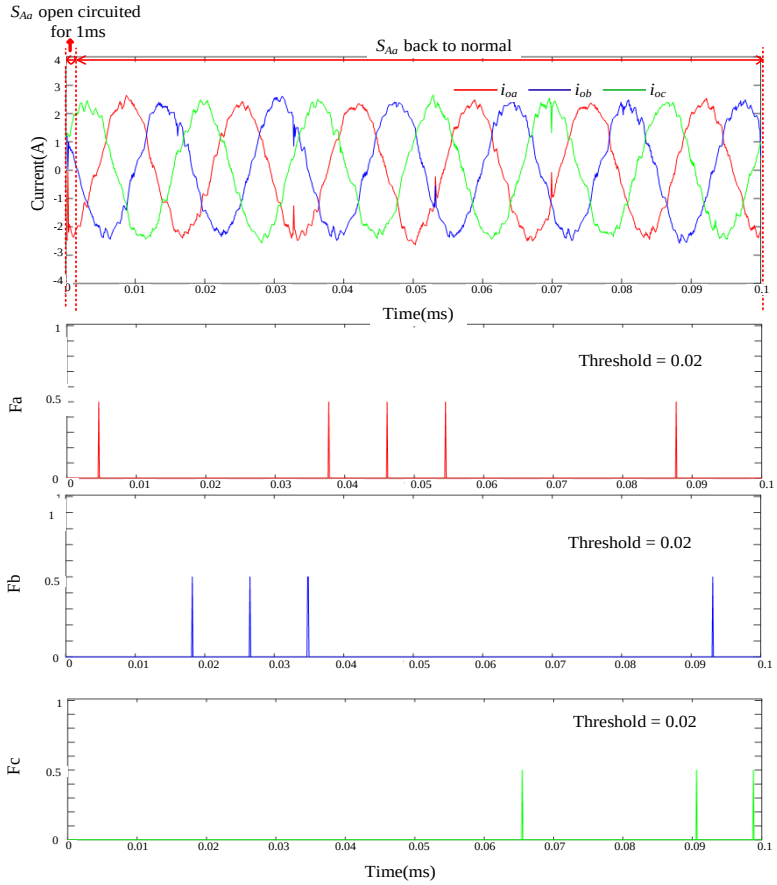


Figure 9.58: Fault diagnosis on experiment number 7, threshold value $th = 0.02$

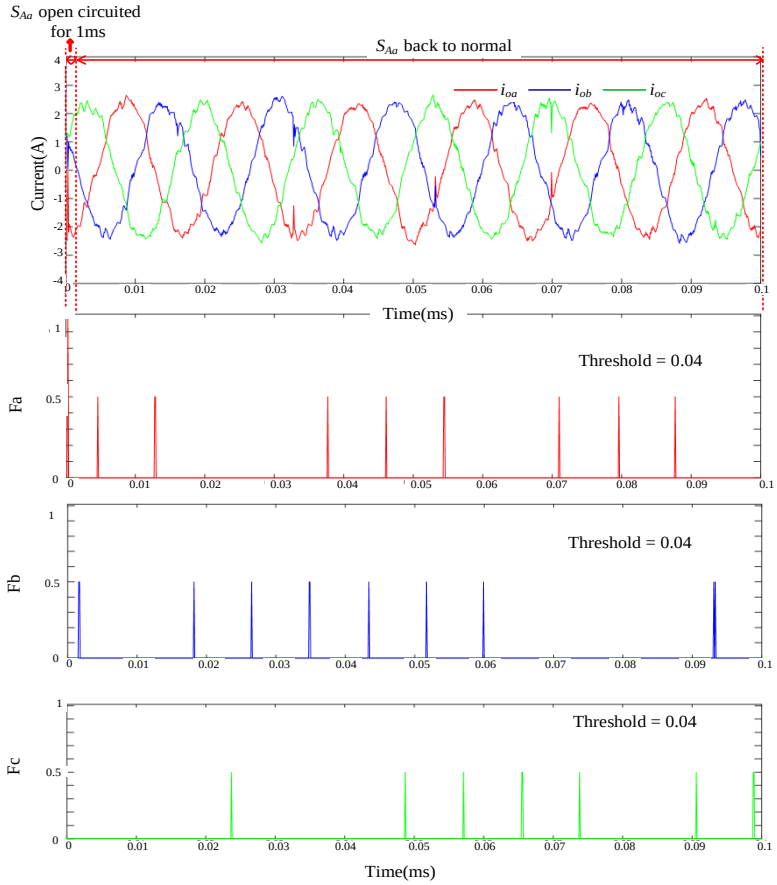


Figure 9.59: Fault diagnosis on experiment number 7, threshold value $th = 0.04$

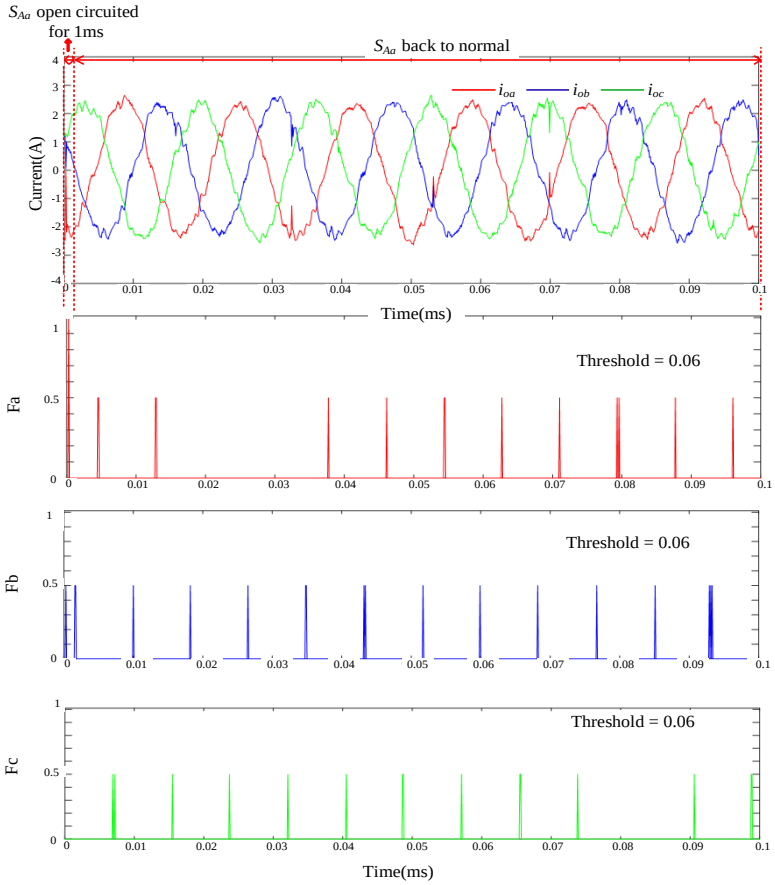


Figure 9.60: Fault diagnosis on experiment number 7, threshold value $th = 0.06$

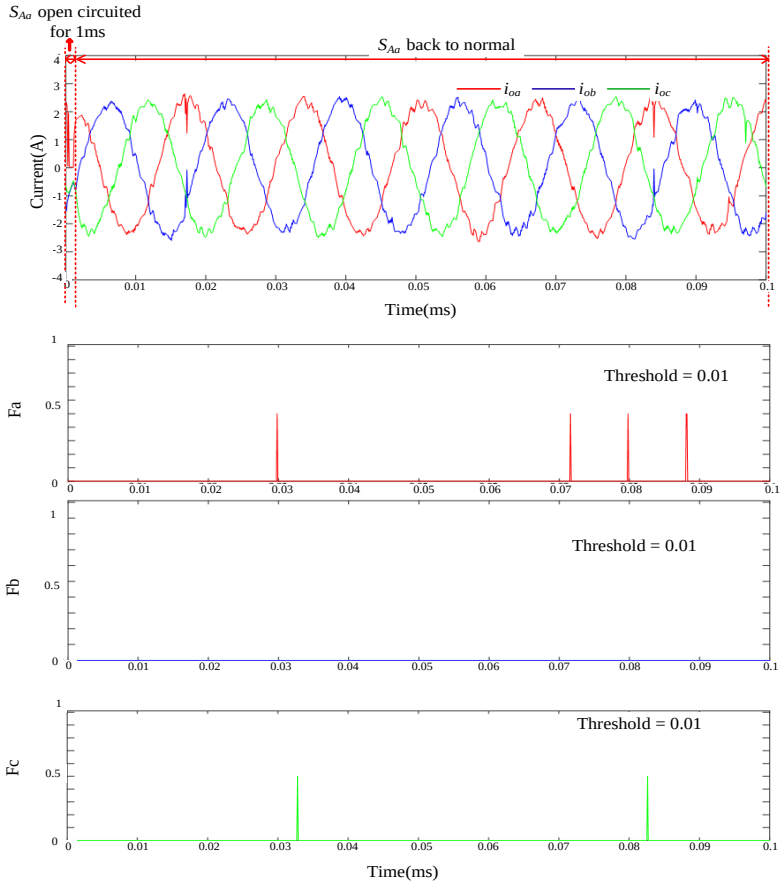


Figure 9.61: Fault diagnosis on experiment number 8, threshold value $th = 0.01$

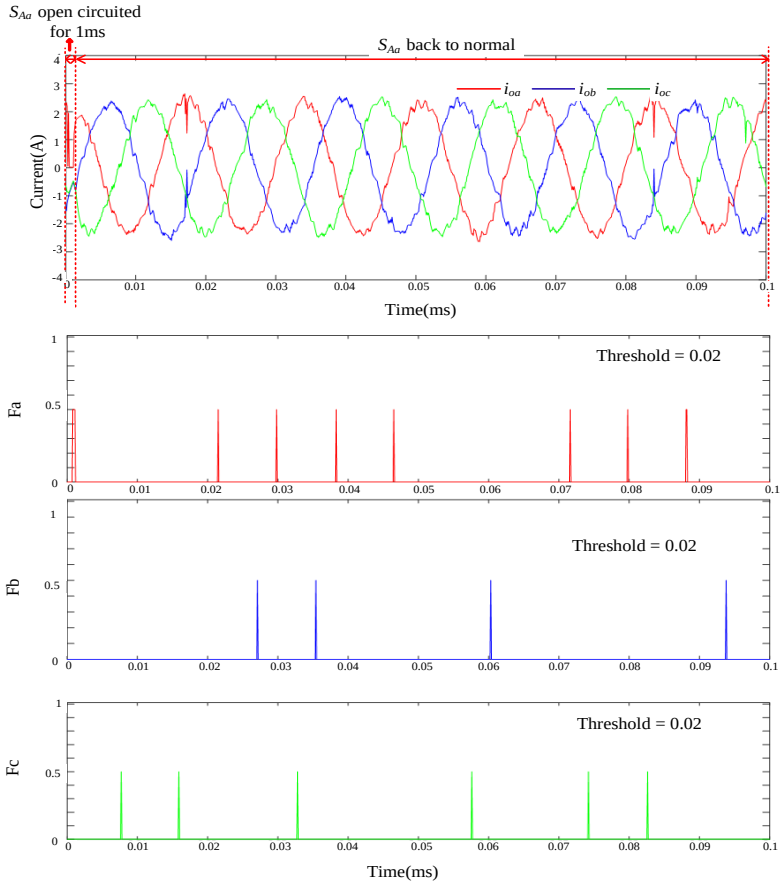


Figure 9.62: Fault diagnosis on experiment number 8, threshold value $th = 0.02$

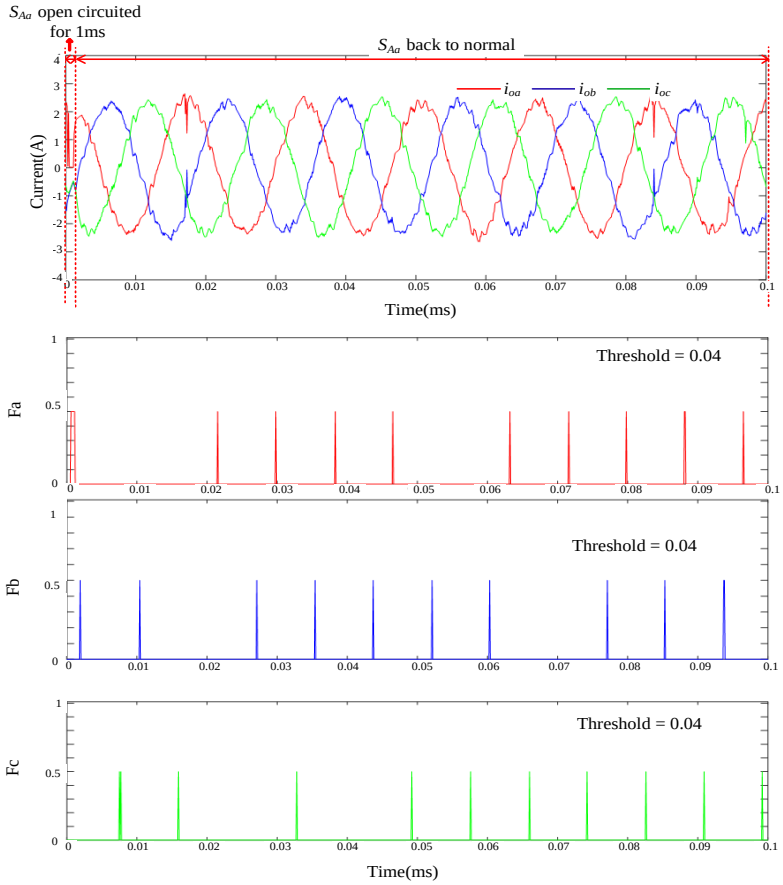


Figure 9.63: Fault diagnosis on experiment number 8, threshold value $th = 0.04$

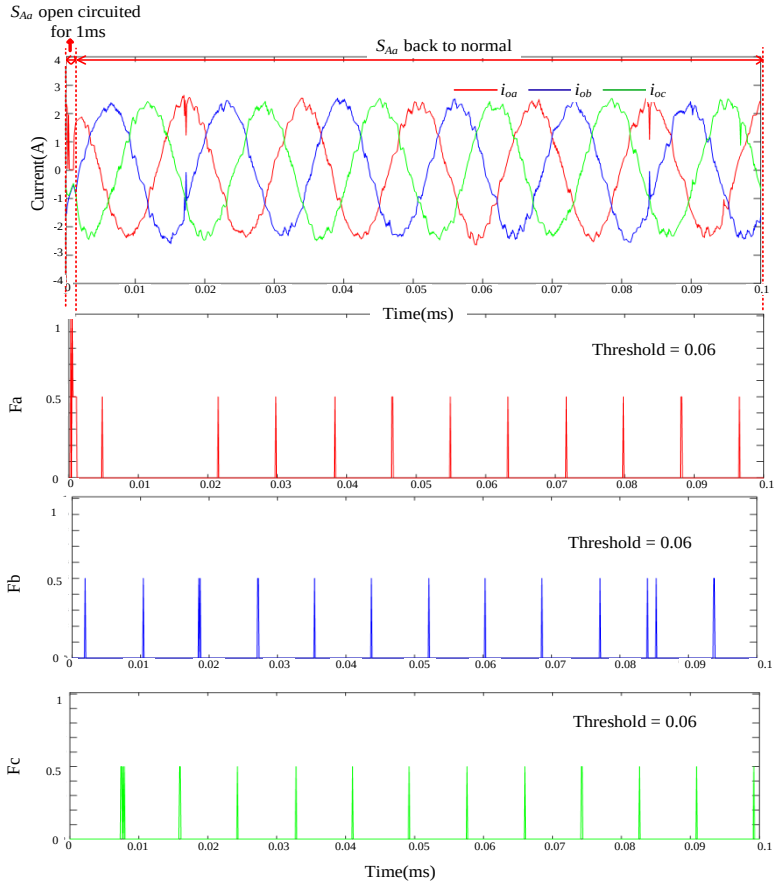


Figure 9.64: Fault diagnosis on experiment number 8, threshold value $th = 0.06$

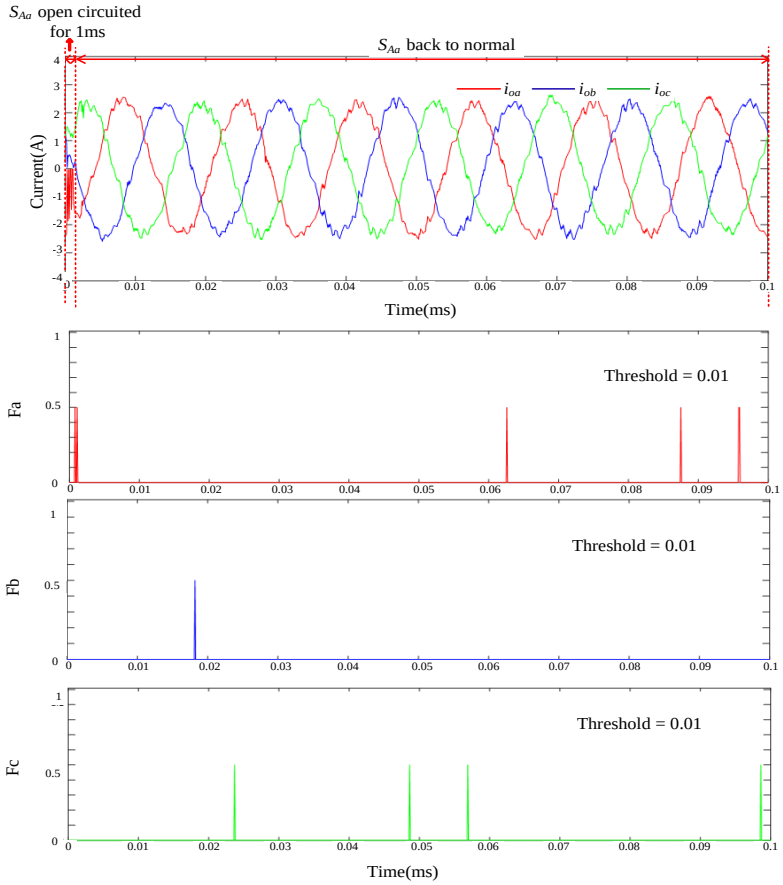


Figure 9.65: Fault diagnosis on experiment number 9, threshold value $th = 0.01$

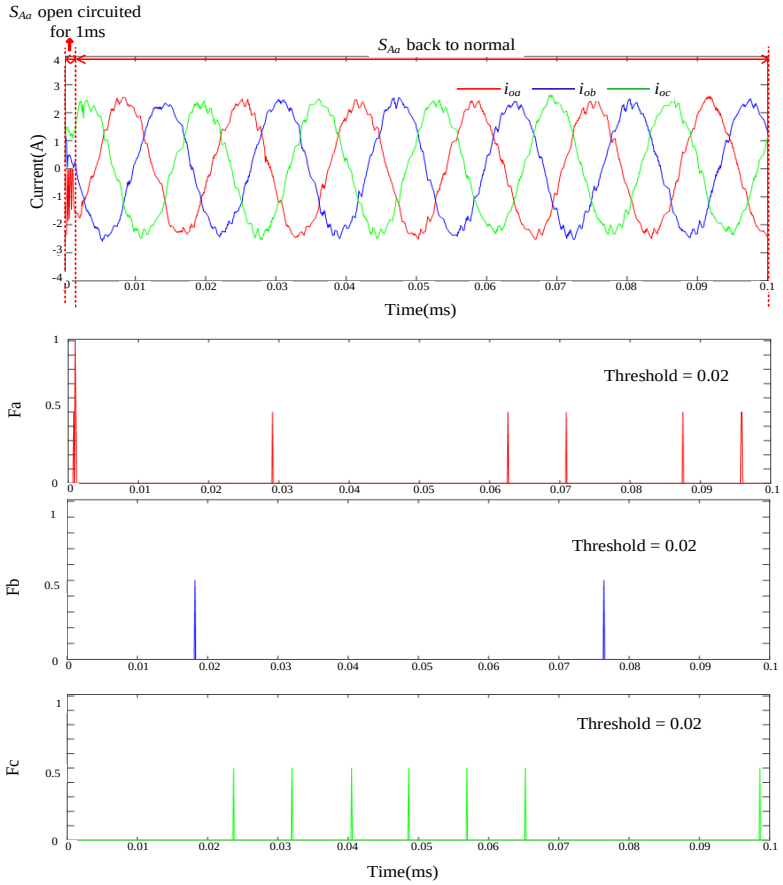


Figure 9.66: Fault diagnosis on experiment number 9, threshold value $th = 0.02$

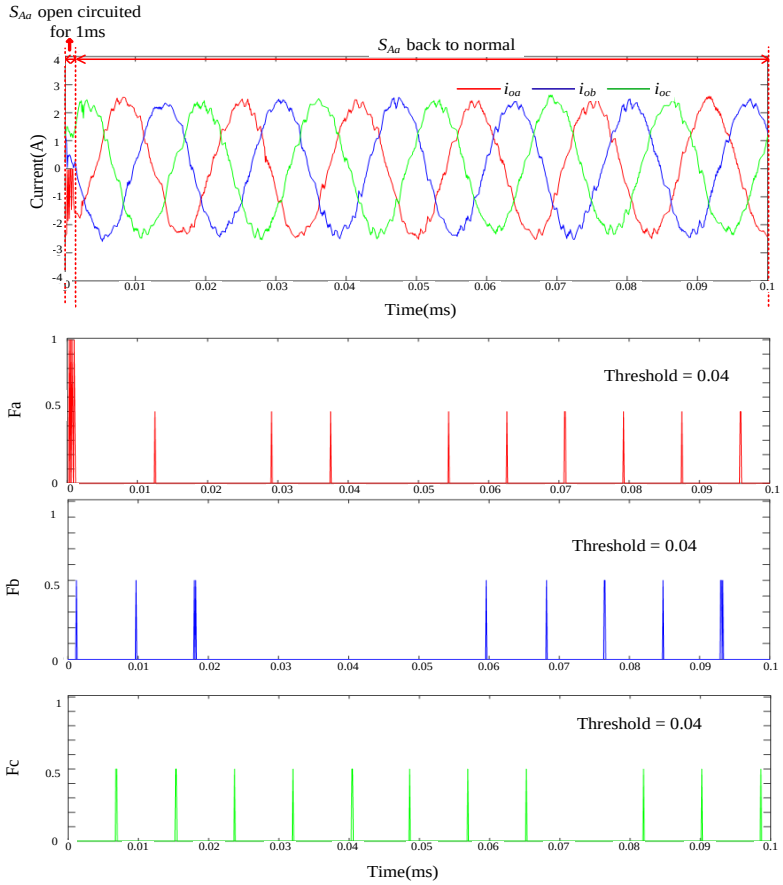


Figure 9.67: Fault diagnosis on experiment number 9, threshold value $th = 0.04$

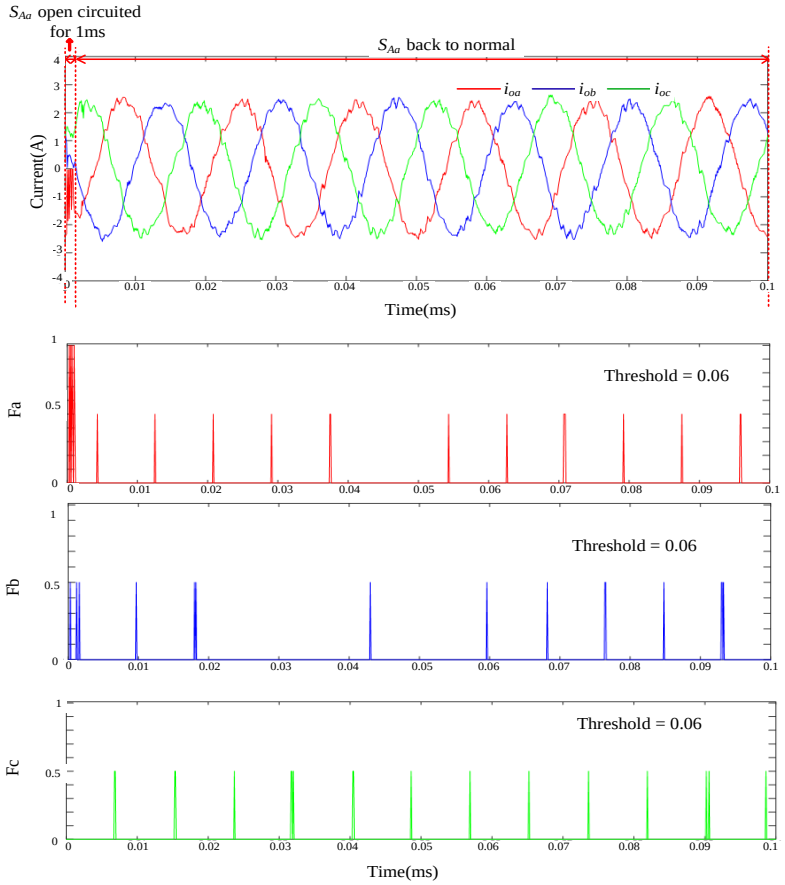


Figure 9.68: Fault diagnosis on experiment number 9, threshold value $th = 0.06$

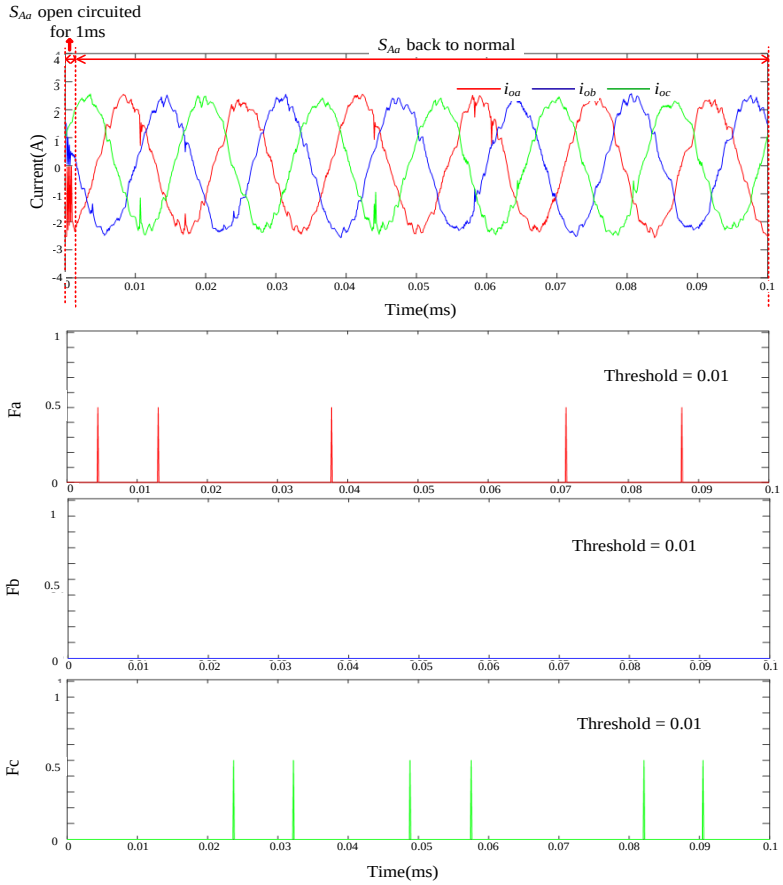


Figure 9.69: Fault diagnosis on experiment number 10, threshold value $th = 0.01$

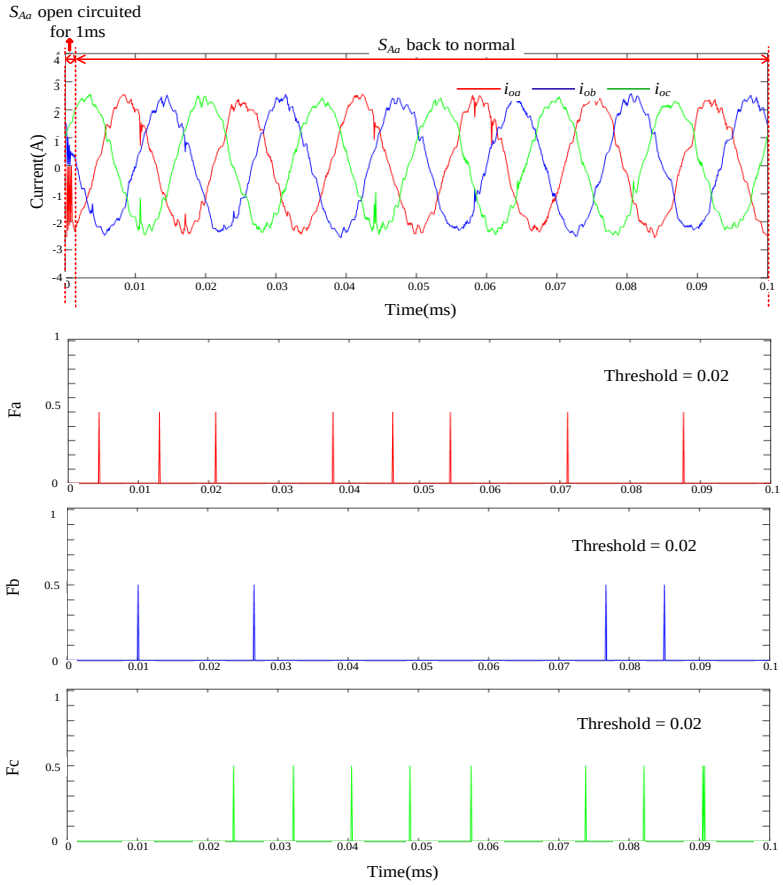


Figure 9.70: Fault diagnosis on experiment number 10, threshold value $th = 0.02$

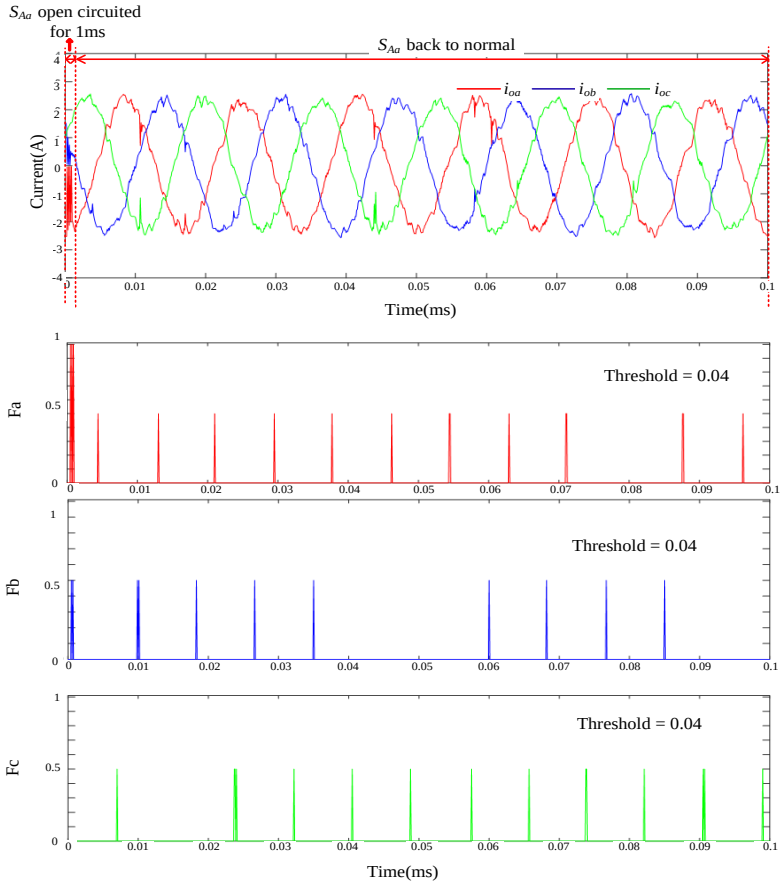


Figure 9.71: Fault diagnosis on experiment number 10, threshold value $th = 0.04$

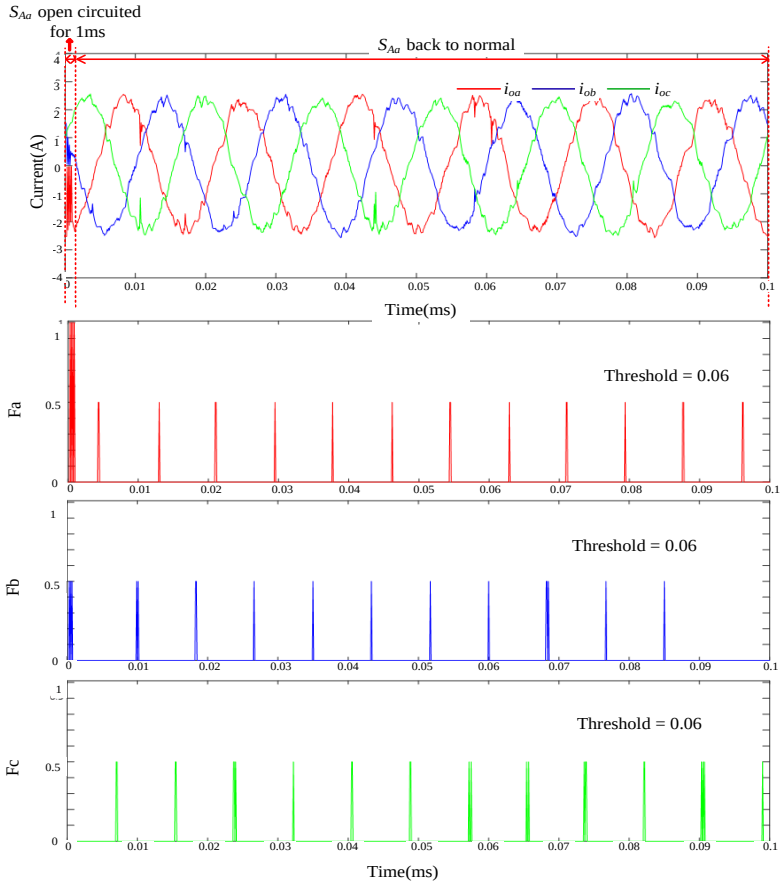


Figure 9.72: Fault diagnosis on experiment number 10, threshold value $th = 0.06$

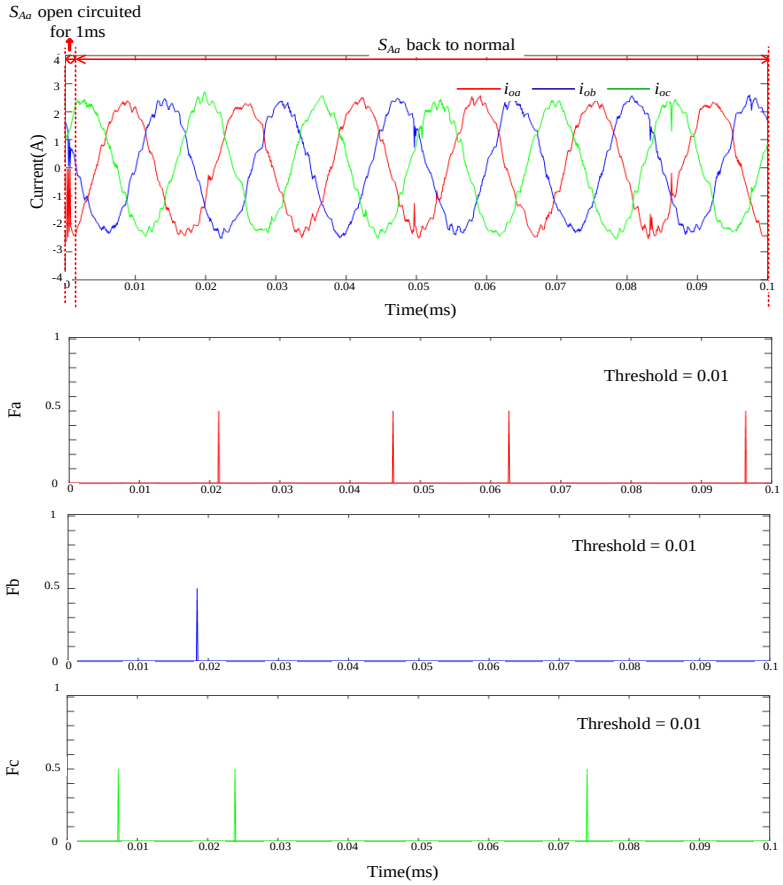


Figure 9.73: Fault diagnosis on experiment number 11, threshold value $th = 0.01$

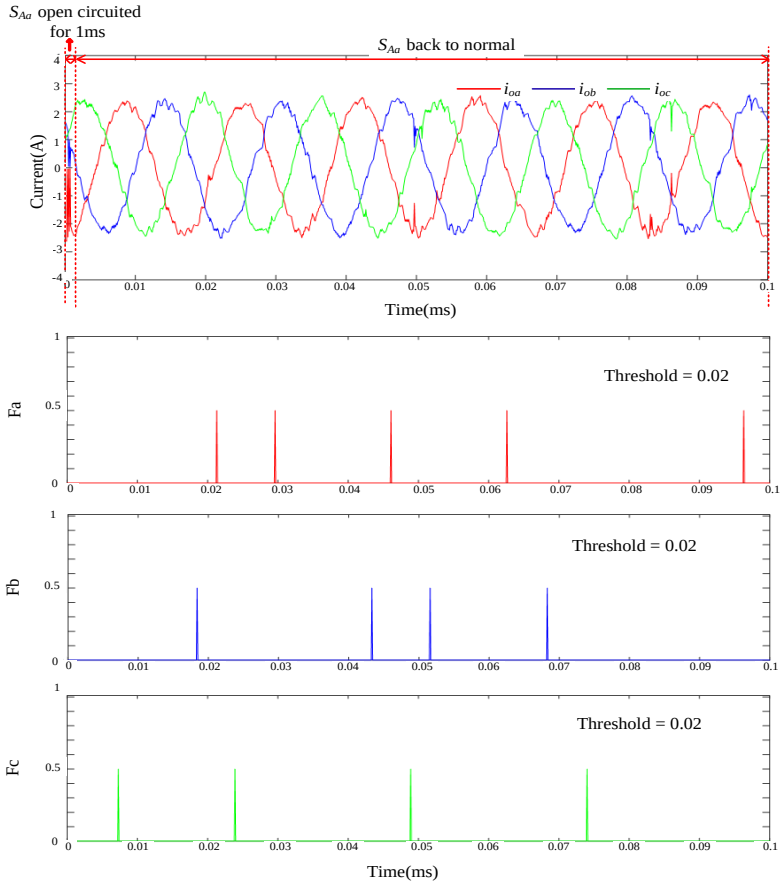


Figure 9.74: Fault diagnosis on experiment number 11, threshold value $th = 0.02$

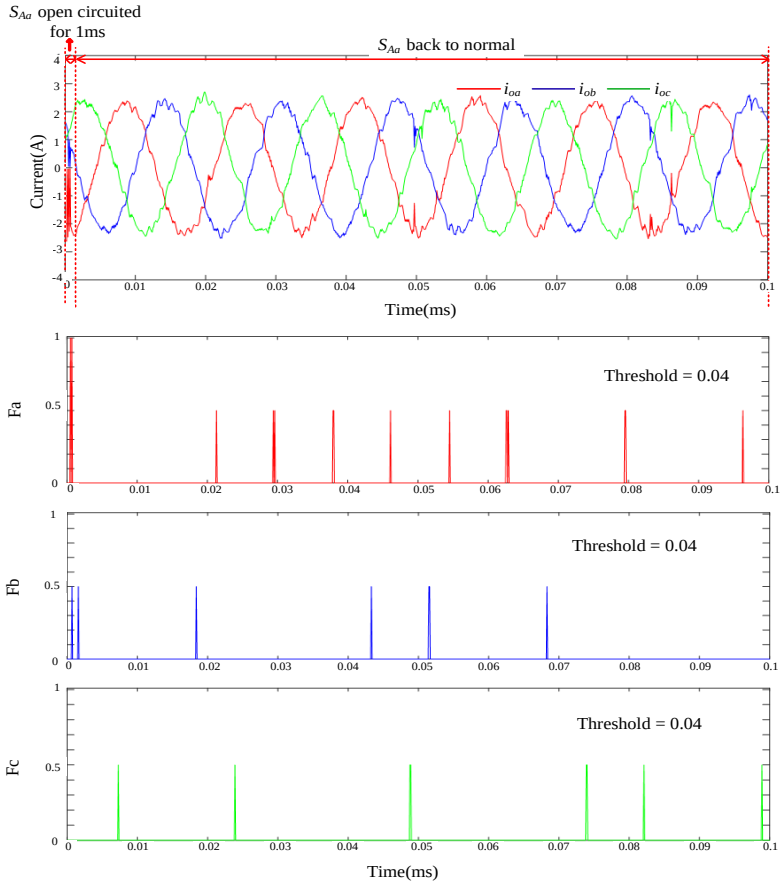


Figure 9.75: Fault diagnosis on experiment number 11, threshold value $th = 0.04$

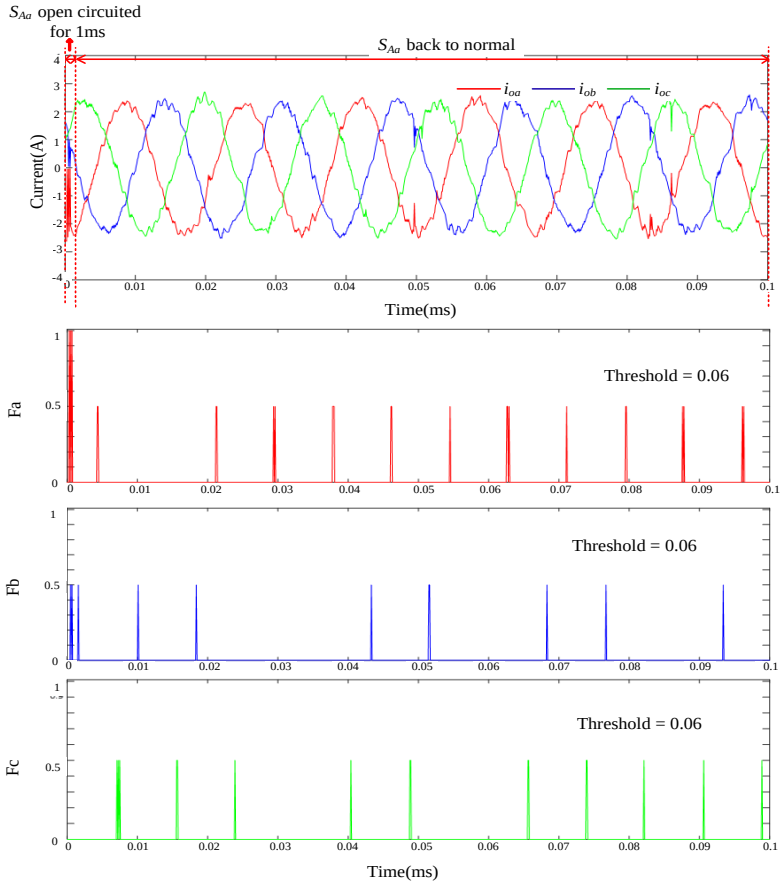


Figure 9.76: Fault diagnosis on experiment number 11, threshold value $th = 0.06$