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**INVESTIGATION OF THE ELECTRICAL AND
OPTICAL PROPERTIES OF ADVANCED
SEMICONDUCTORS MATERIALS AND
DEVICES**

by

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ABSTRACT

This thesis reports on an investigation of deep level defects in InAs quantum dots intermediate band solar cells (QD-IBSCs) and InAs/InGaAs quantum dot lasers structures that have applications in photovoltaics and optoelectronic technologies. In fact, it is of paramount importance to understand the characteristics of the defects and their influence on the quality of materials and the performance of devices. In this work, the effect of electrically active defects on the structural, optical and electrical properties of a set of intermediate band solar cells grown by Metal Organic Vapour Phase Epitaxy (MOVPE) and self-assembled InAs/InGaAs QDs based laser structures grown by Molecular Beam Epitaxy was studied using Atomic Force Microscopy, Transmission Electron Microscopy, Photoluminescence, current-voltage (I-V), capacitance-voltage (C-V), deep level transient spectroscopy (DLTS), and Laplace DLTS (LDLTS) techniques. In addition, the effect of Gamma irradiation on the properties of laser structures was also investigated.

Electrically active defects present in a set of p-i-n InAs/GaAs QD-IBSCs grown by MOVPE on GaAs substrates have been studied systematically. The device's structures are almost identical, differing only in the growth temperature and thickness of the GaAs layers that cover each InAs QD layer. In order to distinguish between the roles played by the growth temperature and the insertion of the QDs in the active region of the devices, reference solar cells with the equivalent temperature growth sequence as the ones used for the fabrication of the QD-IBSCs were grown and their DLTS results were compared. These differences induce significant changes in the solar energy conversion efficiency of the photovoltaic cells. DLTS and Laplace DLTS measurements on control samples and the studied

solar cell devices have clearly shown that electrically active traps play an important role in the device figures of merit, such as open circuit voltage, short circuit current, and shunt resistance. In particular, it was found that the well-known EL2 defect negatively affects both the open circuit voltage and shunt resistance, more in structures containing QDs, as a consequence of the temperature cycle required to deposit them. Other unidentified defects, that are absent in samples in which the QDs were annealed at 700 °C, contribute to a reduction of the short circuit current, as they increase the Shockley-Read-Hall recombination.

Extensive work on InAs QDs grown on GaAs substrates has been reported in the literature, however, research in the use of different substrate materials such as silicon to achieve an ideal and full integration of photonic and electronic systems is still under development. In this work we have investigated the effect of the substrate material (Si and GaAs) and strain reducing layer (SRL) on the electrical and optical properties of InAs QDs based laser structures grown by MBE. Two InAs QD laser structures with similar active regions grown on GaAs and Si substrates using SRL consisting of InAs QDs/6nm $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ SRL have been investigated. Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM), photoluminescence (PL), I-V, C-V, DLTS and LDLTS have been used for the characterization of the grown samples. The formation of fairly similar QDs in both structures was evidenced, with higher strain for QDs in the sample grown on a Si substrate. A red shift of the InAs QD PL peak energy was observed for the sample grown on a Si substrate as compared to the sample grown on a GaAs substrate, which was associated with residual biaxial strain from the Si/GaAs heterointerface. This red-shift of the PL peak energy is accompanied by a broadening of the PL spectrum from ~31 meV to a value of ~46 meV. This

broadening is attributed to the QD size inhomogeneity increase for samples grown on a Si substrate. DLTS and LDLS showed that InAs QD laser devices grown on Si substrate showed more defects than the structures grown on GaAs substrates, suggesting that QDs/GaAs lasers should have better properties than QDs/Si lasers. However, the use of Si substrates to grow InAs QDs' based lasers opens up new possibilities for controlling the density and size of QDs, and therefore the emission of InAs QDs, for photonic devices integration using Si substrates when using specific type of SRL/substrate.

A significant number of lattice defects are produced in semiconductors as a result of radiation in space, which reduce the devices' performance. The effect of gamma irradiation on the electrical properties of InAs QD lasers grown on GaAs and Si substrates was studied. The number of traps either decreased, remained the same or new defects were created after irradiation. Moreover, the DLTS and Laplace DLTS have been able to reveal a close connection between the grown-in defects and those induced by radiation.

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- Investigation of Electrically Active Defects in InAs Quantum Dots Intermediate Band Solar Cell Using Deep Level Transient Spectroscopy Technique - 19th International Conference on Extended Defect in Semiconductors 2018 (EDS2018) 24-29 June , 2018, Thessaloniki, Greece.

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CHAPTER 1: INTRODUCTION

1.1 INTRODUCTION

Semiconductors are currently used in a wide variety of electronic and photonics technologies, such as computers (CPUs, memories), lasers, solar cells, light emitting diodes (LEDs), optical fibres, optical storage media (CDs, DVDs) and so forth [1, 2]. Hence, this diversity in the electronic and optoelectronic devices has led to semiconductors becoming an important subject for researchers. As early as 1833, Michael Faraday studied the temperature dependence of the electrical conductivity of silver sulphide (Ag_2S). He found that the resistance of Ag_2S decreased dramatically as the temperature increased. This was the first study on semiconductors [3].

The invention of the transistor led to a revolution in semiconductor technology, which has profoundly altered the electronic and optoelectronic industries [4]. The first transistor was made by Shockley, Bardeen, and Brattain in 1947 at Bell laboratories [5] using germanium (Ge). This was followed by another important development in semiconductors in 1958 by J. Kilby who invented the first integrated circuit (IC) which was based on silicon (Si), one of the most studied semiconductor material [4, 5]. Soon thereafter, gallium arsenide (GaAs) was discovered and became one of the most widely used compound semiconductors in devices such as infrared emitting diodes, laser diodes, integrated circuits at microwave frequencies, and photovoltaic cells. This is because some electronic properties of GaAs are superior to those of Si. GaAs (1.42 eV) has a larger energy gap than Si (1.12 eV), and therefore GaAs offers a wider range of operating temperatures and much higher radiation hardness, which is a significant advantage

for example in space applications. Another major advantage is that GaAs has a direct forbidden energy gap, which makes it more useful for optoelectronic devices as it emits light more effectively than Si, whose bandgap is indirect. In addition, GaAs has a high electron mobility and a high saturated electron velocity compared to Si, allowing transistors made of GaAs to operate at high frequencies (> 250 GHz). However, Si has major advantages over GaAs for integrated circuit manufacturing technologies: (i) Si is abundant and relatively low in costs due to well established processing techniques, (ii) Si has a native SiO_2 , which is one of the best insulators and can easily be incorporated onto silicon circuits, (iii) Si has greater physical strength than GaAs which enables the production of larger wafers (12" (~ 300 mm) compared to 8" (~ 150 mm) diameter for GaAs), (iv) Si has a higher hole mobility which allows the fabrication of higher-speed P-channel field effect transistors that are required for CMOS (complementary metal–oxide–semiconductor) logic.

In general, materials based on III-V compound semiconductors offer excellent properties for high-performance electronic and optoelectronic devices [6, 7].

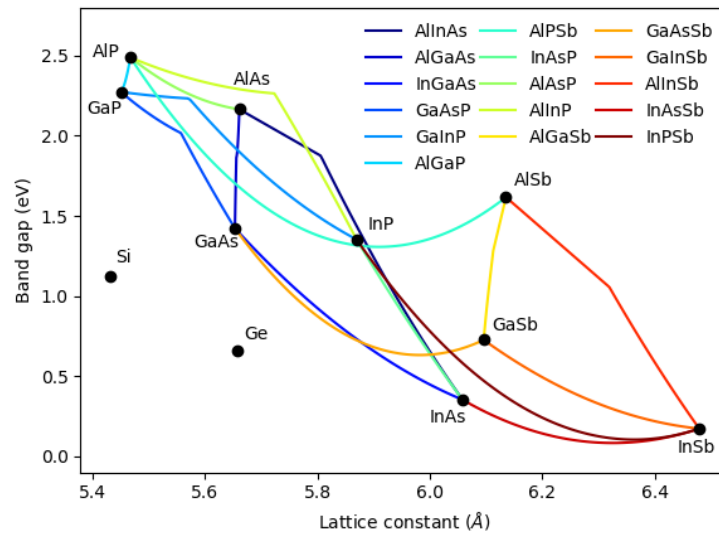


Figure 1.1: Bandgaps of selected semiconductors as a function of lattice constant [12].

There are several optoelectronic applications that depend on GaAs materials, one of which is GaAs-based solar cells for space applications, and therefore it has become vital to improve their performances further. One approach to enhance the efficiency of solar cells is to use semiconductor nanostructures, for example, InAs quantum dots (QDs) to implement what are called GaAs-based intermediate band solar cells (IBSC) [8]. Luque et al (1997) introduced a novel photovoltaic concept, the intermediate band solar cell (IBSC). This was created to exceed single gap solar cell performance [9-11]. The principal function of these cells is to introduce electronic bands of one or more energy levels (known as intermediate bands) within the main bandgap of a conventional semiconductor. The introduction of these additional energy bands using these nanostructures allows more absorption. This in turn results in an increase of the short circuit current. Figure 1.1 shows the bandgaps of the most common semiconductors with their lattice constants.

On the other hand, a variety of optoelectronic applications rely on self-assembled QDs such as lasers, photodetectors, amplifiers, and solar cells [13-15]. Since InAs QDs have the potential to emit light across the communication wavelength bands [16-18] they have attracted extensive research attention among QD systems. It should be pointed out that InAs/GaAs-based QD lasers operate at 1.3 μm , an attractive alternative to InP-based QW lasers that require more expensive InP substrates and suffer from poor temperature stability [19, 20].

The reported results on InAs/GaAs quantum dot lasers epitaxially grown on silicon substrates seem to support the hypothesis that quantum dots are less sensitive to dislocations than quantum wells [21-23]. In order to improve the quality of electrical and optical properties of InAs QDs grown on both GaAs and Si substrates, new avenues in research have concentrated on studying suitable capping layer

(CL) and/or strain reducing layer (SRL) materials for covering InAs QDs grown on both GaAs and Si substrates.

One of the most important feature that makes semiconductors widely used is doping, which involves changing the electronic and photonic properties of semiconductors by adding small amounts of impurities [24]. By changing the doping concentration, the electrical and optical properties of devices can be changed. In addition to intentional incorporation of impurities into the lattice of semiconductors, some undesired defects may occur, usually deep in the band gap (termed deep-level defects) [24]. These defects adversely affect the performance of a device, and therefore it is important to study their properties such as activation energy, capture cross-section and trap concentration. Deep Level Transient Spectroscopy (DLTS) [25], a powerful electrical technique, is used to investigate the electrically active defects and determine their parameters.

The study described in this thesis relates to the characterization of a range of different semiconductor materials systems namely InAs Quantum Dots intermediate band solar cell (IBSC), and InAs/InGaAs QD lasers which can be used in different applications such as photovoltaic devices and nanoelectronic technology. Ideally, the characteristics of the defects present in the materials should be carefully determined for such applications; this will help in understanding how they affect the quality of the material and the performance of the devices.

1.2 MOTIVATION

Electrically active defects play a significant role in electronic and optoelectronic devices. The main motivation of this thesis is to investigate the presence of

electrically active defects in InAs/GaAs QD IBSCs using Current - Voltage (J-V), Capacitance - Voltage (C-V), conventional Deep Level Transient Spectroscopy (DLTS) and Laplace DLTS (LDLTS) measurements. In order to distinguish between the roles played by the growth temperature and the insertion of the QDs in the active region of the investigated devices, reference solar cells with the equivalent temperature growth sequence as the ones used for the fabrication of the QD-IBSCs were grown and their DLTS results were compared.

In addition, the same methods are used to investigate the effect of the substrate material on the structural, optical and electrical (especially the electrically active defects) properties of InAs QDs based laser structures. Two InAs QD laser structures with similar active regions grown on GaAs and Si substrates using strain reducing layer (SRL) consisting of GaAs/InGaAs have been investigated. Moreover, the effect of gamma (γ -) irradiation on the electrical properties of InAs/InGaAs QD lasers grown on GaAs and Si substrates using Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM), Photoluminescence (PL), I-V, C-V DLTS and LDLTS measurements.

1.3 SCHEME OF THE THESIS

This thesis is arranged as follows:

Chapter 1 presents the research motivations and structure of the thesis.

Chapter 2 gives a description of the basic concepts of semiconductors, crystal structure, the principles of heterostructure devices and quantum confinement. The properties of GaAs, InAs, InGaAs, AlAs, AlGaAs and Si materials are covered in this chapter.

Chapter 3 provides information on the crystal defects and theoretical background of carrier kinetics.

Chapter 4 describes the experimental techniques used in this thesis including current-voltage (I-V), capacitance-voltage (C-V), DLTS, Laplace DLTS and Photoluminescence (PL). The hardware and software required to implement these methods are also presented.

Chapter 5 lists the samples used in this thesis and briefly presents the details of the measurements set up.

Chapter 6 investigates the electrically active defects in InAs Quantum Dots intermediate band solar cell (IBSC) grown by Metal-Organic Chemical Vapor Deposition (MOCVD) using DLTS.

Chapter 7 presents the electrical and optical properties of self-assembled InAs quantum dots lasers grown on gallium arsenide and silicon substrates by Molecular Beam Epitaxy (MBE)

Chapter 8 describes the effects of gamma (γ -) radiation on the electrical properties of InAs/InGaAs quantum dots lasers grown on GaAs and Si substrates by MBE.

Chapter 9 includes overall conclusions of the research work carried out in this thesis and offers suggestions for future work.

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CHAPTER 2: FUNDAMENTAL CONCEPTS OF SEMICONDUCTORS

This chapter discusses some of the fundamental properties of semiconductors such as crystal structures, energy gaps, direct and indirect energy gaps, temperature dependent energy gaps, quantum confinement, density of states, heterostructures, lattice mismatch, atom size, electronegativity and band alignments. Additionally, some of the important properties of GaAs, AlGaAs, InAs, InGaAs and Si are also described.

2.1 SEMICONDUCTORS

In recent years, the key important materials to current electronic technology are semiconductors. These are used in devices such as computers, CD/DVD lasers and in the basic components of optical fiber communication, high efficiency solar cells, general lighting LED displays and so on. Therefore, a great deal of research has been undertaken in the field of semiconductors [[1](#), [2](#)].

The electrical conductivity of semiconductor materials lies between insulators and conductors' materials. These materials have an electrical resistivity in the range of 10^{-2} to $10^9 \Omega \cdot \text{cm}$.

The elementary and compound semiconductors are two classes of semiconductor materials. An elementary semiconductor consists of a single element from the periodic table, such as Silicon (Si) and Germanium (Ge). These are from group IV. A compound semiconductor is made of two or more elements from the periodic

table. For example, binary and ternary compounds are made of two (GaAs) and three (InGaAs) elements, respectively [3].

2.1.1 UNDOPED AND DOPED SEMICONDUCTORS

Another way to classify semiconductor materials is by their doping type. If these materials are pure without any doping, they are called intrinsic or undoped semiconductor. They can be either elemental or compound semiconductors. In intrinsic semiconductors, the number of electrons in the conduction band is equal to the number of holes in the valence band. Additionally, intrinsic semiconductors behave as insulators at a temperature of 0 K because the valence band is completely filled and the conduction band is completely empty and, therefore, there are no free charge carriers.

One of the most important features that make semiconductors widely used is doping, which involves adding small amounts of impurities into the host semiconductor material. This results in a change of their electronic and photonic properties [4]. A doped semiconductor is also called an extrinsic semiconductor.

A semiconductor is considered n-type once it has been doped in such a way that makes electrons the majority carriers. However, if the holes are majority carriers, the semiconductors are called p-type. For example, if an elemental semiconductor from group IV (Si) is doped with an element from group V (As), it becomes an n-type semiconductor. The result of this process is that bonds are formed between four electrons in As and the surrounding silicon atoms leaving one electron from As free for n-type conduction. Similarly, if boron, a trivalent impurity material (group III in the periodic table), is added to pure Si, the three valence electrons of the boron atom form covalent bonds with four surrounding Si atoms. This leaves

one hole free for p-type conduction.-When an excess number of holes are produced by the dopant atoms, a p-type semiconductor is created. The impurity atoms providing excess electrons (n-type) and holes (p-type) are called donors and acceptors, respectively [3, 5].

2.2 CRYSTAL STRUCTURES AND PROPERTIES

The crystal structure, which is dependent on how the atoms are arranged, plays a crucial role in the performance of semiconductor devices.

2.2.1 CRYSTAL STRUCTURES

Perfect crystal structures comprise a unit cell, incorporating a collection of atoms whose arrangement is repeated periodically and infinitely. There are many different crystal structures. Figure 2.1 shows examples of such structures, including the face-centred cubic (fcc), the body-centred cubic (bcc), and the simple cubic (sc). The simplest crystal structure is the cubic lattice, where the atoms are situated at every corner of a cube (Figure 2.1 (a)). A body-centred cubic lattice (Figure 2.1 (b)) has the same arrangement of atoms on every corner of the cube, with a single atom at the cube's centre. Figure 2.1 (c) shows a face-centred cubic lattice, where there is an atom on each of the cube's faces, in the centre, as well as atoms on every corner [6].

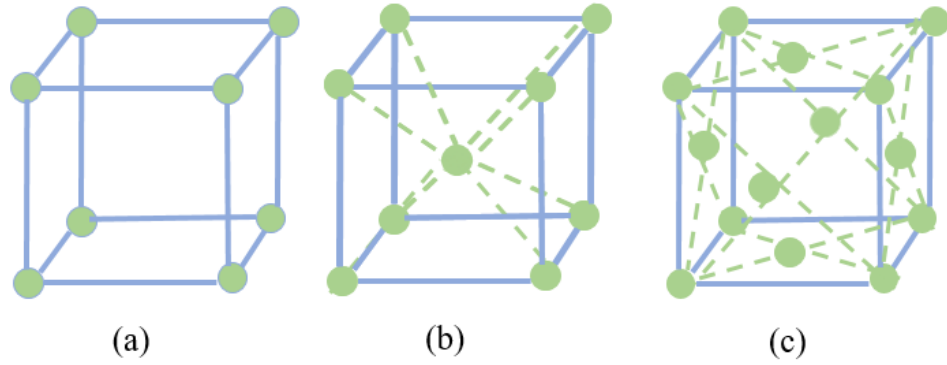


Figure 2.1: Unit cell of (a) simple cubic, (b) body-centred cubic and (c) face-centred cubic

For semiconductors, the diamond (Figure 2.2 (a)) and zincblende structures (Figure 2.2 (b)) are the other most significant forms of crystal structure. All the atoms of such structures possess covalent bonds with the four adjacent atoms in a regular tetrahedron and may be regarded as pairs of inter-penetrating fcc lattices. Every site in these diamond structures contains identical types of atoms. However, in zincblende, each site contains two forms of atoms. Examples of diamond and zincblende structured semiconductors are Si and Ge, and GaAs and InAs, respectively [3].

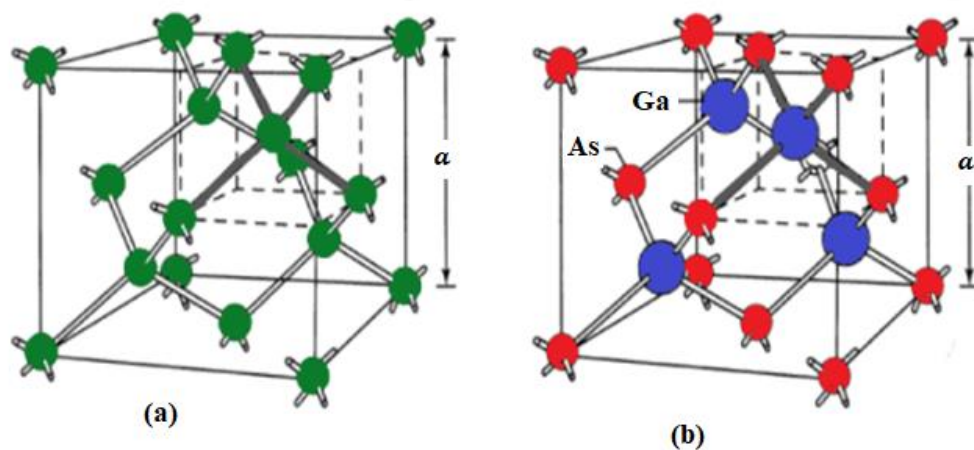


Figure 2.2: (a) Diamond structure for Si. (b) Diamond structure for GaAs.

To fabricate semiconductor devices, it is necessary to know the semiconductor crystal orientation and its surface properties. Generally, information about a semiconductor crystal's orientation is provided by Miller indices of a plane, which are determined by using three primitive basis vectors $\mathbf{a}$, $\mathbf{b}$, and $\mathbf{c}$ to describe the crystalline solid along the $(\mathbf{x}, \mathbf{y}, \mathbf{z})$ orientations [4].

An example of a plane having Miller indices (3,2,2) is shown in Figure 2.3.

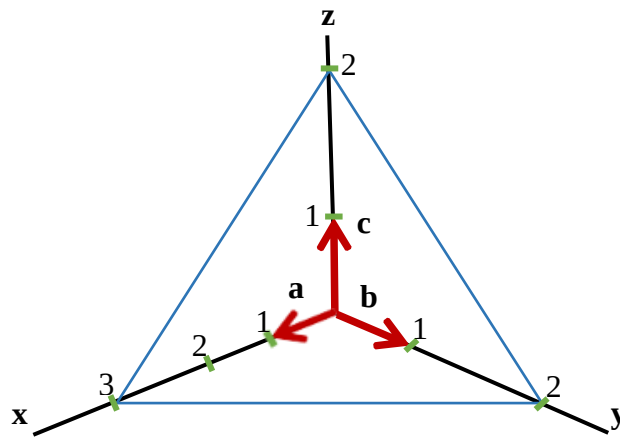


Figure 2.3: Illustration of a plane having Miller indices (3,2,2)

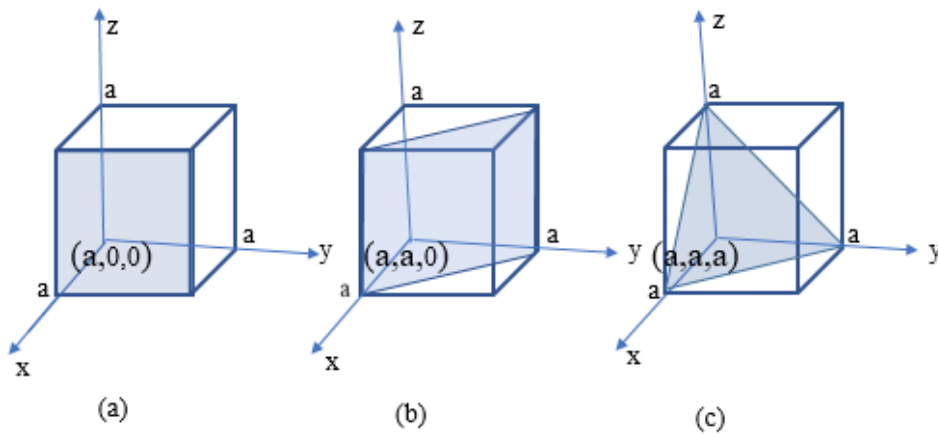


Figure. 2.4: Illustration of crystal planes (a) (100) plane, (b) (110) plane, and (c) (111) planes in a cubic crystal.

Figure 2.4 illustrates Miller indices of some planes in a cubic crystal. The direction of any general vector $\mathbf{R}$ can be expressed in terms of set of indices h, k, l . The directions and planes of the crystals can be presented by using the following symbols:

1. $[hkl]$ represents a direction.
2. $\langle hkl \rangle$ represents a family of directions.
3. (hkl) represents a plane.
4. $\{hkl\}$ represents a family of planes.

The crystalline solid, along the $\mathbf{x}$, $\mathbf{y}$ and $\mathbf{z}$ directions, is described by three primitive basis vectors ($\mathbf{a}$, $\mathbf{b}$ and $\mathbf{c}$).

At any given position of vector $\mathbf{R}$, the crystal structure will remain the same as illustrated by:

$$\mathbf{R} = m\mathbf{a} + n\mathbf{b} + p\mathbf{c} \quad (2.1)$$

where m, n and p are integers.

The reciprocal lattice basis vectors $\mathbf{a}^*$, $\mathbf{b}^*$, $\mathbf{c}^*$ in term of primitive lattice basis vectors ($\mathbf{a}$, $\mathbf{b}$, $\mathbf{c}$) can be defined by

$$\mathbf{a}^* = 2\pi \left[\frac{(\mathbf{b} \times \mathbf{c})}{\mathbf{a} \cdot (\mathbf{b} \times \mathbf{c})} \right] \quad (2.2)$$

$$\mathbf{b}^* = 2\pi \left[\frac{(\mathbf{a} \times \mathbf{c})}{\mathbf{a} \cdot (\mathbf{b} \times \mathbf{c})} \right] \quad (2.3)$$

$$\mathbf{c}^* = 2\pi \left[\frac{(\mathbf{a} \times \mathbf{b})}{\mathbf{a} \cdot (\mathbf{b} \times \mathbf{c})} \right] \quad (2.4)$$

where $\mathbf{a} \cdot \mathbf{a}^* = 2\pi$, $\mathbf{a} \cdot \mathbf{b}^* = 0$, and so on.

It is important to recognise that the denominators are identical because $\mathbf{a} \cdot (\mathbf{b} \times \mathbf{c}) = \mathbf{b} \cdot (\mathbf{c} \times \mathbf{a}) = \mathbf{c} \cdot (\mathbf{a} \times \mathbf{b})$ and they denote the volume enclosed by these vectors ($\mathbf{a}$, $\mathbf{b}$ and $\mathbf{c}$).

The general reciprocal lattice vector ($\mathbf{G}$) is given as:

$$\mathbf{G} = h\mathbf{a}^* + k\mathbf{a}^* + l\mathbf{a}^* \quad (2.5)$$

where h , k and l are integers.

The relationship between the direct lattice vector $\mathbf{R}$ and the reciprocal lattice vector ($\mathbf{G}$) is given by:

$$\mathbf{G} \cdot \mathbf{R} = 2\pi \times \text{integer} \quad (2.6)$$

Note that the planes (100), (110) and (111) are called low index planes and any plane that has at least one index higher than 0 and 1 (i.e. 2 or higher) is named a high index plane [4].

2.2.2 ENERGY BANDGAPS

In solid state physics, the difference in energy between the bottom of the conduction band (CB) and the top of the valence band (VB) is referred to as the energy gap (E_g) or bandgap, as shown in Figure 2.5.

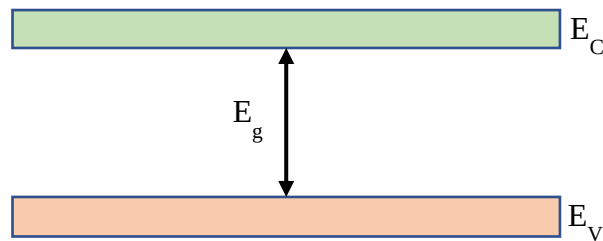


Figure 2.5: Schematic energy band diagram of a semiconductor.

Materials can be classified into three categories depending on their energy gap, namely, metals, semiconductors, and insulators. The energy gaps for metals, semiconductors and insulators are ~ 0 eV, ~ 0.17 eV (InSb) to ~ 6 eV (AlN) and $> \sim 6$ eV, respectively.

A semiconductor's bandgap is generally represented using the energy-wave vector (E-k) relationship as shown in Figure 2.6. When $k=0$ the conduction band's minima and valence band's maxima are roughly parabolic in shape and their energy is given by:

$$E_c = E_g + \frac{\hbar^2 k^2}{8\pi^2 m_e^*}, E_v = -\frac{\hbar^2 k^2}{8\pi^2 m_h^*} \quad (2.7)$$

where E_c is the energy of the conduction band, E_v is the energy of the valence band, $\hbar$ is Planck's constant, k is Boltzmann constant, m_e^* is the effective mass of the electron, and m_h^* is the effective mass of the hole. At very low temperatures (~ 0 K) all the electrons are confined to the valence band, and therefore the semiconductor behaves as an insulator. At higher temperatures, some electrons can acquire sufficient energy to make a transition to the conduction band and contribute to the conduction process.

2.2.3 DIRECT AND INDIRECT ENERGY BANDGAPS

Semiconductors can be classified as direct or indirect depending on how the bottom of the conduction band and the top of the valence band are positioned with respect to the wave vector (k).

In direct bandgap semiconductors, the valence band maxima and conduction band minima occur at the same k value, i.e. $k = 0$. In indirect bandgap semiconductors,

these two bands occur at different values of wave vector (k). GaAs and Si are the most common direct and indirect semiconductor, respectively. The $E(k)$ relationships of the two semiconductors are illustrated in Figure 2.6 [4].

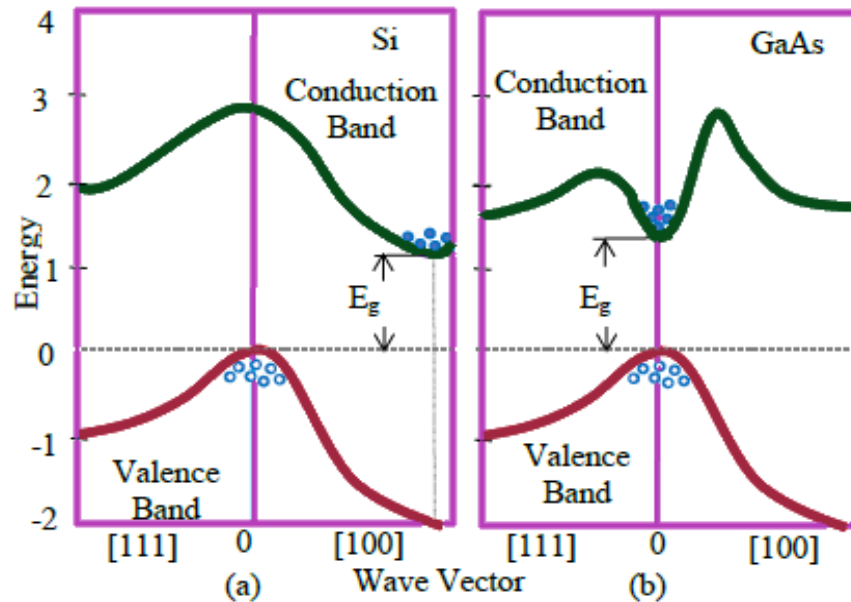


Figure 2.6: Energy-band structures of (a) Si which has an indirect band gap and (b) GaAs which has a direct band gap [7]. The full and open circles denote electrons and holes, respectively.

2.2.4 TEMPERATURE DEPENDENT ENERGY BANDGAPS

For semiconductor materials, the energy bandgap decreases as the temperature increases. With a rise in temperature, there is a corresponding rise in the atoms' thermal vibrational energy and vibration amplitude. Therefore, there is an increase in interatomic spacing which causes the potential of the electrons within the material to be reduced. As a result, the energy gap's size reduces correspondingly [8].

Varshni [9] formulated the empirical correlation for the energy bandgap (T)'s temperature dependency, which is given by:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \quad (2.8)$$

where $E_g(0)$ is the energy bandgap at 0 K, and α and β represent empirical parameters associated with the material. Table 2.1 lists empirical parameters for GaAs, Si and InAs at room temperature [10].

Table 2.1 Experimental parameters for temperature dependency of GaAs, Si and InAs bandgaps.

Parameter	Gallium Arsenide (GaAs)	Silicon (Si)	Indium arsenide (InAs)
E_g (eV)	1.42	1.12	0.35
α (meV/K)	0.541	0.473	0.276
β (K)	204	636	83

2.2.5 QUANTUM CONFINEMENT

In comparison with bulk materials, nanostructured materials have unique electronic and optical properties. Such unique properties of semiconductor nanomaterials are a result of what is known as the quantum size/quantum confinement effect, which arises when the system size is small when compared with the Bohr excitonic radius.

As Figure 2.8 shows, there are four classifications of semiconductors materials in relation to their material dimensions, these being three-dimensional (3-D)

structures (bulk), two-dimensional (2-D) structures (quantum well), one-dimensional structures (1-D) (quantum wire) and 0-dimensional (0D) structures (quantum dot). With bulk structures quantisation of particle motion does not exist and thus the particle has freedom of movement in all dimensions.

In quantum well structures, there is a uni-directional quantisation of particle motion, leaving the particle freedom of movement in the remaining two directions. This means that the continuous energy levels which exist in bulk materials turn into discrete energy levels within such layers.

With quantum wire structures, quantisation is bi-directional, and so there is only freedom of movement in a single direction. Quantisation is present in all three directions in quantum dot structures, so the particle has no freedom of movement. Figure 2.7 shows a diagram of a typical quantum well structure, generally created through the growth of a thin layer of semiconductor material, sandwiched by layers of a different semiconductor material with a larger bandgap. Two materials that can be employed to create a semiconductor quantum well are GaAs/AlGaAs with the quantum well being created within the thin GaAs layer surrounded by the AlGaAs barrier layers possessing a larger bandgap [\[11\]](#).

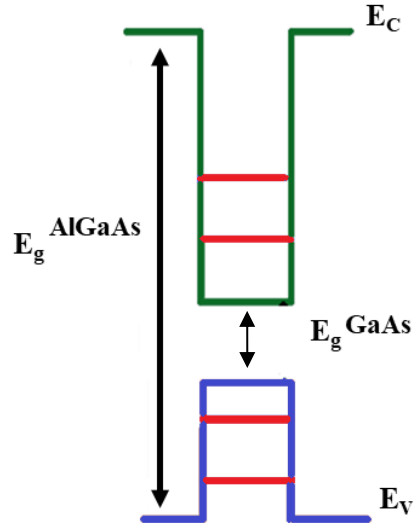


Figure 2.7: A typical diagram of a single quantum well. The red lines represent the allowed energy levels for an electron and a hole within the quantum well.

2.2.6 DENSITY OF STATES

It is important for the determination of carrier distribution in a semiconductor to consider how many states can exist for every energy. As atoms within solid materials are closely spaced, their interaction takes place via their electric field. As a result of this, their energy levels can be divided into a finite range of electronic states [12, 13].

Energy bands are created from the fact that their sublevels are closely spaced since electrons generally fill all lower energy states available. This results in two highest energy bands known as valence and conduction bands. In the conduction process, electrons can be excited to move from the valence band to the conduction band. Consequently, a positive charge (a hole) is created in the valence band. A semiconductor material's density of states ($N(E)$) represents the number of states available to be occupied at a specific energy level.

$N(E)$ is dependent on the confinement of the charge carriers. For 3D systems, $N(E)$ is related to energy via a square root function, $N(E) \propto E^{1/2}$ (Figure 2.8 (a)); in 2D systems $N(E)$ possesses a step-like function as a function of energy (Figure 2.8 (b)); in 1D systems $N(E)$ is proportional to $E^{-1/2}$ (Figure 2.8 (c)); in 0D systems $N(E)$ is independent of (delta function) energy (Figure 2.8 (d)) [4, 14].

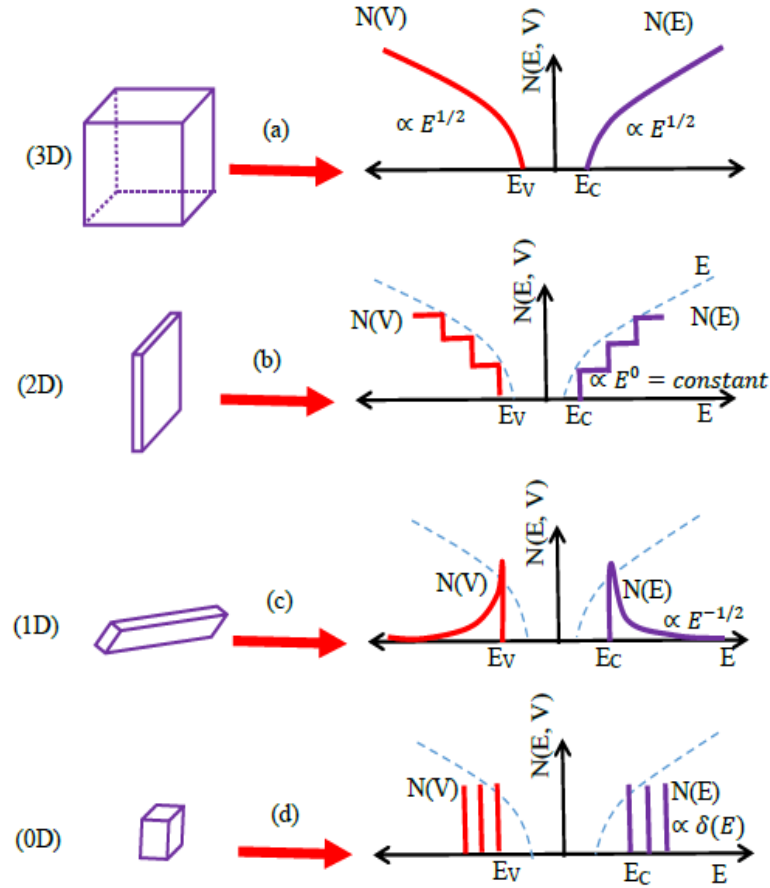


Figure 2.8: density of states for (a) bulk material (3D), (b) quantum well (2D), (c) quantum wire (1D) and (d) quantum dot (0D).

2.3 HETEROJUNCTION STRUCTURES

Homojunctions and heterojunctions are the most common structures.

Homojunction structures are formed by growing layers of identical semiconductor

materials one on top of the other. Generally, such materials have identical bandgaps but with different doping, as illustrated by Figure 2.9 (a). Heterojunction structures are fabricated by using different semiconductor materials that possess different energy bandgaps (and/or lattice constants) as shown in Figure 2.9 (b) [6].

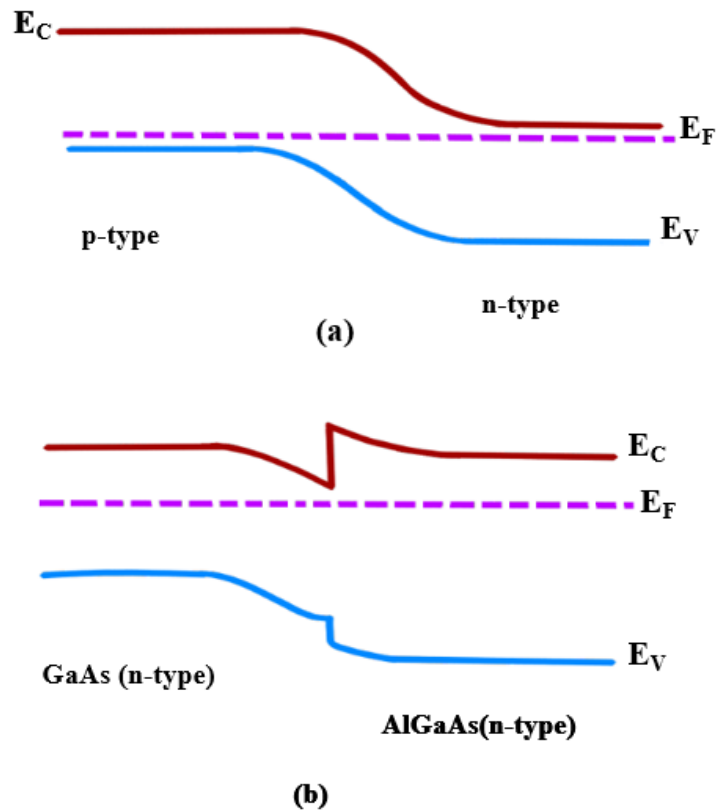


Figure 2.9: Energy band diagram showing (a) a homojunction structure and (b) a heterojunction structure.

2.3.1 LATTICE MISMATCH

A lattice-matched structure consists of two semiconductor materials that have identical lattice constants (Figure 2.10 (a)). However, when two semiconductor materials with different lattice constants are grown on top of each other the structure is referred to as a lattice-mismatched structure. The lattice mismatch, which represents the change in lattice constant at the interface, is given by:

$$\frac{\Delta a}{a_s} = \frac{a_{layer} - a_s}{a_s} \quad (2.9)$$

where a_{layer} represents the lattice constant of the epilayer and a_s is the lattice constant of the substrate [4].

In these structures, defects are generally produced at the heterojunction's interface. The greater the difference between the materials' lattice constants, the more defects there are. In lattice-mismatched systems two types of strain are created, namely compressive and tensile strain. If the lattice constant of the epitaxial material is higher than that of the substrate then compressive strain is produced as shown in Figure 2.10 (b). Tensile strain arises when the epilayer has a smaller lattice constant than the substrate (Figure 2.10 (c)).

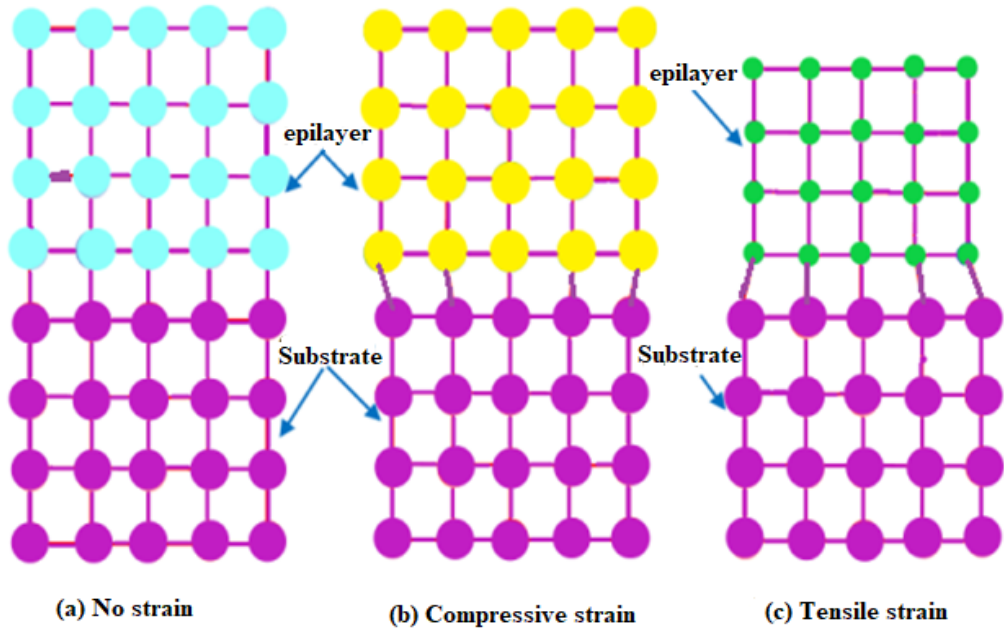


Figure 2.10: Schematic diagram showing: (a) lattice matched system, and (b) and (c) lattice-mismatched systems.

2.3.2 ATOM SIZE AND ELECTRONEGATIVITY

In addition to lattice mismatching, other parameters such as the atom size, energy band alignment, and electronegativity (χ) play a major role in the growth of heterostructures. If the size of the atoms of the two different materials is different, then strain is produced during the growth process of heterostructures. Electronegativity (χ) is generally regarded as an atom or molecule's ability to attract electrons towards itself to form chemical bonds [4]. Electronegativity (χ), which is a dimensionless quantity, is usually described using a Pauling scale. Linus Pauling published the first major paper on electronegativity in 1932 [15]. Pauling's theory states that if a heterostructure is formed from two different semiconductor materials A and B, the difference in the electronegativity of these two materials can be expressed by:

$$\chi_A - \chi_B = \left[(eV)^{-\frac{1}{2}} \right] \sqrt{E_D(AB) - \frac{[E_D(AA) + E_D(BB)]}{2}} \quad (2.10)$$

where χ_A and χ_B represent the electronegativity of A and B, respectively. $E_D(AB)$, $E_D(AA)$ and $E_D(BB)$ are the dissociation energies in eV between the atoms AB, AA and BB, respectively. The factor $\left[(eV)^{-\frac{1}{2}} \right]$ is used to make the value of electronegativity a dimensionless quantity.

2.3.3 BAND ALIGNMENTS

Energy band alignment between two semiconductor materials is another important parameter in the formation of heterojunctions. Figure 2.11 illustrates three forms of band alignments, namely straddled alignment (type-I), staggered alignment (type-II), and broken gap alignment (type-III). In the type-I band alignment, the valence band for the material with the lower energy gap (B) lies within the valence band of

the material with the larger energy gap (A); similarly, the conduction band of material B lies within the conduction band of material A [4]. InGaAs/InP and AlGaAs/GaAs are examples of type-I heterojunctions. Type-II band alignment occurs when the valence band of material B lies in the valence band of material A, and the conduction band of material A lies within the conduction band of material B. GaSb/GaAs heterojunction is an example of staggered alignment. However, when both the conduction and valence bands of material A lies within the conduction band of gap material B, a type-III band alignment is formed, such as in GaSb/InAs [12].

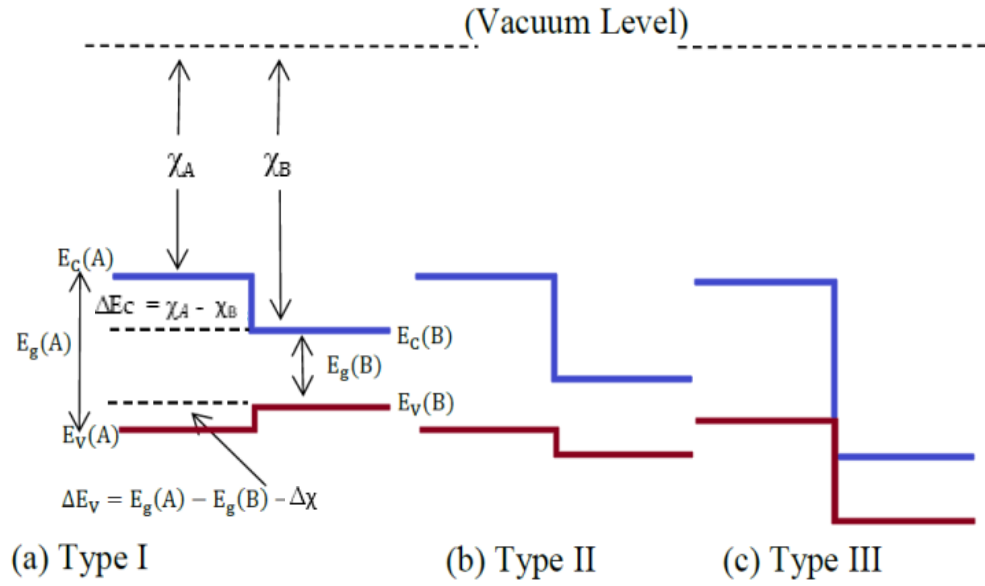


Figure 2.11: Energy bands alignment of (a) Type I (straddling), (b) type II (staggered) and (c) type III (broken-gap) heterojunctions.

In 1962 Anderson [16] suggested that the band offset for an ideal semiconductor heterostructure could be calculated using the electron affinity rule. In this model, due to the difference in affinities of electrons in the two different materials ($\chi_A -$

χ_B .) the conduction bands (ΔE_C) and valence bands (ΔE_v) offset energies are expressed as:

$$\chi_A - \Delta E_C - \chi_B = 0; \Delta E_C = \chi_A - \chi_B \quad (2.11)$$

$$\Delta E_v = \Delta E_g - \Delta\chi \quad (2.12)$$

where χ_A and χ_B represent the electronegativity of materials A and B, respectively.

$\Delta E_g = E_{gA} - E_{gB}$, where E_{gA} and E_{gB} are the energy bandgap of material A and B, respectively.

Nevertheless, there are limitations with this electron affinity model, which considers only intrinsic semiconductors, because it does not into account dislocations, surface interface states, and defect states.

2.4 GENERAL PROPERTIES OF SELECTED SEMICONDUCTOR MATERIALS

This section will present a review of some of the main properties of semiconductors investigated in this thesis.

2.4.1 GALLIUM ARSENIDE (GaAs)

Gallium arsenide (GaAs) is one of the most well-known and important III-V compound semiconductor material. This compound is formed using a combination of gallium (Ga, group (III)) and arsenic (As, group V) elements. Although the compound was discovered in 1920 by Goldschmidt, its properties were not discovered until 1952. The energy band diagram for this compound is illustrated in Figure 2.12. As can be clearly seen in this figure, GaAs is a direct band gap semiconductor, where the minima of the conduction band and the maxima of the

valence band occur at $k = 0$. This means that the transition of an electron from the valence band to the conduction band requires only a change in energy as the momentum is conserved. The direct bandgap nature of GaAs makes it a potential material for optoelectronic devices in comparison to indirect bandgap semiconductors such as Si.

GaAs is employed as a semi-insulating substrate in high-frequency integrated circuits due to its extremely high resistivity ($\sim 10^8 \Omega\text{-cm}$) in comparison with Si ($\sim 6.4 \times 10^2 \Omega\text{-cm}$). This high resistivity property, for example, reduces parasitic capacitive effects. Furthermore, devices employing GaAs are capable of operating at greater temperatures than Si devices as a result of its higher energy gap as compared with Si. Table 2.2 lists some of the important properties of intrinsic GaAs at room temperature (300 K) [17].

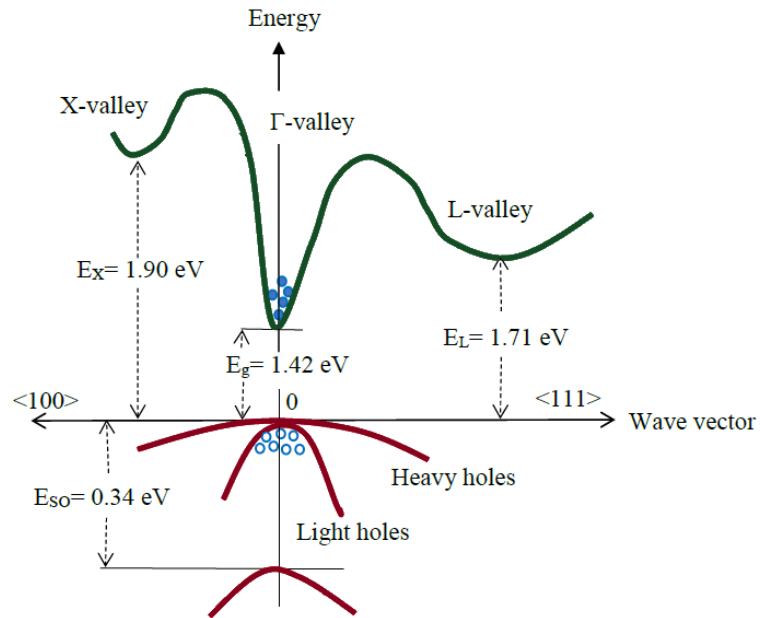


Figure 2.12: Band structure of GaAs. E_{SO} , E_Γ (E_g), E_X , E_L are energies of spin-orbital splitting, Γ -valley, X-valley and L-valley, respectively.

2.4.2 INDIUM ARSENIDE (InAs) AND INDIUM GALLIUM ARSENIDE (InGaAs)

2.4.2.1 INDIUM ARSENIDE (InAs)

The semiconductor material Indium arsenide (InAs) is made of indium (group III) and arsenic (group V). InAs, which is a direct band gap, has similar properties to GaAs. InAs is used in many electronic and optoelectronic devices including infrared detectors in the wavelength range 1–3.8 μm (when used as an InGaAs alloy) and quantum dots (QDs) lasers. The QDs (0D nanostructures) in the active layer of a laser can be formed because of the difference between the lattice constant of InAs and GaAs [18]. Table 2.2 illustrates some selected properties of InAs. Figure 2.13 illustrates the different stages involved in the growth of InAs QDs on a GaAs substrate: (a) a GaAs substrate is used as a template for the growth of the epilayers; (b) deposition of an undoped GaAs epitaxial buffer layer; (c) deposition of an InAs epitaxial layer with a thickness above the critical thickness for the formation of QDs; (d) a thin GaAs capping layer is grown on top of InAs QDs in order to enhance their optical efficiency by preventing problems associated with surface recombination effects [19] .

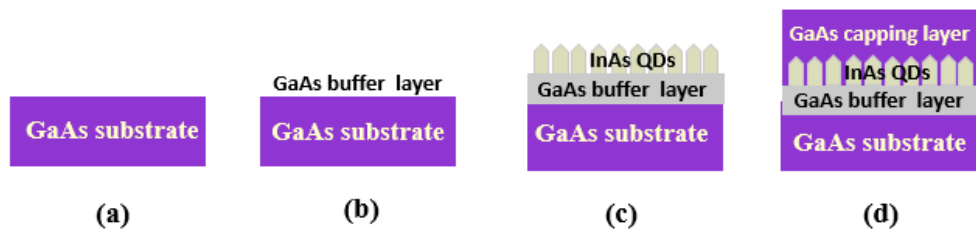


Figure 2.13: Epitaxial deposition processes involved in the growth of InAs quantum dots on a GaAs substrate.

2.4.2.2 INDIUM GALLIUM ARSENIDE (InGaAs)

Indium Gallium Arsenide (InGaAs), made from InAs and GaAs, is a widely used semiconductor, especially in photonics and electronics applications. For example, InGaAs has been used as a high-speed and high sensitivity photodetector in optical fibre telecommunications [20]. It is important to point out that different indium compositions (x) result in different optical properties of $\text{In}_x\text{Ga}_{1-x}\text{As}$ [20].

A single III-V semiconductor crystal substrate, for example GaAs and InAs, that have a lattice parameter close to that of InGaAs alloy could lead to the deposition of InGaAs single crystal epitaxial films. It is essential to have a good match between the lattice constants of the substrate and epitaxial thin film in order to maintain single crystal properties and avoid strain in the epilayer.

Table 2.2. shows some of the properties of InGaAs at room temperature (300K) [21].

2.4.3 ALUMINIUM ARSENIDE (AlAs) AND ALUMINIUM GALLIUM ARSENIDE (AlGaAs)

Aluminium Gallium Arsenide ($\text{Al}_x\text{Ga}_{1-x}\text{As}$) with a crystal structure similar to GaAs is the second most well-known III-V material after GaAs. The energy gap of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ can be tuned between that of GaAs (1.42 eV) and AlAs (2.168 eV). The nature of the energy gap of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ depends on the Al composition x . For $x \sim 0.45$ and $x > 0.45$, the band gap changes from direct to indirect, respectively [22]. The properties of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ crystal fall between those of GaAs and AlAs. The range of applications of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ span from near infrared to visible region

[12]. The energy change of the different conduction valleys (X, Γ , and L) at 300K as a function of Al content (x) is shown in Figure 2.14

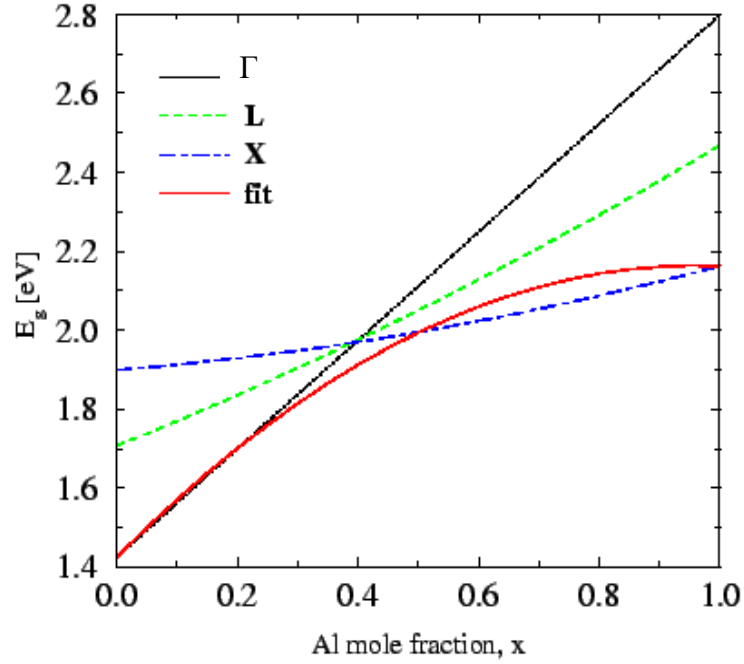


Figure 2.14: Differences in the conduction band valleys in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ as a function of Al composition (x) at 300 K [7, 23] The black, green and blue lines represent Γ , L and X, respectively. The red line represents the fit of the band gap of AlGaAs as a function of Al composition.

The lattice constant (a) of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ is calculated, to an initial approximation, by linearly interpolating the lattice constants of AlAs and GaAs. The room temperature lattice constant of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ can be expressed by:

$$a(x) = (0.56533 + 0.00078x) \text{ nm} \quad (2.13)$$

The difference between the lattice constants of GaAs and AlAs crystals is <0.5%, meaning that AlAs is nearly lattice matched to GaAs and therefore very smooth interfaces can be obtained between GaAs and AlGaAs. This lattice matching

condition helps greatly in the reduction of defects which could affect the performance of devices significantly. Selected room temperature properties of intrinsic $\text{Al}_x\text{Ga}_{1-x}\text{As}$ are presented in Table 2.3 with those of GaAs and AlAs for comparison purposes.

2.4.4 SILICON (Si)

Silicon is a chemical element with the symbol Si and atomic number 14. Silicon is the seventh-most abundant element on Earth [\[24\]](#) and is widely used as a semiconductor in the microelectronics industry. One of the main reasons why silicon is the most widely used semiconductor material is because of its abundance which makes it inexpensive compared to III-V semiconductors for example. Another reason why silicon is popular is the ease with which it forms oxides. Silicon dioxide is the most widely used insulator in integrated circuit (IC) technology due to its exceptionally stable chemical nature.

Doping of silicon semiconductor can be achieved by substituting silicon atoms with other atoms that have different numbers of valence electrons. For example, the introduction of boron and phosphorus impurities into the silicon crystal can provide the extra electrons (n-type) and holes (p-type), respectively, in silicon. The crystalline structure of silicon, which belongs to the group IV of the periodic table, consists of face centric cubic lattice structure (a diamond like structure). Silicon is an indirect semiconductor as shown in Figure 2.6, with a moderate energy band gap of 1.12 eV at room temperature. The temperature dependence of the band gap of silicon was determined by W. Bludau et al measured with optical means [\[25\]](#).

Table 2.2: Important properties of intrinsic GaAs, InAs and Ga_xIn_{1-x}As at 300K.

hh and lh represent heavy hole and light hole, respectively [8, 21, 26]

Parameter	GaAs	InAs	Ga _x In _{1-x} As	Si
Crystal Structure	Zincblende	Zincblende	Zincblende	Diamond
Lattice constant (Å)	5.6533	6.0583	6.0583-0.405x	5.43095
Crystal density (g/cm ³)	5.360	5.68	5.68-0.37x	5.02 10 ²²
Energy band gap (eV)	1.42	0.354	0.36+0.63x+0.43x	1.12
Band type	Direct	Direct	Direct	Indirect
Electron effective mass	0.063m ₀	0.023m ₀	(0.023 + 0.037x + 0.003x)m ₀	0.98m ₀
Hole effective mass	0.62m ₀ (hh) 0.087m ₀ (lh)	0.41m ₀ (hh) 0.026m ₀ (lh)	(0.41+0.1x)m ₀ (hh) (0.026+0.056x)m ₀ (lh)	m _h =0.49m ₀
Dielectric constant (static)	12.85	15.15	12.3-1.4x	11.9
Electron affinity (eV)	4.07	4.9	4.9 - 0.83x	4.05

Table 2.3: Some important properties of intrinsic $\text{Al}_x\text{Ga}_{1-x}\text{As}$ at 300K [23]. GaAs and $\text{Al}_x\text{Ga}_{1-x}\text{As}$ are also shown for comparison purposes.

Parameter	GaAs	$\text{Al}_x\text{Ga}_{1-x}\text{As}$
Crystal Structure	Zincblende	Zincblende
Lattice constant (Å)	5.6533	$5.6533 + 0.0078x$
Crystal density (g/cm ³)	5.360	$5.360 - 1.6x$
Energy band gap E_g (eV) at 300K	1.42	For $x < 0.45$ $E_g = 1.424 + 1.247x$ For $x > 0.45$ $E_g = (1.9 + 0.125x + 0.143x^2)$ $x > 0.45 \quad 1.9 + 0.125x + 0.143x^2$
Band type	Direct	Changes from direct to indirect for Al content $x > 0.45$
Electron effective mass	$0.063m_0$	$(0.063 + 0.083x)m_0$ ($x < 0.45$)
Hole effective mass	$0.62m_0$ (hh) $0.087m_0$ (lh)	$(0.62 + 0.14x)m_0$ (hh) $(0.087 + 0.063x)m_0$ (lh)
Dielectric constant (static)	12.85	$12.85 - 2.84x$

In summary, this chapter has dealt with some relevant topics related to semiconductors, crystal structures, heterojunctions and general properties of selected semiconductor materials (GaAs, InAs, AlAs , AlGaAs and Si)

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CHAPTER 3: SEMICONDUCTOR DEFECTS AND THEIR PROPERTIES

This chapter presents the different types of defects and their properties as trapping and generation recombination centres. Deep level defects and their carrier kinetics processes are also discussed. Additionally, this chapter describes some of the defects in GaAs.

3.1 CLASSIFICATION OF DEFECTS

A periodic arrangement of unit cells along the crystal orientation forms a perfect crystal [1, 2]. However, the crystal is often not perfect due to many types of defects including point, complexes, and extended defects. This chapter will discuss the different type of defects.

3.1.1 POINT DEFECTS

In material science, a point defect or a zero-dimensional defect is when an atom is missing or is irregularly located in the lattice structure. The crystal arrangement at an isolated site is altered by a point defect. Point defects include for example vacancies, interstitials, antisite, and substitutional defects, while extended defects include edge and screw dislocations.

Figure 3.1 illustrates several different types of defects. If the defect is the result of a missing atom at a certain crystal lattice site in a crystal structure as shown in Figure 3.1(a), it is called a vacancy defect. Figure 3.1(b) shows a substitutional impurity, when a foreign atom impurity replaces and occupies a regular lattice site of the host atom. One of the most common defects in weakly ionic materials or

covalently bonded ones is an antisite defect. This defect is an atom on a site which is normally occupied by a different atom as illustrated in Figure 1(c). For example, in GaAs a Ga atom can occupy an As site [As antisite (Ga_{As})] and vice versa [Ga antisite (As_{Ga})]. Figure 1 (d) shows the well-known interstitial defect in semiconductors which is created when an atom occupies the space between regular lattice sites. This defect has two types, one of them is self-interstitial which occurs when the atom is the same as the host crystal. The second type is foreign-interstitial which occurs when the atom is a foreign atom.

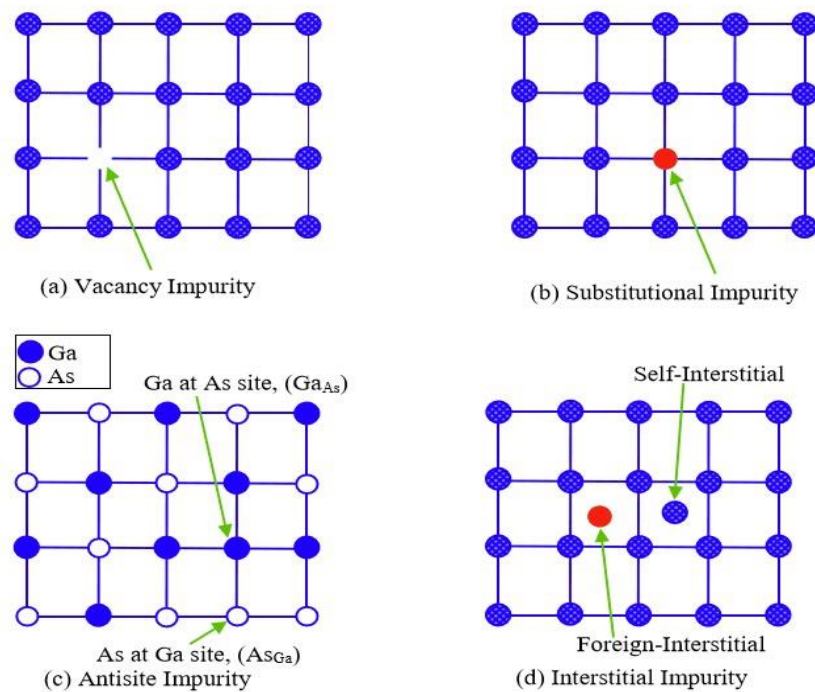


Figure 3.1: The different types of point defects in crystalline semiconductors: (a) Vacancy defect; (b) Substitutional defect; (c) Antisite defect; and (d) Interstitial defect.

3.1.2 COMPLEXES OF POINT DEFECTS

When one or more-point defects are bounded to each other, complexes of point defect can be created. This occurs in a similar way to that of bounded atoms in molecules. As can be seen in Figure 3.2 (a) one of the complex defect types is the

split-interstitials defect which is created by two interstitial atoms forming a pair. These defects are created by either a pair of two interstitial atoms of the same host material or by a pair of two defect interstitial atoms. Figure 3.2 (b) shows the different kinds of complexes in a crystalline material which can be formed by vacancy defects. Specifically, when two vacancies produce a pair, the resultant complex is termed Di-vacancy. Moreover, when a vacancy and self-interstitial atom form a pair, the resultant complex is called the Frenkel defect. Likewise, when there is an interaction between a pair of vacancy and foreign-interstitial, a complex is formed known as a vacancy-impurity. Furthermore, a split vacancy is created when two vacancies and interstitial atom form a pair. In addition, when a substitutional impurity atom forms a pair with an interstitial impurity atom, an additional complex defect is formed. This is known as an impurity-pair and is shown in Figure 3.2 (c).

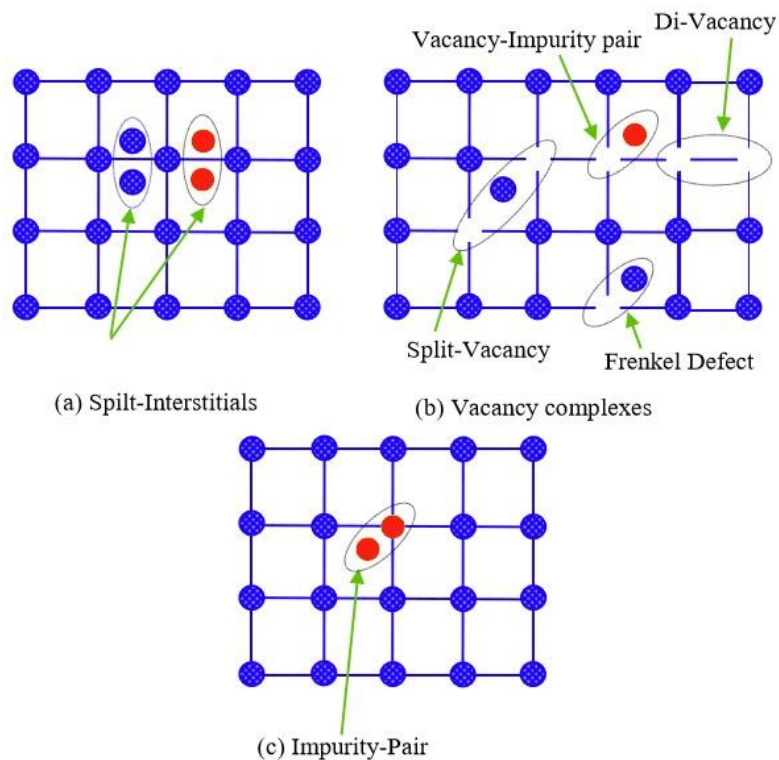


Figure 3.2: The different types of complex defects: (a) spilt-interstitials, (b) vacancy complexes, and (c) complexes of impurity-pair.

3.1.3 LINEAR DEFECTS

When a line of atoms is out of its regular position in the crystal, the linear defects, (dislocations), which are one-dimensional defects, can be created. The main types of these linear defects are edge dislocations and screw dislocations. The distortion of close atoms and an edge dislocation are created due to an extra half-plane of atoms being inserted into the crystal lattice as shown in Figure 3.3 (a). Furthermore, when one part of the crystal lattice is moved with regard to the other crystal part, a screw dislocation is created. This is illustrated in Figure 3.3 (b)

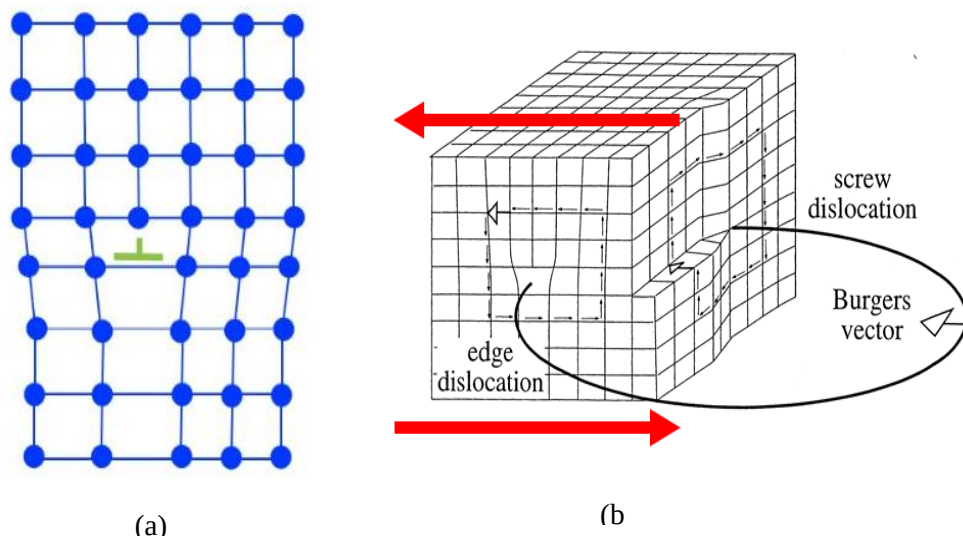


Figure 3.3: Illustration of different forms of linear defects: (a) edge dislocations and (b) screw dislocations [3].

3.2 DEFECTS AND THEIR CARRIER KINETICS

3.2.1 SHALLOW LEVELS AND DEEP LEVELS DEFECTS

Any type of impurities will have a significant impact in a semiconductor if it has its energy level inside the bandgap of the semiconductor. Defects are classified according to their energies, namely shallow and deep levels. When the energy of

the defects is nearer to the conduction or valence band, the defects are known as shallow-level impurities. These have low ionisation energies (< 0.1 eV), enabling them to be easily ionised at room temperature, and therefore this results in an increase of the electrical conductivity of the semiconductors. Another term for shallow-level defects is dopant atoms as they are deliberately incorporated in the semiconductor. They are known as shallow donors if they donate electrons to the conduction band of the host material or shallow acceptors if they donate holes to the valence band. Conversely, if a defect has energy levels higher than 0.1 eV below the conduction band or above the valence band, it is known as a deep-level impurity. These deep energy level defects can affect the electrical and optical properties of semiconductor materials and the performance of electronic and optoelectronic devices. Deep levels are key in semiconductors as they may serve as generation–recombination centres or trapping centres[4-7]. Figure 3.4 demonstrates the shallow and deep levels within the band gap of a semiconductor.

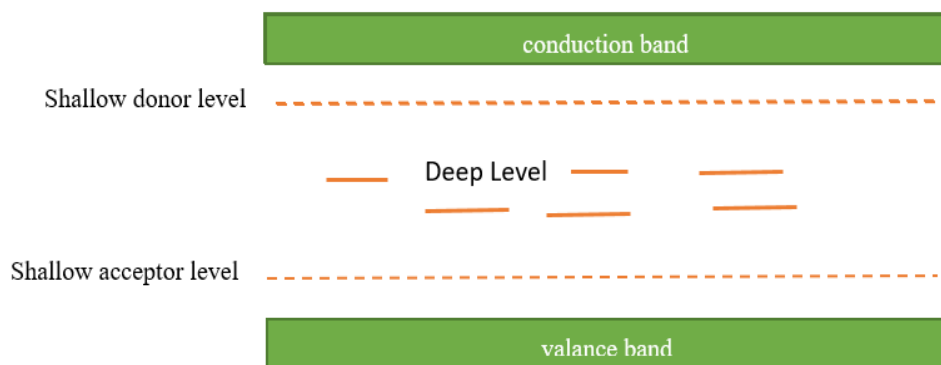


Figure 3.4: Schematic diagram showing shallow and deep levels in a semiconductor.

3.2.2 SHOCLEY-READ-HALL THEORY: GENERATION – RECOMBINATION PROCESSES

Deep-level impurities within a semiconductor are frequently referred to as generation–recombination (G–R) centres (see Figure 3.5) [1, 2, 5, 7]. At equilibrium, the emission and capture rates of carriers are used to determine the occupancy of a deep level. Recombination of electrons and holes occurs in a semiconductor in two ways. Direct recombination, a band-to-band process, usually occurs in pure semiconductors, while indirect recombination happens via deep energy levels that are present within the bandgap of the material.

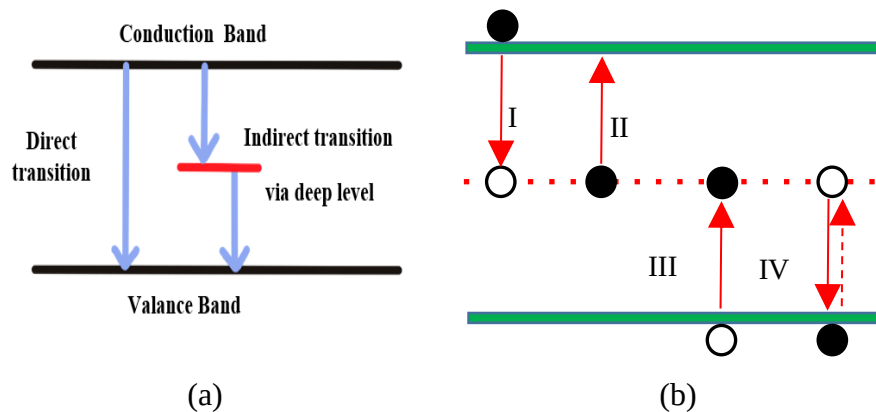


Figure 3.5: Schematic diagrams showing (a) a band-to-band recombination (direct transition) and recombination through a deep level (indirect transition via an intermediate level ET); (b) the capture and emission processes: (I) electron capture, (II) electron emission, (III) hole capture and (IV) hole emission.

Consider the case in which a deep-level impurity with energy (E_T) in the forbidden gap has a concentration (N_T) distributed across the semiconductor. Initially, an assumption can be made that an electron in the conduction band is captured by the centre (Figure 3.5 (I)). This captured electron can be characterised by its electron

capture coefficient (c_n). Following this, the electron can be either re-emitted to the conduction band, which is referred to as electron emission (e_n) (Figure 3.5 (II)), or a hole from the valence band can be captured by the centre, a process that is referred to as hole capture (c_p) as shown in Figure 3.5 (III). It should be noted that, if one of these two processes occur, a hole will occupy the deep centre, which leads to the following potential outcomes. First, as indicated in Figure 3.5 (IV), the hole can be emitted back to the valence band by the centre (referred to as hole emission, or e_p) or an electron can be captured from the conduction band (Figure 3.5 (I)). It is important to point out that the process detailed in Figure 3.5 (IV) is often regarded as an electron emission from the valence band to the centre, as indicated by the dashed arrow in Figure 3.5 (IV). It should also be noted that the processes detailed in Figure 3.5 (b) are the only processes that can occur between the conduction band, valence band, and impurity energy levels.

A process including electron capture (Figure 3.5 (I)) followed by hole capture (Figure 3.5 (III)) is referred to as a recombination process. However, as noted in Figure 3.5 (II), a generation process occurs when an electron emission takes place towards the conduction band and then a hole is emitted to the valence band, as demonstrated in Figure 3.5 (IV). However, a process called trapping, which does not involve generation or combination, can also take place. The trap centre is a deep level at which electron capture precedes the emission of an electron towards the conduction band or at which hole capture precedes the emission of the same hole towards the valence band. Only the conduction or valence bands participate in the trapping process with the impurity level. In contrast, in the generation or recombination process both the conduction and valence bands as well as impurity level are involved in the process [5].

The centres situated in the upper half of the band gap are typically characterised by an electron emission rate that far exceeds the hole emission rate. Likewise, the centres that are situated in the lower half of the band gap, the hole emission rate is greater than the electron emission rate. It should also be noted that a G–R centre can be filled by an electron or a hole. It is said to be in the n_T state in the former case and in the p_T state in the latter case. When a G–R centre is a donor, the n_T state is neutral while the p_T state is positively charged. In contrast, when the G–R centre is an acceptor, the n_T state is negatively charged while the p_T state is neutral. The total density of G-R centers (N_T) filled by of electrons (n_T) or hole (p_T) is given by:

$$N_T = n_T + p_T \quad (3.1)$$

When an electron or hole is generated by a centre or recombine in a centre, the density of electrons in conduction band ‘ n ’, the density of holes ‘ p ’ in valence band and charge states of the centers ‘ n_T ’ and ‘ p_T ’ are all time dependent.

When a center captures an electron from the conduction band (I) the density of electrons in the conduction band is reduced and the electron density increases in conduction band as emission increases (II). The rate of change of electrons in G-R center is given by:

$$\frac{dn}{dt} |_{G-R} = (II) - (I) = e_n n_T - n c_n p_T \quad (3.2)$$

where (I) and (II) are electron capture and electron emission processes.

It is important to point out that radiative and Auger recombinations are not taken into consideration in equation (3.2). Here, only the G-R mechanism is considered. From equation 3.1, $e_n n_T$ (process II) does not depend on electrons being in the

conduction band. However, to capture an electron ($nc_n p_T$; process I) there must be electrons in the conduction band.

A similar relation for the hole applies and is given by:

$$\frac{dp}{dt} |G-R = (IV)-(III) = e_p p_T - p c_p n_T \quad (3.3)$$

where (III) and (IV) are hole capture and hole emission processes.

It is important to note that the electron capture coefficient c_n (or hole capture coefficient c_p) is dependent upon the electron (hole) thermal velocity $\langle v_n \rangle_{th}$ ($\langle v_p \rangle_{th}$) and the electron (hole) capture cross-section σ_n (σ_p) of the G-R centre.

$$c_n = \langle v_n \rangle_{th} \sigma_n \quad (3.4)$$

Whenever an electron or hole is emitted or captured, the occupancy of the G-R state changes. This rate of change is calculated from equation 3.2 and 3.3, and is given by:

$$\frac{dn_T}{dt} = \frac{dp}{dt} - \frac{dn}{dt} = (c_n n + e_p)(N_T - n_T) - (c_p p + e_n)n_T \quad (3.5)$$

For the steady state condition

$$\frac{dn_T}{dt} = 0$$

and therefore n_T can be expressed in the following way:

$$n_T = \frac{e_p + c_n n}{e_n + c_n n + e_p + c_p p} N_T \quad (3.6)$$

Equation 3.6 is taken into account for most of deep-level impurity measurements [5, 8].

The detail balance principle states that at thermal equilibrium the rates of creation and absorption in semiconductors are equivalent. In view of this principle, the following relation can be stated:

$$e_n n_T = c_n n p_T \quad (3.7)$$

By using equation (3.4) for c_n and equation (3.7):

$$e_n n_T = \langle v_n \rangle_{th} \sigma_n n p_T \quad (3.8)$$

A similar equation can be used for the case of holes as given below:

$$e_p p_T = \langle v_p \rangle_{th} \sigma_p p n_T \quad (3.9)$$

The total density of deep levels N_T is related to the Fermi-Dirac distribution, f , and can be formulated in the following way:

$$N_T = n_T + p_T = N_T f + N_T (1 - f) \quad (3.10)$$

where ‘ f ’ is the Fermi Dirac distribution function which represents the number of states occupied by electrons, and ‘ $(1-f)$ ’ represents the number of states occupied by holes.

The Fermi Dirac distribution function is expressed by:

$$f = \left[\frac{1}{1 + \exp \left(\frac{E_T - E_F}{k_B T} \right)} \right] \quad (3.11)$$

where E_F represents the energy of the Fermi level, k_B denotes the Boltzmann constant and T is the temperature.

Combining Equations 3.7, 3.10 and 3.11 yield the following expression for e_n :

$$e_n = \sigma_n \langle v_n \rangle_{th} n \exp \left(\frac{E_T - E_F}{k_B T} \right) \quad (3.12)$$

where n represents the electron density in the conductance band, which can be expressed as follows:

$$n = n_i \exp \left(\frac{E_F - E_i}{k_B T} \right) = N_c \exp \left(-\frac{E_c - E_F}{k_B T} \right) \quad (3.13)$$

where $n_i = N_c \exp \left(\frac{E_i - E_c}{k_B T} \right)$ and is the density of the states of the intrinsic material.

Using equations 3.12 and 3.13 e_n can be expressed as:

$$e_n = \sigma_n \langle v_n \rangle_{th} N_c \exp \left(-\frac{E_c - E_T}{k_B T} \right) \quad (3.14)$$

where N_c is the density of states in the conduction band, $N_c = 2 \left(\frac{2\pi m_e^* k_B T}{h^2} \right)^{\frac{3}{2}}$, $\langle v_n \rangle_{th}$

is the thermal velocity of electrons, $\langle v_n \rangle_{th} = \left(\frac{3k_B T}{m_e^*} \right)^{\frac{1}{2}}$, and m_e^* represent the effective mass of electrons.

Similarly, by substituting $p = N_v \exp \left(-\frac{E_F - E_v}{k_B T} \right)$ into equation 3.9 yields the following expression for e_p :

$$e_p = \sigma_p \langle v_p \rangle_{th} N_v \exp \left(-\frac{E_T - E_c}{k_B T} \right) \quad (3.15)$$

where N_v represents the state density in the valence band, $N_v = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{\frac{3}{2}}$, $\langle v_p \rangle_{th}$ denotes the thermal velocity of holes, $\langle v_p \rangle_{th} = \left(\frac{3kT}{m_p^*}\right)^{\frac{1}{2}}$, and m_p^* represent the effective mass of holes.

In turn, $\langle v_n \rangle_{th}$, N_c , $\langle v_p \rangle_{th}$ and N_v can be substituted into equations 3.14 and 3.15, yielding the following:

$$e_n = AT^2 \sigma_n \exp\left(-\frac{E_c - E_T}{k_B T}\right) \quad (3.16)$$

where A refers constant value, $A = 2\left(\frac{2\pi m_e^* k}{h^2}\right)^{\frac{3}{2}} \frac{(3k)^{\frac{1}{2}}}{m_e^*}$:

$$e_p = AT^2 \sigma_p \exp\left(-\frac{E_T - E_v}{k_B T}\right) \quad (3.17)$$

3.3 DEFECTS IN GALLIUM ARSENIDE

The use of semiconductor materials in modern electronics has grown tremendously over the past few decades. However, it is difficult to produce perfect crystals of these materials. Every crystal has imperfections/defects due to either the ability of foreign atoms to enter the crystal structure or because some atoms occupy different sites in the crystal lattice [9]. Generally, these defects affect the performance of devices by altering their electrical and optical properties [5].

To significantly increase the performance for example of solar devices, it is essential to understand and optimise the growth fabrication and processing processes in order to minimise the defects that affect the properties of photovoltaic

devices. In the following section a brief literature review of defects in GaAs will be presented.

Generally, Gallium arsenide (GaAs), a III-V compound semiconductor, is considered to be an important material and is used extensively in optoelectronics devices. However, there are different types of native defects in GaAs. These defects, which can be created during the growth process, include vacancies, interstitials, and antisite defects. The most significant intrinsic defect in GaAs is the electron trap EL2. The energy of this defect is usually in the range of 0.70 eV to 0.85 eV[10]. Typically, this defect has a concentration of $\sim 10^{16} \text{ cm}^{-3}$ and $\sim 10^{14} \text{ cm}^{-3}$ in bulk and epitaxially grown materials, respectively [9]. It originates from the isolated Arsenic antisite defect (As_{Ga}) [11-13] or complex defect including As_{Ga} and arsenic interstitial [13, 14] .

EL3 is also a well-known trap in GaAs with an energy of approximately $\sim 0.575 \text{ eV}$ [8]. This defect is generally associated with complexes of off-center substitutional oxygen on arsenic sites (ocO_{As}) [15]. EL5 is also another common defect with an energy of $\sim 0.43 \text{ eV}$ in GaAs. This defect was assigned to complexes involving As interstitials- Ga vacancies ($\text{As}_i\text{V}_{\text{Ga}}$) [16].

A further intrinsic defect in GaAs is EL6 which has an activation energy of $\sim 0.35 \text{ eV}$ [12]. This defect was attributed to the complex defect involving arsenic antisite defect (As_{Ga}) and arsenic vacancy (V_{As}) [17]. In addition, there is another intrinsic defect in GaAs with a low activation energy trap of $\sim 0.18 \text{ eV}$ and is labelled as EL10. The nature of EL10 is related to an arsenic vacancy (V_{As}) complex defect involving an impurity [18, 19].

Table 3.1: Some important defects in GaAs

The Defect	The Activation Energy trap	The Origin
EL2	0.70 eV to 0.85 eV	The isolated Arsenic antisite defect (As_{Ga}) or complex defect including As_{Ga} and arsenic interstitial
EL3	~ 0.575 eV	associated with complexes of off-center substitutional oxygen on arsenic sites (ocO_{As})
EL5	~ 0.43 eV	assigned to complexes involving As interstitials- Ga vacancies ($\text{As}_i\text{V}_{\text{Ga}}$)
EL6	~ 0.35 eV	The complex defect involving arsenic antisite defect (As_{Ga}) and arsenic vacancy (V_{As})
EL10	~ 0.18 eV	An arsenic vacancy (V_{As}) complex defect involving an impurity

In conclusion, the classification of defects in semiconductors and their carrier kinetics, and relevant defects in GaAs were presented. .

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CHAPTER 4: EXPERIMENTAL TECHNIQUES

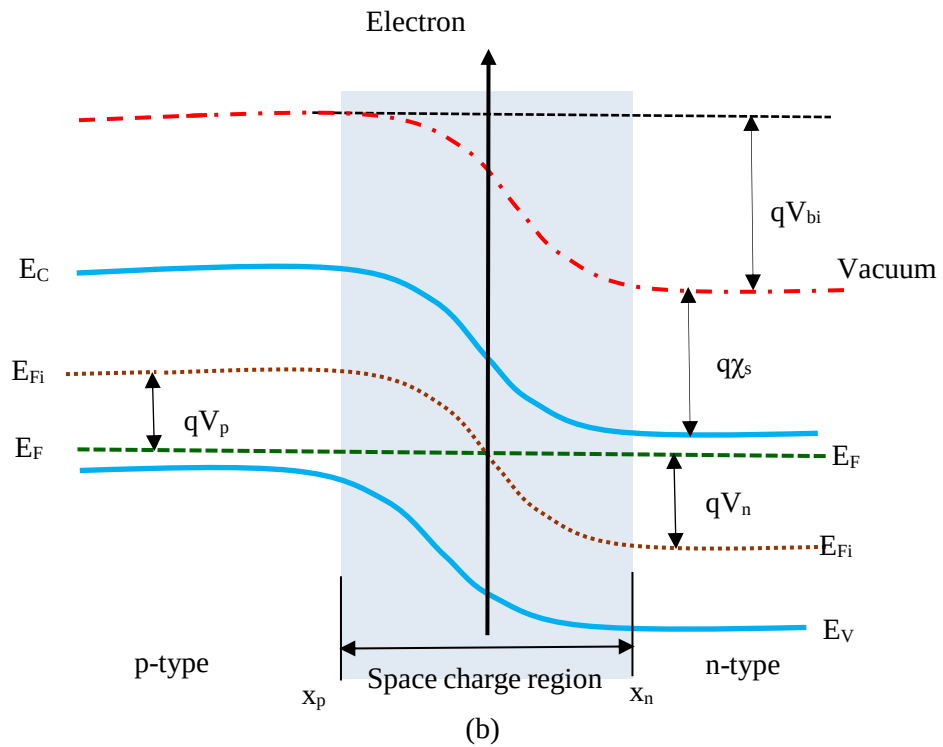
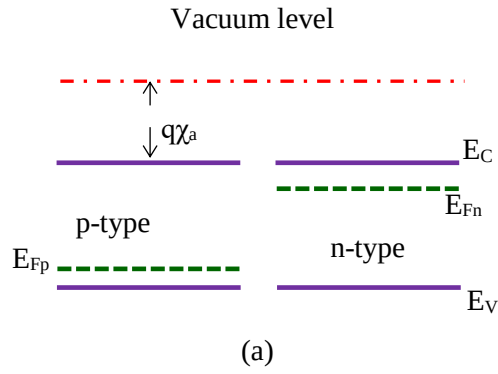
Semiconductors are important materials which are used in wide-ranging applications including electronic and optoelectronic devices because of their ability to form different types of electrical junctions [1]. Some examples of the preferred structures for DLTS measurements are electrical junctions such as P-N junctions, P-I-N junctions and Schottky diodes. The first step to understanding and explaining the physics of different semiconductor devices is to comprehend how these junctions operate. In addition, in order to investigate semiconductors diodes, a wide range of electrical and optical characterisation techniques are available. In this chapter the fundamental properties of a p-n junction and a Schottky diode will be reviewed. Current-voltage (I-V), capacitance-voltage (C-V), deep level transient spectroscopy (DLTS), Laplace DLTS and photoluminescence (PL) techniques used to investigate the electrical and optical properties of the samples will be presented. Moreover, this chapter will consider the principles and details of the hardware and software implemented using these techniques.

4.1. THE P-N JUNCTION

A semiconductor is considered n-type once it has been doped in a way that makes electrons majority carriers. However, if the holes are majority carriers, the semiconductor is called p-type. When materials from both types come into contact, the electrons from the n-type semiconductor transfer to the p-type semiconductor, and holes from the p-type transfer to the n-type, creating a p-n junction [2].

Figure 4.1 presents diagrams of the energy bands of the p-n junction before and after the junction formation under thermal equilibrium conditions (and without the

implementation of a voltage bias) along with the various discrete regions of a p–n junction . χ is the electron affinity of the semiconductor material. E_{Fn} and E_{Fp} are the electron and hole Fermi levels, respectively, and qV_{bi} is the built-in potential. E_c , E_v , and E_{Fi} depict the conduction band energy, valence band energy and intrinsic Fermi level, respectively. The potential difference between the Fermi level and intrinsic Fermi level in n-region and p-region are represented as V_n and V_p , respectively. x_n and x_p are the depletion layer widths in the n and p regions, respectively [1] .



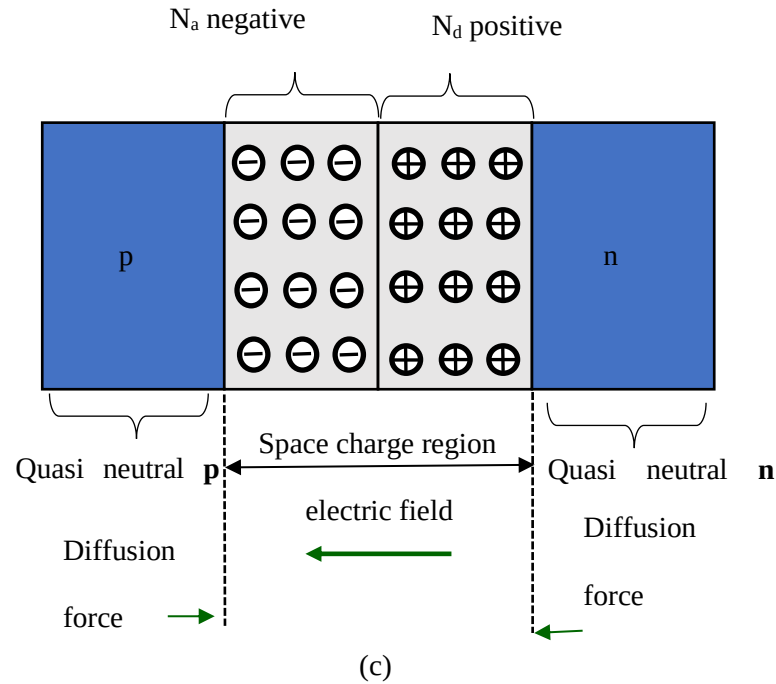


Figure 4.1: Diagrams of a p–n junction: (a) the energy band of p-type and n-type semiconductors, (b) the energy band of p–n junction and (c) p–n junction showing the depletion region (or space charge region).

Note that the p–n junction’s Fermi level (E_F) is constant across the entire region when the junction is in thermodynamic equilibrium, as shown in Figure 4.1(b). Furthermore, the figure indicates that the n and p regions are uniformly doped and that an abrupt transition exists between the two regions, establishing what is referred to as an abrupt junction (also termed a step junction or shallow diffused junction). In contrast, a linearly graded junction (also described as a deep diffused junction) is established when the p–n junction region does not have a uniform doping concentration. As a result, the modification in doping at the metallurgical junction is subject to grading. Figure 4.1(c) outlines the following distinct regions of the p–n junction: the quasi-neutral p and n regions (QNR) and the space-charge (or depletion) region (SCR). The former is situated away from the metallurgical

junction, and the latter consists of ionised shallow acceptors and ionised shallow donors (in the p-depletion and n-depletion regions, respectively).

Figure 4.2 (a) shows an abrupt junction due to a sharp change in the impurity concentration occurring at the p-n junction, where N_D and N_A represent the concentration of donor and acceptor atoms, respectively. For linearly graded junctions, the impurity concentration is modified in a linear way according to the distance from the junction as shown in Figure 4.2 (b).

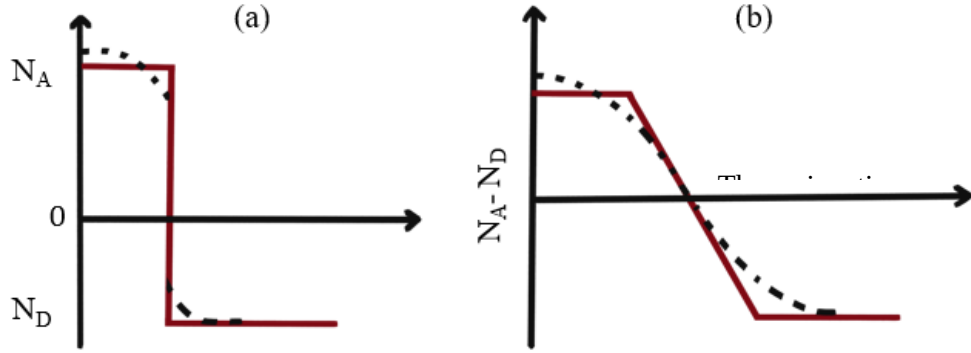


Figure 4.2: (a) A step junction and (b) a linearly graded junction with the junction depth.

Equations (4.1) and (4.2) below describe the electron and hole concentrations in the two regions of the p-n junction:

$$n = n_i \exp\left(\frac{V_n}{V_T}\right) \quad (4.1)$$

and

$$p = n_i \exp\left(\frac{-V_p}{V_T}\right) \quad (4.2)$$

where n_i is the intrinsic carrier density, $V_T = \frac{k_B T}{q}$ is the thermal voltage (k_B is the Boltzmann constant, q is the electric charge and T denotes temperature), and V_n and V_p represent the electrostatic potential in the n and p regions of the junction, respectively.

For abrupt and linearly graded p–n junctions, it is possible to use Poisson’s equation and the continuity equation to determine the carrier distribution, built-in potential, electric field, and potential profile in the junction’s SCR.

In general terms, the potential V of the junctions is described by a one-dimensional version of Poisson’s equation:

$$\frac{d^2 V}{dx^2} = \left(\frac{d\varepsilon}{dx} \right) = \frac{\rho(x)}{\varepsilon_s} = \frac{q}{\varepsilon_s} [N_D^+(x) - n(x) - N_A^-(x) + p(x)] = 0 \quad (4.3)$$

where ρ denotes the charge density, ε_s represents the semiconductor’s permittivity; $n(x)$ and $p(x)$ are the carrier densities at distance x from the junction, and $N_D^+(x)$ and $N_A^-(x)$ are the uncompensated donor and acceptor ions, respectively.

To solve equation (4.3), it is first necessary to perform a simplification by applying the depletion approximation. The central assumptions of this process are that the sole doping impurities are ionised (namely, N_D^+ and N_A^-) within the SCR and that the way in which the free carriers (namely, n and p) contribute to the local charge should be neglected. In addition, the space-charge regions are assumed to be completely depleted, meaning that there is an absence of free electrons in the depletion region on the n-type side and an absence of free holes in the depletion region on the p-type side. The charge densities within the depletion regions are

equivalent to the n-type material and to the p-type material (in which the metallurgical junction is assumed to be the origin). Consequently, it is possible to utilise suitable boundary conditions (along with equations (4.1), (4.2), and (4.3)) to determine the built-in potential, electric field, and charge distribution in various regions of the p–n junction. Previous studies have shown that the total charge density is equal to zero in the QNR. This means that, under the assumption of complete ionisation, equation (4.3) can be rewritten into equation (4.4):

$$[n - p - N_D - N_A] = 0 \quad (4.4)$$

where N_A and N_D represent the hole and electron densities on the p-side and n-side, respectively. It should also be noted that in the quasi-neutral n region, if it is assumed that N_A is zero (or $N_A \ll N_D$), $p \ll n$, and $N_A = p = 0$, it is possible to obtain the electrostatic potential (V_n) at the edge of the depletion layer by substituting the above assumptions into equations (4.4) and (4.1). Thus, it is possible to state the following:

$$n = N_D \quad (4.5)$$

$$N_D = n_i \exp\left(\frac{V_n}{V_T}\right) \quad (4.6)$$

Taking the log of the right-hand and left-hand sides of equation (4.6) and solving for the potential gives the following:

$$V_n = V_T \ln\left(\frac{N_D}{n_i}\right) \quad (4.7)$$

With the use of similar assumptions, the electrostatic potential (V_p) at the edge of the depletion layer can be formulated as follows:

$$V_p = -V_T \ln\left(\frac{N_A}{n_i}\right) \quad (4.8)$$

Lastly, it is possible to calculate the internal built-in potential (V_{bi}), which comes about as a consequence of the charge displacement by subtracting equation (4.8) from equation (4.7). This yields the following:

$$V_{bi} = V_n - V_p = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (4.9)$$

Separating positive and negative charge densities results in the formation of an electric field in the depletion region. To keep things simple, it should be assumed that, within the depletion region, n is equal to p and both are equal to zero and ionisation is complete. In view of this, it is possible to derive the following from equation (4.3):

$$\frac{d^2V}{dx^2} = \left(\frac{d\varepsilon}{dx}\right) = \begin{cases} \frac{qN_A}{\varepsilon_s} & -x_p \leq x \leq 0 \\ -\frac{qN_D}{\varepsilon_s} & 0 \leq x \leq x_n \\ 0 & x \leq x_n \text{ and } x \geq x_n \end{cases} \quad (4.10)$$

where x_n and x_p denote the depletion layer widths in the n and p regions, respectively (see Figure 4.1(b)). After the integration of equation (4.10), the electrical field can be described as follows:

$$\varepsilon(x) = -\frac{qN_A(x_p + x)}{\varepsilon_s} \quad \text{for } -x_p \leq x \leq 0 \quad (4.11)$$

$$\varepsilon(x) = -\frac{qN_D(x_n - x)}{\varepsilon_s} \quad \text{for } 0 \leq x \leq x_n \quad (4.12)$$

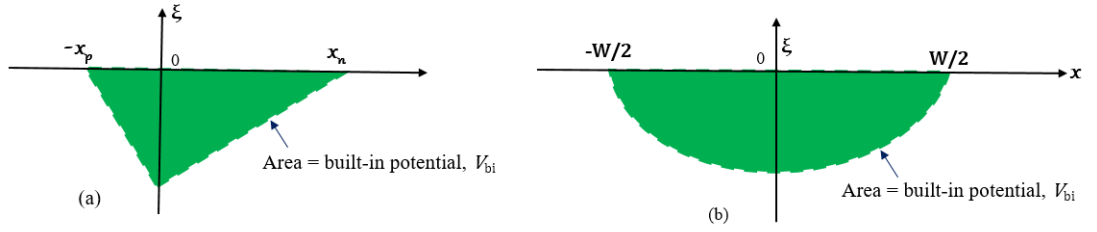


Figure 4.3: Illustration of the electrical field distribution in (a) a step junction and (b) a linearly graded junction. It should be noted that ε_m represents the maximum electric field and W is the width of the depletion region.

As illustrated in Figure 4.3(a), the electrical field changes linearly in the depletion region. This process occurs until the maximum value at $x = 0$ is established (at the point of the metallurgical junction). In view of this, it is possible to yield the maximum electric field (ε_m) from equations (4.11) and (4.12) at $x = 0$. This is given by the following equation:

$$|\varepsilon_m| = \frac{qN_A x_p}{\varepsilon_s} = \frac{qN_D x_n}{\varepsilon_s} \quad (4.13)$$

It should be noted that the potential (V) and electrical field are inextricably linked since $\varepsilon(x) = -\frac{dV}{dx}$. In view of this, the integration of equation (4.11) yields the following:

$$V(x) = \frac{qN_A}{2\varepsilon_s} (x_p + x)^2 \quad \text{for } -x_p \leq x \leq 0 \quad (4.14)$$

$$V(x) = V(0) + \frac{qN_D}{\varepsilon_s} \left(x_n x - \frac{x^2}{2} \right) \quad \text{for } 0 \leq x \leq x_n \quad (4.15)$$

Hence, using equation (4.14), it is possible to describe the potential across the p region in the following way:

$$V_p = \frac{qN_A x_p^2}{2\epsilon_s} \quad (4.16)$$

Moreover, using equation (4.15), it is possible to describe the potential across the n-region as follows:

$$|V_n| = -\frac{qN_D x_n^2}{2\epsilon_s} \quad (4.17)$$

In view of this, the built-in potential can be expressed as follows:

$$V_{bi} = V_p + |V_n| = V(x_n) = \frac{\epsilon_m}{2} (x_p + x_n) \quad (4.18)$$

$$\text{Where } |\epsilon_m| = \sqrt{\frac{2qN_A V_p}{\epsilon_s}} = \sqrt{\frac{2qN_D |V_n|}{\epsilon_s}} \quad (4.19)$$

Owing to the continuity of the electrical field at the junction interface, the following should be noted:

$$N_A x_p = N_D x_n \quad (4.20)$$

It is possible to calculate the depletion width with respect to x_p and x_n by using equations (4.18) and (4.20). Hence,

$$x_p = \left(\frac{2\epsilon_s V_{bi}}{q} \frac{N_D}{N_A(N_A + N_D)} \right)^{\frac{1}{2}} \quad (4.21)$$

Similarly, x_n can be expressed as:

$$x_n = \left(\frac{2\epsilon_s V_{bi}}{q} \frac{N_A}{N_D(N_A + N_D)} \right)^{\frac{1}{2}} \quad (4.22)$$

In view of this, W (namely, the space-charge width in the p–n junction) can be obtained in the following way:

$$W = x_p + x_n = \left(\frac{2\varepsilon_s V_{bi}}{q} \frac{N_A + N_D}{N_A N_D} \right)^{\frac{1}{2}} \quad (4.23)$$

In equation (4.23), it is important to recognise that the doping density of the lightly doped side is what determines the depletion width. If $N_A \gg N_D$, it follows that $W \approx \left(\frac{2\varepsilon_s V_{bi}}{q N_D} \right)^{\frac{1}{2}}$. From this, one can conclude that the depletion region fraction is greater on the side of the junction with reduced doping (in the present case, on the junction's n-side). This is referred to as a one-sided abrupt p–n junction [3, 4].

In the case of a linearly graded p–n junction, Poisson's equation can be formulated as follows:

$$-\frac{d^2 V}{dx^2} = \left(\frac{d\varepsilon}{dx} \right) = \frac{\rho(x)}{\varepsilon_s} = \frac{q}{\varepsilon_s} [p(x) - n(x) + ax] \quad (4.24)$$

where a represents the doping gradient (measured in cm^{-3}).

With the implementation of comparable reasoning, it is possible to derive the built-in potential, V_{bi} , the electrical field, ε , and the depletion width, W , for a linearly graded p–n junction at thermal equilibrium. In view of this, ε of this junction is presented as follows:

$$\varepsilon(x) = -\frac{qa}{2\varepsilon_s} \left[\left(\frac{w}{2} \right)^2 - x^2 \right] \quad -\frac{w}{2} \leq x \leq \frac{w}{2} \quad (4.25)$$

In addition, the maximum electric field at the junction interface is given as follows:

$$|\varepsilon_m| = \frac{qaW^2}{8\varepsilon_s} \quad (4.26)$$

Furthermore, the built-in potential can be obtained in the following way:

$$|V_{bi}| = \frac{qaW^3}{12 \epsilon_s} \quad (4.27)$$

Finally, the depletion width, W , is given by:

$$W = \left(\frac{12\epsilon_s V_{bi}}{qa} \right)^{\frac{1}{2}} \quad (4.28)$$

4.1.1 THE P-N JUNCTION UNDER BIAS CONDITIONS

The non-equilibrium condition of the p–n junction occurs when an external bias is implemented between the p and n regions. This results in a situation in which the current begins to flow through the junction. The flow of the current is dependent upon the polarity of the external bias, and this can be characterised as either the forward bias condition or the reverse bias condition. It should be noted that the application of a reverse bias voltage results in the separation of charge carriers from the junction, meaning that the carriers encounter resistance when attempting to pass through the depletion region. As Figure 4.4(c) indicates, the reverse bias voltage condition involves an increase in the potential barrier across the junction to $(V_{bi} + V)$, while the width of the depletion increases such that the current flow across the junction decreases. In view of this, it is possible to state that the reverse bias condition is characterised by the flow of current only due to thermal effects. In contrast, Figure 4.4(b) indicates that the implementation of the forward bias voltage condition results in a reduced potential barrier across the junction to $(V_{bi} - V)$, thereby resulting in a reduction of the depletion width. This creates a situation in which the flow of current across the junction rises considerably. In the context of negligible bias, Figure 4.4(b) indicates that the Fermi level remains continuous across the junction, whereas in cases in which a forward bias voltage is applied to

the diode, E_{Fn} moves down to the half-occupancy equilibrium level for holes in the p region, and the converse takes place for E_{Fp} . It is noteworthy that, as a consequence of the recombination of carriers, the Fermi levels convene at a distance from the depletion region. In addition, Figure 4.4(c) indicates that, in the context of a reverse bias condition, the Fermi level in the n region is reduced compared to that of the p region [2].

When voltage reduction in the p and n quasi-neutral regions is neglected, and the solution of the Poisson's equation is modified at zero bias (see the previous section) with $(V_{bi} \pm V)$ instead of V_{bi} , it is possible to determine the depletion width for abrupt junctions under bias conditions in the following way:

$$W = \left(\frac{2\epsilon_s(N_A + N_D)}{qN_A N_D} (V_{bi} \pm V) \right)^{\frac{1}{2}} \quad (4.29)$$

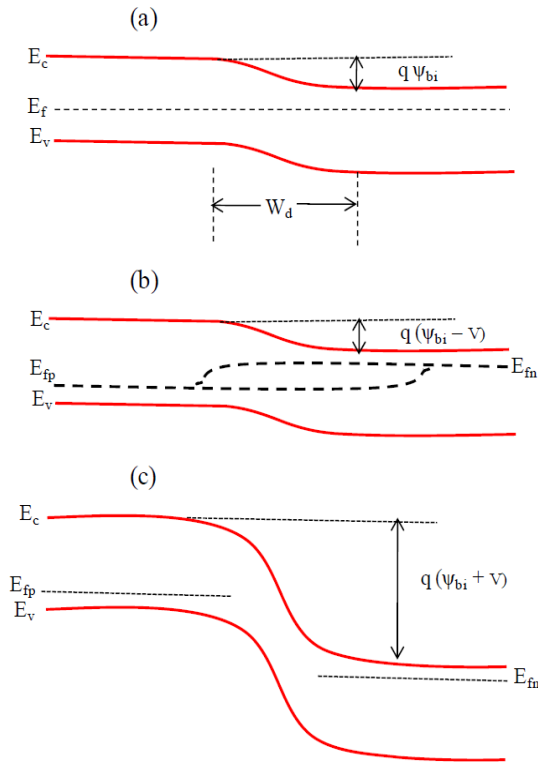


Figure 4.4: Energy band diagram of a p–n junction under (a) zero- bias, (b) forward bias and (c) reverse bias conditions.

The depletion width for the linearly graded junction under bias conditions is given below in a comparable manner:

$$W = \left(\frac{12\varepsilon_s}{qa} (V_{bi} \pm V) \right)^{\frac{1}{3}} \quad (4.30)$$

It should be noted that the plus-minus symbols in equations (4.29) and (4.30) are utilised to indicate reverse and forward bias conditions. In addition, if one supposes that $W \approx x_n$ and $x_n \gg x_p$, the approximation of the maximum electric field at a reverse bias for an abrupt junction is as follows:

$$\varepsilon_m = \frac{qN_D x_n}{\varepsilon_s} \approx \frac{2(V_{bi} - V)}{W} \quad (4.31)$$

Under comparable assumptions, the maximum electric field for a linearly graded junction at a reverse bias can be formulated in the following way [3, 4]:

$$\varepsilon_m \approx \frac{3(V_{bi} - V)}{2W} \quad (4.32)$$

The characterisation of the p–n junction is dependent upon the depletion capacitance of the space charge region.

4.2 DEPLETION LAYER CAPACITANCE

In this section, the depletion capacitance of the space charge region of a p–n junction will be discussed, because this parameter is significant to understand the characteristics of this junction. Another parameter is the built-in potential of a junction. This is defined by measuring the capacitance of a device as a function of reverse-bias voltages. Additionally, the carrier density profile of a Schottky diode

or p-n junction is estimated by using the capacitance-voltage analysis, which is a standard method [4].

According to reference [5], the p-n junction is a double layer of hole and electron charge carriers separated by the depletion region. The capacitance of the p-n junction diode can be regarded as the capacitance of a parallel plate capacitor, as given by the following:

$$C = \frac{dQ}{dV} = \frac{d(qN_A x_p)}{dV} = \frac{d(qN_D x_n)}{dV} \quad (4.33)$$

where dQ is the charge in the depletion region and dV is the applied voltage. Also, the capacitance of the parallel plate capacitor can be extracted as a function of the junction depletion width, W , as follows:

$$C = \frac{A\epsilon_s}{W} \quad (4.34)$$

where A is the area of the junction and ϵ_s is the dielectric constant of the semiconductor material [1, 4]. When applying a reverse bias and assuming $N_A \gg N_D$, equations (4.33) and (4.34) can be written as follows:

$$C = \frac{dQ}{dV} = \frac{A}{2} \left[\frac{2\epsilon_s q N_D}{V_{bi} \pm V} \right]^{\frac{1}{2}} \quad (4.35)$$

When this equation is applied, the capacitance decreases as the reverse bias increases. Also, it is possible to obtain the doping concentration (N_D) from the slope of the plot of $1/C^2$ versus V (reverse-bias voltage), as shown in Figure 4.5. The built-in potential (V_{bi}) can be obtained from the intercept at $1/C^2 = 0$ [2].

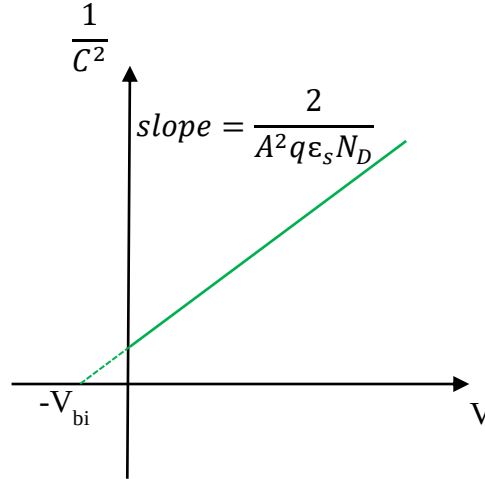


Figure 4.5: Plot of $1/C^2$ versus applied reverse-bias voltage for a one step-junction diode.

4.3 CURRENT- VOLTAGE CHARACTERISATION

The thermionic emission model with a series resistance (R_s) (see equation 4.36) is used to analyse the Schottky diodes or p-n junction current-voltage (I-V) characteristics [2]:

$$I = I_S \left[\exp\left(\frac{q(V - IR_S)}{nk_B T}\right) \right] \quad (4.36)$$

where q is the electronic charge, V is the applied voltage, k_B is the Boltzmann constant, n is the ideality factor, I_S is the saturation current, and T is the absolute temperature in Kelvin.

The experimental data is used to determine the values of n and I_S .

The saturation current I_S is expressed as follows:

$$I_S = AA^{**}T^2 \exp \frac{-q\phi_B}{kT} \quad (4.37)$$

where A is the diode area and A^{**} is the effective Richardson's constant for a semiconductor material, and ϕ_B is the barrier height.

The thermionic diode current for forward bias $(V - IR_S) \gg kT$ is given by:

$$I = I_S \left[\exp \left(\frac{q(V - IR_S)}{nkT} \right) \right] \quad (4.38)$$

By using the first derivative of I with respect to V (Equation (4.38)) will give:

$$dI/dV = 1 \left(\frac{q}{nkT} - \frac{qR_S}{nkT} \frac{dI}{dV} \right) \quad (4.39)$$

Using the above equation and substituting dI/dV with the conductance (G) the expression formula will be:

$$\frac{G}{I} = \frac{q}{nkT} - \frac{qR_S}{nkT} G \quad (4.40)$$

Figure. 4.6 shows the plot of the conductance divided by current (G/I) versus conductance (G). The parameters n and R_S can be obtained from the y-intercept and the slope, respectively.

This process of obtaining n and R_S experimentally is called Werner's method [6].

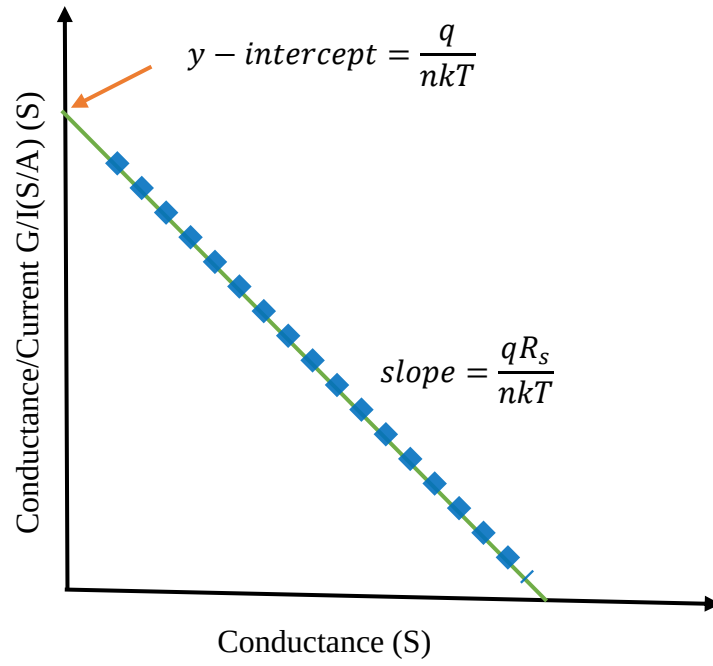


Figure 4.6: A model plot of G/I versus G used for extracting the I-V characteristics parameters.

I_s and ϕ_B can be determined by taking the logarithm of equation (4.36) as shown below:

$$\ln(I) = \ln(I_s) + \frac{q(V - IR_s)}{nkT} \quad (4.41)$$

Thus, the I_s value can be obtained from the y-intercept of the plot of $\ln(I)$ versus $(V - IR_s)$, and consequently ϕ_B can be calculated by using Equation (4.37).

4.4 DEEP LEVEL TRANSIENT SPECTROSCOPY (DLTS)

Various techniques are used for the microscopic analysis of deep level defects in semiconductors [7]. Deep Level Transient Spectroscopy (DLTS) [8], a powerful electrical technique, is used to investigate the electrically active defects and

determine their parameters. Lang discovered DLTS for the first time in 1974 [9]. This technique is based on the difference of the depletion width as a function of temperature. It applies the concept of space charge capacitance to obtain the activation energies and capture cross-sections of defects.

4.4.1 CAPACITANCE TRANSIENTS

The DLTS method needs a junction, such as a Schottky diode or a p-n junction device for the measurement of the capacitance transients which arise from the alteration in the space charge region. The charge occupancy changes of the defect level at different bias conditions in a Schottky diode are illustrated in Figure 4.7. The occupancy of the defects is disturbed by the periodic application of bias pulses to the diode. These are applied at a fixed repetition frequency. This process of applying the pulses between reverse bias V_R and filling bias V_P (where $V_P < V_R$) with a certain filling pulse width t_p is repeated.

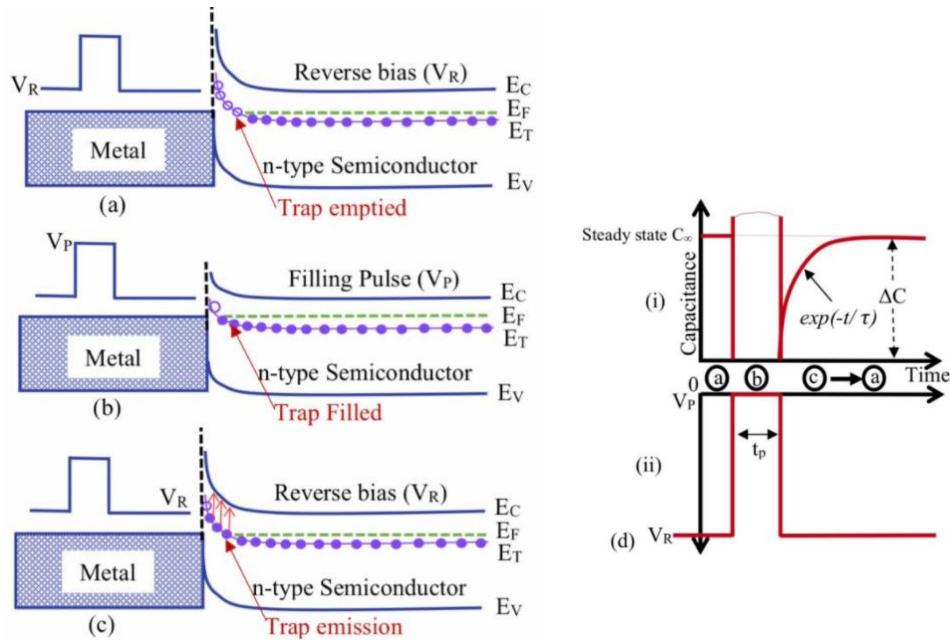


Figure 4.7: Diagrams of a Schottky diode displaying the charge possession changes of the defects level through (a) traps emptied on reverse bias ($V = V_R$), (b) traps filled on filling pulse ($V = V_P$) and (c) traps thermally emitting electrons during reverse bias ($V = V_R$), (d) DLTS pulse and the corresponding capacitance transient.

Figure 4.7 shows that in the stage (a) at the initial exposure of the junction to reverse bias V_R , establishment of a space charge region occurs. There are no charge carriers in the traps above the Fermi level, E_F , which are empty. Moving to stage (b), the width of the depletion region narrows on application of a filling pulse V_P . Therefore, the region that had earlier been emptied of carriers will experience an inflow of electrons from the conduction band and these will be captured by the region's traps (filled by carriers). If it is assumed that the process of electron capture is pure (i.e., no charge carriers emitted) and following the capture process kinetics given by Equation 3.5 in Chapter 3, the following rate equation is used to calculate the filled trap density:

$$\left(\frac{dn_T}{dt}\right) = (N_T - n_T) \quad (4.42)$$

where c_n , N_T and n_T represent the electrons' capture coefficient, total available number of trap states and number of trap states the electrons occupy, respectively.

The electron capture coefficient can be expressed by the following equation:

$$c_n = \sigma_n < v_{th} > n \quad (4.43)$$

in which σ_n represents the electron capture cross-section, $< v_{th} >$ represents the electrons' mean thermal velocity, and $n = N_d - N_T \approx N_d$ represents the effective doping concentration. When a filling pulse (t_p) of sufficient length is applied, electrons will totally fill the traps, making $n_T = N_T$. Nevertheless, in stage (c) the depletion region returns to the original width following re-establishment of the reverse bias, and therefore carriers will begin to be emitted by the filled traps. Corresponding emission rates can be found using the kinetics of the emission process:

$$\frac{dn_T}{dt} = e_p N_T - n_T (e_n + e_p) \quad (4.44)$$

in which e_n represents electron emission and e_p represents hole emission. If one assumes that the deep level is solely an electron interacting centre, the time dependences of n_T in the capture (Equation (4.42)) and emission (Equation (4.44)) phases are given by [10]

$$n_T(t) = N_n \{1 - \exp(-c_n t)\}, \quad c_n \gg e_n, e_p, c_p \quad (4.45)$$

and

$$n_T(t) = N_T \exp\left(-\frac{t}{\tau}\right), \quad e_n \gg c_n, e_p, c_p \quad (4.46)$$

where c_p is the capture coefficient of holes and τ is the inverse of the electron emission rate, i.e. $\tau = 1/e_n$.

Using this equation, it is found that there is an exponential trend in the reduction of filled trap concentration, which translates to a capacitance transient with a time constant τ as schematically illustrated in Figure 4.7 (d).

Fluctuations in the trap occupancy are susceptible to indirect measurement through monitoring capacitance fluctuations at the junction. Therefore, there is an added contribution to the total capacitance due to the filled traps $n_T(t)$ in the space charge region and Equation (4.35) can be expressed as:

$$C = \frac{dQ}{dV_R} = \frac{A}{2} \left[\frac{2\varepsilon_S q N_D^*}{V_{bi} + V_R} \right]^{1/2} \quad (4.47)$$

with $N_D^* = N_D - n_T$

When $n_T \ll N_D$, Equation (4.47) can be expanded, thus:

$$\Delta C = C_{\infty} \left(1 - \frac{n_T}{2N_D}\right) \quad (4.48)$$

with ΔC representing the capacitance transient's amplitude and C_{∞} the steady-state capacitance which can be expressed as:

$$C_{\infty} = \frac{A}{\sqrt{2}} \left[\frac{2\varepsilon_S q N_D^*}{V_{bi} + V_R} \right]^{1/2}$$

Through substitution of Equation (4.46) with Equation (4.48), the time dependence information for capacitance in majority carrier traps emission is given by:

$$\Delta C = C_{\infty} \left[1 - \frac{N_T}{2N_D} \exp\left(-\frac{t}{\tau}\right) \right] \quad (4.49)$$

Following from this, the deep level trap concentration can be determined by using the capacitance transient amplitude, and the electrons' emission rate using the time constant. Figure 4.8 illustrates the trap emission process as a function of temperature and the corresponding capacitance changes as a function of time.

It should be noted that with minority carriers traps, the capacitance transient sign opposes that of majority carrier traps.

4.4.2 CONVENTIONAL DLTS

The concept of a rate window is taken into consideration in the DLTS technique, where the capacitance of the depletion region is changed between two interval times, t_1 and t_2 ($t_1 < t_2$), for a p-n junction or a Schottky diode. Fundamentally, the DLTS signal $[S(t)]$ is the difference in capacitance $[\Delta C = C(t_1) - C(t_2)]$ as a function of temperature, and is given by the following expression:

$$S(T) = \Delta C = C(t_1) - C(t_2) = \Delta C_0 [\exp(-e_n t_1) - \exp(-e_n t_2)] \quad (4.50)$$

where e_n is the electron thermal emission coefficient in s^{-1} and ΔC_0 is the change in capacitance at $t = 0$ and is expressed by the following equation:

$$\Delta C_0 = \frac{C_\infty N_T}{2N_D} \quad (4.51)$$

where C_∞ is the capacitance at maximum reverse bias (V_r) (when the traps are empty). Using the inverse of the emission rate ($\tau = \frac{1}{e_n}$), Equation (4.50) can be rewritten as follows:

$$S(T) = \Delta C(t) = C(t_1 - t_2) = \Delta C_0 \left[\exp\left(-\frac{t_1}{\tau}\right) - \exp\left(-\frac{t_2}{\tau}\right) \right] \quad (4.52)$$

A maximum peak for $S(t)$ is obtained only when a transient occurs within the inverse of the emission rate [$\tau \approx (t_1 - t_2)$]. Nevertheless, the DLTS signal will be small if $\tau \gg (t_1 - t_2)$ or $\tau \ll$

$(t_1 - t_2)$, as presented in Figure 4.8(a) [9]. If $S(T)$ is at its maximum, equation (4.52) can be differentiated, and the result can be set to zero [$dS(T)/d\tau = 0$] to get the maximum of the inverse of emission ($\tau_{\max}$):

$$\tau = \tau_{\max} = \frac{(t_2 - t_1)}{\ln\left(\frac{t_2}{t_1}\right)} \quad (4.53)$$

Equation (4.53) is known as the ‘rate window’. The value of the rate window may be changed by changing the values of t_1 and t_2 , which will produce different maximum DLTS peaks at different temperatures, as demonstrated in Figure 4.8(b). The Arrhenius plot of the emission rates (of DLTS peaks) as a function of temperature is used to determine the trap activation energy, as seen in Figure 4.8(c). Therefore, the activation energy, E_T , and apparent capture cross-section, σ_n , of the

trap can be obtained from the slope and intercept of the Arrhenius plot, respectively. Additionally, the trap concentration, N_T can be determined by Equation (4.51), where ΔC_0 corresponds to the conventional DLTS peak amplitude.

Generally, the DLTS signals depend on the ratio t_2/t_1 but not on their absolute values.

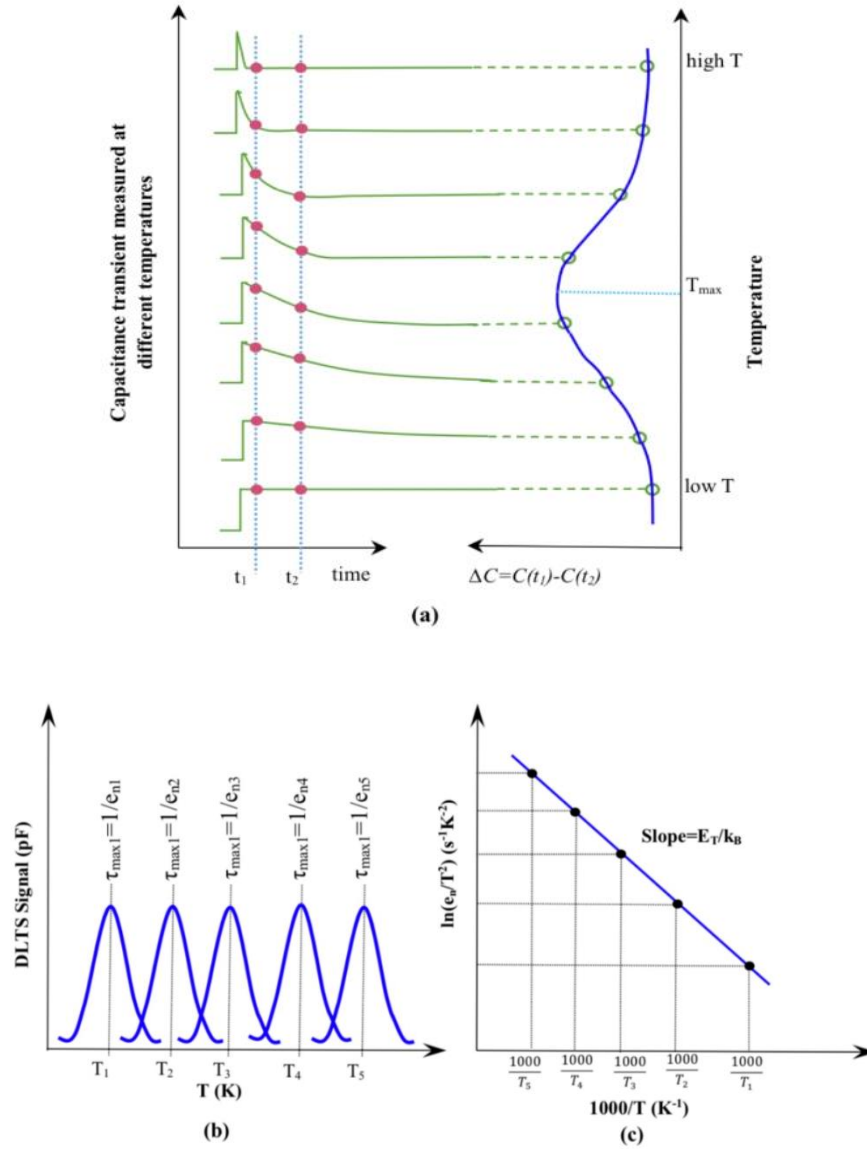


Figure 4.8: (a) Generation of a DLTS signal using one rate window, (b) DLTS signals at different rate windows and (c) Arrhenius plot of DLTS peaks.

4.5 LAPLACE DLTS SPECTROSCOPY

Despite the efficiency of DLTS for studying deep-level defects, there are some issues that influence its resolution. One of the hindrances of DLTS is the difficulty of accurately measuring temperature during a thermal scanning process. Increasing or lowering the temperature results in an inaccurate measurement of the traps' activation energies. The resolution of the time constant is also problematic as DLTS cannot distinguish among closely spaced defects with comparable emission rates. This poor resolution results in a broad peak on the DLTS spectrum [11]. The LDLTS technique is utilised to reduce the problems associated with conventional DLTS. LDLTS is an isothermal technique in which a diode remains at a fixed temperature during the measurement process. It takes into consideration the capacitance transients to be characterized by a spectrum of emission rates, during which the recorded transient $[f(t)]$ is provided by the following expression:

$$f(t) = \int_0^{\infty} F(s) \exp^{-st} ds \quad (4.54)$$

where $F(s)$ is the spectral density function. Equation (4.54) represents the transient capacitance as the Laplace transform of the actual spectral density function, $F(s)$. The capacitance transient obtained from LDLTS measurements can be seen in Figure 4.9(a). The real spectrum of emission rates within the transient is attained by applying the relevant mathematical algorithm, which performs an inverse Laplace transform for the recorded capacitance transient [12]. The LDLTS technique uses three main algorithm routines—FLOG, CONTIN and FTIKREG—to solve equation (4.54) [13] and achieve a spectrum of delta-like peaks (Figure 4.9[b]).

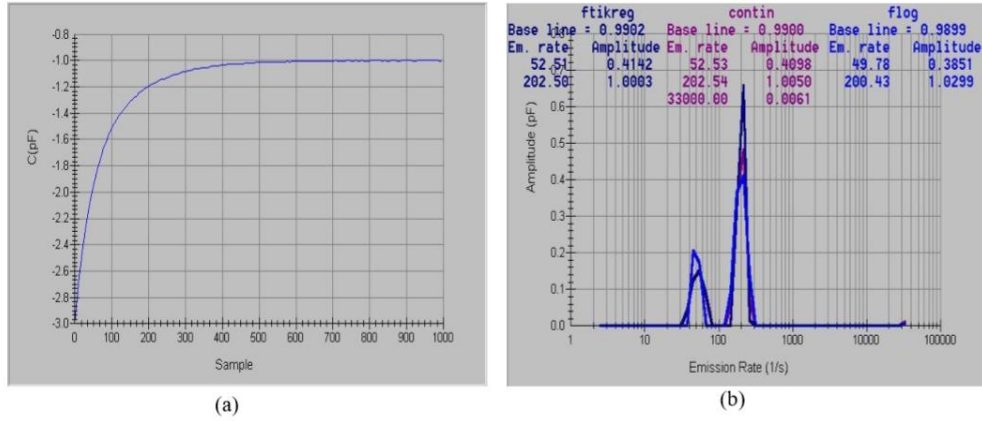


Figure 4.9: (a) Capacitance transient obtained by LDITS and (b) a spectrum of delta-like peaks.

4.6 HARDWARE OF THE DLTS SYSTEM

4.6.1 DESCRIPTION OF SYSTEM HARDWARE

This section covers the main experimental setup used to perform the conventional DLTS and Laplace DLTS measurements. This system consists of the following equipment: (i) Janis cryostat and temperature controller, (ii) Capacitance meter, (iii) Current-Voltage meter, and (iv) Data acquisition and BNC connectors box for analogue Input (I)/Output (O).

A computer controls all this equipment via a GPIB interface. Figures 4.10 and 4.11 illustrate a photograph and a block diagram of the DLTS and Laplace DLTS system, respectively.

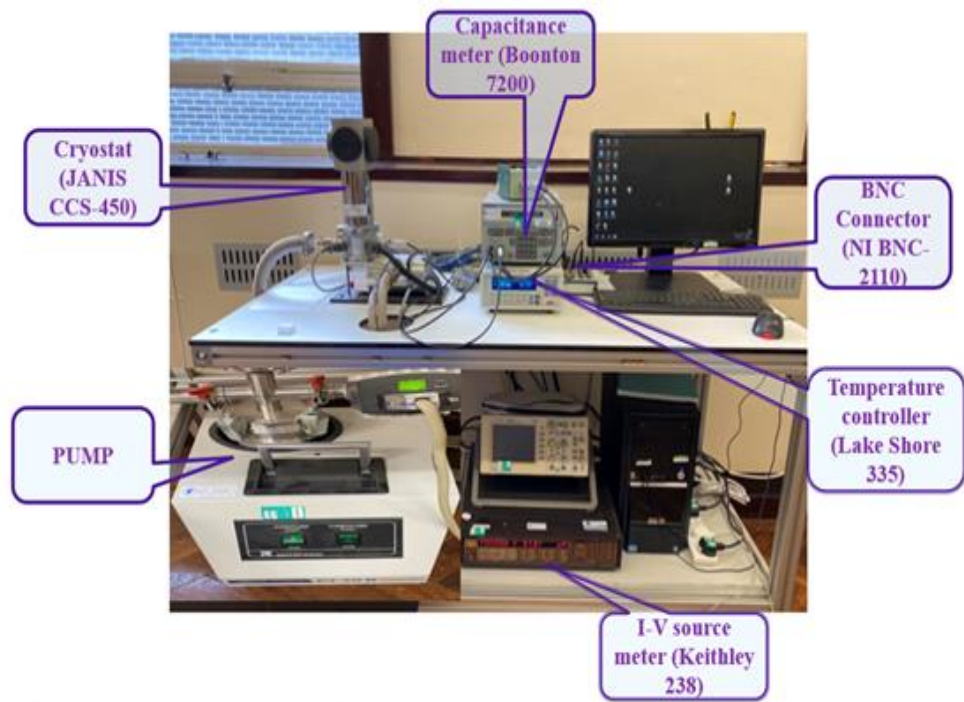


Figure 4.10: Photograph of the DLTS system showing (i) Janis cryostat and temperature controller for monitoring the sample temperature (ii) Capacitance meter for DLTS/LDLTS and standard C-V measurements, (iii) Current-Voltage meter to determine the diode parameters, and (iv) Data acquisition and BNC connectors box for analogue Input (I)/Output (O). Prior to cooling down the samples, the cryostat was evacuated to a low enough pressure by a pumping system.

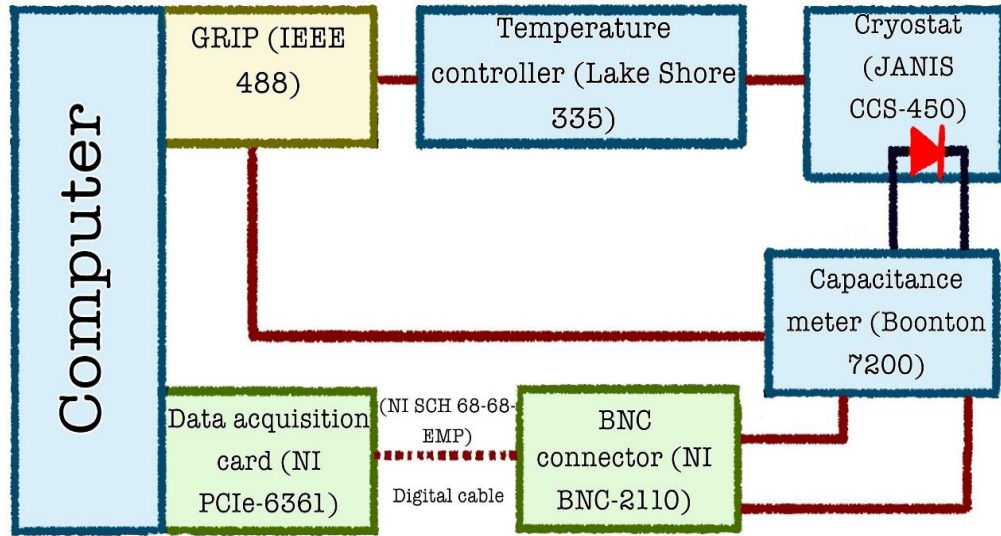


Figure 4.11: Block diagram of DLTS and Laplace DLTS system for data collection using a high-speed general-purpose interface bus (GPIB) allowing the equipment to be controlled using a dedicated software.

4.6.1.1 CRYOSTAT AND TEMPERATURE CONTROLLER

The means whereby charge carriers are emitted from the traps is dependent on thermal energy. Therefore, for the DLTS and Laplace DLTS measurements the sample temperature was controlled with a temperature controller (Model Lake Shore 331) and monitored using a cryostat (Model Janis CCS-450). The cryostat system's internal structure is illustrated in Figure 4.12. Specifically, this system comprises (i) a sample holder linked with a cold finger, (ii) electrical ports for sample contacts, (iii) temperature sensors, (iv) aluminium vacuum shroud and (v) a radiation shield.

The cryostat works in conjunction with a compressor that employs a closed-cycle refrigeration system supplying helium gas (He) continuously via a highly efficient and flexible cryogen transfer line 6 feet in length. The sample temperature can be

controlled in the range between 10 K - 450 K with an accuracy of ± 1 K. The temperature controller is connected to two temperature sensors, one of them is placed as close as possible to the sample to get the most accurate temperature readings.

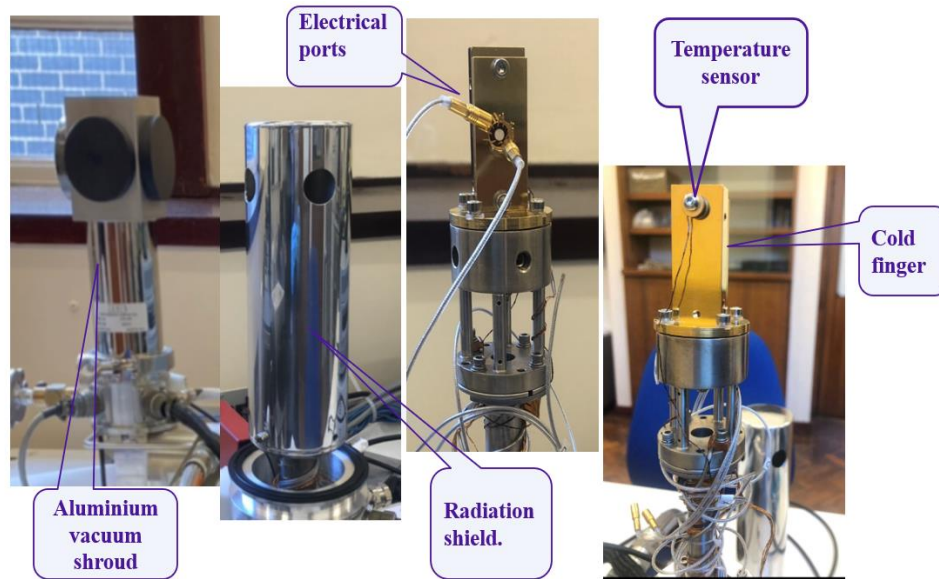


Figure 4.12: Photograph showing different components of the cryostat.

4.6.2 CAPACITANCE METER

A high response time capacitance meter is used to obtain the capacitance transients. The capacitance Boonton 7200 meter with a response time of $\sim 120 \mu\text{s}$ was used for both DLTS/LDLTS and standard C-V measurements at different temperatures. It must be mentioned that this measuring device has a fixed sampling frequency of 1 MHz

4.6.3 CURRENT-VOLTAGE SOURCE METER

In order to determine the diode parameters such as ideality factor (n), barrier height (ϕ_b) and series resistance (R_s), the current-voltage (I-V) measurements have been

performed. In this study, only samples with low leakage currents in the range of μA are used in the DLTS and Laplace DLTS measurements.

The I-V measurements were performed by using Keithley 236 current meter which is controlled by computer software via GPIB interface. This meter provides a source voltage in the range of 100 μV to 110 V with a sensitivity of $\pm 10 \mu\text{V}$ and a source current in the range of 100 fA to 100 mA, with a sensitivity of 10 fA.

4.6.4 DATA ACQUISITION AND BNC-2100 CONNECTOR

A National Instruments (NI) data acquisition (DAQ) card is employed to allow for biasing and pulsing of the diodes. The card can be used to apply an input voltage of maximum $\pm 10.0\text{V}$ with a pulse width of 0.5 μs to the samples. The interface of the NI card and the BNC-2110 connector box is achieved using the SHC68-60-EPM matching cable. Data is collected from the diode and sent to be processed by a computer via the BNC-2110 connector box.

4.6.5 COMPUTER INTERFACE

All equipment used in the experiment are connected to the computer using high-speed general-purpose interface bus (GPIB) allowing the equipment to be controlled using a dedicated software.

4.7 SYSTEM SOFTWARE

Development of the Laplace DLTS software occurred through the shared project “Copernicus Project CIPA CT-94-0172 and The Foundation for Polish Science

Serial No: C3.2.041” between Institute of Physics Polish Academy of Sciences, Warsaw, Poland (Prof. L. Dobaczewski) and University of Manchester (Prof. A. R. Peaker). The software functions in both Laplace DLTS and standard DLTS modes, as detailed below.

4.7.1 CONVENTIONAL DLTS MEASUREMENTS MODE

Sample scanning is achieved in conventional DLTS measurement mode with continuous scanning and temperature variations. Generally, the temperature is set with predetermined boundaries, moving from one to the other in incremental steps of 2K/minute. This measurement may be undertaken by employing the Exponential Fitting, Trap View, and Multi-Rate Window modes. All of these modes employ rate window principle. For the “Multi-Rate” mode, nine different rate windows can be recorded, namely 5 s^{-1} , 10 s^{-1} , 20 s^{-1} , 50 s^{-1} , 100 s^{-1} , 200 s^{-1} , 500 s^{-1} , 1000 s^{-1} and 2000 s^{-1} . In the “TrapView” mode, a single pair of five different pair options of rate windows can be selected at any one point: $(4, 10\text{ s}^{-1})$, $(20, 50\text{ s}^{-1})$, $(80, 200\text{ s}^{-1})$, $(400, 1000\text{ s}^{-1})$ and $(2000, 5000\text{ s}^{-1})$. However, in the “Exponential Fitting” mode, a single rate window can be selected from five rate windows ($10, 20, 50, 100$ and 200 s^{-1}). When the measurements are taken in “Exponential Fitting” mode, the Arrhenius plot is established. This allows an estimation of the activation energies and capture cross-sections of the defects. Additionally, this mode may also be activated in lock-in mode, which offers superior resolution compared to rate window mode. Nevertheless, the lock-in mode offers an inferior signal to noise ratio.

It should be noted that the DLTS experimental parameters, such as temperature range, pulse duration, forward and reverse bias, may be remotely set in every mode.

4.7.2 LAPLACE TRANSIENT PROCESSING MODE

In this mode the sample is kept at a fixed temperature when the measurements are taken. This mode is employed to enhance the signal to noise ratio. Three algorithms are applied for generation of Laplace DLTS signals (FLOG, CONTIN and FTIKREG).

4.8 PHOTOLUMINESCENCE

Photoluminescence (PL) spectroscopy is an efficient, contactless and non-destructive technique which is widely used to investigate the optical properties of semiconductor materials. The technique involves exposing the semiconductor material under investigation to a high photon density employing laser beams. The photons, upon absorption, will cause excess energy into the material via the process known as photo-excitation. Ultimately the semiconductor material will emit the extra energy as light due to the recombination of the carriers which can occur via either radiative or non-radiative processes. If radiative relaxation occurs, the emitted light is called PL. The intensity and spectral content of emitted light provides crucial data regarding the properties of the semiconductor material that has been subjected to the external excitation. Once electrons revert to the equilibrium state having been stimulated to states of greater allowable energy through the photo-excitation processes, the energy is released either as light (radiative process) or heat (non-radiative process). It should be noted that the emitted light's energy is related to the transition energy between the equilibrium state and the excited state. The PL spectrum provides the transition energies, which can be used to determine the electronic energy levels. The PL intensity gives a measure of the relative rates of radiative and nonradiative recombination. The

intensity and full width at half maximum (FWHM) of the PL signal provides information on the quality of the sample. Figure 4.13 (a) shows how photons are absorbed followed by electron hole pair creation. Figure 4.13 (b) illustrates how non-equilibrium electrons and holes relax down to an equilibrium state, i.e. to their band edges. Finally, the electron–hole recombination and photon production are shown in Figure 4.13 (c).

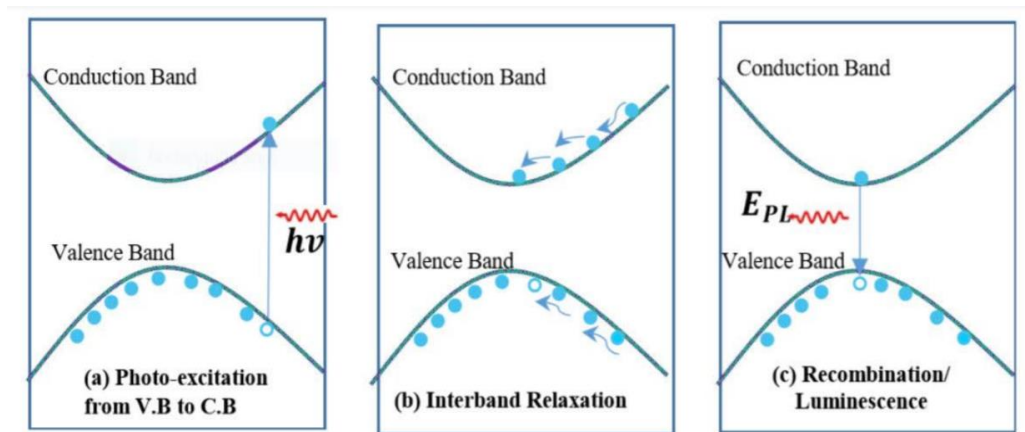


Figure 4.13: Schematic illustration of the basic processes involved in Photoluminescence (PL)

4.8.1 SYSTEM HARDWARE IMPLEMENTATION

In this section, the important elements of the PL system used in this study are described briefly. The PL system is capable of operating over the temperature range 10K-300K. Figures 4.14, 4.15 and 4.16 show the block diagram and images of the PL system.

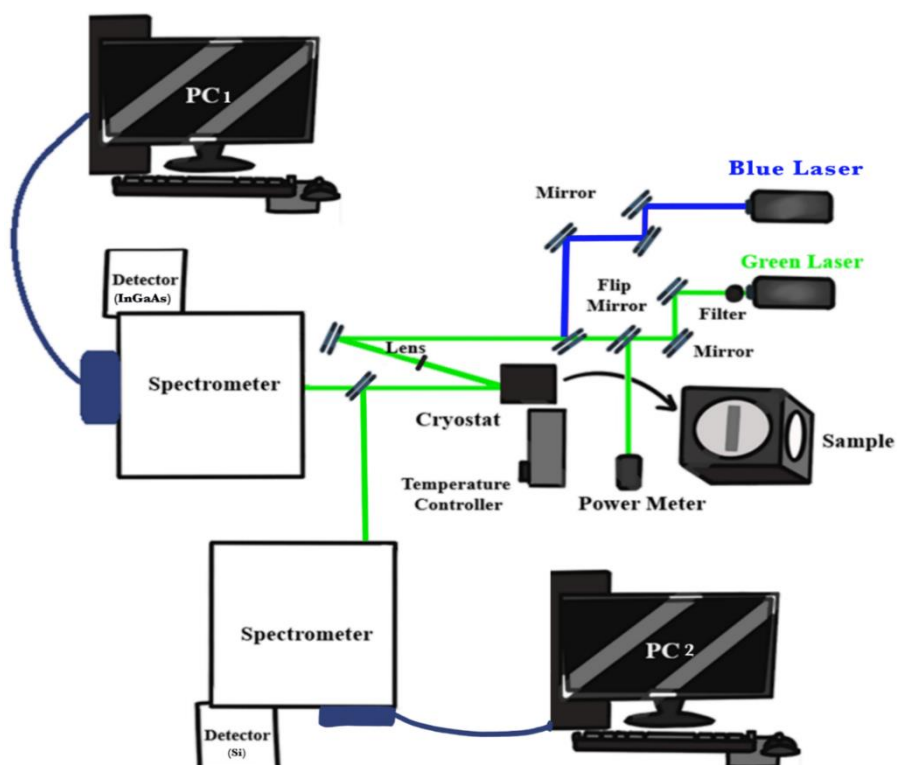


Figure 4.14: A diagram of the photoluminescence (PL) equipment.

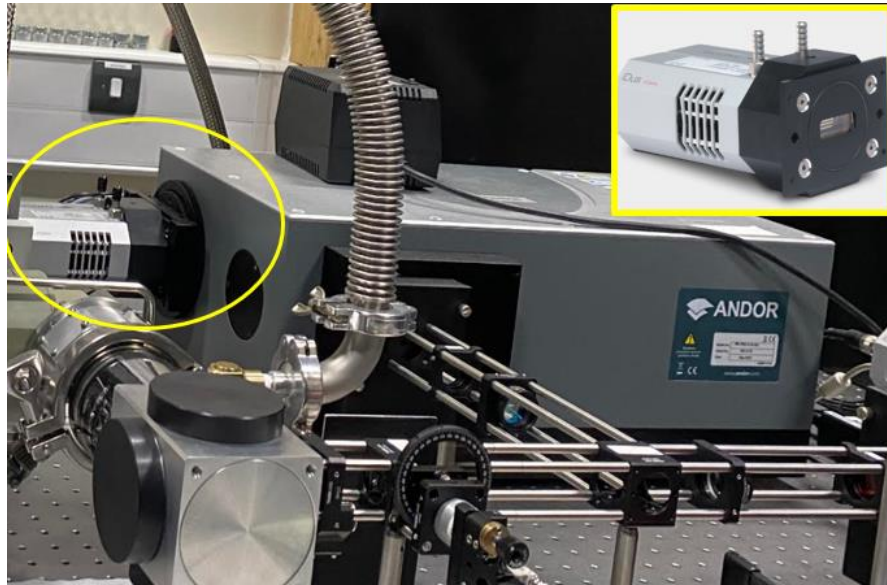


Figure 4.15: Picture of the Andor Shamrock 500i spectrometer with InGaAs detector.

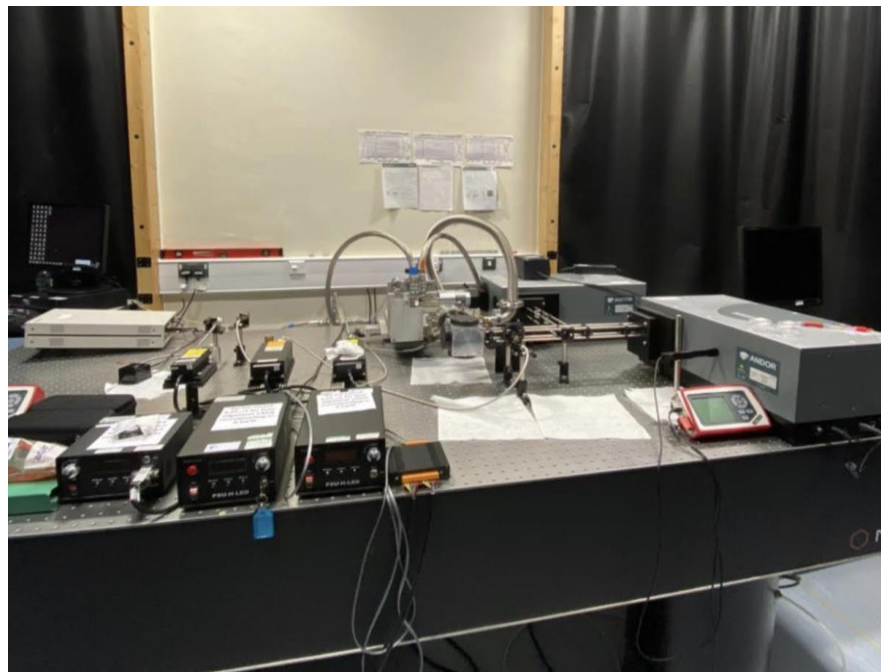


Figure 4.16: Photograph of the photoluminescence (PL) equipment showing two Andor Shamrock 500i spectrometers connected to InGaAs and Si CCD detectors.

4.8.1.1 SPECTROMETER AND DETECTORS

The emitted photoluminescence was dispersed by a grating spectrometer to allow for spectral analysis. The Shamrock 500i spectrometer from Andor has a focal length of 500mm and an aperture of F/6.5. The spectrometer has a CCD camera detector which converts incident photons to electronic signals in order to cover a wide range of wavelengths. This is positioned at the exit of the spectrometer. The PL system has the high sensitivity InGaAs and Si detectors that can cover the optical ranges ~900-1700 nm and ~350-950 nm, respectively (see Figure 4.15). In this study, the InGaAs detector was used.

4.8.1.2 LASERS AND OPTICS

The PL system uses two sources of excitation which are mainly blue and green lasers. A neutral density filter can be used to manually change the laser power incident on the sample. Moreover, to stop unwanted high-order lines from the laser light, a bandpass filter is positioned in the laser light path. The PL system has a number of optics including lenses and reflectors which are used to focus the light onto the sample and to focus the PL signal on the entry slit of the spectrometer are illustrated in Figure 4.14.

4.8.1.3 CRYOSTAT AND TEMPERATURE CONTROLLER

For the temperature-dependent PL measurements, a state-of-the-art helium gas (He) closed-cycle cryostat similar to the one discussed in section 4.6.1.1, model Janis CCS-150 operating in the range 10K-300K was used. The sample temperature was controlled with a temperature controller model Lake Shore 331.

4.8.1.4 COMPUTER INTERFACE

The spectrometer and CCD cameras are interfaced with a computer using Windows 10 via USB ports.

4.8.1.5 SYSTEM CONTROLLING SOFTWARE

Solis was used, which is Andor's CCD cameras and spectrometer system control software. It includes a range of functions for data acquisition and for monitoring and controlling the different components of the PL system. For example, the software can control the turret, which has three gratings, side input slits, and shutters.

In this chapter, accounts of the fundamental properties of p-n and Schottky diodes, the I-V, C-V, DLTS, Laplace DLTS and PL techniques used to investigate the electrical and optical properties of the samples, and the hardware and software to implement these techniques are given.

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CHAPTER 5: EXPERIMENTAL DETAILS

The aim of this chapter is to provide a brief description of the samples, which are used in this study. Additionally, the experimental techniques employed to investigate the devices such as current-voltage (I-V), capacitance-voltage (C-V), conventional DLTS and Laplace DLTS are presented.

5.1 SAMPLES USED IN THIS STUDY

The central motivation of this thesis is to investigate the electrically active defects in different semiconductor materials and devices such as photovoltaic (solar cells) and laser structures with embedded quantum dots, and their effects on the electrical and optical properties of these devices.

Two different types of semiconductors materials have been studied with different structures in this thesis:

- 1- Intermediate Band Solar Cells (IB-SC) p-i-n structures based on GaAs and InAs quantum dots (QDs) grown at different growth temperatures. This study improved the understanding of the physical phenomena that affect the efficiency of these solar cells.
- 2- InAs/InGaAs QDs laser structures grown on GaAs and Si substrates. The aim was to determine the effect of the substrate on the electrical and optical properties of the laser diodes.
- 3- InAs/InGaAs QDs laser structures grown on GaAs and Si substrates were irradiated with a gamma (γ -) cell Cobalt Irradiator (dose rate of 5.143

KGy/hour) at a high dose of 50 kGy to study the effect of γ -irradiation on post-irradiation stability of the electrical properties of these devices.

The growth details and layer structures of each sample are given in each related experimental chapter.

5.2 MEASUREMENT DETAILS

This section presents details of all the measurements employed in this thesis.

5.2.1 I-V MEASUREMENTS

Since the DLTS and Laplace DLTS (LDLTS) techniques are based on the transient of the capacitance, the devices should have low leakage currents in the range of μA or below in order to perform DLTS and LDLTS measurements.

A Keithley 235 source measure unit was used to measure the I-V characteristics of the devices. This unit was controlled by computer software via GPIB interface.

The reverse biases ranged from -1V up to -6V depending on the quality of the diodes with increment of 10 mV. Additionally, the I-V measurements as a function of temperature were also performed in order to study the temperature dependence of the diode parameters as described in Chapter 4.

5.2.2 C-V MEASUREMENTS

The C-V measurements were considered in detail in Chapter 4. The C-V characteristics are important for determining the built-in voltage, the background doping concentration, depletion layer, interface states and concentration depth

profile of the semiconductor materials and devices. The C-V characteristics for all samples investigated in this thesis were obtained using a Boonton 7200 capacitance meter operating at a fixed frequency of 1MHz and controlled by a computer.

5.2.3 DLTS MEASUREMENTS

The electrical active defects detected in the material systems and devices investigated in this thesis were characterised by DLTS and Laplace DLTS techniques, which were discussed in detail in Chapter 4. The samples were first processed into circular mesas with different diameters and mounted on 12 pin TO5 headers. These were then fitted into a sample holder inside a He-closed cycle refrigerator, Model number CCS-450 cryostat. The samples were first cooled down to a temperature of 10K and then the DLTS measurements started by ramping the temperature at a rate of 2K/min up to around 450K. A pulse generator (National instrument Box) generated a train of electrical pulses, which were applied to the sample. A Boonton 7200 capacitance meter was used to record the capacitance transients, which were stored in a computer as a DLTS signal at the chosen reverse bias (V_R) and filling pulse (V_P).

5.2.4 LAPLACE DLTS MEASUREMENTS

The isothermal Laplace DLTS method, which was described in detail in Chapter 4, was used to resolve broad peaks typically obtained in conventional DLTS. In this technique, the temperature is fixed during the measurements, which are carried out within a range of temperatures where the DLTS peak is detected.

5.2.5 PHOTOLUMINESCENCE MEASUREMENTS (PL)

PL spectroscopy is a well-known technique that is commonly used to probe the electronic structure of semiconductor materials. It is a contactless and non-destructive method.

Low temperature photoluminescence measurements as described in Chapter 4 have been performed using a He-closed-loop cryogenic PL system, which operates in the temperature range ~ 10 K - 300 K. The excitation light was generated using a solid-state green laser having a wavelength $\lambda = 532$ nm. Briefly, the sophisticated PL system consists of an Andor Shamrock 500i spectrometer which has a focal length of 500mm and an aperture of F/6.5. The spectrometer covers the Near-infrared (NIR) wavelength range from 900-2300nm and is fitted with a high sensitivity Si (~ 350 -950 nm) and InGaAs (~ 900 -1700 nm) CCD camera to cover the visible to mid-infrared bands.

CHAPTER 6: INVESTIGATION OF ELECTRICALLY ACTIVE DEFECTS IN InAs QUANTUM DOTS INTERMEDIATE BAND SOLAR CELL USING DEEP LEVEL TRANSIENT SPECTROSCOPY TECHNIQUE

This chapter presents a comprehensive study into the effects of electrically active defects on the electrical properties of a set of intermediate band solar cell (IBSC) grown by Metal Organic Vapour Phase Epitaxy (MOVPE) using Current - Voltage (J-V), Capacitance - Voltage (C-V), conventional Deep Level Transient Spectroscopy (DLTS) and Laplace DLTS measurements in the temperature range between 10 and 450K.

6.1 INTRODUCTION

The intermediate band solar cell (IBSC), which is a novel photovoltaic concept introduced by Luque et al. (1997), was designed to exceed the performance of single gap solar cells [1]. It was predicted that the efficiency of solar cell devices would increase from 40.7% to 63.1% according to the Shockley and Queisser model limit, which is based on single-gap solar cells [2, 3]. Figure 6.1 shows the principle of quantum dot IBSC (QD IBSC), which depends on the intermediate band (IB) of the material located between the conduction band (CB) and valence band (VB) in a semiconductor [4]. The IB is also present in low-dimensional structure materials such as QDs. IBs allow for the generation of electron-hole pairs. In this technique, an electron that does not have enough energy to be excited from the VB to the CB can move from the VB to the IB, and then from the IB to the CB [4].

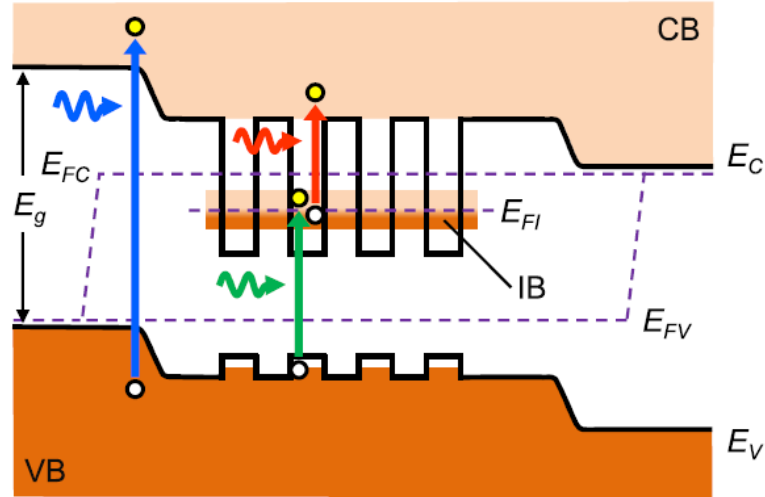


Figure 6.1: Energy band diagram of a QD IBSC [5]. An IB solar cell's photon absorption mechanism and quasi-Fermi level split. CB, VB and IB are the conduction band, valence band and intermediate band, respectively. E_C and E_V are the energy of the conduction band and valence band, respectively. E_g and E_{FI} are the energy gaps of the host material and the quasi-Fermi level of QD IBSC, respectively. E_F is Fermi level and E_{FV} and E_{FC} are quasi-Fermi levels. The arrows indicate the photon absorption processes in QD IBSC.

The significant feature of IBSC compared with conventional single-junction solar cells is that the electron-hole pair is created by the mid-gap intermediate band, because IBSC permits two sub-bandgap photons to create this pair. However, the QD technique enables absorption of a single high-energy photon that generates multiple electron-hole pairs (excitons) in QDs with low-energy band gaps, which in principle produces quantum efficiencies over 100% [6].

In the IBSCs structure, within the bandgap of a semiconductor material, an energy band is created which leads to allowing sub-bandgap absorption and thus increasing the short circuit current (I_{sc}) without substantially lowering the open circuit voltage (V_{oc}). A portion of the solar spectrum's photons with energies below the matrix

material bandgap are absorbed. Electrons are promoted from the valence band to the intermediate band, and from the intermediate band to the conduction band, thus raising I_{sc} , whereas the matrix (host) material bandgap determines the V_{oc} ultimately. Nevertheless, despite significant progress in recent years [4, 5, 7, 8] the experimentally obtained efficiencies for IBSCs are still some way from the theoretically expected values.

The QD technique is one of the most important approach used to fabricate IBs for use in IBSCs [1]. Luque and Marti explored the feasibility of fabricating IBSCs and of engineering the IB using QD theory [3, 4]. They found that the important fundamental concepts of IBSC is the photocurrent that can be generated from the absorption of below band-gap energy photons and the population of electrons in each band which is best represented by its own quasi-Fermi level. The quasi-Fermi level of IB materials is measured between the VB and CB [3, 4].

The intermediate band can be created in a variety of ways, including the incorporation of a high concentration of impurities [9, 10], or through the use of quantum dot (QD) layers [11], where the intermediate band is formed through the electronic ground state of the QDs. In general, QD-IBSCs use InAs quantum dots embedded in GaAs layers. Although the optical transition energies provided by this device are not optimal for maximum energy conversion efficiency as it is still in its infancy [12], QD-IBSCs with figures of merit equal to or better than an equivalent cell without the intermediate band have already been realised.

While silicon solar cells are widely used for terrestrial applications, GaAs-based solar cells are preferred in industry as they have higher efficiencies, and they are more radiation resistant in space than silicon. An additional advantage of using

higher efficiency GaAs solar cells in space is the reduction of size and weight of spacecraft, and consequently, cost of the solar panels [13, 14].

InAs/GaAs QDs are widely regarded as holding significant promise for the implementation of IBSCs, which have gained much interest as possible candidates of the next generation of photovoltaic technology. By allowing an extra optical transition utilising a band of electron states inside the bandgap energy, they can attain greater conversion efficiency than traditional single gap solar cells [15, 16]. Past investigations into InAs/GaAs QD solar cells have demonstrated that they also offer an improvement in an extended photo-response in comparison to GaAs solar cells with identical structure [17, 18]. However, imperfections in the QD layers can reduce the open-circuit voltage (Voc), thereby nullifying any improvements in efficiency that are achieved through the use of QDs [17, 19]. These imperfections in the QD layers are caused by cumulative strain that develops as the multilayers of InAs/GaAs QDs are grown. This strain is caused by the lattice mismatch between GaAs and InAs [17, 20]. To create highly efficient QD solar cells, this cumulative strain must be reduced in order to prevent imperfections in the QD layers. For example, IBSC QDs developed using InAs/GaAs QDs led to a 50% increase in power conversion efficiency [21].

Defects affect the optical and electrical properties of electronic devices, especially solar cells, as well as the conversion efficiency of semiconductors. For example, Schmieder et al. [22] recently demonstrated that the EL2 defect, an As_{Ga} antisite associated with another point defect [23-26], reduces the solar cell efficiency in GaAs solar cells.

In this Chapter the effects of the growth temperature and i-region on the electrical

properties of a set of p-i-n quantum dots intermediate band solar cells (QD-IBSCs) grown by Metal Organic Vapour Phase Epitaxy (MOVPE) at Pontifical Catholic University of Rio de Janeiro in Brazil, are investigated by utilizing conventional current-voltage (I-V), capacitance-voltage (C-V), deep-level transient spectroscopy (DLTS) and Laplace DLTS (LDLTS) techniques.

The results are presented in three sections. Firstly, a study of the effect of the growth temperature (T_g) of the GaAs spacer layer (see Figure 6.2 a) on the electrically active defects in two QD-based IBSC solar devices, namely QD6-700 ($T_g = 700$ °C) and QD 6-630 ($T_g = 630$ °C). Secondly, an investigation of the impact of the thickness of the GaAs capping layer (h_{CL}) on the electrically active defects in QD 6-700 ($h_{CL} = 6$ nm) and QD 3-700 ($h_{CL} = 3$ nm) devices (see Figure 6.2 a). Finally, a study of the effect the growth temperature on the electrically active defects in control samples where the active layer is just GaAs (i.e. without QDs) but with the same thickness as that of the QD-IBSC, namely structures SC-630 ($T_g = 630$ °C) and SC-700 ($T_g = 700$ °C) (See Figure 6.2 b), and SCycle where the active layer was grown by periodically changing the growth temperature between 490 °C and 700 °C, similar to the temperature cycle used for the deposition of QDs in structures (See Figure 6.2 c).

This study will help to get a better understanding of the physical phenomena that affect the efficiency of the above solar cell structures.

6.2 THE SAMPLES

6.2.1 SAMPLE GROWTH DETAILS AND STRUCTURES

Metalorganic vapour phase epitaxy (MOVPE) was used to grow three series of structures on (001) GaAs substrates in an Aixtron AIX 200 reactor at 100 mbar. All

samples have similar structures except the i-region (active region) as shown in Figure 6.2.

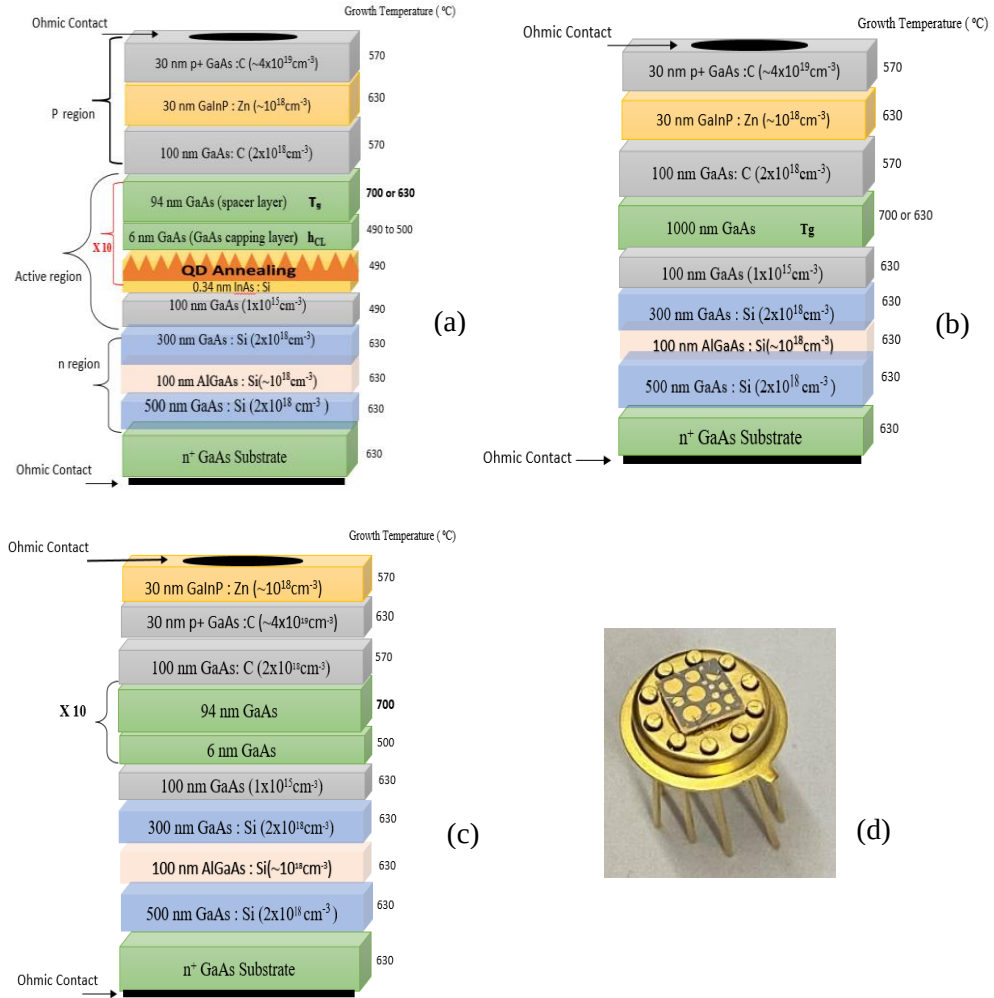


Figure 6.2: Schematic diagrams of three different series of structures investigated. (a) first series consists of three InAs QD-IBSC p-i-n structures, namely QD3-700, QD6-700 and QD6-630, where T_g is the growth temperature of the 94nm GaAs spacer layer (630 or 700 °C) and h_{CL} is the GaA capping layer thickness (3 or 6 nm). (b) Second series consists of two similar structures as (a), labelled SC-630 ($T_g = 630$ °C) and SC-700 ($T_g = 700$ °C), where the active layer is just GaAs (i.e. without QDs) but with the same thickness as that of the QD-IBSC structures. (c) series three consists of only one sample, SCycle, where the active layer was grown by periodically changing the growth temperature between 490 °C and 700 °C, similar to the temperature cycle used for the deposition of QDs in structures shown in (a). (d) Photograph of samples mounted on TO5 header.

Aluminium, gallium, indium, and arsenic were generated using trimethylaluminum (TMAl), trimethylgallium (TMGa), trimethylindium (TMIn), and arsine (AsH₃) or tributylarsenide (TBAs), respectively. The p-doping sources were CBr₄ and dimethylzinc (DMZn), whereas the n-doping source was SiH₄.

All p-i-n samples were grown on n-type GaAs substrates. The n-region consisted of a 500 nm GaAs/100 nm AlGaAs/300 nm GaAs layers doped with silicon (Si) ($\sim 1\text{-}2 \times 10^{18} \text{ cm}^{-3}$). This was followed by a 100 nm undoped GaAs layer (background doping = $1 \times 10^{15} \text{ cm}^{-3}$), which was used as a spacer layer between the n-region and the i-region. All layers were grown at 630 °C.

The top p-region consisted of also three layers: a 100 nm GaAs layer doped with carbon (C) ($2 \times 10^{18} \text{ cm}^{-3}$) grown at 570 °C, a 30 nm GaInP layer doped with zinc (Zn) ($\sim 10^{18} \text{ cm}^{-3}$) grown at 630 °C, referred to as optical window, and a 30 nm GaAs layer doped with C ($\sim 4 \times 10^{19} \text{ cm}^{-3}$) grown at 570 °C.

The significant difference between all three series of samples is the composition and growth temperature of the i-region (active region). The first series, shown in Figure 6.2 (a), consists of three InAs QD-IBSC p-i-n structures, namely QD3-700, QD6-700 and QD6-630, where the first number (3 or 6) refers to the GaAs capping layer thickness ($h_{CL} = 3 \text{ or } 6 \text{ nm}$) and the second number (630 or 700) represents the growth temperature ($T_g = 700 \text{ or } 630 \text{ °C}$) of the 94 nm GaAs spacer layer. The active region contains a stack of ten layers consisting of 0.34 nm InAs QDs doped with Si/100 nm GaAs. In all three samples the QDs were grown at 490 °C, n-doped to an electronic density of $2 \times 10^{17} \text{ cm}^{-3}$, and deposited for 24 s, resulting in a density of $1.8 \times 10^{10} \text{ cm}^{-2}$ and a height of about 3.5 nm [27]. In contrast, the two samples in the second series labelled SC-630 and SC-700 had no QDs in the active region

and were grown at 630 °C and 700 °C, respectively. This region shown in Figure 6.2 (b) consisted of an undoped GaAs layer with the same thickness (1000 nm) as that of the QD-IBSC structures (Figure 6.2(a)).

The third series illustrated in Figure 6.2 (c) consists of only one sample, SCycle, where the active layer was grown by periodically changing the growth temperature between 490 °C and 700 °C, similar to the temperature cycle used for the deposition of QDs in structures shown in Figure 6.2 (a).

6.3 RESULTS AND DISCUSSION

6.3.1 CAPACITANCE-VOLTAGE OF ALL SAMPLES INVESTIGATED

One of the most essential parameters for the study of p-i-n junction samples is the depletion width, which could be determined by using equation (4.35) in Chapter 4. Since the solar cell is a p-i-n structure composed of different layers, it is important to determine the size of the depletion layer under different reverse bias voltages through capacitance measurements. With this information, the reverse bias can be selected so that the detected depletion area is located in the active area of the solar cell. Data obtained from different samples can then be meaningfully compared.

As shown in Figure 6.3(a), in the -0.25 to -4 V reverse bias voltage range (this voltage range was used in DLTS measurements), the depletion width varies between 616 nm and 854.4nm for QD 6-700, QD3-700 and QD3-700 samples, where the QDs in the intrinsic area are n-doped. It is important to note that this depletion layer accounts for around 57–78 per cent of the active layer.

Figure 6.3(b) shows the change in depletion width as a function of reverse bias of the solar cells without QD. For applied reverse bias between -0.25 and -4 V, the depletion layer width of the SC630 and SC700 samples is approximately 900 nm, corresponding to approximately 82% of the intrinsic region, while for SCycle sample has the depletion width is 670 nm. This value is about 67% of the active layer. It should be noted that due to the residual C doping found in the MOVPE grown samples, the intrinsic region is actually slightly p-type.

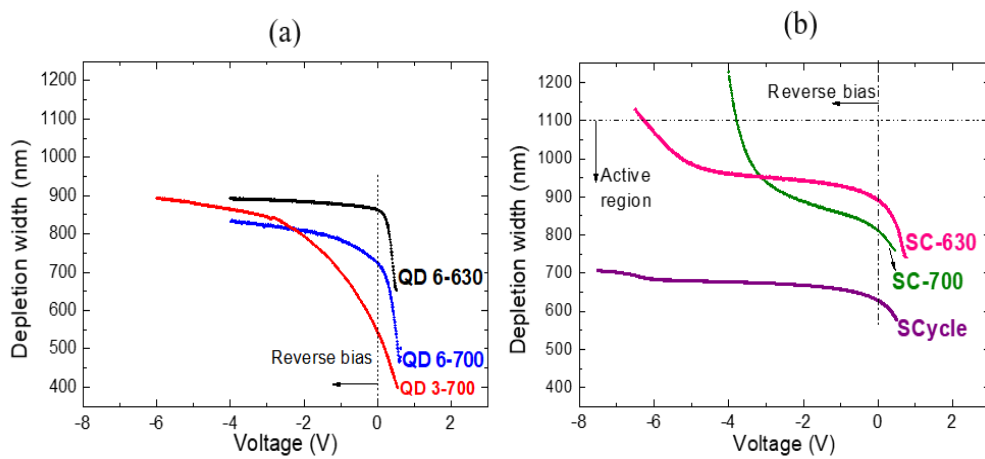


Figure 6.3: The charge depletion width of all investigated QD-IBSCs samples as a function of reverse bias.

6.3.2 EFFECT OF GROWTH TEMPERATURE

6.3.2.1 CURRENT-VOLTAGE MEASUREMENTS

I-V measurement is the first step for determining the suitability of the diodes for the investigation of electrically active defects using DLTS and LDLTS techniques. The devices should have a very low reverse current in the μA range in order to perform DLTS and LDLTS measurements. In this study, a Keithley 236 Source Measure Unit was used to measure the room temperature (300 K) I-V characteristics of GaAs-based solar cell devices (QD6-700 and QD6-630) as shown in Figure 6.4. Low reverse currents are observed in both samples, which makes

them appropriate for DLTS and LDLTS measurements. Since the areas of the samples are different, the current density (J) is plotted in Figure 6.5 instead of current (I). As is clearly seen in Figure 6.5, at a reverse bias of -4V QD6-700 sample has a smaller current density ($\sim 2.9 \times 10^{-7} \text{ A/m}^2$) than QD6-630 sample $1.03 \times 10^{-6} \text{ A/m}^2$). This may suggest that QD6-700 sample has fewer defects [28] than QD6-630, but this hypothesis requires confirmation with DLTS and LDLTS measurements.

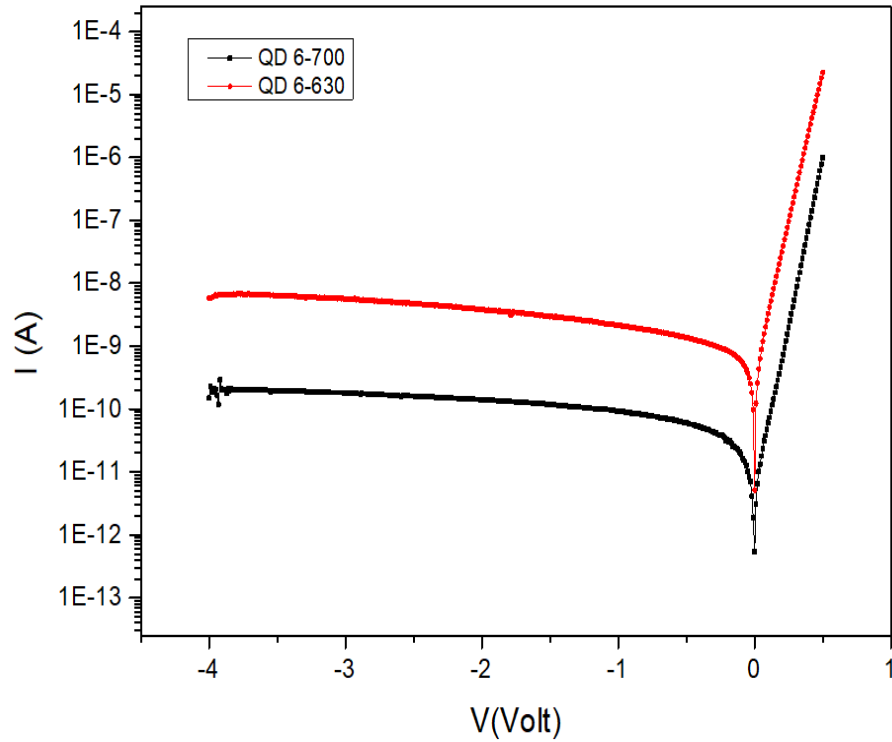


Figure 6.4: Room temperature semi-log plot of I-V characteristics of the QD 6-700 and QD 6-630 samples.

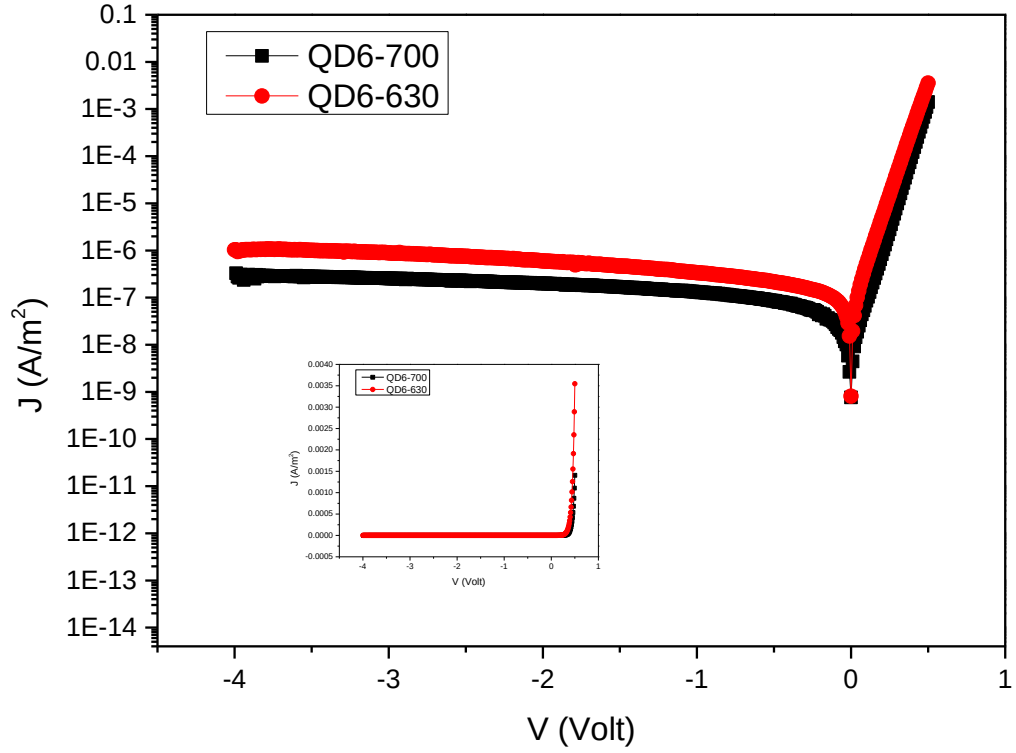


Figure 6.5: Room temperature semi-log plot (J-V) characteristics for QD6-700 and QD6-630 samples. The inset shows a linear J-V plot in the forward bias condition.

6.3.2.2 CAPACITANCE-VOLTAGE MEASUREMENTS

C-V measurements were taken at 300 K using a BOONTON 7200 capacitance meter to determine the free carrier concentration (N_d) of the two samples. Figure 6.6 (a) shows that the change of capacitance per unit area at 300 K as a function of reverse bias is similar for both samples. However, as shown in Figure 6.6 (b) the capacitance per unit area of QD6-630 sample at 20K was higher than that of QD6-700 sample. For QD6-700 device a plateau is observed. This behaviour is attributed to the growth temperature of the QDs capping layer since all other parameters were the same for both structures. The plateau structure in QD6-700 device is observed

in the temperature range 20 - 120 K as shown in Figure 6.7, while it is absent in QD6-630 sample for all temperatures. This finding needs further investigation to understand this behaviour.

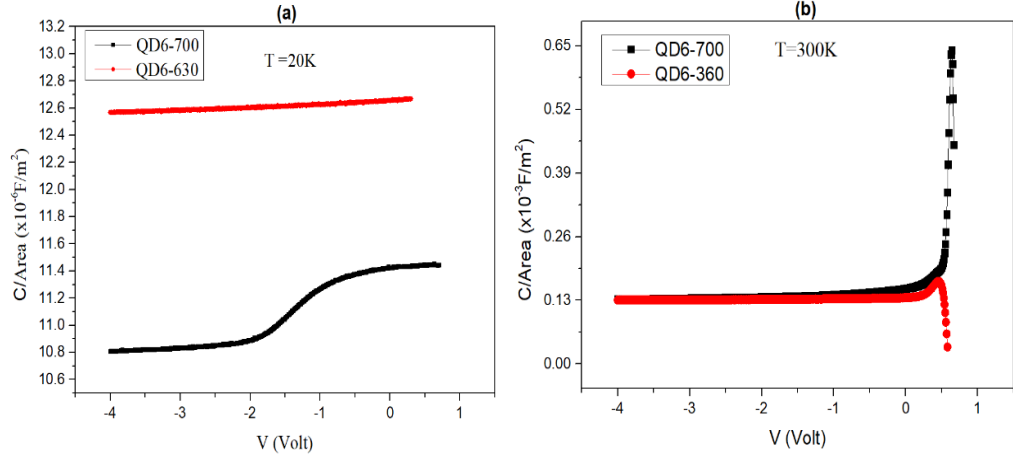


Figure 6.6: Variation of capacitance/area with voltage for QD6-700 and QD6-630 samples at (a) 20K and (b) 300K.

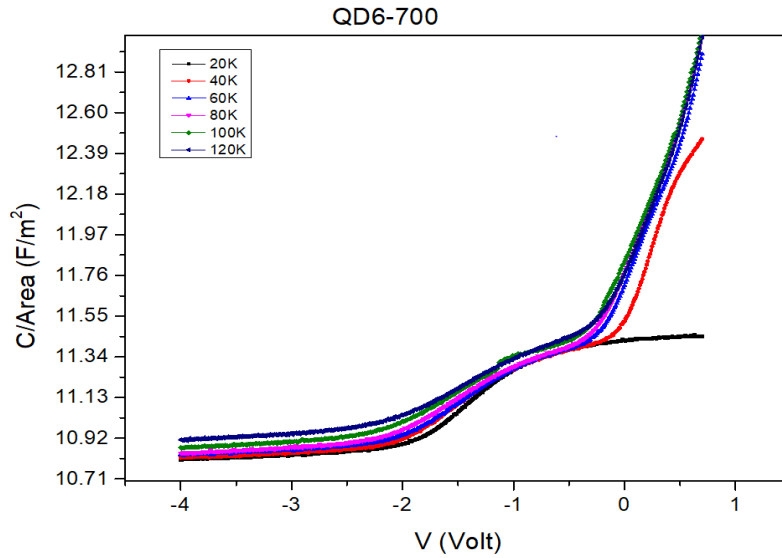


Figure 6.7: Variation of capacitance/area with voltage for QD6-700 at different temperatures.

In general, the free carrier concentration is obtained from the slope of the plot of $(1/C^2)$ versus reverse-bias voltage (V_r) using equation 4.35 discussed in Chapter 4,

and as shown in Figure 6.8. Both samples show more than one slope indicating that the doping concentration is not uniform with distance from the junction. QD6-700 shows two concentrations depth profiles of $1.60 \times 10^{16} \text{ cm}^{-3}$ and $5.47 \times 10^{16} \text{ cm}^{-3}$, while QD6-630 displays three profiles of $1.58 \times 10^{17} \text{ cm}^{-3}$, $7.08 \times 10^{16} \text{ cm}^{-3}$ and $2.67 \times 10^{16} \text{ cm}^{-3}$. It appears that the reduction in the growth temperature of the GaAs spacer layer from 700°C to 630°C leads to an increase in doping concentrations in the QD6-630 sample compared to the QD 6-700 sample [29].

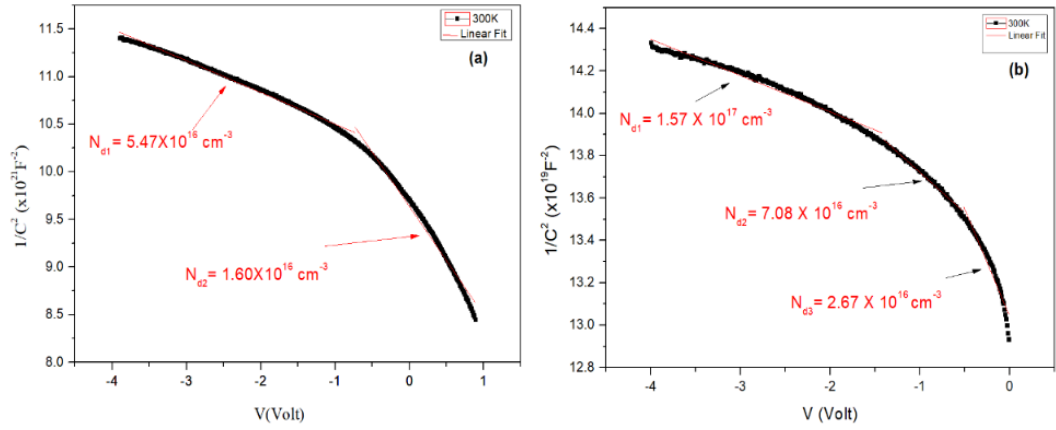


Figure 6.8: Plot of $(1/C^2)$ versus reverse bias (V_r) for (a) QD6-700 sample; (b) QD6-630 sample.

6.3.2.3 DLTS AND LDLTS MEASUREMENTS

DLTS and LDLTS were performed in both samples (QD6-700 and QD6-630) to investigate deep-level defects at a filling pulse height $V_P=0\text{V}$, pulse width of $t_P=1$ msec, rate window of 200 s^{-1} and different reverse biases of $V_r = -0.25, -1$ and -4 V) [30, 31]. These measurements were obtained over the temperature range $20 - 450 \text{ K}$.

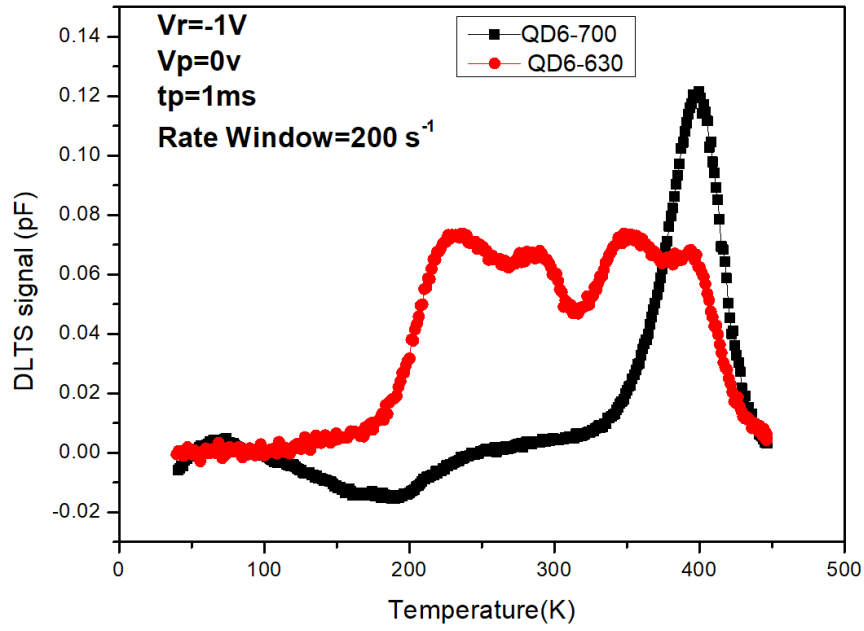


Figure 6.9: DLTS spectra for QD6-630 and QD6-700 samples at $V_r = -1V$.

Figure 6.9 shows DLTS spectra for both samples for bias conditions $V_r = -1V$ and $V_p = 0V$. In the QD6-700 sample one sharp peak at 400 K and two small peaks at low temperatures were detected. For the QD 6-630 sample four broad peaks were observed.

The DLTS spectra of the two samples show distinguished behaviour, and this could be attributed to the difference in the growth temperature of the GaAs spacer layer. Laplace DLTS will be discussed later to further understand these defects.

Figure 6.10 illustrates the DLTS signals detected in QD6-700 and QD6-630 samples at different reverse biases, namely -0.25V, -1V and -4V. These biases were used to investigate traps near the interface and away from the interface of the p-i-n junction. As seen in Figure 6.10(a), the amplitude of the DLTS peak detected in the temperature range of 300–450 K is positive and smaller near the interface (for $V_r =$

-0.25V: EA1^{-0.25V}) than the peaks away from the interface [$V_r = -1V$ (EA2^{-1V}) and $V_r = -4V$ (EA1^{-4V})]. This indicates that the defect is an electron trap (majority carrier) and predominantly away from the interface between p and n regions. It is most probably present in the i region. In addition, for $V_r = -1V$, the trap (HA1^{-1V}) exhibits a negative DLTS signal in the temperature range of 125 - 225K, indicating that this trap is a hole trap (minority carrier). It may be near the interface, located in the i or undoped GaAs ($1 \times 10^{15} \text{ cm}^{-3}$) regions.

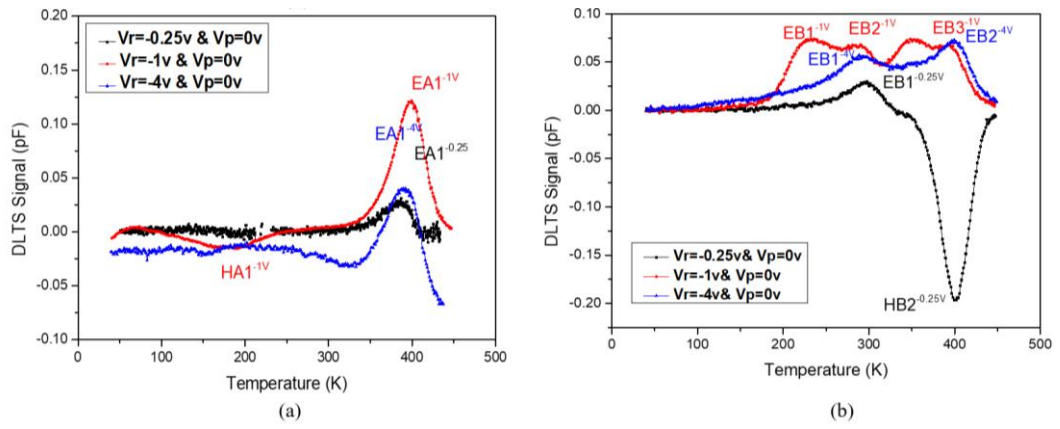


Figure 6.10: DLTS signals at different reverse biases for (a) QD6-700 sample and (b) QD6-630 sample. A and B refer to QD6-700 and QD6-630, respectively.

The different growth temperatures of the GaAs spacer layer led to completely different DLTS spectra for samples QD6-700 and QD 6-630, grown at 700 °C and 630 °C, respectively. For example, for $V_r = -0.25 \text{ V}$ (Figure 6.10(b)), QD6-630 exhibited a negative DLTS signal, indicating that this trap (HB2^{-0.25V}) is a hole trap (minority carrier). Due to the low reverse applied bias, this trap is near the interface, located in the i or undoped GaAs ($1 \times 10^{15} \text{ cm}^{-3}$) regions. In addition, for this bias, the EB1^{-0.25V} trap in the temperature range 250–350 K was present also at high reverse biases [$V_r = -1V$ (EB2^{-1V}) and $V_r = -4V$ (EB1^{-4V})]. For high applied reverse

biases, namely -1 V and -4 V in the temperature range $300\text{--}450\text{ K}$, the DLTS signals $\text{EB3}^{-1\text{V}}$ and $\text{EB2}^{-4\text{V}}$ were similar to those observed in QD6-700 sample. However, QD6-630 exhibited broad and asymmetric signals across a wide range of temperatures indicating that there may be more peaks in this range. The high resolution LDLTS techniques was used in order to resolve the broad and asymmetric peaks observed in both samples and determine the parameters of the traps. All the peaks in both samples were related to electrically active defects [32].

The activation energy (E_T), trap concentration (N_T) and captured cross-section (σ_∞) of all defects detected in both samples were obtained from the Arrhenius plot of $\ln(e_n / T^2)$ versus $(1000/T)$, as shown in Figures 6.11, 6.12 and 6.13 for reverse biases of -0.25 V , -1 V and -4 V , respectively. These parameters are summarised in Table 6.1

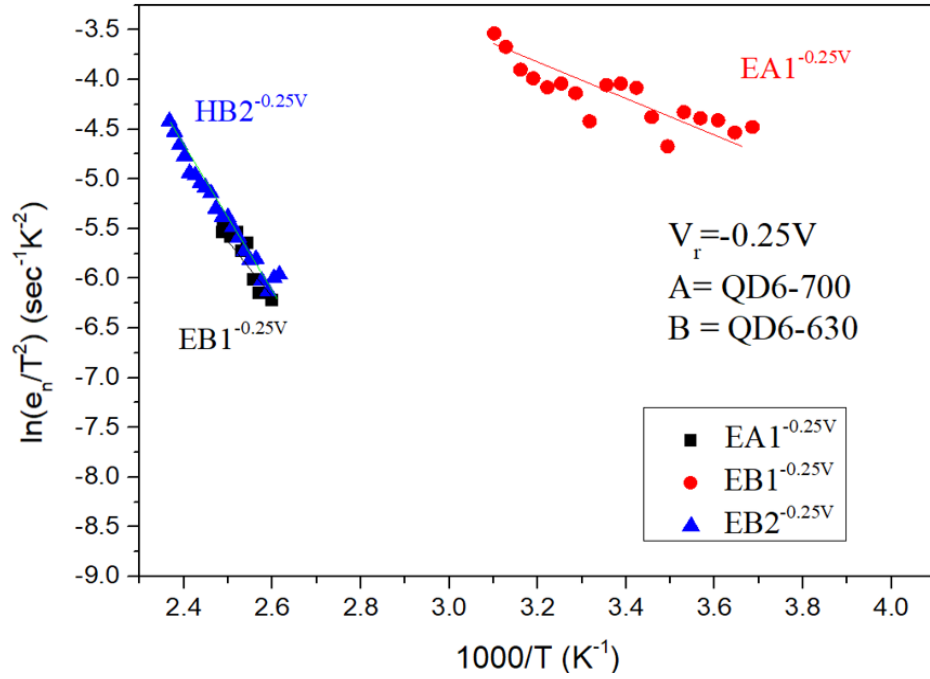


Figure 6.11: Arrhenius plots for both samples obtained by LDLTS using reverse biases of $V_r = -0.25\text{V}$ and $V_p = 0\text{V}$. A and B refer to QD6-700 and QD6-360, respectively.

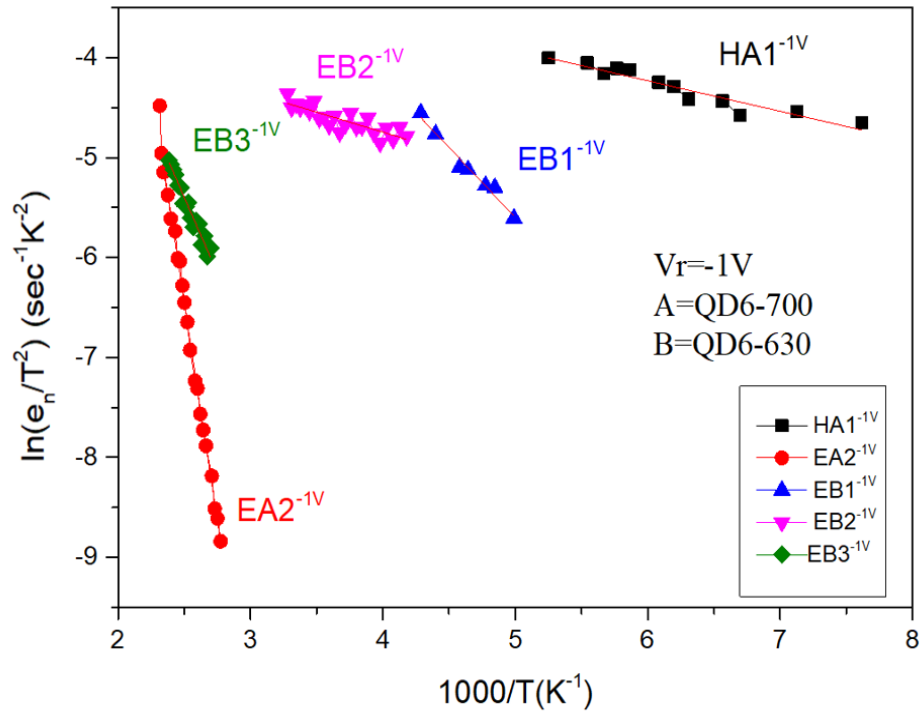


Figure 6.12: Arrhenius plots for both samples obtained by LDLTS using reverse biases of $V_r = -1\text{V}$ and $V_p = 0\text{V}$. A and B refer to QD6-700 and QD6-630, respectively.

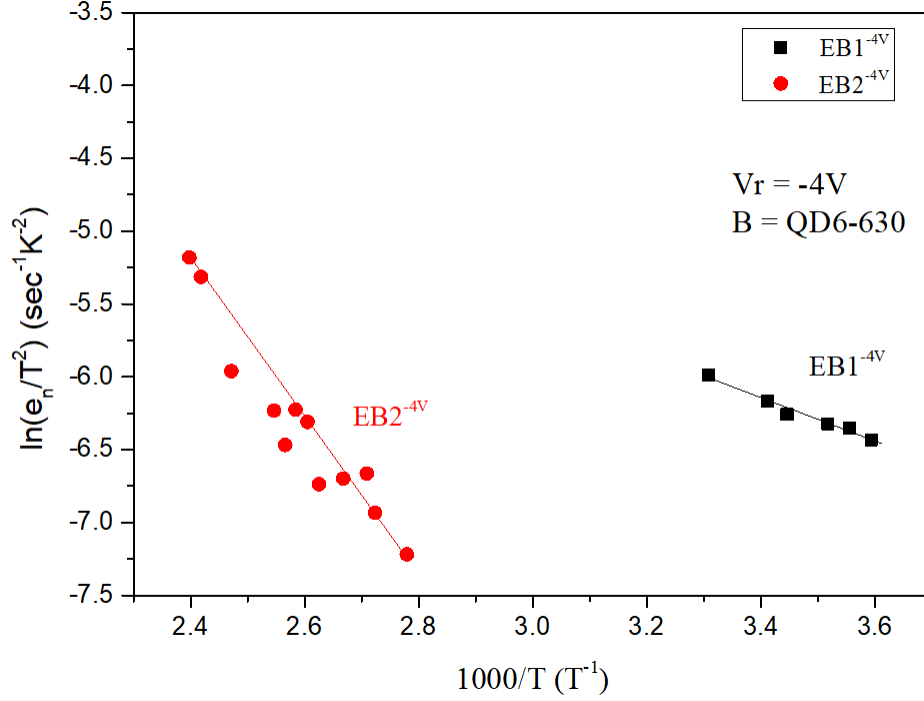


Figure 6.13: Arrhenius plot of the LD LTS results obtained for QD 6-630 sample with reverse biases of $V_r = -4V$ and $V_p = 0V$. B refer to QD6-630.

Table 6.1 shows that for $V_r = -0.25V$, $EA1^{-0.25V}$ in QD6-700 is a deep-level trap with an activation energy of 0.42 ± 0.03 eV. $EB1^{-0.25V}$ and $HB2^{-0.25V}$ in QD6-630 are also deep-level traps, and they have energies of 0.12 ± 0.02 eV and 0.59 ± 0.02 eV, respectively. For $V_r = -1V$, in QD6-700, $HA1^{-1V}$ is a shallow-level trap and $EA2^{-1V}$ is a deep-level trap, with energies of 0.026 ± 0.003 eV and 0.77 ± 0.01 eV, respectively. In QD6-630, on the other hand, $EB1^{-1V}$ and $EB3^{-1V}$ are deep-level traps with energies of 0.12 ± 0.01 eV and 0.26 ± 0.01 eV, respectively, but $EB2^{-1V}$ is a shallow-level trap with an energy of 0.035 ± 0.005 eV. The peak $EA1^{-4V}$ disappears for $V_r = -4V$. At $V_r = -4V$, $EB1^{-4V}$ and $EB2^{-4V}$ in QD6-630 are deep-level traps with energies of 0.13 ± 0.01 eV and 0.42 ± 0.04 eV, respectively.

It should be noted that at a high temperature one of the traps ($EA2^{-0.25V}$ and $EB2^{-4V}$) has an energy of ~ 0.42 eV in both samples and thus may be related to the well-

known defect EL5. It is believed to originate as a result of an isolated arsenic antisite defect (As_{Ga}) [33]. Moreover, $\text{EA2}^{-1\text{V}}$ has an energy of ~ 0.77 eV, which could be attributed to the well-known defect in GaAs called EL2. This is a complex defect involving As_{Ga} and an arsenic interstitial [23-25, 34]. The hole trap $\text{HB2}^{-0.25\text{V}}$ (~ 0.59 eV) could not be identified in this work. However, these traps might be related to the MOCVD growth mechanism used for these samples.

The traps $\text{EB1}^{-0.25\text{V}}$, $\text{EB1}^{-1\text{V}}$ and $\text{EB1}^{-4\text{V}}$, which were detected at different reverse biases in Sample QD6-630, have very low activation energies and capture cross-sections of 0.12 - 0.13 eV and 10^{-21} - 10^{-22} cm^2 . These activation energies could be compatible with electron thermal emission from confined states in InAs QDs embedded in GaAs [35]. The electronic ground and first excited states for sample QD 6-630 should be about 0.19 eV and 0.16 eV from the GaAs conduction band [36]. The electron trap $\text{EB3}^{-1\text{V}}$ with an activation energy of ~ 0.27 eV could not be identified in this work.

All of these defects could be located in the intrinsic regions of both samples. Laplace DLTS should be used at different biases to support this assumption. The $\text{HA1}^{-1\text{V}}$ (0.026 ± 0.003 eV) and $\text{EB2}^{-1\text{V}}$ (0.035 ± 0.005 eV) shallow traps could not be identified in this work. However, these could be related to intentional (shallow dopants) and/or unintentional impurities (background) introduced during the growth process of the structures.

Table 6.1: Activation energies, capture cross-sections and concentrations of defects detected in QD6-700 and QD6-630 samples at ($V_r = -0.25$ V, $V_p = 0$ V), ($V_r = -1$ V, $V_p = 0$ V) and ($V_r = -4$ V, $V_p = 0$ V), with $t_p = 1$ msec at rate window $= 200$ s⁻¹.

Sample	Reverse Bias (V)	Trap	Activation Energy (eV)	Trap Concentration (cm ⁻³)	Capture Cross-section, σ_0 (cm ²)
QD6-700 (A)	-0.25	EA1 ^{-0.25V} (EL5) [33]	(0.42±0.03)	9.3x10 ¹³	4.95x10 ⁻¹⁹
	-1	HA1 ^{-1V}	(0.026±0.003)	1.69x10 ¹⁴	5.12x10 ⁻²³
		EA2 ^{-1V} (EL2) [23-25, 34]	(0.77±0.01)	1.33x10 ¹⁵	4.5x10 ⁻¹⁵
	-4	QD6-700 does not have any detectable defects			
QD6-630 (B)	-0.25	EB1 ^{-0.25V}	(0.12±0.02)	1.83x10 ¹³	9.38x10 ⁻²²
		HB2 ^{-0.25V}	(0.59±0.02)	1.21x10 ¹⁴	7.83x10 ⁻¹⁷
	-1	EB1 ^{-1V}	(0.12± 0.01)	1.22x10 ¹⁴	2.28x10 ⁻²¹
		EB2 ^{-1V}	(0.035±0.005)	1.12x10 ¹⁴	2.44x10 ⁻²³
		EB3 ^{-1V}	(0.260±0.014)	1.13x10 ¹⁴	5x10 ⁻²¹
	-4	EB1 ^{-4V}	(0.13±0.01)	2.16x10 ¹⁴	1.96x10 ⁻²²
		EB2 ^{-4V} (EL5) [33]	(0.42±0.04)	2.75x10 ¹⁴	3.09x10 ⁻¹⁹

6.3.3 EFFECT OF THE GaAs CAPPING LAYER THICKNESS

6.3.3.1 CURRENT-VOLTAGE MEASUREMENTS

The GaAs spacer layer of QD6-700 and QD3-700 samples were both grown at the same temperature, but the thickness of the GaAs capping layer (h_{CL}) was different (see Figure 6.2 a). h_{CL} was 6 nm and 3 nm for QD6-700 and QD3-700, respectively.

I-V measurements as a function of temperature (20-440 K with 20 K intervals) were performed in order to determine the diodes' parameters such as ideality factor (n), built-in potential energy (V_{bi}), and series resistance (R_s).

The room temperature dark current density (J) - voltage (V) characteristics of QD6-700 and QD3-700 samples are shown in Figure 6.13. As seen in Figure 6.13, both the forward and reverse current densities are affected by the thickness of the GaAs capping layer. From the J-V characteristics the defects seem to be higher in QD3-700 sample than in QD6-700 sample. It is well-known that leakage current can take place via the defects present in the device [37].

The diffusion process of conduction electrons can normally be used to describe the I-V characteristics of ideal diodes [38]:

$$I = I_0 \left[\exp\left(\frac{q(V - IR_s)}{nK_B T}\right) - 1 \right] \quad (6.1)$$

where q is the electronic charge, V is the applied voltage, R_s is series resistance, K_B is the Boltzmann constant, n is the ideality factor, I_0 is the saturation current, and T is the absolute temperature in Kelvin.

The experimental data was used to obtain the values of n and I_0 . The saturation current I_0 is calculated as follows:

$$I_0 = AA^{**}T^2 \exp\left(\frac{-q\phi_B}{K_B T}\right) \quad (6.2)$$

or $J_0 = I_0/A = A^{**}T^2 \exp\left(\frac{-q\phi_B}{K_B T}\right)$

where A is the diode area (A is equal to $7.07 \times 10^{-4} \text{ cm}^2$ and $2.83 \times 10^{-3} \text{ cm}^2$ for QD6-700 and QD3-700, respectively), J_0 is the saturation current density and A^{**} is the effective Richardson's constant ($A^{**} = 8.16 \text{ A cm}^{-2} \text{ K}^{-2}$) for n-type GaAs, [39] and V_{bi} is built-in potential energy. The electrical parameters of the diodes (n, V_{bi} and R_s) were obtained using Werner's approach [40], which was discussed in details in Chapter 4.

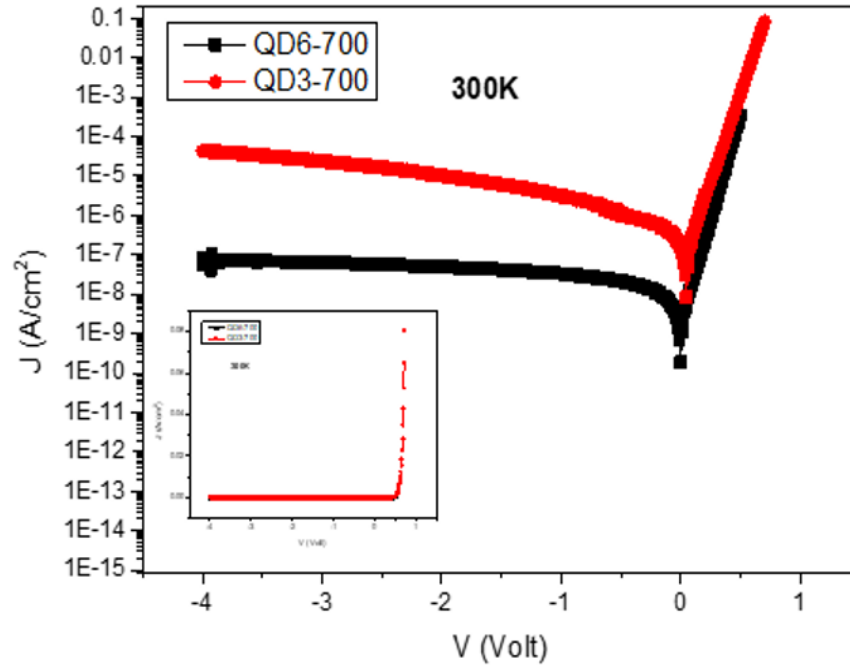


Figure 6.13: Room temperature semi-log plot (J-V) characteristics of QD3-700 and QD6-700 samples. The inset shows the linear J-V characteristics.

Figure 6.14 illustrates the plots of G/J versus G (conductance) and $\ln(J)$ versus ($V-JR_s$) for both samples. These are utilised to obtain the diode parameters as explained in section 4.3 of Chapter 4. A summary of these room temperature parameters is given in Table 6.2. QD6-700 sample has a lower ideality factor (1.54) and a slightly lower built-in potential energy (~ 0.65 eV) as compared to QD3-700 sample ($n=1.82$; $V_{bi}=0.67$ eV). The decrease in the thickness of the capping layer affects the series resistance (R_s) [41] as demonstrated in Figure 6.15, which shows the change of series resistance at various temperatures. At high temperatures, R_s of both samples are somewhat similar but for temperatures below ~ 250 K R_s values are higher in QD3-700 sample than in QD6-700 sample.

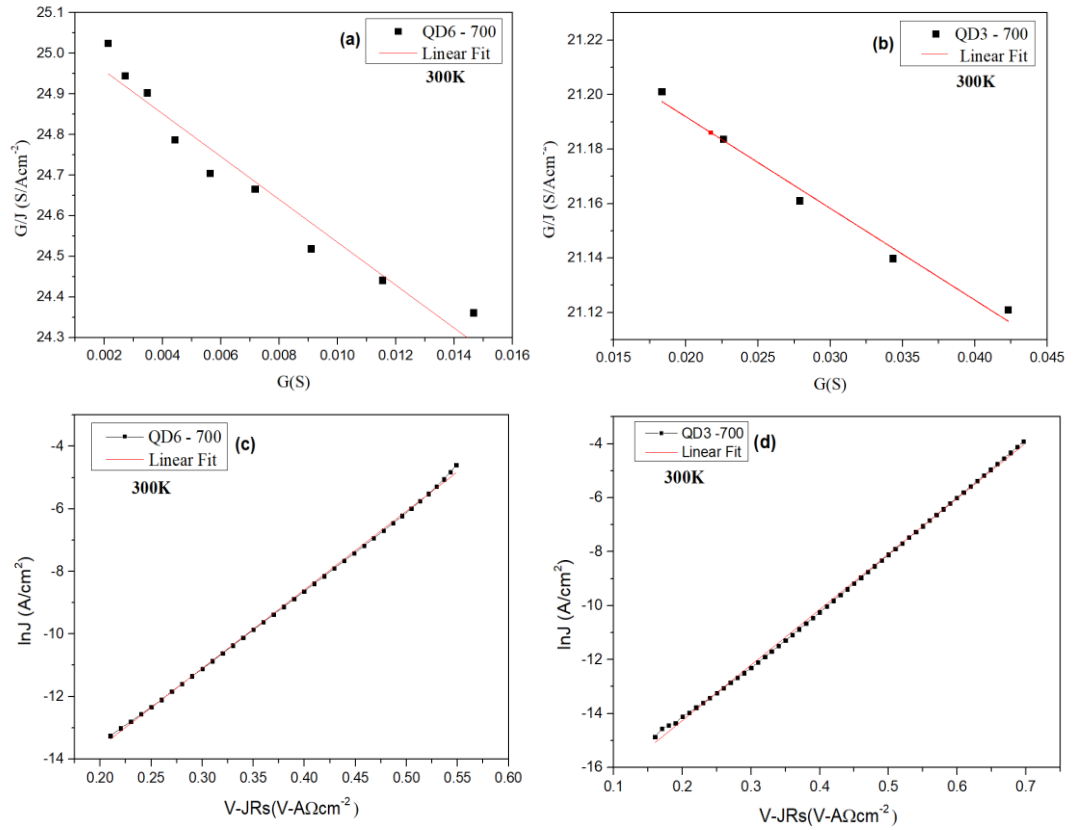


Figure 6.14: The plot of G/J versus G for (a) QD6-700 and (b) QD3-700 samples. The plot of $\ln(J)$ versus ($V-JR_s$) for (c) QD6-700 and (d) QD3-700 samples.

Table 6.2: Ideality factor (n), built-in potential energy (V_{bi}) and series resistance (R_s) at room temperature for QD6-700 and QD3-700 samples

Sample	n	V_{bi} (eV)	R_s (K Ω)
QD6-700	1.54 ± 0.03	0.65 ± 0.01	8.90 ± 0.53
QD3-700	1.82 ± 0.01	0.67 ± 0.01	31.0 ± 3.2

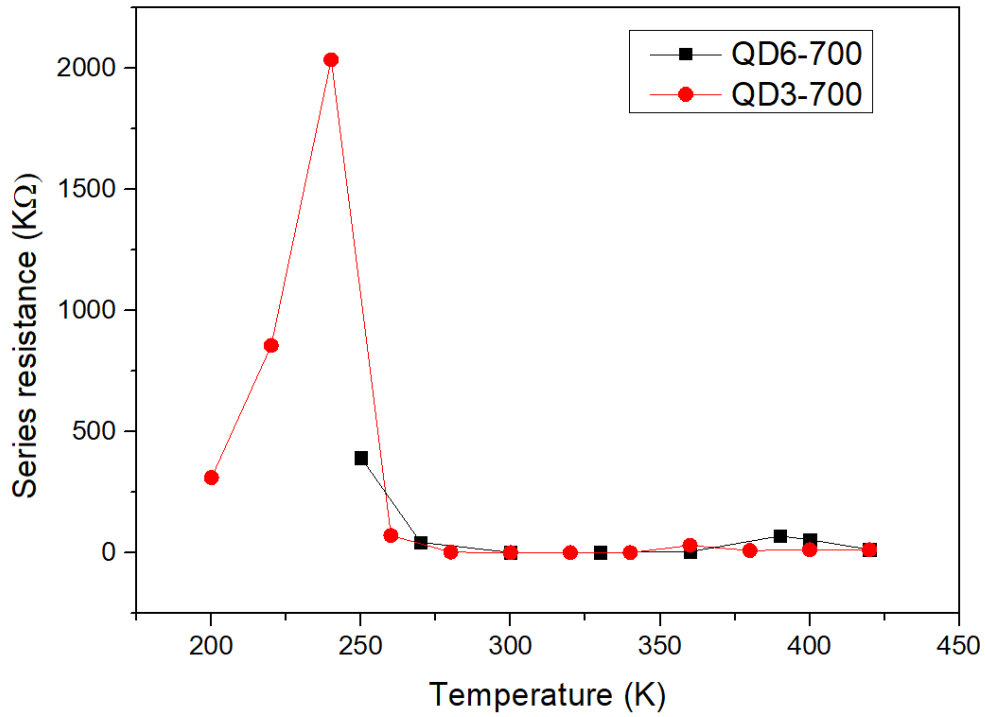


Figure 6.15: Temperature dependence of the experimental series resistance R_s determined from J–V characteristics of QD6-700 and QD3-700 samples.

In the high temperature ranges of 380–420 K and 280–420 K, the plot of $\ln (J_0/T^2)$ versus $1000/T$ for QD6-700 sample (Figure 6.16(a)) and QD3-700 sample (Figure 6.16(a)), respectively, follows a straight line. This behaviour shows that the

diffusion process controls the conduction mechanism, and the saturation current may be calculated using Equation (6.2) [42]. Moreover, the Richardson constants could be determined from the intercept of the straight line of $\ln(J_0/T^2)$ versus $1000/T$ plot. The Richardson constant was found to be $2.126 \times 10^{-2} \text{ A cm}^{-2} \text{ K}^{-2}$ and $3.88 \times 10^{-6} \text{ A cm}^{-2} \text{ K}^{-2}$ for QD6-700 and QD3-700, respectively. These values are much lower than the well-established value of $8.16 \text{ A cm}^{-2} \text{ K}^{-2}$ of GaAs. The spatial inhomogeneous built-in potential energy and potential fluctuations at the interface that consist of low and high built-in potential energies could account for the deviations from the well-known Richardson constant [43]. However, it can clearly be seen that a different behaviour in terms of slope of $\ln(J_0/T^2)$ as a function of $1000/T$ plots is observed for both samples in the temperature ranges of 250-360 K (QD6-700 sample) and 200-280 K (QD3-700 sample). This behaviour could be due to an additional current contribution as a result of the lowering of the built-in potential energy [43].

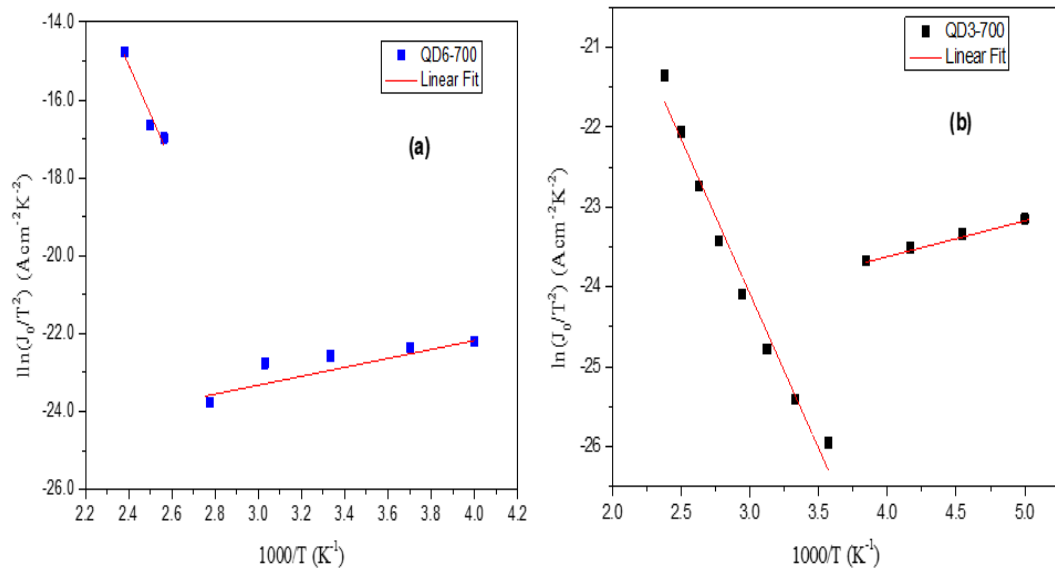


Figure 6.16: Plots of $\ln(J_0/T^2)$ versus $1000/T$ for (a) QD6-700 and (b) QD3-700 samples.

Figures 6.17 and 6.18 illustrate the temperature dependence of the built-in potential (V_{bi}) and ideality factor (n) for both samples, respectively. One important result is that the built-in potential energy increases with increasing temperature, whereas the ideality factor decreases in QD3-700 sample. This behaviour is caused by the nonuniformity of interfacial charges. Additionally, the current does not follow the diffusion mechanism because the carriers are frozen at low temperatures. On the other hand, sample QD6-700 has peculiar behaviour where the built-in potential energy increases with decreasing temperature as shown Figure 6.17. A possible explanation for this behaviour could be that the sample behaves like a metal where the bandgap decreases with increasing temperature [44, 45]. Moreover, at low temperatures, the values of the ideality factor are higher due to the fact that the current flows through the interface states [46, 47] in both samples.

It is worth pointing out that carriers can overcome lower built-in potential energy at low temperatures, and the transport mechanism will be dominated by the current flowing through the regions with the lowest built-in potential energy. Carriers generate enough energy to overcome larger built-in potential energy as the temperature increases, resulting in an increase in built-in potential energy with temperature [47, 48]. It can clearly be seen that the deviation from a linear relationship of the plot V_{bi} versus n as shown in Figure 6.19 (a and b) could be due to the uncertainties in the calculation of the ideality factor [49, 50].

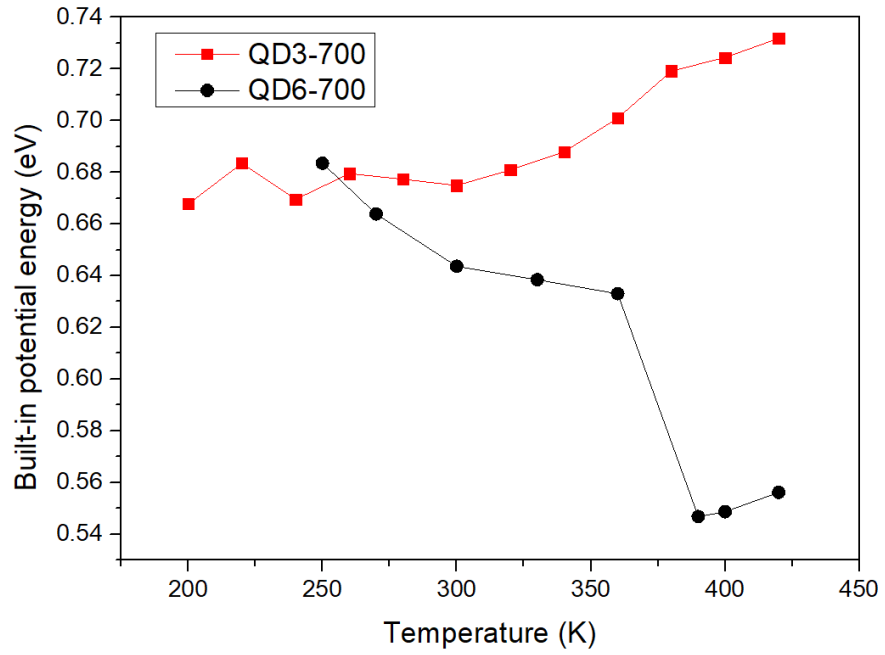


Figure 6.17: Plots of built-in potential energy (eV) (V_{bi}) versus temperature for both samples obtained from J–V characteristics.

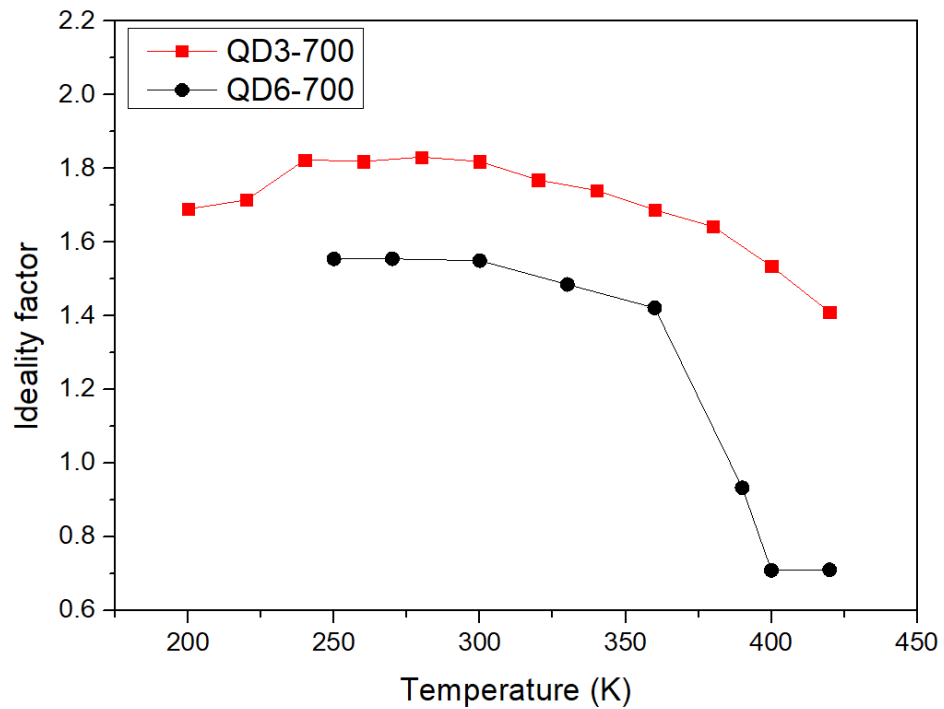


Figure 6.18: Plots of ideality factor (n) versus temperature for both samples obtained from J–V characteristics.

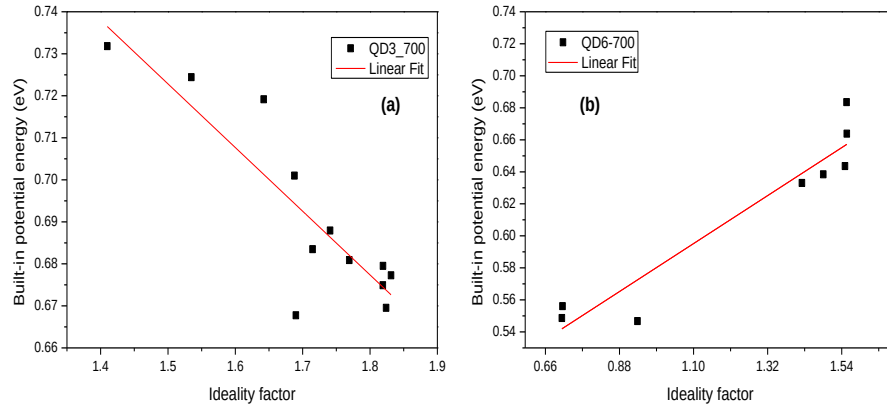


Figure 6.19: Built-in potential energy (V_{bi}) versus ideality factor (n) for (a) QD3-700 and (b) QD6-700.

6.3.3.2 CAPACITANCE-VOLTAGE MEASUREMENTS

The C-V characteristics of QD3-700 and QD6-700 samples at room temperature are shown in Figure 6.20. It can be seen that the values of the capacitance per area of QD3-700 and QD6-700 samples are similar for reverse biases greater than ~ -1 V. However, QD3-700 has higher C/Area for reverse voltages less than ~ -1 V.

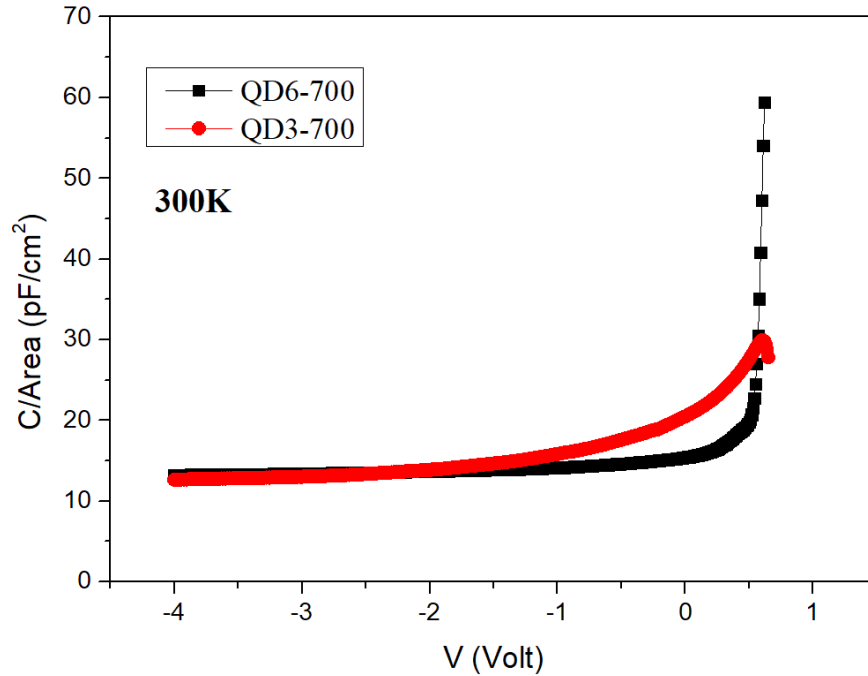


Figure 6.20: Variation of capacitance/area with reverse bias for QD6-700 and QD3-700 samples at room temperature.

The free carrier concentration for QD 6-700 and QD 3-700 samples is calculated using the slope of the plot of $(1/C^2)$ versus reverse-bias voltage (V). Both samples have more than one slope, as shown in Figure 6.21. This behaviour is caused by the fact that the doping concentration is not uniform and varies with distance from the diode's junction interface. The doping concentrations of QD6-700 and QD3-700 were found to be $1.60 \times 10^{16} \text{ cm}^{-3}$ and $5.47 \times 10^{16} \text{ cm}^{-3}$, and $3.06 \times 10^{16} \text{ cm}^{-3}$, $1.39 \times 10^{16} \text{ cm}^{-3}$ and $7.88 \times 10^{16} \text{ cm}^{-3}$, respectively.

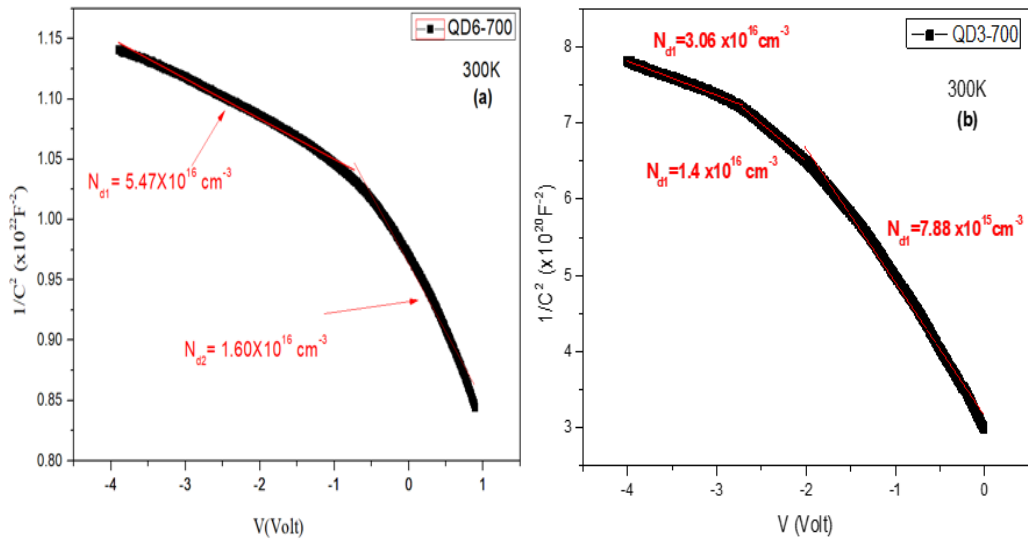


Figure 6.21: Variation of $1/C^2$ versus V for (a) QD6-700 and (b) QD3-700 samples at room temperature

6.3.3.3 DLTS AND LDLTS MEASUREMENTS

DLTS measurements were performed on the IBSCs samples to explore the effect of the GaAs capping effects on the electrically active defects [30]. These measurements were carried out at reverse biases $V_r = -1 \text{ V}$, a filling pulse height,

$V_p = 0V$, a filling pulse time, $t_p = 1 \text{ msec}$ and a rate window of 200 s^{-1} for both samples. The samples' temperature was scanned from 10 K up to 440 K.

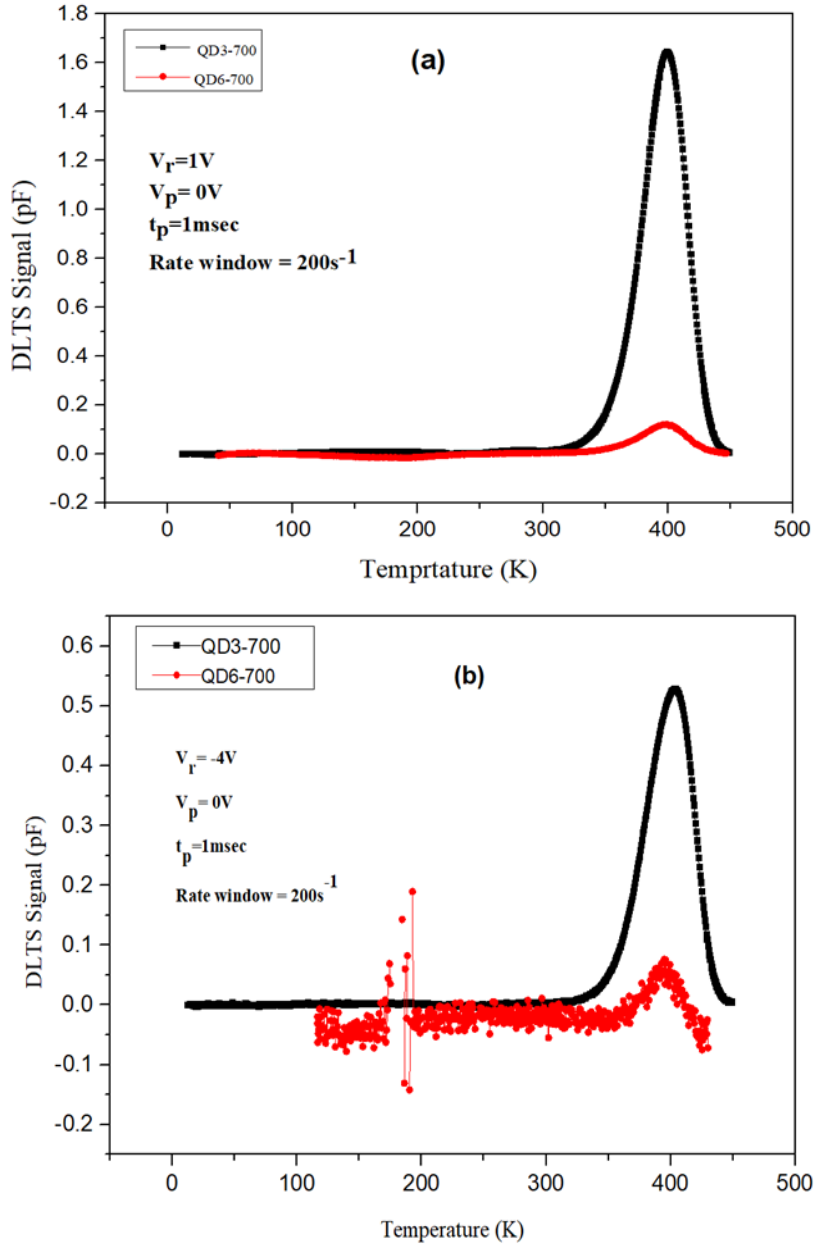


Figure 6.22: DLTS signals for QD6-700 and QD3-700 samples at (a) $V_r = -1V$ and (b) $V_r = -4V$ with $V_p = 0V$.

Figure 6.22 illustrates the DLTS spectra of QD6-700 and QD3-700 samples at different reverse biases to investigate deep traps near ($V_r = -1 \text{ V}$) and away from the junction interface ($V_r = -4 \text{ V}$). Only one sharp peak at 400K has been detected in both

samples at both biases. It is relevant to note that when the thickness of the GaAs capping layer increases, the DLTS signal's amplitude decreases. Furthermore, an increase in the reverse bias (away from the interface) causes the amplitude of the DLTS signal to decrease. These results indicate that the concentration of the trap is not uniform and is highest near the junction interface.

Figure 6.23 shows the Arrhenius plots at these reverse biases, and Table 6.3 illustrates the trap parameters (activation energies, trap concentrations and capture cross- sections) for both samples at $V_r = -1$ V, and $V_r = -4$ V.

From Figures 6.10, 6.22 and 6.23 and Tables (6.1 and 6.3), at $V_r = -1$ V, both samples have a trap with the same activation energy of ~ 0.77 eV. This trap may be attributed to the well-known defect in GaAs called EL2. This is a complex defect involving As_{Ga} and an arsenic interstitial [23-25, 34]. The EL2 trap was also observed in QD3-700 at $V_r = -4$ V but it disappeared in QD6-700 at the same bias. This defect could be located in the intrinsic regions of both samples. On the other hand, QD6-700 has also a shallow-level trap (hole) with energies of 0.03 ± 0.003 eV.

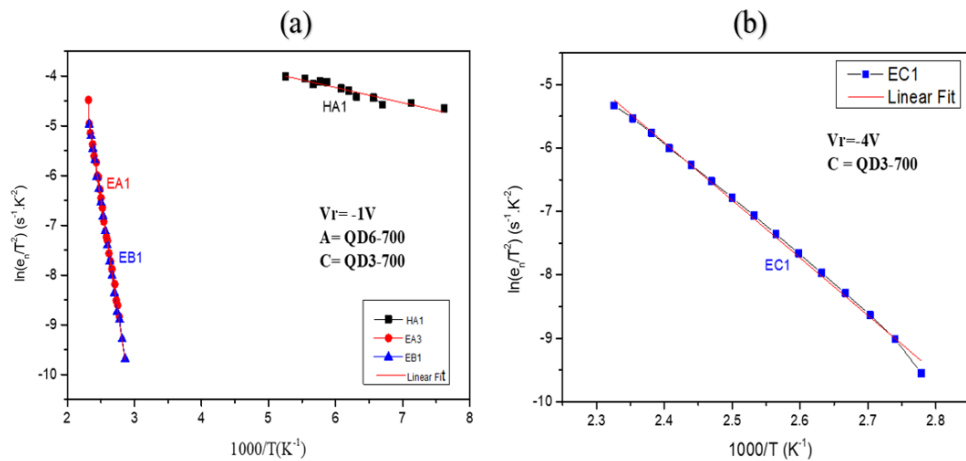


Figure 6.23: Arrhenius plots for QD6-700 and QD3-700 samples at (a) $V_r = -1$ V and (b) $V_r = -4$ V

Table 6.3: Traps parameters (activation energies, capture cross-sections and concentrations) of Q6-700 and QD 3-700 samples at ($V_i = -1$ V, $V_p = 0$ V) and ($V_i = -4$ V, $V_p = 0$ V), with $t_p = 1$ msec and rate window = 200 s^{-1} .

Sample	Reverse Bias (V)	Trap	Activation Energy (eV)	Trap Concentration (cm^{-3})	Capture Cross-section, σ_∞ (cm^2)
QD6-700 (A)	-1	HA1 ^{-1V}	(0.026 $\pm$ 0.003)	1.69×10^{14}	5.12×10^{-23}
		EA2 ^{-1V} (EL2) [23-25, 34]	(0.77 $\pm$ 0.01)	1.33×10^{15}	4.5×10^{-15}
	-4	QD6-700 does not have any detectable defects			
QD3-700 (C)	-1	EC1 ^{-1V} (EL2) [23-25, 34]	(0.77 $\pm$ 0.01)	2.2×10^{15}	3.8×10^{-15}
	-4	EC1 ^{-4V} (EL2) [23-25, 34]	(0.78 $\pm$ 0.01)	2.3×10^{14}	3.9×10^{-15}

6.3.4 EFFECT OF THE GROWTH TEMPERATURE AND COMPOSITION OF THE INTRINSIC-REGION (ACTIVE) OF P-I-N STRUCTURES

This section reports the effect of the growth temperature and composition of the i-region the electrically active defects in control p-i-n and QD-based IBSC solar devices. This investigation was performed by using current-voltage (I-V), capacitance-voltage (C-V) measurements and deep-level transient spectroscopy (DLTS) and Laplace DLTS (LDLTS) techniques.

This study utilised four set of samples consisting of: (i) p-i-n IBSCs with InAs self-assembled QDs incorporated in the i-region (active layer) (QD3-700; Figure 6.1 a); (ii) p-i-n devices where the i-layer (active layer) is just GaAs (i.e. without QDs) (SC630 and SC700 grown at 630 and 700 °C, Figure 6.1 b) but with the same thickness as that of the QD-IBSC structure; (iii) p-i-n structure where the i-layer (active layer) was grown by periodically changing the growth temperature between 490 °C and 700 °C (SCycle, Figure 6.1 c), similar to the growth temperature cycle used for the deposition of QD3-700.

6.3.4.1 CURRENT-VOLTAGE MEASUREMENTS

Room temperature I-V characteristics of GaAs-based solar cell devices, namely QD3-700, SC-630, SC-700 and SCycle are shown in Figure 6.24. Low reverse currents are observed in all four samples, which makes them suitable for DLTS and LDLTS measurements.

Since the areas of the samples were different, the current density (J) is used instead of I, as plotted in the inset of Figure 6.24. As observed in this figure, SC-700 sample has the lowest current density for reverse biases up to - 4V. The current density at - 4V of SC-700, QD3-700, SC-630 and SCycle was approximately 0.017A/cm², 0.11 A/m², 20.98 A/cm², and 0.186 A/cm², respectively.

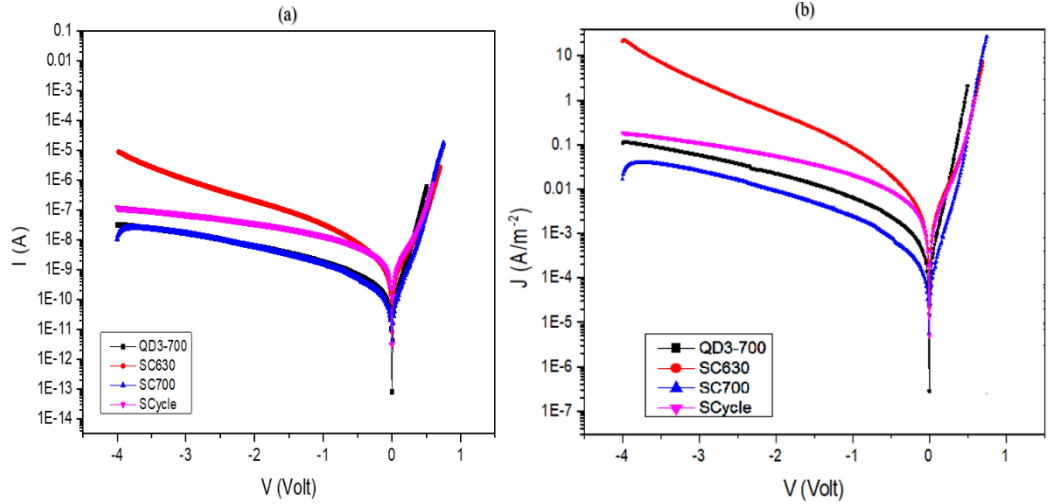


Figure 6.24: Room temperature semi-log plots (a) (I-V) characteristics; (b) current density J-V plot for all samples

The lowest current density observed in SC-700 sample may indicate that it has fewer defects [28]. This is due probably to the fact that the active region does not incorporate QDs and is grown at the highest growth temperature of 700 °C. This assumption requires confirmation via DLTS and LDLS measurements. However, QD3-700 sample has a lower current density than SC-630 sample which was grown at 630 °C and does not incorporate InAs QDs in the active layer. SCycle, a control sample with no QDs in the i-region but grown by periodically changing the growth temperature between 490 °C and 700 °C, has the highest reverse current density.

6.3.4.2 CAPACITANCE-VOLTAGE MEASUREMENTS

Figure 6.25 shows the C-V characteristics of all samples at room temperature. It can be seen from this figure that QD3-700 sample has the highest capacitance per area for reverse biases $< \sim -2\text{V}$. This could be because the QDs in the i-region have an increased number of defects [51].

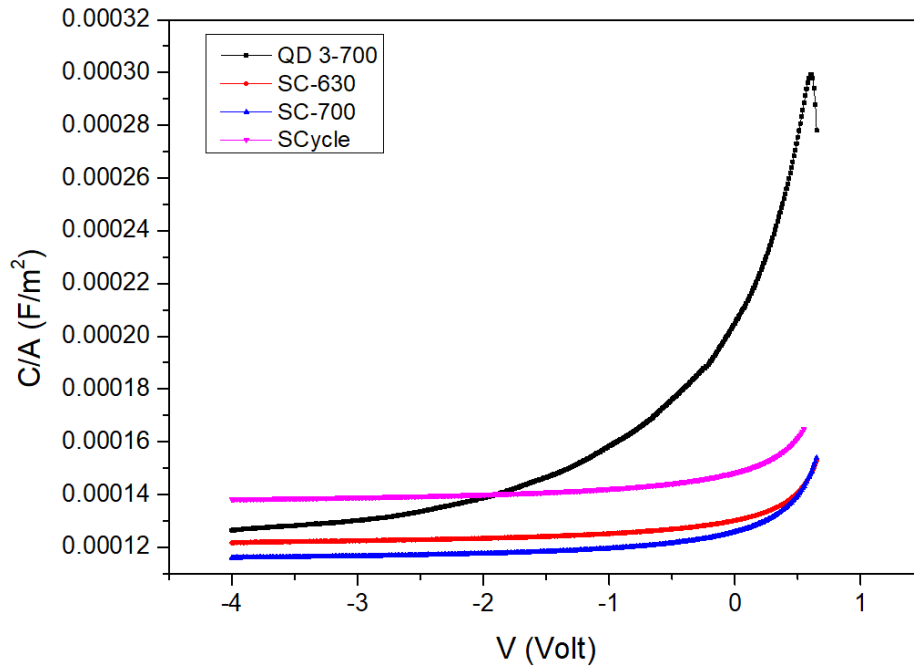


Figure 6.25: Variation of capacitance/area with voltage for QD3-700, SC630, SC700 and SCycle samples at room temperature.

The slope of the plot of $(1/C^2)$ versus reverse-bias voltage (V) is used to obtain the free carrier concentration for all samples. Figure 6.26 shows that all samples have more than one slope indicating that the doping concentration is not uniform with distance from the junction interface. Thus, these samples have various doping concentrations as a function of distance from the interface. The following concentrations were found: (i) QD3-700: $3.06 \times 10^{16} \text{ cm}^{-3}$, $1.4 \times 10^{16} \text{ cm}^{-3}$, and

$7.88 \times 10^{16} \text{ cm}^{-3}$; (ii) SC-630: $1.02 \times 10^{15} \text{ cm}^{-3}$, and $2.47 \times 10^{15} \text{ cm}^{-3}$; (iii) SC-700: $7.63 \times 10^{16} \text{ cm}^{-3}$, $1.33 \times 10^{16} \text{ cm}^{-3}$, and $2.8 \times 10^{15} \text{ cm}^{-3}$; (iv) SCycle, $1.38 \times 10^{17} \text{ cm}^{-3}$ and $3.23 \times 10^{16} \text{ cm}^{-3}$.

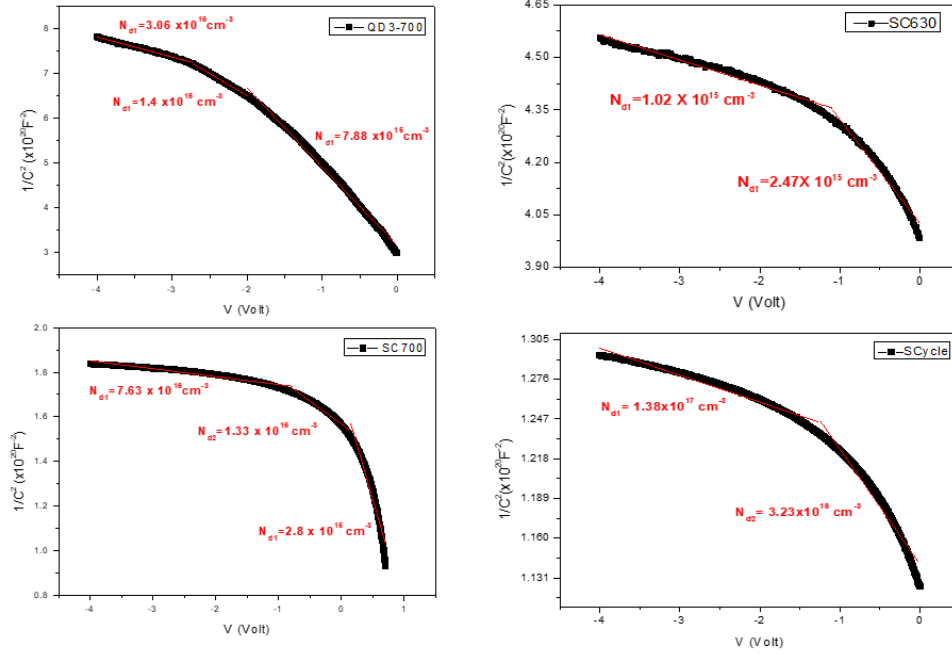


Figure 6.26: Variation of $1/C^2$ versus V for QD 3-700, SC630, SC700 and SCycle samples at room temperature.

6.3.4.3 DLTS AND LDLTS MEASUREMENTS

DLTS measurements were carried out on p-i-n structures with no QDs in the i-region and InAs QDs-based IBSC solar devices to identify the electrically active defects [30, 31]. The parameters used for these measurements were reverse bias voltage $V_r = -1\text{V}$ and -4V , a forward pulse voltage $V_p = 0\text{V}$, a filling pulse width $t_p = 1 \text{ ms}$, and rate window of 200 s^{-1} for all samples. Samples were scanned from 20K to 450K. Figure 6.27 displays the DLTS signals detected in all four samples at different reverse biases, specifically -1V and -4V . The different biases were used to investigate traps near the interface and away from the junction interface of the p-

i-n and QDs-based IBSC devices. As can clearly be seen in Figure 6.27, QD3-700 has a dominant peak ~ 400 K.

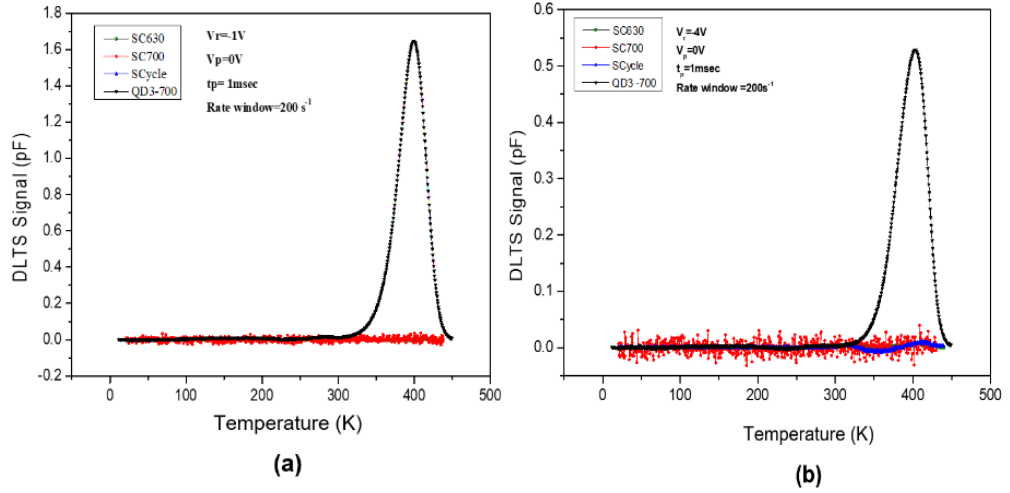


Figure 6.27: DLTS signals for SC700, SC630, SCycle and QD3-700, samples at (a) $V_r = -1$ V and (b) $V_r = -4$ V with $V_p = 0$ V.

Figures 6.28a and 6.28b show DLTS spectra of InAs QDs-based IBSC device (QD3-700) and control sample (SC630 which does not incorporate InAs QDs), respectively, for $V_r = -1$ and -4 V. In QD3-700 sample, one sharp peak at 400K was detected along with two small peaks (see inset in Figures 6.28a and 6.28b). However, for SC630 sample, three different peaks were observed but with much reduced amplitudes. One of them is a minority trap labelled HD2. The main differences in the DLTS spectra between the two samples are the nature and amplitude of the DLTS peaks. This difference could be related to the presence of QDs in the i-region of QD 3-700 sample [33].

Figure 6.29 shows the DLTS spectra of SC700 and SCycle which do not incorporate InAs QDs. From these spectra, it can be seen that no significant trap is

observed in SC700 sample but in SCycle sample two majority traps, namely EF1 and EF3, and one minority trap HF2 are detected.

In addition, at high reverse biases as shown Figures 6.28a and 6.28b for all devices, it was observed that the amplitude of all DLTS peaks decrease. This behaviour shows that the concentration of the trap decreases away from the interface. For example, as seen in Figure 6.28 for QD3-700, the amplitude of the DLTS peak observed in the temperature range of 300 - 450K is lower near the interface (for -1V: EC1^{-1V}) than the peak further away from the interface [-4V (EC1^{-4V})]. This indicates that this trap has higher concentration near the interface of the p-i-n junction.

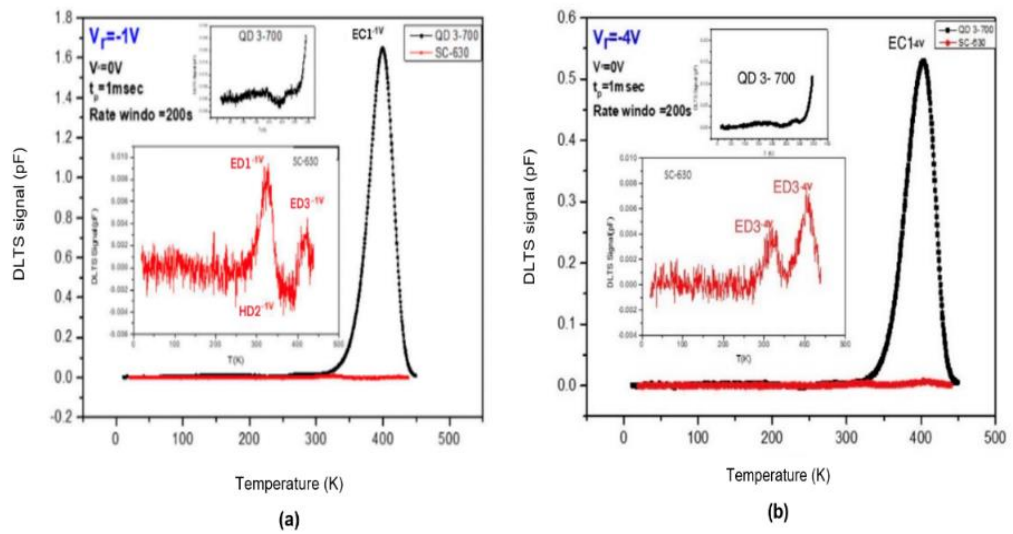


Figure 6.28: DLTS spectra of QD3-700 and SC630 samples at (a) $V_r = -1V$ and (b) $V_r = -4V$ with $V_p = 0V$

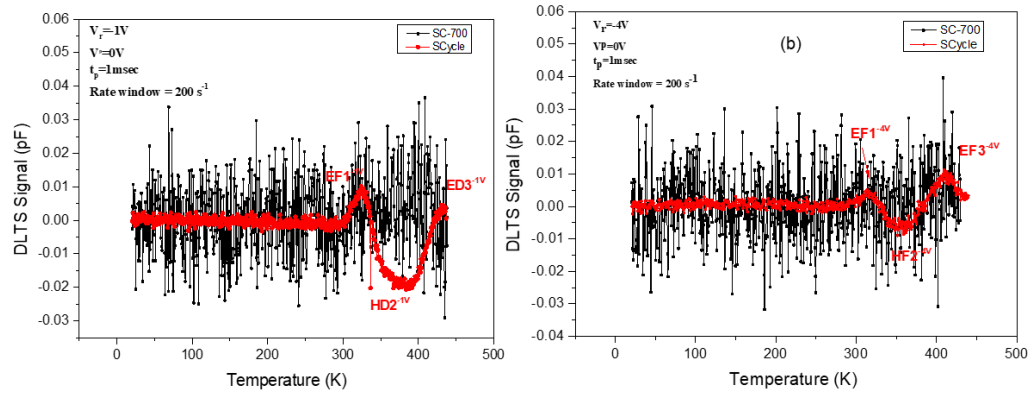


Figure 6.29: DLTS signals of SC700 and SCycle samples at (a) $V_r = -1V$ and (b) $V_r = -4V$ with $V_p = 0V$.

In addition, in QD3-700, two broad peaks with small amplitudes were observed in the temperature ranges of 100-250K and 250-300K. Due to the broadness of these peaks, high resolution LDLS was used to resolve them [31]. Furthermore, at high temperatures (400 - 440K) and reverse applied biases of -1V (near the junction interface) and -4V (away from the junction interface), the observed DLTS signals for SC630 were similar but with much smaller amplitudes at -4V. However, the DLTS peaks observed in SC630 control sample are broad extending over a wide range of temperatures, indicating that there may be more peaks in this range. In SC630 sample which does not incorporate QDs for $V_r = -1V$ (Figure 6.28 a), $HB2^{-1V}$ trap exhibits a negative DLTS signal in the temperature range 340K - 400K, meaning it is a hole trap (minority carrier). Furthermore, at high temperatures (400 - 440K) and reverse applied biases of -1V (near the junction interface) and -4V (away from the junction interface), the observed DLTS signals for SC630 were similar but with much smaller amplitudes at -4V. However, the DLTS peaks observed in SC630 control sample are broad, indicating that there may be more peaks in this range. On the other hand, no defects were detected in SC700 sample while three traps are present in SCycle sample. It is worth pointing out that SC630

and SCycle (not containing InAs QDs) have similar number of defects (two electron traps and one hole trap) but with different DLTS peak amplitudes. This difference in amplitude in the DLTS spectra could be attributed to the low growth temperature of 500 °C used in the part of the structure which incorporated InAs QDs in SCycle. This thermal cycling shown in Figure 6.2b was used to mimic the growth condition of QD3-700 sample.

The activation energy (E_T), trap concentration (N_T), and capture cross-section (σ_∞) of defects were obtained for all three samples from the Arrhenius plot of $\ln(e_n/T^2)$ versus ($1000/T$), as shown in Figures 6.30 and 6.31 and Table 6.4 for reverse biases of -1V and -4V.

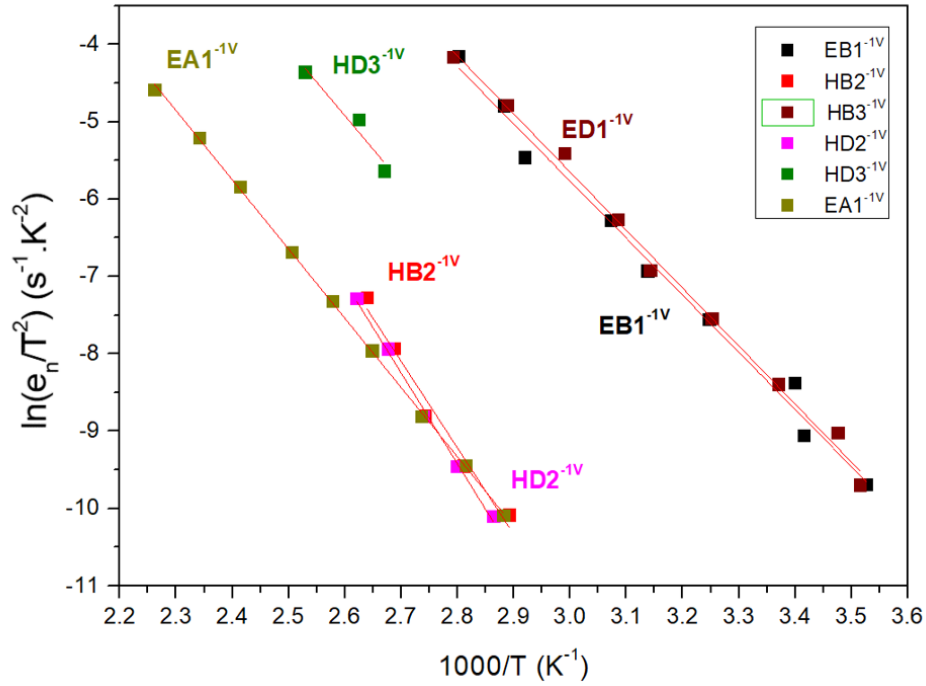


Figure 6.30: Arrhenius plots for SC630, SC700 and SCycle samples at $V_r = -1\text{V}$. C, D and F refer to QD3-700, SC630 and SCycle, respectively. QD3-700 is not included in this figure because no detectable defects were observed.

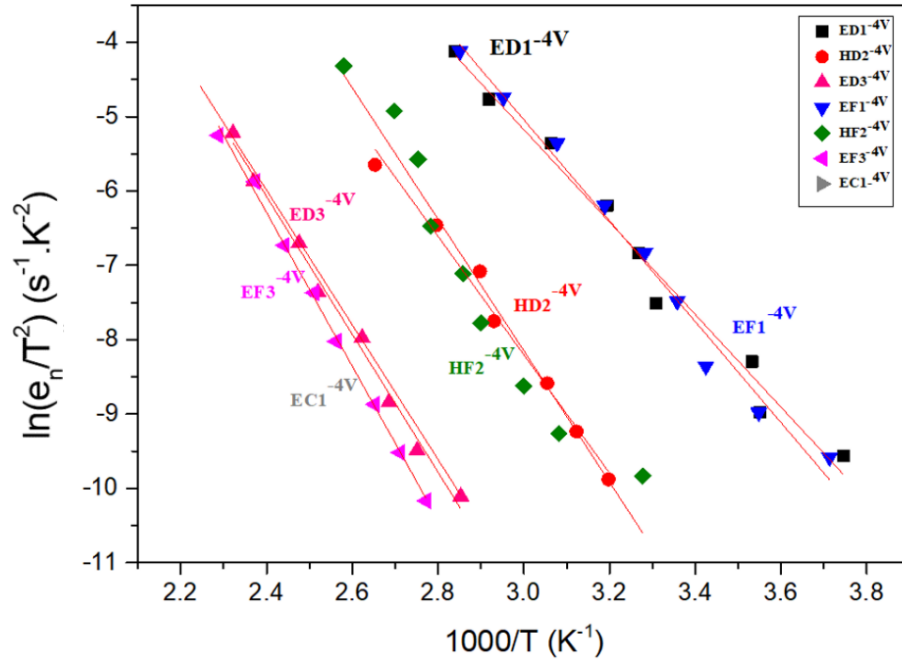


Figure 6.31: Arrhenius plots for QD3-700, SC630 and SCycle samples at $V_r = -4V$. C, D and F refer to QD3-700, SC630 and SCycle, respectively. SC700 is not included in this figure because no detectable defects were observed.

Table 6.4 shows the trap parameters for $V_r = -1$ and $-4V$. For example, at $V_r = -1V$, $EC1^{-1V}$ in QD3-700 sample is a deep-level trap with an activation energy of ~ 0.77 eV. Moreover, $ED1^{-1V}$ and $HD2^{-1V}$ in SC630 sample are also deep-level traps, and they have energies of 0.64 ± 0.03 eV and 0.96 ± 0.09 eV, respectively. In addition, at $V_r = -1V$ SCycle sample has three deep-level traps: $EF1^{-1V}$, $HF2^{-1V}$, and $EF3^{-1V}$ with activation energies of 0.65 ± 0.02 eV, 1.01 ± 0.04 eV, and 0.75 ± 0.17 eV, respectively. However, it is important to note that the DLTS signals observed in all samples at high temperatures and corresponding to the electrons traps $EC1^{-1V}$, $EC1^{-4V}$, $ED2^{-4V}$ and $EF3^{-1V}$ with similar activation energies (~ 0.78 eV), could have the same origin. This trap may be attributed to the well-known EL2 defect in GaAs. This is a complex defect involving As_{Ga} and an arsenic interstitial [23-25, 34]. Additionally, $ED1^{-4V}$ and $EF1^{-4V}$ have an energy of ~ 0.56 eV, which could be

associated with EL3 (0.56 eV). This trap is likely related to the complexes of off-centre substitutional oxygen on arsenic sites (oc-OAs) [52]. However, the hole traps $\text{HD2}^{-1\text{V}}$ and $\text{HF2}^{-1\text{V}}$ with activation energies of ~ 0.96 and 1.01 eV, respectively, could be of the same origin. These hole traps could be related to a particular configuration of the As vacancy–interstitial pair [53]. However, these activation energies also agree well with the energy level of arsenic antisite $\text{As}^{++}_{\text{Ga}}$ (0.90 eV) within the band gap of GaAs [54]. Moreover, the deep electron traps $\text{ED1}^{-1\text{V}}$, $\text{EF1}^{-1\text{V}}$ and $\text{EF3}^{-4\text{V}}$ with activation energies 0.64, 0.65 and 0.89 eV, respectively could not be precisely identified in this work. However, $\text{EF3}^{-4\text{V}}$ (0.89 eV) could be tentatively ascribed to EL2 trap.

Table 6.4: Traps parameters (activation energy, capture cross-section and concentration) of QD3-700, SC630, SC700 and SCycle samples at ($V_r = -1$ V, $V_p = 0$ V) and ($V_r = -4$ V, $V_p = 0$ V), with $t_p = 1$ ms at rate window = 200 s⁻¹.

Sample	Reverse bias (V)	Trap	Activation Energy (eV)	Trap concentration (cm ⁻³)	Capture cross section (cm ⁻²)
QD3-700	-1	EC1 ^{-1V} (EL2) [23-25, 34].	0.77 ± 0.01	2.2 x 10 ¹⁵	3.8 x 10 ⁻¹⁵
	-4	EC1 ^{-4V} (EL2) [23-25, 34].	0.78 ± 0.01	2.3 x 10 ¹⁴	3.9 x 10 ⁻¹⁵
SC630	-1	ED1 ^{-1V}	0.64 ± 0.02	9.5 x 10 ¹¹	6.7x10 ⁻¹⁵
		HD2 ^{-1V}	0.96 ± 0.09	4.1 x 10 ¹¹	2.2 x 10 ⁻¹²
	-4	ED1 ^{-4V} (EL3)[52]	0.54 ± 0.03	2.5 x 10 ¹¹	4.1 x 10 ⁻¹⁶
		ED2 ^{-4V} (EL2)	0.79 ± 0.03	3.1 x 10 ¹¹	5.9 x 10 ⁻¹⁵
SC700	SC-700 does not have any detectable defects				
SCycle	-1	EF1 ^{-1V}	0.65 ± 0.02	7.3 x 10 ¹²	1.2 x 10 ⁻¹⁴
		HF2 ^{-1V}	1.01 ± 0.04	1.5 x 10 ¹³	8.8 x 10 ⁻¹²
		EF3 ^{-1V} (EL2)	0.75 ± 0.17	1.5 x 10 ¹³	2.5 x 10 ⁻¹⁴
	-4	EF1 ^{-4V} (EL3)[52]	0.59 ± 0.03	1.8 x 10 ¹³	2.6 x 10 ⁻¹⁵
		HF2 ^{-4V}	0.76 ± 0.07	2.7 x 10 ¹³	5.4 x 10 ⁻¹⁴
		EF3 ^{-4V}	0.89 ± 0.02	3.5 x 10 ¹³	6.1 x 10 ⁻¹⁴

6.4 DISCUSSION OF THE ROLE OF THE DEFECTS ON THE PERFORMANCE OF THE QD-IBSCs

The current density versus voltage (J-V) characteristics measured under standard test conditions (AM1.5G, 100 mW/cm^2 and 25°C) for QD solar cells and SC700 reference sample, which does not incorporate QDs in the i-region that was grown at 700°C , are shown in Figure 6.32. The measurements were performed at Pontifical Catholic University of Rio de Janeiro, Brazil.

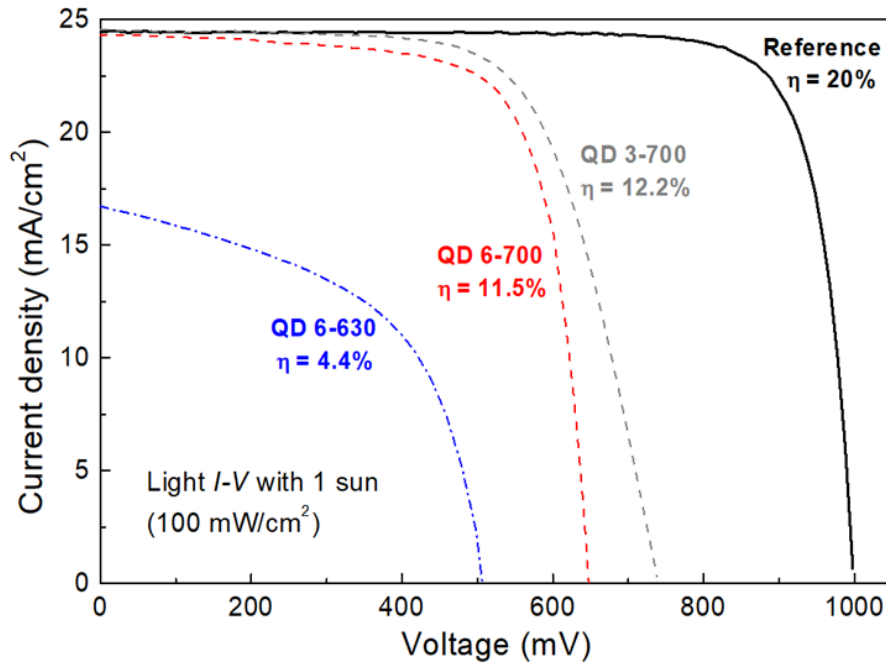


Figure 6.32: Current density–Voltage characteristics of QD6-630, QD6-700 and QD3-700, and reference (SC-700) samples.

It can be clearly seen from Figure 6.32 that the presence of QD reduces V_{oc} and the low growth temperature of the i-region significantly reduces short-circuit current density (J_{sc}). The V_{oc} values of QD6-630, QD6-700, QD3-700 and reference SC-700 samples are 503.3, 653.3, 733.3 and 1000 mV, respectively.

QD6-700 and QD3-700 have an I_{sc} value of $\sim 24.4 \text{ mA/cm}^2$ similar to that of the reference sample (SC-700). However, QD6-630 sample has the lowest I_{sc} value of 16.74 mA/cm^2 .

The performance indicators of these solar cells are shown in Table 6-5. From the current density given by equation 6.3 obtained using the solar cell equivalent circuit model, it can be inferred that V_{oc} is highly dependent on the shunt resistance (R_{SH}):

$$J = J_L - J_0 \left[\exp\left(\frac{qV}{nK_B T}\right) - 1 \right] - \frac{V}{AR_{SH}} \quad (6.3)$$

where J_L is the current density generated by light, J_0 is the drift current density of the diode, n is the ideal factor of the diode, K_B is the Boltzmann constant, T is the temperature, and A is the area of the device. R_{SH} times the sample area (A) is determined by the negative value of the reciprocal of the J-V curve at a voltage close to J_{sc} . It is found that for the reference sample SC-700, R_{SH} is about 20 times larger than that of QD6-630 sample. It can be seen from Table 6.5 that the larger R_{SH} , the larger V_{oc} . Low R_{SH} indicates that the sample has an alternate current path, which is attributed to the defect that provides low-energy recombination for carriers.

The EL2 defect exists in all these QD solar cell structures except the reference sample SC-700, and the concentration rises from zero for the reference cell to $1.2 \times 10^{16} \text{ cm}^{-3}$ for the QD6-630 sample.

A strong correlation was observed between the increase in the EL2 concentration and the decrease in V_{oc} and R_{SH} . This revealed the significant role of the EL2 trap

in impeding the performance of the devices. The concentration of EL2 in these different solar cells is shown in Table (6.5).

Table 6.5: Room temperature short circuit Current density (J_{sc}), open circuit voltage (V_{oc}), fill factor (FF), conversion efficiency (η), and shunt resistance (R_{SH}), and EL2 concentration for SC700, QD6-630, QD6-700 and QD3-700 samples.

Sample	J_{sc} (mA/cm ²)	V_{oc} (V)	FF	η (%)	R_{SH} (K Ω)	EL2 concentration (cm ⁻³)	
						-1V	-4V
SC-700 (Reference)	24.4	0.998	0.82	20	35.5 $\pm$ 6.2	-	-
QD6-630	16.8	0.511	0.52	4.4	1.81 $\pm$ 0.03	1.2x10 ¹⁶	-
QD6-700	24.4	0.648	0.73	11.5	8.90 $\pm$ 0.53	1.33x10 ¹⁵	-
QD3-700	24.1	0.738	0.67	12.2	31.0 $\pm$ 3.2	2.2 x10 ¹⁵	2.3x10 ¹⁴

The V_{oc} of QD IBSC is expected to be lower than that of the reference sample without QDs [4], which is mainly due to the partial thermal extraction of carriers from the electron QD level, resulting in a reduction of the effective band gap of the active region. Nonetheless, it should be noted that the samples grown at 700°C experience higher Ga diffusion into the InAs QDs resulting in an increase of their fundamental transition energy. However, it is estimated that this increase in transition energy would be at most 80 meV [27] far below the 250 meV needed to

explain the measured increase in Voc. A similar connection between EL2 concentration and Voc has been reported for conventional solar cells which were grown at different growth rates [22].

In the case of QD IBSC, the low temperature range required for QD deposition further highlights this effect and facilitates the formation of such defects, as described above. SCAPS (solver for drift diffusion model, under different loss scenarios [55]) has been used by our collaborators at Sao Carlos University, Brazil, to simulate the I-V curves of sample QD3-700 (not shown here) to quantitatively estimate the impact of each loss source on Voc.

Based on this analysis, it can be inferred that the effective band gap energy of the intrinsic layer is 1.32 eV (reduced by 100 meV), which reduces Voc by 27% (96 mV). At the same time, the detected defect contributes 73% (266 mV) of the total loss.

It is important to note that according to the J-V curves of sample QD3-700, the slope around Voc is significantly less steep than the other QDs samples, indicating that its series resistance is higher. This observation could be related to the presence of the defects under investigation. However, the obtained data disagree with this claim because QD3-700 exhibits the best figures of merit and the lowest defect concentration. This could be an artifact attributed to a processing step. On the other hand, it is important to note that Jsc is mainly affected by the growth temperature of the i-region. The obtained results indicate that when the QDs are annealed at a temperature of 700 °C, the origin for such a large reduction in Jsc is suppressed. A reduction of Jsc is usually associated with a large number of Shockley Read Hall (SRH) recombination [56, 57].

6. 5 CONCLUSIONS

I-V, C-V, DLTS and Laplace-DLTS techniques were used to investigate deep-level defects in p-i-n InAs QDs based intermediate band solar cells and conventional solar cells with equivalent structures without quantum dots grown by MOVPE technique.

From J-V measurements, some of the electrical parameters such as: ideality factor (n), built-in potential energy (V_{bi}) and series resistance (R_s) at room temperature for QD6-700 and QD3-700 were determined. The ideality factor was higher in QD3-700 sample (1.82) than that of QD6-700 (1.54). Moreover, the built-in potential energy was similar in both samples, namely 0.65 eV and 0.67 eV in QD6-700 and QD3-700, respectively. The series resistance was found to be higher in QD6-700 (2.10Ω) than QD3-700 (1.6Ω). One could conclude that sample QD6-700 has better electrical properties than sample QD3-700 due to the lower leakage currents and less number of defects present in sample QD6-700.

The well-known trap level EL2 defect in GaAs (0.82 eV) was present in all samples, and its concentration rose from zero for the reference cell to $1.2 \times 10^{16} \text{ cm}^{-3}$ for the QD6-630 sample. Moreover, the EL5 defect with an activation energy of $\sim 0.42 \text{ eV}$ was also observed in QD6-700 and QD6-630 samples. On the other hand, EL3 defect with an activation energy of $\sim 0.595 \text{ eV}$ was detected in QD6-630, SC630 and SCycle samples.

It can clearly be seen that the presence of electrically active defects which have relatively high concentrations ($\geq 10^{15} \text{ cm}^{-3}$), impedes the solar cells' figures of merit.

The requirement for low growth temperatures for the deposition of QDs in QD-IBSCs or any QD solar cell is a key restriction since it promotes the nucleation of such defects.

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CHAPTER 7: ELECTRICAL AND OPTICAL of SELF-ASSEMBLED InAs QUANTUM DOTS LASERS GROWN ON GALLIUM ARSENIDE AND SILICON SUBSTRATES BY MOLECULAR BEAM EPITAXY

In this chapter, the effects of the substrate material on the electrical and optical properties of self-assembled InAs QDs based laser structures will be reported. Two InAs QD laser structures with similar active regions grown on GaAs and Si substrates using strain reducing layer (SRL) consisting of GaAs/InGaAs have been investigated using Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM), Photoluminescence (PL), current-voltage (I-V), capacitance-voltage (C-V), and Deep Level Transient Spectroscopy (DLTS) measurements.

7.1 INTRODUCTION

Self-assembled quantum dots (QDs) are very promising nanostructures for a wide range of applications in optoelectronics such as lasers, photodetectors, amplifiers, and solar cells [1-3]. Considerable efforts have been devoted to investigating QDs lasers as an innovative way to enhance the gain of quantum well (QW) lasers. Quantum dot lasers were first produced in 1982 and their performance has been enhanced considerably over time [4] due improvement in growth techniques, optimization of growth conditions and layer design.

Among the QDs systems, InAs QDs attracted an intensive research activity motivated by the possibility to achieve light emission covering the optical communication wavelength bands [5-7]. Many strategies have been used for the

extension of the wavelength including growing larger QDs [8] and using strain reducing layer (SRL) [7, 9]. In spite of photoluminescence (PL) emissions closer to 1.3 μm have been observed [7-9], the larger lattice-mismatch strain between GaAs and InAs ($\sim 7\%$) had resulted in inhomogeneous dot size distribution and smaller dot density limiting the device performance. It was found that the best way to preserve InAs QD size is the use of SRL [10-12]. Huang et al. [13] reported that $\text{GaAs}_{1-x}\text{Sb}_x$ SRL improved the performance of InAs/GaAs quantum-dot infrared photodetectors. Recently, Salhi et al. [7, 10] have shown that the emission wavelength reached 1.32 μm when the InAs QDs are either covered by InGaAs or GaAsSb, while the incorporation of 1% of Sb in the InGaAs SRL extends further the wavelength to 1.37 μm . Due to their potential uses in advanced optical fibre communication systems [14-19], high-performance GaAs-based quantum dot (QD) lasers are of significant interest. QDs have the benefit of being able to produce low threshold current density and large differential gain due to the increased density of states resulting from three-dimensional confinement of carriers [15, 16, 19-22]. InAs QD lasers have been found to exhibit high power and efficiency, and temperature insensitivity [16, 19, 21, 23]. However, the intrinsically low surface density (NQD) of a single-layer QD structure usually limits laser performance [19] [24].

It is important to point out that GaAs-based QD lasers operating at 1.3 μm are an attractive alternative to InP-based QW lasers, which require more expensive InP substrates and have poor temperature performance [25, 26]. In addition, InP-based 1.3 μm QW lasers have a low characteristic temperature (T_0) of about 60 K, which can be enhanced to about 100 K by using InGaAlAs confining layers. A perfect QD laser, on the other hand, should have a T_0 of infinity. Researchers have enhanced

T_0 to ~ 150 K by using the technique of p-type modulation doping of quantum dots [25-27].

Extensive work on InAs QDs grown on GaAs substrates has been reported in the literature, however, research in the use of different substrate materials such as silicon to achieve an ideal and full integration of photonic and electronic systems [28] is still under development.

Direct epitaxial growth of III-V semiconductor material on silicon substrates offers a viable method for producing a low-cost, large-scale, high-yield on-chip light sources. However, large differences in their properties, such lattice constant and thermal expansion coefficient, cause several monolithic integration difficulties. A high number of defects are produced in the epitaxial layer due to the large lattice mismatch (4.1%) and difference in thermal expansion coefficient (200%) between GaAs and Si. The type of faults that form at the interface include threading dislocations (TDs), microcracks, and antiphase boundaries, among other defects [22]. These defects, which might result in non-radiative recombination centres, have a significant impact on the quality and performance of both the epitaxial layers and the device characteristics. Many methods, such as dislocation filter layers (DFLs) and thermal annealing (TA), have been adopted to overcome these obstacles and increase device performance. It is worth pointing out that the use of QDs to reduce the dislocation effect was proposed in 1991 [29]. The reported results of In GaAs QDs lasers epitaxially grown on silicon substrates seem to support the hypothesis that quantum dot nanostructures are less sensitive to dislocations than quantum wells [29-31].

The needs of low threshold current density (J_{th}), insensitivity to TDs, and high temperature stability, require specific properties of quantum dots as active layers in semiconductor lasers [22]. Therefore, studies to find suitable capping layer (CL) or SRL materials for covering InAs QDs grown on both GaAs and Si substrates are highly motivated by an enhancement of their morphology quality, electrical and optical properties, as well as exploring possibilities for monolithic photonic integration on silicon platform.

In this chapter, the effects of the substrate material and SRL on the morphology, optical and electrical properties of InAs QDs based laser structures are reported. Two InAs QD laser structures with similar active regions grown on GaAs and Si substrates using strain reducing layer (SRL) consisting of GaAs/InGaAs have been investigated. It is well known that there are many challenges to achieve high-quality epitaxial growth of III-V materials on Si. The lattice and thermal expansion mismatches between silicon and most III-V materials are the most important of these challenges. However, to alleviate the problems associated with the lattice mismatch, InGaAs/GaAs multilayers defect filter layers are used. It was observed that the type of the substrate has important effect of the size of QDs, PL properties and the electrically active defects in these structures introduced during growth and/or processing. Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM), Photoluminescence (PL), current-voltage (I-V), capacitance-voltage (C-V), and Deep Level Transient Spectroscopy (DLTS) measurements have been used.

7.2 SAMPLE GROWTH DETAILS AND STRUCTURES

The two InAs QD lasers studied in this work were p-i-n laser diodes with InAs self-assembled QDs incorporated in the i-region grown on (100) GaAs (sample A: control sample) and (100) Si (sample B) substrates using a Veeco Gen20A Molecular Beam Epitaxy system (MBE) system equipped with a valved cracker to generate As₂. These samples were grown at King Abdulaziz City for Science and Technology (KACST), in Riyadh, Saudi Arabia. The layer sequence of QDs sample A, grown on n-type GaAs substrate, is depicted in Figure 1(a) and consists of the following layers: a 50 nm n-type GaAs buffer layer, a 1500 nm n-type Al_{0.42}Ga_{0.58}As cladding layer, a 108 nm undoped GaAs spacer layer, 5× [2.5 monolayers (MLs) InAs QDs/6nm In_{0.15}Ga_{0.85}As (SRL)/ 40 nm GaAs], a 64 nm undoped GaAs spacer layer, a 1500 nm p-type Al_{0.42}Ga_{0.58}As cladding layer, a 300 nm p-type GaAs layer.

The InAs QDs were grown at 500 °C and at a growth rate of 0.03 ML/s. A short growth interruption under As₂ flux was introduced before the growth of the 6 nm-thick In_{0.15}Ga_{0.85}As Strain Reducing Layer followed by 10 nm-thick GaAs layer at the same temperature. The growth temperature was then ramped to 570 °C to grow the remaining GaAs cap layer. The spacers, claddings and contacts layers were grown at 570°C.

The laser structure on silicon substrate (Sample B), was grown by using the same process and growth conditions as the one used for sample A grown on a GaAs substrate except the buffer layer which is designed and used to reduce the defects resulting from lattice mismatch between Si and GaAs substrates. The defect filter undoped buffer layer consisted of 5 nm AlAs, 1000 nm GaAs, 4 periods of [6×

InGaAs (10nm)/GaAs (20nm)]/ nm GaAs], 5 periods of AlAs (10nm)/GaAs (10nm), 50 nm GaAs and 200nm Al_{0.5}Ga_{0.5}As (Fig.1b). More details regarding the growth of the dislocation filter can be found in reference [7]. The purpose of this specific buffer layer was to reduce dislocations between silicon substrate and the active layers due to the large lattice mismatch between Si and GaAs. The rest of the structures is similar to sample A. It is important to highlight that the formation of InAs QDs was verified by means of Reflection High Energy Electron Diffraction (RHEED) where a chevron patterns in the RHEED screen was clearly observed.

For atomic force microscopy (AFM) analysis, uncapped QDs grown on GaAs and Si (with dislocation filter) substrates were also grown. AFM was used to characterize the morphology of the uncapped QDs and the optical properties of the samples were characterized using temperature and power-dependent photoluminescence (PL). Transmission Electron Microscopy (TEM) was used for the structural analysis of InAs/InGaAs QDs grown on GaAs and Si substrates like the ones shown in Figure1.

Photoluminescence (PL) signal of both samples were investigated as a function of laser power and temperature using a Janis closed-loop helium cryostat. The samples were excited with a 532 nm solid state green laser. The PL spectra was collected in an Andor Shamrock 500i spectrometer coupled with a high sensitivity Andor iDus InGaAs CCD camera.

(a): Sample A (GaAs substrate)

(b): Sample B (Si substrate)

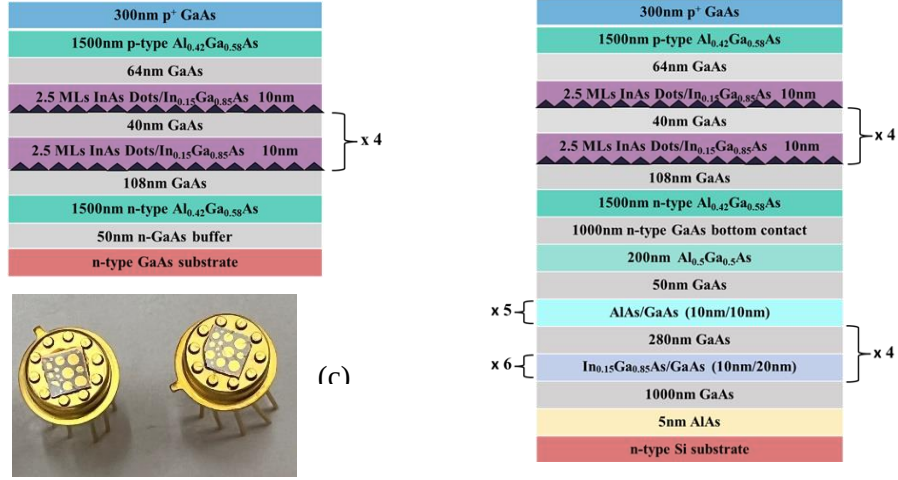


Figure 7.1: Schematic structure of QDs laser samples grown on (a) GaAs substrate (Sample A) and (b) on Si substrate (Sample B). (c) Photograph of samples mounted on TO5 header.

Atomic Force Microscopy (AFM) was used to characterize the morphology of the uncapped QDs and the results are shown in Figure 7.2 (a,b). The obtained values of the QDs' density is $\sim 1.8 \times 10^{10} \text{ cm}^{-2}$ for both samples grown on GaAs and Si substrates, however, we noticed a reduction of the QDs aspect ratio for the sample grown on Si. The average diameter and height of the QDs grown on GaAs and Si substrates were $30.8 \pm 2.1 \text{ nm}$ and $13.3 \pm 0.9 \text{ nm}$, and $30.7 \pm 4.2 \text{ nm}$ and $11.8 \pm 1.9 \text{ nm}$, respectively. During the capping process, the QDs size was reduced in both samples as showed in the bright field transmission electron microscopy (TEM) images (Figure 7.2 (c,d)). In fact, for both samples, the diameter ranges between 20 and 25nm and the height was reduced slightly to 10nm which is the same as the width of the In_{0.15}Ga_{0.85}As QWs (Figure 7.2 (c) and Figure 7.2 (d)).

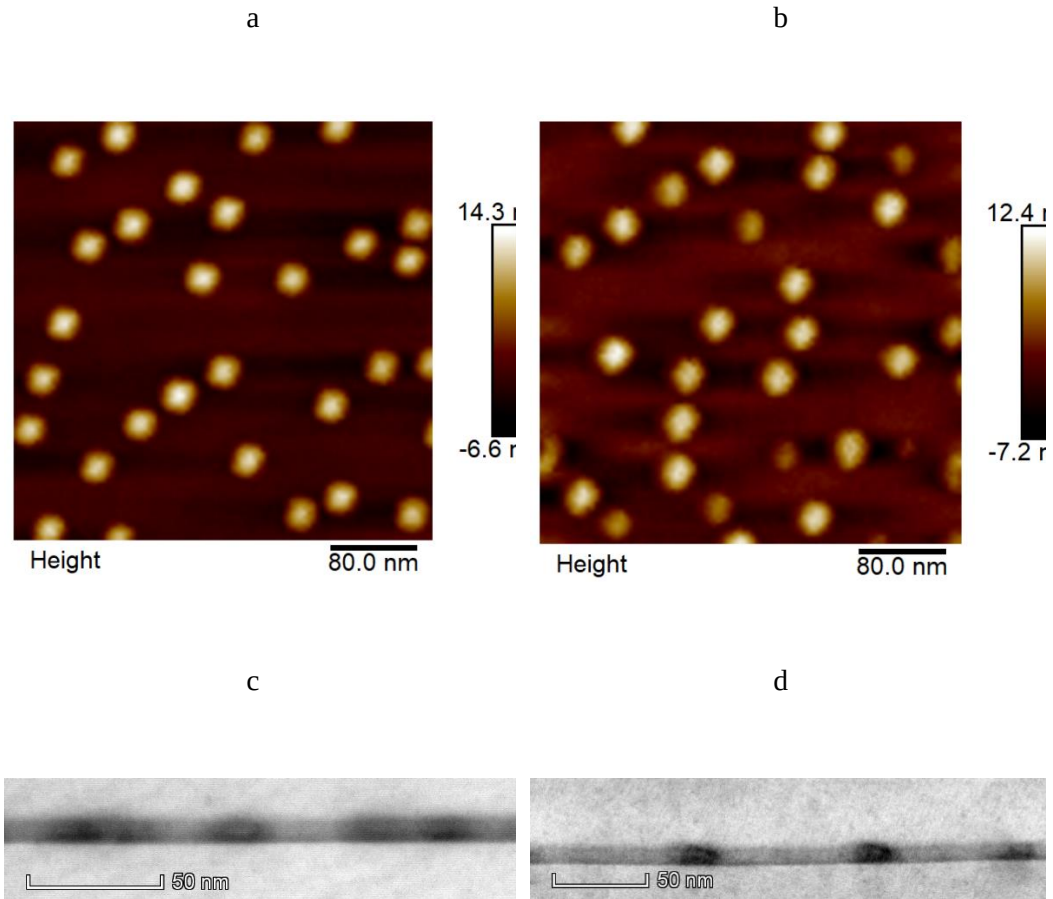


Figure 7.2. AFM images ($0.4\mu\text{m}\times 0.4\mu\text{m}$) of 2.5 MLs uncapped InAs QDs grown on (a) GaAs substrate and (b) Si substrate. Bright field TEM images of InAs/InGaAs QDs grown on GaAs substrate (c) and Si substrate (d).

From AFM and TEM results shown above, it is clear that dislocation filter and buffer layer have reduced the lattice mismatch effect on the growth of QDs on Si substrate as compared to the ones grown on GaAs.

7.3 RESULTS AND DISCUSSION

7.3.1 PHOTOLUMINESCENCE (PL) SPECTRA

Figure 7.3 shows typical PL spectra of (InGaAs/GaAs) QDs for Sample A (GaAs substrate) and Sample B (Si substrate), at 10 K and laser excitation power $P_{\text{EXC}}=40\text{mW}$. The dominant peak at 1.02 eV in Sample A is ascribed to interband transition occurring from the electron ground state E_0 to the heavy hole ground state HH_0 of the InAs dot (E_0 - HH_0). This PL band also exhibits some asymmetry in the high-energy side that could be ascribed to reduced filling of QDs excited states, not well distinguishable and resolved in PL spectra. In addition, a small peak at 1.477 eV is attributed to the GaAs capping layer. For Sample B, the observed E_0 (1.00 eV), E_1 (1.11 eV) and E_2 (1.07eV) PL peaks are well resolved and correspond to ground state transition, first and second excited states, respectively. It is plausible to suggest the presence of these same excited states peaks on the high energy shoulder of the PL spectra of Sample A, although they are not well pronounced and well resolved as in Sample B.

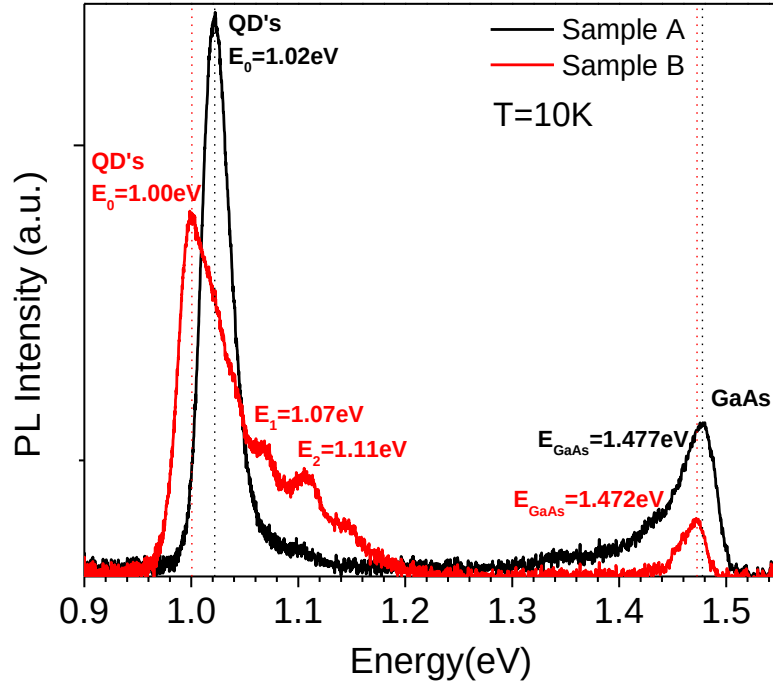


Figure 7.3: PL spectra of InGaAs/GaAs QDs grown on GaAs (Sample A) and silicon (Sample B) substrates at laser power $P_{\text{EXC}}=40\text{mW}$ and 10K. The PL bands attributed to InAs QDs and GaAs capping layer are indicated.

Figure 7.4 (a) presents the PL spectra for Sample A measured under different excitation power intensities at 10 K. At low excitation power (3 mW) only one symmetric peak is present at 1.02 eV (ground state transition E_0 to HH_0) and it remains nearly symmetric and unchanged up to an excitation power < 10 mW. With increasing excitation power, one additional peak is evidenced on the high-energy side of the PL spectra (1.1 eV, see inset), which corresponds to the filling of the first excited state E_1 .

Figure 7.4(c) shows the E_0 PL peak (1.00 eV) observed in Sample B, and it is clearly asymmetric and broader than the one detected in Sample A. The peak energy also

remains nearly unchanged with increasing excitation power. Therefore, the broad and asymmetric PL peak at 1.00 eV may reflect an inhomogeneous size distribution of the QDs, associated with E_0 transition induced from the finite-size distribution of the QDs as a consequence of carrier's random distribution at low temperatures. As the laser power increases, additional peaks are revealed. These peaks are probably due to excited states of the self-assembly QDs as discussed before. Figure 7.4 (b,d) shows that the QD PL intensity decreases for Sample A in the temperature range of 30-120 K, and quenches completely at temperatures above ~ 180 K, while for Sample B although the PL intensity at 10K is smaller than Sample A, it decreases and quenches completely at a higher temperature of ~ 220 K than Sample A. This decrease of the PL intensity as function of temperature is usually attributed to thermal escape of carriers from the QD ground states into the continuum followed by nonradiative recombination in the InGaAs and GaAs barriers (SRL and capping layer) at higher temperatures, when the thermal escape becomes dominant [32-34]. As will be discussed below, the difference in the PL intensity between the two samples shown in Figure 7.3 is mainly attributed to the different defect density in the structures.

The effect of the silicon substrate on the QDs' PL emission is clearly demonstrated by the following observations (from Sample A to Sample B): (i) the QD PL peak red-shifted from 1.02 eV to 1.00 eV; (ii) the PL intensity decreased by a factor of ~ 1.75 ; and (iii) the Full Width at Half Maximum (FWHM) increased from 31 meV to 46 meV (at a laser excitation power of 3mW). In our previous discussion we showed that the size of the QDs is similar for both samples, with a slight reduction of the aspect ratio from Sample A to Sample B, which is a negligible effect in terms of quantum confinement between the two samples. Although the redshift in the PL

energy has been reported and explained by different mechanisms along with strain and carrier confinement, in this case it is probably due to the residual strain of the GaAs/Si heterointerface rather than carrier confinement in the dots. This explanation is supported by the fact that the GaAs capping layer PL peak (Figure 7.3) is also redshifted for Sample B (1.472 eV) when compared to Sample A (1.477 eV), which is consistent with a residual biaxial strain induced by expansion mismatch between Si and GaAs [35, 36]. It is important to note that dislocation filters do not eliminate completely heterointerface defects, but have an important role to reduce their presence in Sample B [7, 33, 37, 38]. Additionally, the decrease of the PL intensity of Sample B as compared to Sample A indicates that the density of defects which act as nonradiative recombination centres was increased in the InAs QDs active region when Si substrate is used.

Furthermore, the QDs PL peak of Sample A (FWHM= 31 meV) at 10K and 3mW laser power excitation is narrower than that for Sample B (FWHM= 46 meV) by considering only the deconvoluted transition associated with E_0 . As discussed before, the distribution of the InAs QD size in the samples grown on GaAs and Si substrates is possibly affecting the changes observed in the PL results. The observed narrower PL FWHM for the GaAs substrate sample could indicate that the QD size distribution is better in Sample A than in Sample B, meaning that the QDs distribution is more inhomogeneous in Sample B than in Sample A, since the FWHM is inversely correlated with QD size and shape uniformity. It is important to note that the FWHM can also increase due to the introduction of defects in addition to the QDs becoming more inhomogeneous in terms of size and shape. These defects may have been caused by the relatively higher number of threading dislocations in the active region, while the increase of the FWHM confirms a less

uniform QD size distribution for this sample. Therefore, the use of Si substrates can have a profound impact on the optical properties of InAs QDs.

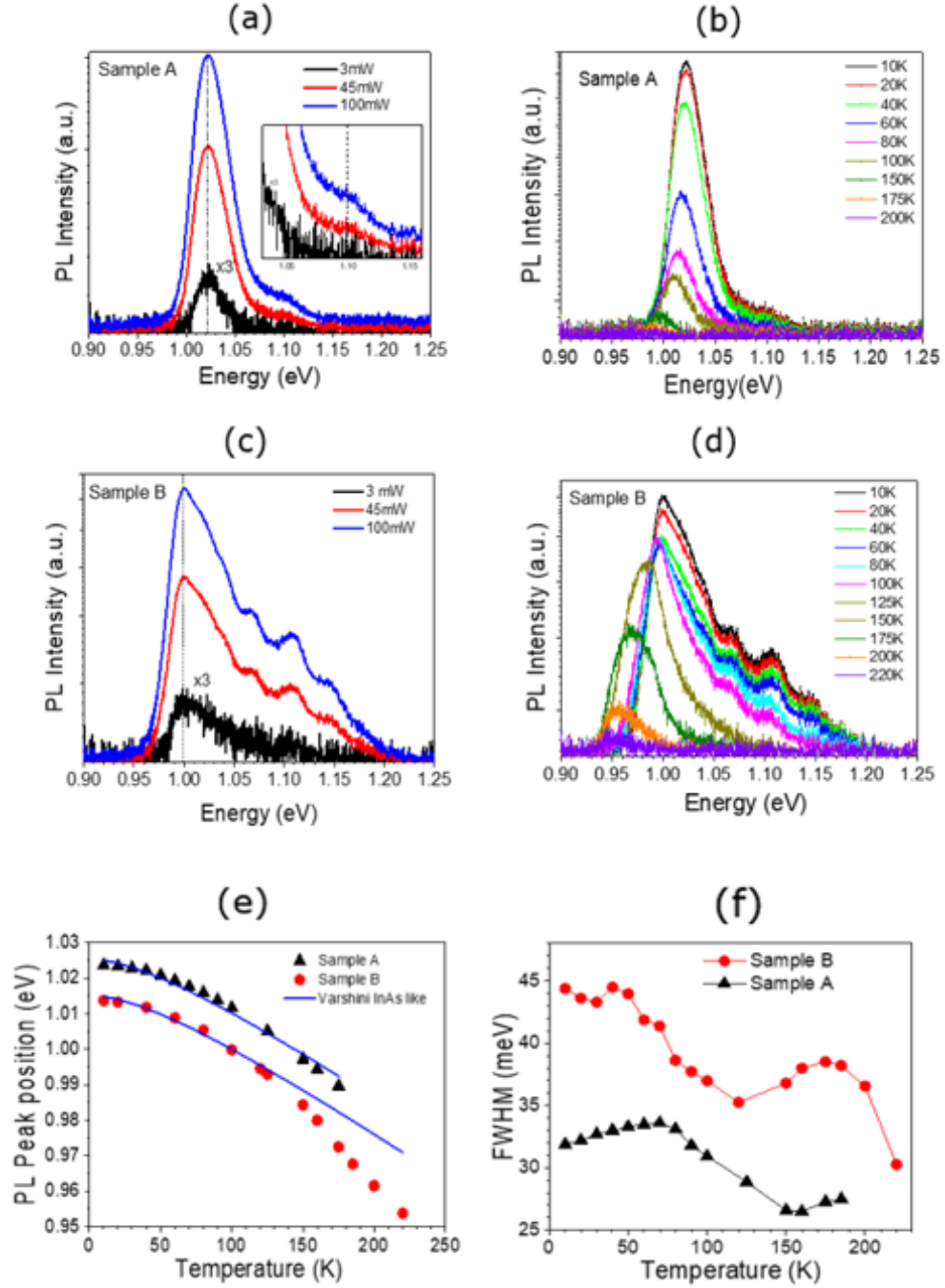


Figure 7.4: 10K PL spectra as function of laser power (a: Sample A, c: Sample B). PL spectra as function of temperature for a laser excitation power $P_{\text{EXC}}=40\text{mW}$ (b: Sample A, d: Sample B). (e) PL peak energy and (f) PL FWHM of E_0 transition as a function of temperature for InAs/GaAs QDs grown on GaAs (Sample A) and Silicon (Sample B) substrates at a laser excitation power $P_{\text{EXC}}=25\text{mW}$. Solid lines in (e) are the InAs band gap shrinkage obtained from Varshni law. The results of E_0 transition from PL data was obtained from the deconvoluted PL spectra (excluding effects of QD excited states).

Figure 7.4 (e) shows the E_0 PL peak as function of temperature as well as the InAs-like band gap decrease by using the Varshni approximation fitting [39]. The PL peaks match well with the band gap variation up to 150 K. However, the QD PL peak redshifts faster when further increasing the temperature. The competing mechanisms of the carrier's thermal escape and recapture between the QDs, results in the redshift of the PL peak energy and the narrowing of the FWHM as the temperature increases [34]. This behaviour indicates that the carriers experience a transfer from the smaller QDs with deeper energy levels to the larger QDs with shallower energy confinement under thermal excitation, which results in a lower interband emission energy and a red-shift of the PL peak position [40]. This same carrier transfer process could also be evidenced by the temperature dependence of the PL FWHM for E_0 transition for both samples as shown in Figure 7.4 (f), and will be discussed below.

The PL FWHM presents a similar trend for both samples, with a decrease of the FWHM as the sample's temperature increases. The PL FWHM variation with temperature is generally attributed to the carrier thermal redistribution amongst QDs with different sizes. A decrease of the FWHM together with a red shift of the PL emission, when the temperature rises up to 150 K, are usually observed in the mid temperature range and explained by thermal escape of carriers occurring at lower temperatures for high-energy dots and carriers being recaptured by dots emitting on the low-energy side of the distribution [32]. Sample B also shows the largest FWHM variation and has the highest FWHM for all temperature ranges. With a further increase of the temperature above 150 K, the broadening of PL FWHM is likely attributed to the electron-phonon scatter over QDs with different sizes [40, 41].

In general, our results indicate that the use of Si substrate combined with a SRL to grow InAs QDs is a promising approach to integrate them with Si technology. However, there are still some important issues for obtaining the appropriate design and materials for the dislocation filter at the Si/GaAs heterointerface in order to reduce biaxial strain and consequently improve the optical properties of the QDs.

7.3.2 CURRENT-VOLTAGE MEASUREMENTS

The current-voltage (I-V) characteristics at room temperature of both samples are shown in Figure 7.5. As clearly seen in Figure 7.5, the sample grown on Si substrate (Sample B) has a better I-V characteristics than the sample grown on GaAs substrate (Sample A). However, both samples display low reverse currents which make them suitable for DLTS and LDLTS measurements.

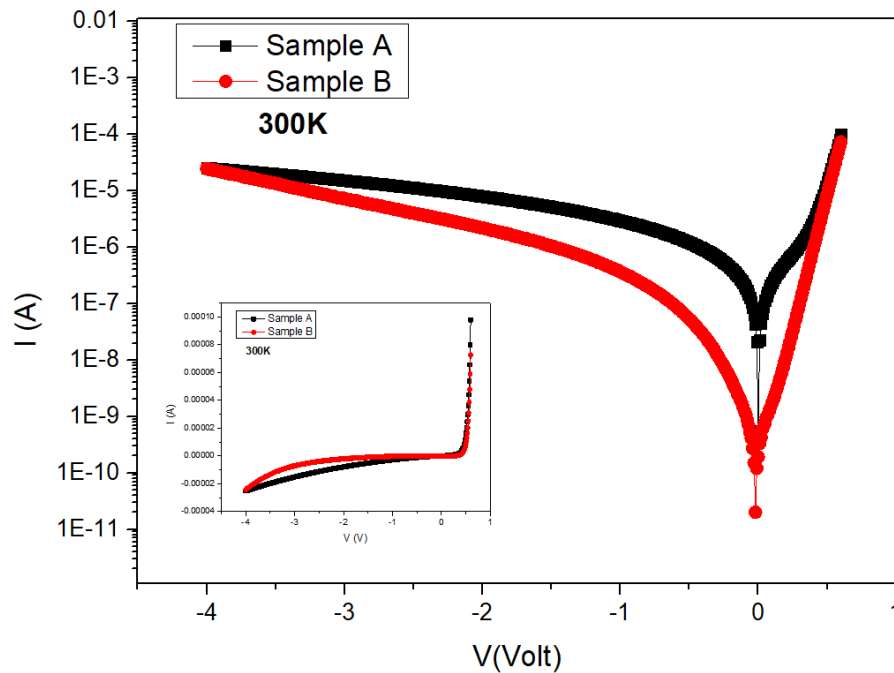


Figure 7.5: Semi-logarithmic I-V plots for Sample A (GaAs substrate) and Sample B (Si substrate). The inset shows the linear I-V plots.

In order to investigate the effect of different substrates on the electrical properties of InAs/InGaAs QDs laser structure diodes, I-V measurements at different temperatures were carried out. From these measurements, the electrical parameters such as ideality factor (n), built-in potential energy (V_{bi}), and series resistance (R_s) over the temperature 100 -420 K were obtained.

As discussed in Chapters 4 (section 4.3) and 6, Werner's approach was used to obtain the electrical parameters of both samples (n , V_{bi} and R_s) [42] by plotting G/I versus G (conductance) and $\ln(I)$ versus $(V-IR_s)$ as shown in Figure 7.6. Table 7.1 summarises these parameters at room temperature. Sample A has a lower ideality factor ($n= 1.54$), a slightly lower built-in potential energy ($V_{bi} = 0.63\text{eV}$) and a higher series resistance ($R_s = \sim 221\text{ k}\Omega$) when compared to sample B ($n= 1.71$; $V_{bi} = 0.78\text{ eV}$; $R_s = \sim 27\text{ k}\Omega$). The change of series resistance (R_s) as a function of temperature for both samples is shown in Figure 7. 7. R_s of both samples show a similar trend as function of temperature. From 110K to 140K the series resistance of both samples decreased sharply, but between 140K to 420K R_s showed only a slight decrease.

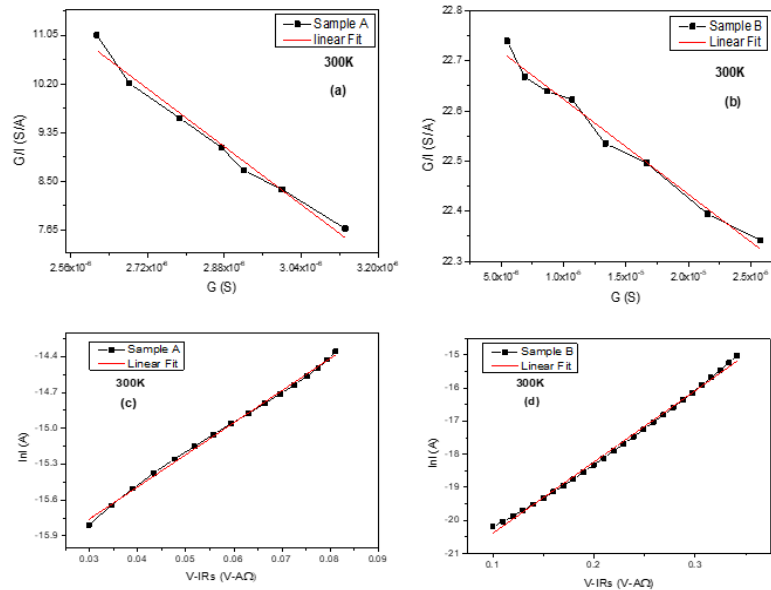


Figure 7.6: The plot of G/I versus G for (a) Sample A and (b) Sample B. The plot of $\ln(I)$ versus $(V-IR_s)$ for (c) Sample A and (d) Sample B.

Table 7.1: Ideality factor (n), built-in potential energy (V_{bi}) and series resistance (R_s) at room temperature for Samples A and B

Sample	n	V_{bi} (eV)	R_s (K Ω)
Sample A	1.54	0.63	221.58
Sample B	1.71	0.78	27.58

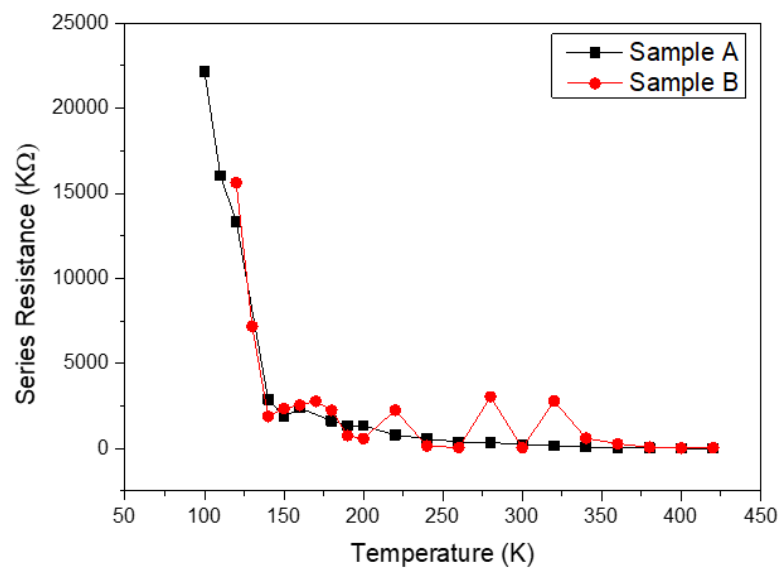


Figure 7.7: Temperature dependence of the experimental series resistance R_s determined from I–V characteristics of Samples A and B.

The plot of $\ln(I_0/T^2)$ versus $1000/T$ for Sample A in the temperature range 100–420 K is linear as shown in Figure 7.8 (a). Due to the diffusion process, which controls the conduction mechanism, this behaviour is expected. By using Equation (6.2) in Chapter 6, it is possible to calculate the saturation current [43]. However, it is noted

in Figure 7.8 (b) that Sample B shows a different behaviour. $\ln(I_0/T^2)$ increased significantly between 360-420K, but it decreased sharply between 110-360K.

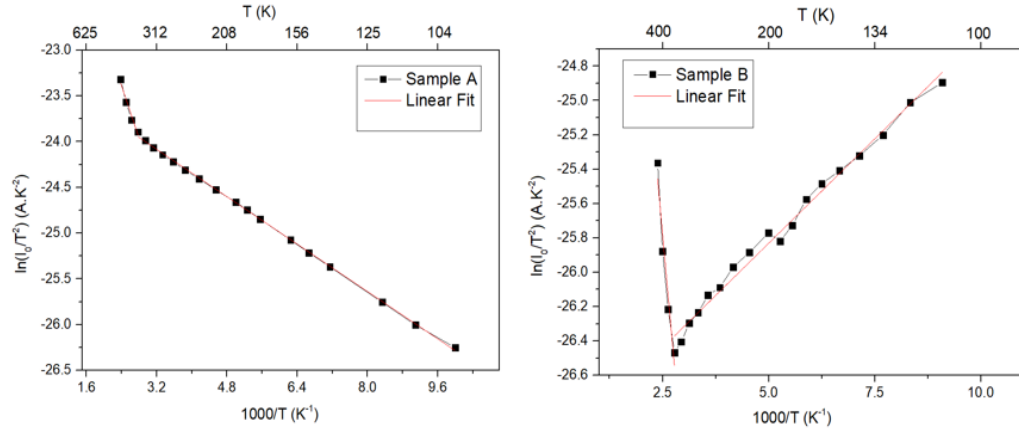


Figure 7.8: Plots of $\ln(I_0/T^2)$ versus $1000/T$ for (a) Sample A and (b) Sample B.

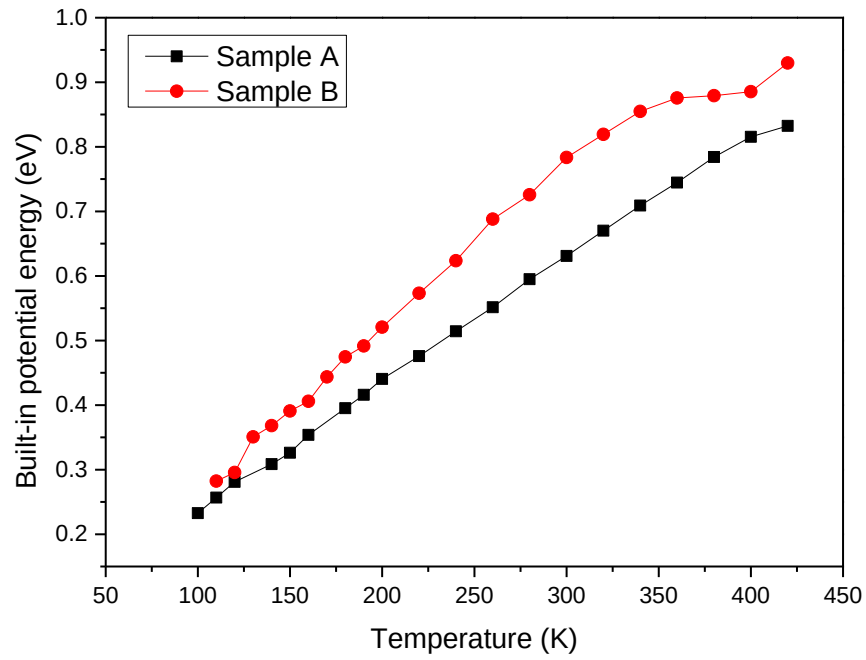


Figure 7.9: Plots of built-in potential energy (V_{bi}) versus temperature for both samples obtained from I–V characteristics.

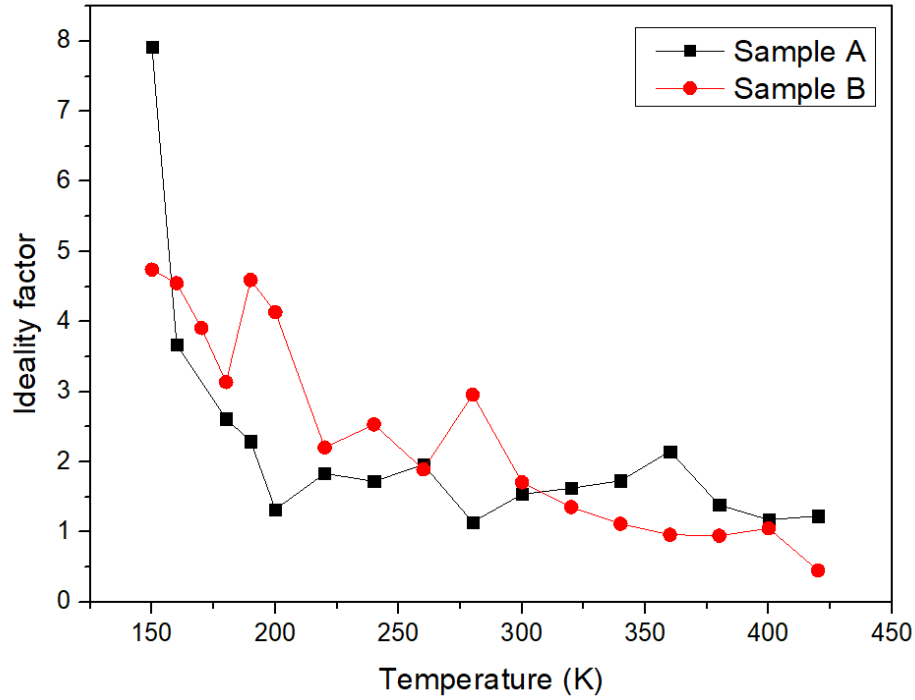


Figure 7.10: Plots of ideality factor (n) versus temperature for both samples obtained from J–V characteristics.

The temperature dependency of the built-in potential energy (V_{bi}) and ideality factor (n) for both samples is depicted in Figures 7.9 and 7.10, respectively.

The built-in potential energy of both samples increases with increasing temperatures; however, this increase is larger for sample B especially at higher temperatures. However, Sample B has an ideality factor greater than Sample A over the temperature range 150 – 300 K which could be due to the nonuniformity of interfacial charges. Moreover, at low temperatures the carriers are frozen and due to this, the current does not follow the diffusion process mechanism in both samples.

It should be noted that carriers may surmount lower potential energy at low temperatures, and the transport mechanism will be controlled by the current flowing through the regions with the lowest built-in potential energy.

Carriers acquire enough energy to surmount large potential energy when the temperature increases, which leads to an increase in built-in potential energy with temperature [44, 45].

Figure 7.11 (a and b) illustrates the plot V_{bi} versus n for both samples. As clearly seen in Figure 7.11 (a), this plot deviates from a linear relationship for sample A, and this behaviour may be attributed to the uncertainties in the calculation of the ideality factor [24, 46]. However, for sample B this plot follows a linear trend indicating an inhomogeneity of the built-in potential energy.

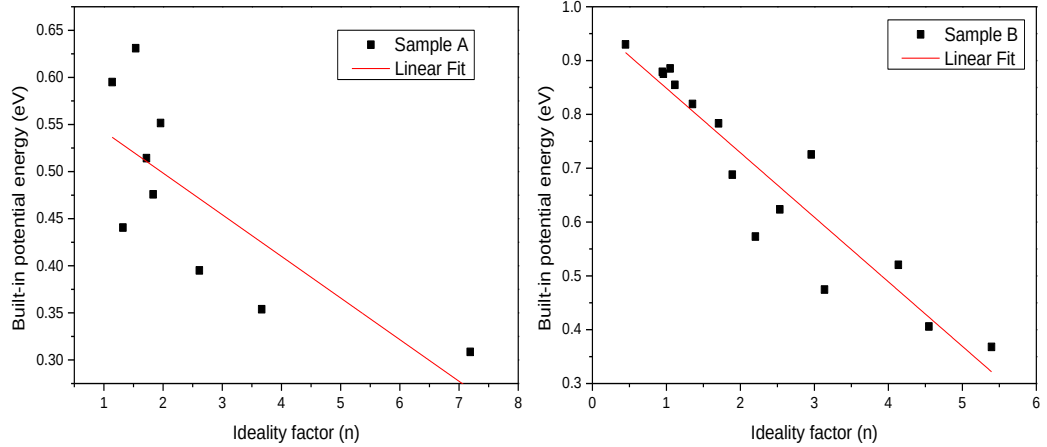


Figure 7.11: Built-in potential energy (V_{bi}) versus ideality factor (n) for (a) Sample A and (b) Sample B.

7.3.3 CAPACITANCE-VOLTAGE MEASUREMENTS

C-V measurements were recorded at 300 K using a Boonton 7200 capacitance meter to determine the free carrier concentration (N_d) of the two samples. Figure 7.12 shows that the change of capacitance at 300 K as a function of reverse bias has a similar trend in both samples, however, the capacitance of Sample A is higher than Sample B. This could possibly be attributed to a reduction of net ionized dopant concentration or higher defects that capture more free charge carriers in the sample grown on silicon substrate.

Figure 7.13 shows plots of $1/C^2$ versus reverse bias V for both samples at room temperature. From the slope of the best fit to the plot $1/C^2$ versus reverse bias the free carrier concentration N_d was obtained for both samples at room temperature. As indicated in Figure 13, both samples have similar free carrier concentrations and their concentration profiles are not uniform with distance from the junction. Values of free carrier concentrations for Sample A and Sample B are $4.02 \times 10^{17} \text{ cm}^{-3}$ and $2.90 \times 10^{17} \text{ cm}^{-3}$, and $4.02 \times 10^{17} \text{ cm}^{-3}$ and $2.16 \times 10^{17} \text{ cm}^{-3}$, respectively.

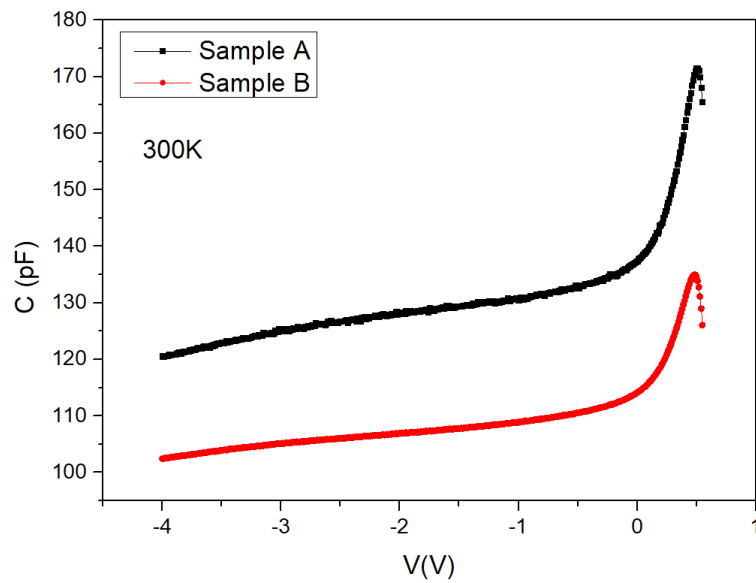


Figure 7.12: Variation of capacitance C versus reverse bias V for Sample A and Sample B at room temperature

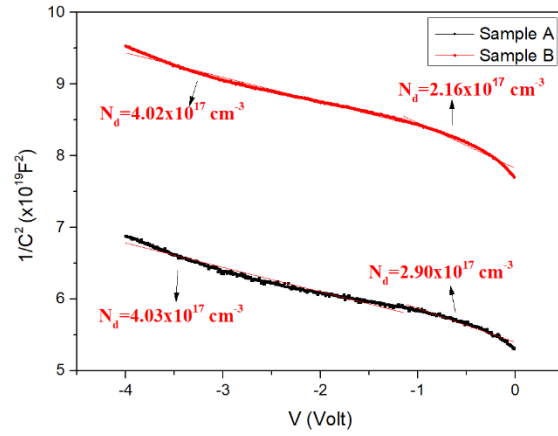


Figure 7.13: Plots of $1/C^2$ versus V for both samples at room temperature.

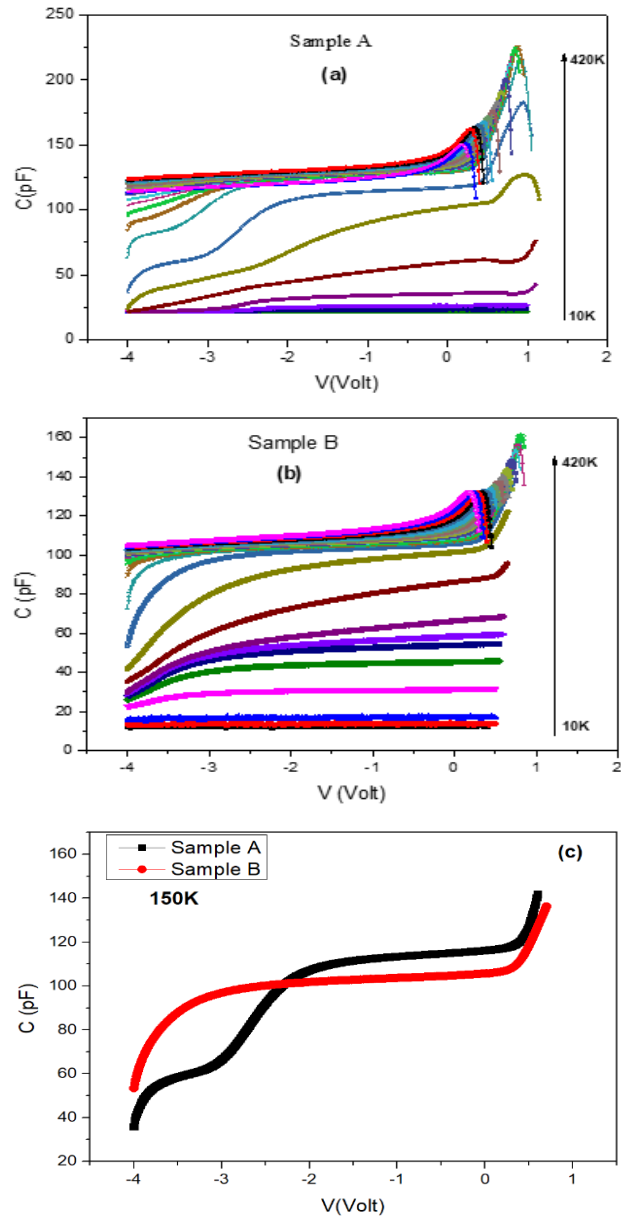


Figure 7.14 : Variation of capacitance/area with reverse bias voltage for (a) Sample A and (b) Sample B at different temperatures (c) Both samples at 150K.

Figure 7.14 (a, b) shows the capacitance versus reverse bias voltage (0V to -4V) at different temperatures. As expected, the capacitance in both samples decreases with increasing reverse bias. In addition, in the temperature range 100 - 200K the capacitance in both samples increases suddenly. This behaviour could be attributed to the release of charges captured by QDs in the activation region [24]. For example, from Figure 7.14 (c) at 150K, the most notable features observed in the C-V characteristics are plateaux or multiple steps detected in both samples. It is important to point out that Sample A has more steps/plateaux than Sample B. It is also worth noting that Kim et al. [47] observed a hump shape at a very small forward voltage of 0.4 V in InAs/GaAs QDs Schottky diodes grown by MBE. This hump was attributed to carrier accumulation in the QDs layer.

7.3.4 DLTS AND LDLTS MEASUREMENTS

DLTS and LDLTS [48, 49] were carried out in both samples in the temperature range 20 - 420 K to investigate deep-level defects. The experimental parameters used were: a filling pulse height $V_P=0V$, pulse width of $t_P=1$ msec, rate window of 200 s^{-1} and different reverse biases of $V_r = -1$ and -4 V.

Figures 7.15 and 7.16 show the DLTS spectra of the two samples A and B at $V_r = -1$ and $-4V$. From both figures, it is evident that Sample A has a large and broad DLTS signal especially at $V_r = -4V$ while sample B has more small broad peaks at the same bias. This notable difference in the DLTS spectra of both samples can be attributed to the difference in the nature of the substrates. To further understand these differences and defects, and to resolve the broad peaks Laplace DLTS was performed.

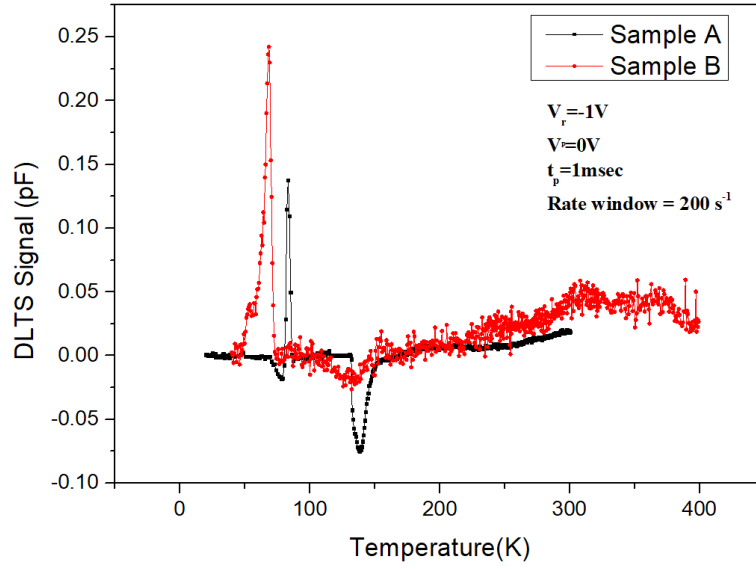


Figure 7.15: DLTS signals of Sample A and Sample B at $V_r = -1V$ with $V_p = 0V$.

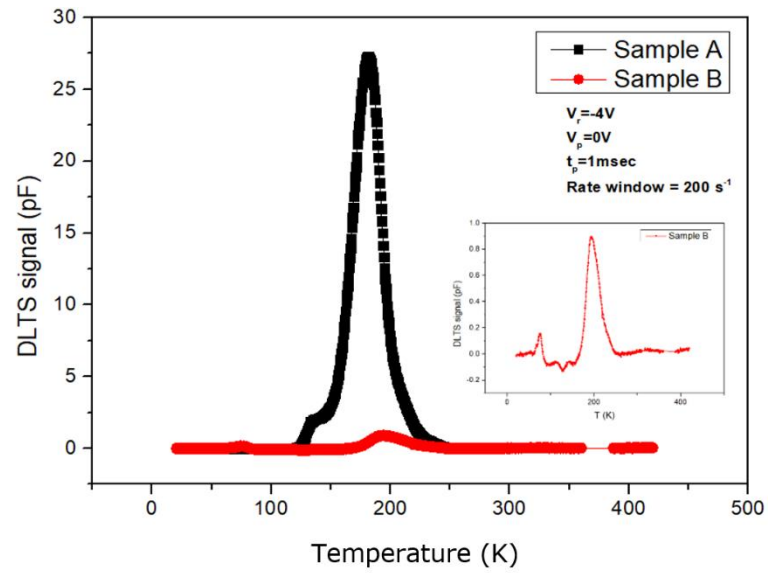


Figure 7.16: DLTS signals of Sample A and Sample B at $V_r = -4V$ with $V_p = 0$

Figures 7.17 and 7.18 (a and b) show the Arrhenius plots of $\ln(e_n/T^2)$ vs $(1000/T)$ of Sample A and Sample B for reverse biases of -1V and -4V, respectively. The activation energy (E_T), trap concentration (N_T), and captured cross-section (σ_∞) of all defects observed in both samples were determined using these plots and the DLTS/LDLTS spectra. Table 7.2 summarises these parameters.

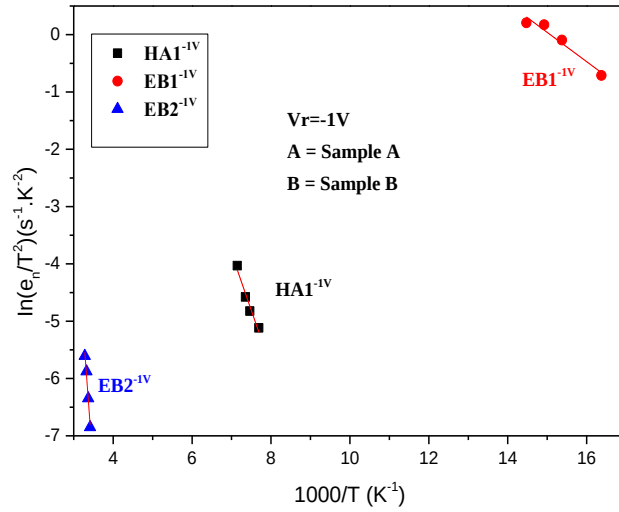


Figure 7.17: Arrhenius plots obtained from Laplace DLTS spectra with reverse biases $V_r = -1$ V, filling pulse height $V_p = 0$ V, and filling pulse time $t_p = 1$ msec. The labelling A and B, and E and H refer to Sample A and Sample B, and electron and hole traps, respectively. The solid lines represent the best fit to the data points.

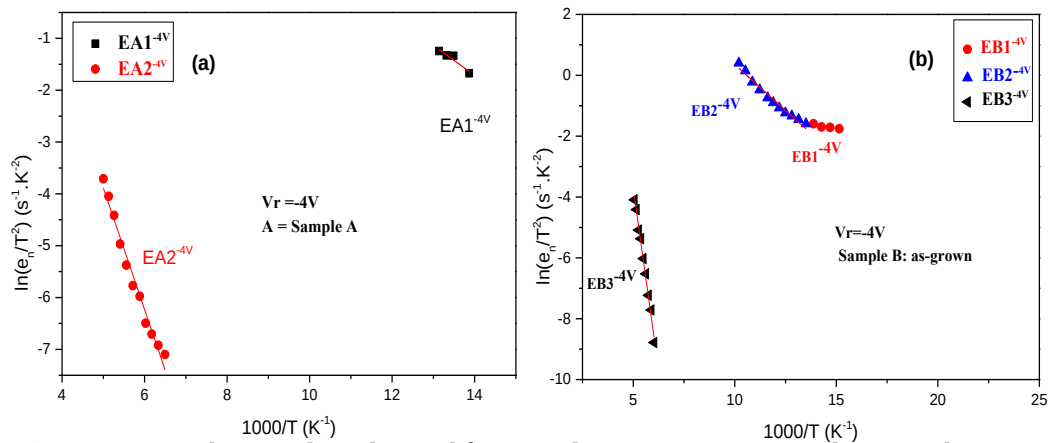


Figure 7.18: Arrhenius plots obtained from Laplace DLTS spectra with reverse biases $V_r = -4$ V, filling pulse height $V_p = 0$ V, and filling pulse time $t_p = 1$ msec. The labelling A and B, and E and H refer to Sample A and Sample B, and electron and hole traps, respectively. The solid lines represent the best fit to the data points.

Table1 7.2: Activation energy, capture cross-section, and concentration of the detected traps in Sample A and Sample B at ($V_r = -1$ V, $V_p = 0$ V) and ($V_r = -4$ V, $V_p = 0$ V) with $t_p = 1$ msec and rate window = 200 s^{-1} .

Sample	Reverse Bias (V)	Trap	Activation Energy (eV)	Trap Concentration (cm^{-3})	Capture Cross-section σ_∞ (cm^2)
Sample A	-1	HA1 ^{-1V}	0.15±0.04	3.8x10 ¹⁴	1.87x10 ⁻¹⁷
	-4	EA1 ^{-4V}	0.05 ±0.01	7.58x10 ¹⁴	3.02x10 ⁻¹⁸
		EA2 ^{-4V} (EL5)[50]	0.45±0.08	2.7x10 ¹⁶	2.87x10 ⁻¹⁷
Sample B	-1	EB1 ^{-1V}	0.040±0.007	3.27x10 ¹⁴	1.47x10 ⁻¹⁷
		EB2 ^{-1V} (EL2) [50, 52]	0. 81±0.07	1.06x 10 ¹⁴	4.71x10 ⁻¹⁸
	-4	EB1 ^{-4V}	0.0030±0.00 02	4.96x10 ¹⁵	2.12x10 ⁻¹⁷
		EB2 ^{-4V}	0.067±0.003	8.54x10 ¹⁵	1.8x10 ⁻¹⁷
		EB3 ^{-4V} (EL5) [50]	0.41±0.01	3.3x10 ¹⁵	3.9x10 ⁻²⁰

As can be seen from these tables, the number of defects at both reverse biases is larger in the samples grown on Si substrates. In addition, the number of defects near the interface of the p-i-n junction of both Sample A and Sample B is generally smaller than the number of defects away from the interface.

At $V_r = -1V$, Laplace DLTS measurements revealed that Sample A has one hole trap ($HA1^{-1V}$) with activation energy of 0.15 ± 0.04 eV. However, Sample B has two electron traps namely $EB1^{-1V}$ (0.040 ± 0.007 eV) and $EB2^{-1V}$ (0.81 ± 0.07 eV).

At $V_r = -4V$, the number of defects increased for both samples. Sample A has two electron traps, namely $EA1^{-4V}$ (0.05 ± 0.01 eV) and $EA2^{-4V}$ (0.45 ± 0.08 eV), however, the number of defect traps (electron traps) in Sample B increased to three, namely $EB1^{-4V}$ (0.0030 ± 0.0002 eV), $EB2^{-4V}$ (0.067 ± 0.003 eV) and $EB3^{-4V}$ (0.41 ± 0.01 eV).

The hole trap $HA1^{-1V}$ with an activation energy of 0.15 eV detected in Sample A, could be associated with unique defects in the QD stack structure and/or hole traps related to QD levels [51]. The deep electron trap $EB2^{-1V}$ (0.81 eV) in Sample B could be assigned to the well-known complex deep trap EL2 variants such as As_{Ga} antisite defect [52, 53].

Moreover, the electron traps $EA2^{-4V}$ (0.45 ± 0.08 eV) and $EB3^{-4V}$ (0.41 ± 0.01 eV) observed in Sample A and Sample B, respectively, have similar activation energies and therefore could be of the same origin. They could be associated with EL5 (0.408 eV - 0.58 eV) deep level which was assigned to complexes involving As interstitials- Ga vacancies (As_iV_{Ga}) [50, 54].

It is worth pointing out that the shallow traps $EA1^{-4V}$ (0.05 eV), and $EB1^{-1V}$ (0.040 eV), $EB1^{-4V}$ (0.0030 eV) and $EB2^{-4V}$ (0.067 eV) detected Sample A and Sample B, respectively, could not be identified in this work. However, these could be related to shallow impurities introduced either intentionally (dopant species used for the p and n layers of p-i-n laser structure) or unintentionally (background impurities).

In summary, Sample B (grown on Si substrate) has more defects than Sample A (grown on GaAs substrate), meaning that QDs/GaAs lasers samples can potentially have better properties than QDs/Si lasers samples.

7.4 CONCLUSIONS

In summary, the structural, morphological, optical and electrical properties of two InAs QD p-i-n laser structures with similar active regions grown on GaAs and Si substrates by MBE using strain reducing layer (SRL) have been investigated using AFM, TEM, PL, I-V, C-V, DLTS and Laplace-DLTS techniques.

Our results evidenced the formation of quite similar QDs in both structures, with higher strain for QDs in sample grown on Si substrate. It was observed that the PL intensity from QDs grown on Si substrate decreased by a factor of ~ 1.7 when compared with those grown on GaAs substrate control sample, indicating a difference in the density of defects and other nonradiative recombination centers in the QDs. In addition, a red-shift of the PL peak energy of about 20 meV, due to the residual strain at the GaAs/Si heterointerface, was also observed in the InAs QDs grown on Si substrate, accompanied by a broadening of the PL spectrum from ~ 30 meV to a value of ~ 52 meV for an excitation power of 3 mW. This broadening is attributed to the QD size inhomogeneity increase during the growth on Si substrate.

From I-V measurements, ideality factor (n), built-in potential energy (V_{bi}) and series resistance (R_s) at room temperature for both samples were determined. The ideality factor was higher in sample grown in Si substrate (Sample B) than that of sample grown on GaAs substrate (Sample A). Furthermore, the built-in potential energy and

series resistance were found to lower and higher, respectively, in Sample A than in Sample B. Sample grown on Si substrate showed more defects than the sample grown on GaAs substrate, suggesting that QDs/GaAs lasers should have better properties than QDs/Si lasers. However, the use of Si substrates to grow InAs QDs' based lasers opens up new possibilities for controlling the density and size of QDs when using specific type of SRL/substrate.

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CHAPTER 8: THE EFFECTS OF GAMMA RADIATION ON THE ELECTRICAL PROPERTIES OF InAs/InGaAs QUANTUM DOTS LASERS GROWN ON GaAs AND Si SUBSTRATES BY MOLECULAR BEAM EPITAXY

This Chapter describes the effect of gamma (γ -) irradiation on the electrical properties of InAs/InGaAs QD lasers grown on GaAs and Si substrates using Current - Voltage (I-V), Capacitance - Voltage (C-V), Deep Level Transient Spectroscopy (DLTS) and Laplace DLTS measurements.

8.1 INTRODUCTION

Within the field of QDs systems the area of InAs QDs has attracted much research activity, which is due to the possibility of achieving light emission covering the optical communication wavelength bands [\[1-3\]](#). The study of the electrical and optical properties of any semiconductor materials is important in order to understand the possibility of using them in different applications. For example, Schottky diodes are commonly used in a wide variety of semiconductor devices for different applications as well as a tool for investigating the physical and electrical properties of a semiconductor. PN junctions and Schottky diode's electrical properties are affected by a multitude of factors. These include interface chemistry, processing methodology, the existence of native defects referred to as interface states and doping concentration of the semiconductor [\[4\]](#). In addition, modifying the atomic configuration and inducing other defects into the lattice has been found to take place through exposure of semiconductor materials to radiation, which

consequently changes their electrical and optical properties [4, 5]. It is therefore important to investigate the effect of radiation on the performance of semiconductor-based devices such as Schottky diodes, solar cells, lasers, heterostructures and metal-insulator/oxide-semiconductors due to the fact that they are used in satellites. A significant number of lattice defects are produced in semiconductors as a result of radiation in space, which reduce the devices' performance [6, 7]. Moreover, the study of the defects induced by radiation led to better devices used in space which are more radiation-resistant.

To investigate the effect of electron irradiation and proton hydrogenation on the electrical properties of GaAsN device grown by Chemical Beam Epitaxy (CBE) on the main nitrogen-related nonradiative recombination center E1 which has activation energy of 0.33 eV below the bottom edge of the conduction band, B. Bouzazi *et al.* [8] employed DLTS technique. Their study proposed that the origin of this defect is related to the compensation of the tensile strain in the film produced by the small atomic size of N atom compared to that of As. Also, the density of E1 increased with increasing the fluency doses of electron irradiation.

Additionally, the effect of gamma irradiation on the electron traps present in as-grown liquid encapsulated Czochralski GaAs was described by T. Hashizume and H. Hasegawa [5]. They discovered that following irradiation, the concentration of EL6 (0.35 eV) trap was reduced by a factor of 3-5, whereas the density of EL3 (0.56 eV) increased by a factor of one order of magnitude [5, 9].

The effect of gamma (γ -) irradiation on dilute GaAsN layers with different nitrogen concentrations ranging from 0.2 to 1.2% grown on n+ GaAs substrates by Molecular Beam Epitaxy (MBE) was investigated by N. Al Saqri *et al.* [10] by

using DLTS and Laplace DLTS (LDLTS) techniques. According to their study, the number of traps either decreased, remained the same or new traps were created after irradiation depending on the nitrogen content.

This Chapter presents an experimental investigation on the effect of gamma irradiation on InAs/InGaAs QD lasers grown on GaAs and Si substrates using I-V, C-V, DLTS and Laplace DLTS measurements

8.2 SAMPLE DETAILS

In this work, the samples utilised are p-i-n laser diodes with InAs self-assembled QDs incorporated in the i-region. The samples' structures, which were presented in Chapter 7 (section 7.2.) and illustrated in Figure 7.1 (a and b), were irradiated with a gamma cell Cobalt Irradiator (dose rate of 5.143 KGy/hour) at a high dose of 50 kGy in the Institute of Physics at the University of Brasília, Brazil.

8.3 RESULTS AND DISCUSSION

8.3.1 CURRENT-VOLTAGE MEASUREMENTS

In order to investigate the effect of Gamma irradiation on the electrical properties of InAs/InGaAs QDs laser structures grown on GaAs (Sample A) and Si (Sample B) substrates, I-V measurements at different temperatures were performed. Figure 8.1(a) and Figure 8.2(a) illustrate the current-voltage (I-V) characteristics at room temperature of Sample A and Sample B, respectively, before and after irradiation. However, due to the different areas of the samples and for comparison purposes,

the current density (J) versus reverse bias is plotted for both samples as shown in Figure 8.1(b) and Figure 8.2(b).

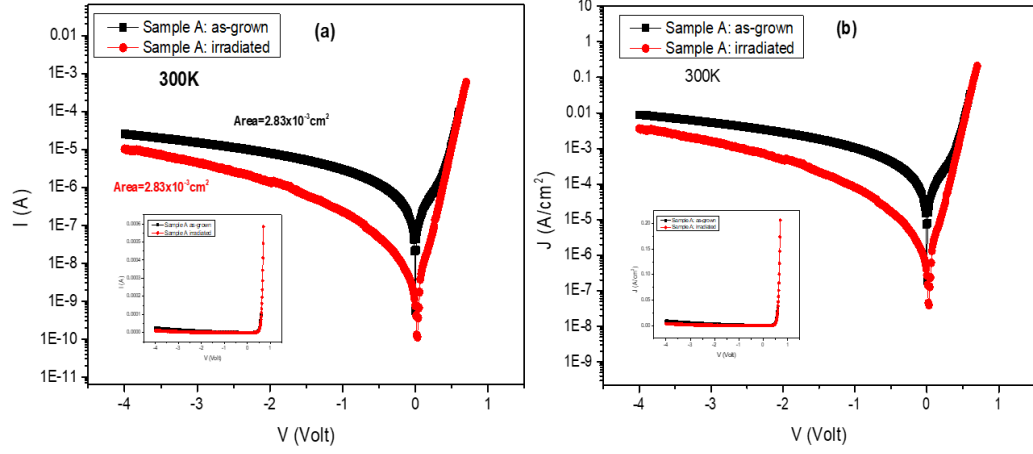


Figure 8.1: (a) Room temperature semi-log plot (I-V) characteristics of Sample A: as-grown and irradiated. (b) Semi-log plot (J-V) characteristics of Sample A: as-grown ($A = 2.83 \times 10^{-3} \text{ cm}^2$) and irradiated ($A = 2.83 \times 10^{-3} \text{ cm}^2$). The insets in (a) and (b) show a linear I-V plot and a linear J-V plot, respectively.

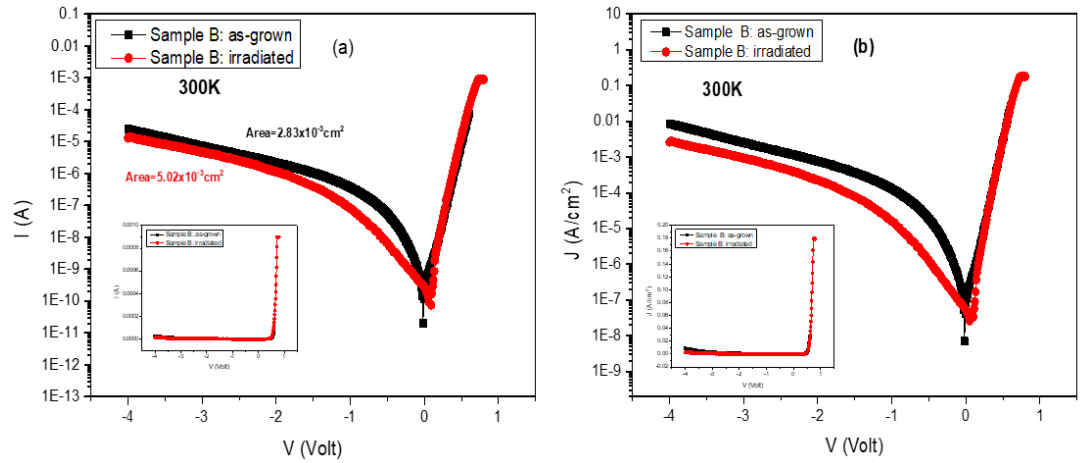


Figure 8.2: (a) Room temperature semi-log plot (I-V) characteristics for Sample B: as-grown and irradiated. The inset shows a linear I-V plot. (b) Room temperature Semi-log plots of dark J-V characteristics for Sample B: as-grown ($A = 2.83 \times 10^{-3} \text{ cm}^2$) and irradiated ($A = 5.02 \times 10^{-3} \text{ cm}^2$). The insets in (a) and (b) show a linear I-V plot and a linear J-V plot, respectively.

As shown in Figure 8.1(b), the J-V characteristics of Sample A improved after irradiation. The reverse current of the irradiated Sample A is lower than that of the as-grown Sample A. On the other hand, since the contact areas of as-grown Sample B (effective diode area $A = 2.83 \times 10^{-3} \text{ cm}^2$) and irradiated ($A = 5.02 \times 10^{-3} \text{ cm}^2$) are different, the current density (J) is plotted in Figure 8.2 instead of current (I). As clearly seen in Figure 8.2, Sample B grown on Si substrates also exhibited lower reverse currents after irradiation. However, the decrease in reverse current density after irradiation is larger for Sample A. For example, at $V_r = -1 \text{ V}$, the current density in Sample A decreased from $1.04 \times 10^{-3} \text{ A}$ to $8.04 \times 10^{-5} \text{ A}$ after irradiation, while at the same reverse voltage, the current density of Sample B decreased from $1.28 \times 10^{-4} \text{ Acm}^{-2}$ to $1.57 \times 10^{-5} \text{ Acm}^{-2}$. This decrease in reverse current after irradiation in both Sample A and Sample B may indicate that the density of the defects in as-grown samples decreased and/or the number of defects changed by annihilation or generation. In addition, the deep level defects can act as a generation recombination centers and most likely they will play a role of carrier recombination in the reverse current characteristics [11, 12].

In order to study the electrical parameters of the diodes, Werner's approach was used [13] as discussed in detail in Chapters 4 (section 4.3) and 6. These electrical parameters such as ideality factor (n), barrier height (ϕ_B), and series resistance (R_s) over the temperature 160 - 420 K were obtained. The J-V characteristics for all samples were analysed further to understand their properties by calculating the local ideality factor, $n(V)$, using the following approximated equation [14, 15].

$$n(V) = \frac{d(V/V_t)}{d[\ln(I)]} \quad (8.1)$$

where V_t is the thermal voltage.

V_t is given by $V_t = k_B T / q$ (k_B is the Boltzmann constant, q is the electric charge, and T is the temperature). The local ideality factors for all samples are calculated at room temperature and their values change with voltage as shown in Figure 8.3. As can be seen from Figure 8.3, for each device there are two noticeable behaviours observed at low voltage (~ 0.08 V) and high voltage (0.3 V) regions. In particular, at high voltages Sample A exhibit a clear peak before and after irradiation. In addition, irradiated Sample A shows a pronounced peak at low voltages. However, for Sample B these peaks are less significant at low voltages and absent at high voltages for both as-grown and irradiated devices. This behaviour of the local ideality factor could indicate that there are different conduction mechanisms occurring in the investigated devices [14, 15]. Moreover, in all samples the values of the ideality factor are greater than unity for voltages greater than ~ 0.05 V, indicating carrier recombination mechanisms such as band-to-band radiative recombination, Shockley-Read-Hall recombination (also called trap-assisted recombination) through defects, and defect-assisted tunneling or surface recombination [16, 17]. These processes could possibly explain the large ideality factors observed in these samples which incorporate QDs in the intrinsic region and which create an additional current component that contributes to the total current of the devices. It is worth pointing out that Sample B (as-grown and irradiated) has a different trend at high voltage ranges (i.e. no peak is observed) which suggests that some mechanisms are presumably suppressed or enhanced by growing on Si substrates, and some of the mechanisms are possibly unique to the devices grown on Si.

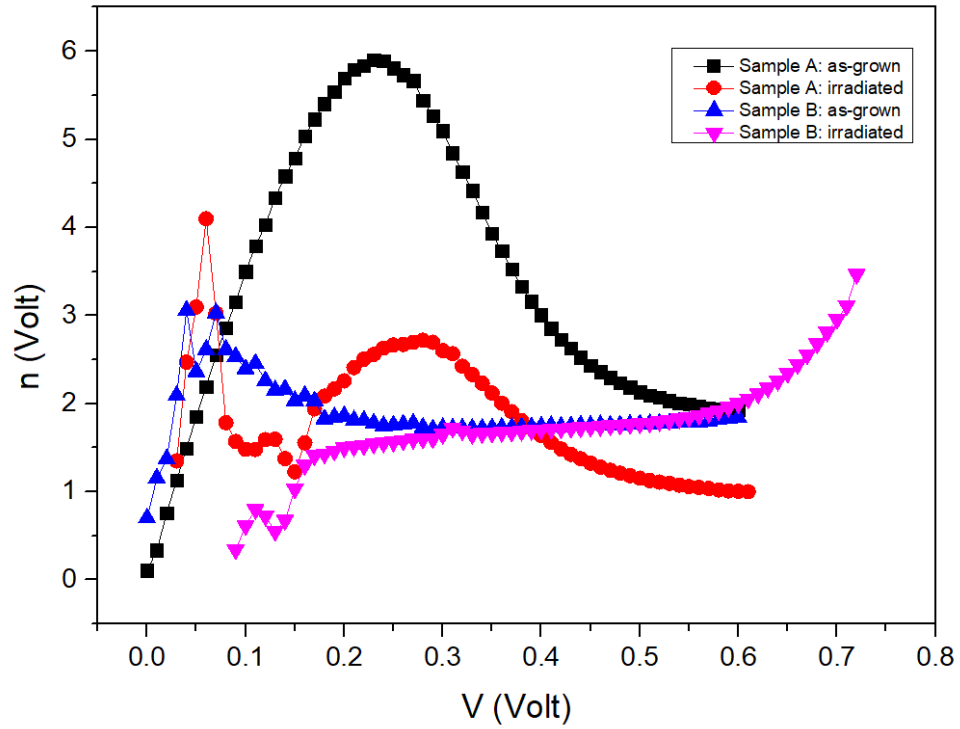


Figure 8.3: Voltage dependence of the local ideality factor for as-grown and irradiated Sample A and Sample B at 300 K.

Table 8.1 summarises the electrical parameters of the diodes at room temperature. As-grown Sample A has a lower ideality factor ($n = 1.54$), a slightly lower built-in potential energy ($V_{bi} = 0.63 \text{ eV}$) and a higher series resistance ($R_s = \sim 221 \text{ k}\Omega$) when compared to irradiated Sample A ($n = 2.39$; $V_{bi} = 0.73 \text{ eV}$; $R_s = \sim 436.27 \text{ k}\Omega$). At room temperature, all as-grown samples have ideality factor close to unity, whereas a deviation of n from unity can indicate that the conduction mechanism can be dominated by the diffusion mechanism and other factors such as series resistance, interface states, generation-recombination mechanism [18-21].

Table 8.1: Ideality factor (n), built-in potential energy (V_{bi}) and series resistance (R_s) at room temperature for Samples A and B: as-grown and irradiated. It is important to note that as-grown Sample B has a smaller area than irradiated Sample B.

Sample	n	V_{bi} (eV)	R_s (K Ω)
Sample A: as-grown	1.54	0.63	221.58
Sample A: irradiated	2.39	0.73	436.27
Sample B: as-grown	1.70	0.62	2.31×10^{-3}
Sample B: irradiated	1.73	0.67	3.5×10^{-4}

Figures 8.4, 8.5 and 8.6 show the behaviours of built-in potential (V_{bi}), series resistance (R_s) and ideality factor (n) as a function of temperature for Sample A and Sample B before and after irradiation. As shown in Figure 8.4, the built-in potential energy increases with increasing temperature before and after radiation for Sample A. This temperature dependence of the built-in potential energy is due to the effect of potential in-homogeneities at the p-i-n interface [22]. The built-in potential energy of Sample A after irradiation increased for all temperatures as compared to the as-grown sample. Similar trend was observed for irradiated Sample B for temperatures up to ~ 280 K, but for temperatures $> \sim 280$ K ϕ_B of as-grown and irradiated Sample B was similar.

Figure 8.5. shows the dependence of the series resistance as a function of temperature of Sample A and Sample B before and after irradiation. As shown in Figure 8.5, this behaviour is different for both samples. The series resistance of the as-grown Sample A, which decreased with increasing temperature, became very

small and practically independent of temperature. However, for Sample B, the low and temperature insensitive series resistance of the as-grown structure, showed a decaying behaviour with increasing temperature after irradiation.

The ideality factor of the irradiated samples A and B became more uniform and did not change very much for temperatures greater than ~ 225 K and ~ 275 K, respectively, as shown in Figure 8.6. However, the ideality factor of samples A and B were smaller after irradiation for temperatures lower than 200 K and 250 K, respectively.

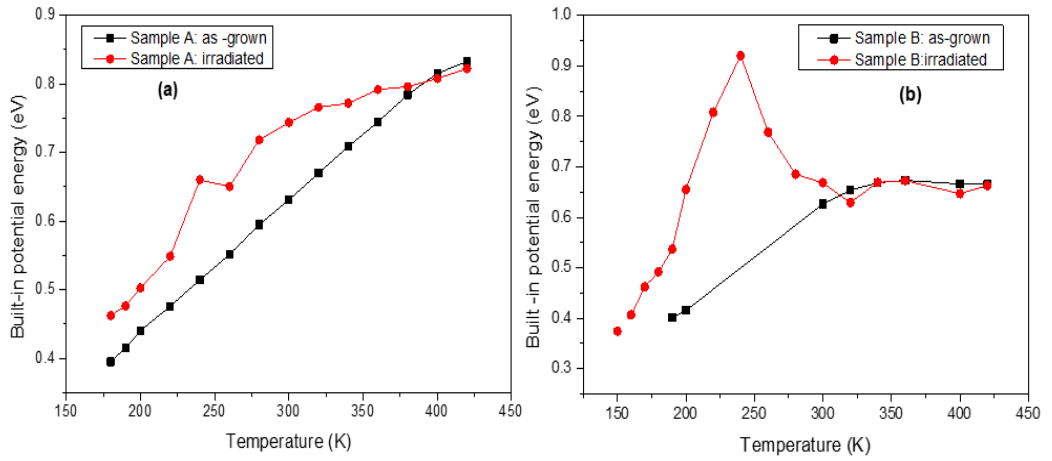


Figure 8.4: Temperature dependence of the experimental built-in potential energy of as-grown and gamma irradiated: (a) Sample A; (b) Sample B.

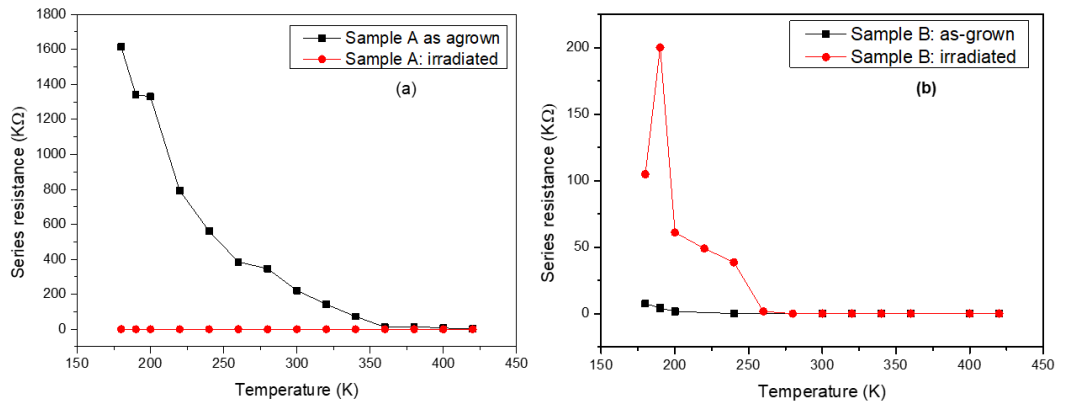


Figure 8.5: Temperature dependence of the experimental series resistance determined from I-V characteristics of as-grown and gamma irradiated: (a) Sample A; (b) Sample B. It is important to note that the as-grown sample has a smaller area than the irradiated sample.

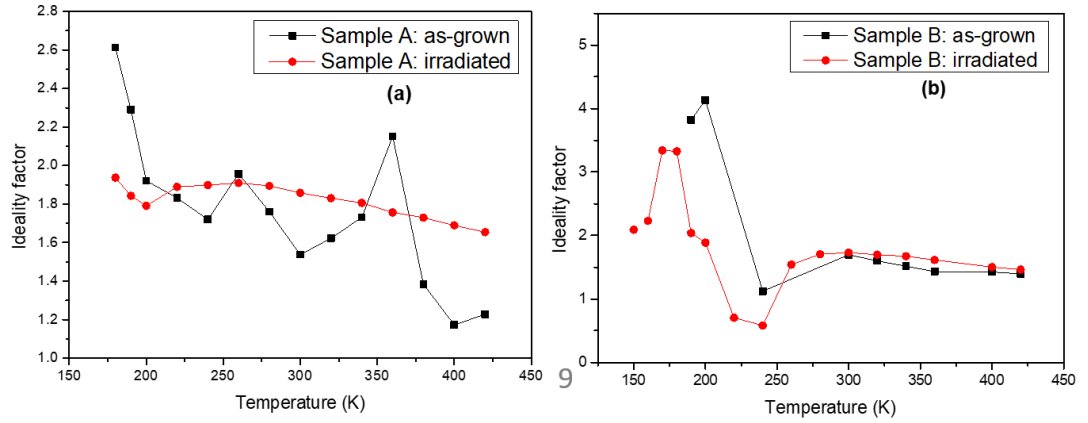


Figure 8.6: Temperature dependence of the experimental ideality factor of as-grown and gamma irradiated: (a) Sample A; (b) Sample B.

8.3.2 CAPACITANCE-VOLTAGE MEASUREMENTS

C-V measurements were recorded at room temperature utilizing a BOONTON 7200 capacitance meter to determine the free carrier concentration (N_d) of both samples. Figure 8.7(a) and 8.8(a) illustrate the capacitance-voltage (C-V) characteristics at room temperature of Sample A and Sample B, respectively, before and after irradiation. On the other hand, due to the difference in the area of the samples, the change of capacitance per area at room temperature as a function of reverse bias of all samples is plotted as shown in Figures 8.7(b) and 8.8(b) for comparison purposes. Figure 8.7 (a,b) shows that the change of capacitance is similar for Sample A before and after irradiation. The capacitance of as-grown and irradiated Sample B also follows a similar trend as shown in Figures 8.8 (a) and 8.8 (b), respectively. As clearly seen in Figures 8.7 and 8.8 the capacitance of both Sample A and Sample B decreases after irradiation. However, the decrease in capacitance/area is more pronounced in the irradiated Sample A than in irradiated Sample B.

It is important to note from Figures 8.7 and 8.8 that after irradiation, the capacitance values decreased in all samples. This decrease can be attributed to the dielectric constant change at the p-i-n interface and/or the reduction of net ionized dopant concentration due to the capture of charge carriers by defects [23-25].

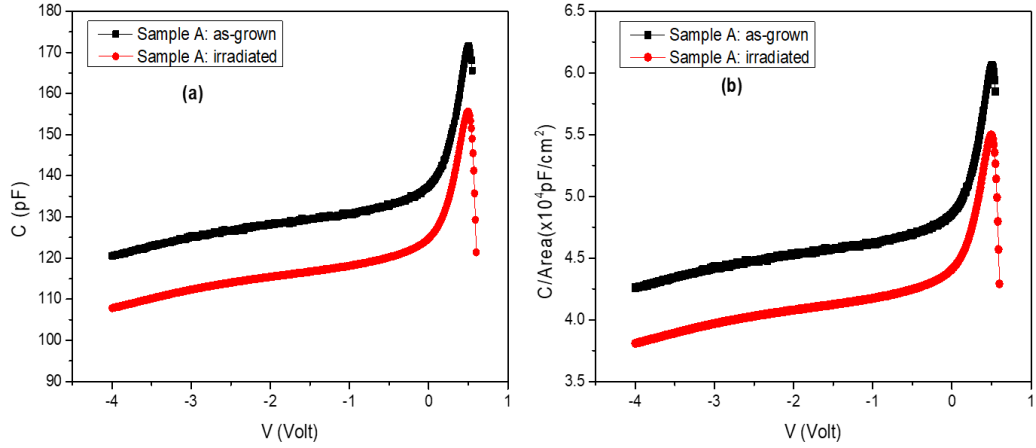


Figure 8.7: (a) Variation of capacitance C versus reverse bias V at room temperature for Sample A: as-grown and irradiated. (b) C/Area – V characteristics for Sample A: as-grown ($A = 2.83 \times 10^{-3} \text{ cm}^2$) and irradiated ($A = 2.83 \times 10^{-3} \text{ cm}^2$).

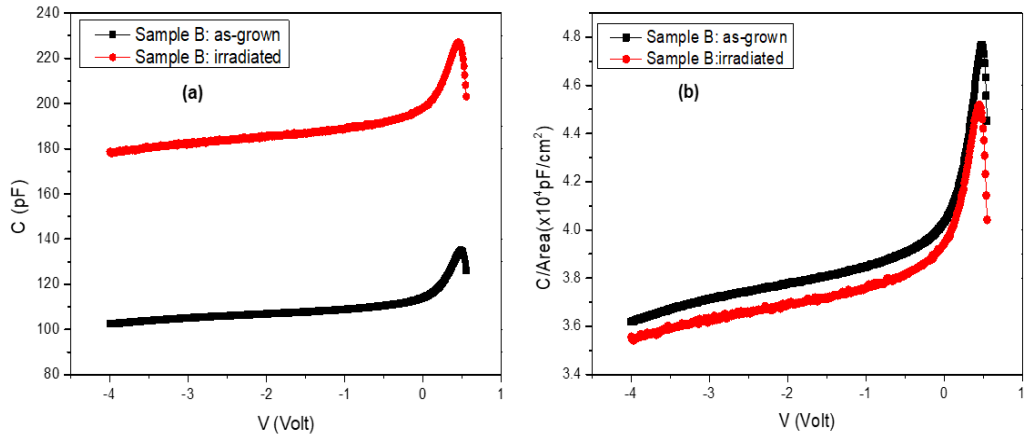


Figure 8.8: (a) Variation of capacitance C versus reverse bias V at room temperature for Sample B: as-grown and irradiated. (b) C/Area – V characteristics for Sample B: as-grown ($A = 2.83 \times 10^{-3} \text{ cm}^2$) and irradiated ($A = 5.02 \times 10^{-3} \text{ cm}^2$).

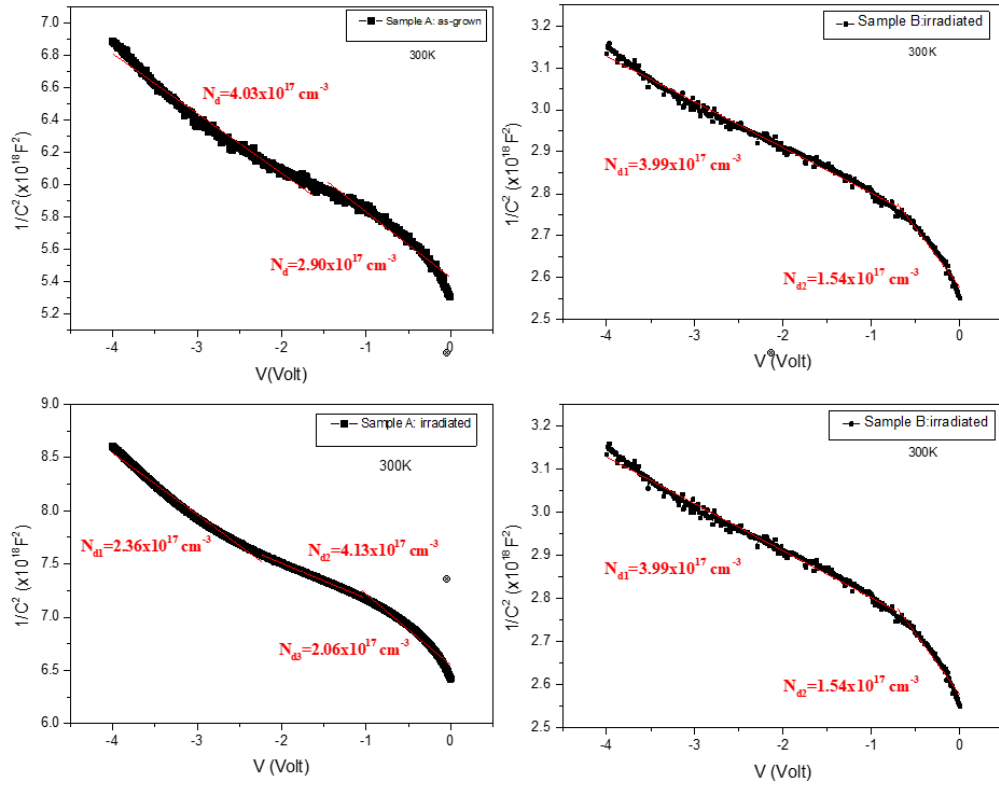


Figure 8.9: Plots of $1/C^2$ versus V for both as-grown and irradiated samples at room temperature. The solid lines represent the best fit to the data points.

Figure 8.9 illustrates plots of $1/C^2$ versus reverse bias V for all samples at room temperature. From the slope of the best fit to the plot $1/C^2$ versus reverse bias the free carrier concentration N_d was determined for all samples at room temperature. As indicated in Figure 8.9, both samples have similar free carrier concentrations, and their concentration profiles are not uniform with distance from the junction. Values of free carrier concentrations for as-grown and irradiated Sample A are $4.03 \times 10^{17} \text{ cm}^{-3}$ and $2.90 \times 10^{17} \text{ cm}^{-3}$, and $2.36 \times 10^{17} \text{ cm}^{-3}$, $4.13 \times 10^{17} \text{ cm}^{-3}$ and $2.06 \times 10^{17} \text{ cm}^{-3}$, respectively. For Sample B before and after irradiation the values of free carrier concentrations are $4.02 \times 10^{17} \text{ cm}^{-3}$ and $2.16 \times 10^{17} \text{ cm}^{-3}$, and $3.99 \times 10^{17} \text{ cm}^{-3}$ and $1.54 \times 10^{17} \text{ cm}^{-3}$, respectively. Both Sample A and Sample B show

similar trends with irradiation, where the free carrier concentration profile becomes less uniform.

8.3.3 DLTS AND LDLTS MEASUREMENTS

DLTS and LDLTS measurements [26, 27] were performed in the temperature range of 20 - 440 K in both Samples A and B before and after irradiation in order to investigate the effect of gamma irradiation on deep-level defects at a filling pulse height $V_p=0V$, pulse width of $t_p=1$ msec, rate window of 200 s^{-1} and different reverse biases of $V_r = -1$ and -4 V .

At reverse bias of $-1V$, the DLTS signals of both Sample A and Sample B decreased after irradiation and became more noisy as shown in Figure 8.10 (a, b). On the other hand, Figure 8.11 (a, b) presents the DLTS spectra, before and after irradiation for both samples with reverse bias of $-4V$. It can be seen that the DLTS signal of Sample A did not change after irradiation. Whereas the DLTS signal of Sample B decreased by approximately half after irradiation.

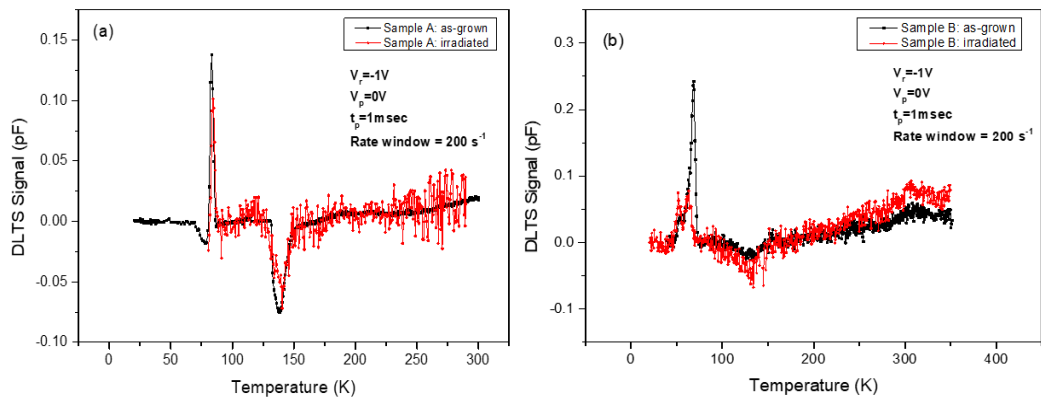


Figure 8.10: DLTS spectra of as-grown and irradiated: (a) Sample A and (b) Sample B at $V_r=-1V$

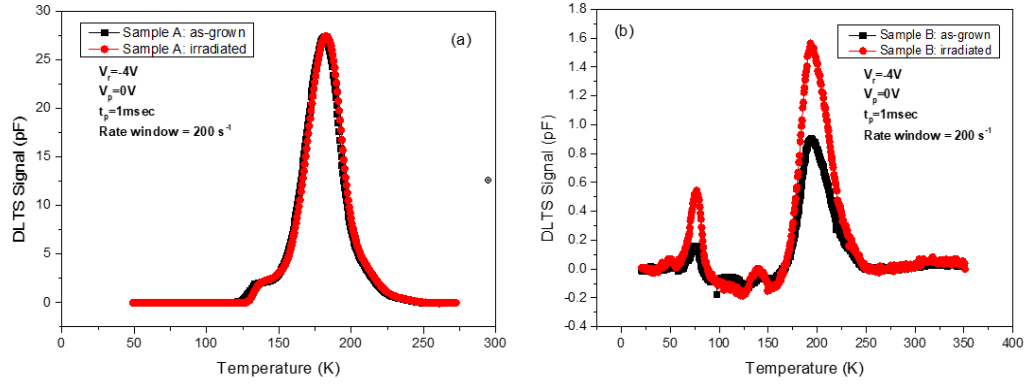


Figure 8.11: DLTS spectra of as-grown and irradiated: (a) Sample A and (b) Sample B at $V_r = -4V$

Laplace DLTS was used to resolve the broader peaks observed in conventional DLTS. Figures 8.12, 8.13, 8.14 and 8.15 (a and b) show Arrhenius plots of $\ln(e_n/T^2)$ vs $(1000/T)$ for reverse biases of -1V, and -4V for Sample A and Sample B before and after radiation.

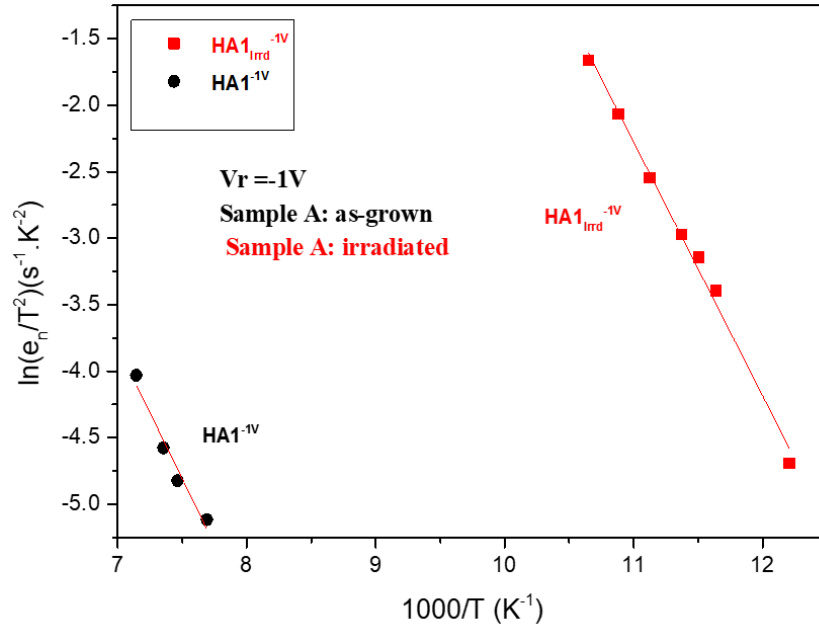


Figure 8.12: Arrhenius plots obtained from Laplace DLTS spectra with reverse biases $V_r = -1V$, filling pulse height $V_p = 0V$, and filling pulse time $t_p = 1$ msec. The labelling A and H refer to Sample A (before and after irradiation) and hole traps, respectively. The solid lines represent the best fit to the data points.

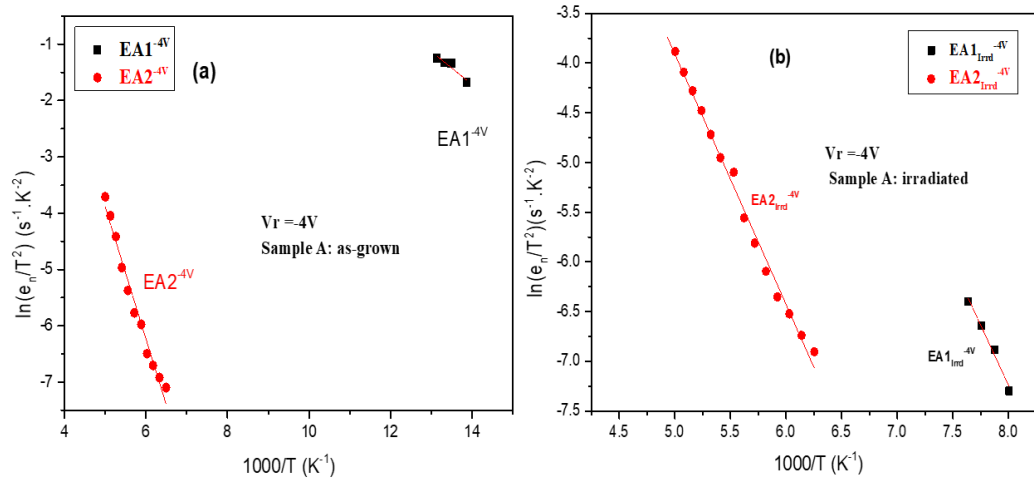


Figure 8.13: Arrhenius plots obtained from Laplace DLTS spectra with reverse biases $V_r = -4V$, filling pulse height $V_p = 0V$, and filling pulse time $t_p = 1$ msec. For Sample A (a) as-grown and (b) after irradiation. The labelling A and E refer to Sample B (before and after irradiation) and electron traps, respectively. The solid lines represent the best fit to the data points.

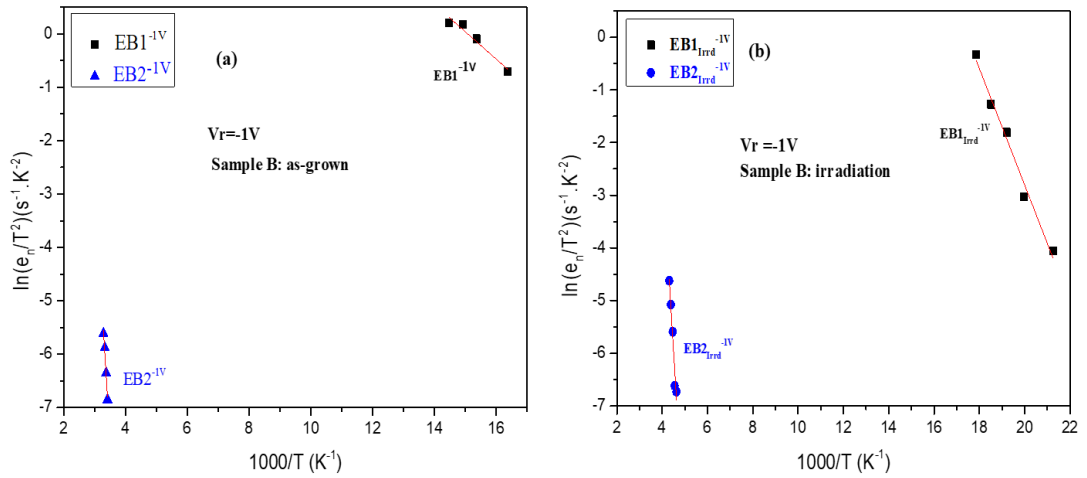


Figure 8.14: Arrhenius plots obtained from Laplace DLTS spectra with reverse biases $V_r = -1V$, filling pulse height $V_p = 0V$, and filling pulse time $t_p = 1$ msec. For Sample B (a) as-grown and (b) irradiated. The labelling B and E refer to Sample B (before and after irradiation) and electron traps, respectively. The solid lines represent the best fit to the data points

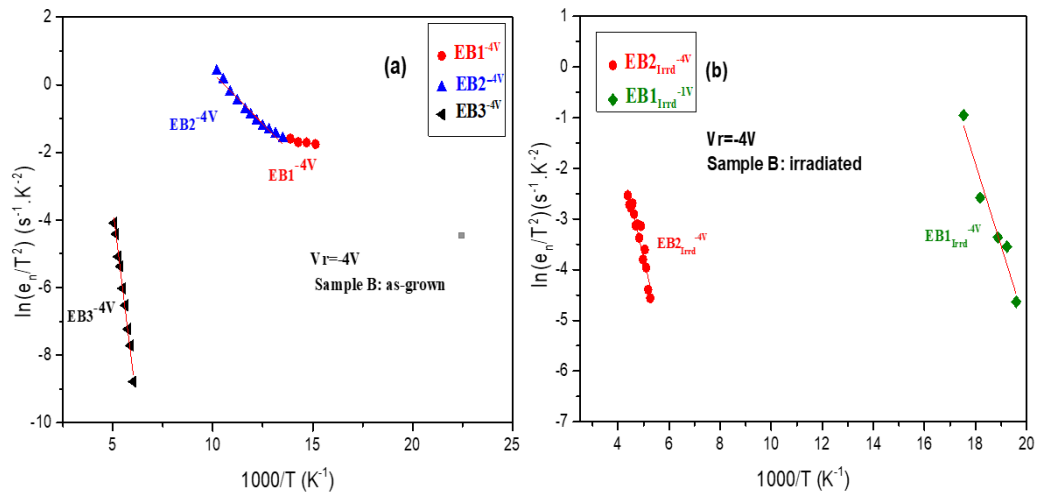


Figure 8.15: Arrhenius plots obtained from Laplace DLTS spectra with reverse biases $V_r = -4V$, filling pulse height $V_p = 0V$, and filling pulse time $t_p = 1$ msec. For Sample B (a) as grown and (b) after irradiation. The labelling B and E refer to Sample B (before and after irradiation) and electron traps, respectively. The solid lines represent the best fit to the data points.

The activation energy (E_T), trap concentration (N_T), and captured cross-section (σ_∞) of all defects detected were extracted from these plots and the DLTS/LDLTS spectra. Table 8.2 and Table 8.3 summarise these parameters.

Table 8.2: Activation energy, capture cross-section, and concentration of the detected traps in Sample A before and after irradiation at ($V_r = -1$ V, $V_p = 0$ V) and ($V_r = -4$ V, $V_p = 0$ V) with $t_p = 1$ msec and rate window = 200 s⁻¹.

Sample	Reverse Bias (V)	Trap	Activation Energy (eV)	Trap Concentration (cm ⁻³)	Capture Cross-section σ_∞ (cm ²)
Sample A As-grown	-1	HA1 ^{-1V}	0.15±0.04	3.8x10 ¹⁴	1.87x10 ⁻¹⁷
	-4	EA1 ^{-4V}	0.05 ±0.01	7.58x10 ¹⁴	3.02x 0 ⁻¹⁸
		EA2 ^{-4V} (EL5)[28]	0.45±0.08	2.7x10 ¹⁶	2.87x10 ⁻¹⁷
Sample A irradiated	-1	HA1 _{irr} ^{-1V}	0.16±0.01	3.6x10 ¹⁴	6.16x10 ⁻¹³
	-4	EA1 _{irr} ^{-4V} (EL10)[29]	0.21 ±0.02	7.60x10 ¹⁵	8.10x10 ⁻¹⁶
		EA2 _{irr} ^{-4V} (EL10)[29]	0.22±0.01	1.52x10 ¹⁷	3.23x10 ⁻¹⁷

Table 8.3: Activation energy, capture cross-section, and concentration of the detected traps in Sample B before and after irradiation at ($V_r = -1$ V, $V_p = 0$ V) and ($V_r = -4$ V, $V_p = 0$ V) with $t_p = 1$ msec and rate window = 200 s^{-1} .

Sample	Reverse Bias (V)	Trap	Activation Energy (eV)	Trap Concentration (cm^{-3})	Capture Cross-section σ_∞ (cm^2)
Sample B As-Grown	-1	EB1 ^{-1V}	0.040±0.007	3.27x10 ¹⁴	1.47x10 ⁻¹⁷
		EB2 ^{-1V} (EL2)	0.81±0.07	1.06x 10 ¹⁴	4.71x10 ⁻¹⁸
	-4	EB1 ^{-4V}	0.0030±0.0002	4.96 x10 ¹⁵	2.12x10 ⁻¹⁷
		EB2 ^{-4V}	0.067±0.003	8.54 x10 ¹⁵	1.8x10 ⁻¹⁷
		EB3 ^{-4V} (EL5)	0.41±0.01	3.3 x 10 ¹⁵	3.9x10 ⁻²⁰
Sample B irradiated	-1	EB1 _{Irrd} ^{-1V} (EL10)	0.10±0.01	4.76x10 ¹⁴	1.15x10 ⁻¹²
		EB2 _{Irrd} ^{-1V}	0.62±0.08	6.16x10 ¹³	1.22x10 ⁻¹⁸
	-4	EB1 _{Irrd} ^{-4V} (EL10) [29]	0.14±0.02	6.94x10 ¹⁴	2.73x10 ⁻²⁰
		EB2 _{Irrd} ^{-4V} (EL10) [29]	0.22±0.02	6.58 x10 ¹⁵	3.24x10 ⁻¹⁸

Tables 8.2 and 8.3 show that the number of defects at both reverse biases is larger in the samples grown on Si substrates. In addition, the number of defects near the interface of the p-i-n junction of both Sample A and Sample B is generally smaller than the number of defects away from the interface. It is also important to note that in general, the defects detected in both samples (A and B) after irradiation have different parameters than those observed in as-grown samples (A and B).

At $V_r = -1V$, as-grown Sample A has one hole trap ($HA1^{-1V}$) with activation energy of 0.15 ± 0.04 eV. This hole defect was also detected (negative peak) after irradiation with an activation energy of 0.16 ± 0.01 eV. On the other hand, both as-grown and irradiated Sample B have two electron traps each but with different parameters, namely $EB1^{-1V}$ (0.040 ± 0.007 eV) and $EB2^{-1V}$ (0.81 ± 0.07 eV), and $EB1_{Irrd}^{-1V}$ (0.10 ± 0.01 eV) and $EB2_{Irrd}^{-1V}$ (0.62 ± 0.08 eV), respectively.

At $V_r = -4V$, the number of defects increased to two for both as-grown and irradiated Sample A. As-grown and irradiated Sample A displayed two electron traps each, namely $EA1^{-4V}$ (0.05 ± 0.01 eV) and $EA2^{-4V}$ (0.45 ± 0.08 eV), and $EA1_{Irrd}^{-4V}$ (0.21 ± 0.02 eV) and $EA2_{Irrd}^{-4V}$ (0.22 ± 0.01 eV), respectively. However, as-grown Sample B has three electron traps $EB1^{-4V}$ (0.0030 ± 0.0002 eV), $EB2^{-4V}$ (0.067 ± 0.003 eV) and $EB3^{-4V}$ (0.41 ± 0.01 eV), while the number of defect traps in irradiated Sample B decreased to two, namely $EB1_{Irrd}^{-4V}$ (0.14 ± 0.02 eV) and $EB2_{Irrd}^{-4V}$ (0.22 ± 0.02 eV).

In Sample A, the hole trap $HA1$ present near the p-i-n interface (reverse bias = $1V$) was not affected by irradiation; both its activation energy and concentration before ($HA1^{-1V}$: 0.15 eV; $3.8 \times 10^{14} \text{ cm}^{-3}$) and after irradiation ($HA1_{Irrd}^{-1V}$: 0.16 eV; $3.6 \times 10^{14} \text{ cm}^{-3}$) did not change appreciably. However, the capture cross-section

increased dramatically from $1.87 \times 10^{-17} \text{ cm}^2$ to $6.16 \times 10^{-13} \text{ cm}^2$ when the sample was irradiated. As discussed in Chapter 7 this hole trap could be caused by defects in the QD stack structure and/or holes trapped by QD levels [30]. In comparison, as-grown Sample B has a shallower ($\text{EB1}^{-1\text{V}}$: $0.040 \pm 0.007 \text{ eV}$) and a deeper trap with activation energy of 0.81 eV ($\text{EB2}^{-1\text{V}}$), which could be associated with the well-known complex deep trap EL2 (0.82 eV) variants such as As_{Ga} antisite defect [10, 31, 32]. This defect was also observed in InAs/GaAs quantum dots by using DLTS technique. They assigned this trap to deep centers in bulk GaAs material [33]. However, after irradiation the 0.81 eV trap was annihilated and a new deep defect was created with activation energy of 0.62 eV ($\text{EB2}_{\text{Irrd}}^{-1\text{V}}$). This trap could be the same trap M6 ($\text{EC} = 0.62 \text{ eV}$) which is typically observed in GaAs layers grown by MBE [34]. This trap was also reported by Al Saqri *et.al* in gamma irradiated dilute GaAsN samples containing different nitrogen concentrations [10]. Moreover, the shallow trap ($\text{EB1}^{-1\text{V}} = 0.040 \text{ eV}$) in as-grown Sample B could be related to the well-known electron trap in GaAs M0 (0.10 eV) [34]. This trap originated from chemical impurities during growth [34, 35]. It is worth noting that Alhassan *et.al* observed several new traps in GaAsBi Schottky diodes grown by Molecular Beam Epitaxy when they were subjected to gamma irradiation [36]. In addition, at higher reverse bias voltage $V_r = -4\text{V}$, the traps $\text{EA2}^{-4\text{V}}$ ($0.45 \pm 0.08 \text{ eV}$) and $\text{EB3}^{-4\text{V}}$ ($0.41 \pm 0.01 \text{ eV}$) with similar activation energies and present in both as-grown samples (Sample A and Sample B) could also be of the same origin and attributed to EL5 ($\sim 0.43 \text{ eV}$) which was assigned to complexes involving As interstitials- Ga vacancies ($\text{As}_i\text{V}_{\text{Ga}}$) [37]. After irradiation this trap was annihilated in both samples, and new deep defects were created, namely $\text{EA2}_{\text{Irrd}}^{-4\text{V}}$ and $\text{EB2}_{\text{Irrd}}^{-4\text{V}}$, with similar activation energies of $\sim 0.22 \text{ eV}$. These traps could be of the same origin, and could

be related to EL10 (~ 0.18 eV) which was ascribed to an arsenic vacancy (V_{As}) complex defect involving an impurity[29] [34, 38].

It is important to note that the shallow traps EA1^{-4V} (0.05 eV), EB1^{-4V} (0.0030 eV) and EB2^{-4V} (0.067 eV) detected only in as-grown samples, could not be identified in this work, but these could be related to shallow impurities introduced either intentionally or unintentionally. It is important to mention that no shallow defects were observed in irradiated samples.

In summary, the gamma radiation has an effect on the electrically active defects present in as-grown InA/InGaAs QDs lasers grown on GaAs and Si substrates. This effect led to the number of traps either decreasing, remaining the same or new traps being created after irradiation.

8.4 CONCLUSION

I-V, C-V, DLTS and Laplace DLTS were used to investigate the effect of gamma irradiation on the electrical properties of InAs/InGaAs QD lasers grown on GaAs and Si substrates by MBE.

From I-V measurements, the ideality factor (n) was increased in both samples after radiation. However, the series resistance (R_s) at room temperature increased in Sample A after radiation, while it decreased in irradiated Sample B.

In terms of gamma radiation effect on the electrically active defects, the number of traps either decreased, remained the same or new defects were created after irradiation. Moreover, the DLTS and Laplace DLTS have been able to reveal a close connection between the grown-in defects and those induced by radiation.

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CHAPTER 9: CONCLUSION AND FUTURE WORK

The results of the research work presented in this thesis on a variety of advanced semiconductor structures and devices, namely InAs quantum dots intermediate band solar cells and InAs/InGaAs quantum dot lasers structures, are summarised in this chapter. These heterostructures were investigated using AFM, TEM, PL, I-V, C-V, DLTS and Laplace DLTS characterization techniques. The future direction of device design and characterization on these photovoltaic and optoelectronic samples is also discussed.

CHAPTER 9: CONCLUSION

9.1 CONCLUSION

9.1.1 InAs QUANTUM DOTS INTERMEDIATE BAND SOLAR CELL SAMPLES

Electrically active defects were studied in a set of p-i-n intermediate band solar cells (IBSC) grown by Metal Organic Vapour Phase Epitaxy (MOVPE). The effect of the growth temperature of the GaAs spacer layer, thickness of the GaAs capping layer, and composition of the i-region (with and without InAs quantum dots (QDs)) on the electrical properties and performance of the devices were analysed in detail.

I-V measurements showed that the samples grown at high temperature (700 °C) have the lowest leakage currents suggesting fewer defects and better ideality factors. In addition, the control samples (i.e. the one that did not incorporate InAs QDs in the i-region) grown at 700 °C showed better electrical properties than all the other samples. Furthermore, DLTS measurements detected a common deep level defect which was assigned to the well-known EL2 defect in GaAs. It was

found that this defect negatively affects both the open circuit voltage and shunt resistance, much more so in structures containing QDs in the i-region, as a consequence of the temperature cycle required to deposit them. The requirement for low growth temperatures for the deposition of QDs in QD-IBSCs or any QD solar cell is a key restriction since it promotes the nucleation of such defects.

9.1.2 InAs/InGaAs QUANTUM DOT LASERS STRUCTURES GROWN ON GaAs AND Si SUBSTRATES

AFM, TEM, PL, I-V, C-V, DLTS and Laplace DLTS measurement techniques were used to investigate the effects of the substrate material on the structural, optical and electrical properties of self-assembled InAs QDs based laser structures grown by Molecular Beam Epitaxy (MBE) using strain reducing layer (SRL) consisting of GaAs/InGaAs.

The AFM and TEM results confirmed the formation of quite similar QDs in both structures grown on GaAs and Si substrates, with higher strain for QDs in sample grown on Si substrate.

The PL measurements show that the PL intensity of QDs grown on Si substrate reduced by factor of ~ 1.7 when compared with those grown on GaAs substrate. This could be due to a difference in the density of defects and other nonradiative recombination centers in the QDs. In addition, a red-shift of the PL peak energy and broadening of the PL spectrum were observed in the InAs QDs grown on Si substrate. The red-shift could be due to the residual strain at the GaAs/Si heterointerface.

DLTS and Laplace DLTS confirmed that the samples grown on Si substrate showed more defects than the samples grown on GaAs substrate, suggesting that QDs/GaAs lasers should have better properties than QDs/Si lasers.

9.1.3 EFFECT OF GAMMA RADIATION ON InAs/InGaAs QUANTUM DOT LASERS STRUCTURES GROWN ON GaAs AND Si SUBSTRATES

In order to improve the quality and performance of devices used in space, gamma irradiation was performed in order to understand its effects on the electrical properties of InAs QD lasers grown by MBE on GaAs and Si substrates.

I-V measurements show that the ideality factor increased in both samples after radiation.

C-V characteristics confirmed that the capacitance of both samples decreases after irradiation. However, the decrease in capacitance/area is more pronounced in the irradiated sample grown on GaAs than in the irradiated sample grown on Si.

DLTS and Laplace DLTS evidenced that the number of traps either decreased, remained the same or new defects were created after irradiation.

9.2 FUTURE WORK SUGGESTIONS

Following the results discussed in this thesis, it is suggested that further investigations are carried out as follows:

- (i) In order to improve the photovoltaics properties of the intermediate band solar cell (IBSC), it would be important to perform a systematic investigation of the effects of the growth parameters (growth temperature, growth rate, growth interruption, and III-V flux ratio) and the design of the

i-region (e.g. number of QD layers, thickness of the GaAs capping layer, and other capping materials such as InGaAs).

(ii) Direct epitaxial growth of III-V semiconductor material on silicon substrates offers a viable method for producing a low-cost and large-scale manufacturing technology for photovoltaic and optoelectronic devices. It is therefore important to investigate different capping layer (CL) and strain reducing layer (SRL) materials for covering InAs QDs, and dislocation filter buffer layers to reduce the number of defects produced in the epitaxial layer due to the large lattice mismatch (4.1%) and difference in thermal expansion coefficient (200%) between GaAs and Si.

(iii) In order to understand further the role of gamma radiation on the electrically active defects, it would be interesting to carry out a systematic study using different doses.

(iv) Heat and hydrogenation treatment processes are well known to reduce the concentration of defects, annihilate and passivate completely defects. Therefore, it is proposed to investigate the effect of thermal annealing and hydrogen irradiation on the electrical, optical and structural properties of the materials and devices with the aim to improve them.