

Design of a Solar-Powered Charging Station for Electric Vehicle

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Abstract

The increasing adoption of electric vehicles (EVs) has driven the need for sustainable charging solutions. This study investigates the feasibility to increase the effectiveness of a solar-powered EV charging system with integrated energy storage and a high-efficiency power converter. The proposed solution aims to address the challenges associated with limited charging capacity, fluctuating energy generation, and costs. By optimizing the energy generation and storage components, the system enables efficient energy management and maximizes the utilization of solar power.

The study also focuses on the development of a bidirectional three-level interleaved DC-DC converter as an interface to support 800V architecture in PV-EV charging. The converter offers reduced voltage stress and current on switches, better response, smaller ripple current, and smaller magnetic size. An improved control strategy for the system is proposed to manage power flow and the stability of the system including inductor current and flying capacitor voltage. The simulation model is developed and analysed using the PLECS software.

A 6-kW laboratory prototype has been built to validate the system performance and efficiency. The thesis is structured in seven chapters, covering a comprehensive literature review, optimization of the PV-EV charging system, investigation of converter topologies, proposal of a suitable converter topology, development of guidelines for passive component sizing, loss estimation, and experimental validation. The findings of this study contribute to the advancement of sustainable and efficient solar-powered EV charging solutions.

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List of Publications

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Nomenclature

α	solar altitude angle
β	panel elevation
δ	Solar Declination
φ	Latitude
η	Efficiency
λ	Weighting factor
τ	PV panel orientation
ω	solar time
ΔI_L	Current ripple in inductor
$\Delta Q_H, \Delta Q_L$	Amount of charge
ΔV_H ,$\Delta V_L, \Delta V_{cf}$	Voltage ripple
ΣLx	Inductance
B_{size}	Battery Size
D	Day
D, D_A, D_B	Duty Cycle
C	Capacitance
C_{fA}, C_{fB}	Flying capacitor capacitance
DoD	Depth of Discharge
e	error
E_B	Battery energy
E_{load}	Energy consumed by load
E_{pv}	Energy generated by PV
ESS_{charge}	Energy needed to charge battery
$ESS_{discharge}$	Energy discharged from battery

$g, g1, g2, g3$	Cost function
f_s	Switching frequency
I_A, I_B	Inductor current
k	Coupling coefficient
K_p	Proportional gain
K_i	Integral gain
K_{cf}	Voltage balancing gain
L, L_A, L_B	Inductance
L_{kA} or L_{kB}	Leakage inductance
N	Number of
M	Mutual inductance
m	Integer of $(2 \times D)$
P_{load}	Power needed by load
P_m	Power Mismatch between load and source
PR	Performance Ratio
Rad_{pv}	solar radiation on PV panel
Rad_{solar}	solar radiation
SA1+, SA2+, SB1+, SB2+	Upper switches of B3LI DC/DC converter
SA1-, SA2-, SB1-, SB2-	Lower switches of B3LI DC/DC converter
$S1_U$, $S2_U$	Upper switches of DC/DC converter
$S1_L$, $S2_L$	Lower switches of DC/DC converter
SoC	State of Charge
T_s	Sampling time
v_A, v_B	Inductor voltage
V_B	Battery voltage
V_{cf}	Flying capacitor voltage
V_{dc}	Higher side voltage, DC bus voltage

V_{node}	Node voltage
V_{Ld}	Low side voltage, load voltage, battery voltage
X	State space variable
Y	Input variable

List of Abbreviations

AC	Alternating Current
ACR	AC resistance
ADC	Analogue to Digital Converter
AM	Air Mass
BESS	Battery Energy Storage SYstem
B3LI	Bidirectional Three Level Interleaved
CAGR	Compound Annual Growth Rate
CAPEX	Capital Expenditure
CCS	Code Composer Studio
	Combined Charging System
CE	Collector Emiter
CPU	Central Processing Unit
DAB	Dual Active Bridge
DC	Direct Current
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
ESS	Energy Storage System
EV	Electric Vehicle
EVCS	Electric Vehicle Charging Station
EVSE	electric vehicle supply equipment
FPGA	Field Programable Gate Array
GaN	Gallium Nitride
GUI	Graphic User Interface
HPI	Host Port Interface
ICE	Internal Combustion Engine
IEC	International Electrotechnical Commission

IGBT	Insulated Gate Bipolar Transistor
LCOE	Levelized Cost of Energy
LDV	Light-duty vehicle
MPC	Model Predictive Controller
MPPT	Maximum Power Point Tracking
OPEX	Operational Expenditure
PC	Personal Computer
PEMC	Power Electronics, Machines and Control
PI	Proportional-Integral
PL	Parking Lot
PV	Photovoltaic
PWM	Pulse Width Modulation
RC	Resistor Capacitor
RMS	Root Mean Square
ROI	Return on Investment
SAE	Society of Automotive Engineering
SiC	Silicone Carbide
V2G	Vehicle to Grid
V2L	Vehicle to Load
V2V	Vehicle to Vehicle
VTR	Voltage Transfer Ratio
ZVS	Zero Voltage Switching

Chapter 1
Introduction

1.1 Background

Air pollution resulting from the CO2 emissions of over a billion petrol-based vehicles on the road, coupled with the volatility of fuel prices, has driven the technology development and regulations for electric vehicles (EVs) as a viable alternative to internal combustion engine (ICE) powered vehicles. Despite the benefits of EVs, there are certain drawbacks that have limited their popularity compared to ICE vehicles. First, challenges such as the relatively low energy density of batteries that causes large mass needed for the battery pack and the longer charging time needed by batteries have impeded their widespread adoption [1]. Second, having to develop a new infrastructure for of EV charging stations that relies on an existing and already congested electric power system with two critical parts power generation (that needs to use only green energy) and transport, which are not yet able to support a full conversion to a fully electric transportation, raises sustainability and stability concerns. Therefore, in line with these challenges, it is very important to investigate long-term planning scenarios that are aiming to utilize predominantly (or fully only) renewable energy sources to power electric vehicles, thereby mitigating the potential adverse impacts of climate change on a global scale[2], [3], [4], [5].

The development of photovoltaic (PV) charging station infrastructure for electric vehicles (EVs) is a feasible option to achieve a sustainable and renewable energy solution to address the environmental concerns and reduce dependence on fossil fuels. Developing PV powered charging system facilities are able to provide advantages such as mitigating load demand from

distribution networks during daytime, contributing to stability in the distribution system by minimizing strain during high-power demand periods [6], [7]. The technical compatibility between PV and EV batteries, both operating with direct current (DC), ensures efficient power transfer with minimal losses and requires minimal maintenance due to the absence of moving parts, compared to using wind turbines.

The challenges to implement PV powered-EV charging station exist in terms of PV reliability, optimization scenarios and market interest[8]. PV system efficiency is influenced by environmental factors, such as high temperature, cloud cover, dust accumulation, pollution and rain, resulting in reduced energy collection [9]. High power extraction requires larger surface areas to meet the demanding charging requirements of EVs as well as careful consideration of installation locations and optimization scenarios [10]. Additionally, the selection of suitable PV powered EV charging methods entails trade-offs between energy availability, charging time, cost, and driver behaviour [11]. PV produces electrical power only during the day and that the power profile may be fairly predictable. However, there may be a requirement to provide charging power also during the night and for that reason, a buffer energy storage facility may need to be integrated in a PV powered charging station. The investment on energy storage enables the full utilization of collected solar energy, albeit with the consequence of a higher initial cost.

Furthermore, the adaptability of power conversion systems to accommodate various charging power and voltage options is crucial for seamless integration with the grid and standalone operation modes [12], [13] Addressing these challenges and considerations is essential to realize the full potential of PV charging systems in powering EVs sustainably and efficiently.

1.2 Problem statement

The integration of solar panels for electric vehicle (EV) charging offers a promising solution for sustainable and clean transportation. However, several challenges hinder the widespread adoption and effective implementation of solar-powered EV charging systems. These challenges include limited charging capacity, fluctuating PV power generation and high upfront costs.

To address these issues, this study investigates the feasibility and effectiveness of a solar-powered EV charging system with integrated energy storage, aiming to optimize charging capacity, stabilize energy supply, and mitigate cost concerns.

Firstly, the proposed solution involves PV energy generation, power conversion, energy storage and charging cycle at stand-alone solar-powered EV charging infrastructure to enable reliable charging within limitations of intermittent solar generation. Optimization of the energy generation and energy storage component allows for efficient energy supplied, maximizing the utilization of solar power and optimizing charging capacity. This study aims to address the daily challenges associated with power difference between supply and demand of solar-powered EV charging by investigating the feasibility of aligning PV generation power profile with anticipated charging loads, thereby promoting the adoption of sustainable and efficient charging practices. While there may be considerations regarding upfront costs and space requirements, if the advantages of increased charging capacity and stabilized energy supply outweigh these limitations, integrating energy storage becomes a valuable option for solar-powered EV charging systems.

Secondly, the proposed solution also involves the investigation and development of a high-efficiency and compact power converter specifically designed for solar EV charging systems that may accommodate a wide range of voltages and powers as specified by the charging standards (including fast charging). By analysing the power conversion characteristics, control strategies, and system integration aspects, this study aims to design and evaluate the effectiveness of the proposed power converter in maximizing power transfer efficiency of solar EV charging.

By investigating and studying both optimising the PV power and solar energy generation and the efficient power conversion to accommodate latest capabilities required by fast charging, this study aims to address the main challenges associated with suboptimal power conversion in solar EV charging and promote the utilization of renewable energy sources in transportation. Furthermore, the advantages of improved energy conversion efficiency and reduced reliance on grid electricity makes the development and

implementation of a high-efficiency power converter able to operate in a wide range of powers and battery voltages a valuable solution for efficient and sustainable solar EV charging systems.

1.3 Aims and objectives

This study aims to investigate the feasibility and benefits of designing a PV powered EV charging station where the PV panels sizing and orientation is matching the expected EV charging profiles minimising the size of a buffer energy storage system, as well as developing a novel DC/DC power converter that can operate efficiently in a wide range of powers and battery voltages as needed by a wide varieties of EVs. To achieve this aim, the main project objectives are:

- to investigate converter topologies for solar-powered EV charging by considering their benefits, drawbacks, and applications
- to optimize the PV-EV charging system while finding strategies to minimize the need of energy storage in the system needed by a PV-EV charging station
- to propose a converter topology that supports PV-EV charging with a wider power/voltage range and to find corresponding control techniques to effectively provide a proper operation for the system
- to develop a prototype of the proposed converter at reasonable power and voltage level.
- to implement the design through simulation and experimental work and present losses distribution for the proposed converter
- to conduct experimental validation at a reasonable power/voltage level.

1.4 Thesis outline

This thesis is structured into seven chapters. Chapter 2 presents a comprehensive literature review related to solar charging stations, the research and market of solar charging station offering also a justification for the need to develop a specialised power converter to be able to charge a wide range of EVs with a wider range of battery voltages and charging power levels. In Chapter 3, the focus is on the formulation and development of an optimized algorithm aimed at minimizing the buffer energy storage requirements of the PV powered EV charging station. Chapter 4 introduces the conceptualization of the proposed converter, detailing its design and functionality. Chapter 5 is dedicated to the verification of the proposed system through simulation methodologies. Subsequently, Chapter 6 presents the experimental rig developed to assess the system's performance and relevant experimental results that validate the converter's capability to charge batteries of a wide voltage range and also ability to provide future functionality such as V2x. Finally, Chapter 7 encapsules the work and the conclusions presented in this thesis, summarizes the contributions of the study, and proposes potential future research directions.

Chapter 2

Solar-Powered Charging Station Development

The number of electric cars in 2023 increases sixfold compared to 5 years prior (Appendix 1.1(a)). Appendix 1.1 (b) shows this growth is accompanied by an expansion in charging infrastructure. In the region where access to home charging is limited, the availability of public charging infrastructure becomes more critical either it is a fast charger or a slow charger. Appendix 1.1(c) depicted global ratio between Electric Vehicle and Electric vehicle Supply Equipment (EVSE)[14]. In the United Kingdom, the most commonly used public charging locations are at work or places of education, as well as in the car parks of shopping malls[15]. An adequate coverage of public charging alleviates concerns regarding range anxiety and inconvenience. The availability in charging network should also consider the quality of public charging. To assess the quality, various metrics can be employed, such as location, charging points per km, space, and power rating. For instance, the charging power capacity per electric vehicle is a factor to consider in public charger, a fast chargers can accommodate more electric vehicles than slow chargers in term of the use charging point. While fast chargers provide quick turnarounds for individual vehicles, slow chargers can often accommodate more vehicles collectively when deployed in higher numbers, especially in scenarios where simultaneous charging and cost efficiency are priorities.

Solar energy, with its significant potential for clean electricity generation through photovoltaic (PV) panels, presents a promising solution to be integrated with the available public space charging stations. The infrastructure of PV-EV stations comprises of photovoltaic (PV) panels,

DC/DC and DC/AC converters, and energy storage buffer systems. An open space is essential for the development of this type of charging station, as it provides a substantial surface area for the installation of photovoltaic infrastructure. This is particularly important in locations such as railway stations or airport parking, where a significant open ground area is available for electric vehicles to park and connect to charging ports for extended periods. By incorporating these features, the stations can provide convenience to drivers and contribute to the growth of sustainable transportation [16].

This chapter presents the requirements for an electric vehicle (EV) charging station with solar support installed to ensure effective and sustainable operation, the implementation and reviews the power conversion technology that can be used, and the future market of PV-EV charging stations.

2.1 Car Charging Infrastructure

An EV charging station is a part of an electrical grid located in residential garages, commercial buildings, streets, or public parking spaces. The actual charger can be found either onboard the vehicle which means the input is AC or offboard in which case power is fed to the EV as DC. Electric vehicles come with an onboard charger that is integrated within the vehicle with limited charging power up to 22kW. While the offboard DC charger is not installed in the vehicle and connects directly to the EV battery. This allows for a higher power flow and facilitates a reduction in both weight and volume of the car. Off board charging usually only applicable in public EV charging station and fleet and logistic hub. Requirements standard for EV charging stations in UK for conductive connection to the vehicle is provided in reference [17]. The tolerance between the output current of the DC EV charging station compared to the required value sent by the electric vehicle shall be ± 2,5 A for the requirement below 50 A, and ± 5 % of the required value for 50 A or more. The DC EV charging station shall control the output current within 1 second after the request from vehicle, with a current control the specified accuracy and with a minimum changing rate of 20 A/s or more.

Currently, home charging predominantly fulfils the charging needs of electric vehicles. As of the end of 2022, there were approximately 2.7 million public

charging stations worldwide. However, with the increasing number of electric vehicles on the roads, the availability of publicly accessible charging stations which provide convenience and accessibility similar to those of traditional gas stations, is becoming increasingly important [18].

AC charging standards are typically linked to slow charging and are defined by the inclusion of on-board battery chargers. In the United States, Japan, and South Korea, the SAE J1772 standard is employed, offering a maximum power of 1.9 kW for level 1 and 19.2 kW for level 2. Europe and Australia utilize the IEC 61851 standard, which allows for a maximum power of 13.3 kW in mode 1 and 22 kW in modes 2-3. The GB/T standard is used for AC charging in China and India, with a maximum power transfer of 12.8 kW. In November 2022, Tesla introduced its charging standard, now known as the North American Charging Standard (NACS). For AC charging, NACS delivers up to 7.7 kW for mobile connections and 20 kW for wall connections.

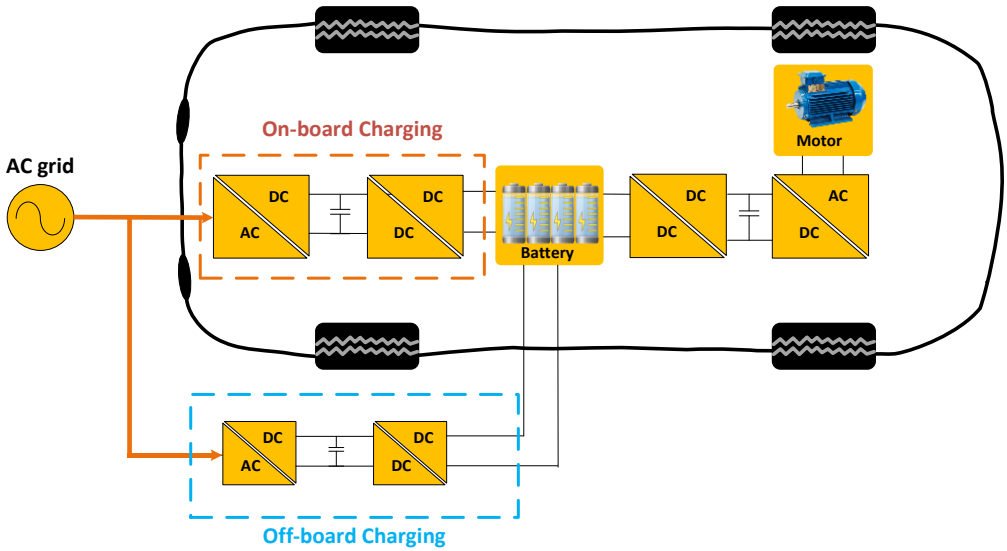


Figure 2.1 Block diagram illustrating the electric vehicle battery charging using both on board and off board chargers

Table 2.1. Charging level standard[19]

Specification	Level 1	Level 2	Level 3	Extreme Fast Charging (XFC)
Charging Power	1.44 kW – 1.9 kW	3.1 kW – 19.2 kW	20kW-350kW	>350kW
Charger Type	On board – slow charging	Onboard-Semifast charging	Offboard- fast charging	Offboard -Ultrafast charging
Charging Location	Residential	Private and commercial	Commercial	Commercial
Charging time	200km: ± 20h	200km: ± 5h	200km: ± 30 min	200km: ± 5min
Power Supply	120/230 Vac, 12-16A, single phase	208/240Vac, 12-80A Single phase/split phase	208/240 Vac & 300-800Vdc 250-500A Three phase	100Vdc and above, 400A and higher polyphase
Supply interface and protection type	Convenience outlet	Dedicated EV supply, breaker in the cable and pilot function	Dedicated EV supply, communication and monitoring between EV and charging station breaker in the cable and pilot function	Dedicated EV supply, communication and monitoring between EV and charging station breaker in the cable and pilot function
Standards	SAE J1772, IEC 62196-2, IEC 61851-22/23	SAE J1772, IEC 62196-2, IEC 61851-22/23	IEC 61851-23/24 IEC 62196-3	IEC62196 SAE J2836/2 & J2847/2

Conductive charging involves a physical connection between the vehicle and the charging inlet, and it is classified into three levels based on power capacity: Level 1, Level 2, and Level 3, as shown in Table 2.1. Levels 1 and 2 operate with alternating current (AC) through onboard chargers[19].

Level 1 charging uses a 120 V or 230 V single-phase AC supply and provides the slowest charging rate. It is typically applied in residential environments, offering up to 1.92 kW without requiring extra infrastructure [20].

Level 2 charging, widely adopted in both private and public settings, enables significantly faster charging. It supplies power up to 19.2 kW (22 kW in Europe) in single-phase or three-phase systems at 208 V or 230 V. This requires dedicated equipment and installation to handle higher power transfer

through the onboard charger. A 50 kWh battery can be recharged within 3 hours at 19.2 kW. Compared with Level 1, level 2 would need roughly 36 hours to be fully charged, it reduces charging time by a factor of 3 to 5[21].

Level 3, also known as direct current (DC) fast charging or off board charger because it supplies high-voltage DC directly to the battery. These systems typically deliver between 20 kW and 350 kW at voltages ranging from 300 Vdc to 800 Vdc, connected to a three-phase power grid. Charging a vehicle with a 90 kW or larger Level 3 charger takes only 0.2–0.5 hours. The growing interest from car manufactures to adopt fast-charging rates that would allow typically less than 30 minutes for a full charge of an electric vehicle battery. As a result, these charging stations are more complex in terms of their topology and are more expensive[22], [23], [24]. At the cutting edge, extreme fast charging (XFC) technologies aim to replicate the quick refueling experience of internal combustion engine (ICE) vehicles. delivering over 350 kW with an 800 Vdc bus, allowing battery recharge in about 5 minutes [25].

EV manufacturers transition to 800V architecture to improve the efficiency and performance of their charging systems[25]. The move is to improve efficiency, performance, and to reduce the overall footprint of the charging station because higher voltage means lower current for the same power. This results in benefits like reduced cable size, improved thermal management, and lower system costs. The 800V architecture allows for a faster charging due to higher power output. However, designing components to handle the increased voltage/power and addressing safety concerns are challenges. Despite that, the main benefits are improved efficiency, performance, and reduced energy losses.

2.2 Charging Electric Vehicle with Solar Power

2.2.1 Introduction to photovoltaic systems

The Earth receives around 4 million exajoules of solar energy, out of which a practical amount of 5×10^4 EJ is harvestable. This sustainable and clean energy source is highly desirable [26]. Solar energy is now the most cost-

effective source of electricity. Appendix 1.2 shows the potential of solar energy globally. In several countries, the cost of solar power has surpassed that of both coal and natural gas. The decreasing cost trend of solar PV panels has significantly contributed to enhancing their competitiveness. This technology has exhibited the most remarkable improvement among all renewable energy sources. The cost of the PV panel varies, depending on the technology used. The lower-cost modules are priced as low as USD 0.22/W, while high-efficiency modules are priced up to USD 0.44/W [27].

Regarding solar radiation on a PV panel, during clear skies, it primarily depends on solar incidence. The highest power is achieved when solar incidence is perpendicular to the PV panel. The efficiency of the PV panel depends on the technology used for example, 22% power conversion efficiency could be achieved using Monocrystalline Silicon PV panel [28]. The mathematical models are important for estimating the maximum power from solar panel array in a system[29], [30], [31].

Using a tracking PV panel maintains the best solar incidence angle during the day and collects maximum energy. Research has shown that a single axis tracking PV panel captures 15% more energy than a fixed panel [32]. Single axis tracking works well in many regions, However, in high latitudes, the sun remains lower in the sky, even during summer. This shallow angle reduces the effectiveness of tracking method. Moreover, using a solar mechanical tracker will increase both the investment and maintenance costs and consume energy for the steering mechanism. Another method to avoid the cost of automatic steering is by using a semi-fix PV panel with an orientation that can be adjusted periodically [33]. However, this will come with the disadvantage of the requirement of manual intervention.

For a fixed installation PV panel, The optimal tilt angle depends on factors such as latitude, seasonal performance and application whether it is a grid-tied or off-grid. Generally, the tilt angle is roughly equal to the latitude for maximum annual output. The south orientation is the best orientation for fixed PV panels installed in the Northern hemisphere by convention (north for Southern hemisphere) to collect maximum solar energy [34]. However, this orientation produces a large power surplus at midday and a symmetric rising

and falling power slope in the morning and afternoon, the surplus energy during midday would require a larger power buffer. The alternative approach is to adopt the east and west orientation. It saves 33% of space for the same installed PV panel capacity compared to the south orientation since the solar panel could be arranged with minimal spacing between rows, as the panels are tilted in opposite directions, reducing shading [35], [36]. However, it may lead to lower total energy production compared to the South only direction [4]. In cases of east or west orientation, an asymmetric load profile will result in conjunction with moving the time of the power peak earlier(east)/later(west).

2.2.2 The need to employ energy storage

PV panels could be installed on rooftops, car parks, office buildings, and industrial areas as depicted in Figure 2.2 but this green power/energy is available only during daytime. Energy storage allows for the excess solar energy generated during the day to be stored for use at night or during periods of low sunlight, thereby increasing self-consumption and reducing dependence on the grid. Battery is the most used energy storage for PV panels. But in some applications, the energy storage system could be combined to improve its performance, for example, batteries as the main energy storage tank due to its higher energy density dedicated to meeting average power demands and supercapacitors as auxiliary power storage characterized by rapid response times and a long lifecycle. Supplementary energy storage such as capacitor, in conjunction with the main storage such as batteries, can support the system during challenging transient states, high power demands, and load fluctuations [37], [38], [39].

Electric vehicle battery charging supported by solar energy generation could reduce energy costs, power grid losses, and voltage problems in the distribution network or microgrid whilst guaranteeing no CO2 emissions. An inverter is typically used to convert direct current (DC) generated by solar panels into alternating current (AC), in case the main power bus is AC. This AC power can then be used to export electricity to the national grid or provide power to electric vehicle charging stations that use on-board (AC) charging.

A PV-EV charging station can use energy storage or directly utilize the generated power for charging the vehicles, without the need for a storage system. However, a grid connection is important to ensure a consistent electricity supply for charging the vehicles, especially given the variable nature of PV generation.

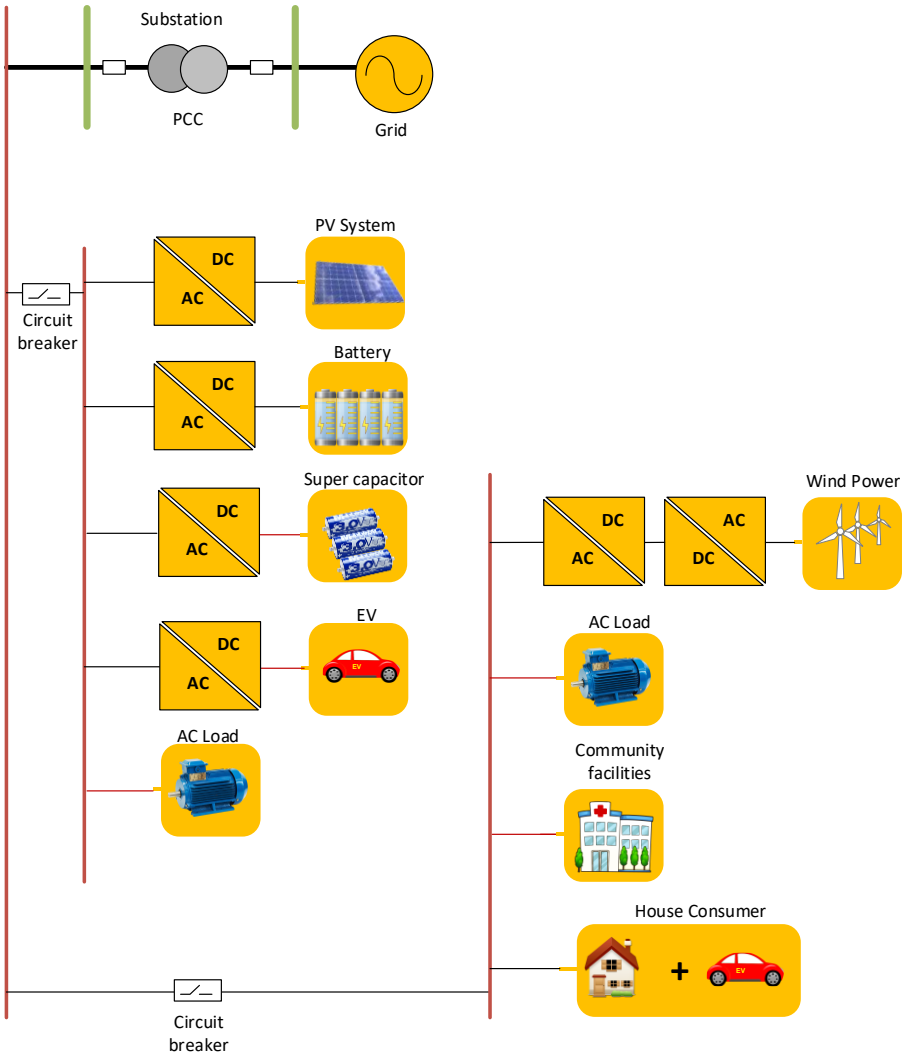


Figure 2.2 Example of a PV powered charging station integrated in a local AC distribution power system

2.2.3 Design aspects for a solar charging station

The key design aspect of the development of solar-powered charging stations considers certain parameters such as location and orientation of the solar panels to optimize sunlight exposure throughout the day. Secondly,

determining the appropriate solar panel capacity should be based on the expected energy demand of the EV charging station and its daily load profile.

Compared to other energy sources, solar power has a drawback related to the need for a large surface area which are available in commercial parking areas and parking lots (PLs) such as airports, hospitals, and universities. Implementing solar charging to fulfil EV power and energy demand would be beneficial because PLs host multiple cars and have available a wide area to install PV panels[16], [40].

Another issue to consider is the solar power generation pattern. Ideally, the EV charging demand pattern should align as closely as possible with the available solar power generation curve to decrease the need for Energy Storage Systems (ESS). However, the charging demand pattern depends on charging time set by the arrival and departure of the EV/driver, the limitations imposed by the EV battery, and other factors [41], [42]. Therefore, designing a PV charging infrastructure based on daily demand pattern is strongly recommended not only to enhance efficiency but also potentially to reduce the energy storage requirements [43].

The energy storage system is another important component in PV-EV charging stations. BESS provides the necessary power buffering in the system to capture excess PV power available at midday and ensure that EV charging demand is met when solar power is unavailable. The presence of large energy storage in the charging station provides flexibility in the load profile. However, this will lead to an increase in PV-EV investment cost. BESS incurs energy losses during charging and discharging (typically 80–95% round-trip efficiency). Batteries typically have shorter lifespans than PV systems, requiring replacements that increase costs over the lifetime [44]. However, aside from their higher cost, batteries also offer added benefits that PV systems alone cannot provide, such as grid stabilization, peak shaving, and energy arbitrage.

2.3 Review of converter topologies for PV-EV charging station

The AC system shown in Figure 2.2 where all subsystems connect via the AC grid needing each an AC/DC or a DC/AC conversion stage, has lower conversion efficiency compared to a DC system where only DC/DC conversion stages, fewer in numbers, are needed. Therefore, developing a direct current (DC) system presents some advantages, particularly in terms of efficiency and controllability issues compared to an AC system which needs frequency, voltage regulation, and unbalanced compensation.

A grid-tied DC with integrated PV and battery storage charging station, as illustrated in Figure 2.3, was proposed [45], [46], [47], [48], [49]. The station still utilizes various types of power converters, including DC/AC inverters and DC/DC converter. These power converters are managed to distribute energy efficiently among components in the system. The grid-tied inverter facilitates bidirectional power flow, allowing energy to be fed back into the grid or drawn from the grid as needed. This optimizes energy usage and potentially receives green credits for surplus renewable energy fed back into the grid. A trade-off emerges in terms of the greater complexity and costs may appears when attempting to retrofit an existing AC system to DC. Under certain conditions such as remote area, a stand-alone PV system could be a better option.

DC/DC conversion (off-board charging) is recommended for PV-EV charging [12], [22], [23]. This charging type supports fast charging and is more efficient for PV-EV charging because both operate on DC and already at kilowatt levels. The DC/DC converter is utilized in the PV-EV system to convert DC voltage/current/power from one level to another, allowing power transfer to match the optimum voltage rate between solar panels, batteries, and DC loads.

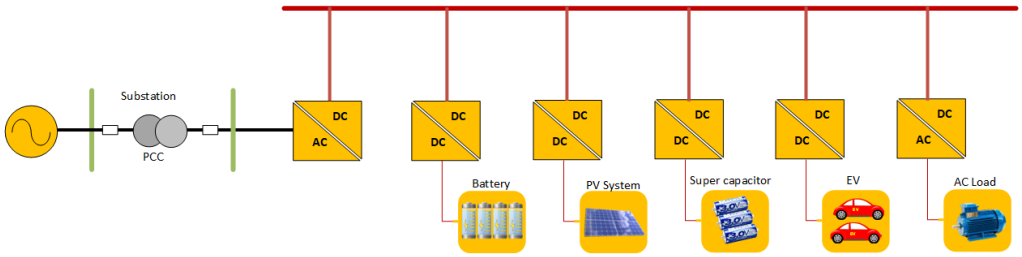


Figure 2.3. Example of a DC charging station with a common DC bus.

There are three design dimensions when developing a DC/DC converters: dynamic performance, maximum power density, and minimal cost. To achieve optimal performance, a lower switching frequency is utilized to minimize switching losses, while a sizeable passive component is employed to reduce voltage and current ripples. However, this approach results in a low power density and bandwidth for the control. To achieve maximum power density, a high switching frequency is needed, utilizing compact magnetic elements. However, this presents thermal and efficiency constraints which may be addressed by using high performance and more expensive components. Lastly, to minimize costs, low-cost components and a simple topology are employed, albeit at the expense of efficiency [50], [51], [52]. It is clearly seen that developing a design to address these three design directions is difficult as their requirements are contradictory.

2.3.1 Classification of DC/DC Converters for Battery Charging

DC/DC converters can be classified into unidirectional and bidirectional as well as isolated or non-isolated[53]. Depending on the application in transportation systems, design objectives may include some features such as high gain, multi-port and bidirectional power flow.

An isolated DC/DC converter provides electrical isolation between input and output which is very useful for safety or place where isolation between different parts of the system is necessary. A non-isolated converter has no transformer and does not require galvanic separation between the input and output. This reduces the complexity and size/weight of non-isolated converters. Moreover, the absence of a transformer contributes to enhanced

efficiency, as there are no losses associated with the transformer operation that need to be considered [54] nor to conversion of DC to AC and viceversa.

Table 2.2 Comparisons between isolated and non-isolated converter topologies[55], [56]

Attributes	Isolated	Non-Isolated
Transformer requirement	Yes	No
Efficiency	Depend on topology and specification, the transformer add core and copper losses	Depend on topology and specification
Number of switches	Depend on topology	Depend on topology
Isolation	Galvanic isolation	No Isolation
Grounding	Separate	Common
Application	High-Medium voltage	Low voltage
Voltage range	High	Moderate
Volume &Weight	High	Low
Power density	Moderate	High
Cost	High	Low
Complexity	Depend on topology	Depend on topology, in general simpler due to the absence of transformer

Many applications use two-level bidirectional DC/DC converters, particularly those used for battery charging. The level of converters typically refers to the number of voltage levels present in the output waveform.

An essential feature of battery charging is bidirectional power flow. Bidirectional DC/DC converters enable power transfer between the connected storage systems with both the energy source and the load. A bidirectional converter could minimize or eliminate variations in the output of renewable energy systems caused by fluctuations in environmental conditions. Figure 2.4 shows the classification of bidirectional DC/DC converter according to [53].

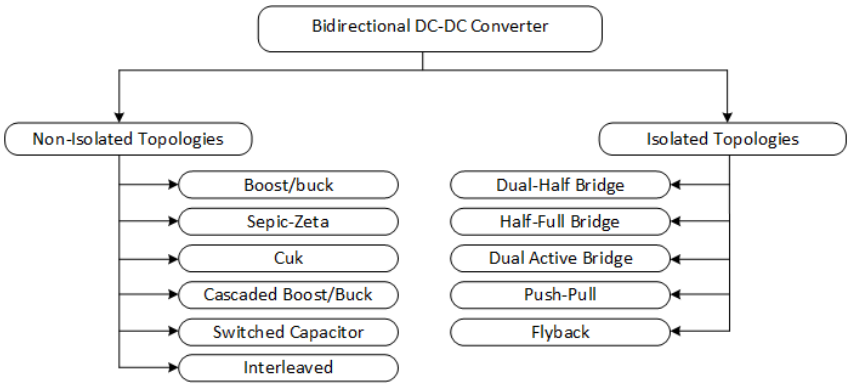


Figure 2.4 Classification of bidirectional DC–DC converters [53]

There are numerous DC–DC converter topologies available, and selecting the most appropriate one for a given application requires a careful evaluation of the trade-offs between their performance characteristics. The following subsections present an overview of selected isolated and non-isolated DC–DC converter configurations.

Isolated DC/DC Converter

A. Dual Active bridge DC/DC Converter

A Dual Active Bridge (DAB) is a popular topology in power electronics applications. This type of DC/DC converters provides bidirectional power flow and galvanic isolation. It is commonly utilized in various applications, such as battery systems, renewable energy, and low to medium voltage grid applications. The DAB's design is flexible, allowing it to accommodate a wide range of specific voltage and power requirements. Moreover, it provides opportunities for soft switching, which enhances its efficiency.

Figure 2.5.(a) shows the Dual Active Bridge topology. It is composed of two full H-bridge inverters with active switches both on the primary and secondary sides. The bridges are separated by a high frequency transformer and inductor. Bidirectional power flow is achieved by controlling the phase shift angle between the voltage waveforms of the two bridges. When the phase shift angle is positive between the input and output bridge voltage, power flows from left to right. Changing the polarity of the phase shift angle enables reverse power flow.

B. Resonance Converter

The other popular isolated DC/DC converter topology is the Full-Bridge LLC resonance converter. Figure 2.5.(b) depicts a Full-Bridge LLC resonance converter equipped with a Full-Bridge diode rectifier. The switching bridge produces a square waveform to stimulate the LLC resonant tank, which subsequently yields a resonant sinusoidal current that is scaled by transformer and then rectified by using rectifier circuit. The output capacitor filters the rectified alternating current, resulting in a direct current output.

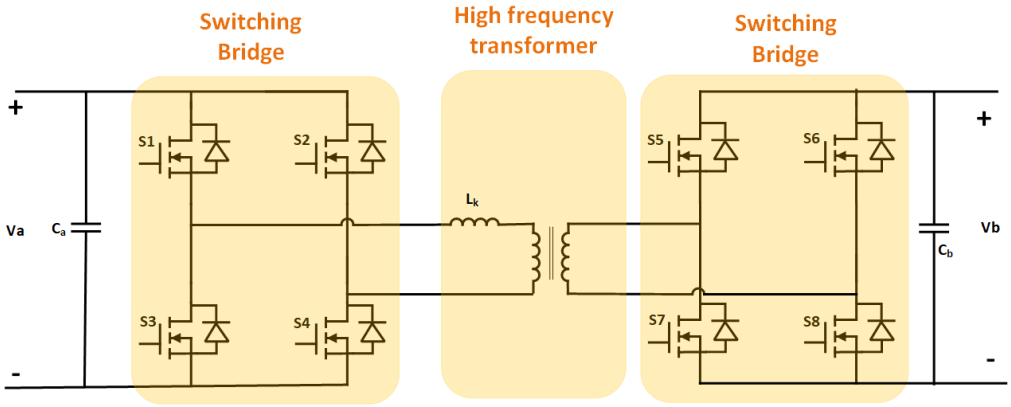
A resonant LLC converter has a number of desirable characteristics, including high efficiency, low electromagnetic interference (EMI), and high-power density.

C. Bidirectional Push-pull converter

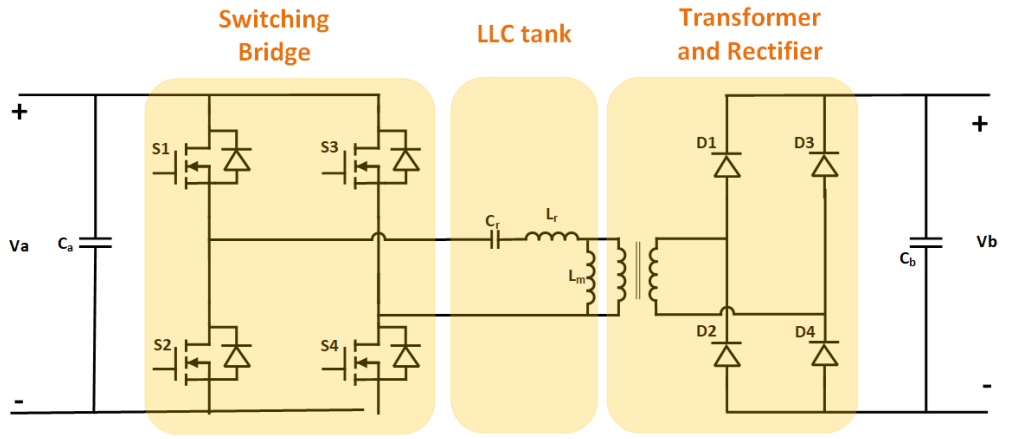
The bidirectional push–pull converter (Figure 26.c) was developed from the unidirectional design to enable bidirectional power flow. Like its unidirectional counterpart, t is derived from the unidirectional push–pull converter but replaces passive rectification devices with active switches on both the primary and secondary sides of the transformer, allowing reversal of power flow

D. Bidirectional Flyback converter

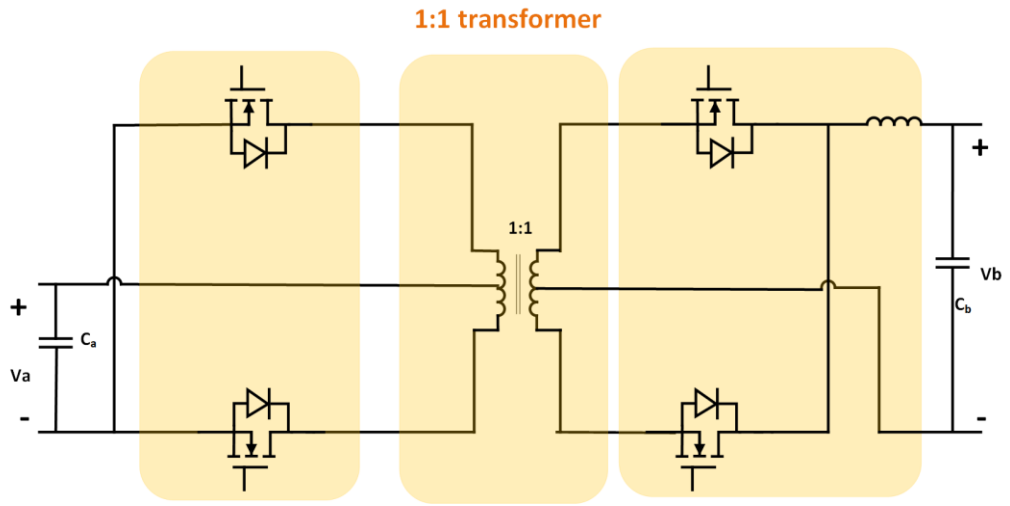
The bidirectional flyback converter (Figure 2.6 d) is an isolated DC–DC topology that enables energy transfer in both directions by replacing the diodes in a conventional flyback converter with actively controlled switches on both the primary and secondary sides of the transformer. it stores energy in the transformer's magnetizing inductance during switch conduction and releases it when the switch turns off, allowing power to flow from source to load or vice versa. This topology has low component count, cost-effectiveness, and inherent galvanic isolation. However, it is less suitable for high-power applications because of higher peak currents, transformer losses, and efficiency limitations


Switching Bridge
High frequency transformer
Switching Bridge
+
Va
C_a
-
S1
S2
S3
S4
L_k
S5
S6
S7
S8
+
Vb
C_b
-

(a)


Switching Bridge
LLC tank
Transformer and Rectifier
+
Va
C_a
-
S1
S3
S2
S4
C_r
L_r
L_m
D1
D3
D2
D4
+
Vb
C_b
-

(b)


1:1 transformer
1:1
+
Va
C_a
-
+
Vb
C_b
-

(c)

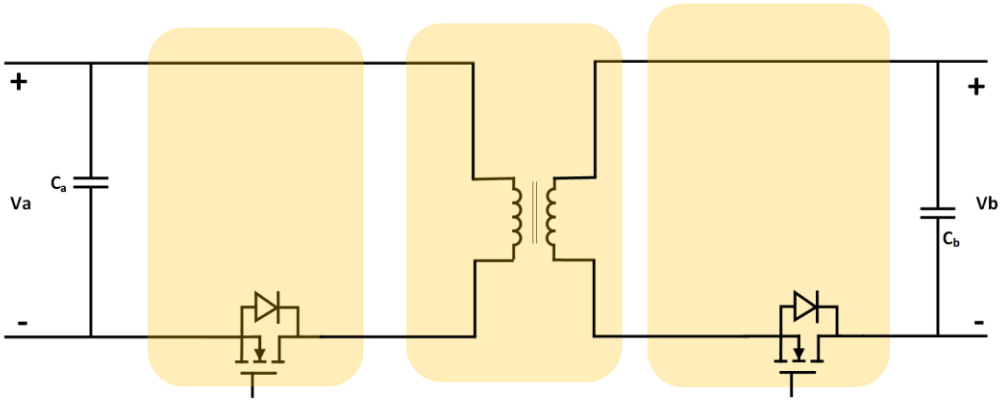


Figure 2.5 Example of isolated DC/DC Converter (a) Dual-Active Bridge, (b) Resonance converter, (c) Bidirectional Push-pull converter, (d) Bidirectional Flyback converter

Non Isolated DC/DC Converter

Non-isolated DC–DC converters are employed in electric vehicle (EV) charging systems due to their structural simplicity, reduced cost, and lower weight. Compared with isolated converter counterparts, they offer higher power and energy density, making them an attractive choice for compact and high-efficiency charging architectures.

The canonical switching cell is recognized as the fundamental building block for various DC–DC converter topologies, including buck, boost, buck–boost, and Ćuk converters. The system comprises a controllable switch, a diode, and energy storage components, specifically an inductor and a capacitor. The functionality of these converters relies on the regulated charging and discharging processes of the inductor and capacitor within the switching cell, facilitating voltage conversion and energy transfer between the input and output stages. Utilizing this principle, multiple cells can be paralleled or configured to enhance conversion efficiency [57].

A. *Interleaved Bidirectional DC/DC Converter*

In an interleaved converter, the load current is distributed among its parallel phases, thus requiring smaller inductances and allowing the converter to carry higher total current. Interleaved converters also improve the current in the DC input bus and output load side by benefiting from the harmonic cancelling out effect of the phase shifted current ripples. Therefore, it requires a smaller size capacitor on both input and output[58], [59].

The interleaved converter shown in Figure 2.6. (a) is built from a single-phase buck-boost bidirectional converter [60], [61], [62], [63]. This circuit is regarded as the fundamental circuit of bidirectional DC/DC converters. The device operates as a boost converter when the flow of power is from the low side voltage to the high side voltage, and as a buck converter in the opposite direction. This converter is the simplest bidirectional converter to be developed in terms of hardware and control.

The Interleaved Bidirectional DC/DC converter topology connects multiple such converter legs in parallel with a phase shift of 360°/N. Interleaved converters provide several advantages, such as reduced output current ripples, improved system efficiency, higher power density, and better thermal capacity. By dividing the current in parallel routes, conduction losses are minimized and lower power switches are needed. The interleaving strategy also reduces ripples in the input voltage and current. However, these benefits come with certain trade-offs. Implementing interleaving increases system complexity and cost due to the larger number of active and passive components, including additional switches, inductors, and control circuitry. Moreover, while the combined output ripple is minimized, each phase experiences a relatively higher ripple current for the same output current of single leg converter. Another critical drawback is the presence of circulating currents between interleaved phases, particularly in converters with mismatched components. These circulating currents not only complicate current sharing but also increase conduction losses, reducing overall efficiency. Hence, designing an interleaved converter requires careful optimization to balance reduced output ripple against circulating current effects and component costs.

B. Cascaded DC/DC Converter

A cascaded DC/DC converter connects multiple DC/DC converter stages in a succession. The primary purpose of this configuration is to enhance the precision of output voltage control and increase the efficiency of energy conversion. This type of configuration is particularly useful in applications where a single-stage DC/DC converter might not provide the desired output voltage levels or efficiency.

Cascaded converters can provide a higher gain of voltage transfer. For example, if a system requires a large voltage step up or down, cascading multiple stages can achieve this more effectively than a single-stage converter. Considering that a non-isolated DC/DC converter always switches the current on the low-voltage side and the voltage on the high-voltage side, by dividing the voltage conversion process into smaller steps, each converter can operate closer to its optimal efficiency point (or better said, further away from the most disadvantageous operating point), reducing overall power losses.

This converter design can be modular, allowing for easy adjustments and scaling of the system. Different converter stages can be designed to handle different parts of the voltage conversion process. Additionally, by sharing the voltage conversion across multiple stages, the electrical stress on each component is reduced, potentially increasing the lifespan and reliability of the components.

One example of this converter is the Cascaded Boost DC/DC Converter shown in Figure 2.6.(b). The working principle of this converter involves several stages. The input DC voltage is fed into the first DC/DC converter stage, which adjusts the voltage to an intermediate level. The output of the first stage is then fed into the input of the next stage. Each subsequent stage further adjusts the voltage as required until the final stage produces the desired output voltage which can be used to power the load or further processes.

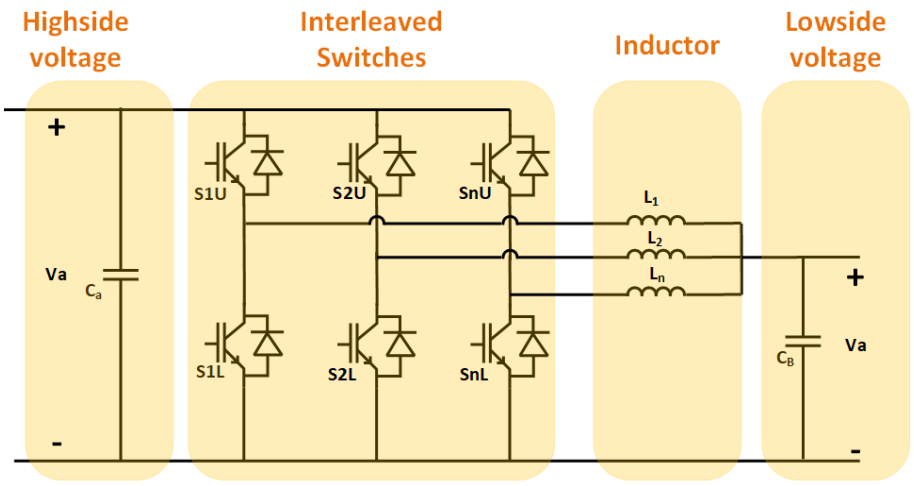
C. Multilevel DC/DC converter

Two-level converters are often used due to their simplicity compared to multi-level converters. They have fewer power electronic switches and components, making them easier to control and implement. Two-level converters have been widely adopted and standardized in various applications, making them a common choice for many power electronics systems. This widespread use has led to the availability of standardized components and control strategies. Two-level converter technology has been extensively researched, tested, and applied in a variety of power electronic systems over the years. The reliability

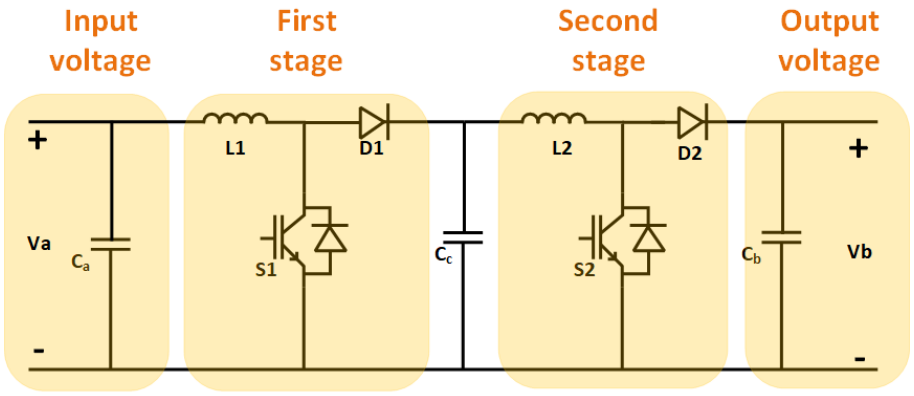
and performance of two-level converters are well-established, contributing to their continued use.

While two-level converters are common and suitable for many applications, they still have some limitations, especially in high-voltage and high-power applications or where power density needs to be maximised. In the worst condition, the voltage/current transitions can be abrupt, causing stress on the system and potential damage to connected devices.

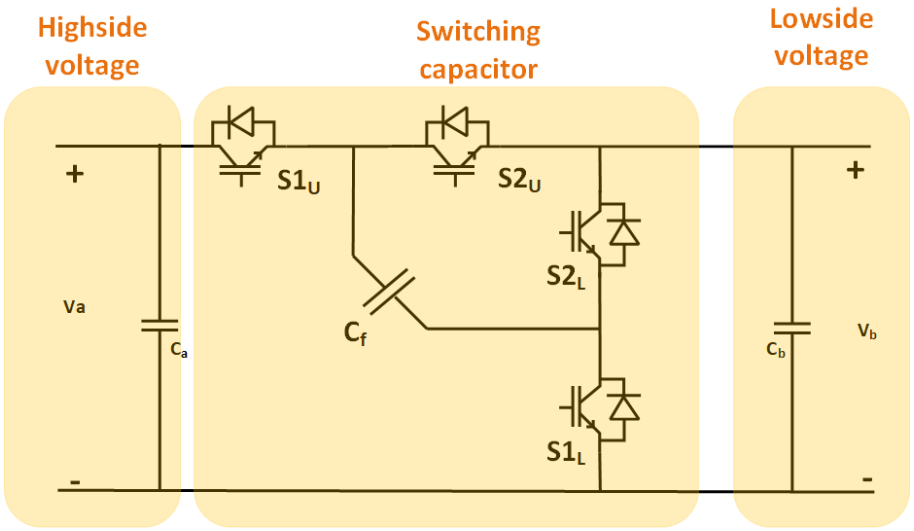
The use a multilevel converter such as switching capacitor converter shown in Figure 2.6.(c) reduces the amplitude of the voltage switched across the switches and inductors therefore reducing switching losses and inductor size. Therefore, multilevel converter can be applied to switches that limit the rate of voltage change (dV/dt). Multilevel converters offer flexibility by enabling operation across a wider range of input voltage and load conditions, making it more flexible and versatile. This converter also has lower heat dissipation and longer lifespan due to lower stress on components. A smaller and lighter designs can also be achieved by operating the converter at higher switching frequencies.



(a)



(b)



(c)

Figure 2.6. Example of Non-isolated DC/DC converter topology. (a) Interleaved bidirectional three-phase converter. (b) Cascaded DC/DC converter- Cascaded boost. (c) Multilevel Converter-Switching capacitor converter.

Recent advancements in high-power electronics have enabled the emergence of ultra- and extremely-fast EV chargers, capable of delivering over 350 kW per vehicle. Although present-day EVs do not yet utilize such power levels, these chargers are future-proofed for next-generation 800 V battery systems while remaining compatible with legacy 400 V platforms. The key enabler of this adaptability is modularity, which allows manufacturers to scale voltage and current through reconfigurable power modules, optimizing both performance and efficiency [64]. The commercial power-electronic charging topologies in still depend on the grid as the primary energy source. In such configurations, the AC input is first processed by a rectification stage to convert the alternating supply into a regulated DC link [64]. This DC bus

subsequently feeds a DC–DC conversion stage, which performs voltage and current regulation according to the battery charging requirements.

Table 2.3 Commercial DC/DC Converter topologies[64]

Topology	Topology	Power (kW)	Input Voltage	Output voltage	DC Bus	Output current	Eff	Ref
ABB Terra 53/54	isolated DC/DC stage based on a proprietary halfbridge LLC converter	50	480 VAC	150-500VDC	N/A	125 A	>94%	[65]
ABB Terra HV high-power charger	The three-channel LLC includes are configurable secondary rectifier.	150	480 VAC	400- and 920VDC	N/A	63A	>94%	[65]
Tritium PKM150	N/A	150/75/50	380-400 VAC	150-950VDC	950 VDC	Up to 350 A	>97%	[66]
Tesla V2 Supercharger	The two-stage power conversion circuit, one passive single-phase bridge per channel with a boost PFC, followed by a phase-shifted full bridge	135	380V-480V	50-450V	400 VDC	Up to 335 A	93%	[67]
Porsche Modular Fast Charging Park A	Phase-Shifting Transforme, Three-Phase Passive Rectifier, Boost PFC, Buck DC/DC		450 VAC	800-V		400-950 VDC	N/A	[68]

ABB's Terra series exemplifies this concept with modular architectures, achieving up to 95 % efficiency through isolated LLC converter stages and scalable 150 kW–600 kW configurations. Tesla's Supercharger network also applies modularity, combining 13 identical on board charger units per cabinet

to reach 150 kW per vehicle (92 % efficiency), with later versions extending to 250 kW. Similarly, Porsche's 800 V charging system employs modular PEBBs with galvanic isolation via grid transformers, PFC-based rectifiers, and multi-channel buck converters that minimize current ripple and permit operation from medium-voltage grids. The system achieves up to 98 % efficiency and supports bidirectional grid services.

A combination or variant/extended of the presented converter topologies may result in a better performance of the system. However, it is important to consider the drawbacks of each topology as well. When used in certain industrial applications.

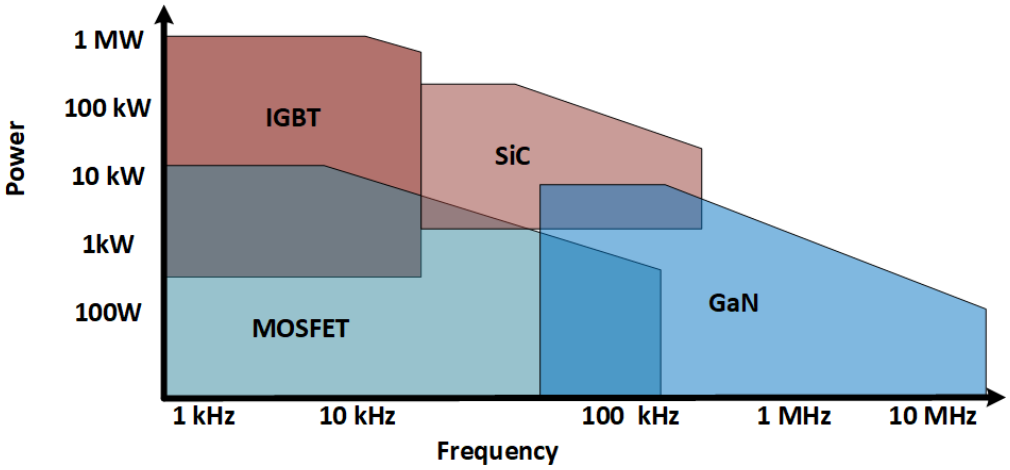
For example, improving the performance of DAB with series resonance incurs increased cost and control [69], [70]. Employing multiple phases and levels in a non-isolated DC/DC converter requires additional power semiconductor devices and circuitry, which can significantly increase the complexity and cost of the system. The increased complexity may introduce potential reliability issues. With more components and circuitry involved, there is a higher chance of failures or malfunctions occurring, leading to system downtime or the need for costly repairs. The increased complexity of multi-level and channel converters may require more sophisticated control algorithms and monitoring systems. However, in some specific applications, the manufacturing cost could potentially be lowered by mass producing a common subsystem that is paralleled to achieve a custom system specification and efficiency may be improved by utilizing a greater number of phases and higher-level converters. The choice between number of phase level converters depends on the specific requirements of the application, such as voltage levels, power ratings, and system complexity.

For EV application, a three-level converter would give benefits due to the upgrading of EV charging infrastructure to 800V. Most electric vehicles use battery configurations with string voltages ranging between 150-450 Vdc, and this high voltage configuration is commonly referred to as the 400V architecture. Upgrading the 400V architecture to 800V architecture results in significantly faster EV charging speeds. The 800V charging architecture reduces weight and/or range while reducing charging times. Cost reduction is

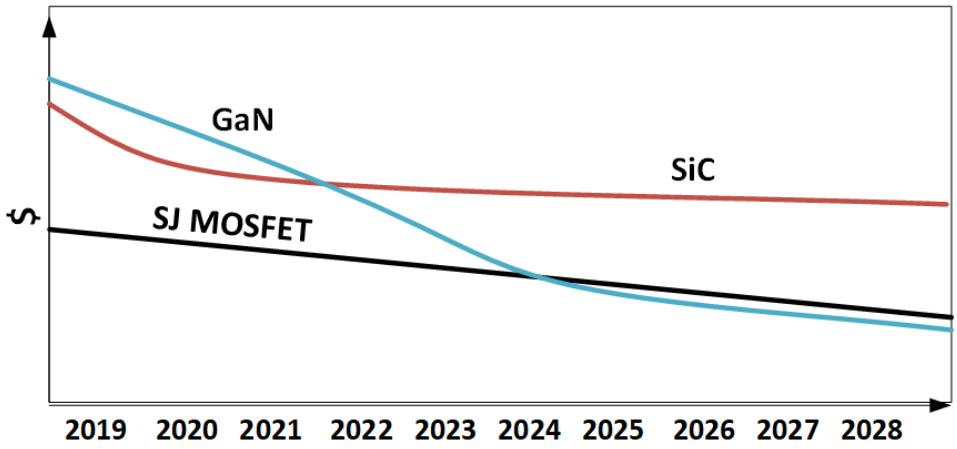
expected in a EV designed for higher voltage because of the less the physical material [71], [72]. This means that when designing a next generation converter for a general EV charging station to suit a wide variety of EVs, that are particularly powered by renewable energy, it must be able to accommodate a wide variety of currents/voltages/powers whilst maintaining a high conversion efficiency.

2.3.2 Switching devices choice

Figure 2.7(a) shows the power device technology mapping available in the near future [73]. Gallium Nitride (GaN) has the capability to handle faster switching frequency with very small commutation time (leading to lower dead time losses) and requires small gate drive voltage. Although currently very expensive, manufacturing cost of GaN is predicted to reduce in the future as shown in Figure 2.7. (b). However, this semiconductor is predicted to be suitable at maximum voltage of only 600-650 V which would make it unsuited for 2-level 800V chargers. Therefore, developing a three-level converter will facilitate higher voltage 800V EV charger implementations whilst being able to benefit from the excellent performance of the GaN device.



(a)



(b)

Figure 2.7 FET switching device technology (a) Power device mapping (b) Relative cost projection

The three-level DC/DC Converter extends power device benefits, particularly when using Gallium Nitride (GaN) and Silicone Carbide (SiC) devices. GaN has the capability to handle faster switching frequency with very small risetime (lower switching losses) and increase efficiency and density, but currently may not have sufficiently large-rated blocking voltages to implement 2-level high voltage chargers. This is why it is proposed that the three-level converter with GaN devices will offer a superior alternative to enable higher-voltage at DC link whilst using 600V rated GaN devices [74]

In case of deciding to use silicon IGBTs, this device has the advantage of being capable of handling higher current. A three-level DC/DC converter alternates switching sequence in the converter leg to double the switching frequency as seen from the inductor either using coupled or discrete inductor. Therefore, despite the slow silicon IGBT switching frequency, applying multi-level converter would be beneficial to downsize the magnetics size whilst processing significant powers at 800V/high currents.

Table 2.4 Decision matrix for 800 V architecture

Function / Constraint	Voltage seen by device	Switching profile	Best fit	The alternatives
3 level	400 V (per device)	40–100 kHz	GaN 650 V	Si: switching loss and diode recovery loss dominate at the desired frequency SiC: over-specification and higher cost/kW at the same rate
3-level at low switching frequency	400 V (per device)	≤ 10 kHz	IGBT <800 V	SiC and GaN: little gain for slow switching and higher cost Si: voltage margin/robustness
2-level design at 800 V	800–900 V	≥20 kHz	SiC 1.2 kV	GaN voltage is insufficient IGBT is not efficient at high frequency

2.4 Future market

EV users mostly use public charging points in car parks in their place of work, travel or where they shop. The demand for charger access in car parks is high, both for slow or rapid charging[15]. The integration of solar power with EV charging infrastructure has emerged as a convenient approach to reducing the carbon footprint associated with transportation. Solar-powered charging stations not only provide clean energy for EVs but also contribute to grid stability and resilience. These stations can generate electricity during daylight hours, complementing grid power during peak demand periods and reducing pressure on traditional power systems.

The global Solar Power Market size is projected to reach USD 377.04 billion by 2029, with a projected CAGR of 7.0% during the forecasting period. The global solar power market industry is gaining momentum owing to technological advancement, also termed as green technologies. The energy generation from solar panels is attracting investments from developing economies driven by the demand from the manufacturing industry. Building 1 MW PV base solar farm could potentially save £500 million annually.

Advances in solar technology have made solar-powered charging stations increasingly feasible and cost-effective. The integration of advanced photovoltaic materials and energy storage systems has enhanced the efficiency and reliability of solar charging infrastructure. Additionally, innovations in smart grid technologies enable optimized management of solar resources, allowing for better synchronization between energy generation and EV charging demand.

The market for solar-powered charging stations for EVs is predicted to increase in the coming years. Market analyses conducted by organizations such as BloombergNEF [44] forecast a continuous increase in the implementation of solar charging infrastructure, driven by government incentives, environmental regulations, and growing consumer demand for in sustainable transportation. Moreover, partnerships between automotive manufacturers, energy companies, and infrastructure developers, as observed in initiatives like the Electric Highway Consortium, indicate a collaborative effort to expand the solar charging network.

Despite the promising outlook, several challenges must be addressed to realize the full potential of solar-powered charging stations. Issues such as intermittency of solar energy generation, land use requirements, and initial investment costs pose significant hurdles to widespread adoption. However, advancements in energy storage technologies and the integration of vehicle-to-grid (V2G) capabilities could mitigate these challenges, enabling greater flexibility and resilience in solar charging infrastructure.

The future market for solar-powered charging stations for electric vehicles holds substantial promise as a sustainable solution for transportation electrification. Continued advancements in solar technology, coupled with supportive policies and strategic collaborations, will drive the expansion of solar charging infrastructure. Addressing challenges through innovation and investment will be crucial to realizing the full potential of this emerging market and accelerating the transition towards a clean and renewable energy future.

2.5 Summary

The development of solar-powered charging stations can offer convenience to drivers and contribute to the growth of sustainable transportation. The use of parking lots to develop these stations can be advantageous as they allow for the installation of photovoltaic infrastructure that requires an open area, and electric vehicles can park and connect to charging ports for a certain period, utilizing the facilities.

The infrastructure of PV-EV stations comprises photovoltaic (PV) panels, converters, and energy storage systems. An optimization is required when designing solar-powered system focusing on EV charging service that allows to better match the PV power generation profile with the EV charging power requirement therefore, reducing the need for buffer energy storage which is too expensive. Chapter 3 of this thesis will propose and validate a design procedure to address this challenge,

On the other hand, PV-EV charging stations should align with the demand of EVs. Therefore, general converters, such as DC/DC converters, are recommended for fast charging. Whether isolated or non-isolated, bidirectional DC/DC converters provide flexibility for EV charging to support V2G or V2V. Two-level bidirectional DC/DC converters are commonly used for battery charging and PV interfaces to implement MPPT functionality. Interleaved three-level bidirectional DC_DC converters extend the voltage and current capability of converters and offer greater flexibility and scalability in EV charging infrastructure. They can accommodate a wide range of input voltages and power levels, making them suitable for various charging scenarios, including parking lot charging stations because their design allows for easy expansion and integration with renewable energy sources particularly solar energy. Chapter 4 of this thesis will analyse the operation of a 3-level interleaved converter whilst chapter 5 will show implementation of control and validation by simulation whilst chapter 6 will present the design and experimental evaluation of an 800V-16Amps DC/DC converter prototype.

Chapter 3

Development of an Optimized PV Panel Orientation Algorithm to Minimize Energy Storage Cycling in Solar Charging Stations

This chapter presents a strategy and algorithm for optimizing solar-powered charging station. Instead of relying solely on a sizable battery, this study suggests minimizing its size by adjusting the orientation of groups of the photovoltaic (PV) panels including estimate the amount of solar radiation at a particular location for the design and economic evaluation of a PV system. This adjustment aims to provide an optimized solar power profile that aligns with a specific load demand pattern, thereby decreasing the need for extensive energy storage. While deviating the PV panels from the south orientation may result in a reduction in overall energy capture, compensatory measures involve increasing the number of panels. Although this increases the cost of PV panels, they are generally more economical than batteries [44], [75], [76], [77]. Consequently, the overall expectation is that this approach will be more cost-effective. Additionally, the study has implications for future energy transactions between vehicles and charging stations, particularly when cars in parking lots serve as temporary energy storage buffers. The study suggests that this approach can lead to a more economical solution for PV-EV charging stations and has implications for future energy transactions between vehicles and charging stations.

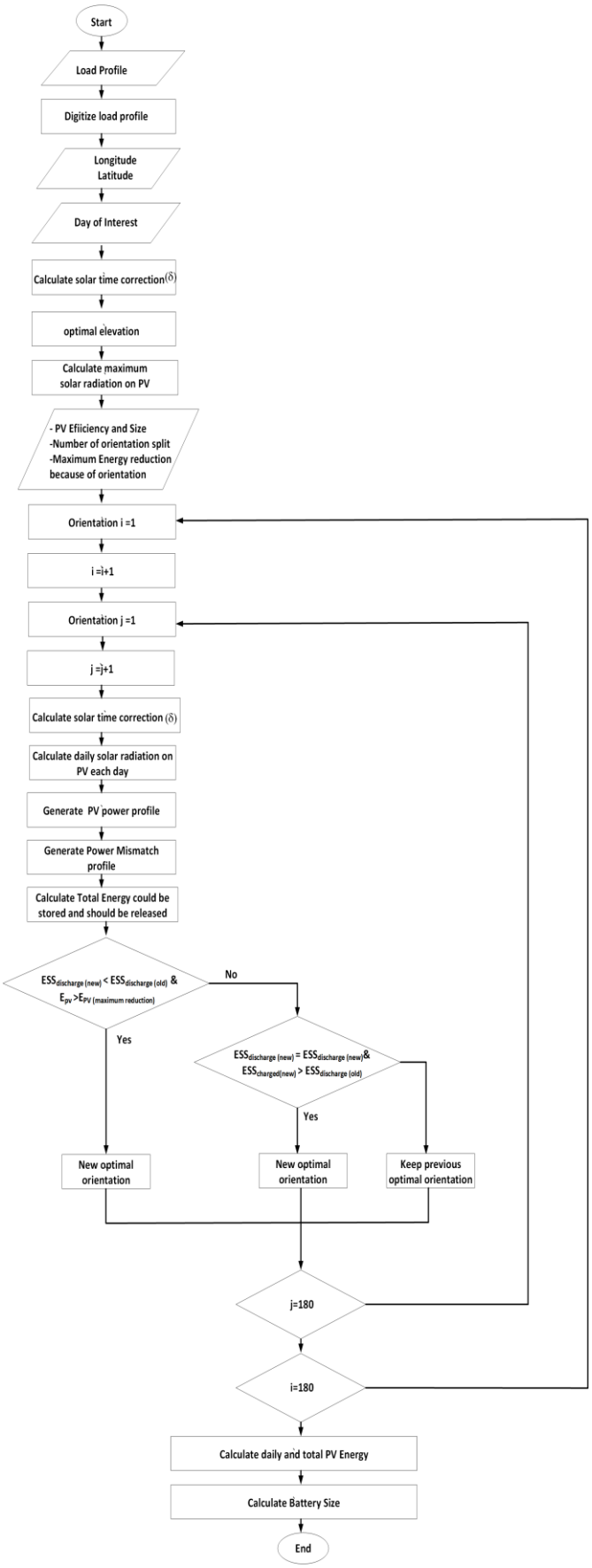


Figure 3.1 Algorithm of the energy storage minimization concept

Figure 3.1 provides an overview of finding the PV orientation and daily energy storage cycling. The solar radiation curves are adjusted within the specified constraints to align PV generation with the demand pattern or load profile. The constraint including maximum energy reduction, size of PV panel and number of orientations. This adjustment ensures more direct energy transfer from PV to EV load within date of interest. Therefore, the energy charge and discharge from the energy storage is minimized. The iteration method was used to determine best panel direction combination.

3.1 Load profile

Recognising the load profile in term of pattern and amplitude is a critical aspect of power procurement planning and capacity sizing. The load profile is used to determine the total daily energy demand E_{load} (in kWh), which can be estimated using the typical power demand of electric vehicles (in kW) using Equation (3.1). The annual energy demand, denoted as $E_{load(year)}$ is calculated by multiplying the daily average energy demand by the number of days (N) in a year, as shown in Equation (3.2). This value represents the total annual energy requirement, which can either be drawn from the electrical grid or the photovoltaic (PV) system within the charging station infrastructure. To ensure accurate energy estimation and effective system design, it is essential to account for the actual charging power profile.

$$E_{load} = \int_0^{24} P_{load}\, dt \approx \sum_0^{24} P_{load}\, \Delta t \tag{3.1}$$

$$E_{load(year)} = N\,.\,E_{load} \tag{3.2}$$

In this study, the energy source is assumed to be a photovoltaic (PV) system. The underlying hypothesis is that employing different PV panel orientations can increase the proportion of direct charging, thereby reducing the cycling of the energy storage system and enabling a reduction in the required battery capacity. This method will be further discussed in the following section.

3.2 Modelling of adjusted PV panel orientation

The quantity of solar radiation, also known as global solar radiation, comprises of direct solar radiation emanating from the sun, diffuse solar radiation reflected by the atmosphere and clouds, and a small amount from the ground surface's reflection. Among these, direct solar radiation is the primary element considered in this design for assessing solar radiation on the PV panel (Rad_{pv}).

Solar radiation on the PV panel (Rad_{pv}) is subject to change based on various factors, such as day, location, and daylight time. The maximum level of Rad_{pv} occurs when the panel is aligned perpendicular to the direction of the solar incidence (Rad_{solar}). The amount of direct solar radiation is associated with declination angle (δ), latitude (φ), solar time (ω), and solar altitude angle (α). The only adjustable parameters for controlling solar radiation on a PV panel are panel elevation (β) and orientation (τ). In this study, the solar radiation on a PV panel was calculated using Equation (3.3) [78].

$$\begin{aligned} Rad_{pv} = Rad_{solar} . (&\sin(\varphi)\sin(\delta)\cos(\beta) \\ &- \cos(\varphi)\sin(\delta)\sin(\beta)\cos(\tau) \\ &+ \cos(\varphi)\cos(\delta)\cos(\omega)\cos(\beta) \\ &+ \sin(\varphi)\cos(\delta)\cos(\omega)\sin(\beta)\cos(\tau) \\ &+ \cos(\delta)\sin(\omega)\sin(\beta)\sin(\tau)) \end{aligned} \tag{3.3}$$

The solar declination (δ) is defined as the relative angle between the sun and the earth's equatorial plane. The declination varies between - 23.45 in the winter solstice (21 December) and 23.45 summer solstice (21 June). The declination degree for any given day throughout the year (δ) can be calculated using Equation (3.4)

$$\delta = sin^{-1}\left(\sin(23.45)\sin\left(\frac{360}{365}(d-81)\right)\right) \tag{3.4}$$

Solar altitude angle (α) is the angular height of the sun which is measured with reference to the horizontal surface. It is determined by latitude (φ) and solar time angle (ω) as expressed in Equation (3.5). At solar noon, when the sun reaches its

highest point in the sky, the solar time angle (ω) is equal to 0, and the solar altitude angle is at its maximum. In the morning, before solar noon, the solar time angle (ω) become negative while in the afternoon it becomes positive, after solar noon.

$$\alpha = sin^{-1}(sin\delta \sin\varphi + cos\delta \cos\varphi \cos\omega) \tag{3.5}$$

The value of solar radiation (Rad_{solar}) reaching the ground is expressed by the empirical Equation (3.6) in kW/m^2 which states that it is equal to 1.353 kW/m2, also known as the solar constant. 0.7 shows only 70% of the radiation incident on the atmosphere is transmitted to the Earth and the power of 0.678 is an empirical value to fit the observed data.

$$Rad_{solar} = 1.353\ x\ 0.7^{AM^{0.678}} \tag{3.6}$$

Where the Air Mass (AM) refers to the reduction of light power as it is absorbed by air and dust upon passing through atmosphere. The Air Mass (AM) is denoted by the function α which represents the ratio of the path length of light through the atmosphere to the shortest path length, which occurs when α equals 90 degrees. By considering earth's curvature, Air Mass (AM) is expressed in Equation (3.7) [79].

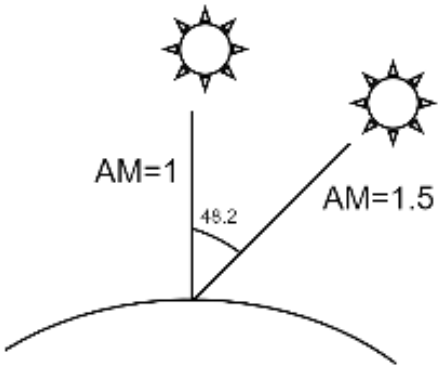


Figure 3.2 Air Mass

$$AM = \frac{1}{\cos(90 - \alpha) + 0.5057(6.0799 + \alpha)^{-1.6364}} \tag{3.7}$$

3.2.1 Calculating power and energy generated by PV

The power generated by a PV panel, P_{pv} is determined by the size of PV panel (A_{pv}) and its efficiency (μ) as shown in Equation (3.8). Therefore, the daily energy produced can be calculated using Equation (3.9). The square brackets indicate that the Equation is a 1 × N sampling time matrix.

The Equation (3.10) expresses the annual energy generated by the system. The performance ratio (PR) was included to represent the system's performance following the calculation of losses in the converter, temperature, and DC cable.

$$[P_{pv}] = [Rad_{pv}].A_{pv}.\mu \tag{3.8}$$

$$E_{pv} = \int_{sunrise}^{sunset} P_{pv}\, dt \approx \sum_{sunrise}^{sunset} P_{pv}\, \Delta t \tag{3.9}$$

$$E_{pv(year)} = PR.\sum_{d=1}^{365} E_{pv} \tag{3.10}$$

3.2.2 Modelling of the energy storage and car charging cycling

The power mismatch (P_m) in the Equation (3.11) is the difference between generated PV power and the demand power from EV charger. $[P_m]$ is a 1 × N matrix with elements derived by subtracting P_{pv} with P_{load} at successive sampling times.

$$[P_m] = [P_{pv}] - [P_{load}] \tag{3.11}$$

The graph shown in Figure 3.3 depicts a case of PV power generation and power demand for a particular day in a year without taking into account factors that lessen the power generation such as cloud or building shading. It is worth noting that the solar power curve results significantly has larger amount of energy captured for longer days, like those in the summer, and smaller amounts during the winter months.

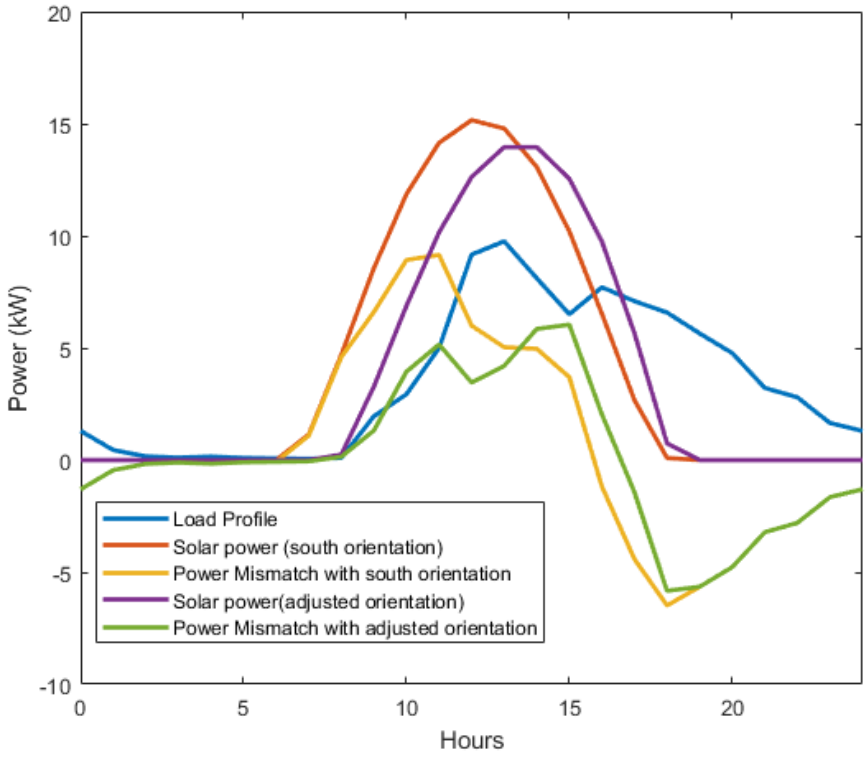


Figure 3.3 PV power of south and adjusted orientation, load demand and power mismatch between load demand and both solar power curve which is linearized hourly[43]

The positive power mismatch (P_m) in Figure 3.3 that happens during daytime signifies that the PV has excess power which is used to charge the ESS (buffer battery). The Equation (3.12) provides the amount of daily surplus energy, ESS_{charge} (in kWh) that needs to be stored in the buffer battery to provide charging power during evenings. Conversely, when P_m is negative, the buffer battery discharges ($ESS_{discharge}$) to support or supply power to electric vehicle demand. The total energy discharged daily is expressed in Equation (3.13).

$$ESS_{charge} = \frac{1}{2}\int_0^{24} (|P_m| + P_m)dt \tag{3.12}$$

$$ESS_{discharge} = \frac{1}{2}\int_0^{24} (|P_m| - P_m)dt \tag{3.13}$$

3.3 Finding adjusted orientation angle of PV panel

In the northern hemisphere, the orientation of photovoltaic (PV) panels ranges could be set up 90° to 90° from east to west and elevation from horizontal up to 90° (vertical). When a PV system is divided into multiple strings, each having different orientation. By applying a 1 degree step in the optimisation process, there are 180 × 180 combinations of orientations for each elevation angles that can be explored.

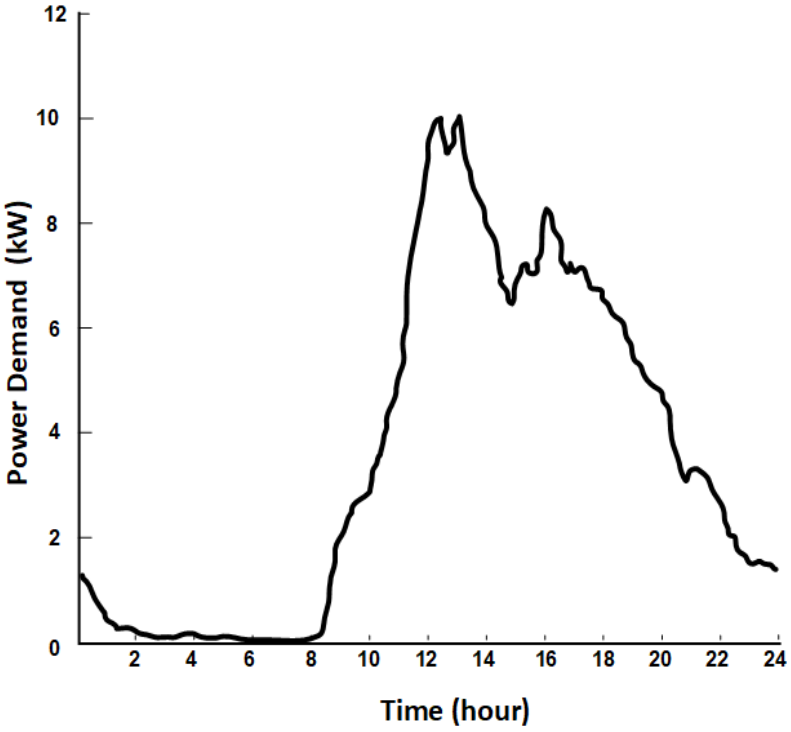
The analysis conducted in this study considered the PV panels are split into two strings of a fixed elevation and having two different orientations. The index variable of the two PV string orientations are denoted by "j" and "k" in Equation (3.14). The number of variables increases with the number of string orientations.

The method employs an iterative process to find the best orientation aimed at finding the optimal orientation that aligns best with the load profile. The purpose of this method is to minimize the size of the buffer energy storage while maintaining the result in term of best orientation based on minimum amount of energy need to be discharged from battery, maximum energy could be stored to battery above the PV power output constraint, thus preventing substantial PV power loss.

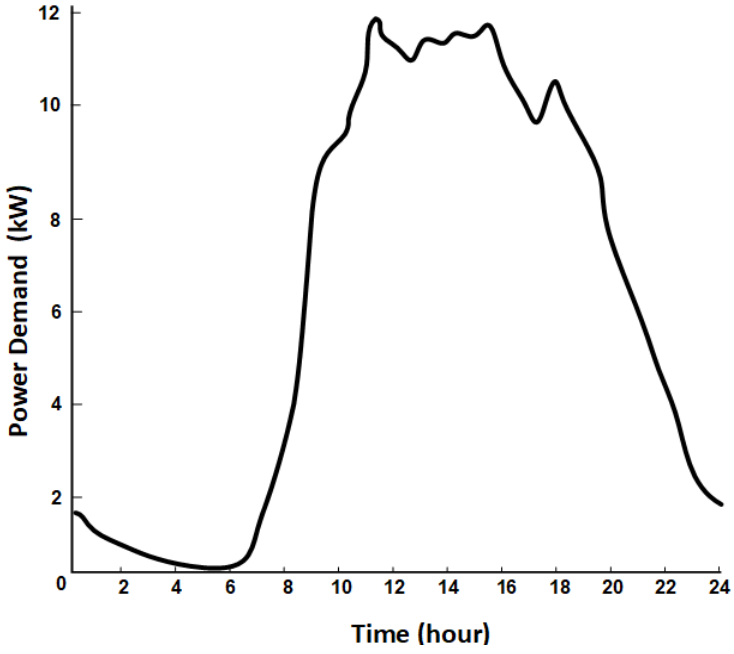
$$j,k = \begin{cases} (j,k)_{new} & for\ ESS_{discharge(new)} < ESS_{discharge(old)} \quad AND \quad E_{pv(new)} > Constraint\ (E_{pv(old)}) \\ (j,k)_{new} & for\ ESS_{discharge(new)} = ESS_{discharge(old)} \quad AND \quad ESS_{charge(new)} > ESS_{charge(old)} \\ (j,k)_{old} & else \end{cases} \tag{3.14}$$

3.4 Simulation result and discussion

Figure 3.4 shows load power consumption power profile data from two parking lots, one situated in a major North American campus network (Case 1) and the other in a London urban area (Case 2) from ref[11]



(a)



(b)

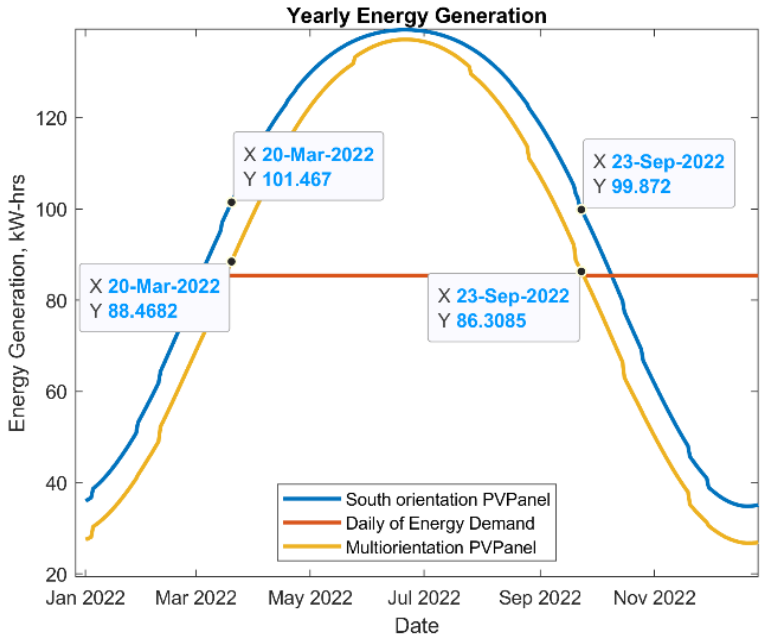
Figure 3.4 Real EV charger load profile as redrawn from ref [11] (a) case 1 (b) case 2

A significant drawback of this power mismatch method is the lack of a universal solution for all situations or scenarios. The method is applied to the load profile of Case 1 that is illustrated in Figure 3.4 (a) as an example. The selected location for the car park has the longitude and latitude coordinates of -0.116067° and 51.502338° North, respectively. It is necessary to design a total daily energy generated higher than that the daily energy demand. In practice, this condition can generally be met only during specific intervals of the year in both the northern and southern hemispheres. The chosen interval when the PV generated daily energy level would exceed the daily EV energy requirement is between the spring equinox on March 20th and the autumn equinox on September 23rd. In higher northern latitudes, solar energy generation becomes less viable during periods when the length of the day is shorter than the length of the night. In such conditions, the limited daylight hours result in insufficient solar irradiance, making energy harvesting economically and technically unworthy. Outside of these intervals, particularly during extended winter nights, the potential for solar energy generation becomes minimal, which reduces the effectiveness of solar-based systems. The other consideration is the maximum elevation. This is introduced if the implementation of solar powered is embedded on roof. It is found that for this location, the best fix panel elevation is 34^{o} and within UK standard of roof slope [80], [81]. PV panel in this case was LG NeonR LG380Q1C-V5 model. It has a higher efficiency (μ) of 22%[82].

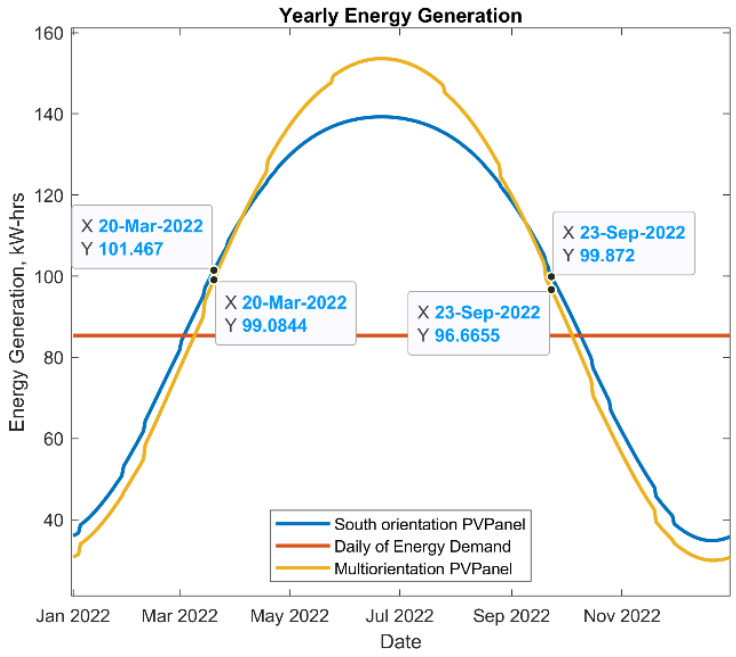
The annual amount of solar energy generated by PV Panel in the Case 1 is illustrated in Figure 3.5(a). In the winter months, the amount of solar energy generated is noticeably lower than the demand, making it logical to design a system that operates when solar energy is able to meet the energy requirements. This day interval is pointed in Figure 3.5 where the PV-generated energy was above the line of the daily energy demand. The amount of solar energy generated annually using multi-orientation is less than south orientation. The level of energy loss due to a non-optimal/skewed (from maximum) orientation is dependent on the design constraints that have been implemented.

The graph presented in Figure 3.5 (a) indicates that the daily energy produced by a 18.54 kW rated power PV system of multiple orientation photovoltaic strings is constantly lower than that energy generated by the same rated power

system if it would was best (south-facing) orientation. An increase in the rated power and therefore in the number of PV panels is required to achieve a comparable level of daily energy output, as shown in Figure 3.5(b).



(a)

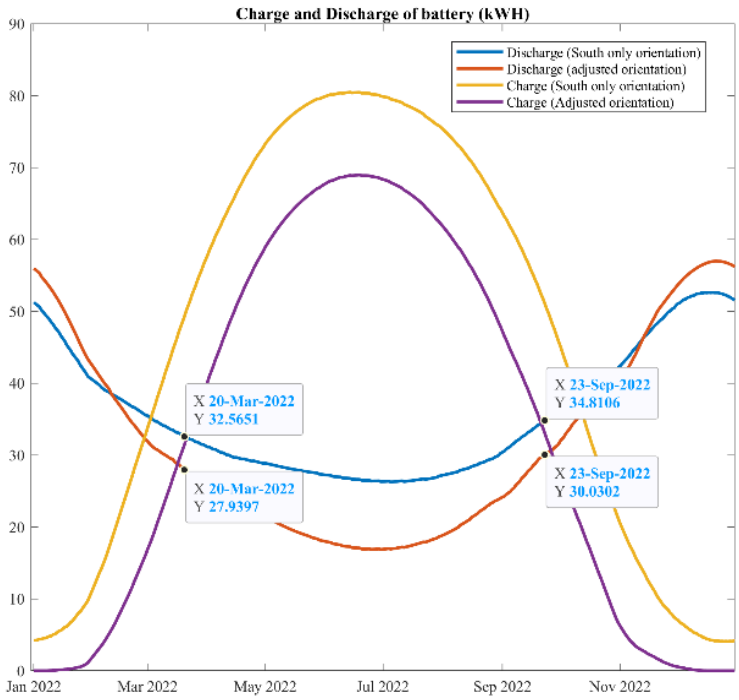


(b)

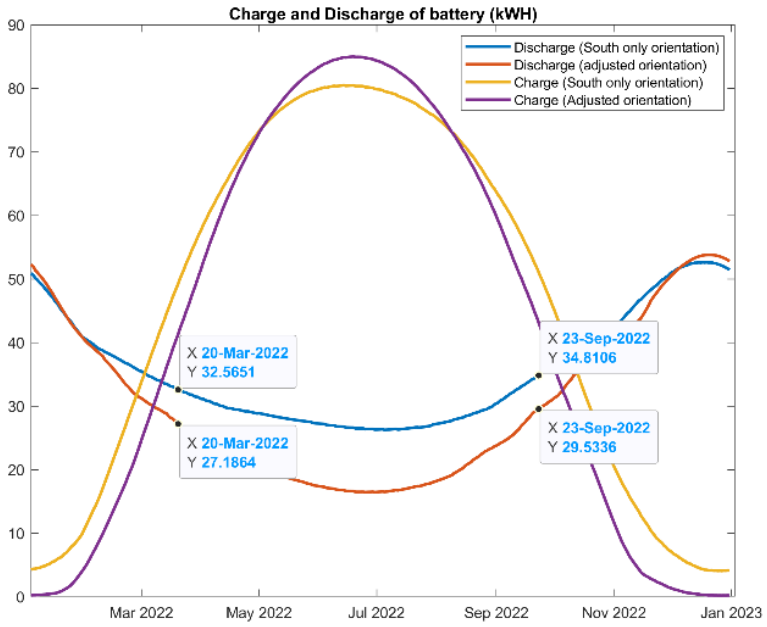
Figure 3.5 Daily PV energy generated during the year by a 18.54kW rated PV system oriented 41 and 50 to the west : (a) without PV size increment (b) after 12% PV size increment.

Figure 3.6 illustrates that the energy supplied or discharged from the battery for the adjusted orientation was less than that for the most convenient (south) orientation, as anticipated. This demonstrates how the modified orientation of the photovoltaic string reduces energy storage.

Figure 3.5(a) shows that the cycling of power charged and discharged from the battery for the PV strings with adjusted orientation to match with load profile is less than that in the south orientation. This is an essential finding for a system that targeting minimizing energy storage. Figure 3.5(b) shows that the size of battery required refers to after an increase in the PV size to achieve similar amount of energy generated with south generation. The maximum daily energy discharged in the specific time chosen in case 1 are 30.03 kWh and 29.53kWh before and after PV panels size increment respectively. This value is less than south only orientation which need 34.81kWh. This critical point value was used for determining minimum energy storage required (E_{Bmin}) in the system. It is noteworthy that the adjusted PV panels are more advantageous in terms of the lower depth of the discharged cycles during the interval time.



(a)



(b)

Figure 3.6 Energy charged and discharged from battery during the year (a) without PV size increment (b) with PV size increment after PV size increment.

Tables 3.1 and 3.2 summarise the results of the proposed method for reducing the size of the buffer energy storage when charging electric vehicles (EVs) using solar power. Although altering the orientation of the solar panel results in a decrease in the overall energy produced, the need for battery storage is reduced. It is important to note that if the orientation is adjusted, there will be a requirement for a larger PV system to produce the same amount of energy as the south (best energy case) orientation, with a corresponding decrease in the energy storage size.

Table 3.1 Comparison between South orientation and adjusted orientation PV panel to minimize energy storage for case 1.

Parameter	***18.54kW PV system peak of South orientation***	***Adjusted orientation***	
		18.54kW PV system peak	***20.83kW PV system peak***
PV Panel			
Elevation	34º	34º	34º
Orientation string #1	0 (south)	41 º (west)	41 º (west)

Parameter	***18.54kW PV system peak of South orientation***	***Adjusted orientation***	
		18.54kW PV system peak	***20.83kW PV system peak***
Orientation string #2	0 (south)	50^{o} (west)	50 ^{o} (west)
Size (m^2)	89	89	100 (+12%)
Annual PV Energy generated (kWh)	34708.19	31365.72	35129.61
Load			
Daily (kWh)	85	85	85
Annual (kWh)	31,025	31,025	31,025
Energy Storage			
Minimum Energy storage between spring to autumnal equinox interval(kWh)	34.81	30.03	29.53
Annual discharge cycle energy to battery(kWh)	13020.11	11686.53	11210.32
Annual charge cycle energy to battery(kWh)	16841.56	12170.86	15516.36

Table 3.2 Annual energy comparison adjusted orientation for case 1 compared to South orientation

Comparison	***18.54 kW PV size increment***	***20.83kW PV size increment***
Annual PV energy generated	90.36 %	100.01%
Minimum Energy storage between spring to autumnal equinox interval(kWh)	86.2%	84.81%
Annual discharge cycle energy to battery(kWh)	89.76 %	86.10%
Annual charge cycle energy to battery(kWh)	72.66 %	92.13%

The same method was also applied to Case 2 for validation. It is assumed that the load pattern in Case 2 occurs at the same location as in Case 1 to be able to discuss differences without having to consider additional aspects related to a different location of the PV system. Tables 3.3 and 3.4, show that an adjusted orientation is recommended to decrease battery size. It is found that the adjusted orientation becomes less effective when there is more demand during nighttime, as the amount of energy that can be stored in the battery is reduced during daylight hours.

Table 3.3 Comparison between south orientation and adjusted orientation pv panel to minimize energy storage for case 2

Parameter	***28.96kWP PV system of South orientation***	***Adjusted orientation***	
		28.96kWP pv system	***30.42kWP pv system***
PV Panel			
Elevation	34°	34°	34°
Orientation of PV string #1	0	-2 ° (east)	-2 ° (east)
Orientation of PV string #2	0	44 ° (west)	44 ° (west)
Size (m^2)	139	139	146
Annual PV Energy generated(kWh)	54207.19	51775.55	54364.3219
Load			
Daily (kWh)	139	139	139
Annual (kWh)	50,735	50,735	50,735
Energy Storage			
Minimum Energy storage between spring to autumnal equinox interval(kWh)	51.58	50.54	49.92
Annual discharge cycle energy to battery(kWh)	19986.45	19418.38	19101.90
Annual charge cycle energy to battery(kWh)	23794.26	21204.84	23542.24

Table 3.4 Annual energy comparison between south and adjusted orientation for case 2

Comparison	***Without PV size increment 28.96kWP***	***With PV size increment 30.42kWP***
Annual PV energy generated	95.51 %	100.28%
Minimum Energy storage between spring to autumnal equinox interval(kWh)	97.98%	96.78%
Annual discharge cycle energy to battery(kWh)	97.16%	95.57%
Annual charge cycle energy to battery(kWh)	87.12 %	98.94%

3.4.1 Return on Investment of six-month seasonal operation of standalone PV-EV charging station

Using two PV strings with adjusted orientation require a lower discharged energy cycle during the interval time. Furthermore, Equation (3.15) presents parameter to design an adjusted battery size in the system[83]. The parameters include the load subsystem efficiency (μ), temperature compensation factor (T) and depth of discharge of battery (DoD) which means the percentage of the battery nominal energy that can actually be accessed during operation.

$$B_{size}(\text{kWh}) = \frac{E_{Bmin} .D.\ T}{\mu\ .DoD} \qquad (3.15)$$

In this approach,E_{Bmin} represents the minimum battery capacity required for daily cycling, rather than the size based on the minimum daily load because the latest gives negative return on investment (ROI) even only using one day of autonomy (D = 1), Referring to data obtained from Case 1 in Tables 3.1 and 3.2, the calculation for the battery energy size E_{Bmin} was 34.81 kWh for south only PV orientation, 30.03 and 29.53 kWh for the adjusted size and orientation of the two string PV panels 18.54 and 20.83 kW PV system peak respectively, a DoD of 50 % (which is suitable for lead acid battery), 85% load sub system efficiency with a 1.19 temperature coefficient factor yields a round up 98 kWh, 85 kWh and 83 kWh for each condition in case 1.

Capital expenditure (CAPEX), include the cost of solar panels, batteries, installation, converters, structures, and other equipment. In evaluating the CAPEX for the off-grid solar model, the costs associated with purchasing and installing solar equipment are calculated by multiplying the approximate cost per peak power by the total peak power of the photovoltaic (PV) plant. While the plant operational expenditure (OPEX) is annual operating and maintenance cost. This includes routine maintenance, inspections, component replacements, and other operational expenses. Based on reference[84] the CAPEX of a PV system is estimated at £2,200 per kWP, excluding energy storage components, while the OPEX is assumed to be 1% of the CAPEX per year. These values are applied in this study as presented in Table 3.5.

Table 3.5 Cost breakdown calculation for PV-EV charging station for case 1

Item	price	18.54kW PV system peak of South orientation	Adjusted orientation	
			18.54kW PV system peak	20.83kW PV system peak
CAPEX £/kWP	2,200	£40,788	£40,788	£ 45826
OPEX £/kWP per year	22	£407.88/year	£407.88/year	£458.26
Battery	100/kWh	£ 9,800	£8,500	£8,300
Battery replacement[a]		£1,225/year	£1062.5 /year	1037.5/year
Electricity price	£0.3/kWh	£3,712.8[b]	£3,712.8[b]	£3,712.8[b]
ROI		2.79%	13.74%	2.40%

[a] every 8 years, [b] 6 months seasonal operation,

Considering a six-month seasonal operation and assuming a 20% unmet load, the annual revenue is estimated to be £3,712.8. The cost of battery storage is incorporated into the CAPEX, while battery replacement costs are accounted for within the OPEX. Using the Equation (3.15), the return on investment (ROI) over a 25-year period (typical for PV systems) is calculated to be 2.79% for the south-only orientation. For the adjusted orientations, the ROI values are 13.74% and 2.40%, respectively. These results indicate that the ROI can be improved by optimising direct charging from the PV array to the EV. However, for the same revenue and seasonal operation time, increasing the PV capacity, may lead to a lower overall ROI.

$$ROI = \frac{-CAPEX + (\sum Revenue - OPEX)}{CAPEX} \; x \; 100\% \tag{3.16}$$

Table 3.6 Cost breakdown calculation for PV-EV charging station for case 2

Item	price	28.96kW PV system peak of South orientation	Adjusted orientation	
			28.96kW PV system peak	30.42kW PV system peak
CAPEX £/kWP	2,200	£63,712	£63,712	£ 46574
OPEX £/kWP per year	22	£637.12	£637.12 per year	£465.74
Battery	100/kWh	£ 14,500	£14,200	£14,000
Battery replacement[a]		£1,812.5/year	£1,775 /year	£1,750 /year
Electricity price	£0.3/kWh	£6,071.5[b]	£6,071.5[b]	£6,071.5[b]
ROI		15.77%	17.42%	12,83%

[a] every 8 years, [b] 6 months seasonal operation,

The system operates for only six months each year, which represents the primary financial constraint. During summer, the PV array generates more than the load demand. In an off-grid configuration, this surplus energy must be stored to supply the load during cloudy periods and at night. Consequently, a very large battery bank is required, resulting in significant capital expenditure and substantial unused energy. Under these conditions, battery investment becomes the dominant cost component influencing the ROI. Apart from grid connection the V2V can improve the system as it can be alternative energy buffer

Although the methodology in this section is based on using a relatively small battery to meet the daily load, the fundamental issue remains the mismatch between the high capital expenditure and the relatively low annual revenue. In both Case 1 and Case 2, the use of a smaller battery combined with a 20% assumption of unmet load results in a system that is still financially plausible although yields only small profit either for south orientation or directed orientation.

In a parking lot, the installation of a PV-powered EV charging station adds value by providing shade for electric vehicles and allowing their batteries to be charged while they are parked. Figure 3.1 illustrates a standalone photovoltaic powered-electric vehicle (PV-EV) charging station equipped with energy storage system.

The system can be improved by facilitating Vehicle to Vehicle (V2V) charging capability. This scenario is simulated in Chapter 5. In parking lots with extended stay durations, a transactional energy system between vehicles could help reduce the size of the buffer energy and to the EV owners, the possibility to benefit from reduced parking fees. However, it is crucial to make the operation rule of charging stations to efficiently utilize resources and enhance overall user satisfaction.

3.5 Summary

This study examined the impact of adjusting the PV panel orientation of some of two groups/strings of PV panels to minimize the required size of the buffer energy storage needed by a PV powered-EV charging station. The study concluded that better panel orientation could increase the amount of PV power directly being supplied to the EVs, thus reducing the need/size of the buffer

energy storage battery in off grid solar-powered charging station, even though the total solar energy produced during the day decreases due to suboptimal solar energy capturing. Two cases of real power profiles published in [11] consumed by EVs whilst parked in a public car park were rescaled to match the parameters of a simulation study. When optimising the PV panels orientation for Case 1, it was found that a reduction of 15 % of the original battery size was possible and more with the increase in the PV size. In Case 2, the battery size reduction is not significant because the nighttime load demand is relatively high. These findings are relevant to investors in deploying renewables when designing public EV chargers especially in remote locations where power grid available power is limited and when trying to minimize investment in solar-charged electric vehicles in car parks.

However, this study was subject to two potential methodological weaknesses. Firstly, it was assumed that the exact load demand was recurrent every day, therefore, a 20% unmet load was included to account for variability. Secondly, it does not consider the weather variability that affect daily solar energy production, such as temperature and shading on solar panels. Although the results may vary depending on location, the findings of this study have important implications for future research and practice in minimizing the size/ the cycling of the buffer energy storage facility that may be required to be available in a public charging station/car park.

Several operational limitations accompany a stand-alone PV-EV charging station. The service quality becomes less reliable because charging availability cannot be guaranteed. Moreover, all generated solar energy is wasted on days with no customers and insufficient battery to store the energy. Additionally, the effective operation requires intelligent control, as the PV system component within the charging station must coordinate to fulfil the charging demand. The proposed converter and control will be discussed in the next chapters.

Although a stand-alone system is suitable for deployment in remote locations where grid access is limited, integrating a grid connection remains the most practical and economically advantageous approach. A grid-connected configuration eliminates the need for large battery storage, increases system

reliability, and maximizes the utilisation of the charging station throughout the year.

Future research could explore lower energy storage requirements for standalone PV powered charging stations by applying power smoothing management, which utilizes EVs parked for long durations in the parking lot as temporary energy storage buffers.

Chapter 4

Modelling of a Compact Bidirectional Three-Level Interleaved DC/DC Converter

Compared to conventional power converter, multilevel and multiphase/interleaved converters offer several key performance advantages that make them the choice for high-power, high-performance applications: reducing input and output capacitance, improving thermal performance and efficiency at high load currents, as well as improving overshoot and undershoot during load transients [85], [86], [87].

This chapter presents a comprehensive introduction of the bidirectional three-level interleaved (B3LI) DC/DC converter, including B3LI circuitry, distinctive attributes, and a comprehensive mathematical model. The B3LI DC/DC converter comprises two-phase of three-level flying capacitor converters, each with four switches and a flying capacitor. The converter operates alternating between inductor energization, capacitor charging, capacitor discharging, and inductor de-energization.

The B3LI DC/DC converter incorporates bidirectional DC power flow, three voltage levels, and interleaving techniques to enhance performance and with voltage/current distribution that allow efficient power conversion solution for high voltage/current/power electric vehicle charging applications. The bidirectional feature enables efficient charging and discharging of batteries in electric vehicles, while the three-level configuration reduces voltage stress on switches compared to two-level converters. The interleaved configuration, share the current between the parallel power stages with individual inductors and switches, improves thermal performance, efficiency, and transient response. The mathematical model and operational principles discussed in this chapter to

provide a foundational framework for understanding and controlling the B3LI converter in high-power, high-performance applications.

4.1 Maximizing power density with B3LI DC/DC converter topology

In Chapter 2, it was mentioned that operating DC/DC converters in two-voltage level mode poses challenges in scaling to higher voltage ranges and increases of passive component sizes. This limitation primarily comes from the high $^{dv}/_{dt}$ stress imposed on the power semiconductor switch and the insulation of the inductor winding. A potential solution discussed involves using multi-voltage level converter topologies and the interleaving method to split the voltage and current levels and stresses whilst also allowing a smaller size of passive components to be used in the associated filters.

Compared to conventional two-level converters, higher level design offers significant advantages, including reduced voltage stress on semiconductor devices, diminished electromagnetic interference (EMI) issues, and lower output harmonic distortion. These benefits have facilitated its adoption in both AC/DC and DC/DC conversion systems. The first multi-level converter introduced was NPC (Neutral Point Clamped) three level inverter by reference [88] which has positive, negative and neutral point. Reference [89] introduced a three-level DC/DC converter NPC leg with galvanic isolation. Reference [90] expanded upon this concept by integrating two three-level diode-clamped. While in the context of non-isolated, reference [91] gives a systematic method to derive a non-isolated three-level DC/DC converters.

4.1.1 From two-level to three-level DC/DC converter

In case of isolated three level converter, the popular NPC can be integrated into an isolated dual-active-bridge (DAB) or other isolated stages Figure 4.1(b). The challenge three-level NPC converter in practical deployment is limited by the inherent difficulty of maintaining voltage balance across the neutral point [92]. The non-isolated three level NPC DC/DC converter typically realized as DC–AC–DC (rectifier) rather than a direct chopper.

While in the context of non-isolated electric vehicle (EV) charging, standardized mechanisms have not yet been fully established [17]. Two notable candidates for non-isolated three-level topologies are the bidirectional three-level buck converter [93], [94]and flying-capacitor converter as illustrated in Figure 4.1(c) and (d). In both topologies, the input and output voltage polarities remain fixed, while the current can flow bidirectionally. The adoption of a three-level structure increases the inductor current ripple frequency to twice the switching frequency, which facilitates a reduction in the size of passive components. Nevertheless, each topology presents unique voltage-balancing challenges: in the flying-capacitor converter, the voltage across the flying capacitor must be regulated to half of the DC-link voltage, whereas in the three-level buck converter, neutral-point voltage stability must be preserved. An additional advantage of the flying-capacitor converter is its provision of a common ground between the input and output terminals and modularity[95], which can simplify system integration and grounding design.

The 3-level flying capacitor DC/DC converter is designed with a floating capacitor, C_f, and two pairs of switches instead of one pair in the conventional two-level converter, as shown in Figure 4.1. This configuration maintains the flying capacitor at half the input voltage; therefore, the switch node voltage are 0, $V_{dc}/2$, and V_{dc}. When the high side voltage exceeds twice the lower side voltage, the switch node alternates between 0 and $V_{dc}/2$. When the high-side voltage falls below twice the low-side voltage, the switch node alternates between $V_{dc}/2$ and V_{dc}.

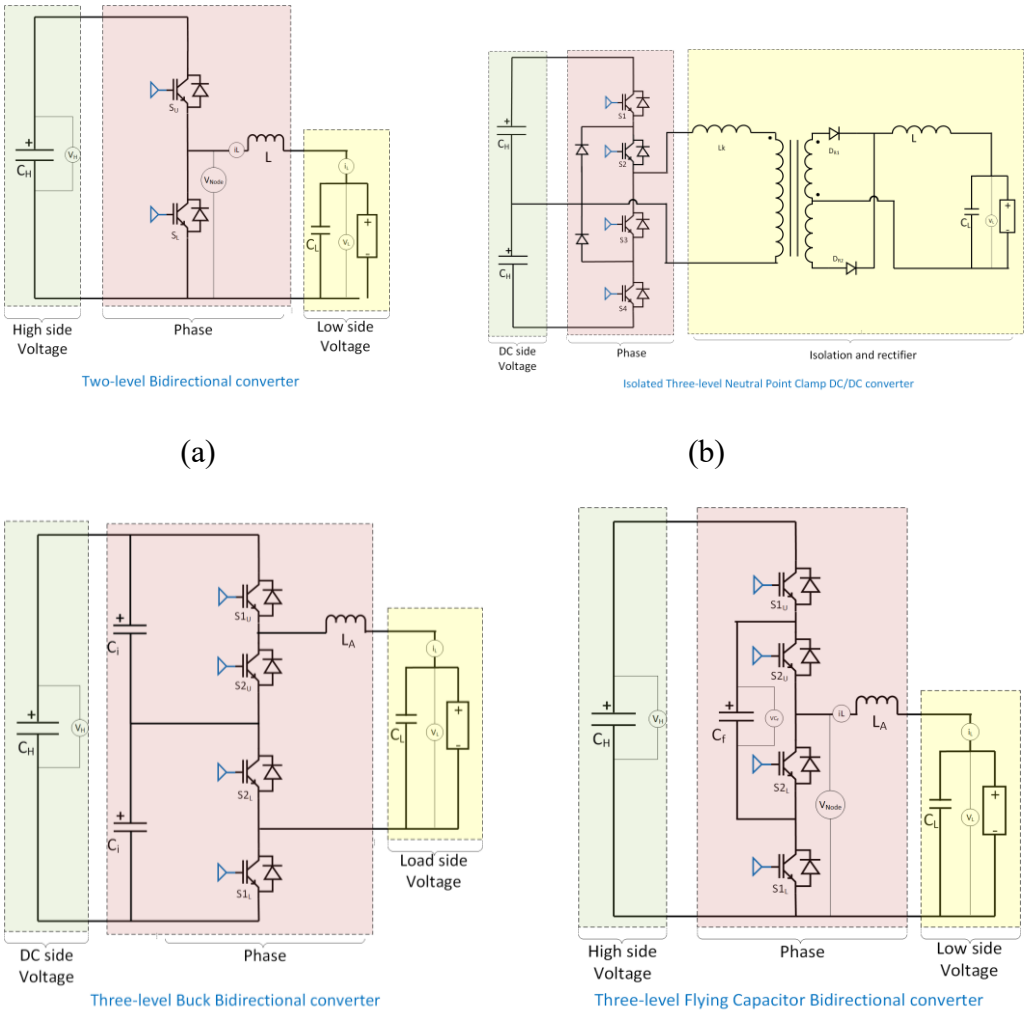


Figure 4.1 DC/DC converter (a) Conventional two-level converter, (b) isolated three-level NPC Converter, and (c) three-level buck converter and (d) three-level flying capacitor converter

Figure 4.2 shows the operation cycling three-level flying capacitor converter for buck operation when D< 0.5. The cycle consists of four stages. First is when $S1_U$ and $S2_L$ are on, this will make the flying capacitor, C_f get charged and the inductor is energized. Since V_{cf} is half of V_{dc}, at the switch node, V_{node}, the voltage is equal to $V_{dc}/2$. In the second stage both $S1_L$ and $S2_L$ are turned on, connecting the switch node to the ground therefore the V_{node} become 0 and the flying capacitor C_f disconnected. At this stage the inductor is de-energized. During the third stage, $S2_U$ and $S1_L$ are on, the flying capacitor C_f is directly connected across the switch node. At this time the capacitor is discharge and the inductor energized. The last stage, $S2_U$ and $S1_L$ are on again as the second stage,

this make V_{node} goes to zero, while the capacitor disconnected, and the inductor de-energized. The stages are the same as boost operation when D>0.5 with current flow in the opposite direction.

At duty cycle equal to 0.5, the flying capacitor remains connected and undergoes charging and discharging processes as in the first stage and third stage. Consequently, the voltage at the switch node is maintained at half of the V_{dc}, and current flowing through the inductor is ripple free. At this operating point, the topology operates as a switched-capacitor converter, and under ideal conditions, the use of inductors is unnecessary.

When the duty cycle is higher than 50%, $S1_U$ and $S2_U$ are turned on simultaneously at the second and fourth stages. Therefore, in this time the switch node alternates between $V_{dc}/2$ and V_{dc}. Figure 4.3 shows the operation cycling three-level flying capacitor converter when D> 0.5. The stages are the same as boost operation when D<0.5 with current flow in the opposite direction.

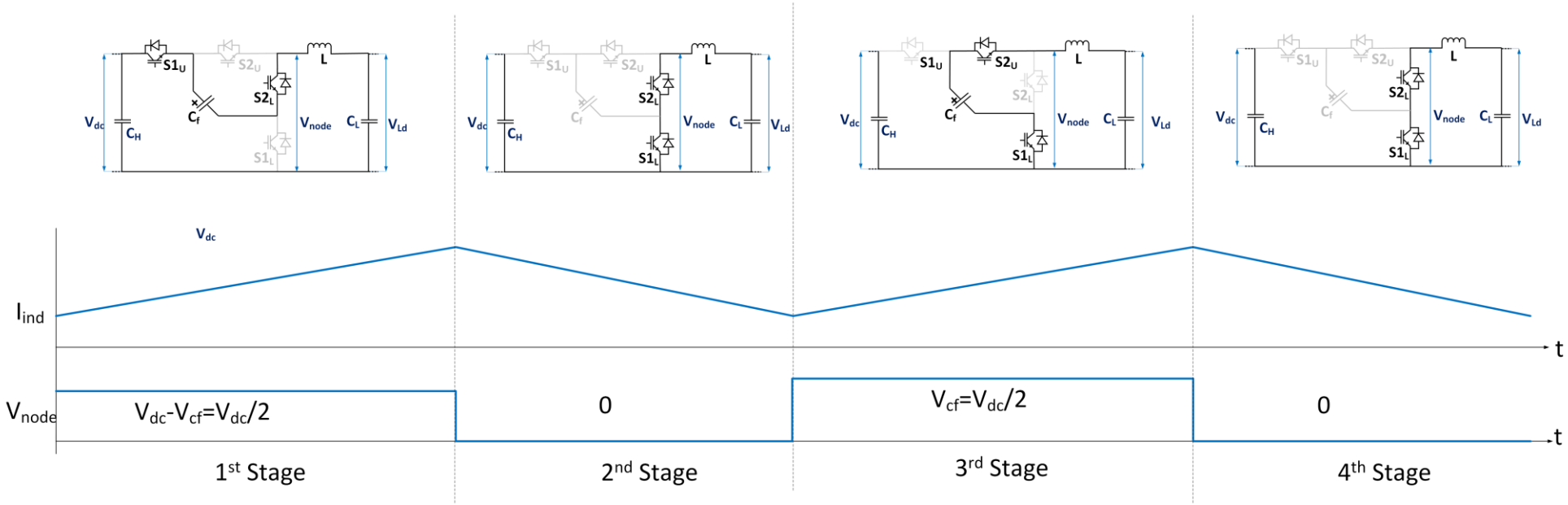


Figure 4.2 Single phase three-level flying capacitor operation for buck operation when D <0.5 or boost operation when D>0.5

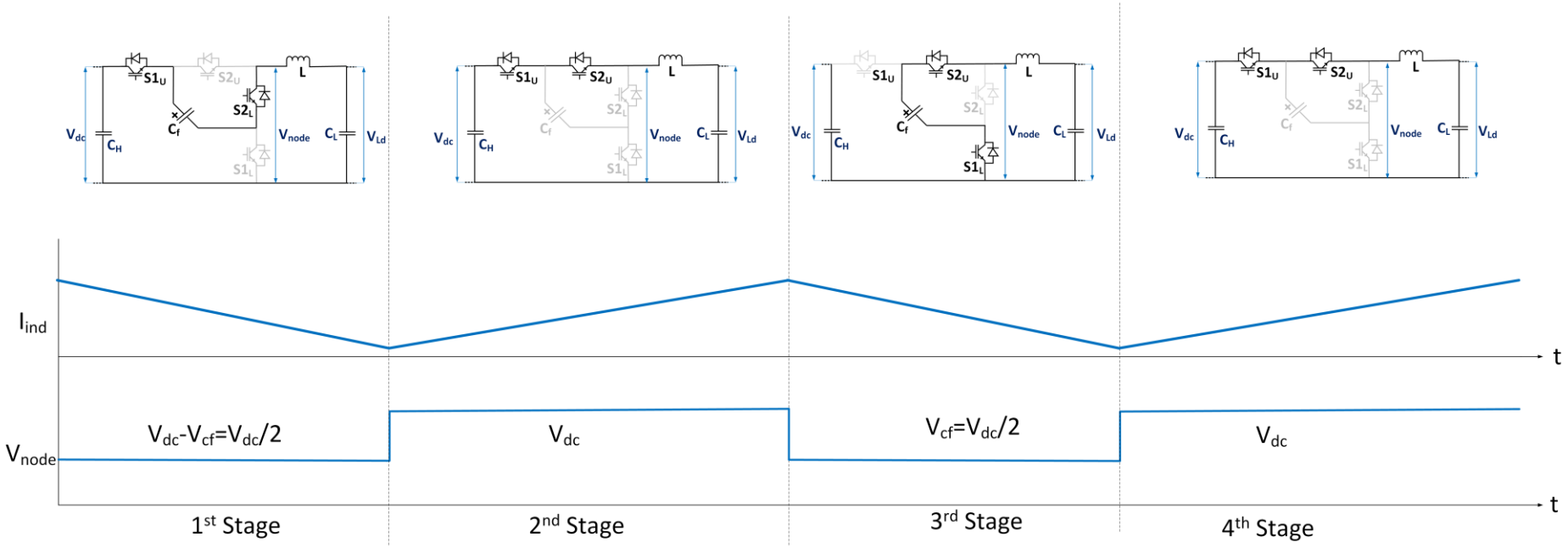


Figure 4.3 Single phase three-level flying capacitor operation when D > 0.5 or Boost operation when D<0.5

All operations have two distinct stages, one in which the flying capacitor is charged and another in which it is discharged. The quantity of charge energy at the initial stage will be released during the latter stage as depicted in Figure 4.4. As a result, the capacitor's voltage is maintained at $V_{dc}/2$ in a steady-state operation. It is crucial to maintain this flying capacitor voltage to ensure the voltage across switches and inductor also at $V_{dc}/2$. This can be done by apply a specific voltage controller.

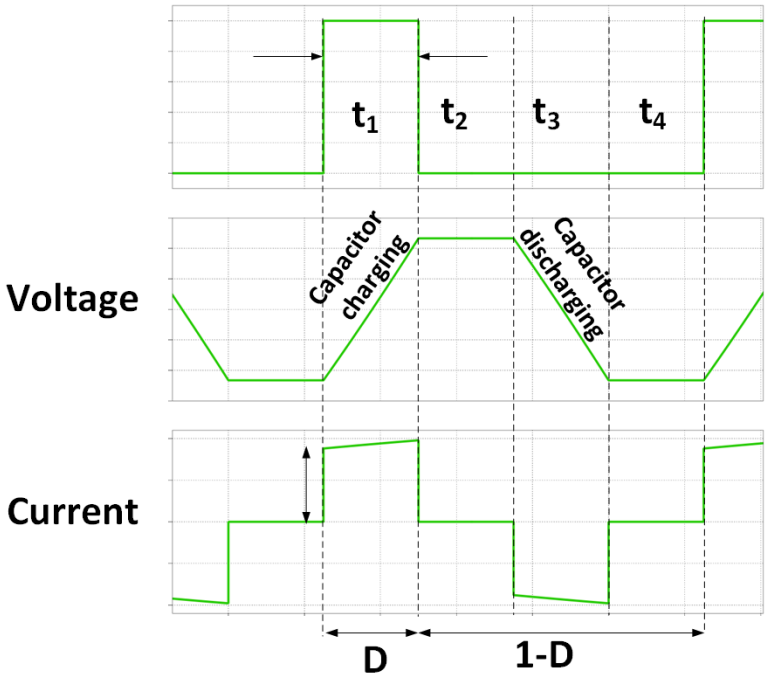


Figure 4.4 Flying capacitor charging and discharging when D < 0.5 for buck operation or D >0.5 for boost operation

In case of the flying capacitor voltage to be lower than $V_{dc}/2$, it is necessary to charge the flying capacitor until it reaches $V_{dc}/2$, thus ensuring the proper functioning of the converter. This may be accomplished by either extending the charging time or shortening the discharging time. On the other hand, if the voltage exceeds $V_{dc}/2$, the charging time must be reduced, and an increase in the discharging time should be implemented to bring the voltage of the flying capacitor to $V_{dc}/2$. This following the capacitor general formula as expressed in Equation (4.1) .

$$V(t) = \frac{1}{C}\int_{0}^{t} i\,dt + V_0 \tag{4.1}$$

The 3-level converter discussed offers significant advantages. Firstly, voltage stress across the inductor and the switches is reduced by half during all operational modes. Therefore the 3-level switches only require blocking half of the input voltage to achieve their transitions, thereby reducing the associated switching losses. Secondly, the switching frequency at the switch node doubles. These two factors decrease the maximum inductor current ripple four times compared to a conventional two-level converter. Figure 4.5 depicted the ripple current reduction from the two-level to the three-level DC/DC converter which is mathematically expressed by the Equation (4.2), (4.3) and (4.4). In two-level interleaved DC/DC converters [96] the carrier signal for each of the leg's PWM is phase shifted 180°. However, in terms of current ripple reduction, this configuration benefits from ripple cancellation between phase at the output node.

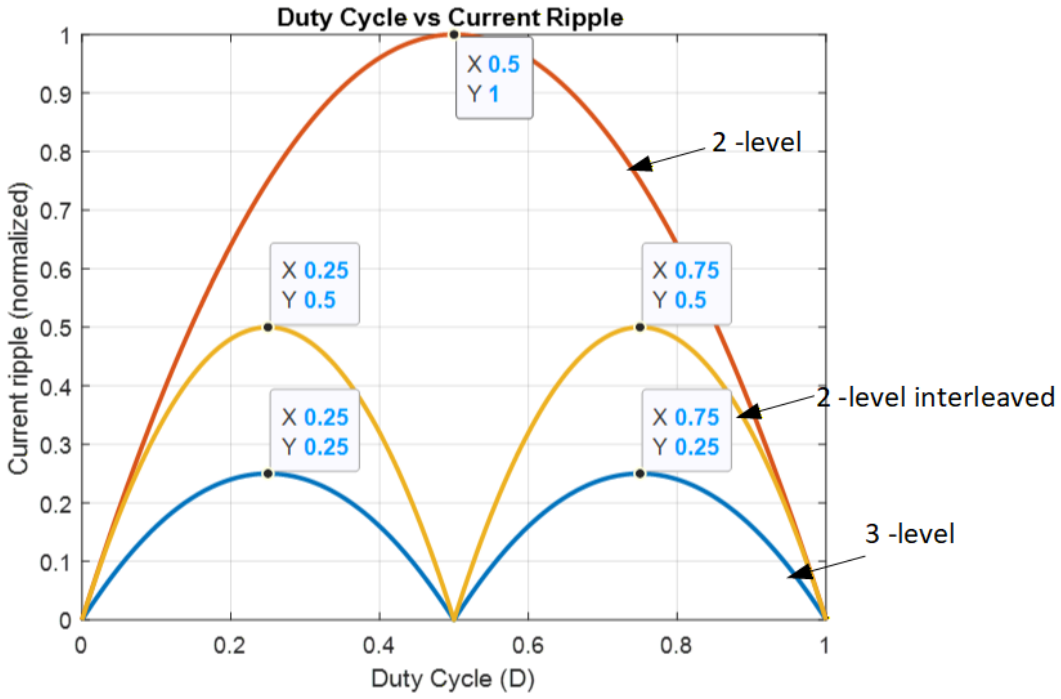


Figure 4.5. Normalized current ripple comparison on inductor between 2-level and 3-level DC/DC converter

$$\Delta I_{L\,two-level} = \frac{V_{dc}\,D(1-D)}{L\,f_s} \tag{4.2}$$

$$\Delta I_{L\,two-level\,interleaved} = \frac{V_{dc}\,D(1-\mathrm{D})}{L\,f_s}\sqrt{\left(D-\frac{m}{2}\right)\times\left(\frac{m+1}{2}-D\right)} \tag{4.3}$$

With $m = integer\ of\ (2\ \times D)$

$$\Delta I_{L\,three-level} = \frac{V_{dc}(\,D-0.5\,m)(0.5-(D-0.5m))}{8L\,f_s} \tag{4.4}$$

With $m = integer\ of\ (2\ \times D)$

The inductor current ripple, ΔI_L is used to determine the inductance value L, The smaller ripple current flows also affect the capacitance value required to effectively filter out the fluctuations of the low side voltage of the converter as in Equation (4.5). Where T is the switching period. Figure 4.6 show the expected voltage reduction on the low side voltage which follow the Equation (4.1).

In term of sizing, the smaller current ripple characteristic of three-level DC/DC converter permits the utilization of a smaller inductor. However, reducing the inductance value leads to an increase in ripple, necessitating a corresponding increase in capacitor size in the to ensure proper filtering. Therefore, careful consideration is warranted.

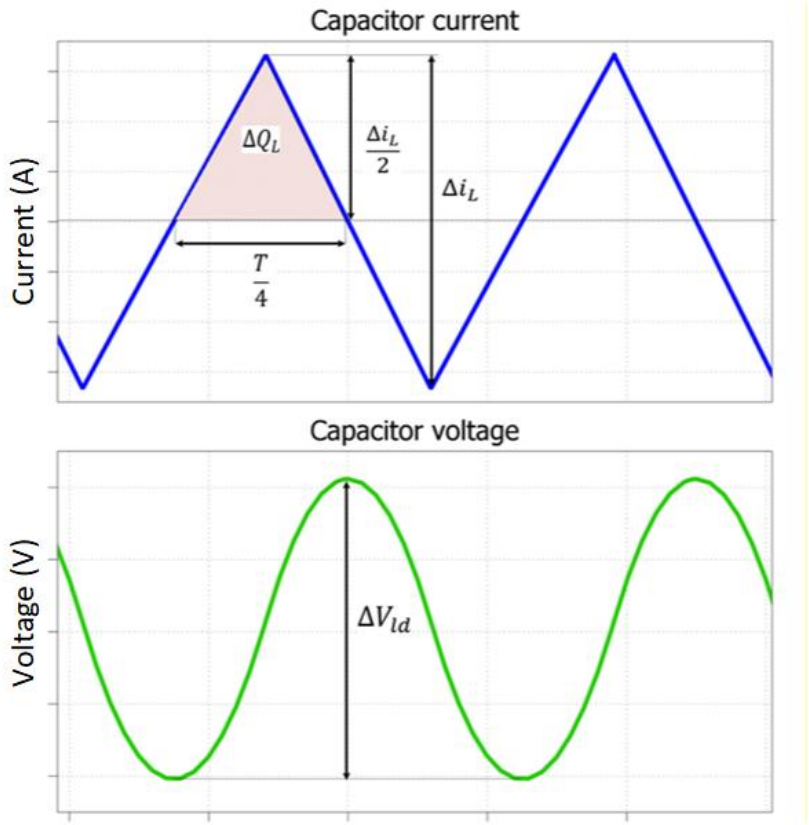


Figure 4.6. Lowside capacitor steady state ripple current and voltage.

$$|\Delta Q_L| = C_L \cdot \Delta V_{ld} = \frac{\Delta i_L \, T}{16} \tag{4.5}$$

The high-side voltage ripple can be seen in Figure 4.7 with charging of input capacitor as in Equation (4.6)

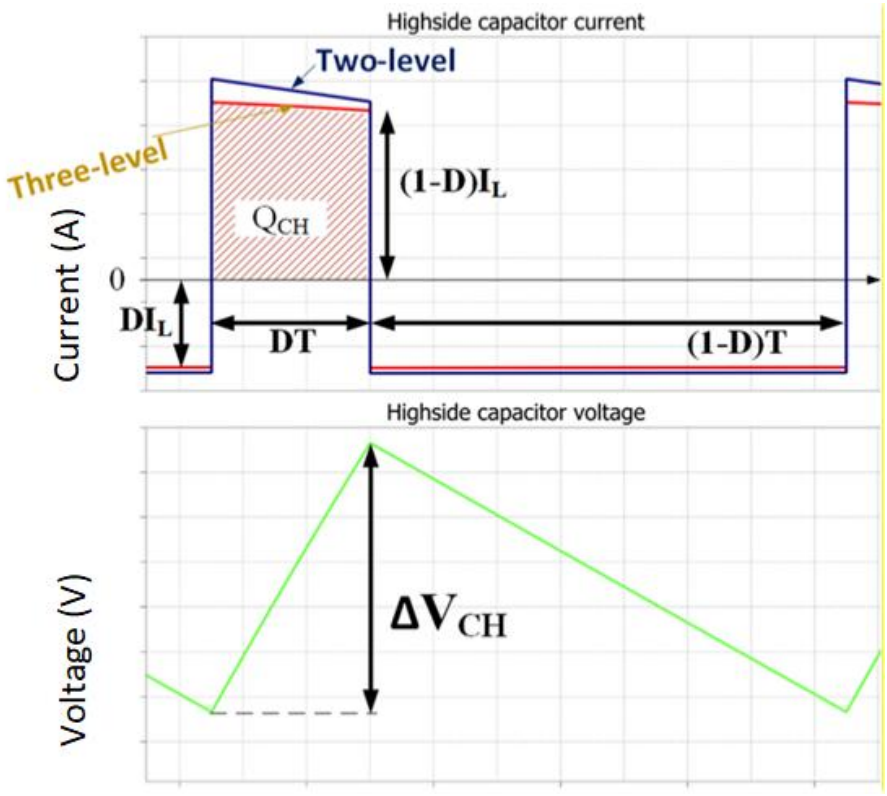


Figure 4.7 Highside side capacitor steady state ripple current of two-level and three-level converter.

$$|\Delta Q_H| = C_H \cdot \Delta V_{dc} = (1 - D)D \times T \times I_L \tag{4.6}$$

4.1.2 Three-level interleaved DC/DC converter

This section gives justification the use of the three-level interleaved DC/DC converter (Figure 4.8) which combines the benefit of interleaving technique and multilevel topology.

Interleaved DC/DC converters is a technique aimed at reducing the total current ripple seen by the load, although the individual inductor current ripples may be larger. During steady-state operation of two-level DC/DC converter, individual phases activate at intervals spaced 360°/N apart throughout the switching period, where N represents the total number of phases. by having multiple phases that operate phase-shifted with each other, effectively cancelling out a significant part of the ripple that would be present in a single-phase system. On the other side, a flying capacitor three-level DC/DC converter topology exhibit superior ripple cancellation compared to two-level converter due to switching frequency is multiplied by two on the switching node. Whilst, by maintaining flying capacitor

voltage to half of DC link, the volt-seconds across voltage ripple seen across the inductor is also reduced by half. This combination gives one ripple current reduction compared to two-level level DC/DC converter for the same inductor size and frequency as discussed in the previous section [97].

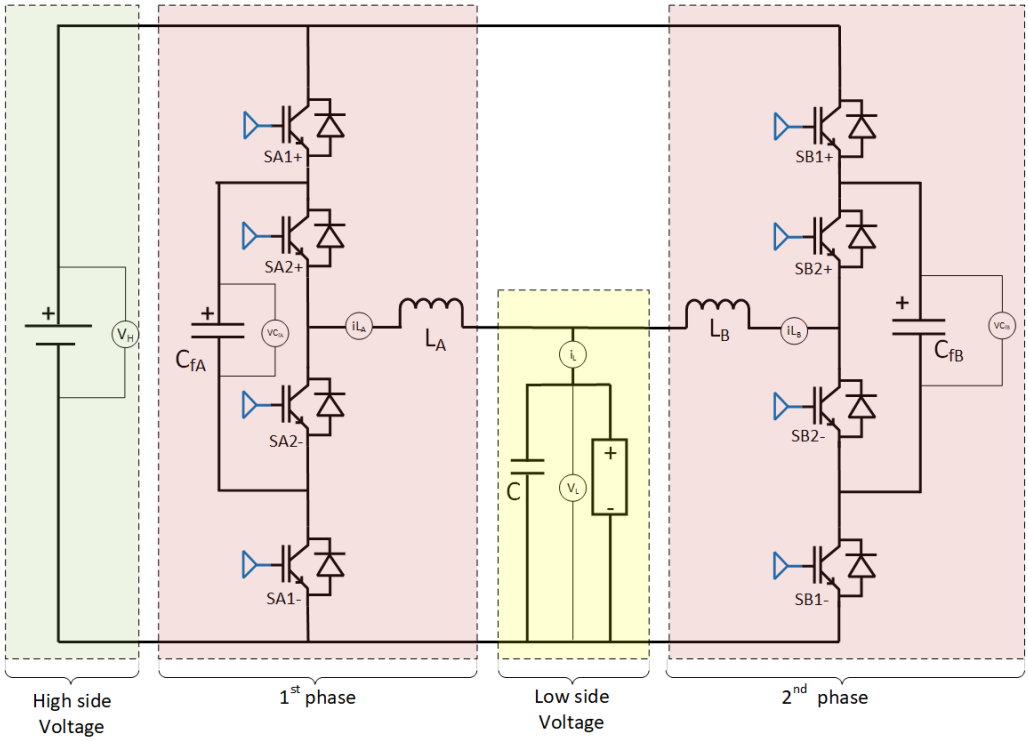


Figure 4.8 Bidirectional Three-Level Interleaved DC/DC Converter

Integrating both concepts of three-voltage level and the interleaved configurations with the total current ripple reduction is derived as expressed in Equation (4.7). This condition can be achieved when the carrier signals are shifted by 180/N degree (N is 2 for three-level two phase interleaved). This phase shift provides maximum ripple cancellation between phases, unlike the 360°/N shift typically used in conventional two-level interleaved DC–DC converters. Figure 4.9 show the expected current ripple reduction for three-level interleaved converter.

$$\Delta I_{L\ three-level\ interleaved} = \frac{V_{dc}(4D-m)(1-(4D-m))}{8\,L\,f_s}$$

With $m = integer\ of\ (4 \times D)$ (4.7)

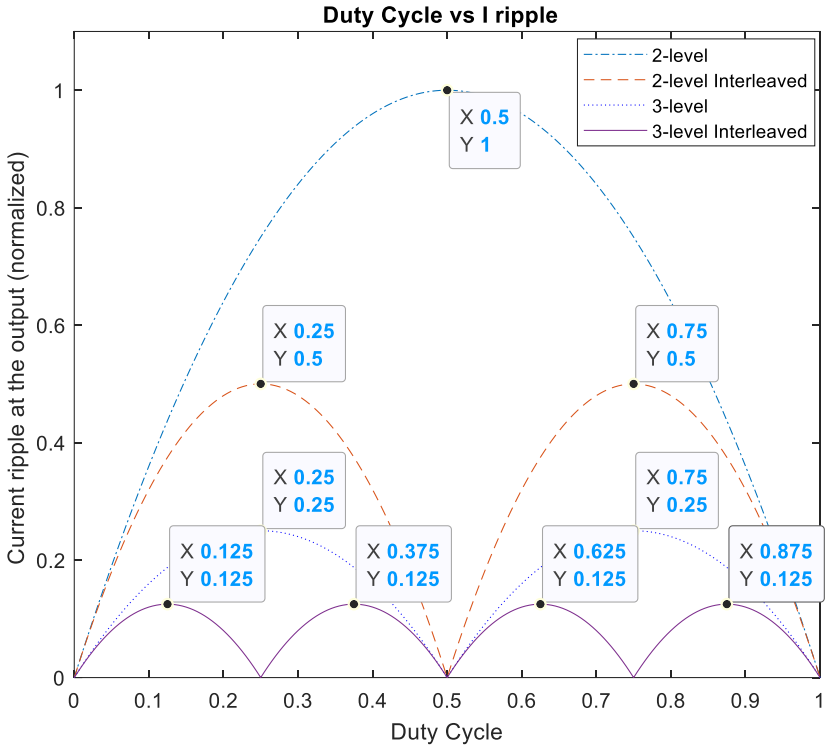
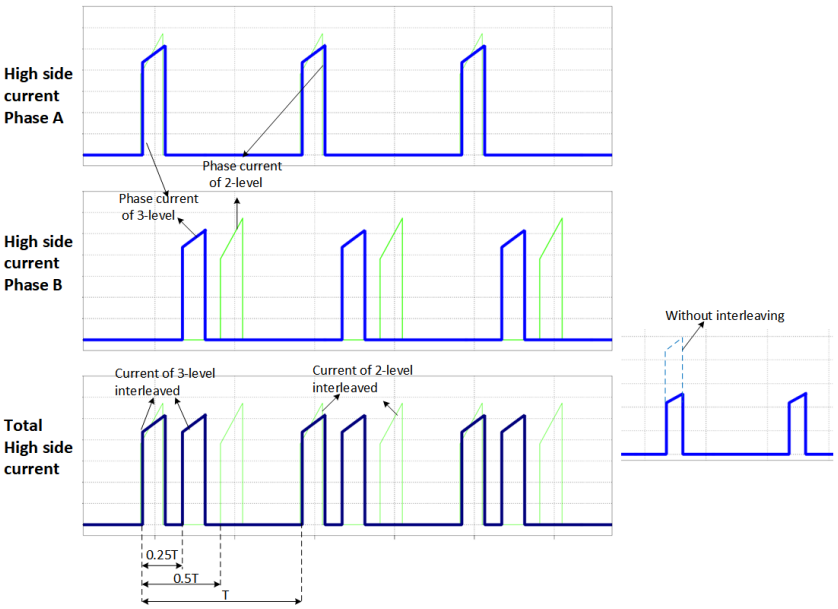
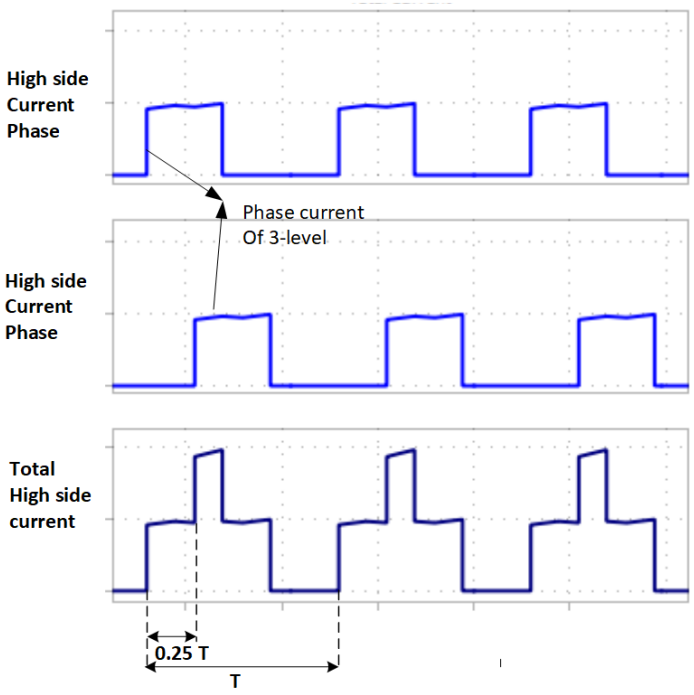


Figure 4.9 Normalized current ripple comparison on inductor between single phase and 2 phase interleaved of 2-level and 3 level DC/DC converter

Adding additional phases to a design will decrease the RMS current flowing through the decoupling capacitors as depicted in Figure 4.10, therefore reducing the ripple voltage. Consequently, lower size capacitors are needed to maintain voltage ripple within specified limits. This also mitigates self-heating effects within the capacitors caused by equivalent series resistance (ESR). However, B3LI DC/DC converter generally has higher voltage ripple compared to two-level interleaved DC/DC converter at the higher side voltage particularly when duty cycle between $0.25< D<0.75$.


High side current Phase A
Phase current of 2-level
Phase current of 3-level
High side current Phase B
Without interleaving
Current of 3-level interleaved
Current of 2-level interleaved
Total High side current
0.25T
0.5T
T

(a)


High side Current Phase
Phase current Of 3-level
High side Current Phase
Total High side current
0.25 T
T

(b)

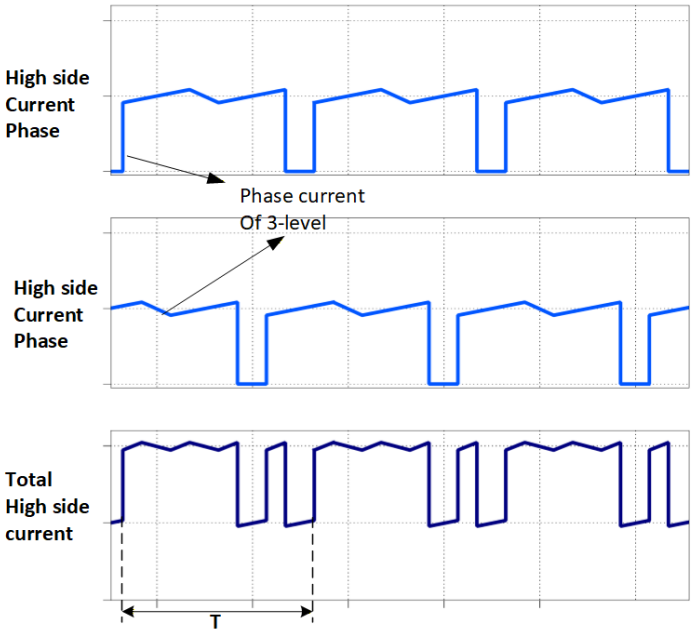


Figure 4.10 (a) Current ripple on high side of B3LI DC/DC converter D< 0.25 (b) 0.25< D<0.75 (c) D>0.75

The trade-off of interleaved converters that share a common DC link, it can develop circulating currents between phases. These currents do not deliver output power but increase RMS device stress and losses. To analyse ripple and circulation, the two-phase interleaved legs can be represented in form of a three-node network as seen in Figure 4.11.

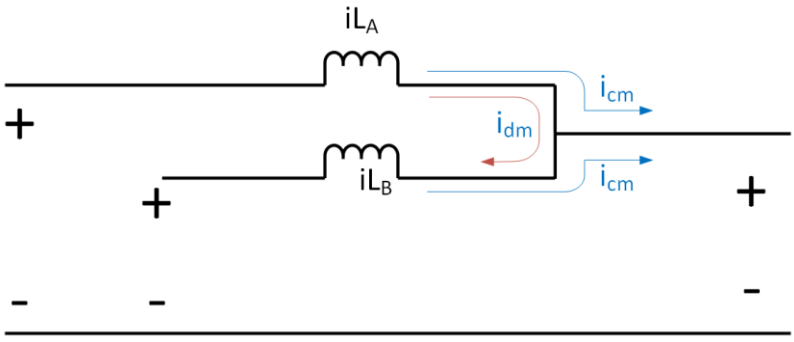


Figure 4.11 Interleaved current flow

The inductors current can be decomposed into common-mode (CM) and differential-mode (DM) components. The CM current carries useful power to the load, whereas the DM current represents circulating components between phases.

$$iL_A = i_{cm} + i_{dm} \quad \text{and} \quad iL_B = i_{cm} - i_{dm} \tag{4.8}$$

Therefore,

$$i_{cm} = \frac{iL_A + iL_B}{2} \quad \text{and} \quad i_{dm} = \frac{iL_A - iL_B}{2} \tag{4.9}$$

Inverse-coupled inductor is used to reduce the undesired the per-phase ripple and circulating currents inherent in interleaved common-DC-link operation. The implementation is discussed next section**.**

4.1.3 Three-level interleaved DC/DC converter with coupled inductor

An interleaved converter is capable of producing a lower output ripple compared to a single-phase converter. The downside of the interleaved is that each phase still carries a larger ripple fraction relative to its own inductance value. The interleaved technique with coupled inductor structure lessen this issue with the reduced channel ripple [98].

Interleaved converters with coupled inductors are commonly utilized to distribute load current in high-power applications. Similar to the interleaved converters with individual channel inductors [99], [100]. It provides an output current ripple reduction potential whilst allowing for the use of smaller magnetic components. Furthermore, an interleaved converter with coupled inductor allows reduced phase current ripple for same output ripple [98], [101]. Together with multilevel structure, a compact design with a better performance either in phase or output can be achieved.

The coupled inductor model is represented by an ideal transformer with a 1:1 turns ratio, leakage inductance in each phase (L_{kA}, L_{kB}) and mutual inductance (M). The relationship of self-inductance, mutual inductance and leakage inductance represented by Equation (4.10), (4.11) and (4.12). When the coupling coefficient k is equal to 1 (unity), which mean the flux of one coil cuts all of the turns of the second coil, that is the two coils are perfectly coupled.

$$L_{kA} = L_A - \frac{M^2}{L_B} \text{ and } L_{kB} = L_B - \frac{M^2}{L_A} \tag{4.10}$$

$$k = \sqrt{1 - \frac{L_{kA}}{L_B}} = \sqrt{1 - \frac{L_{kB}}{L_A}} \tag{4.11}$$

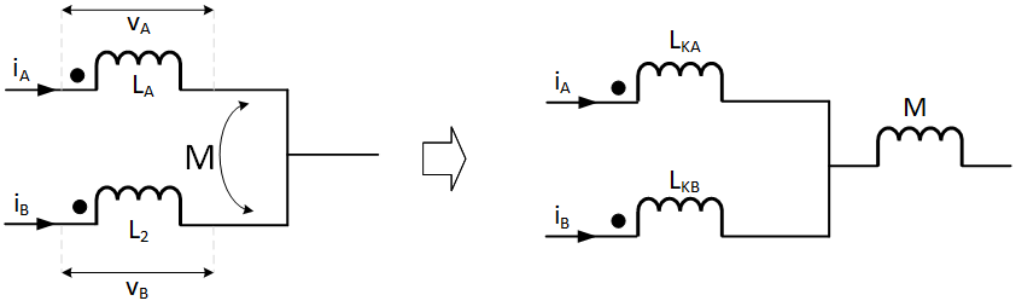
$$M = k\sqrt{L_A L_B} \tag{4.12}$$

Where, L_{kA} *or* L_{kB} = leakage inductance

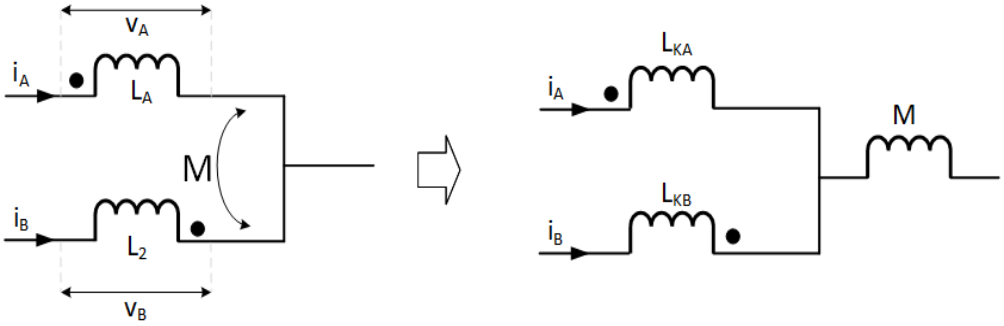
M = mutual inductance

L_A or L_B = self inductance on leg A and B

Two inductors can be coupled either in a direct or inverse direction, The coupling arrangement is identified with dot sign in the circuits [101]. The inverse direction coupling means that the dotted terminals are connected such that the magnetic flux generated by one winding's current opposes the flux generated by the other winding's current. This is crucial for cancellation effect.



(a)



(b)

Figure 4.12 Coupled inductor model (a) Direct coupling (b) Inverse coupling

The voltage across inductor v_A and v_B for direct coupling can be characterized by two sets of identical formulas:

$$v_A = L_A \frac{di_A}{dt} + M \frac{di_B}{dt} \tag{4.13}$$

$$v_B = L_B \frac{di_B}{dt} + M \frac{di_A}{dt} \tag{4.14}$$

While for inverse coupling

$$v_A = L_A \frac{di_A}{dt} - M \frac{di_B}{dt} \tag{4.15}$$

$$v_B = L_B \frac{di_B}{dt} - M \frac{di_A}{dt} \tag{4.16}$$

if $L_A = L_B = L$ and $\alpha = \frac{M}{L}$

The current change for direct coupling inductor ,

$$\frac{di_A}{dt} = \frac{v_A + \alpha\, v_B}{(1+\alpha^2)L} \tag{4.17}$$

$$\frac{di_B}{dt} = \frac{v_B + \alpha\, v_A}{(1+\alpha^2)L} \tag{4.18}$$

And an inverse coupling inductor used

$$\frac{di_A}{dt} = \frac{v_A - \alpha\, v_B}{(1-\alpha^2)L} \tag{4.19}$$

$$\frac{di_B}{dt} = \frac{v_B - \alpha\, v_A}{(1-\alpha^2)L} \tag{4.20}$$

Figure 4.13. shows the comparison of different topologies of the DC/DC converters which are previously discussed. The current ripple equation and their graphical comparison representations is implemented using MATLAB. The peak-to-peak ripple current depends on frequency and inductance. The higher the switching frequency and the inductance, the smaller ripple current.

The following section of this chapter will discuss further into the operation of the three-level interleaved DC/DC converter.

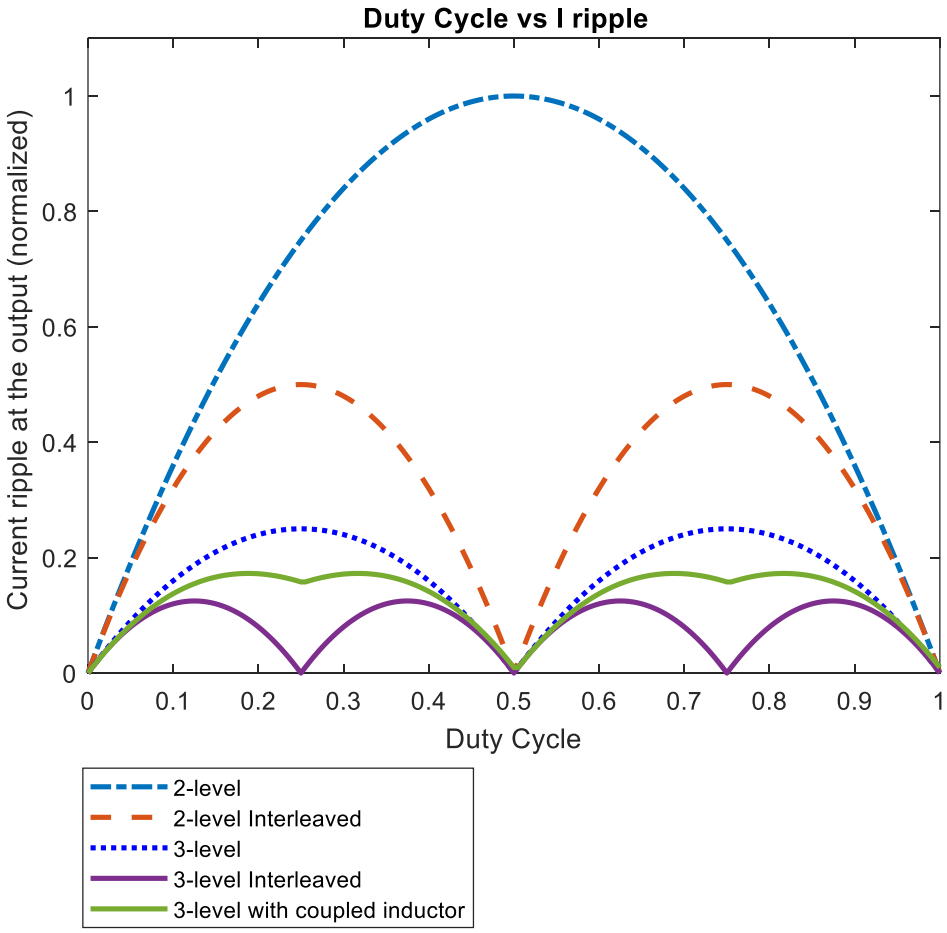


Figure 4.13 Duty cycle vs normalised ripple current to maximum value of single-phase for the converter topologies under comparison.

4.2 Operation of Bidirectional Three-Level Interleaved DC/DC Converter

The Bidirectional Three-Level Interleaved (B3LI) DC/DC converter with coupled inductor, as depicted in Figure 4.13, comprises of two branches/legs of three-level flying capacitor converters. There are four switches that operate on each branch (SA1+, SA1-, SA2+, SA2- for leg A, and SB1+, SB1-, SB2+, SB2- for leg B. The inclusion of positive (+) and negative (-) polarities in the switch designator reveals the complementary of the actions of these switch. The numbers used in the switch labels "1" and "2" denote the switch signal shifting, while the upper case letter identifiers "A" and "B" highlight the respective

converter leg. V_{dc} represents the high-voltage (DC bus) side, whereas V_L indicates the low-voltage (load/battery) side. The flying capacitors (Cf_A and Cf_B) are interconnected between the upper and lower switches.

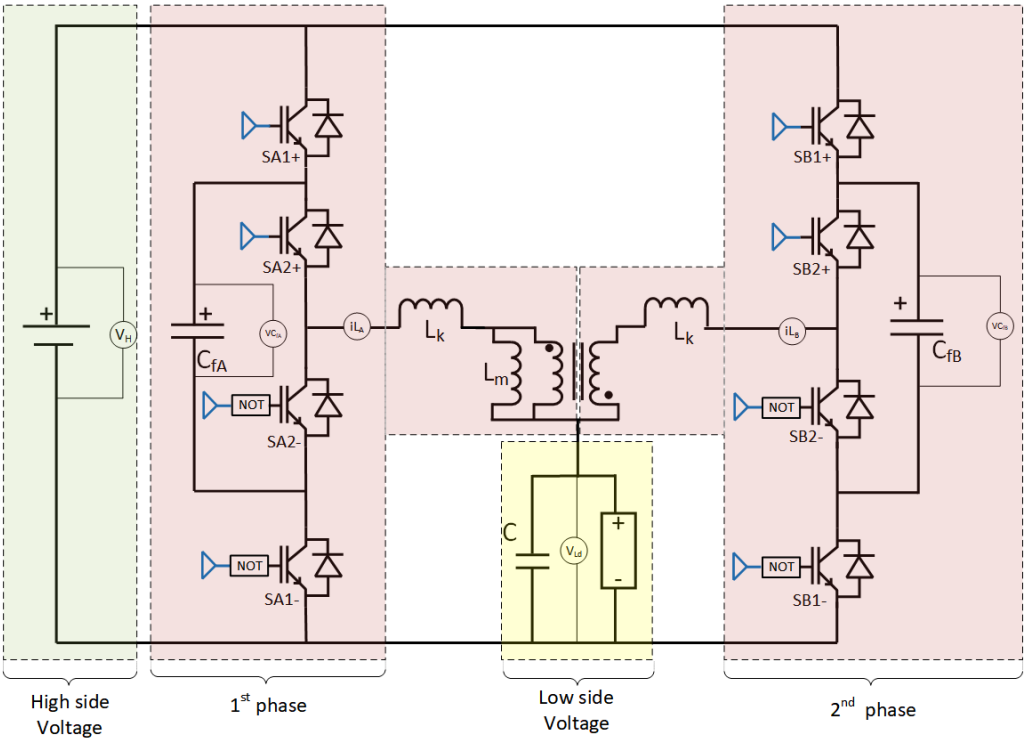
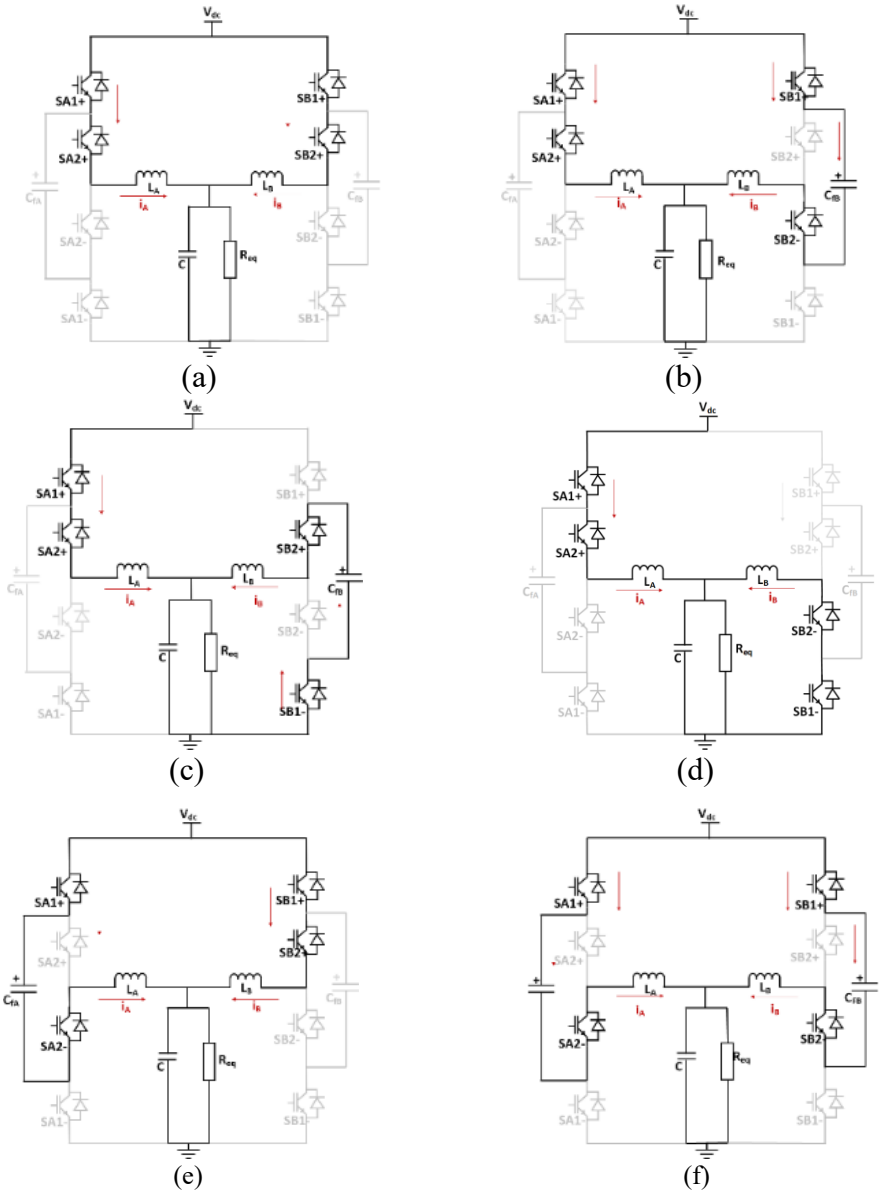


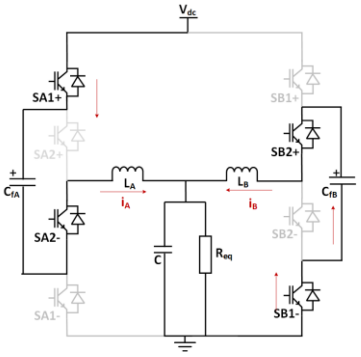
Figure 4.14 Schematic of the bidirectional three-level interleaved (B3LI) DC/DC converter with coupled inductor

The B3LI DC/DC converter provides bidirectional power flow operation, three voltage level capability and paralleled interleaving for minimising load current ripple when sharing the load current. The bidirectional feature facilitates power flow in both directions. This feature is essential for charging and discharging the battery of an electric vehicle [102]. This section discusses the operation of B3LI DC/DC converter either uses coupled or discrete inductors.

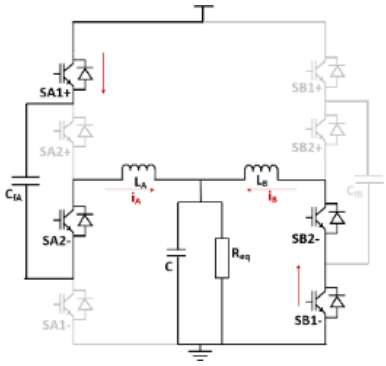
Figure 4.15 (a) to (p) details all switching configuration of the B3LI converter. Even though the converter encompasses of a combination of total of sixteen allowable states, each branch only experiences four stages as explained previously explained in section 4.1.1. The first stage is the direct energization of the inductor from the input source via S1+ and S2+ while the flying capacitor C_f is bypassed. During the second stage is the charging of the capacitor coupled with the energization of the inductor. During the third stage, the capacitor

disengages from source and is discharging while the inductor relinquishes its stored energy. The fourth stage signifying inductor de-energization while source and capacitor are disconnected. Throughout the period the switch node alternates its voltage at rate 0, $V_{dc}/2$ and V_{dc}. The stage depends on the duty cycle of the converter. This principle applied to the other branch of the converter with delay one-fourth of the cycle time.

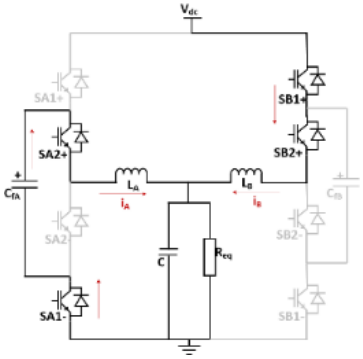



Vdc
SA1+
SB1+
SA2+
SB2+
CfA
LA
LB
iA
iB
CfB
SA2-
C
Req
SB2-
SA1-
SB1-

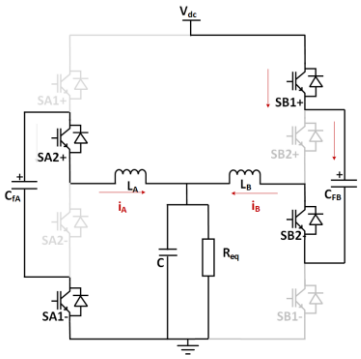
(g)


SA1+
SB1+
SA2+
SB2+
CfA
LA
LB
iA
iB
CfB
SA2-
C
Req
SB2-
SA1-
SB1-

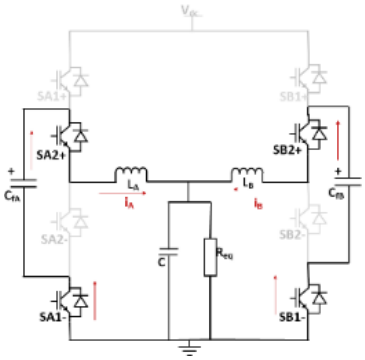
(h)


Vdc
SA1+
SB1+
SA2+
SB2+
CfA
LA
LB
iA
iB
CfB
SA2-
C
Req
SB2-
SA1-
SB1-

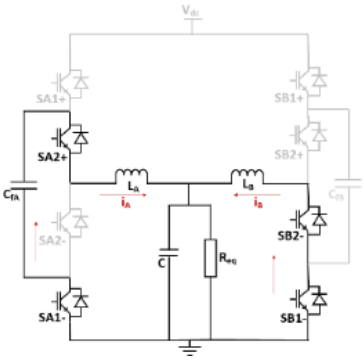
(i)


Vdc
SA1+
SB1+
SA2+
SB2+
CfA
LA
LB
iA
iB
CfB
SA2-
C
Req
SB2-
SA1-
SB1-

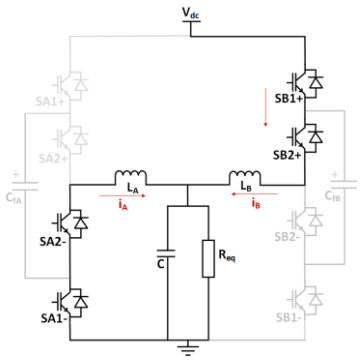
(j)


Vdc
SA1+
SB1+
SA2+
SB2+
CfA
LA
LB
iA
iB
CfB
SA2-
C
Req
SB2-
SA1-
SB1-

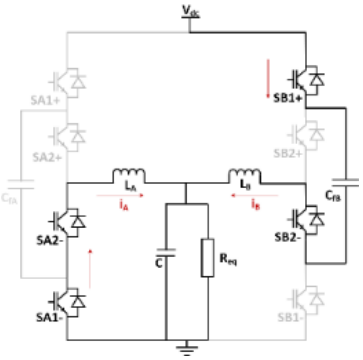
(k)


Vdc
SA1+
SB1+
SA2+
SB2+
CfA
LA
LB
iA
iB
CfB
SA2-
C
Req
SB2-
SA1-
SB1-

(l)


Vdc
SA1+
SB1+
SA2+
SB2+
CfA
LA
LB
iA
iB
CfB
SA2-
C
Req
SB2-
SA1-
SB1-

(m)


Vdc
SA1+
SB1+
SA2+
SB2+
CfA
LA
LB
iA
iB
CfB
SA2-
C
Req
SB2-
SA1-
SB1-

(n)

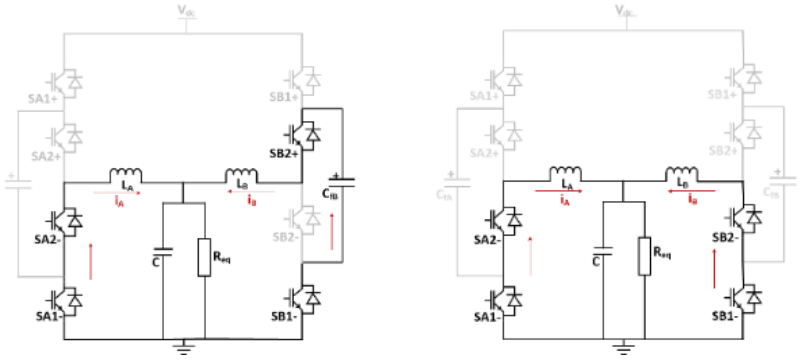
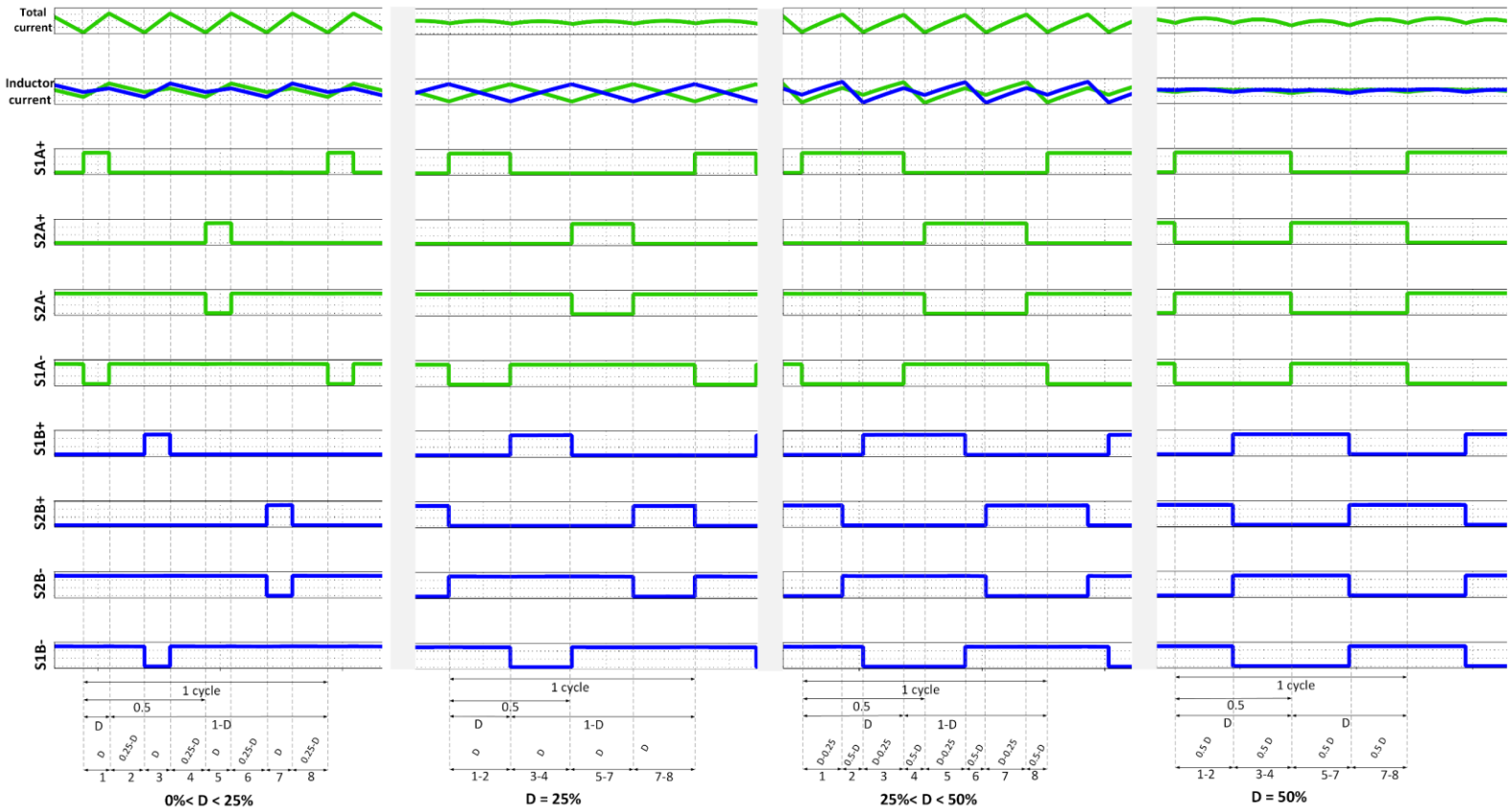


Figure 4.15 Operation states of Bidirectional 3-Level Interleaved DC/DC Converter (a)1111, (b)1110, (c)1101, (d)1100, (e)1011, (f)1010, (g)1001, (h)1000, (i)0111, (j)0110, (k)0101, (l)0100, (m)0011, (n)0010, (o)0001, (p)0000.

Figure 4.16. illustrates the seven particular situations relevant for the operation of the B3LI converter when the voltage transfer ratio, VTR< 0.25, =0.25, 0.25< VTR <0.5, VTR=0.5, 0.5<VTR > 0.75, VTR=0.75 and VTR >0.75. The signal switch shifting on respective leg is 180^{o}, therefore, frequency of current ripple in the inductor is twice of switching frequency. Because of ripple frequency has been doubled, leg B is delayed by 90^{o} than leg A, therefore the minimum ripple current on inductor is achieved.


Total current
Inductor current
S1A+
S2A+
S2A-
S1A-
S1B+
S2B+
S2B-
S1B-
1 cycle
0.5
D
1-D
0%< D < 25%
D = 25%
25%< D < 50%
D = 50%

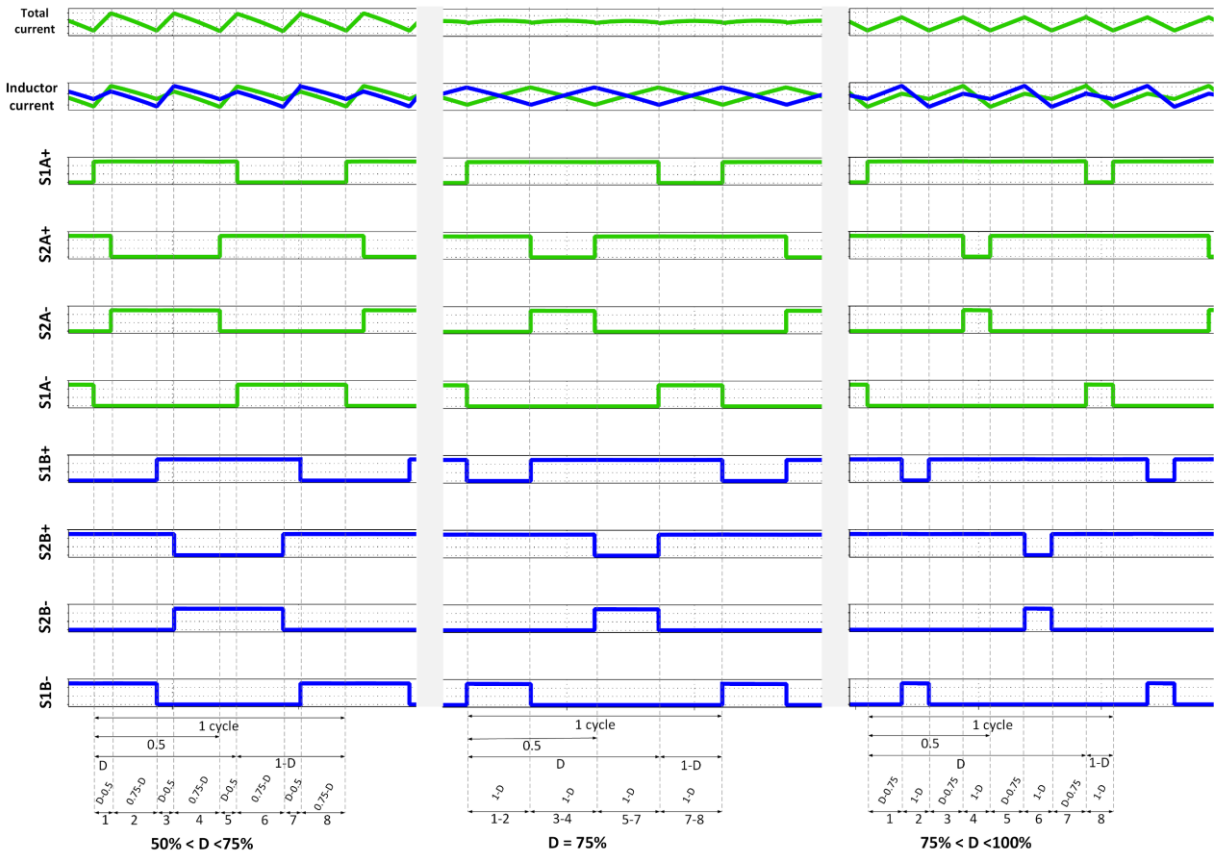


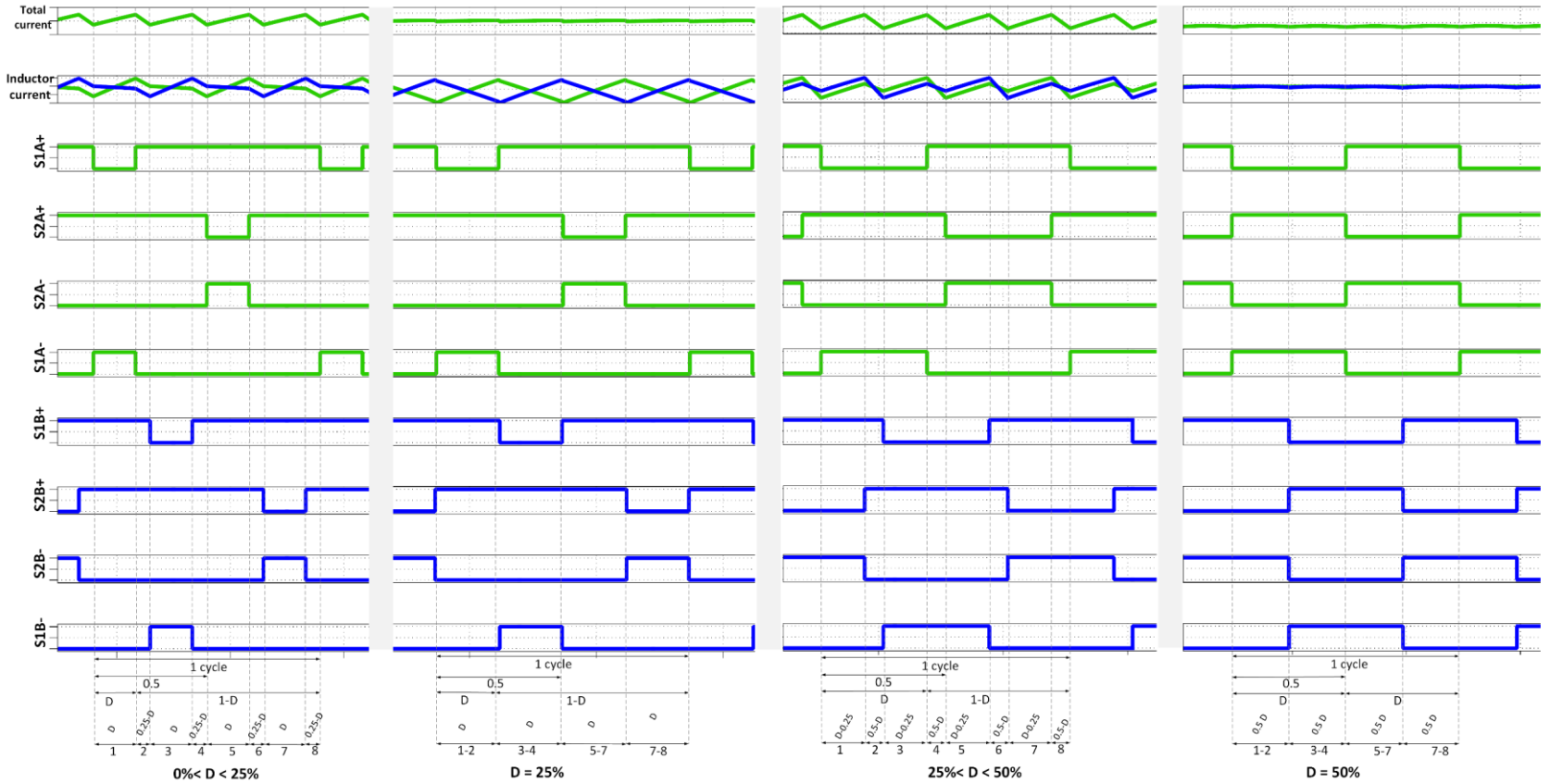
Figure 4.16 Inductor current flow analysis for different duty cycles for battery charging operation (power flow is from DC bus to battery)

The table 4.1 represent switching sequence of the switch S1A+,S2A+, S1B+ and S2B+ respectively when given specific duty cycle during buck operation that has been shown in Figure 4.4.

Table. 4.1 Switching sequence depending on voltage transfer ratio.

Voltage transfer ratio	Switching state (SA1+, SA2+, SB1+, and SB2+)							
	1	2	3	4	5	6	7	8
0-25%	1000	0000	0010	0000	0100	0000	0001	0000
25%	1000	1000	0010	0010	0100	0100	0001	0001
25-50%	1001	1000	1010	0010	0110	0100	0101	0001
50%	1001	1001	1010	1010	0110	0110	0101	0101
50%-75%	1101	1001	1011	1010	1110	0110	0111	0101
75%	1101	1101	1011	1011	1110	1110	0111	0111
75-100%	1111	1101	1111	1011	1111	1110	1111	0111

During boost operation, the current flows in the opposite direction. The switching sequence in table 4.1. can also be used but the duty cycle of the signal is represented by S1A-, S2A-, S1B- and S2B- respectively as illustrated in figure 4.5.


Total current
Inductor current
S1A+
S2A+
S2A-
S1A-
S1B+
S2B+
S2B-
S1B-
1 cycle
0.5
D
1-D
0%< D < 25%
D = 25%
25%< D < 50%
D = 50%

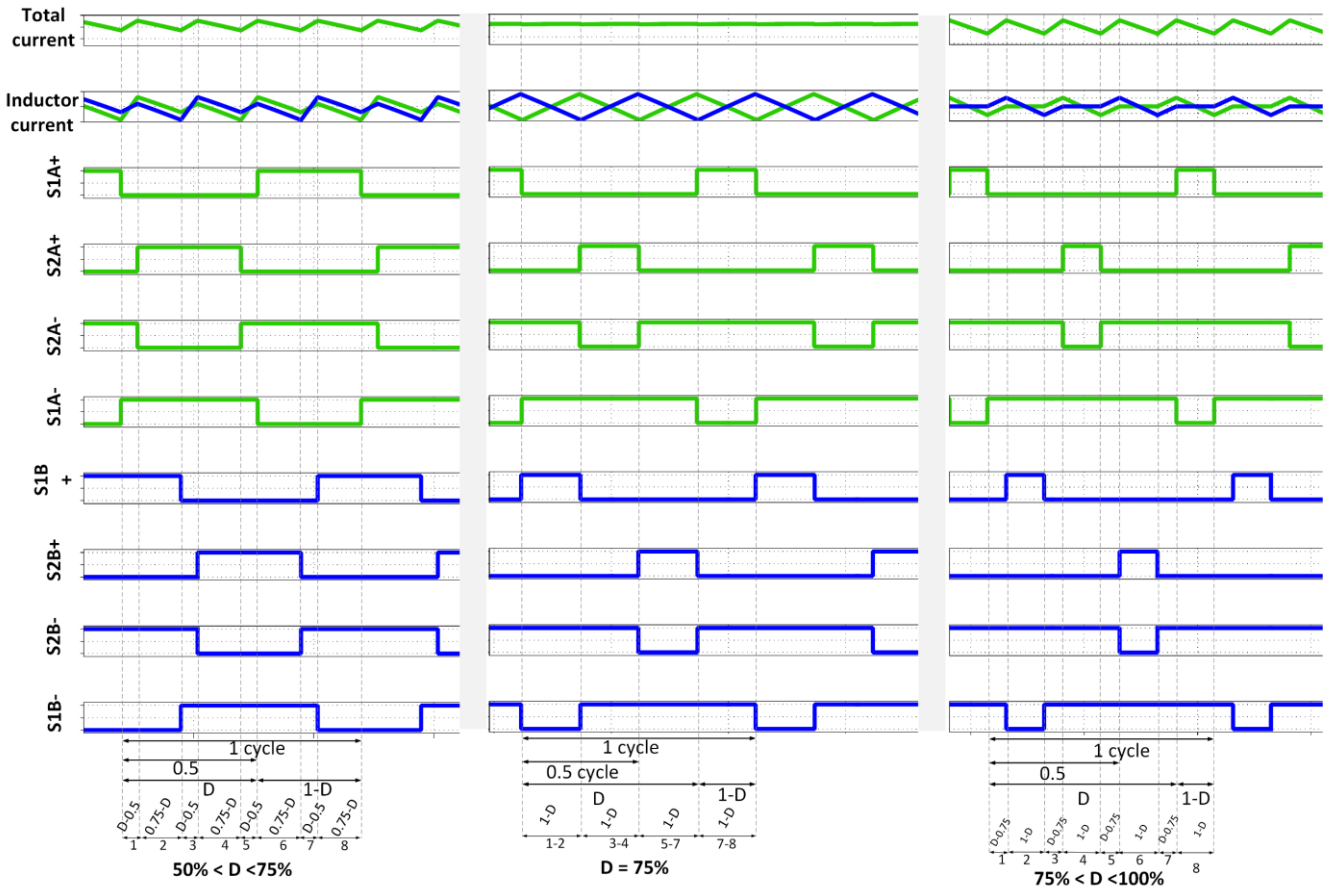


Figure 4.17 Converter operation at different voltage transfer ratios

4.3 Mathematical Model of the Three-Level Interleaved DC/DC converter

The dynamic model for B3LI converters can be formulated through the utilization of the state-space average technique. The following description of the state-space average technique is based on deriving the generalized equations for converter under investigation operating in continuous conduction mode and omitting the processes associated with the charging and discharging of the output filtering capacitors. As previously mentioned, the B3LI DC/DC converter experiences 16 switching states which depends on the voltage transfer ratio. Due to the use of the coupled inductor, the switching state of one leg will affect the other leg.

State-space variables of the converter are defined as the set of the inductor currents I_A and I_B, and the output filtering capacitor voltage, which is also the output load voltage V_{Ld}. X is the state-space variable of output capacitor voltage and inductor currents written in a matrix configuration. The matrices A and B are the state-space matrices attributes of the converter during each state conditions. Meanwhile, Y designates the input variable of the flying capacitor voltage V_{cf} and voltage V_{dc}.

$$\dot{x} = AX + BY \tag{4.21}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{Ld}}{dt} \end{bmatrix} = \mathrm{A} \begin{bmatrix} i_A \\ i_B \\ V_{Ld} \end{bmatrix} + B \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} \tag{4.22}$$

4.3.1 *Small*-signal Modelling of B3LI Converter

The process of small signal modelling involves linearizing the non-linear elements within a converter with respect to the duty cycle, denoted by $\overline{D}$ .This method examines the effect of a small perturbation in the duty ratio, represented as d on the overall system. The ratio of the change in duty ratio, d to the original duty ratio, $\overline{D}$, is typically quite small [103], [104].

Consider the presence of a small signal variation d with respect to the duty ratio D, which will result in a corresponding small variation x of the state variable X.

Appendix 3.1 and 4.1 present the detailed derivation for the converter during buck mode operation. This section systematically develops the mathematical representation of the system by defining the relevant state variables and formulating their differential equations based on the circuit's switching configuration. The resulting state-space model is used for analyzing the dynamic behavior of the converter under buck operation.

$$\frac{\dot{x}}{d} = \frac{\begin{bmatrix} \frac{V_{dc}}{\Sigma Lx}(s + \frac{1}{R\,C}) \\ \frac{V_{dc}}{\Sigma Lx}\left(s + \frac{1}{R\,C}\right) \\ \frac{2V_H}{C\,\Sigma Lx} \end{bmatrix}}{s^2 + s\frac{1}{R\,C} + \frac{2}{\Sigma LxC}} \tag{4.23}$$

The voltage transfer function :

$$\frac{\dot{V}_{ld}}{d} = \frac{2V_{dc}}{C\,\Sigma Lx}\frac{1}{s^2 + s\frac{1}{R\,C} + \frac{2}{\Sigma LxC}} \tag{4.24}$$

If $\frac{d\mathrm{i}}{dt} = \frac{di_A}{dt} = \frac{di_B}{dt}$, the current transfer function :

$$\frac{i}{d} = \frac{V_{dc}}{\Sigma Lx}\frac{(s + \frac{1}{R\,C})}{s^2 + s\frac{1}{R\,C} + \frac{2}{\Sigma LxC}} \tag{4.25}$$

Similar steps for the operation of the converter when 0.25 <D <0.5, 0.5 <D< 0.75 and 0.75<D<1 as can be seen in Appendix 3.1. They follow voltage balancing process, although they have different sequences during its operation.

In the case of discrete inductor instead of coupled being used, the inductor variable ΣLx is equal to inductor value because there is no magnetizing effect from the other inductor from another phase

The voltage and current transfer function of B3LI DC/DC Converter are second order transfer functions in the s-domain. The system possesses two left-half plane conjugate poles, indicating stability with an oscillatory response.

Additionally, it features one left-half-plane zero in the current transfer function, necessitating further design considerations in the control system to maintain stability in the closed-loop control of current. While, the voltage transfer function does not have zeros, implying that the control loop is stable.

While the derivation for the boost mode operation is presented in Appendix 4.2, which provides the step-by-step solution of the corresponding circuit equations.

$$\frac{\dot{x}}{d} = \frac{\begin{bmatrix} \frac{V_{dc}}{\Sigma Lx}\, s + \frac{1}{\Sigma Lx\mathrm{C}}\left(\frac{V_{dc}}{\mathrm{R}} + 2i_L(1-D)\right) \\ \frac{V_{dc}}{\Sigma Lx}\, s + \frac{1}{\Sigma Lx\mathrm{C}}\left(\frac{V_{dc}}{\mathrm{R}} + 2\, i_L(1-D)\right) \\ 2\left(\frac{V_{dc}}{\Sigma Lx}\frac{1-D}{\mathrm{C}} - s\,\frac{i_L}{\mathrm{C}}\right) \end{bmatrix}}{s^2 + \frac{1}{\mathrm{RC}}\mathrm{s} + \frac{(1-D)^2}{\Sigma Lx\, C}} \tag{4.26}$$

The above voltage transfer function can be represented in term of V_{ld} and I_L laced using the relationship as follow:

$$2I_L = \frac{I_{dc}}{1-D} = \frac{V_{dc}}{R\,(1-D)} \tag{4.27}$$

$$V_{dc} = \frac{V_{ld}}{1-D} \tag{4.28}$$

Therefore the voltage transfer function is :

$$\frac{\dot{V}_{dc}}{d} = 2\frac{V_{ld}}{RC\,(1-D)^2} \quad \frac{\left(\frac{R(1-D)}{\Sigma Lx} - s\right)}{s^2 + \frac{\mathrm{s}}{\mathrm{RC}} + \frac{(1-D)^2}{\Sigma Lx\, C}} \tag{4.29}$$

And the current transfer function is:

$$\frac{\dot{i}}{d} = \frac{V_{ld}}{\Sigma Lx(1-D)} \frac{s + \frac{2}{\mathrm{RC}}}{s^2 + \frac{\mathrm{s}}{\mathrm{RC}}\mathrm{s} + \frac{(1-D)^2}{\Sigma Lx\, C}} \tag{4.30}$$

The boost operation exhibits a second-order dynamic behavior characterized by two left-half plane (LHP) conjugate poles. Its output voltage transfer function in Equation (4.29), however, contains a right-half plane (RHP) zero, which introduces non-minimum phase behaviour. The presence of the RHP zero

complicates the implementation of a straightforward voltage feedback control. To improve system stability and dynamic performance, an inner current control loop is can be integrated into the boost converter control structure.

Knowing the transfer function of B3LI converter offer advantages, particularly in the design, control, and optimisation of converter performance. A primary benefit of comprehending the transfer function is its application in stability analysis. For instance, utilising Bode plots enables the determination of phase margin and gain margin, which indicate the system's resilience against instability. Furthermore, this allows for the design of appropriate compensators (such as PI controllers) that ensure the system tracks the desired output.

Although small-signal analysis serves as a valuable tool, and phase and gain margins provide useful metrics for assessing the local stability of a linearized model around a given operating point, they do not ensure global stability of the original nonlinear system. This limitation stems from the fact that the linearized model remains valid only for small perturbations near the operating point and fails to capture nonlinear phenomena.

4.4 Summary

The operation of the B3LI DC/DC converter is presented in this chapter. The B3LI converter features bidirectional power flow, three voltage levels, and interleaving to ensure equal distribution of voltage and load current, as well as to further reduce current ripple. There are total of 16 available switching states for the two-leg interleaved converter. For a specific voltage transfer ratio, whether in buck or boost operation, only 8 switching states are employed in the switching sequence of each cycle. The flying-capacitor three-level DC–DC converter offers superior ripple cancellation compared to a conventional two-level converter, as the effective switching frequency at the switching node is doubled. Additionally, by maintaining the flying-capacitor voltage at half of the DC-link voltage, the volt-seconds contributing to inductor ripple are halved. Collectively, these effects result in a significant reduction in inductor current ripple. In addition, this chapter examines the application of a coupled inductor.

A complete small signal analysis has been developed to mathematically characterise the converter. The state space average technique was utilized for obtaining the state matrix, which is used in the small signal model. The validation of the small signal model is examine the next chapter.

Chapter 5

Control Technique and Simulation of Bidirectional Three-Level Interleaved DC/DC converter

A Bidirectional Three-Level Interleaved (B3LI) DC/DC converter is proposed for Electric Vehicle (EV) battery charging. This topology has the capability to work in a wide range of battery voltages and support bidirectional power transfer with high efficiency for EV applications having also vehicle to vehicle (V2V) and vehicle to grid (V2G) capabilities. This chapter will discuss firstly, the control technique for the B3LI DC/DC converter. The proposed controller aims to enhance the converter's performance under variation of input and load voltage whilst ensuring stable operation. Then, passive component sizing and the controller parameters are calculated. Finally, a detailed simulation study is performed to validate the design and show the effectiveness of the proposed control techniques in allowing the converter to operate in bidirectional mode within a wide range of voltage ratios.

5.1 B3LI component sizing and parameter

The proposed specification of interleaved three-level flying-capacitor DC–DC converter is designed to operate at a nominal rated power of 60 kW, delivering up to 100 A of output current (50 A per phase). The converter interfaces with a high-voltage DC link rated at 800 V, which may originate from a photovoltaic array or DC grid. On the load side, the converter is required to accommodate a wide voltage range of 200 V to 600 V, enabling flexible operation with various electric-vehicle battery systems. This wide voltage conversion capability ensures compatibility with both 400 V and 800 V architecture EV platforms.

5.1.1 Flying capacitor sizing

The flying capacitor is charged and discharged by keeping its average voltage at around half of the high DC-bus voltage V_{dc} with a peak-to peak ripple of ΔV_{cf} as defined in Equation (5.1). ΔV_{cf} is limited by design to be less than 10% of $V_{dc}/2$ to avoid overmodulation and maintain control loop stability. A full modulation index range operation is shown in Figure 5.4 showing that the flying capacitor voltage ripple ΔV_{cf}, peaks at $D_{A/B}$ = 0.5 which is the worst case operating point, as it maximizes voltage ripple, it imposes the highest current stress on the capacitor and challenges charge-balancing mechanisms. At this point however, the converter behaves as a switched capacitor converter because the ripple current in the output inductor is almost zero which means it is the best case operating point for the inductor. At this point, the AC losses in inductor is minimum therefore it can attain the maximum current flow before it reaches saturation.

$$\Delta V_{cf} = \frac{i\,((\,0.5 - \,|\,D_{A/B} - 0.5|)}{C_f\, f_s} \tag{5.1}$$

Figure 5.1 shows the flying capacitor voltage ripple during full modulation index range. Deriving from Equation (5.1) and as depicted in Figure 5.1, for worst case operating point, the sizing of the flying capacitor value (Cf) is determined by imposing the maximum voltage ripple, ΔV_{cf} at $D_{A/B}$=0.5 as in Equation (5.2).

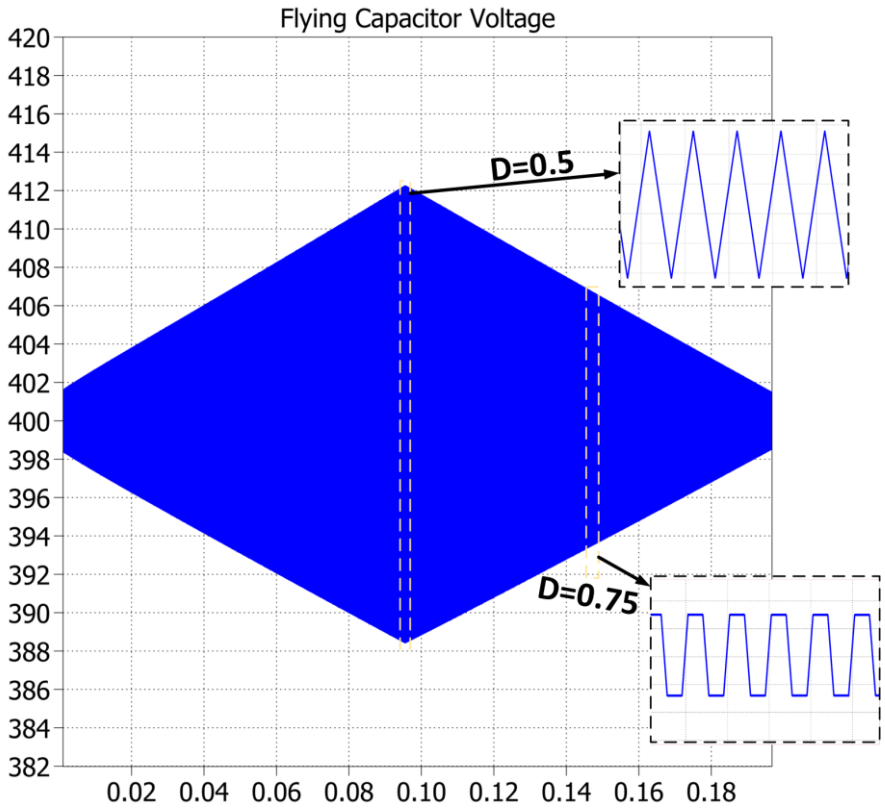


Figure 5.1 Flying capacitor voltage during full modulation index range operation

$$C_{f-min} = {}^{1}/_{2} \frac{i}{\Delta V_{cf-\max} f_s} \tag{5.2}$$

In the simulation, the flying capacitor (C_f) operational voltage is 400 V, expected maximum voltage ripple is 40 V. Therefore with 50 A inductor current (i) and 10kHz switching frequency (f_s), the minimum size of flying capacitor is 62.5 µF. In the simulation 100 µF is selected. Therefore, the expected ripple voltage, ΔV_{cf} is 25 V.

Figure 5.2 simulates the situation where flying capacitor is connected to input on charging cycle and discharging in the opposite switching state when it is connected to the load which is causes incremental rise and fall of the capacitor voltage. There is also a situation where the flying capacitor is disconnected from the circuit so that no changes take place in the capacitor voltage.

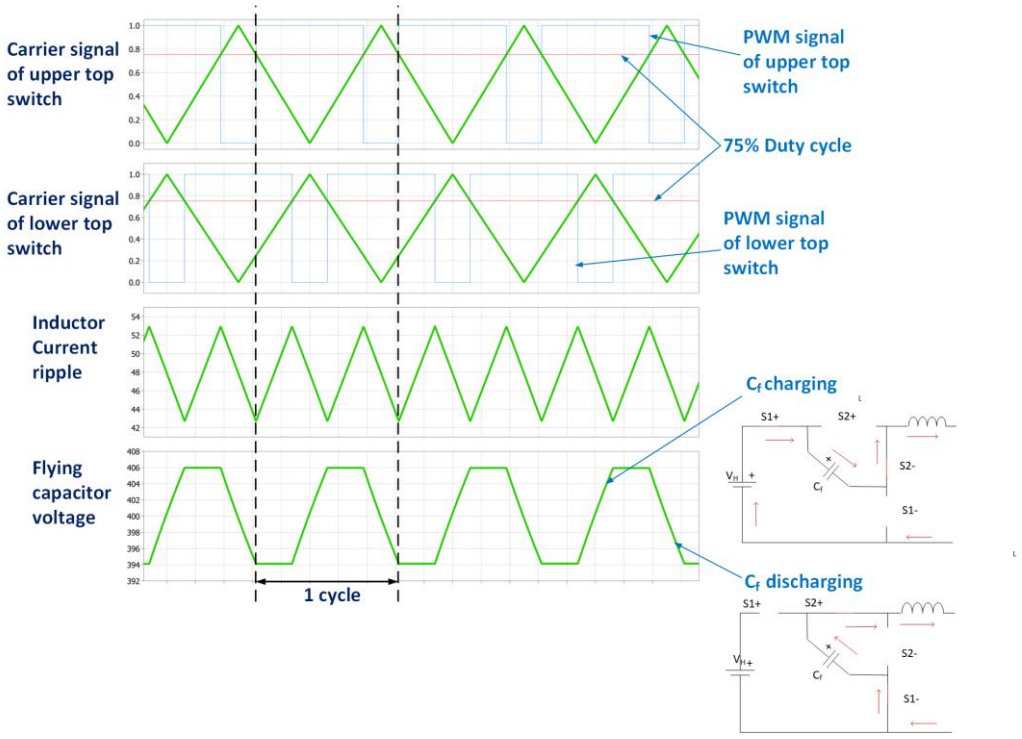


Figure 5.2 Three level operation of the flying capacitor converter leg

5.1.2 Inductor sizing

This inductor design approach ensures that the inductor will handle the maximum expected current, voltage, and power without exceeding its ratings at all operating point. The inductor is energized and deenergized for regulating the current level around its average reference value. During energizing the inductor, the current increases that causes a voltage drop across the inductor. When the inductor deenergizes, the inductor opposes the changes in current producing a voltage across the inductor to oppose the change in current. The frequency of inductor current ripple is twice of signal carrier frequency due to its three-level configuration as shown in Figure 5.2. Because the inductor voltage ripple at the node is only half of the DC bus and the switching frequency is double, the maximum ripple current of the three-level converter, $\Delta i_{(phase)}$, of the inductor is reduced to one-fourth compared to a conventional half bridge two level converter as given by Equation (5.3).

$$\Delta i_{(phase)} = \frac{V_{dc}(\ 0.5\ |\ D_{A/B} - 0.5|\ -\ (D_{A/B} - 0.5)^2)}{L\ f_s} \tag{5.3}$$

Therefore, the sizing of the inductor of the flying capacitor converter is given by Equation(5.4) where the maximum ripple current $\Delta i_{(phase)}$occurred which is at $D_{A/B}$ equal to 0.25 or 0.75.

$$L_{min} = \frac{0.0625\ V_H}{\Delta i_{(phase)-\max}\ f_s} \tag{5.4}$$

As an example, with the requirement 800 V of DC bus voltage V_H, 50 A rated current (i) on phase inductor, the imposed maximum ripple Δi of 10A that corresponds to a relative peak to peak ripple of 20% of inductor current, when switching at 10kHz (f_s), would result in a minimum size of the output inductor of 0.5 mH.

5.1.3 DC Bus/ High side capacitor sizing

Highside capacitor, C_H provide a path for ripple current and stabilize bus voltage during a transient event. In any voltage source converter, the DC link voltage or the high-voltage (DC bus) side, V_{dc} experiences a switching ripple because of the relatively high levels of DC side switching currents (Figure 5.3) produced by the converter legs that need to be handled by the DC bus capacitor. In this converter topology however, by using a three-level configuration and by employing interleaving of the paralleled converter legs, result in a decrease of the Root Mean Square (RMS) DC side current flowing through the decoupling capacitors as shown in Figure 5.4, which subsequently results in smaller voltage ripple on the DC bus/ high-side voltage, V_{dc}. As a result, smaller capacitors are required to maintain the switching voltage ripple within specifications. Moreover, this will reduce the self-heating effects within the capacitors caused by the DC link current ripple passing through the capacitor's Equivalent Series Resistance (ESR).

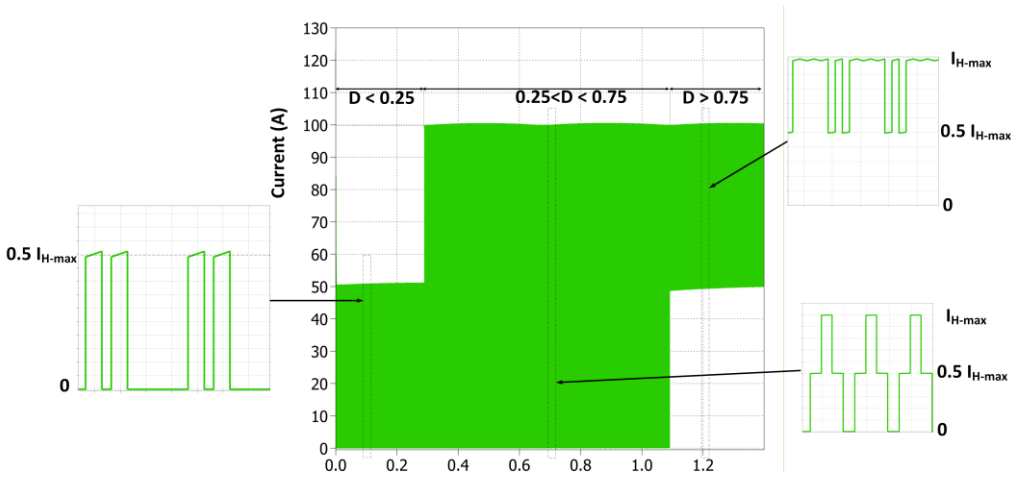


Figure 5.3 High-side current flow when duty cycle sweeps the full duty cycle range

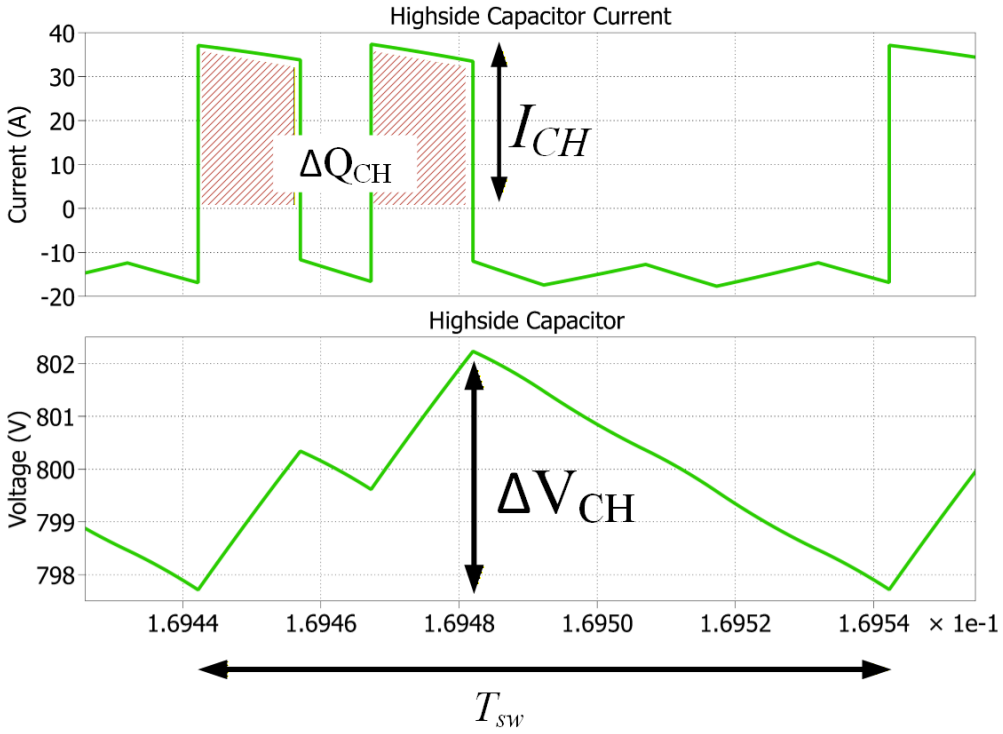


Figure 5.4 High-side capacitor current and voltage at voltage transfer ratio >75%

Subsequently, the variable charges on capacitor are as Equation (5.5) follows, and by considering the maximum ripple voltage (occurred at voltage transfer ratio equal to 0.25 and 0.75), the minimum capacitor size calculated as in Equation (5.6).

$$|\Delta Q_H| = C_H \cdot \Delta V_{dc} \tag{5.5}$$

$$C_{H-min} = \frac{0.125\, I_L\, T}{\Delta V_{dc-max}} \tag{5.6}$$

Therefore with 100 A total current delivered in load side (i_L), expected the worst voltage ripple (ΔV_{dc}) $of\ 1-2\%$ of DC bus voltage rating 800V, at 10kHz switching frequency (f_s), the size of high side voltage capacitor (C_H) is 0.15625 mF. In the simulation study that follows, a DC-link capacitor of 200µF is selected.

5.1.4 *Low*-side Capacitor sizing

The low side/ load capacitor, C_L is required to filter out voltage ripples, stabilize the output voltage. The three-level configuration on leg doubling the frequency of charging and discharging of the low side capacitors while the interleaved process generates an overall current, I_{total}, with current ripple cancellation of which the AC component is absorbed by the low-side capacitor, C_L. The advantages of these combination are the reduction of the low voltage/ load side voltage ripple of B3LI DC/DC converter. Figure 4.6 show the ideal ripple cancellation in during steady state, of the load current I_{total}, with the ripple current cancellation the overall output voltage ripple across the low-side capacitor is also minimized, thereby reducing the required capacitance size to maintain switching ripple of V_{Ld} within specification.

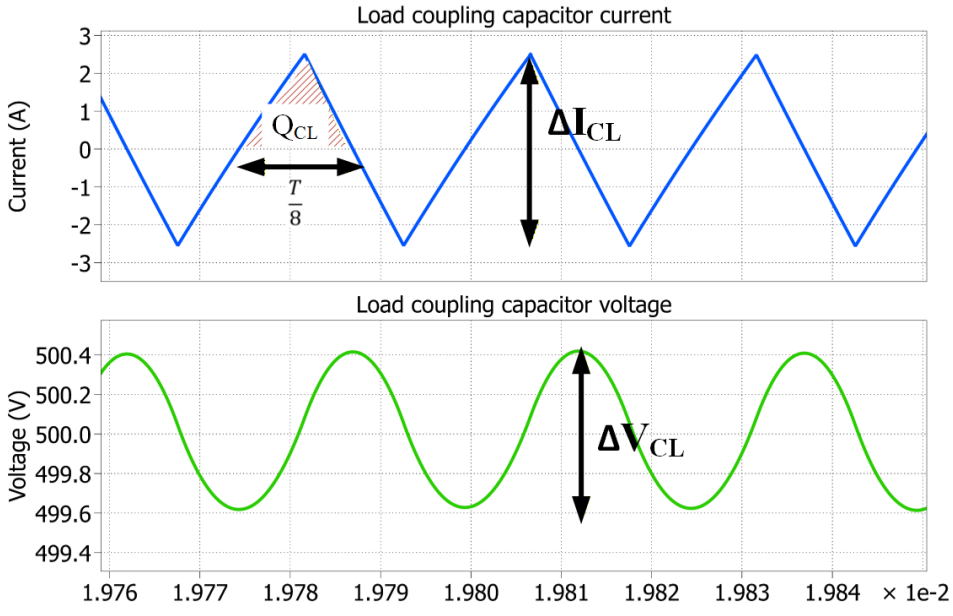


Figure 5.5. Steady state ripple current and voltage at load side capacitor

The capacitance on the low side must be appropriately sized to accommodate the current ripple. Therefore, in the worst-case scenario the low-side output capacitor is calculated based on maximum current ripple, Δi using Equation (5.7).

$$C_{L-min} = \frac{\Delta i}{16 \times f_{sw} \times \Delta V_{CL}} \tag{5.7}$$

However, when only a reduced ripple cancellation is happening, the low-side capacitance has to be sized to deal with this case, In this instance, the low-side output capacitor is calculated with consideration for single-phase operation. With $2 - 4$ V load voltage ripple, maximum 20% ripple current (Δi) in inductor, 10kHz switching frequency (f_s), the calculated size of low side voltage capacitor (C_L) is 15.63-30.13 µF. In this simulation 20 µF was selected.

Table 5.1. Component sizing

Parameters	Symbol	Value	Unit
High side voltage	V_{dc}	800	V
Low side voltage	V_{ld}	200 to 600	V
Leg inductor current	I_{phase}	up to 50	A
Switching frequency	f_s	10000	Hz
Leg Inductor	L	0.5	mH
Flying Capacitor	V_{cf}	100	µF
High voltage side capacitor	C_H	200	µF
Low voltage side capacitor	C_L	20	µF

5.2 Control technique

5.2.1 *Inductor* current equalization control

B3LI DC/DC converter has two paralleled legs (phases) that are switched 180 degrees out of phase with each other as discussed in chapter 4. Each phase has its own output inductor, and the currents through these inductors sum up to feed the load. The inductor current waveforms in each phase have the same shape but

are shifted in time. This phase shift causes the ripple currents to be in antiphase. When the currents from both inductors are combined into the output load, the switching current ripples from each inductor partially or completely cancel each other out, depending on the duty cycle (voltage in/out ratio) and load conditions.

The load voltage and total current reflect the power delivery capacity of the converter output. In an interleaved converter with multiple paralleled legs, each leg carries an equal fraction of the total current. It is crucial to ensure that each leg carries an equal share of the load current to prevent the power components from one converter leg from overheating or being overloaded while others are underutilized which lead to efficiency reduction[105]. An equalized current reduces the stress on individual inductors, capacitors, and switches, which aims to extend the lifespan of components. It should be noted that the share of current loading can be adjusted to balance temperatures when unequal cooling of the multiple paralleled legs is detected.

Figure 5.6 shows the diagram of inductor current control. To ensure the equalized current rate, each leg current is sensed, and the total current can be calculated . This result is then compared to the reference total current to find the error. This error is adjusted separately on each leg based on the current discrepancy between the legs. Finally, the current equalizing controller adjusts duty cycles to distribute the current evenly.

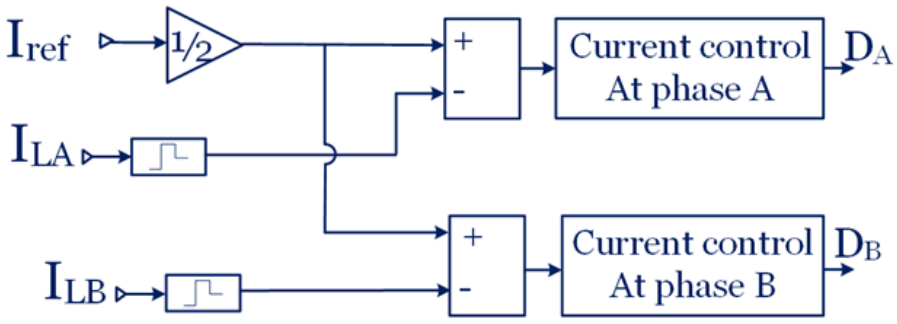


Figure 5.6 Current control

$$e_{A/B} = 0.5\, I_{ref} - I_{LA/LB} \tag{5.8}$$

In order to implement a digital PI controller, the discrete incremental equations of the PI controller are used to calculate the integral term. where i_k is the value at sample number k and T_s is the sample time. Thus, the output digital PI control

D_k is as Equation (5.9). Where *Kp* and *Ki* represent proportional and integrator gains .

$$D_k = K_p e_k + K_i(i_{k-1} + T_s e_k) \tag{5.9}$$

5.2.2 Flying Capacitor Voltage Balancing Control

Chapter 4 discussed the details of the three-level converter configuration and operation. The flying capacitor provides the intermediary voltage levels that reduce the voltage stress of the semiconductor devices and inductor, potentially reducing the converter size and extending its life span due to the lower voltage rating of switches and inductor compared to the two-level configuration. Therefore, a specific voltage control balancing is required to maintain the flying capacitor voltage to a level close to its reference ($V_{dc}/2$).

Figure 5.7 shows the block control diagram of the proposed voltage balancing control in the B3LI DC/DC converter to ensure that the voltage on the flying capacitor is equal to half of high side voltage source. As shown in the previous chapter, the voltage across each flying capacitor directly depends on the duty cycles of the switches. The charging and discharging duty cycle remains constant during a steady state. In the voltage balancing control, when the capacitor voltage is lower than the reference, the charging duty cycle is expanded, and the discharging duty cycle is reduced; in contrast, when the capacitor voltage is higher than the reference, the discharging duty cycle is expanded, and the charging duty cycle is reduced. This cycle is repeated until the target voltage is reached. The duty cycle change is represented in the Equation (5.10).

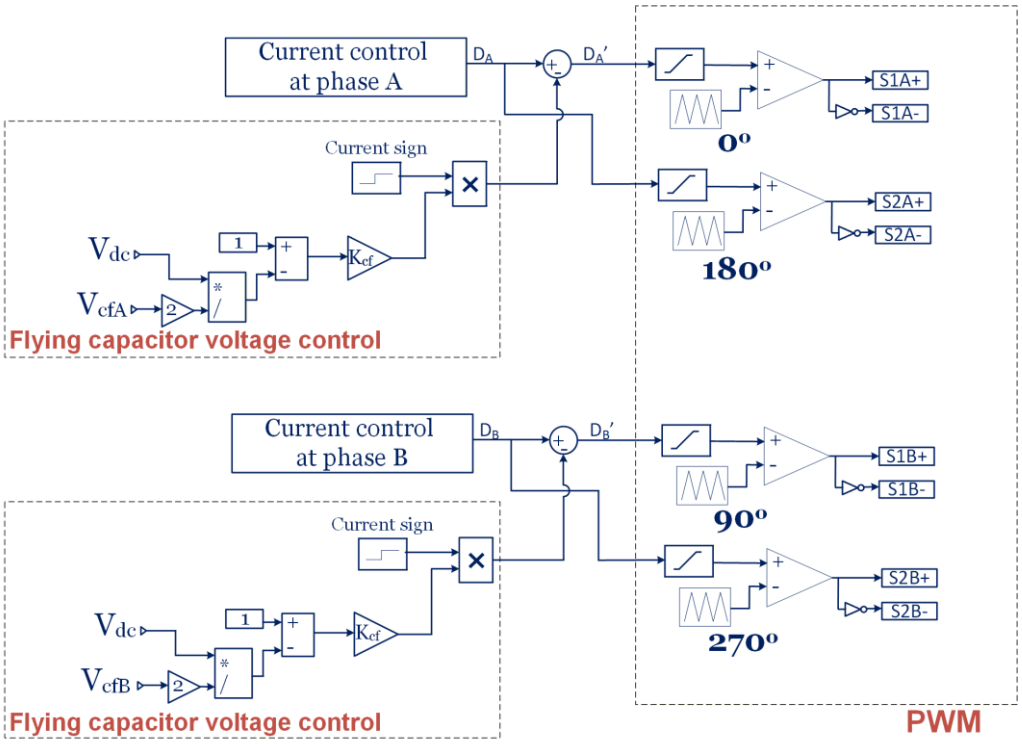


Figure 5.7 Flying capacitor voltage control and PWM generation

$$D'_A = \begin{cases} min\ (1, D_A + K_{cf}\ (1\ -\ (V_{dc}/\ 2V_{cf}))) \ for\ V_{cf} > 0.5\ V_{dc} \\ max\ (0, D_A - K_{cf}(1\ -\ (V_{dc}/\ 2V_{cf}))) \ for\ V_{cf}\ < 0.5\ V_{dc} \end{cases}$$

Where, $V_{cf} \neq 0$ (5.10)

The same formula is applied to D'_B, The gain K_{cf} is applied to manage the speed of the voltage balancing of flying capacitor particularly when capacitor pre-charged at initial point. This K_{cf} value chosen operating slower than the current control loop.

During steady-state operation, where the flying capacitor voltage is maintained at half of the DC-link voltage, the charging and discharging behaviour of the flying capacitor can be expressed as $C_f \frac{dV_{cf}}{dt} = i_L$ and $-C_f \frac{dV_{cf}}{dt} = i_L$ respectively. Therefore, the plant relating the flying-capacitor voltage to the inductor current can be represented as $G_s = \frac{1}{C\,s}$, indicating that the flying capacitor behaves as an integrator in the voltage-balancing control loop.

The current sign block in the diagram detects the direction/polarity of the reference current, which is positive during buck operation and negative during boost operation. This sign is used to swap the duty cycle D adjustment (to expand or to squeeze), because for boost operation, the flying capacitor is charged from the low-voltage side.

5.3 Simulation Result

The developed mathematical model of the proposed three-level interleaved flying-capacitor DC–DC converter in chapter 4 was validated through both simulation results to ensure its accuracy in representing the converter's dynamic behavior. Simulation modelling was conducted in PLECS to validate both the operational performance and the control strategy of the proposed B3LI converter. For the unidirectional power transfer test, a resistive load of 6 Ω was employed. In the bidirectional case, the system was evaluated using an 800 V DC-link supply interfaced up to 600 V battery stack, which was represented using a 3.8 V RC equivalent battery cell model[106]. The parameters value utilized in the simulation can be seen in Table 5.2.

Table 5.2 Simulation parameter of 60 kW B3LI DC/DC converter

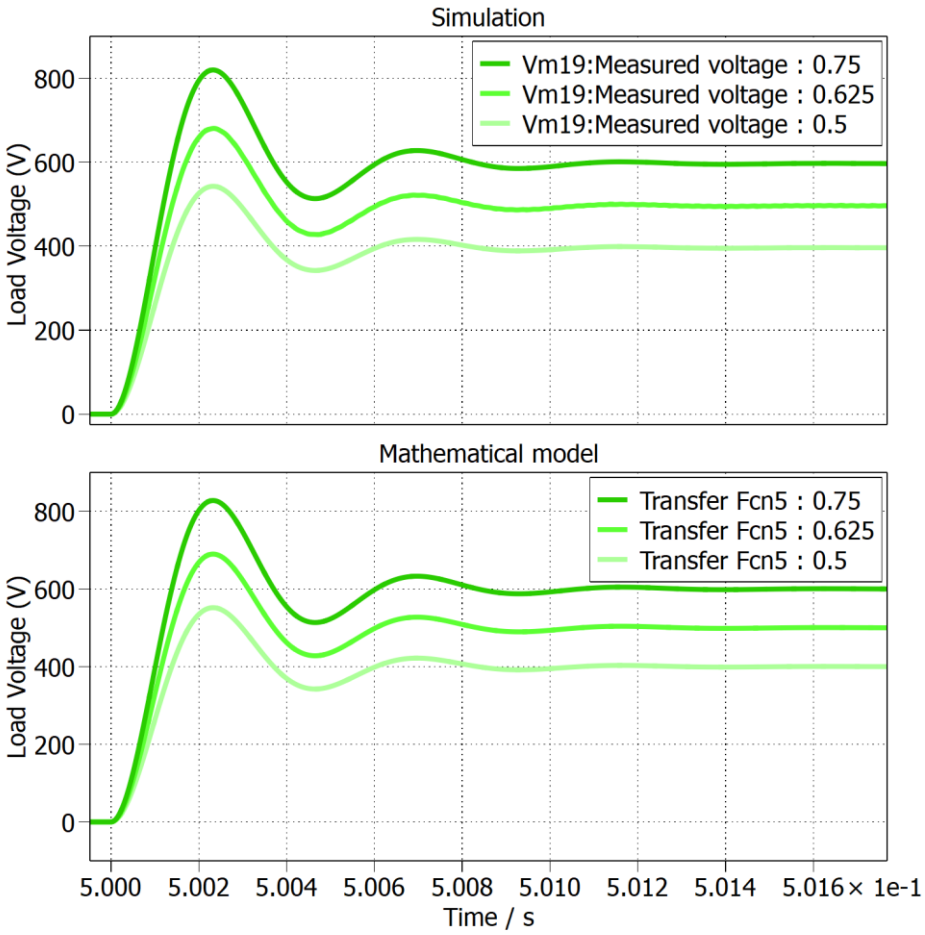
Parameters	Symbol	Value	Unit
High side voltage	V_{dc}	800	V
Low side voltage	V_{ld}	0 to 600	V
Total current	i_L	-100 to 100	A
Duty Cycle	D	0-1	
Switching frequency	f_s	10000	Hz
Leg Inductor	L	0.5	mH
Flying Capacitor	V_{cf}	100	µF
High voltage side capacitor	C_H	200	µF
Low voltage side capacitor	C_L	20	µF
Battery cell in series	ESS	3.84 V x up to 168	V

5.3.1 Open loop Control

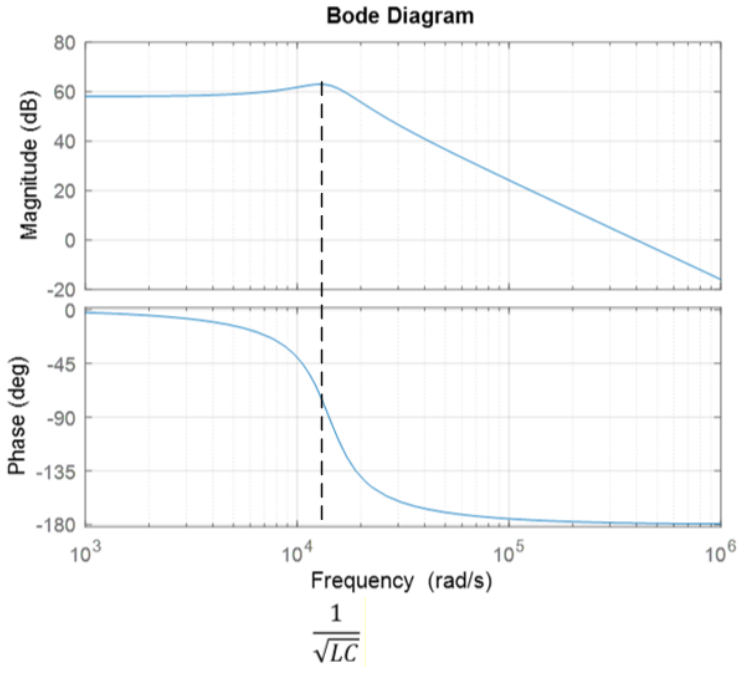
Open-loop control simulation provides a straightforward method to test the basic operation of a DC/DC converter helps in validating the fundamental design and to ensure the components function correctly within the circuit without the influence of feedback control.

The validation was performed by comparing the responses of the mathematical model with those obtained from the simulation, ensuring that both were evaluated under the same operating conditions and component parameters. Simulation test with open loop control is conducted by using parameter as in the Table 5.2. Where L=0.5mH, C=20μF, R=6Ω, Vdc=800V. A step input was applied from different duty in Equation (5.11) and Equation (5.12). The simulated steady-state and transient responses in Figure 5.8 (a) and Figure 5.9(a) closely matched the mathematical waveforms, confirming that the derived state-space equations and control model accurately capture the converter dynamics. The deviations observed at high-frequency transitions due to ripple voltage and current that were not explicitly modeled. Overall, the close agreement with the simulated results validate the correctness of the proposed mathematical model and demonstrates its suitability for control design, system optimization, and further performance evaluation.

$$\frac{\dot{V}_{ld}}{d} = 1.6\,e11\frac{1}{s^2 + 8.33\text{e}3\,s + 2\text{e}8} \tag{5.11}$$



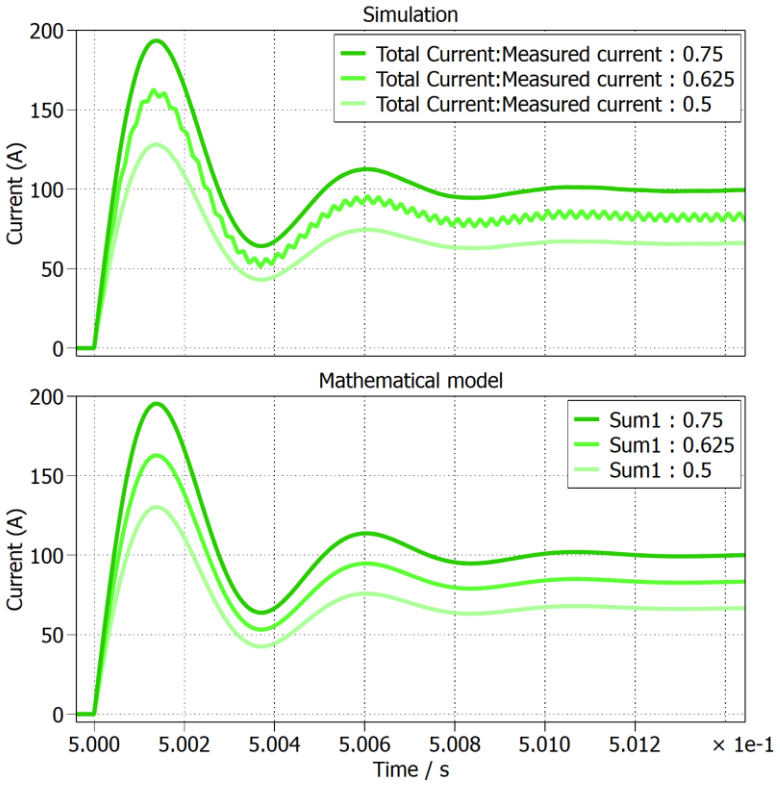
(a)



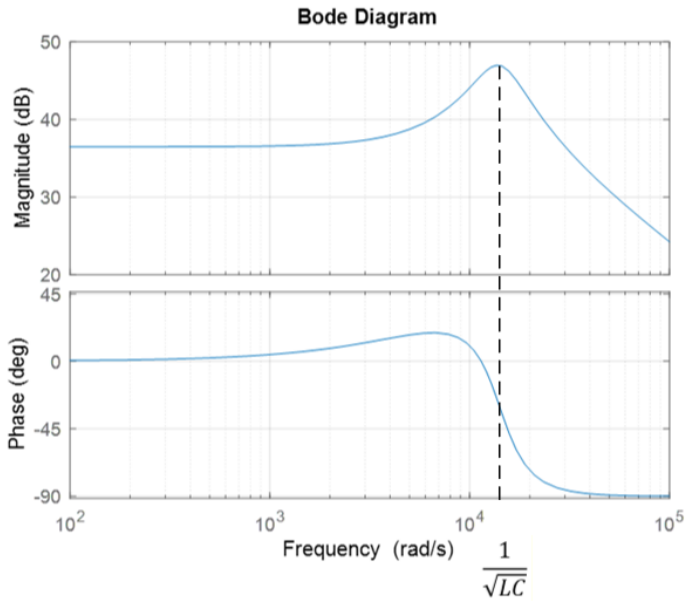
(b)

Figure 5.8 (a) Open-loop step response validation of the voltage transfer function of mathematical model. (b)bode plot of voltage transfer function

$$\frac{\dot{i}}{d} = 1.6e6 \frac{(s + 8333.33)}{s^2 + 8333.33\, s + 2e8} \tag{5.12}$$



(a)



(b)

Figure 5.9 (a) Open-loop step response validation of the current transfer function of mathematical model. (b)bode plot of current transfer function

Figure 5.10 shows the flying capacitor voltage is tested when the voltage transfer ratio equal to 0.5, where at this operating point ripple voltage is maximum. At this point, the flying capacitor is charged until half of the switching time, and discharge during another half switching time. The step current on capacitor resulting triangle voltage ripple of flying capacitor which indicate the flying capacitor always connected to circuit and alternate between these two stages. The value of flying capacitor voltage ripple can be seen in Table 5.3.

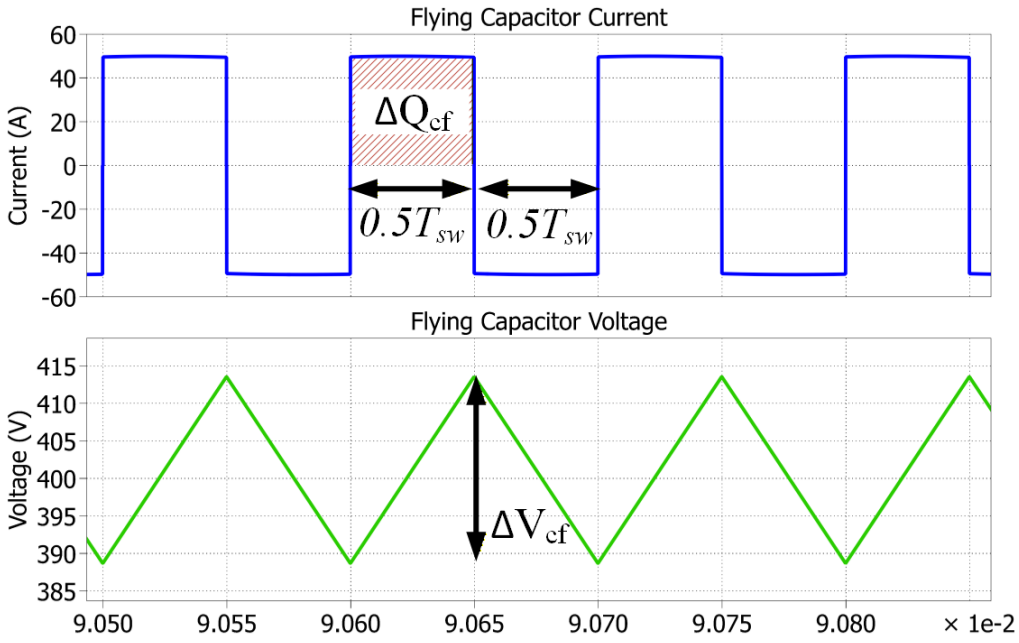


Figure 5.10 Flying capacitor current when voltage transfer ratio is equal to 0.5

The size of inductor is determined to achieve a balance performance and physical size. The inductor is sized for the worst-case operating point to ensure the converter working optimally across the entire range of possible operating points particularly when the application aimed to handle variable load. Figure 5.11 shows the simulation results for inductor current and voltage, when the voltage transfer ratio equals to 0.25 and 0.75 which are the points where maximum ripple occurred on each phase of B3LI DC/DC converter.

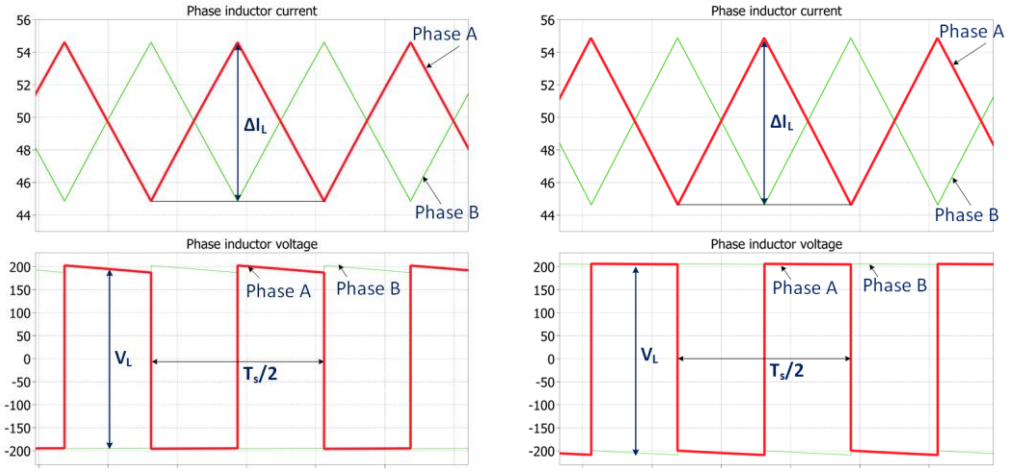
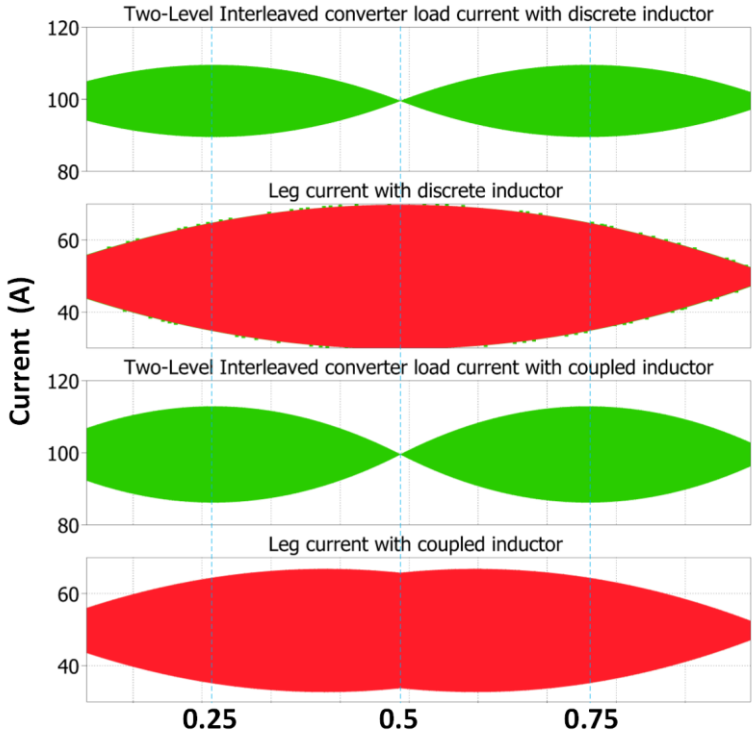
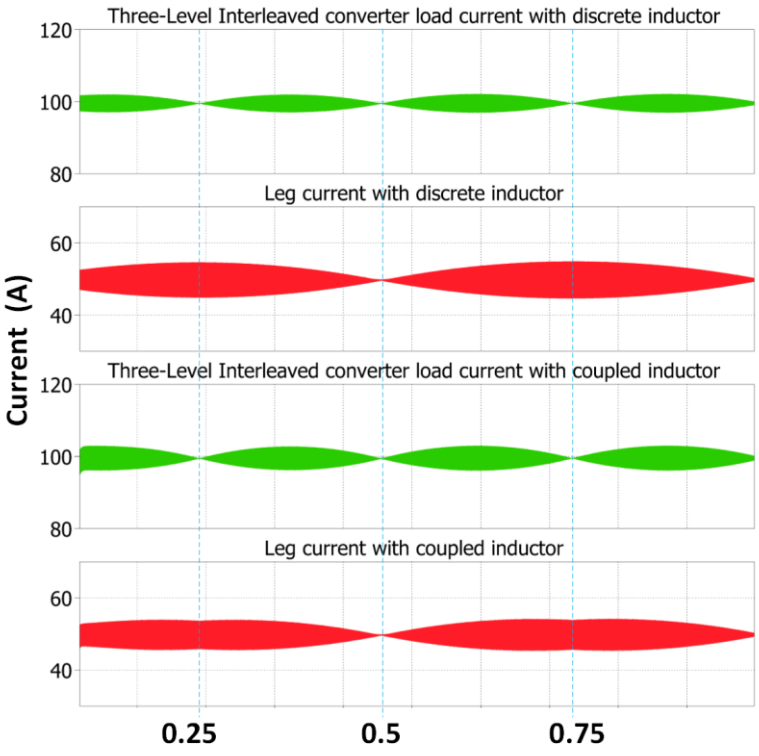


Figure 5.11 Phase inductor currents and voltage at (a) VTR =0.25 and (b) VTR =0.75

From the simulation, the ripple current value 10.25 A obtained. The ripple current is smaller compared to two-level topology either on phase and the total current. The result is validated by sweeping the full range duty cycle as illustrated in Figure 5.12. This figure was generated by linearly ramping up supercapacitor load voltage. The initial supercapacitor voltage was set 40V. Current was given constant at 100 A until the supercapacitor voltage approach 800V. The ripple current on inductor of a two-level interleaved converter is depicted in Figure 5.12(a) and compared to a three-level interleaved converter in Figure 5.12(b). Both converters were simulated by using the same size 0.5 mH inductor value. The figure also compared the discrete and couple inductor where the coupled inductor has mutual inductance 0.25mH.



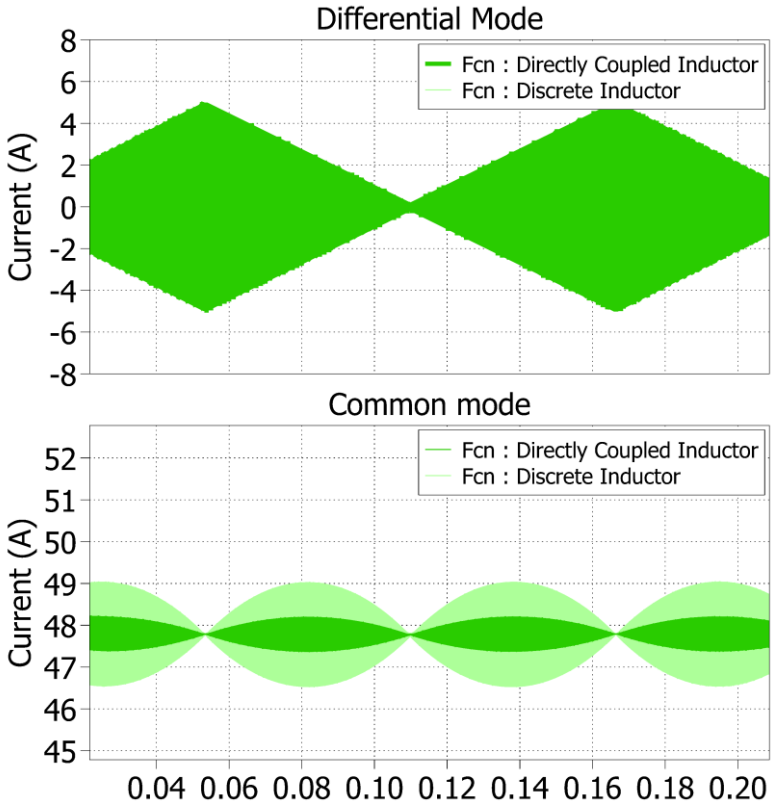
(a)



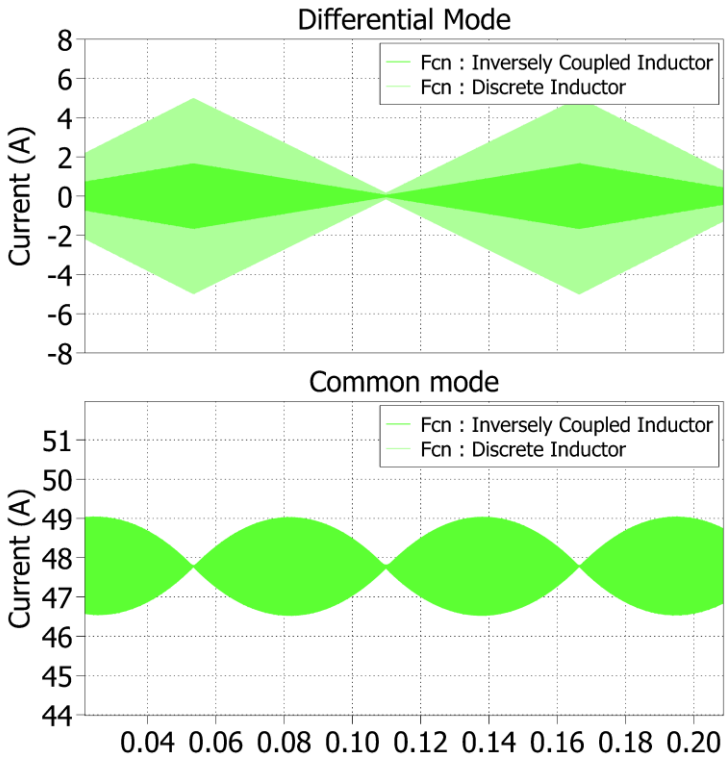
(b)

Figure 5.12 Comparison of three level versus two levels interleaved converter waveforms assuming a supercapacitor type of device charging and discharging process with constant current showing the time domain simulation of: a) Three level interleaved DC/DC converter b) two-level interleaved DC/DC converter the inductor ripple current comparison when dutycycle sweeps the full range

In the interleaved three-level flying-capacitor DC–DC converter, the integration of magnetic coupling between phase inductors influences the level of circulating current. Figure 5.13. shows the comparison between common mode and differential mode using coupled inductors and discrete inductors. Direct coupling of the inductors in Figure 5.13 (a) results increase the flow of circulating current between phases and leads to increased conduction loss in the circuit. On the other hand, inverse coupling as shown in Figure 5.13(b), effectively suppresses circulating current. Therefore, inverse coupling is the favored setup for achieving high efficiency in interleaved three-level converters, as it reduces the amplitude of circulating current.



(a)



(b)

Figure 5.13 Common mode-and differential mode current comparison using discrete and coupled inductor when dutycycle sweeps the full range a) directly coupled vs discrete inductor (b) inversely coupled vs discrete inductor

To sum up the B3LI DC/DC converter design, a comparison of theory calculation and simulation results are provided in Table 5.3.

Table 5.3 Theory and simulation comparison of passive component sizing

Component size	Theory	Simulation	Unit
Flying Capacitor, C_f = 100 µF			
ΔV_{cf} $(maximum)$ when VTR=0.5	25	24.096	V
Inductor, I_L = 0.5 mH			
Ripple current,$\Delta i_{(phase)}$ when VTR=0.75	10	10.2514	A
High side capacitor, C_H =200 µF			
Ripple voltage, ΔV_{cH} when VTR=0.75	6.25	6.125	V
Capacitor Current, I_{CH} at when VTR=0.75	25	24.6114	A
Low side capacitor C_L = 20 µF			
Ripple voltage, ΔV_{cL} when VTR=0.75	6.25	6.125	V
Capacitor Current, I_{CL} when VTR=0.75	5	5.2	A

5.3.2 Close loop control

Close loop control of the B3LI DC/DC converter ensures reliable performance across all operating points. It is crucial to make sure the controller is properly designed to operate stably and able to maintain consistent performance against disturbances and variations in operating conditions. Closed-loop control improves the transient response and the steady-state accuracy of the converter. It allows the converter to quickly react to changes in the load or input voltage and helps in achieving precise regulation according to the reference input despite external variations.

Focus on the current large-signal behavior of the system while neglecting the load ripple. Consequently, the terms that are inversely proportional to C are ignored. The resulting simplified of the current plant in Equation (4.25) to be expressed as Equation (5.13)

$$\frac{i}{d} = \frac{V_{dc}}{L\,s} \tag{5.13}$$

The equation also true in the boost operation of the converter considering the dc link voltage is constant and the current flows in the opposite direction.

The close-loop transfer function therefore,

$$\frac{\dot{i}}{I_{ref}} = \frac{G_c\,G_p}{1 + G_c G_p} \tag{5.14}$$

Where the parameter given is as in the Table 5.4

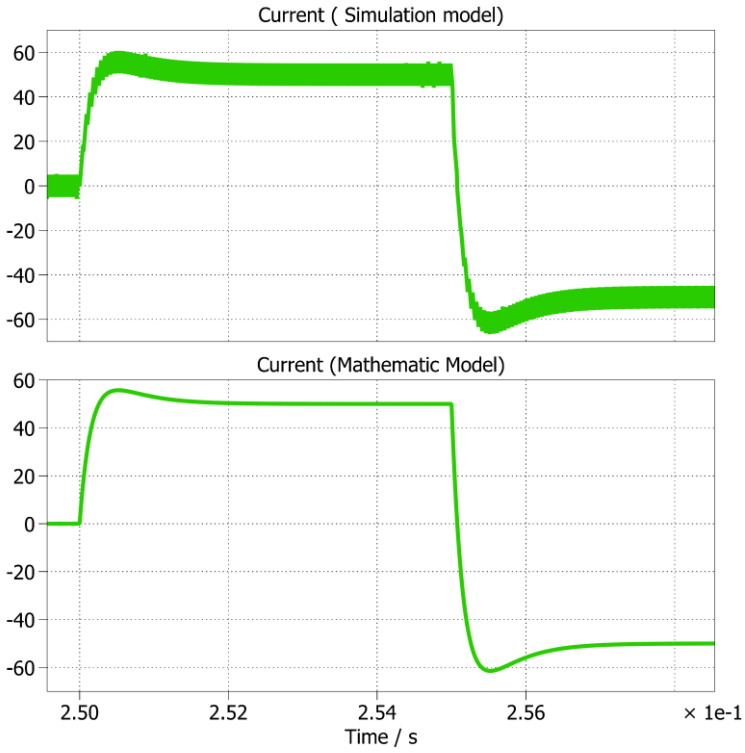
Table 5.4 Controller parameter

Parameters	Symbol	Value
PI Controller		
Proportional	K_p	0.0026
Integral	K_i	4.225
Natural Frequency	ωn	2600 rad/s
Damping ratio	ζ	0.8

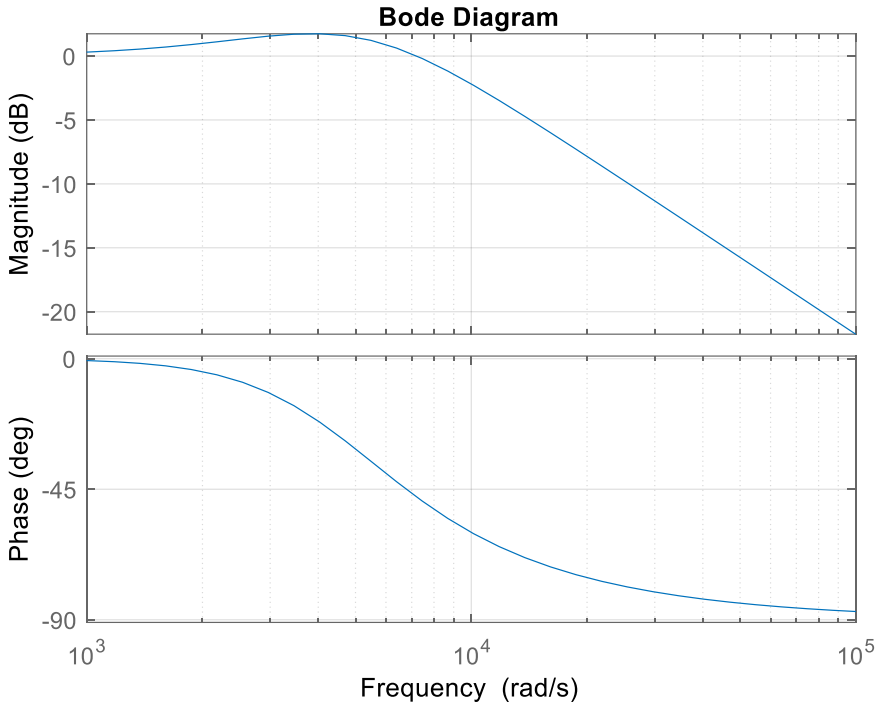
Hence, current transfer function in close loop is expressed as Equation (5.15).

$$\frac{i}{I_{ref}} = \frac{4160s + 6.756e6}{s^2 + 4160s + 6.756e7} \tag{5.15}$$

The simulation employs a battery model on the load side. The resulting waveform, as illustrated in the Figure 5.14, (a) exhibits an overshoot of 17.97% with a corresponding rise time 3.1038×10^{-4}seconds and settling time of approximately 1.9×10^{-3}seconds.



(a)

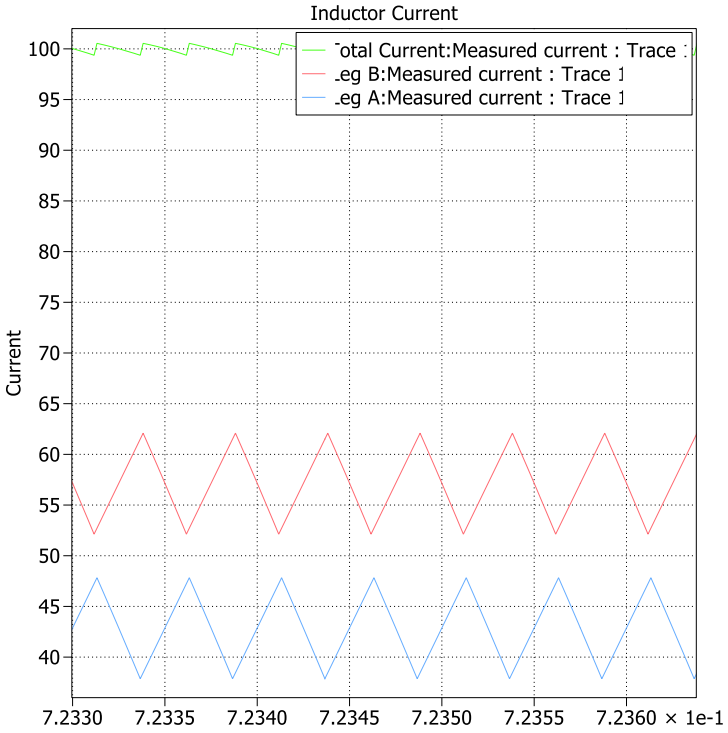


(b)

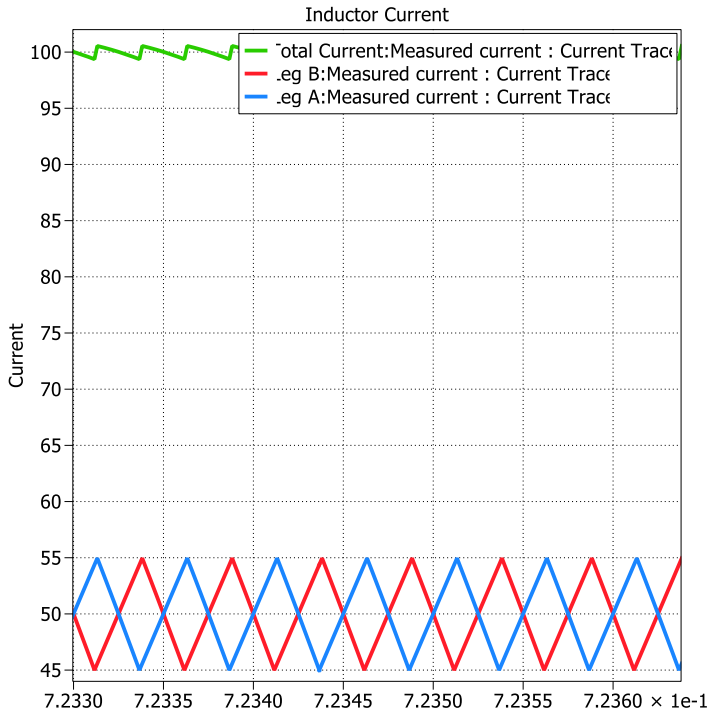
Figure 5.14 Close loop current control (a) Simulation and mathematical model comparison of the step response (b) Bode plot

5.3.2.1 Current equalizing simulation

The unequal converter leg current may happen due to unequal properties of the components such as the internal resistance as illustrated in Figure 5.15(a). Therefore, duty cycle adjustments are made based on the feedback from each leg inductor current. If one leg starts to carry more current than the others, the duty cycle will be adjusted accordingly to maintain the equal current on each leg by minimising the error The simulation of current control after applying equalizing current control can be seen in Figure 5.15 (b). Despite the internal resistance difference, the leg inductors carry the same amount of current. The total current is the sum of the two-phase inductor currents. With the interleaving technique, the phase current in one phase is shifted with respect to the other phase in order to benefit from ripple cancellation in the total current.



(a)



(b)

Figure 5.15 Inductor current with the internal resistance difference R 0.015Ω and 0.02Ω (a) without current equalizing control (b) with current equalizing control

5.3.2.2 *Flying capacitor voltage balancing simulation*

A scenario example is simulated in Figure 5.16, that describes the voltage balancing process in the condition where one converter leg has the flying capacitor voltage V_{cf} value is higher than $V_{dc}/2$ (shown on the top side) and the other leg has a lower flying capacitor voltage value (shown on the bottom plot). In the operation of the system, if the flying capacitor voltage is lower than Vdc/2, the redundant charging state is predominantly utilized during the charging phase, while the discharging state is shortened. On the contrary, the opposite behaviour is applied when the flying capacitor voltage is higher than $V_{dc}/2$. The change of duty cycle is inversely proportional to the voltage difference. As the system approaches the target steady state, the voltage level of both phases progressively converge. At steady state, the duty cycles of both phase for the charging and discharging states become equal, signifying that the rate of electrical charge entering is balanced by the rate of charge leaving the flying capacitor.

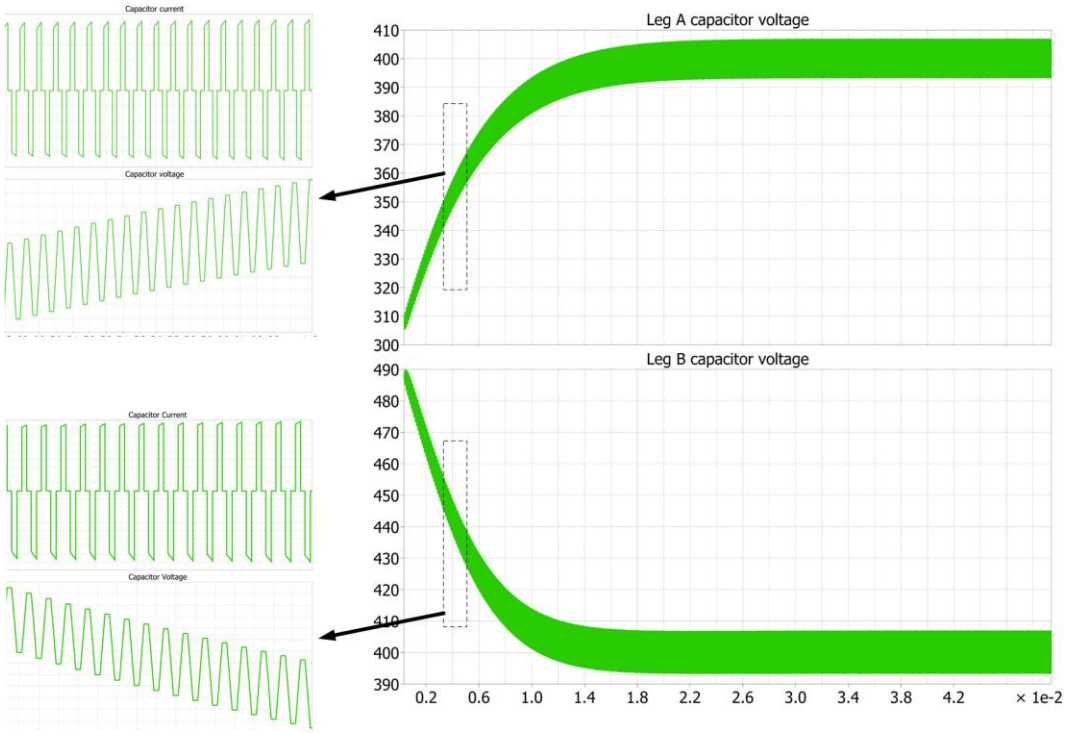
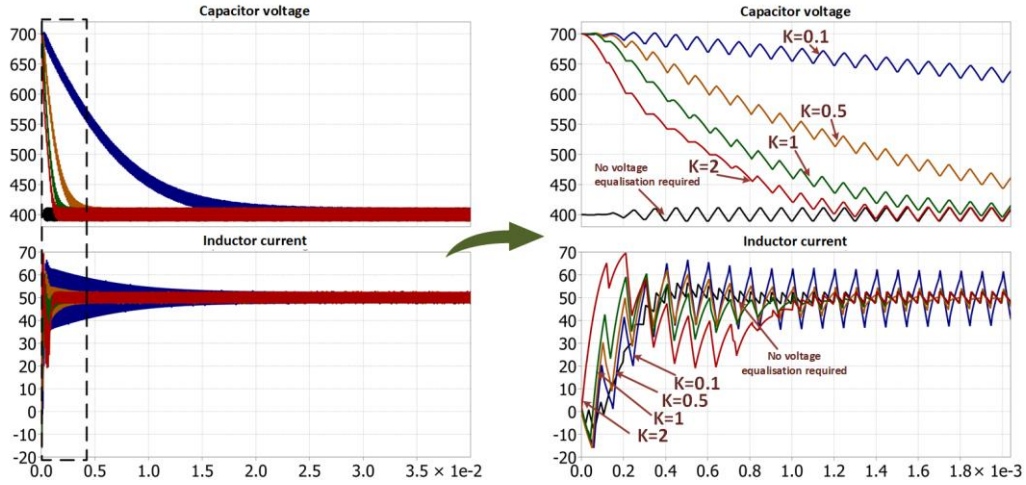


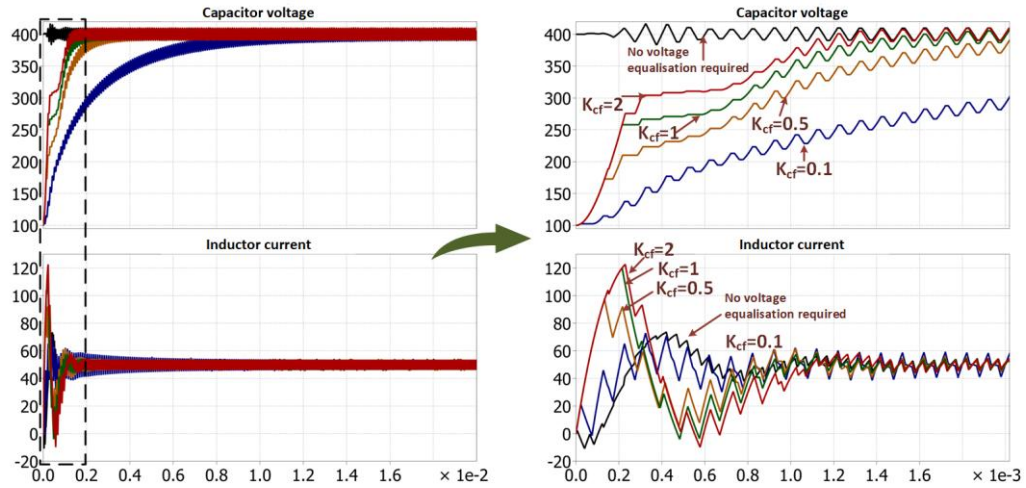
Figure 5.16 Response of the flying capacitor with voltage balancing controller

The gain K_{cf} is applied to optimise the speed of the voltage balancing of the flying capacitor. Ideally the charging and discharging will only affect the flying

capacitor voltage because the control uses redundant switching states that have same effect on the output voltage and current to charge and discharge the flying capacitor. However, since both voltage balancing and current control both are relied on the switching state, during flying capacitor precharging, such as the converter startup, where significant imbalances appear which means the effect of the two switching states on the output are no longer the same, the voltage balancing process may influence the operation of the output current controller. Figure 5.17 shows the effect of using different K_{cf} values on inductor current during startup.



(a)

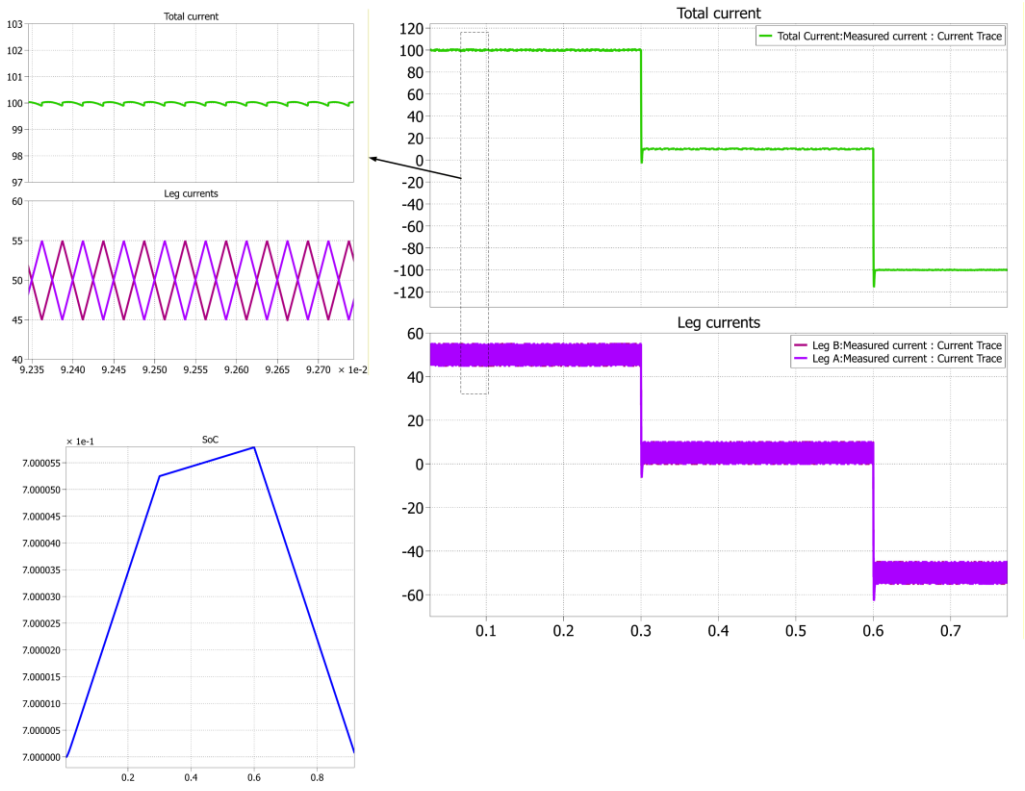


(b)

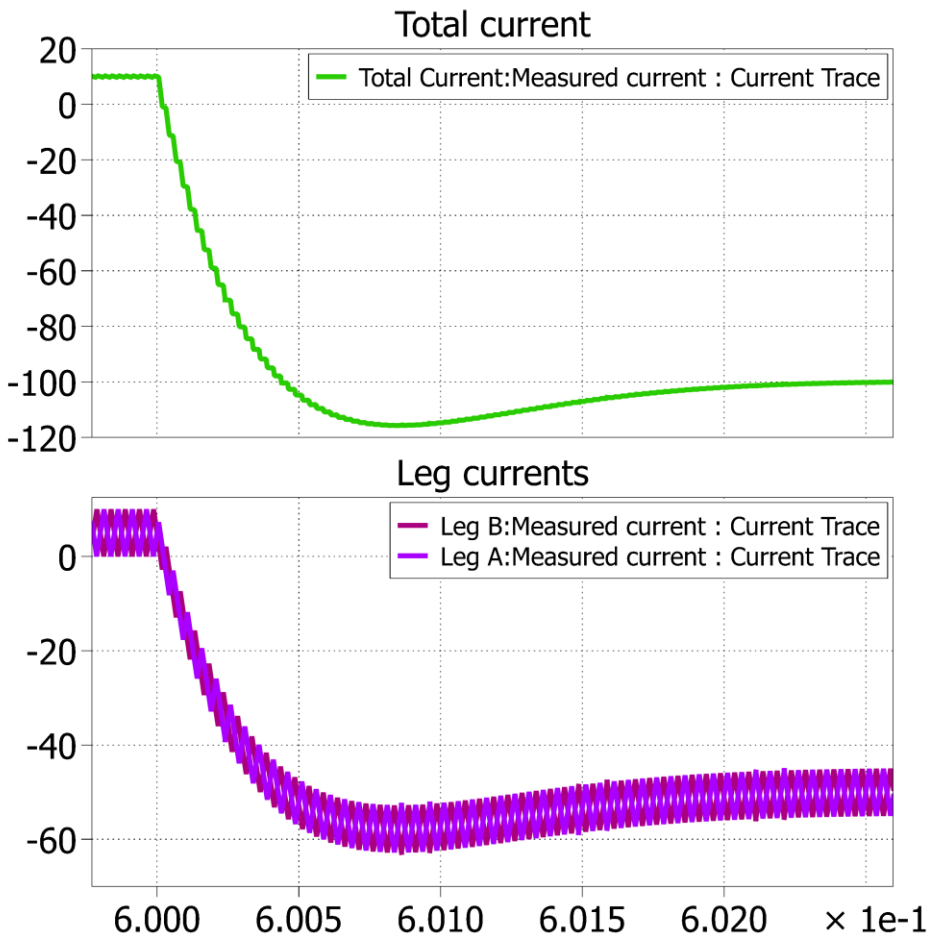
Figure 5.17 Effect of using different K_{cf} values on the response of the flying capacitor voltage controller and the inductor current (a) C_f voltage higher than $V_{dc}/2$, (b) C_f voltage lower than $V_{dc}/2$

5.3.2.3 Simulation of bidirectional power flow operation

B3LI DC/DC converter needs to be able to support bidirectional power flow operation Figure 5.18 (a) shows the simulation of the B3LI system performing step changes from high power charging to low power charging and then to high power discharging. The left bottom of shows the state of charge (SoC) of the battery (based on RC model) responds during this operation. When battery is charged, the B3LI system delivers power to the low voltage side and 100 A ripple free current flows to the output battery. The current on each leg is 50 A which remains balanced although it has different series resistance value.



(a)



(b)

Figure 5.18 (a) The current flows in the phase inductors and total of the B3LI converter (b) Current zoomed in during transient

During low load current flow requirements (0.2<t<0.3), one leg can be deactivated from the system to save on switching losses so that the converter is only working with one leg. This may give efficiency improvement for low power operation, but the output current ripple at low load current is higher because the is ripple cancellation as no interleaving takes place thus the operation will be similar to a single channel three-level DC/DC converter.

During discharging (t>0.3s), the system works moves power from low voltage side to the high voltage side (boost mode). Negative current indicates the power flow direction.

5.3.3 *Alternative* control (Model Predictive Controller)

The PI controller is a popular choice due to its simpler algorithm. It can effectively regulate and maintain the output to follow the reference ensuring stable and consistent performance. A PI controller can be easily tuned to optimise the performance of the DC/DC converter for specific applications. However, its dynamic response is relatively slow, leading to a longer stabilisation time. Additionally, oscillation may occur around the set value [107].

A model predictive controller (MPC) is an alternative method to control the converter. It offers several benefits, including improved performance such as, faster transient response time. MPC algorithms use a model of the system to predict future behaviour and optimise control inputs to achieve desired performance. MPC can help reduce the control system complexity by consolidating multiple control loops into a single model-based control algorithm. However, one potential disadvantage of using a model predictive controller (MPC) in a DC/DC converter require higher computational power, proportional to number of switching combination, to execute due to the need of smaller sampling time and a fast processing time otherwise the controller may not be able to accurately predict and compensate for changes in the system, such as changes in load or input voltage, which can result in reduced performance [108], [109], [110].

This section compares the PI controller method and Model Predictive Controller on a Three-level DC/DC converter where MPC or PI controller outplay each other when the application has two control variables: the inductor current and the flying capacitor. To simplify the comparison, the simulation is carried out only for a single channel of Three Level Flying Capacitor DC/DC Converter as in Figure 5.19.

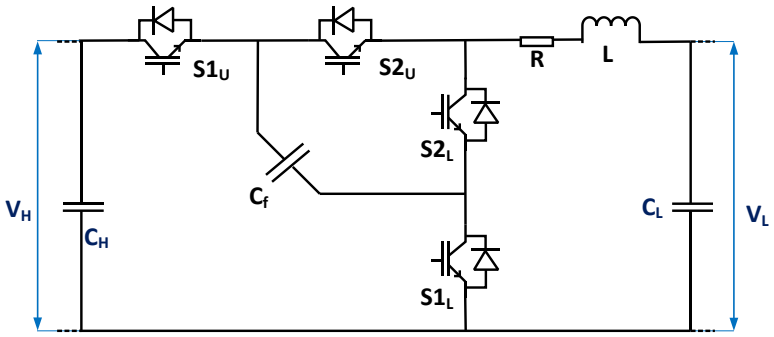


Figure 5.19 Single channel Three Level Flying Capacitor DC/DC Converter

The MPC algorithm selects a converter state that minimises the control parameter error between the reference and the next sampling interval. This process involves two primary steps: prediction and error minimization.

Predictive model

The predictive model is a mathematical representation of the system being controlled, which is used to predict the future system behaviour over a specified prediction horizon. This model allows the controller to anticipate future outcomes based on current and past system states and inputs. In order to predict the parameter, discretization techniques are employed. Among the commonly used methods is the Forward Euler approximation approach as in Equation (5.16):

$$\frac{dI}{dt} \approx \frac{I_{L(k+1)} - I_{(k)}}{T_s} \; and \; \frac{dV}{dt} \approx \frac{V_{(k+1)} - V_{(k)}}{T_s} \tag{5.16}$$

MPC algorithm predicts the inductor current and flying capacitor voltage for all switching states possibilities of the converter. Considering all 4 state possibilities shown in Figure 5.20 and Table 1, during buck operation, the prediction equation of inductor current $I\ (k+1)$ and flying capacitor voltage $V_{cf}(k+1)$ can be obtained as in Equation (5.17) and (5.18) respectively.

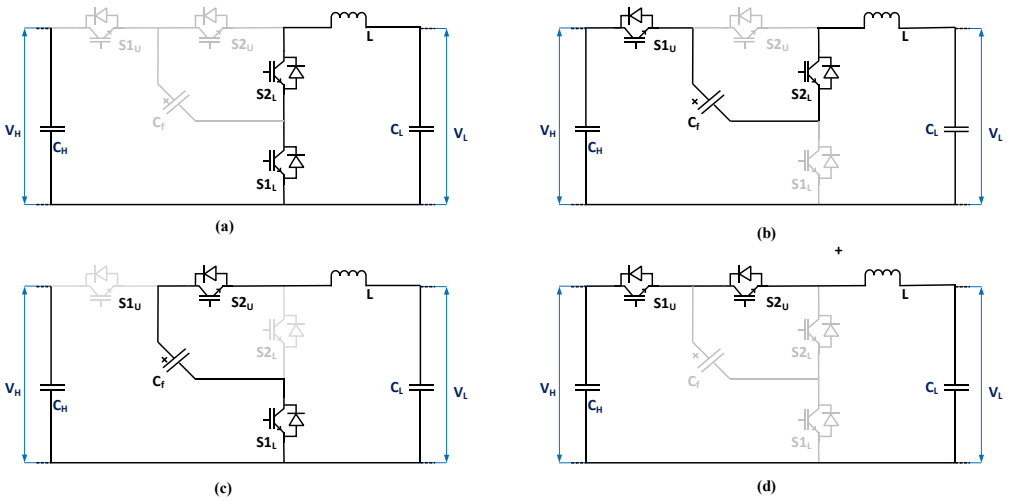


Figure 5.20 Switching state possibilities of converter (a) 00, (b) 01, (c) 10 (d) 11

Table 5.5 Switching states

States	$S2_U$	$S1_U$
1	0	0
2	0	1
3	1	0
4	1	1

$$I^{p}_{L(k+1)} = I_{L(k)} + \frac{T_s}{L}\left(S1_U\, V_H(k) + (S2_U - S1_U)V_{cf(k)} - V_{L(k)}\right) \tag{5.17}$$

$$V^{p}_{cf(k+1)} = V_{cf(k)} + \frac{T_s}{C_f}(S2_U - S1_U)I_{L(k)} \tag{5.18}$$

The Equation (5.17) and (5.18) are true to be implemented for boost operation [111]of the converter apart from the current flow in the opposite direction as in the Equation (5.19) :

$$S1_U = 1 - S1_L \text{ and } S2_U = 1 - S2_L \tag{5.19}$$

Error minimization

The second step in the MPC algorithm is to minimize the error. Unlike other control algorithms, which rely on the difference between the reference and measured values, the MPC algorithm uses the error between the reference and predicted values. This feature allows the algorithm to select the most appropriate

action for the next step to result in lowest error, resulting in improved dynamic capabilities. To determine the error term, cost functions are employed in MPC algorithms.

The cost function is expressed in Equation (5.16) and (5.17), with $g1$ and $g2$ representing the cost function of inductor current and flying capacitor voltage, respectively.

$$g1 = \left|I_{ref} - I^{P}_{L(k+1)}\right| \tag{5.20}$$

$$g2 = \left|V_{ref} - V^{P}_{cf(k+1)}\right| \tag{5.21}$$

Using quadratic cost function as in Equation (5.22) and (5.23) is preferable than the absolute because the large cost function penalized more heavily.

$$g1 = \left(I_{ref} - I^{P}_{L(k+1)}\right)^2 \tag{5.22}$$

$$g2 = \left(V_{ref} - V^{P}_{cf(k+1)}\right)^2 \tag{5.23}$$

Switching event reduction /current ripple adjustment

When implementing a model predictive controller on the B3L DC/DC converter, switching reduction is an important consideration to prevent excessive switching of the converter. Changes in switching events is skipped while keeping the current ripple within the specified limits.

Equation (5.24) expressed the cost function of switching reduction, $g3$. The sum first term and the second term represent the number of the change switching events on S1 and S2 at (k+1) respectively which add up the cost function.

$$g3 = \left|S1_{u\,(k+1)} - S1_{u\,(k)}\right| + \left|S2_{u\,(k+1)} - S2_{u\,(k)}\right| \tag{5.24}$$

Considering that the different terms of the cost function, $g1, g2$ and $g3$ which have different units and magnitudes, weighting factors, λ, are introduced. Adding the weighting factor allows the level of compromise to be adjusted between which reference following and control effort will be implemented so the total cost function is expressed as in Equation (5.25). The flowchart in Figure 5.21 describes the step to apply MPC on B3L converter as discussed.

$$g = \lambda_i g1 + \lambda_v g2 + \lambda_s g3 \tag{5.25}$$

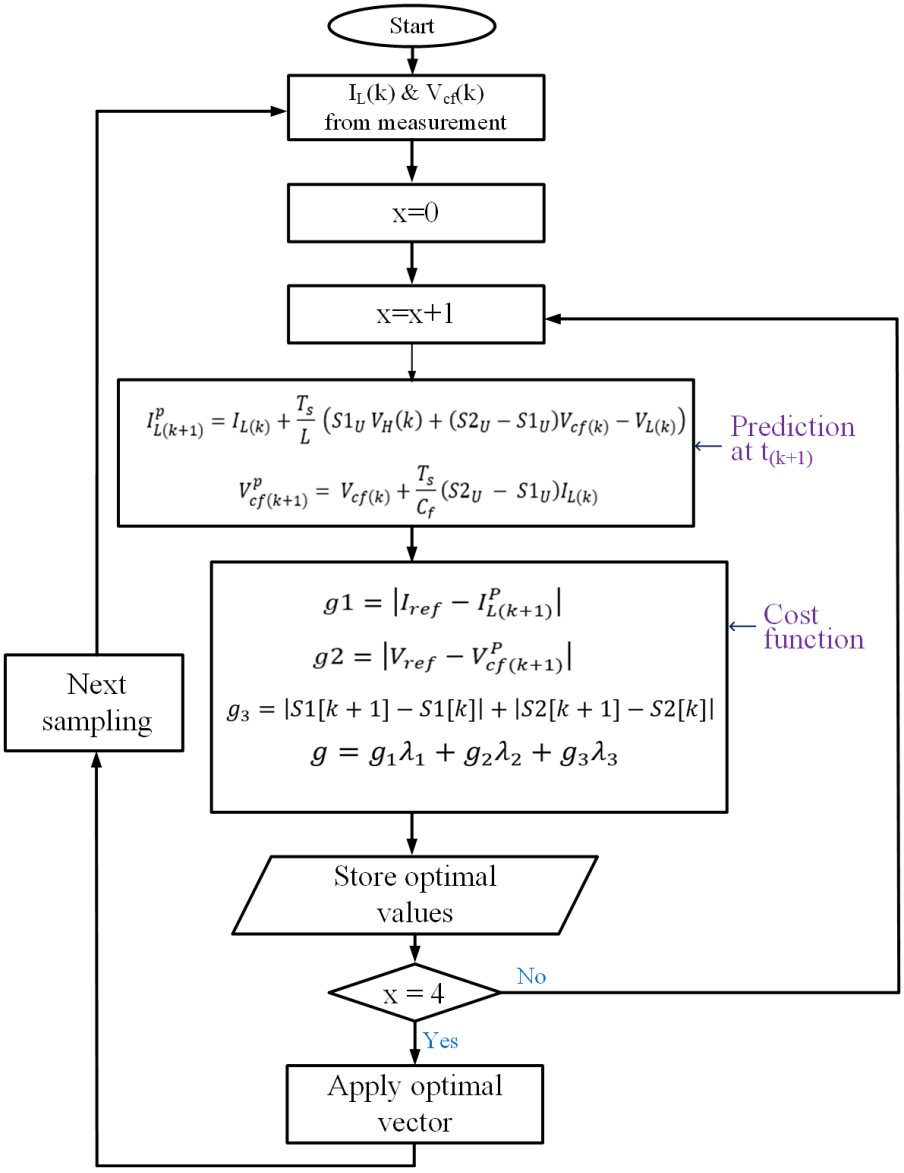
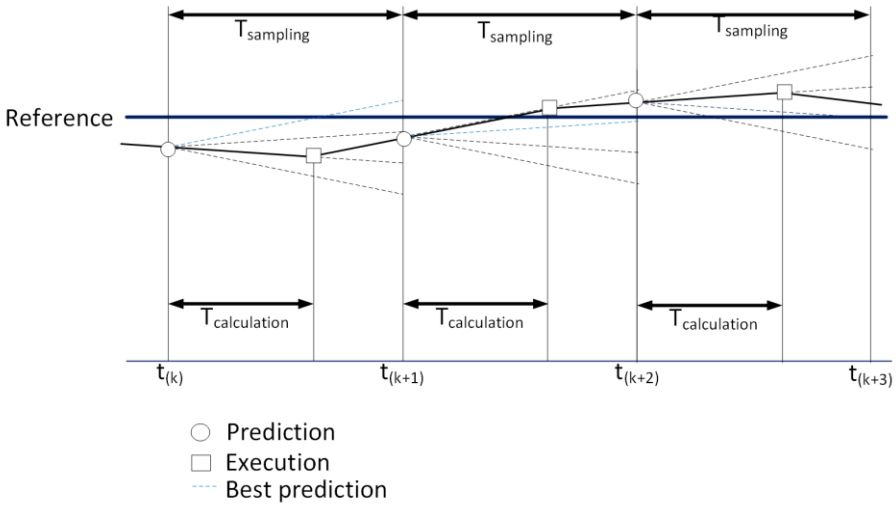


Figure 5.21 Flow diagram of MPC applied to the bidirectional 3-level converter

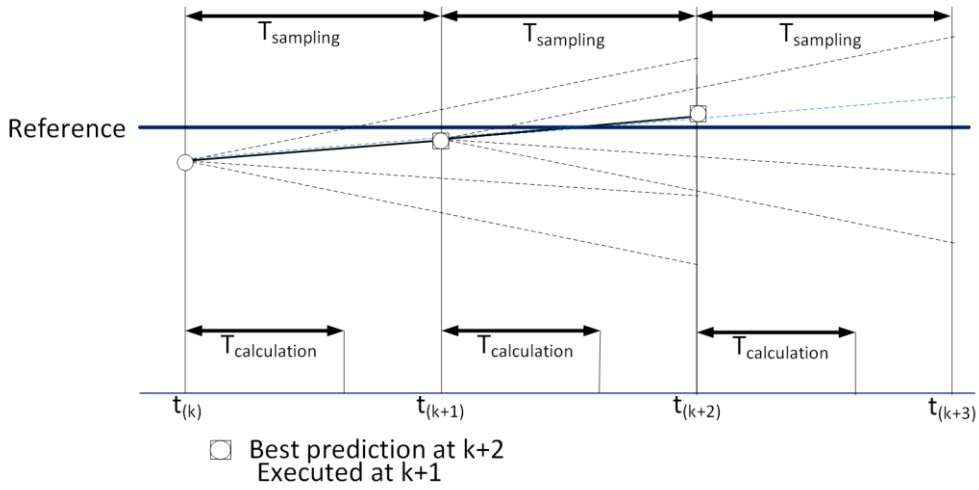
Delay compensation

In an ideal situation, the time needed for calculations is negligible, allowing the predictive control to function as shown in Figure 5.22(a). This ideal scenario is presented for comparison purposes. The currents are measured at moment $t_{(k)}$, and the optimal switching state is assumed to be calculated instantly. The switching state that minimizes the error at moment $t_{(k+1)}$ is selected and applied at time $t_{(k)}$. Consequently, the I_L and V_{cf} reaches the predicted value at $t_{(k+1)}$. However, if the calculation time is significant compared to the sampling time, there will be a delay between the instant at which the currents are measured and the instant of application of the new switching state (a). During this interval, the

previous switching state will continue to be applied. As illustrated in the Figure 5.22(a), the voltage vector selected using measurements at $t_{(k)}$ will persist after $t_{(k+1)}$, causing the current I_L and voltage V_{cf} to move further away from the reference. The next actuation will be selected based on the measurements in $t_{(k+1)}$ and will be applied near $t_{(k+2)}$. As a result of this delay, an increase in oscillation around the reference will occur. A solution to compensate this delay is to consider the calculation time by extending the prediction horizon further and apply the selected switching state after the next sampling instant [109], [112]



(a)



(b)

Figure 5.22 Calculation and sampling time (a) without delay compensation, (b) with delay compensation

The control algorithm with delay compensation is modified as in Figure 5.23. The steps start by undertaking measurements of relevant currents and voltages, and

subsequently, compared to the original control algorithm shown in Figure 5.21, execution of the switching state is moved to the beginning based on the switching state calculated during the previous interval. Subsequently, it estimates the value of the controlled currents and voltages at time $t_{(k+1)}$, taking into account the applied switching state. Next step is prediction the controlled currents and voltage for the next sampling instant $t_{(k+2)}$ for all possible switching states as in Equation (5.26)and (5.27).

$$I^{p}_{L(k+2)} = I_{L(k+1)} + \frac{T_s}{L}\left(S1_U\, V_{H(k+1)} + (S2_U - S1_U)V_{cf(k+1)} - V_{L(k+1)}\right) \quad (5.26)$$

$$V^{p}_{cf(k+2)} = V_{cf(k+1)} + \frac{T_s}{C_f}(S2_U - S1_U)I_{L(k+1)} \quad (5.27)$$

The next step is assessing the cost function for each control parameter as express in Equation (5.28), (5.29) and (5.30). Then as described in Equation (5.31), each cost function is multiplied with its corresponding weighting factor and the results are then summed. The optimal vector is selected based on minimum value of the sum of those three equations. The predictions are calculated using predicted model shifted one step forward in time because the selected optimal vector is applied at $t_{(k+1)}$.

$$g1 = \left|I_{ref} - I^{P}_{L(k+2)}\right| \quad (5.28)$$

$$g2 = \left|V_{ref} - V^{P}_{cf(k+2)}\right| \quad (5.29)$$

$$g3 = \left|S1_{u\,(k+2)} - S1_{u\,(k)}\right| + \left|S2_{u\,(k+2)} - S2_{u\,(k)}\right| \quad (5.30)$$

$$g = \lambda_1 g1 + \lambda_2 g2 + \lambda_3 g3 \quad (5.31)$$

Figure 5.23 depicts the steps to apply the MPC algorithm with delay compensation to the B3L DC/DC converter.

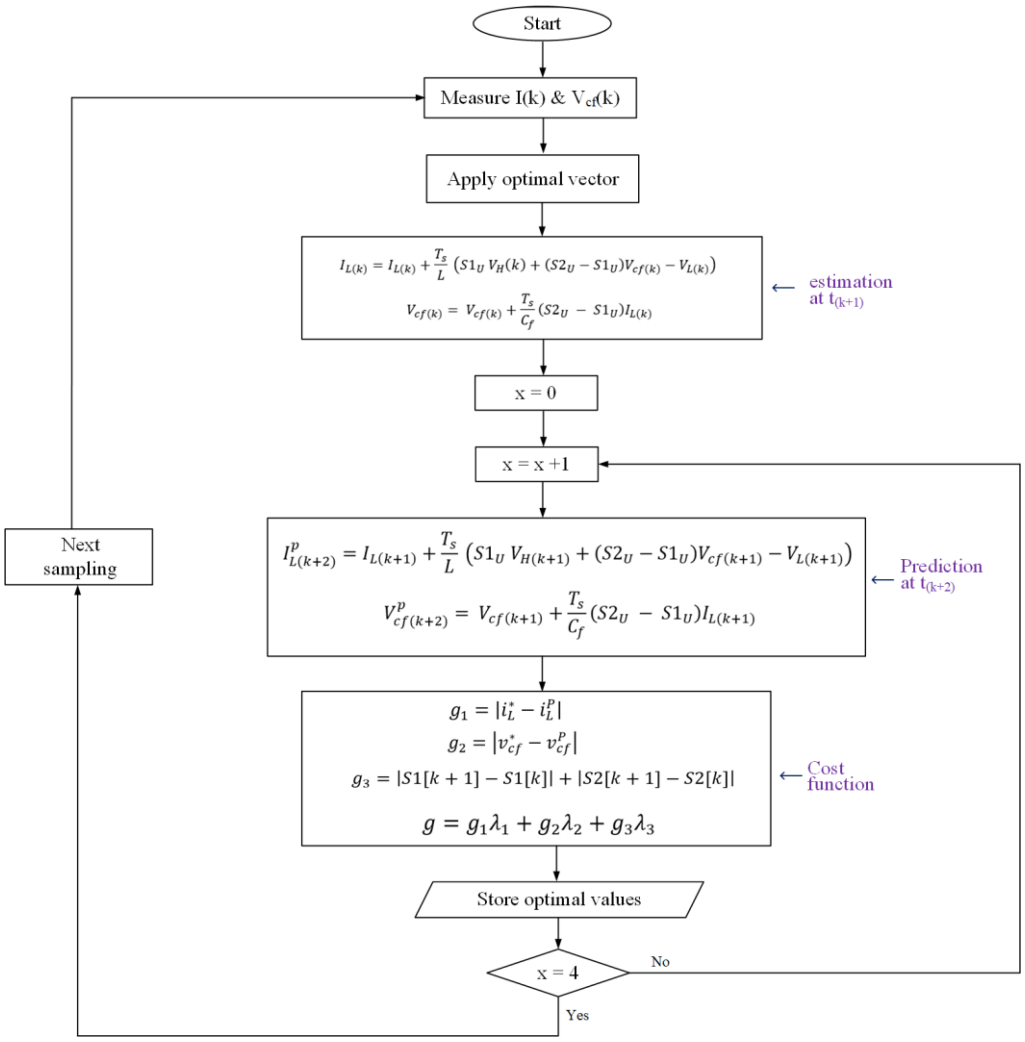


Figure 5.23 Model predictive controller algorithm with delay compensation

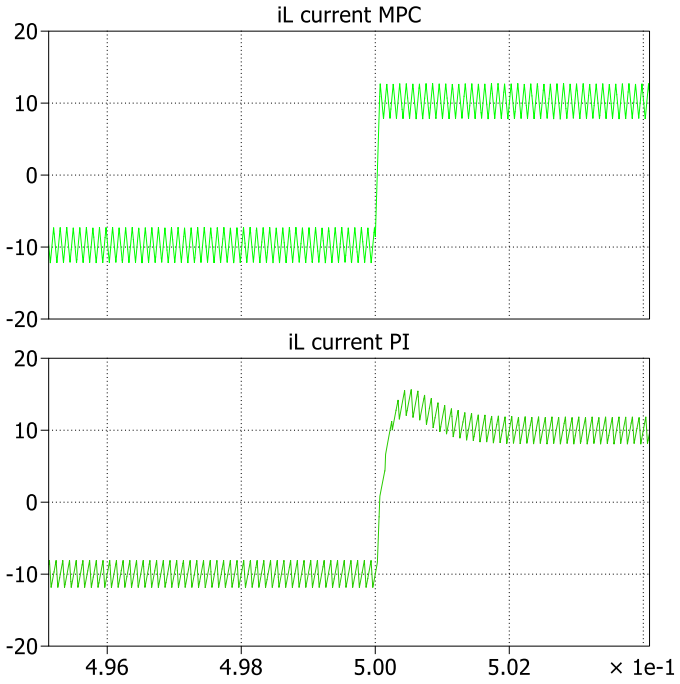
The bidirectional three-level DC/DC converter as described in Figure 5.19 and the proposed MPC control structures is verified and compared to PI controller in simulation studies. The simulation parameters are given in Table 5.6.

Table 5.6 Simulation Parameter

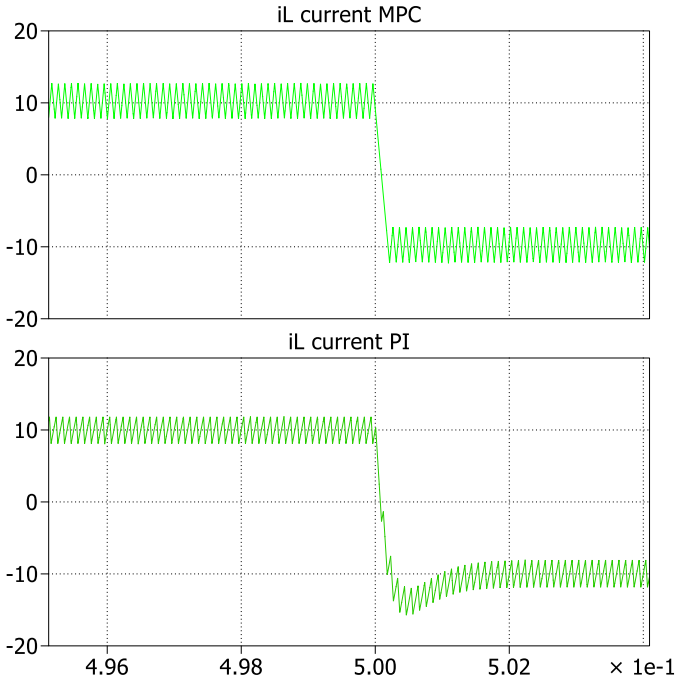
Parameter	Value	Unit
High side voltage ,V_{dc}	800	V
Low side voltage, V_{Ll}	600	V
Inductor current, I_L	-10 to 10	A
Inductance, L	5	mH
Flying capacitor, C_f	100	uF
Switching frequency	5	kHz

The PI controller adjusts the duty cycle using proportional and integral terms based on the error between the reference and actual output inductor current. The flying capacitor voltage controller readjusts duty cycle at control input voltage. While the MPC uses a dynamic model of the converter to predict future behaviour and optimize control inputs over a finite time horizon, by evaluating the cost function, the MPC will make an optimal control decisions.

The dynamic performance of the model predictive current control algorithm has been tested with step changes on the inductor current reference from buck operation (10 A) to boost operation (10A) and vice versa. Figure 5.24 shows the steady state and transient response of both controllers. The PI controllers provide a stable inductor current output but slower responses for transient conditions compared to MPC in DC/DC converters. Furthermore, MPC provides more precise control during transient compared to the PI controller, ensuring that there is no overshoot during the transient response.



(a)



(b)

Figure 5.24 Step transient response of the current controller that are using MPC and PI (a) step up, (b)step down.

A similar situation occurs in the flying capacitor voltage control shown in Figure 5.25 where MPC adjust the switching state to increase the capacitor voltage until 400V set point at a faster rate compared to PI controller. These prove that MPC is more adaptive to changing operating conditions and system dynamics than PI control. This is due to the MPC's nature to predict and anticipate future system behaviour. However, this is achieved with more a complex and computationally intensive effort compared to PI controllers. Although PI controllers exhibit slower response, it is simpler and more effective in steady-state conditions, with switching frequency being constant and predetermined by PWM.

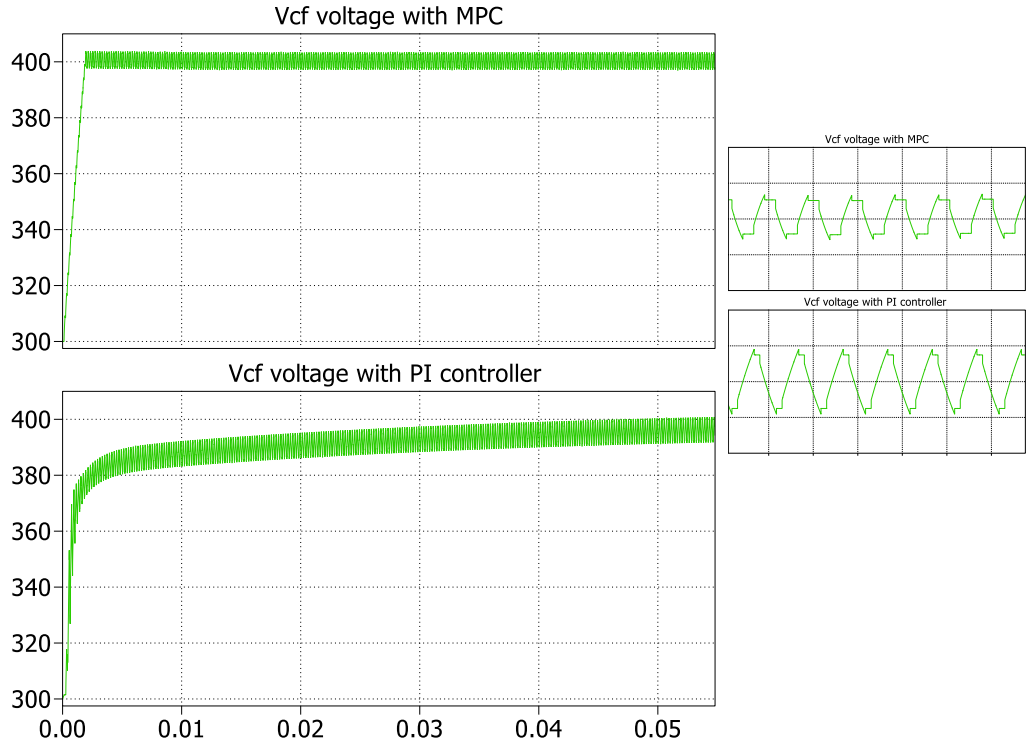
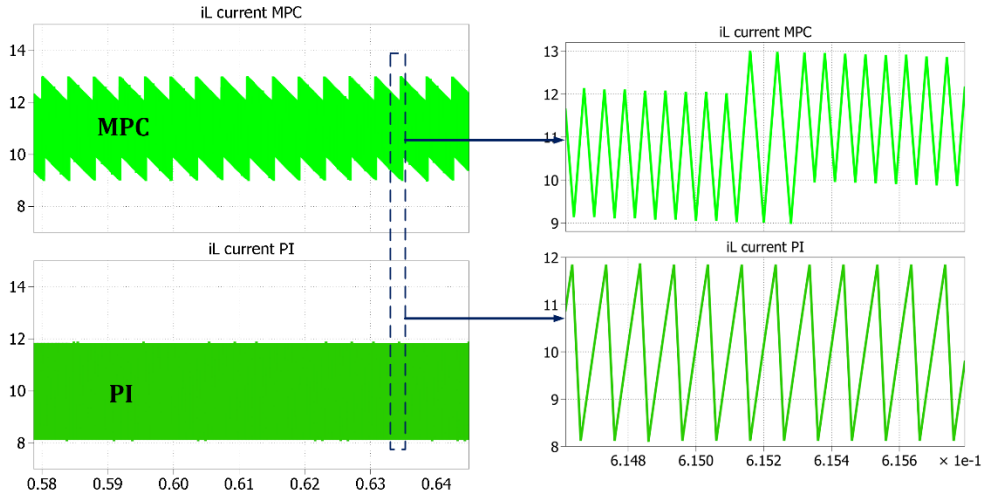
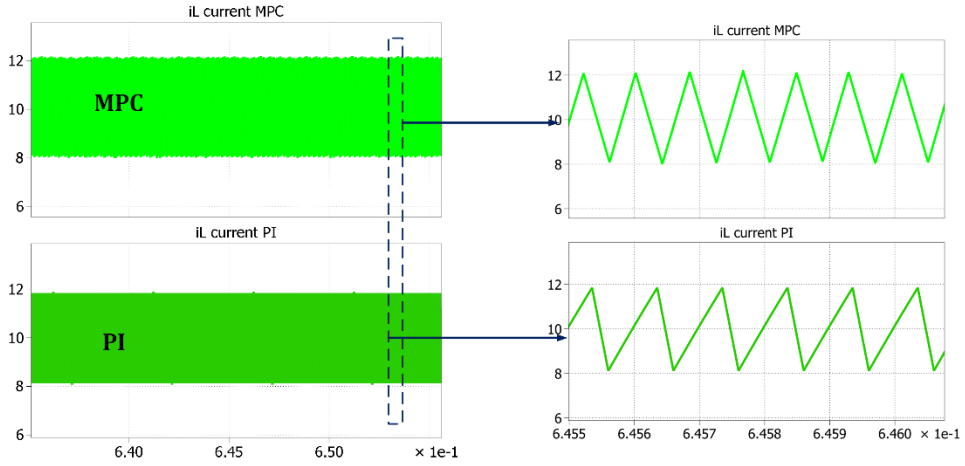


Figure 5.25 Comparison of MPC versus PI structures for flying capacitor voltage control during a voltage balancing transient from 300 V to 400 V.

Switching count reduction in Model Predictive Control (MPC) is achieved by adjusting its weighting factor λ_3. Figure 5.26 compares the performance of Proportional-Integral (PI) control and MPC. It is important to note that the performance of the MPC technique is influenced by the duration of the sampling time. At slower sampling frequency, as shown in Figure 5.26(a), the current control tends to waver. This issue can be resolved by increasing the sampling frequency, as illustrated in Figure 5.26 (b). However faster sampling times will cost the computational burden as shown in Figure 5.27.



(a)



(b)

Figure 5.26 Comparison of 10kHz switching frequency using discrete PI Controller compared to (a) MPC with 10µs sampling time (b) MPC with 1µs high sampling time

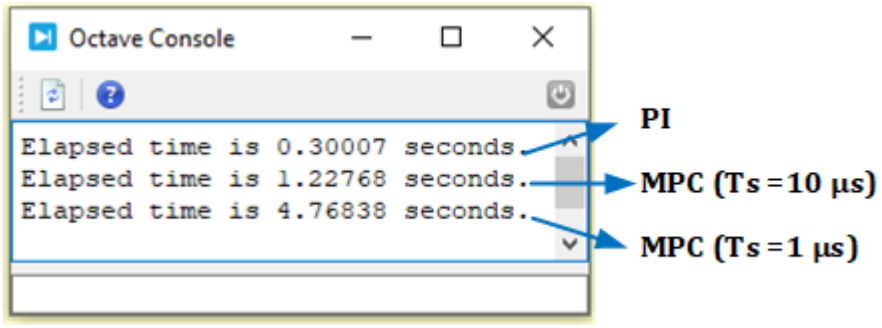


Figure 5.27 The actual simulation time for the three situations shown in Fig 5.24.

Table 5.7 Summary of the comparison between PI Controller and MPC technique applied to the Bidirectional Three-Level DC/DC converter

Comparison	PI	MPC
Performance	Simpler and effective particularly during steady state but has a slower response in handling dynamic system/ transient.	Faster and more precise in handling complex dynamics and non-linear characteristics of converters
Multi-objectives and constraint	Less flexible in multi-objective system, in B3L each controller has its own controller and applied in a cascaded way. Adding more objective and constraint may lead instability	More flexible in terms of handling multi-objective and constraint simultaneously
Sampling time	Longer sampling time	Need much a faster sampling time. A long sampling time may impact controller accuracy
Computational burden	light	heavy
Switching event management	Predetermined using PWM	Adjusted by tuning weighting factor of the switching event or a better option by using continuous control set with modulator

PI controllers represent a mature control system technique that offers steady stability. Multi-objective control could be applied in cascaded way with each control variable needing its own controller. In application to the B3L DC/DC converter, the flying capacitor voltage control was embedded to the output of current control. The switching frequency is constant being predetermined using the carrier signal of PWM. On the other hand, the Model Predictive Control (MPC) algorithm use switching state optimal vector based on predicted minimum cost function. remains open to further development, with potential applications such as the delay compensation and the switching reduction, as previously discussed. Another example of it could also be extended to generate a fixed switching frequency either using a finite or continuous control set [113], [114]. However, this is outside the scope of this thesis. The choice between a PI controller and a Model Predictive Controller (MPC) for DC/DC converter applications is influenced by the particular requirements of the system. PI controllers are straightforward and effective, while MPC offers advanced control capabilities and adaptability to changing conditions at the expense of increased complexity and a faster controller when it comes to application to sampling and calculation. When making a decision, it is essential to consider the trade-offs between simplicity and advanced control based on the specific needs of the DC/DC converter application.

5.3.4 Solar *charging* station of Electric Vehicle

Charging electric vehicles (EVs) using solar panels involves harnessing solar power and energy, storing it and using it to charge the vehicle's batteries. The number and capacity of solar panels depend on factors such as the power and energy requirements of the EV, local sunlight conditions, and available space. Figure 5.28 describes the simplified system of PV-EV charging which will be discussed in this section.

Unidirectional and bidirectional DC/DC converters work as interfaces between the various subsystems. Unidirectional converters function as boost converters to increase voltage from the PV string to a common DC-bus/link, whereas bidirectional converters interface the common DC-bus/link to the station’s main Energy Storage System (ESS) but also may interface to some EVs that allow their battery to be used as energy buffers during long term parking. Solar power

is drawn from PV panels whilst the control system ensures it draws maximum available power. Due to the solar power intermittency, the ESS may store PV energy when PV power is in excess, and it will supply power and energy if there is a shortage of PV power and energy as needed by the EVs and the system. Additionally, the battery of some EVs may also be used to increase the PV energy buffer when needed.

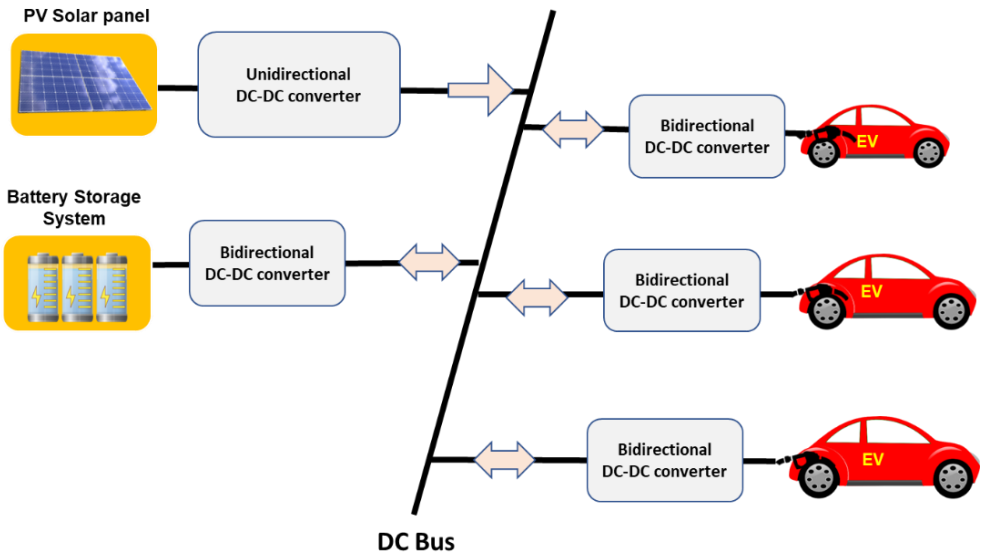
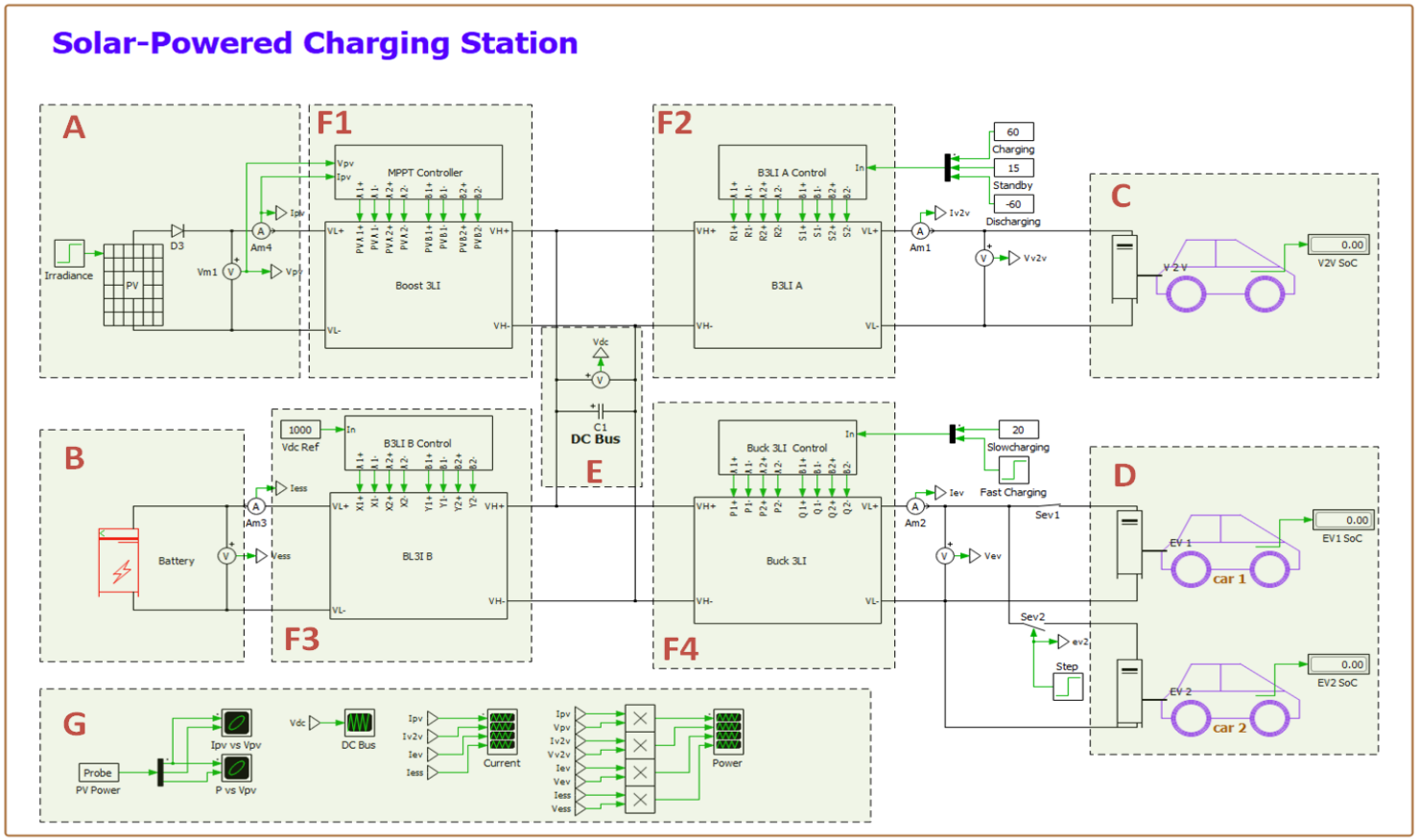


Figure 5.28 Simplified solar-powered charging station system

In chapter 2, it was mentioned that operating DC/DC converters in two-voltage level mode poses challenges in scaling to higher voltage ranges and increases of passive component sizes. This limitation primarily come from the high $^{dv}/_{dt}$ stress imposed on the power semiconductor switch and the insulation of the inductor winding. A potential solution discussed involves using multi-voltage level converter topologies and combining it with the interleaving method to split the voltage and current levels and stresses whilst also allowing a smaller size of passive components to be used in the associated filters. Therefore, in this scenario three-level DC/DC converter will be implemented. Figure 5.29 depicts the overall model of the PV-EV charging station which was modelled using PLECS software version 4.7.5.



A. PV Panel array

B. Battery

C. V2V Car

D. EV Car

E. DC Bus

F1. B3LI with MPPT controller (Boost Operation)

F2. B3LI with current controller (Bidirectional operation)

F2. B3LI with cascade controller (Bidirectional operation)

F4. B3LI with current controller (Buck Operation)

G. Measurement

Figure 5.29 Solar-powered charging station system simulation model using PLECS software.

Table 5.8 Parameters in solar powered charging simulation

Parameters	Symbol	Value	Unit
DC Bus voltage	V_{dc}	800	V
Storage battery voltage	ESS	3.84 x 168	V
V2V Battery : voltage	V_{ld}	3.84 x 168	V
: current	I_{in}	-50 up to 50	A
EV Battery : voltage	V_{ld}	3.84 x 168	V
: current demand	I_{in}	20-100	A
PV Panel MPP : voltage	V_{mpp}	33.2 x 9	V
: Current	I_{mpp}	9.49 x 27	A

The system consists of PV panels modelled according to [29]. In order to find maximum power point which expressed in Equation (5.32), (5.33) and (5.34) where the coefficients C_1 and C_2 depend on short circuit current (I_{SC}), open circuit voltage (V_{OC}), maximum power point voltage (V_{MPP}) and maximum power point current (I_{MPP}.) which is expressed in Equation

$$I_{PV} = I_{SC}.\left[1 - C_1\left(e^{\left(\frac{V_P}{C_2 V_{oc}}\right)} - 1\right)\right] \tag{5.32}$$

Where,

$$C_1 = \left(1 - \frac{I_{MPP}}{I_{SC}}\right).e^{\left(\frac{-V_{MPP}}{C_2 V_{oc}}\right)} \tag{5.33}$$

$$C_2 = \frac{\left(\frac{V_{MPP}}{V_{oc}} - 1\right)}{\ln\left(1 - \frac{I_{MPP}}{I_{SC}}\right)} \tag{5.34}$$

The parameters of the PV panel in Figure 5.29 (A), were replicating the behaviour of LG365Q1C-A5[115]. The system uses a battery energy storage model Figure 5.29 (B) developed in [116], an EV load, and EV that provide V2V feature. Both EV load and V2V EV Figure 5.29 (C) and (D) consist of the same model of Lithium-Ion battery pack emulator[106]. The system is interconnected to DC bus

(Figure 5.29 (E)). The B3LI DC/DC converters serve as interface modules between the various system components as shown in Figure 5.29 (F1-F4).

Various control mechanisms could be applied on the DC/DC converters in the system. The current controller has been implemented for the converter connecting to the EV side to charge or discharge the EV battery. This control mechanism has been discussed previously in section 5.3.2. Typically, the constant current is applied for fast charging until the battery reach 80%[111] .

On the PV panel array side, The Maximum Power Point Tracker (MPPT) controller is working in boost model as depicted Figure 5.30. The MPPT controller is using the incremental conductance algorithm to adjust voltage and current rate of PV input to attain maximum power [117], [118]. MPPT algorithm was developed using state machine block. The method is based on the fact that the slope of the power-voltage (P-V) curve of a PV array is zero at the MPP, positive to the left of the MPP, and negative to the right of the MPP[118]. The method process and diagram can be seen see Appendix 5.2.

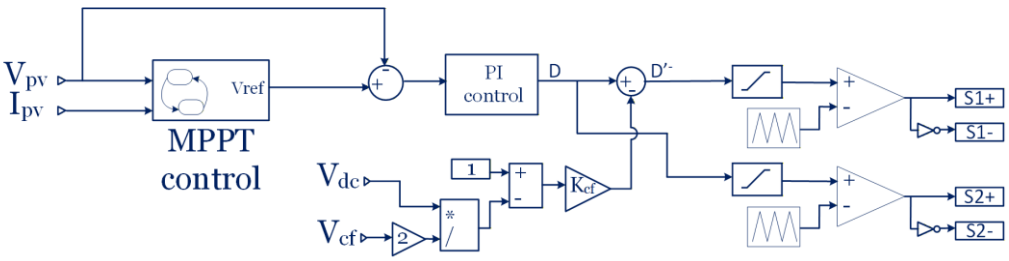


Figure 5.30. MPPT control

A DC link allows system integration by providing a stable and constant voltage level. A DC link in a solar charging station is used as reference to connect multiple solar panels, batteries and load, making it easier to scale the system as needed. The operation of the DC bus voltage is subject to fluctuations resulting from factors such as changes in power demand and irradiation. Therefore, it is necessary to implement specific control measures to maintain the DC-link voltage at a consistent level regardless of the circumstances. This is achieved by applying cascade control on the DC-DC converter that connects the Battery

Energy Storage System (BESS) to the DC Bus. Based on Equation (5.35) and (5.36), the plant transfer function used to maintain DC link voltage utilize $\frac{2}{s\,C}$.

$$E_C = {}^1\!/_2\, C\, V_{dc}^2 \tag{5.35}$$

$$V_{dc}^2 = \frac{2}{C} E_C = \frac{2}{s\,C} P_C = \frac{2}{s\,C}(P_{PV} - P_{ESS}) \tag{5.36}$$

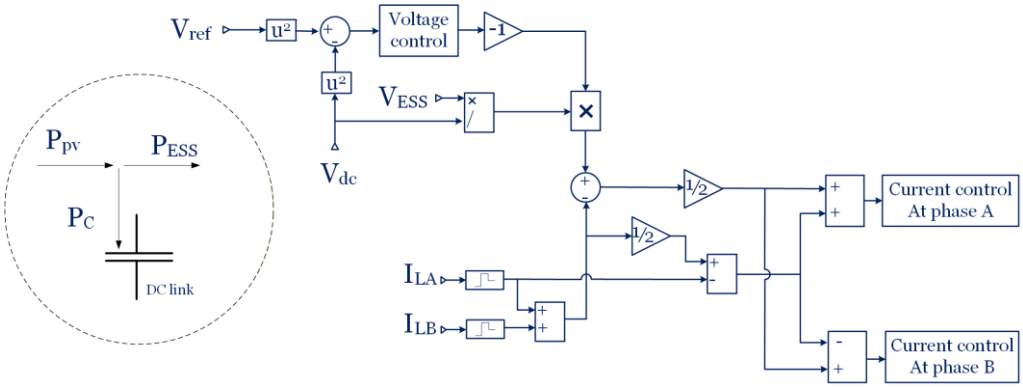
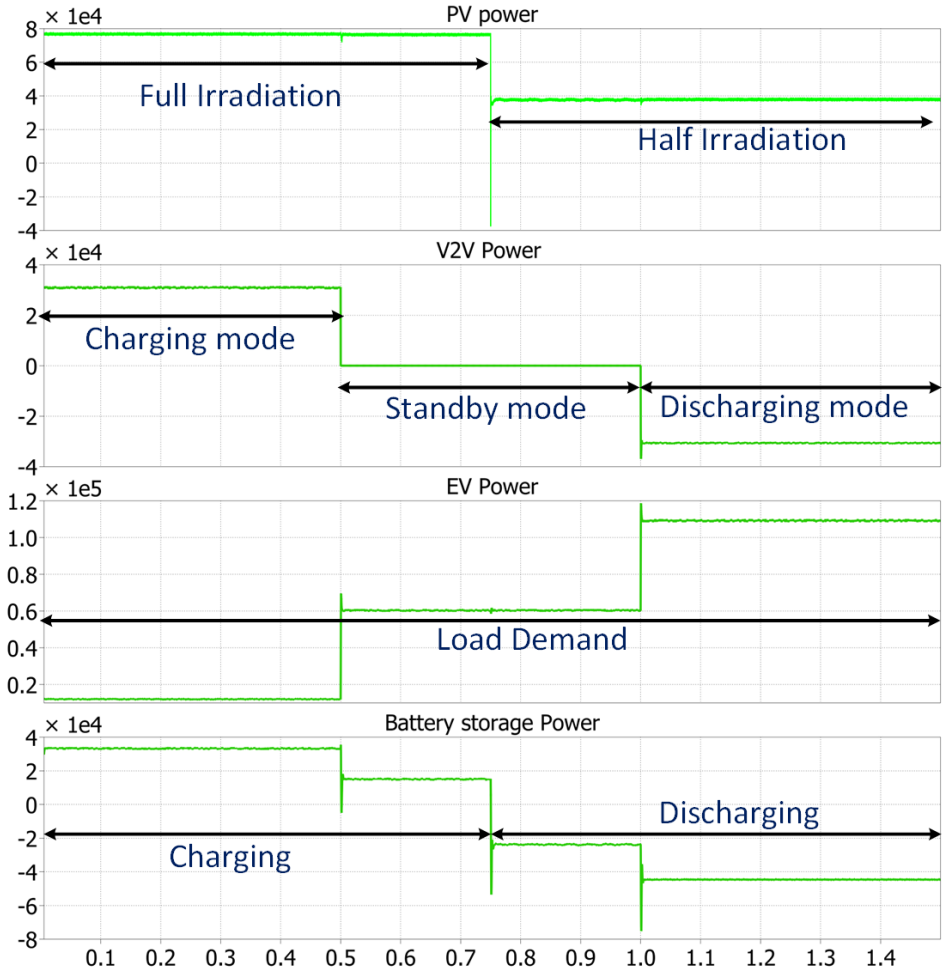


Figure 5.31 Cascade control at ESS

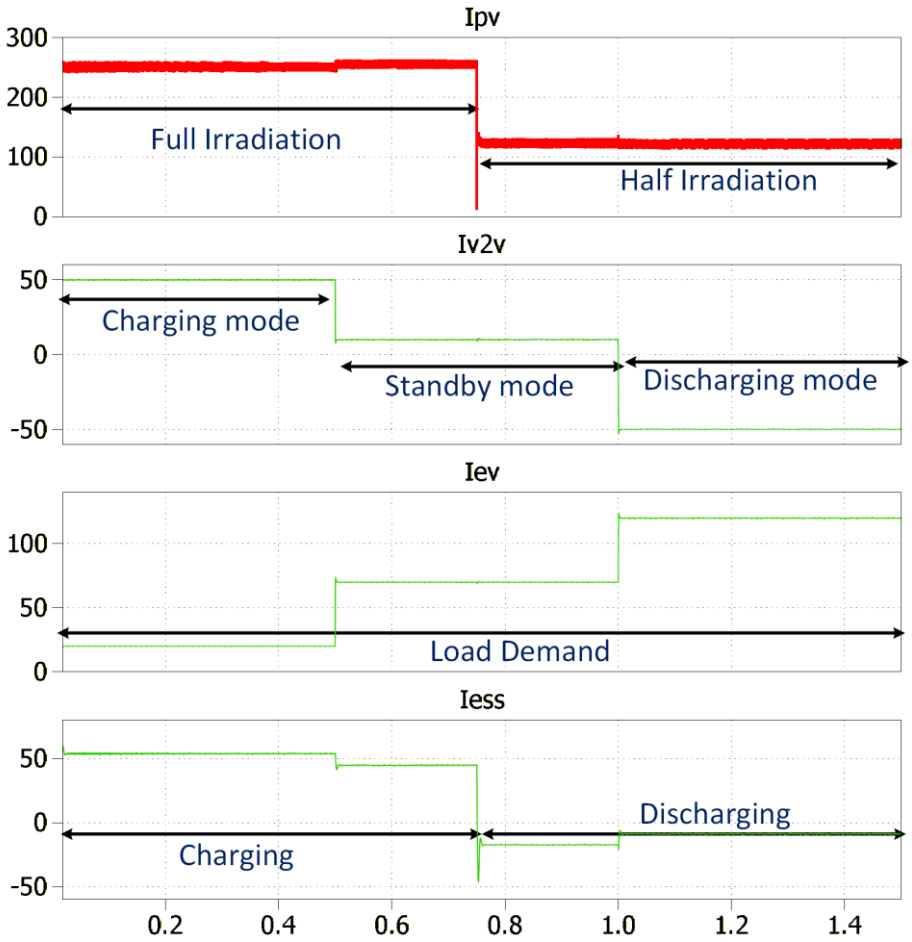
On battery ESS part of the system, the converter operates bidirectionally, enabling both charging and discharging of power while maintaining a constant DC link voltage 800 V. This value becomes the set point of the outer loop. The output of the outer loop is then used to determine the reference current, which becomes the target for the inner control loop.

An example scenario depicted in Figure 5.32 works as follows: firstly, when the photovoltaic (PV) system achieves optimal power (MPPT) production, the PV power is directly supplied to the load and the excess is stored in the battery energy storage system (BESS) or EVs that are available for the vehicle-to-vehicle (V2V) function. Secondly, during periods of increased load demand, the V2V car is placed in standby mode to prioritize charging of electric vehicle (EV) loads that need immediate charging and BESS. Thirdly, when insufficient PV power is generated by the PV panels to fully meet the EV charging demand, the BESS discharges to support the immediate EV charging process. MPPT simulation from full irradiance to half irradiance is shown in Figure 5.33. Lastly, if this is still insufficient to fulfil the immediate EV charging demand, the V2V car are activated to assist in bridging power gaps when high power demand

occurs at the charging station. Figure 5.32 shows the power and current flow during the scenario.

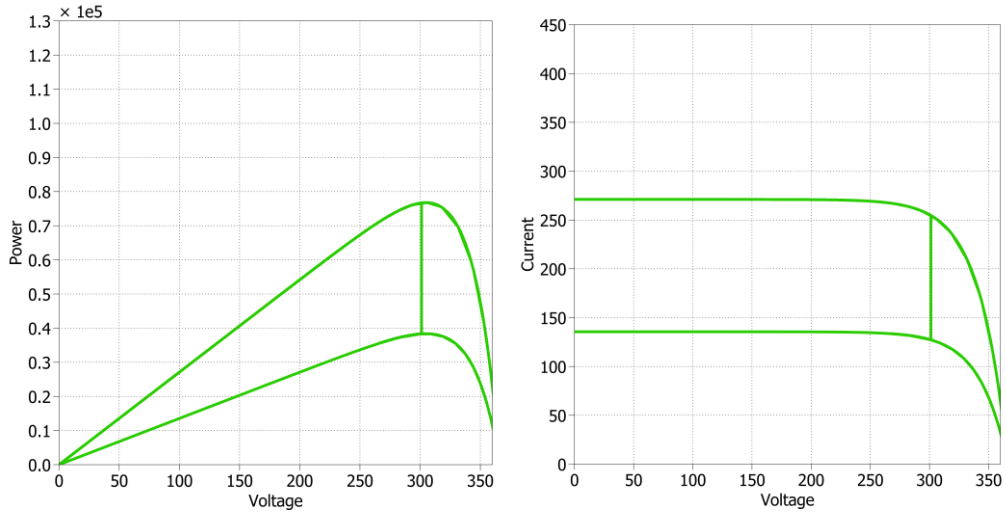


(a)



(b)

Figure 5.32 the charging station operates dynamically based on power availability and demand. When the photovoltaic (PV) system generates maximum power.



(a) (b)

Figure 5.33 MPPT simulation from full irradiance to half irradiance using PLECS software (a) voltage versus power (b) voltage versus current

The DC-link voltage is maintained at a stable level of 800 V asshown in Figure 5.34, serving as the common energy interface between the photovoltaic (PV) array, the ESS, and the battery or electric vehicle (EV) load. Minor voltage fluctuations are observed during transient conditions, primarily caused by variations in solar irradiance, load dynamics. Maintaining a constant DC-link voltage is crucial for ensuring proper power flows between the generation and load sides, as well as for guaranteeing stable and efficient operation of the overall charging station.

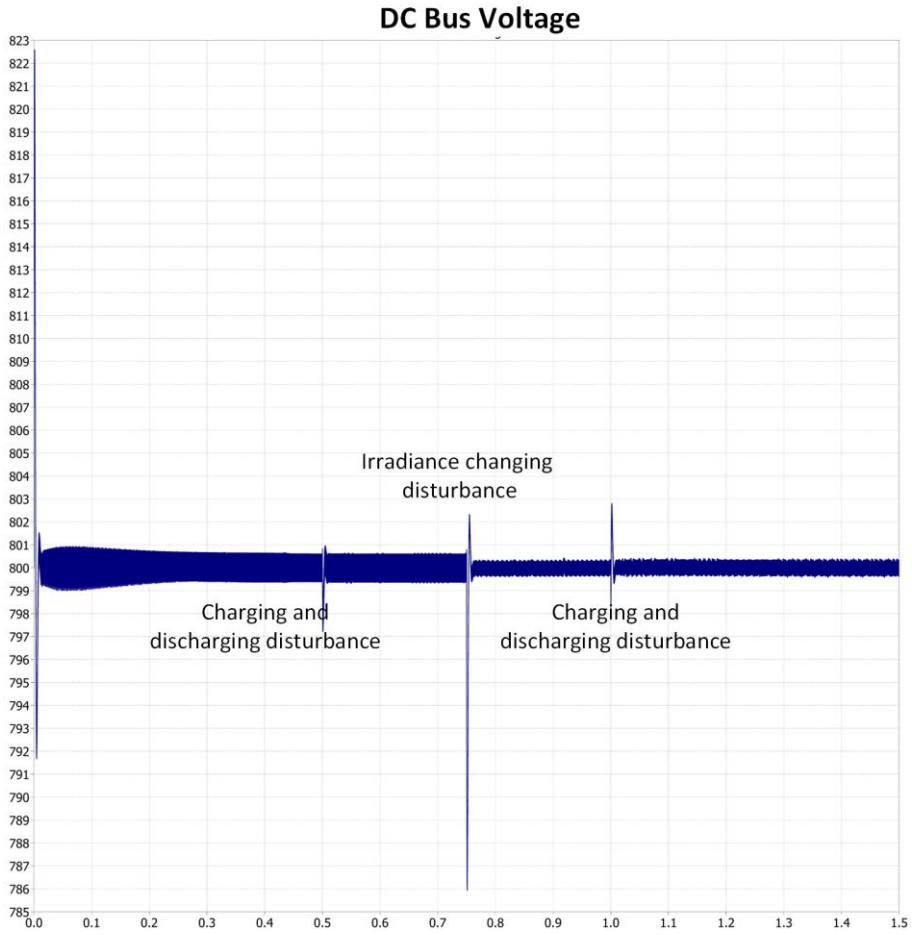


Figure 5.34 DC link voltage during the scenario

5.4

5.4 Summary

A Bidirectional Three-Level Interleaved DC/DC converter with a flying capacitor offers some advantages when charging an electric vehicle (EV) as discussed in Chapter 4. The charging process of an EV is influenced by the specifications of the battery that can be quite different in terms of voltage and amount of recommended charging current in each EV car, making it difficult to create a charger that can accommodate a broad range of currents, voltages, and powers while maintaining high conversion efficiency and low cost/size.

The converter topology choice is utilising the advantages of both the multilevel and interleaved technologies to reduce the size of the magnetics and switching losses. A three-level flying capacitor converter topology, commonly employed in DC/AC applications, is combined with a two-level interleaved implementation, where each switch of the converter only carries half the load current and half the main DC source voltage.

The system controller incorporates phase current equalizing and flying capacitor voltage balancing control to ensure the converter system stability and reliability. The PLECS software is utilised to simulate the proposed converter topology and two control methods and structures. Besides the more established PI control, an alternative control strategy using a Model Predictive Controller is also evaluated. This MPC method exhibits rapid response during transients; however, it requires a faster controller and sampling time for optimal outcomes.

The charging station operates dynamically according to the variations in power availability and demand, requiring a well-designed control strategy to ensure proper power management. Effective coordination between the photovoltaic (PV) generation, battery energy storage system (ESS), and electric vehicle (EV) charging units is essential to maintain power balance and guarantee stable operation under different scenario.

Chapter 6
The Experimental Rig Validation

This chapter describes the laboratory prototype and the experimental evaluation of the power converter that was designed and built to validate the performance and functionality of the proposed Bidirectional Three-Level Interleaved DC/DC converter. The construction and experimental evaluation of this prototype represents the assessment of the thesis main objective.

This chapter provides details regarding specifications of the power converter prototype and its control structure which includes the control platform comprising the TMS320C6713 evaluation DSP board, the FPGA board in charge of producing the PWM pulses and the analogue to digital convertors and the host port interface (HPI) daughter card. Additionally, the boards implementing the sensors for the measurements of key voltage and current signals are discussed. Following the description of the control system, the implementation of the power stage is described including the choice of passive components and gate drivers. Then the initial tests showing the basic functionality of the converter is shown followed by the extensive evaluation of the prototype performing bidirectional DC charging functionality as following:

- To evaluate the B3LI DC/DC converter operation principles that were described in the theoretical and simulation chapters.
- To verify the converter's ability to evenly distribute voltage and current stresses among all the switches in all key operating points. The results of the analysis can then be used to determine whether the converter is capable of handling the specified rated current within the full voltage range without

experiencing any overload conditions. This analysis can also be used to identify any potential design restrictions that may need to be addressed to improve the performance of the converter.

- To confirm the effectiveness of the control performance in delivering a specific reference parameter, including maintaining the flying capacitor voltage and distributing evenly the load current among the leg inductors.
- To assess the efficiency curve of the converter in delivering a wide range of powers at certain output voltage and current levels.

6.1 Design consideration for the experimental rig

This section focuses on presenting the theoretical design of the lab prototype. The simulation study presented in Chapter 5 considered a full size solar charging station which was based on a Bidirectional 3-Level Interleaved DC/DC converter with voltage and current rating of 800 V and 100 A, respectively, at the output, so that the converter produced a power of 60 kW. This full-size charger is however impractical to be built in the lab, therefore it was chosen to prototype a scaled down prototype (reduced current) which is considered sufficient for validating the converter operation principles. The converter prototype was chosen to have same maximum DC bus high-voltage rating as in the simulation, of 800V. This voltage level can support recent EV battery voltage either for 800 or 400 V architecture (appendix 2.1). However, the current is scaled down to 8A on the output side, resulting in a rated power of 6.4 kW. The circuit design process remains the same as detailed in the simulation Chapter 5. Based on this requirement, the components were sizing as in Table 6.2

Table 6.1 B3LI DC/DC converter requirement for experimental rig

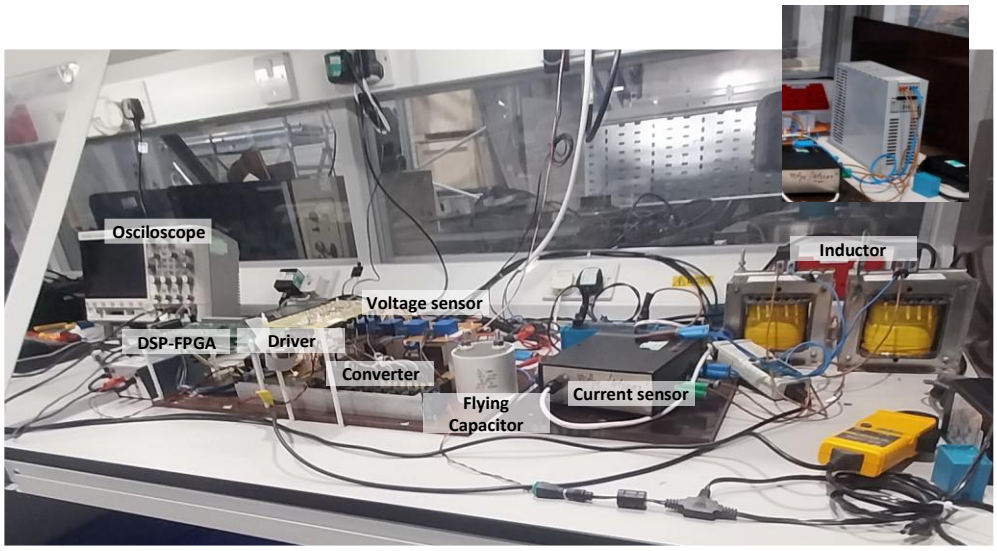
Parameters	**Symbol**	**Value**	**Unit**
High side voltage range	V_{dc}	400-800	V
Low side voltage range	V_{ld}	200-700	V
Load current	I_{ld}	0-8	A
Power	P	0-6	kW
Switching frequency	f_s	5000	Hz

Table 6.2. Component sizing and adjusted value for experimental work

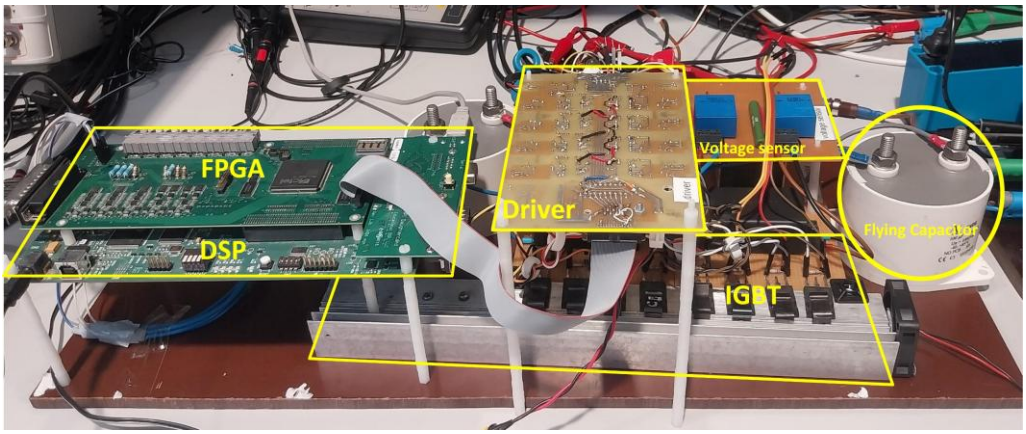
Component	Formula	Value	Unit
Inductor			
- Current , I_{phase}	$\frac{1}{2} I_{ld}$	4	A
- Current ripple, Δi_{phase}	10-40%	0.4-1.6	A
- Size	$\frac{V_{dc}}{2} \frac{0.0625}{\Delta i_{(phase)}\ f_s}$	3.1- 12.5	mH
Flying capacitor			
- Voltage, V_{cf}	$\frac{1}{2} V_{dc}$	400	V
- Voltage ripple, ΔV_{cf}	2 % V_{Cf}	8	V
- Size	$\frac{1}{2} \frac{I_{ld}}{\Delta V_{cf}\ f_s}$	50	µF
Load capacitor			
- I ripple max, ΔI_{CH}	Δi_{phase}	1.6	A
- V ripple, ΔV_{CH}	1 % $V_{Load\text{-}min}$	2	V
- Size	$\frac{\Delta i_{phase}}{16 \times f_{sw} \times \Delta V_{CL}}$	10	µF
DC bus capacitor			
- V ripple, , ΔV_H	1% V_H	8	V
- Size	$\frac{0.25\ I_L}{\Delta V_{cH}\ f_s}$	50	µF
Switches			
- Blocking voltage	$\frac{1}{2} V_{dc} \times 150\%$	600	V
- Current	$\frac{1}{2} I_{ld} \times 150\%$	6	A

The implementation of the 6 kW/800V test rig is shown in Figure 6.1. The main components of the converter test rig include the DC/DC converter prototype power stage, the DSP-FPGA control system and an array of voltage and current measurement sensors. The power supply unit is Delta Electronica SM1500-CP-30 which supply DC power to the system. Together with power resistor bank, both were used to provide a specific range of testing scenarios, including varying output load conditions and DC bus voltages..

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(a)



(b)



(c)

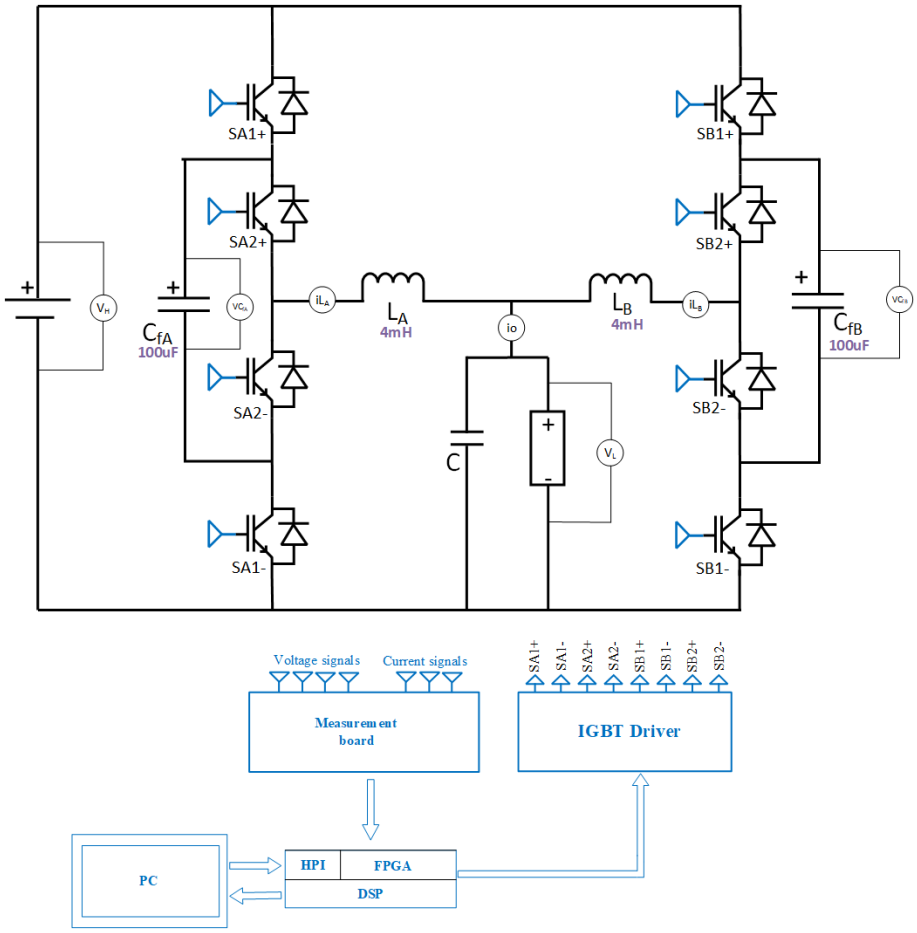


(d)

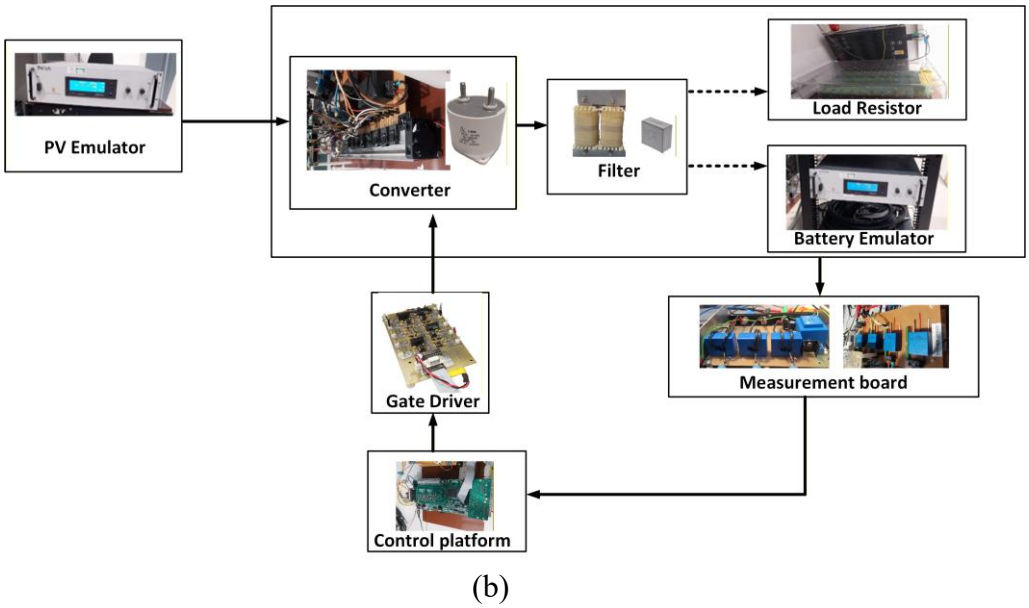
Figure 6.1. Photographs of (a) The test rig (b) The experimental converter prototype (c) power supply (d) load resistors

The block diagram of the DC/DC converter prototype is depicted in Figure 6.2. The power stage has an identical schematic as in simulations modelled in Section

4.1 . For the unidirectional operation, a load resistor is connected at the output to serve as the load as in Figure 6.2.(b). For the bidirectional operation, two bidirectional power supplies are employed to enable power flow in both directions. The primary control system is the DSP-FPGA shown in Fig 6.1b, which governs the operation of the full system. The control signals are directed to the gate driver board to ensure the proper generation of the gate signals voltage levels as required by the IGBT switches of the converter. The relevant voltage and current signal from the converter are acquired through a measurement board and subsequently fed back to the controller through the FPGA board. A detailed discussion of the signals is presented in the following sections of this chapter.



(a)



(b)

Figure 6.2 The experimental system prototype (a) schematic (b) block diagram.

6.1.1 Power converter design

For building the 3-level Interleaved DC/DC Converter, eight (4×2) IXYS discrete IGBTs type IXA17IF1200HJ [119], were used. This IGBT has a built-in antiparallel diode and has an isolated package (ISOPLUS) that allows for all switches to be mounted on same heatsink therefore making the development of the prototype easier. The IGBT switch is rated at 1200V /18 A at 80ºC. This rating is twice higher than required to make sure it can withstand potential overloads typical for prototype development. A photograph, of the IGBT switch, its internal schematic and arrangement of all switches of the power stage on heatsink are shown in Figure 6.3.



(a) (b)



Figure 6.3 IGBT switch (a)photo, (b)schematic (c) and heatsink arrangement of switches in circuit.

The converter leg consists of four switches interconnected with a 100uF/1000 V film type flying capacitor. Figure 6.4(a) shows the film capacitor C4DENPQ6100A8TK from C4DE, which was used in this experimental work. The capacitor was connected between the middle, upper, and lower switches to build a three-level flying capacitor converter leg. Figure 6.4(b) is the 10 μF/900V load coupling capacitor. Figure 6.4 (c) and (d) show the coupled and discrete inductor. The self inductance of the inductor is 4.3 mH and can reach maximum current 8 A. While the discrete inductor is 15mH and has maximum current 15A. Both were used during the experimental work. Figure 6.4 (e) shows the power load which were used for unidirectional operation.

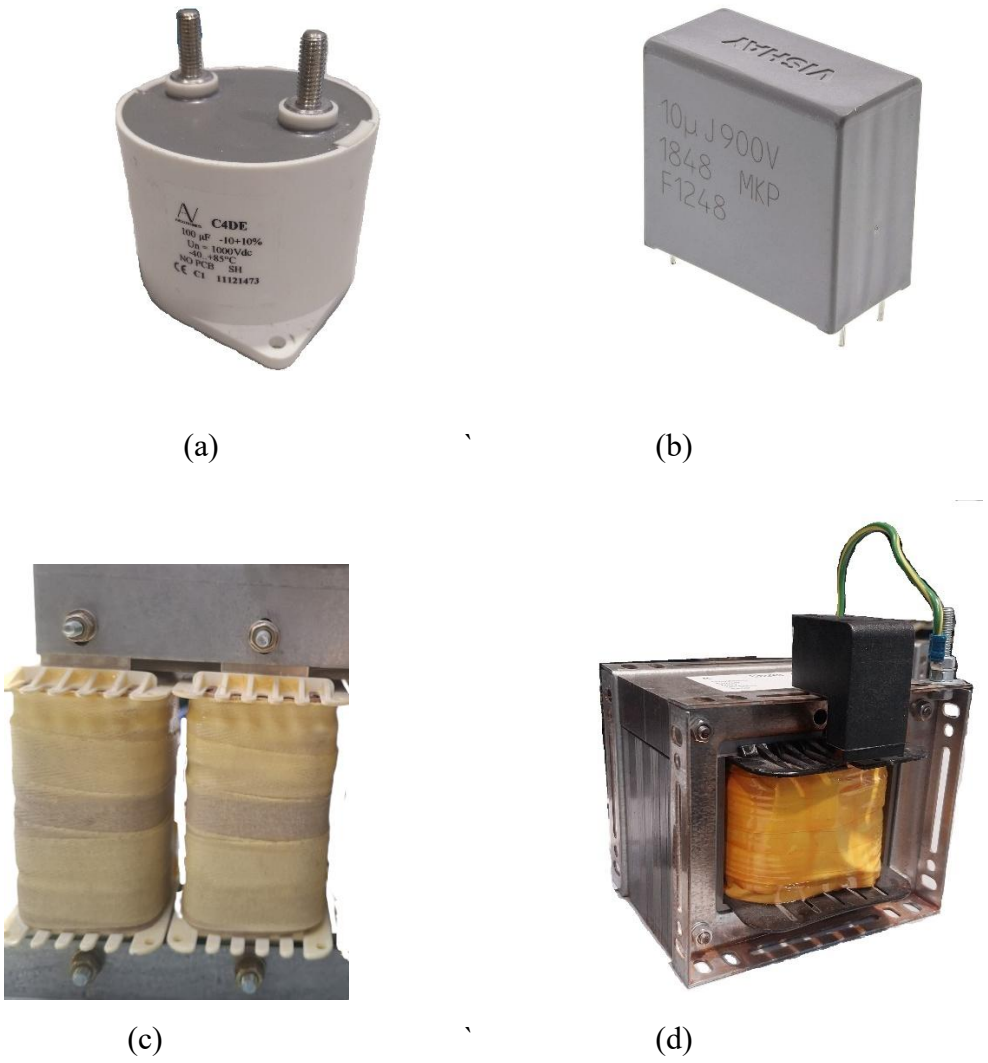


Figure 6.4. Photo of components (a) flying capacitor, (b) load coupling capacitor, (c) coupled inductor, (d) discrete inductor.

6.1.2 Measurement board

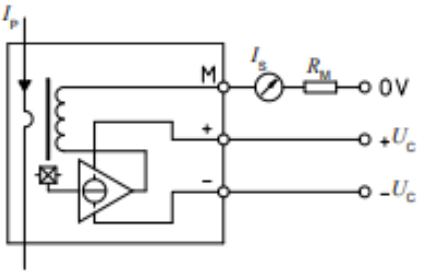
The current and voltage sensor measurement block were built using LA 55-P[120] and LV 25-P [121] transducers which are popular for their linearity and accuracy. These transducers employ the Hall effect current sensors used in a closed loop configuration. Figure 6.6 (a) shows the current sensor LA 55-P and its connection. The sensor delivers on the output the current flow with a ratio of 1:1000 of input main current.

Figure 6.6 (b) presents a photograph and schematic of the LV25-P voltage transducer. This sensor is capable of measuring DC, AC, and pulse voltages. It features galvanic isolation between the primary circuit (which operates at a high

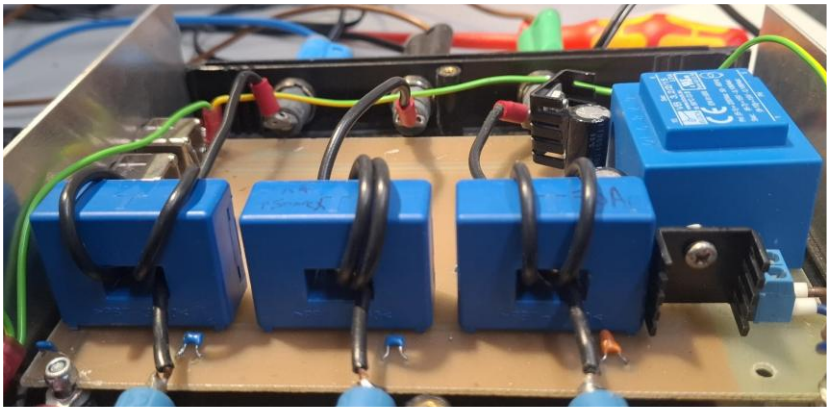
voltage) and the secondary circuit voltage (which is the measurement). An additional 100kΩ/10W external resistors is needed for voltage measurement up to 1000 V. The current flowing through the primary additional resistor is proportional to the measurement voltage. A measurement resistance is used in the output to convert the current into a voltage. A +15/0/-15 V voltage supply is required to power both the current and voltage transducers.



(a)



(b)

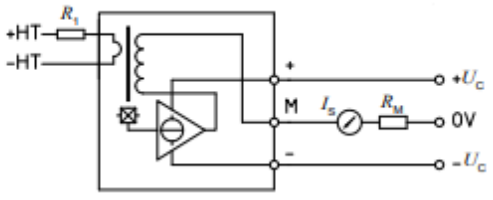


(c)

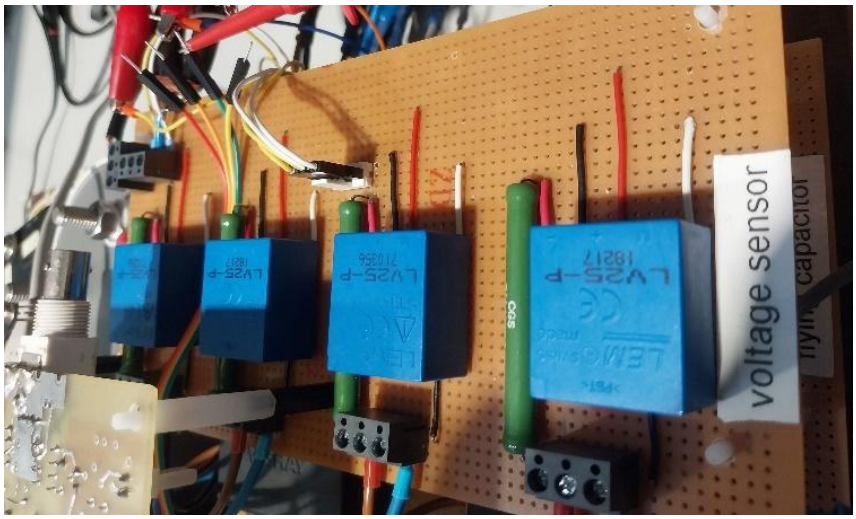
Figure 6.5 Current measurement using LA-55 (a)single picture (b) schematic (c) board



(a)



(b)



(c)

Figure 6.6 Voltage measurement using LV25 (a)photograph (b)schematic (c) board

The voltage measurement board consists of four voltage sensors that are allocated to measure the high side DC-bus voltage, the low side load output voltage, and the two flying capacitor voltages. Three current sensors were used in the current measurement board to measure the two converter legs currents and the total load current.

6.1.3 The control platform

The control platform was a Texas Instruments C6713 DSK DSP evaluation board that works in conjunction to an FPGA board developed by UoN, and a host port interface (HPI) daughter card, as depicted in Figure 6.7. Operating at a clock frequency of 225 MHz, the DSP utilizes a 32-bit wide External Memory Interface, shared with the FPGA board and an HPI daughtercard.

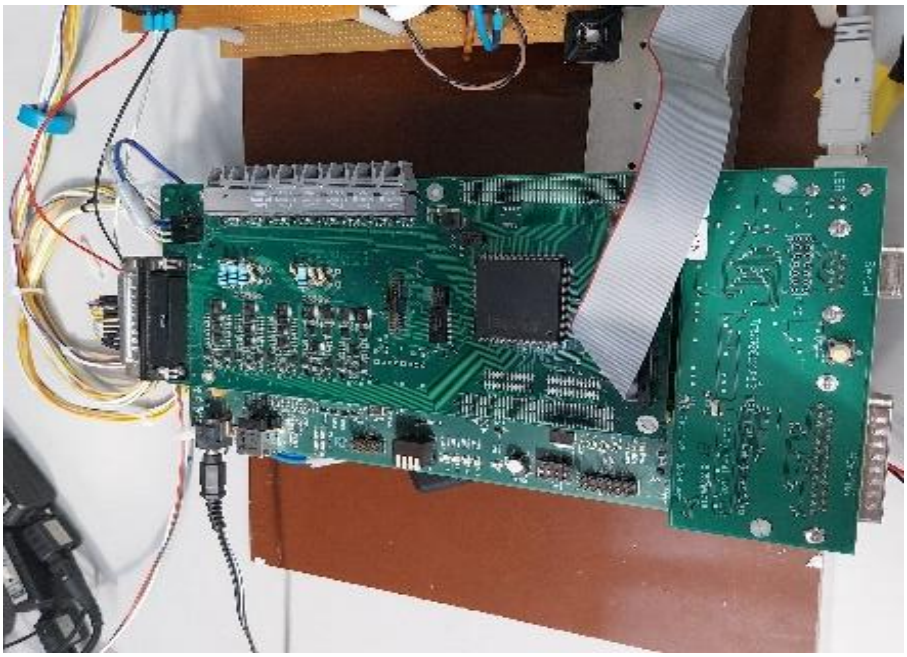


Figure 6.7. TMS320C6713 DSP and FPGA control platform

The control algorithm was implemented in the C language which serves the primary function of determining the duty cycles signal prerequisites for converter switching. Programming the DSP is accomplished using Code Composer Studio (CCS), an integrated development environment (IDE) for Texas Instrument's microcontrollers which include C compiler.

The Host Port Interface (HPI) is a parallel port that allow a host processor to directly access the CPU memory space [122]. HPI daughtercard establishes a communication and facilitate code transfer to the HPI on DSP. Furthermore, this daughtercard enables data exchange between the DSP and the host PC. The interaction between DSP the host PC facilitates real-time monitoring and plotting of the DSP program variables which are displayed with MATLAB Graphic User Interface (GUI).

The FPGA board was built by the Power Electronics, Machines, and Control Group (PEMC) Research Group at the University of Nottingham. It used the ProASIC3 chip. This FPGA board is equipped with connectors that facilitate data exchange between the FPGA and the DSP. Additionally, it hosts several analogue-to-digital converter (ADC) reading channels, supporting up to ten channels. In this configuration, a single FPGA board suffices because the system

requires only seven feedback measurement signals, which is less than the available capacity of ADC channels. The FPGA can be triggered by configuring trip limits for these ADC channels. If any of the ADC channel measured values surpass their respective threshold levels, a trip signal will be transmitted to the FPGA, subsequently leading to deactivation of the PWM signals, ensuring a responsive safety mechanism., as well as optical transmitters, interrupt period control, and trip monitoring functionalities.

6.1.4 The gate driver board

The IGBTs are controlled by the gate driver signal to turn them on and off as shown in Figure 6.8. The gate driver circuit power is provided from a 5 V power supply which has galvanic isolated $\pm$15 V outputs using the NMA0515SC DC/DC converter [123], [124]. The $\pm$15 V output voltage from this DC/DC converter is connected to the optocoupler gate driver HCPL3120 [125] which provide large peak currents needed during the switching moment.

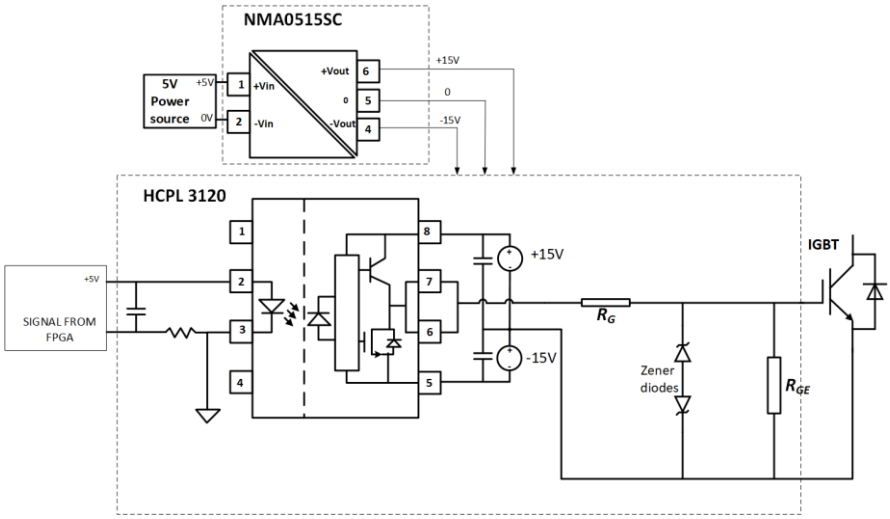
HCPL3120 receives the PWM signal from the FPGA whilst isolate it to protect the controller board from any dangerous voltage levels or incoming surge of high voltage from the power circuit. The dead time to protect the circuit from shoot through was implemented in the FPGA.

The 10 Ω gate resistance, R_g is placed directly in the path between the gate of the IGBT. It is used to controls the switching speed of the IGBT. A higher R_g slows down the switching process, reducing the rate of change of voltage (dV/dt) and current (di/dt), which helps in reducing and overvoltage spikes [126].

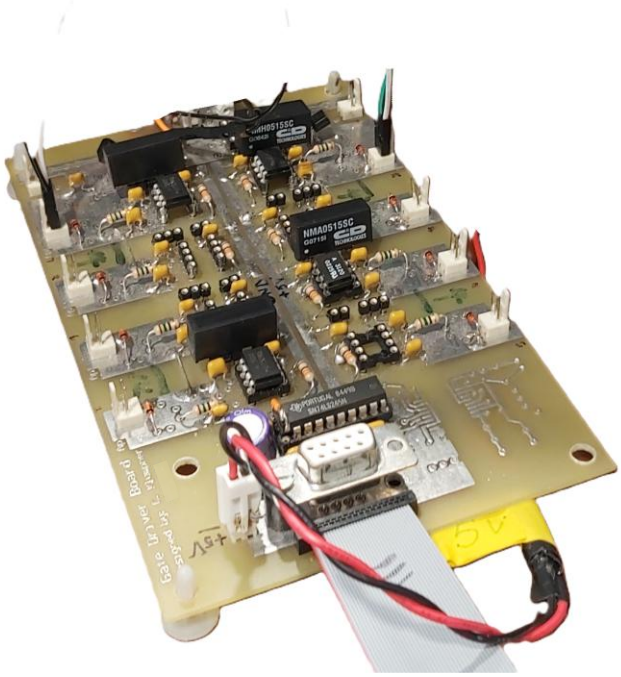
A 10kΩ gate-emiter resistance, R_{ge} is placed between the gate and emitter terminals of the IGBT. It helps with stability, false triggering and damping oscillations when the IGBT is off [127]. However, the drawback of the R_{ge} resistance is that it results in longer switching times.

Two Zener diodes, each with a breakdown voltage of 18V[128], are connected back-to-back, in reverse orientation with respect to each other, to provide protection against overvoltage in both directions. Each Zener diode clamps the voltage when it exceeds the Zener breakdown voltage, whether the surge is positive or negative. The voltage will be clamped to (+18V) in the positive direction and -18V in the negative direction, protecting the circuit from

excessive voltages. The Zener diode can introduce additional losses during switching. however, this is less significant in IGBT, which operate at low dV/dt.



(a)



(b)

Figure 6.8 The gate driver circuit (a) schematic (b) board

6.2 Experimental Results

The experimental parameters of the prototype are listed in Table 6.3. The DC bus (high-side) and output (low-side) voltage and inductor current ranges were the main parameters used to study the behaviour of the converter. For data recording of the experimental voltage and current waveforms, a 200-MHz 4-channel Keysight oscilloscope with differential voltage probes and current probes was used. The experimental result state variables as acquired and processed by the DSP control system were captured via MATLAB, which was interfaced with the DSP via the HPI.

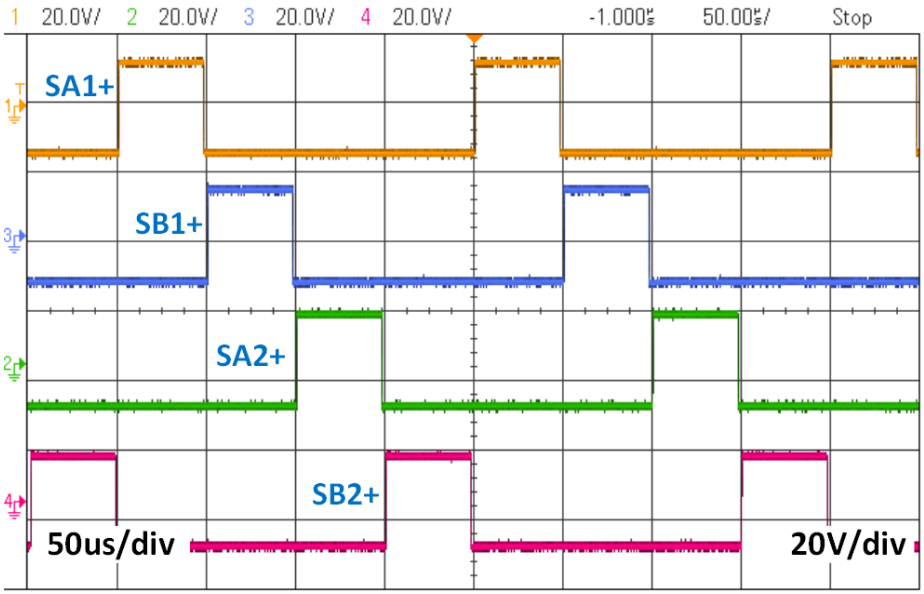
Table 6.3. Adjusted circuit parameters for the converter prototype

Parameters	**Symbol**	**Value**	**Unit**
High side voltage range	V_{dc}	0- 800	V
Low side voltage range	V_{ld}	200-700	V
Inductor current	i_L	0-8	A
Power	P	0-6	kW
Switching frequency	f_s	5000	Hz
Leg Inductor	L		mH
- Coupled Inductor			
Size		4.32 and 4.4	mH
Coupling coefficient	k	0.364	
Mutual Factor	M	1.6	
- Discrete Inductor			
Size		15	mH
Lowside capacitors	C_L	2 x10	µF
Flying Capacitor	C_f	100	µF

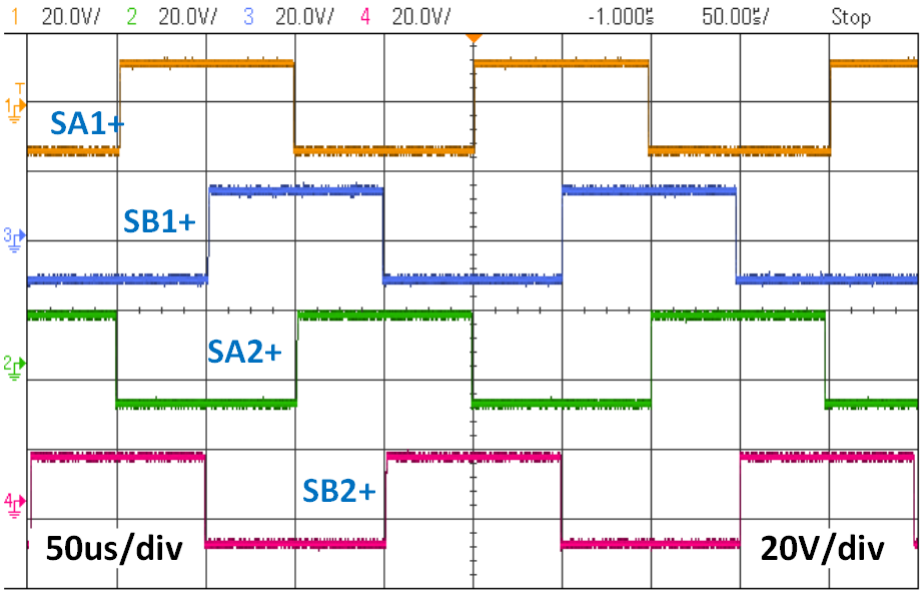
6.2.1 Switching signal and voltage and response

Figure 6.9 depicts the $\pm$ 15 V gate switching signal generated by the gate driver to turn the power IGBT devices on and off. Eight gate drivers are used in total, which equals the number of IGBTs. Figure 6.9 shows upper from top to bottom the gate signals for SA1+, SB1+, SA2+ and SB2+.

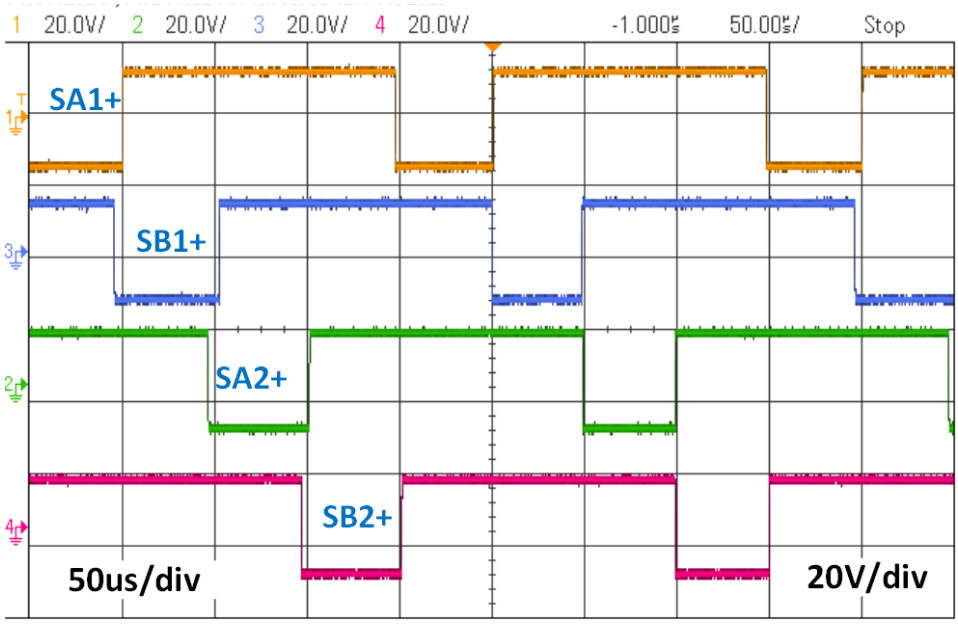
The duty cycle is expressed as a percentage, representing the fraction of time the switch is on. Figure 6.9 (a), (b) and (c) shows duty cycles of 25%, 50% and 75% respectively. It directly influences the output voltage and current characteristics of the converter. The dutycycle implicitly illustrated the state of operations. For instance, when SA1+ and SA2+ is on at the same time, indicate the direct power transfer between high side and lowside while if SA1+ on and SA2+ is off pointing the flying capacitor is involved during power transfer. The phase of the switches on the second leg were shifted by 90 degrees to create current ripple cancellation in inductor because the frequency of the inductor is twice the switching frequency.



(a)

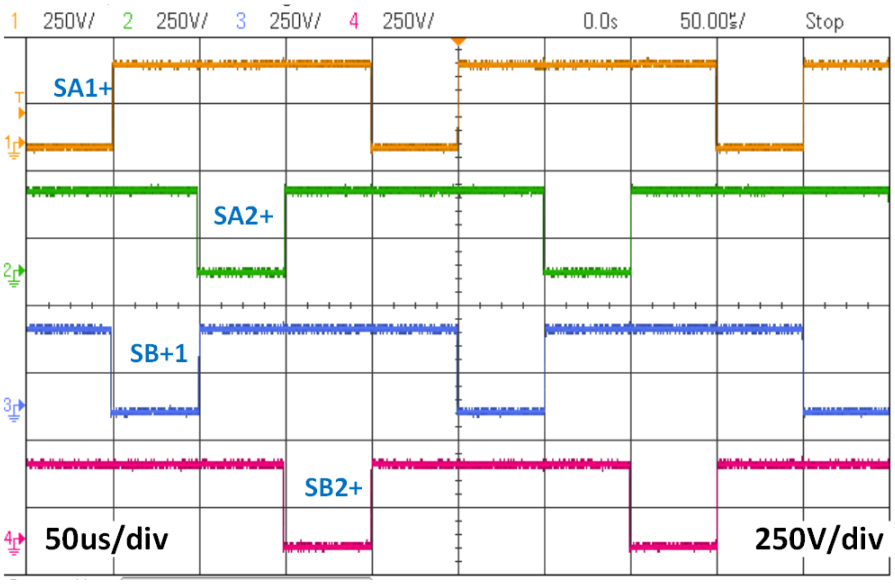


(b)

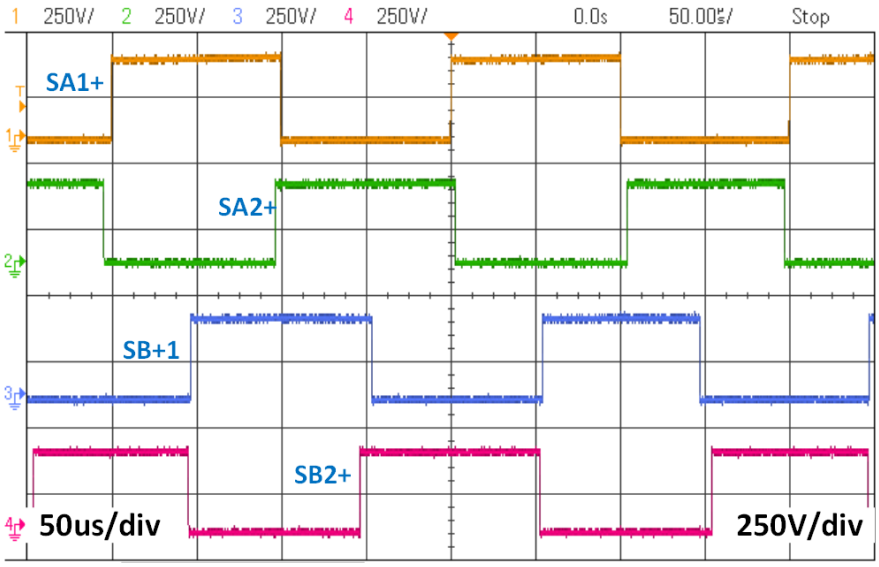


(c)

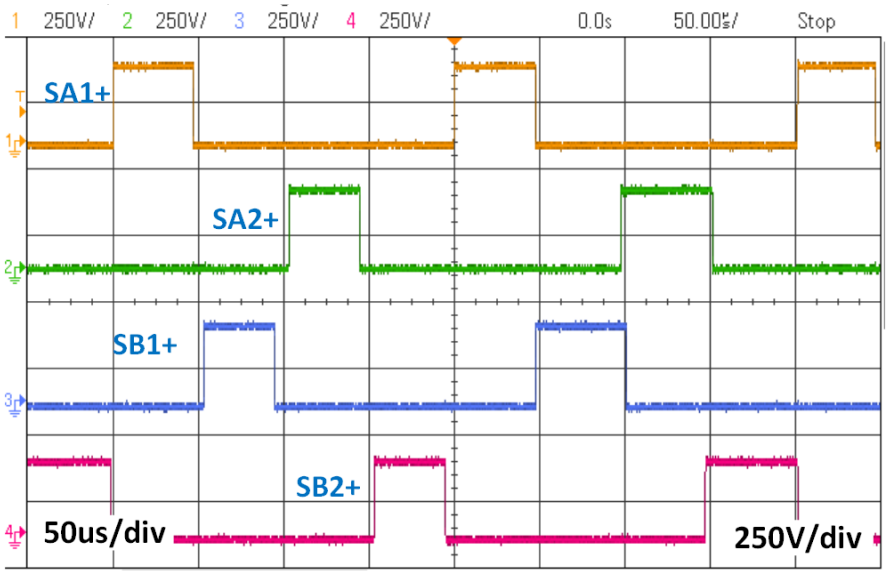
Figure 6.9 Gate driver signals for upper devices with duty cycle (a) 25%,(b) 50%, and (c) 75%


1 250V/ 2 250V/ 3 250V/ 4 250V/ 0.0s 50.00%/ Stop
SA1+
SA2+
SB+1
SB2+
50us/div
250V/div

(a)


1 250V/ 2 250V/ 3 250V/ 4 250V/ 0.0s 50.00%/ Stop
SA1+
SA2+
SB+1
SB2+
50us/div
250V/div

(b)



(c)

Figure 6.10 Upper IGBT voltage with voltage transfer ratio (a) 25%, (b) 50%, and (c) 75%

The gate-driving scheme is similar to that of a traditional two-phase buck converter. A complementary signal drives the outer switches, S1A+ and S1A-, with duty cycle $D = V_{ld}/V_{dc}$. A second complementary signal of equal duty cycle drives the inner switches, S2A+ and S2A-, but is phase-shifted from the outer switches signal by 180 degrees. According to its datasheet [108], IXA17IF1200HJ IGBT has turn on and turn off delays of 70ns and 250ns respectively, Figure 6.11. shows 2us dead time is applied to prevent simultaneous conduction, which could lead to a short circuit across the power supply (shoot-through).

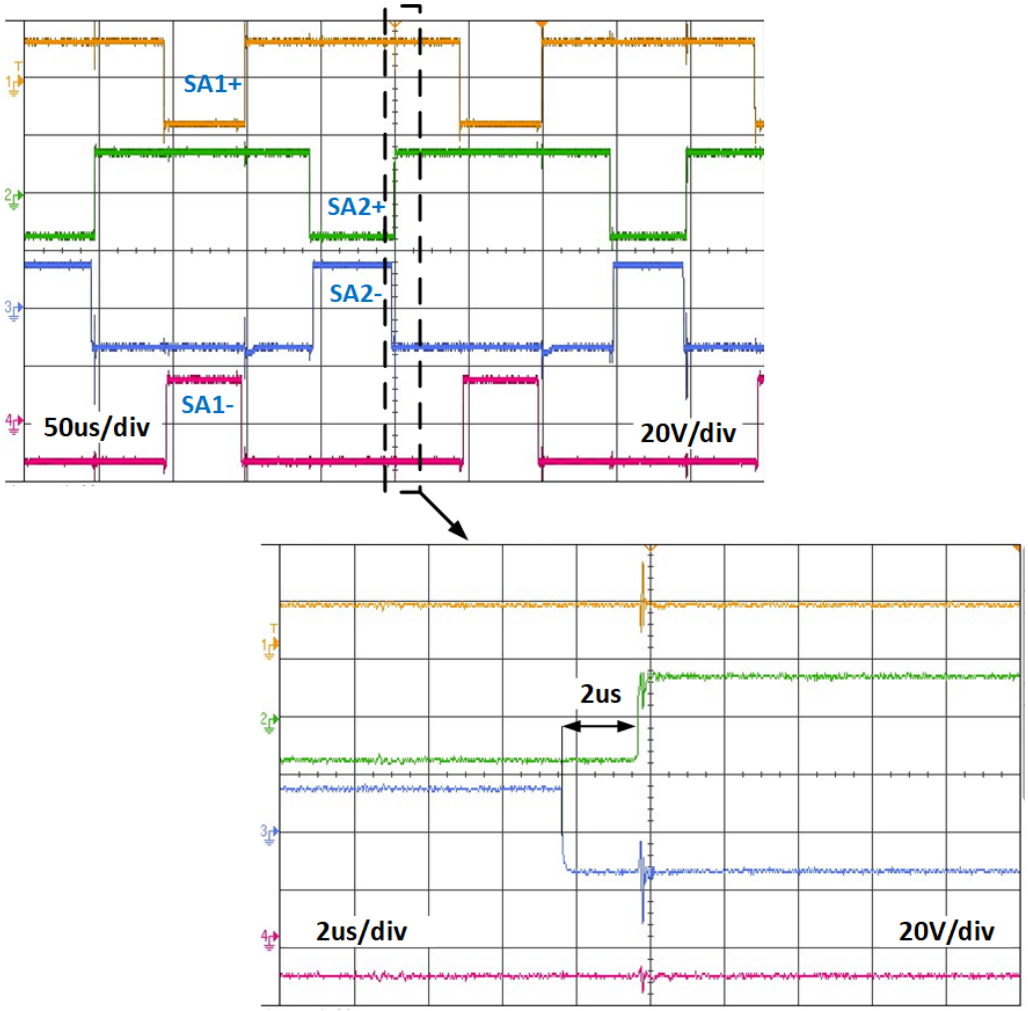


Figure 6.11 Voltage measured across the two complementary IGBT gates revealing the deadtime

Figure 6.12 depicts the CE voltage across the IGBT switches for one inverter leg with a 800V DC link voltage. As can be observed that all the switches are blocking only half of the DC link voltage. Additionally, the arrow in Figure 6.12 highlights a slight increase or decrease in voltage caused by the charging and discharging of the flying capacitors.

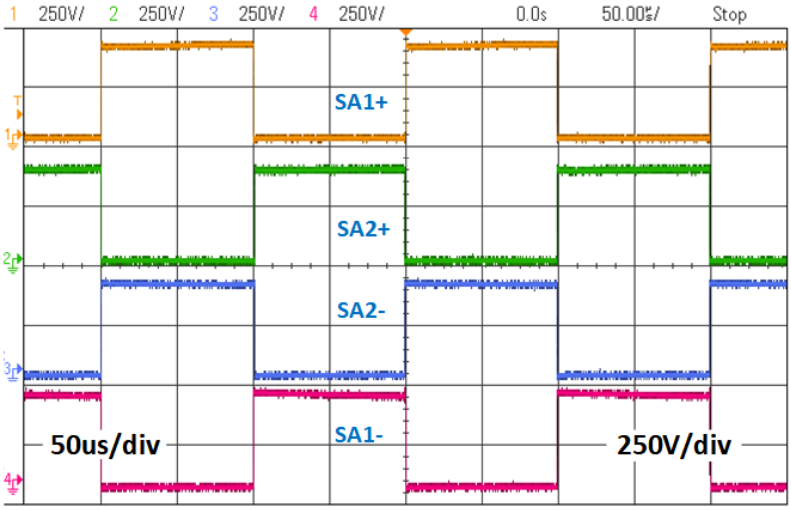
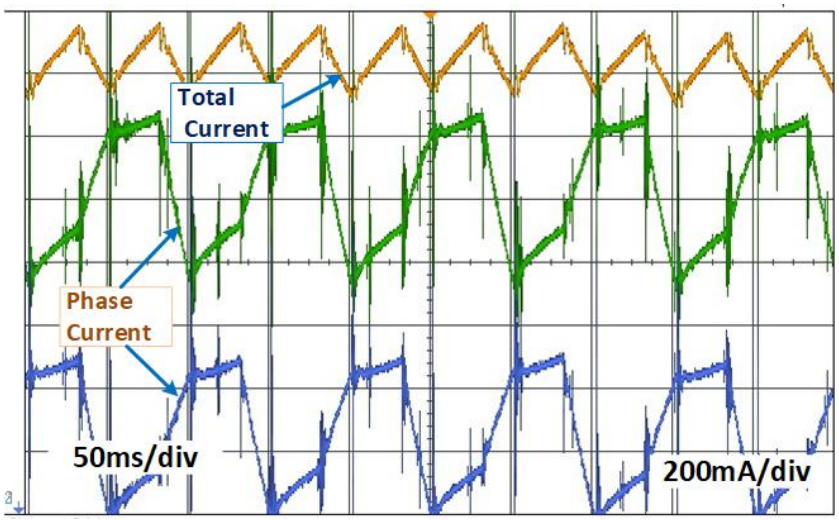


Figure 6.12 The collector-emitter IGBT voltage of the upper four converter leg switches operating with 800V bus voltage, 50% dutycycle and 8 A load current.

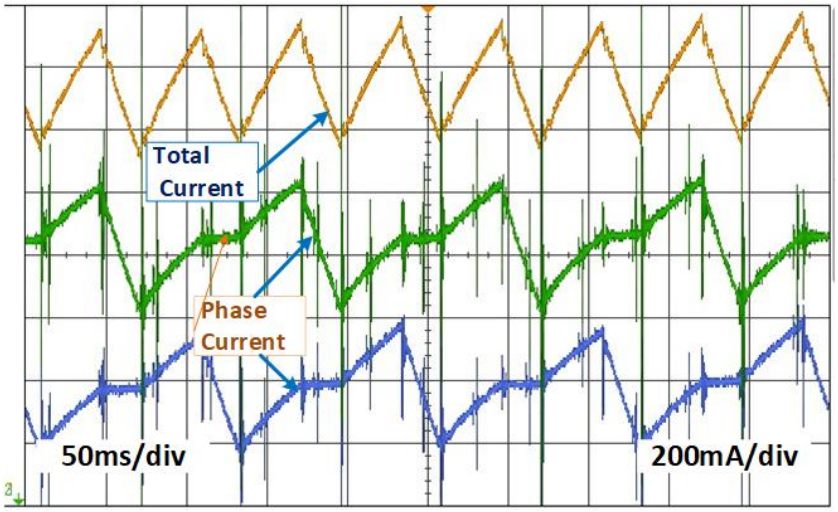
6.2.2 The inductor and total load currents

In the design of DC/DC converters, the selection of passive components, particularly the output inductors, play a key role in determining the overall performance and efficiency. A larger inductor can store more energy and smooth out the current more effectively, reducing the ripple current however, choosing a large inductor lead of slower response times apart from the increase cost.

The experiment involved two setups, one using a 4.3 mH coupled inductor with partial magnetic coupling between its windings, and another employing two 15 mH discrete inductors. The inductors positioned on the load side. When the coupled inductor uses direct connection, the ripple currents on the channel add-up, leading to larger ripple currents on the channel but improved ripple cancellation at the output, as shown in Figure 6.13.a. While the inverse connection results in lower ripple on the leg, though the cancellation at the output is less effective, as depicted in Figure 6.13.b. The inverse connection is designed to minimize conduction losses in the inductor



(a)



(b)

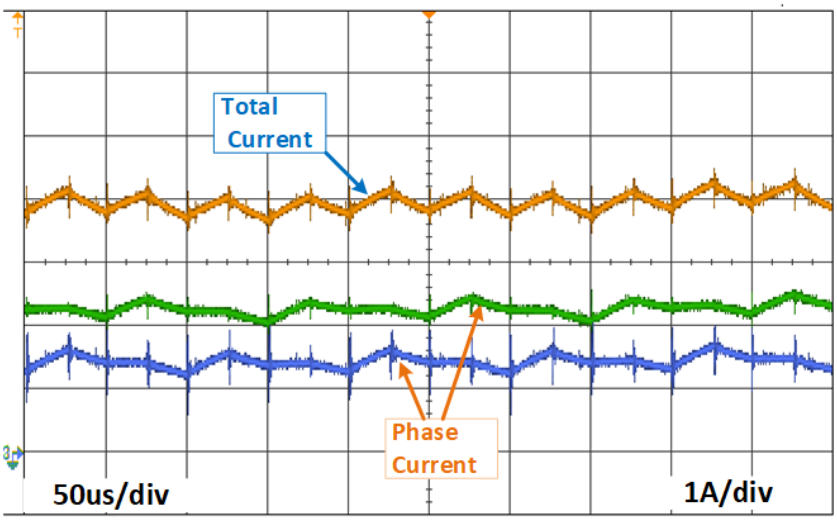
Figure 6.13 Coupled inductor current (a) direct coupling, (b) inverse coupling

From the Figure 6.13 it can be seen that the inverse coupling has smaller ripple on the phase but in term of total current the direct coupling has better ripple cancellation

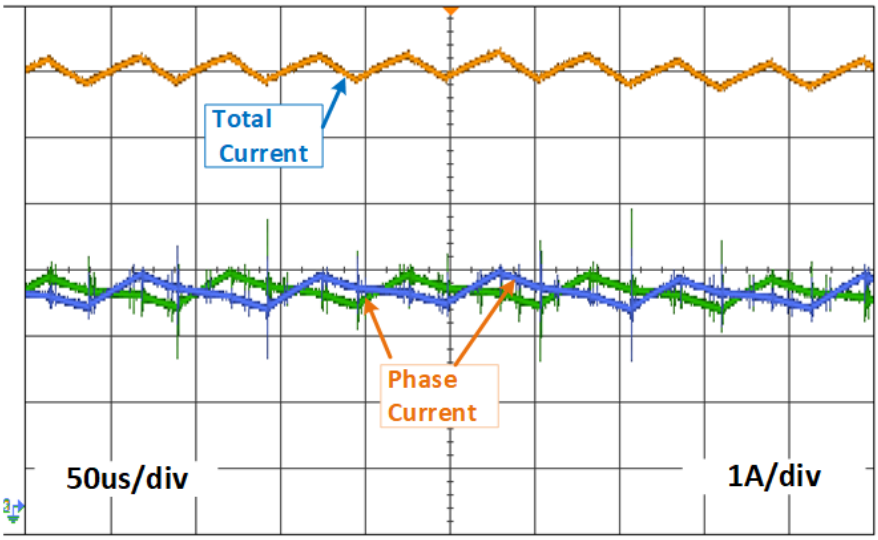
In the interleaved three-level flying-capacitor DC–DC converter, the introduction of magnetic coupling between phase inductors has a decisive effect on the magnitude of circulating current. When the inductors are directly coupled the effective differential-mode inductance decreases, thereby facilitating circulating current flow between phases and increasing conduction loss. Conversely, with inverse coupling (negative mutual inductance), the differential-

mode inductance increases while the common-mode inductance decreases, effectively suppressing circulating current and enhancing phase-current symmetry. Hence, inverse coupling is the preferred configuration for high-efficiency interleaved three-level converters, as it minimizes circulating-current amplitude.

Figure 6.14 and Figure 6.15 show before and after the leg equalization current control was applied. Ensuring equal sharing of the total load current among the converter legs in interleaved converters is necessary to prevent overheating or overloading of one leg, while others remain underutilized. Achieving a well-equalised current distribution is critical for alleviating the stress on individual converter leg components such as leg inductors, capacitors, and power semiconductor switches. This actively maintained equilibrium may contribute to an extended lifespan of these components. The current-equalising controller adjusts slightly the duty cycles to help distribute the load current evenly. Duty cycle adjustments are made by the DSP based on the current feedback from each leg. If one leg starts to carry more current than the others, the duty cycle of that leg is reduced, while the duty cycle of the other leg is increased.

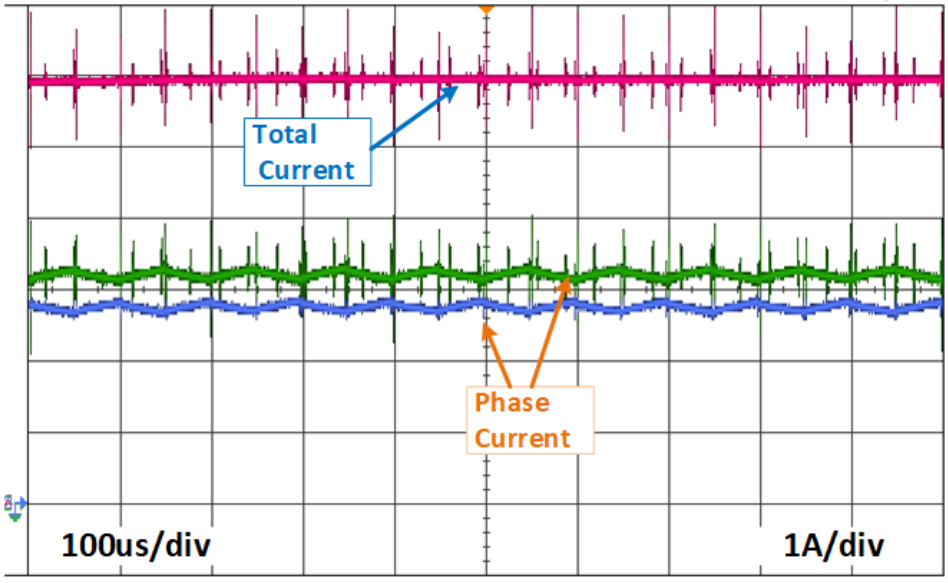


(a)

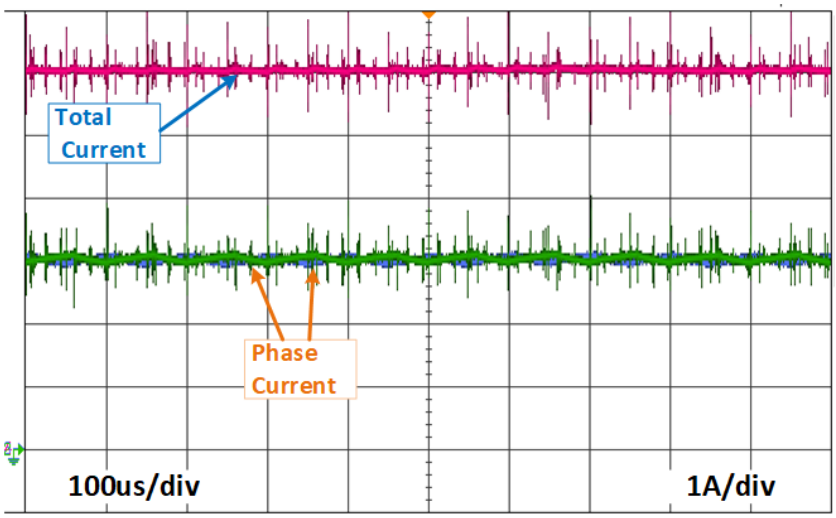


(b)

Figure 6.14 Waveforms of total load current and leg inductor currents when these are (a) unequalised and (b) equalised when leg inductors are coupled.



(a)



(b)

Figure 6.15 Discrete inductor (a) unequal current, (b)equalised current

6.2.3 Flying capacitor voltage

Flying capacitor control employs duty cycle adjustment to regulate the voltage levels of flying capacitors to ensure correct and safe converter performance. Figure 6.16 shows the experiment to test the capability of the proposed balancing technique to mitigate a flying capacitor voltage imbalance towards its target half of the input voltage. There are two flying capacitors in B3LI DC/DC converter. The initial value of one capacitor was higher than reference by overcharging it while the other capacitor initial voltage was lower. Consequently, during the balancing cycle, the overvoltage flying capacitor will experience a longer discharge state than charging state. Conversely, the under-voltage flying capacitor will have a charging state longer than its discharging state until it reaches steady state. Upon achieving steady state, the flying capacitor will charge and discharge at equivalent rates as presented in Figure 6.17.

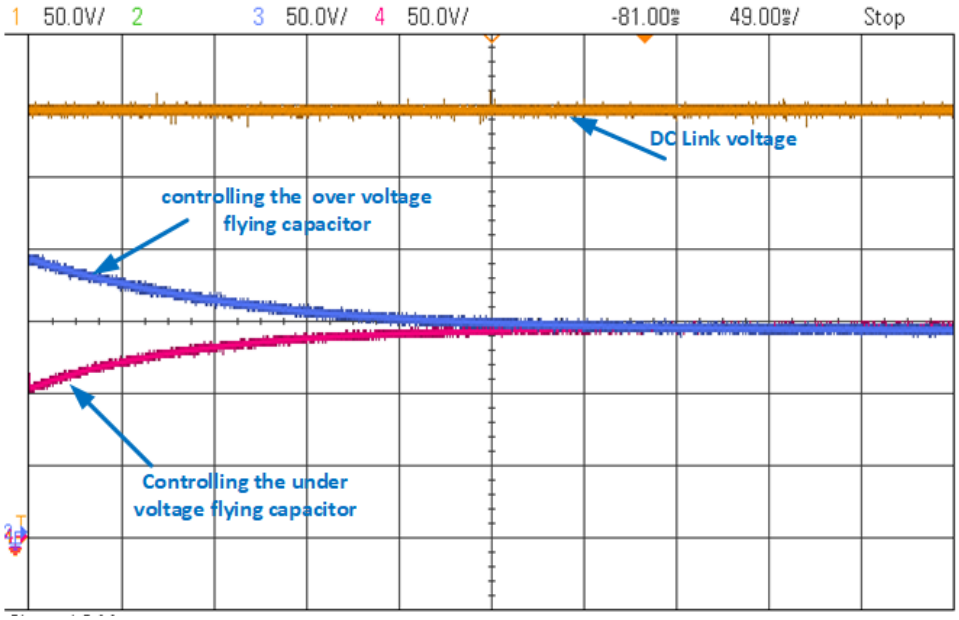


Figure 6.16. Flying capacitor voltage balancing

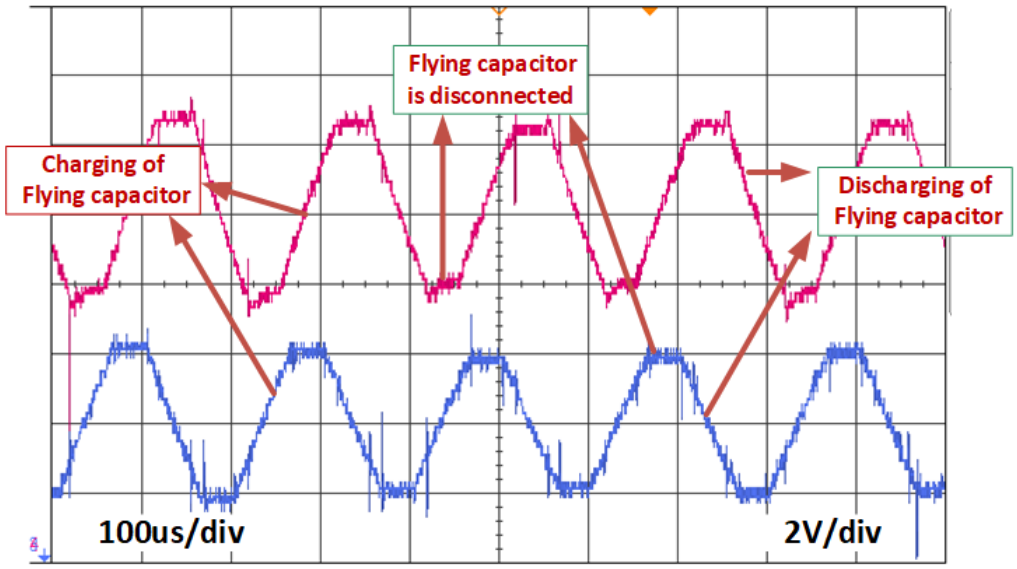
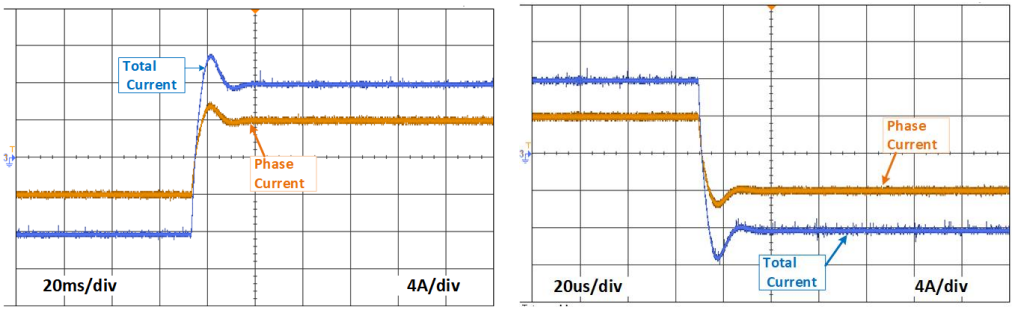


Figure 6.17. Flying capacitor charging and discharging during steady state.

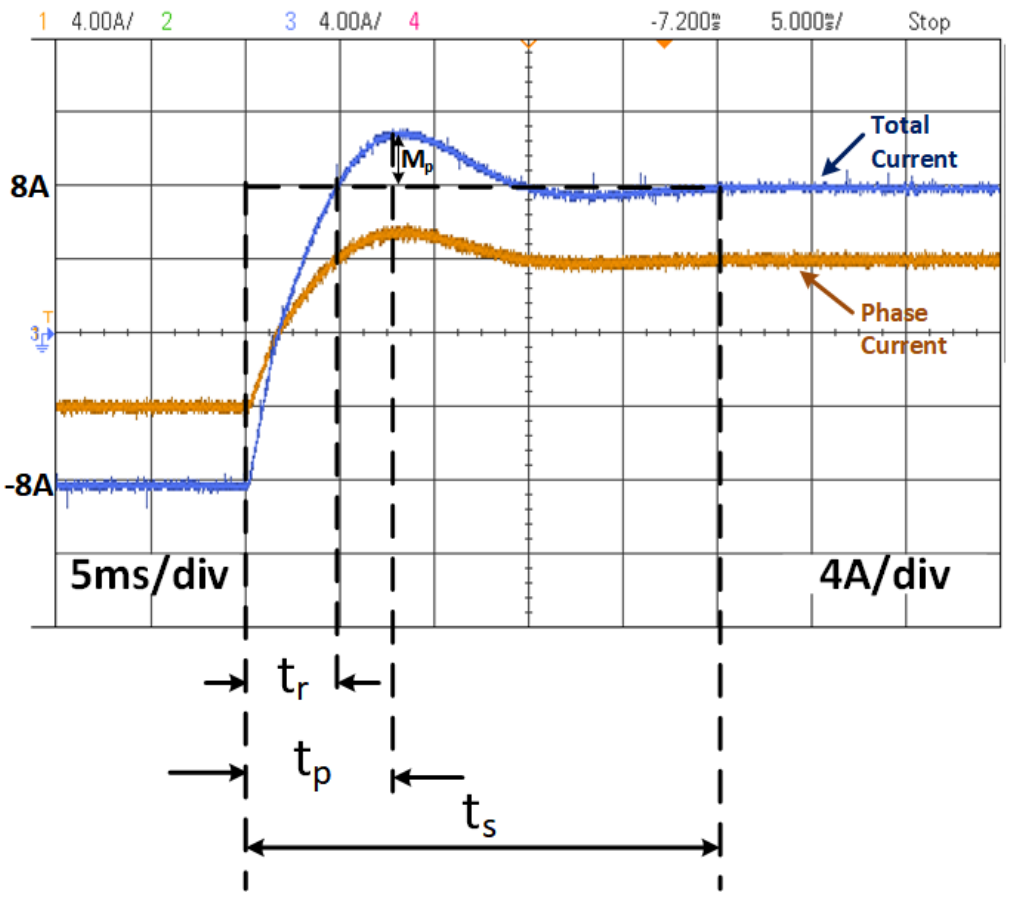
6.2.4 Transient and steady state response

A transient response is a temporary deviation from the steady-state condition due to a sudden change in the reference. Figure 6.18(a) shows the response of the B3LI DC/DC converter system when given step reference current from -8 to 8 A. The response of a power converter is typically characterized by its rise time, settling time, and overshoot. From Figure 6.18, the rise time from (the amount of time it takes for the inductor current to go from 10% to 90% of its final value) is

5 ms, while settling time (the amount of time it takes for the output to reach the reference within a 5% tolerance of its final value) is 20 ms and and peak time 7.5 ms with 3 A overshoot (the amount by which the output exceeds its final value during the transition) giving a percentage of 18% above the reference.



(a) (b)



(c)

Figure 6.18. Transient output current response to (a) -8 to +8A reference step up, (b) +8A to –8A reference step down. (c) zoomed in -8 to +8A reference step up

6.3 Power Losses and Efficiency Evaluation

There are several factors that causes of losses of energy in power conversion such has conduction loss and switching-loss in the power semiconductors, reverse recovery loss in the anti-parallel diode, dead time loss, gate charge loss, operation loss caused by the IC control circuit, power loss in the conductor winding and the magnetic core the inductor and losses in the capacitors. This section discussed the power losses in the semiconductor, inductor and capacitor.

6.3.1 Losses on semiconductor device

The efficiency of the power converter depends on how much power losses are created as metric of the converter performance. The converter losses are produced in the passive components due to the AC and DC resistance of the winding and the core losses of the inductors and the equivalent series resistance of capacitors and in the semiconductor during switching instance and during conduction of load current. Some more losses also occur because of the gate charge and during the deadtime. However, these losses will not be considered in this chapter.

The semiconductor device power losses, during conduction and switching, are generated due to the non-ideality of the devices. The conduction losses occurred when the device is fully on causing a voltage drop across. It happens because of the interaction of the conducting current through the device and the forward voltage (V_{CE}) of the switching device.

$$P_{CL} = V_{CE} \,.\, I_C \tag{6.1}$$

The IGBT conduction losses can be calculated using an IGBT approximation model which uses the IGBT collector-emitter on-state voltage at zero-current (V_{CE0}) and a collector-emitter on-state dynamic resistance (r_C) which gives :

$$V_{CE} = V_{CE0} + r_C . I_C \tag{6.2}$$

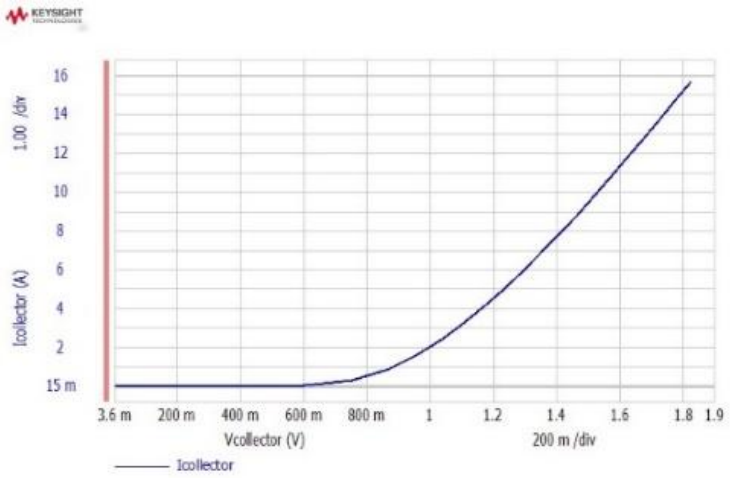
Therefore the instantaneous value of the IGBT conduction losses is expressed in Equation (6.3). Conduction losses, P_{CT} is dependent on the current.

Measurement of the IGBT with curve tracer power device analyser B1505A depicts relationship of current and resistance as shown in Figure 6.19.

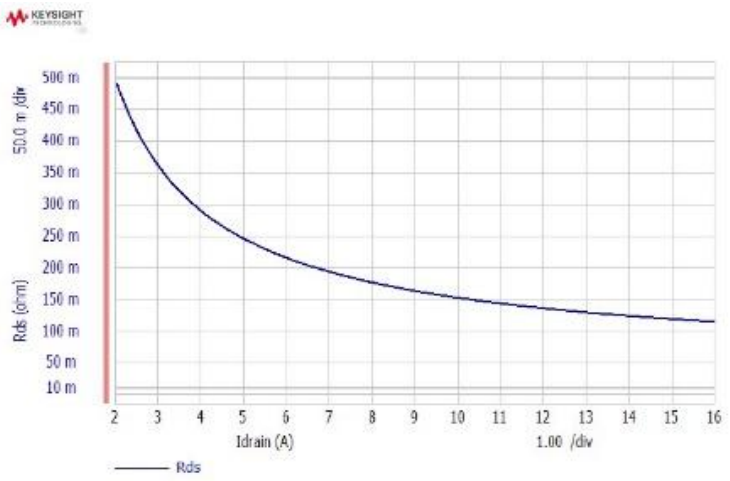
$$P_{CT} = V_{CE0} \, . I_C(t) + \, r_C . I_C^2(t) \tag{6.3}$$

The same approach is used for the anti-parallel diode, by considering voltage drop across diode when it forward biased, V_{D0} and the dynamic resistance of diode r_D gives diode conduction losses

$$P_{c-D} = V_{D0} \, . I_D(t) + \, r_D . I_D^2(t) \tag{6.4}$$



(a)



(b)

Figure 6.19 (a) Collector-emiter voltage and current (b) Collector-emiter resistance

The switching losses are determined by the dissipated energy during the turn-on and turn-off switching which results from the overlap of the device current flowing whilst the voltage across the switching device rises significantly higher than the values stated in (6.5) and (6.6) of the controllable devices (IGBTs) and the reverse recovery mechanism of the fast-recovery diodes.

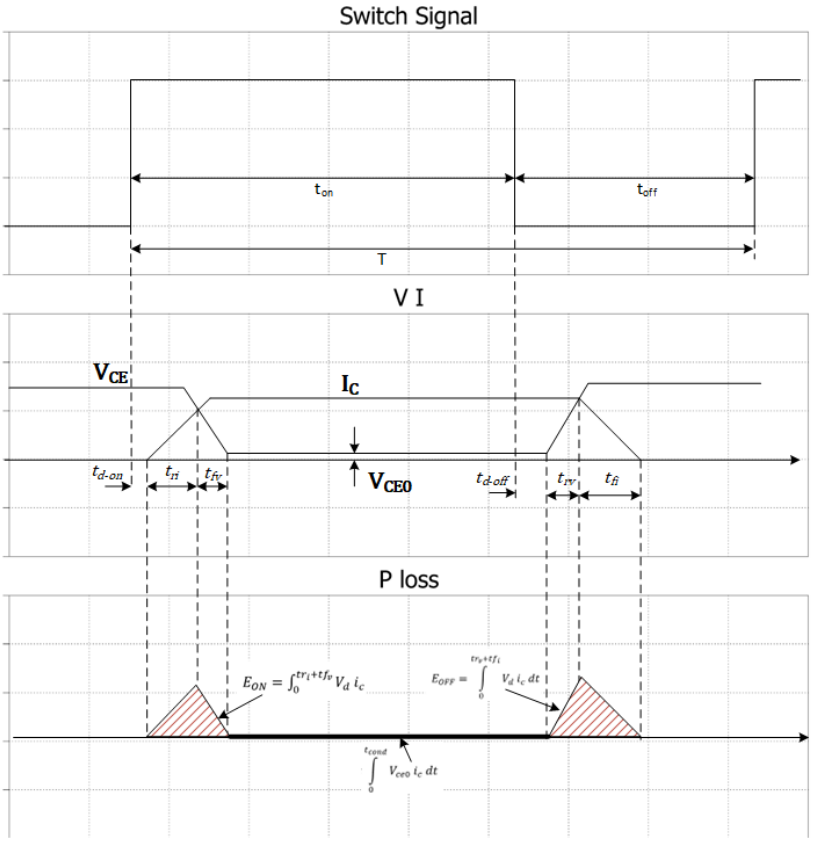


Figure 6.20 Current through and voltage across switching device during an idealised switching instant[129]

$$P_{swT} = (E_{ON} + E_{OFF})f_{SW} \tag{6.5}$$

Where,

$$E_{ON} = \int_0^{tr_i+tf_v} V_d\, i_c\, dt \text{ and,} \tag{6.6}$$

$$E_{OFF} = \int_0^{tr_v+tf_i} V_d\, i_c\, dt \tag{6.7}$$

Switching losses in the diode can be calculated similarly by multiplying the switching energies by the switching frequency (f_{SW}). The turn-on losses,

E_{ON-D}, are relatively small, while the turn-off losses, E_{OFF-D}, are higher due to reverse recovery effects.

$$P_{swD} = (E_{ON-D} + E_{OFF-D}) f_{SW} \tag{6.8}$$

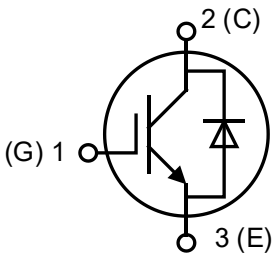
The power losses in the IGBT and anti-parallel diode can be represented as the total conduction and switching losses.

$$P_T = P_{cT} + P_{swT} = V_{CE0} . I_C(t) + r_C . I_C^2(t) + (E_{ON} + E_{OFF}) f_{SW} \tag{6.9}$$

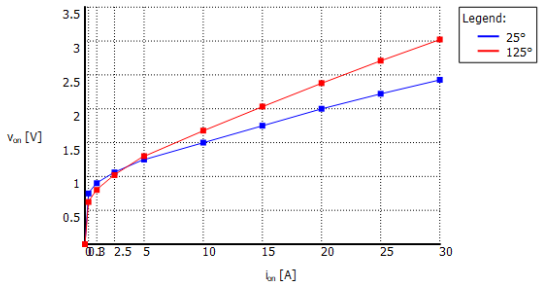
$$P_D = V_{CD0} . I_{CD}(t) + r_D . I_{CD}^2(t) + (E_{ON-D} + E_{OFF-D}) f_{SW\,ON-D} \tag{6.10}$$

The energy losses in the semiconductor switches increase the temperature of the device. A heat sink needs to be installed to take the dissipate the produced heat away from the power semiconductor switch and maintain its temperature at reasonable levels. The increase of temperature however may cause an increase of the specific switching losses and may impact also Vceo (decrease it) and the dynamic resistance (increases).

Figure 6.21 show the relevant graphs characterising the conduction (b,c) and switching (d-f) components of the power losses of the IXA17IF1200HJ which is a single IGBT device with antiparallel diode and its dependency with device temperature. These data based on IXA17IF1200HJ data sheet[130].



(a)



(b)

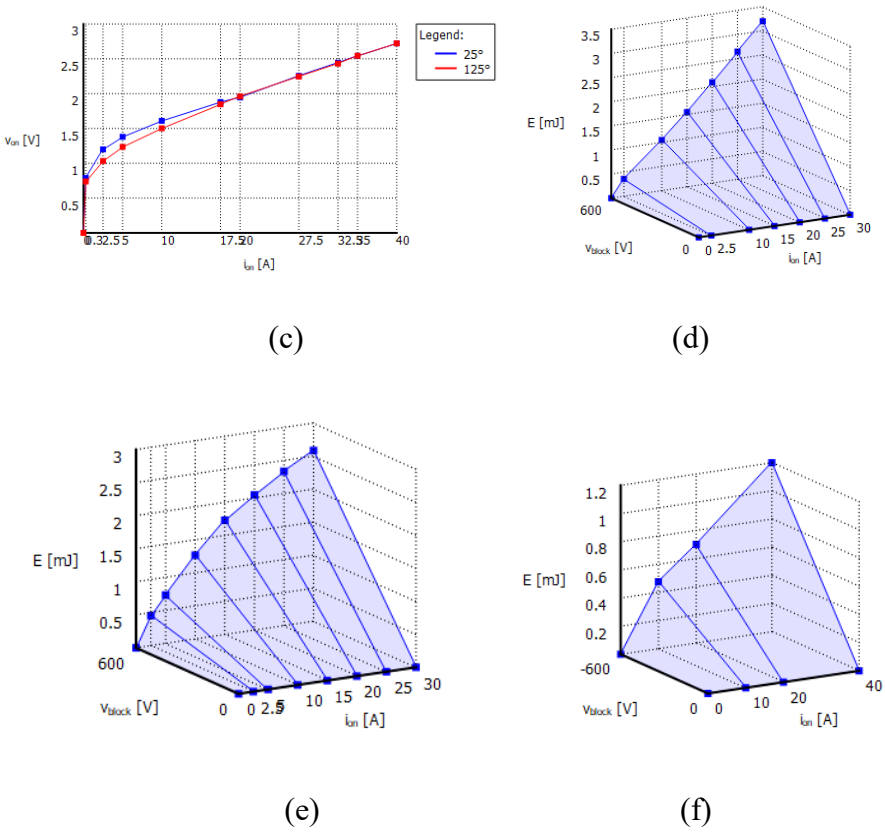


Figure 6.21 Thermal model characteristics include in the simulation model of the IXA17IF1200HJ device comprising of an IGBT with antiparallel diode: (a) symbol (b) IGBT conduction losses (c) Diode conduction losses (d) IGBT turn-on losses, (e) IGBT turn-off losses, (f) IGBT turn-off losses.

6.3.2 Losses on passive component

Inductor losses

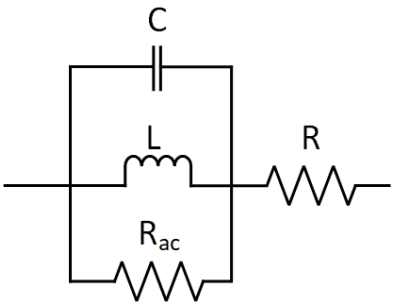


Figure 6.22 Inductor equivalent circuit

Figure 6.22 show the equivalent circuit of an inductor. Power dissipation in the inductor occurs in the windings and the core, and these are termed winding loss and core loss. The optimal efficiency of an inductor is attained when the core and winding losses are at their lowest. Consequently, the aim of maximising

efficiency is achieved by choosing an inductor that delivers adequate inductance to mitigate ripple current, while also minimising losses. It is crucial that the inductor enables current flow without causing the core to saturate or the winding to overheat which will impose a limit on the cross section of the magnetic core and also of the window area, both with an impact on the volume and weight.

The power loss of an inductor is defined by the following formula:

$$P_{loss} = P_{core} + P_{dcr} + P_{acr} \tag{6.11}$$

A common form of the core loss formula for cores is the Steinmetz Equation[131].

$$P_{core} = k\, f^x B^y \tag{6.12}$$

This equation shows that the core loss depends on the frequency (f) and the AC component of the flux density (B). Flux density depends on the ripple current; therefore, both are application-dependent variables. It also shows that the core loss depends on the core material which determines the *k*, *x*, and *y* constants.

Flux density is also a function of the core area (Ae) and the number of turns (N); therefore, core loss is both application-dependent and inductor-dependent.

The DC winding loss is simple to calculate:

$$P_{dcr} = I_{dc}^2\, DCR \tag{6.13}$$

AC winding loss is more complicated and may include the effects of increased resistance at a higher frequency due to both skin effect and proximity effect. ESR (equivalent series resistance) or ACR (AC resistance) curves show some of the increased resistance at higher frequency.

$$P_{acr} = I_{ac(rms)}^2\, ESR \tag{6.14}$$

Figure 6.23 shows the equivalent series resistance vs. frequency profiles, ESR(f) of phases A and B, and L_A and L_B of the coupled inductor used in the experimental prototype. They were measured using an impedance analyser over the relevant range of frequencies where switching ripples are expected to be

produced by the prototype. It is clearly seen that the ESR value increased with frequency.

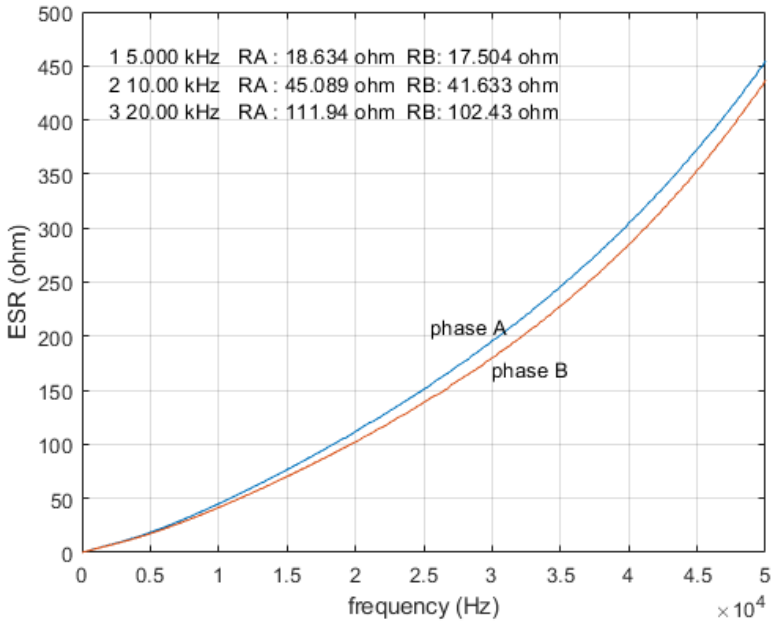


Figure 6.23 ESR-frequency profile

In general, the size of the inductor impedance is inversely proportional to the frequency. The coupled inductor inductance profile vs frequency is depicted in Figure 6.24. The switching frequency of one converter leg to be used in the prototype is 5kHz, but the inductor will be subject of double the value (line-to line) of 10kHz. Due to the non-ideality of the inductor, the inductance LA and LB are slightly different.

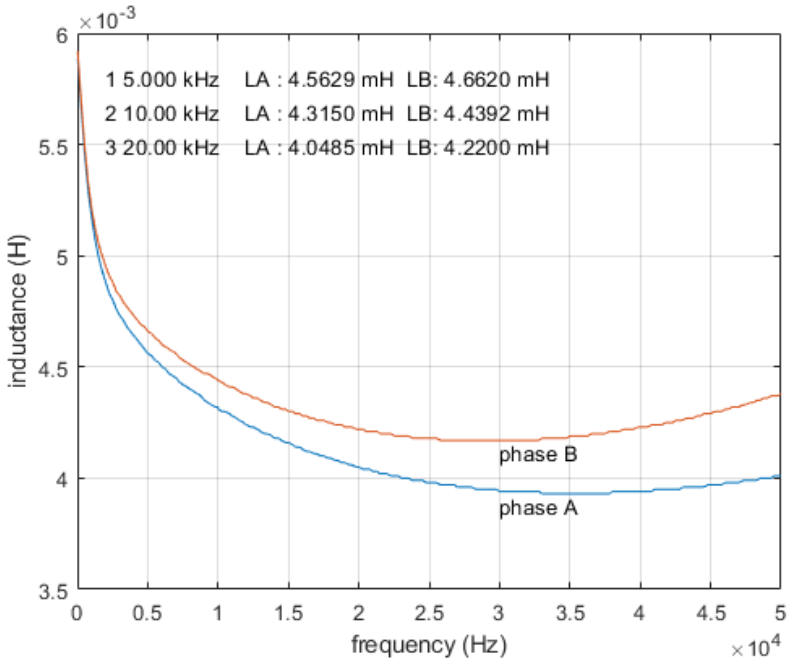


Figure 6.24. Inductance-frequency profile of the two coupled output inductors

Capacitor losses

Another source of loss is Req in the filter capacitors, which is the equivalent series resistance on the capacitor (Figure 6.25). It is used to define the total capacitor losses at a given frequency. The series inductance Ls generates a transient voltage drop Ls ·during the rising and falling di/dt slope, which can be large. The C4DENPQ6100A8TK device which is a 100µF/1000 V film capacitor was used which has a low ESR and ESL only 0.6 mΩ and 25nH respectively.

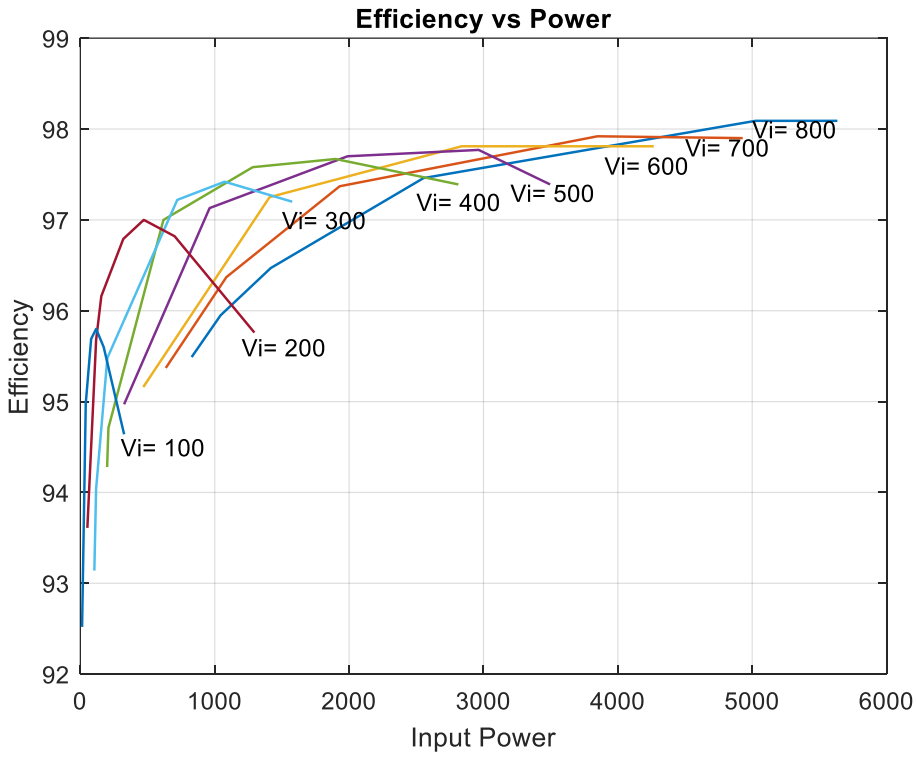


Figure 6.25. Capacitor equivalent circuit

6.3.3 Total power loss

The converter total power loss, P_{Loss}, is measured with the N4L/PPA2530 power analyser by measuring input and output power flows from the prototype at different input voltage levels of 100 V, 200V, 400V, 600V and 800V that result

in power flows of up to 6 kW which is the prototype's power rating whilst using a switching frequency of 5kHz. Based on the total power losses and the power delivered to the load, the experimental efficiency of the power stage can be calculated.



(a)

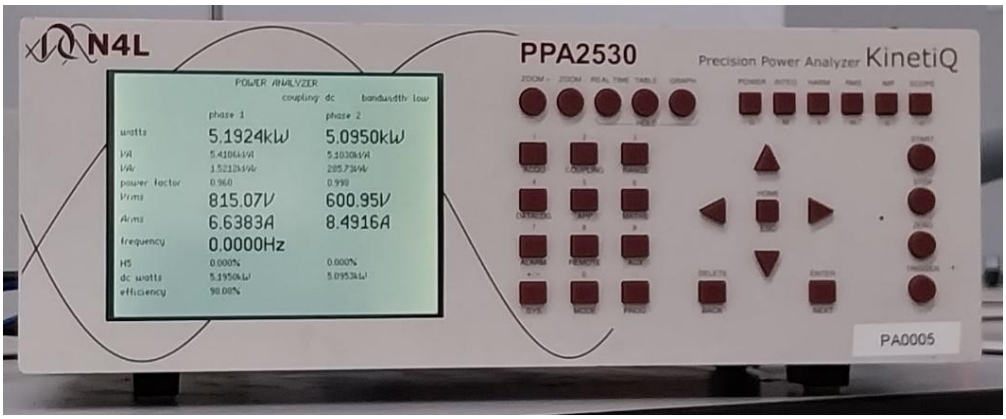


Figure 6.26.(a) Converter efficiency measurement (b) power analyser N4L/PPA2530

Figure 6.27 show the comparison of converter efficiencies operating with different input voltage at different power levels. The PLECS simulation model efficiency

is compared with the experimental one and is found to be higher that the measurement because in simulation considers only the power semiconductor's switching, conduction losses and inductor parasitic element.

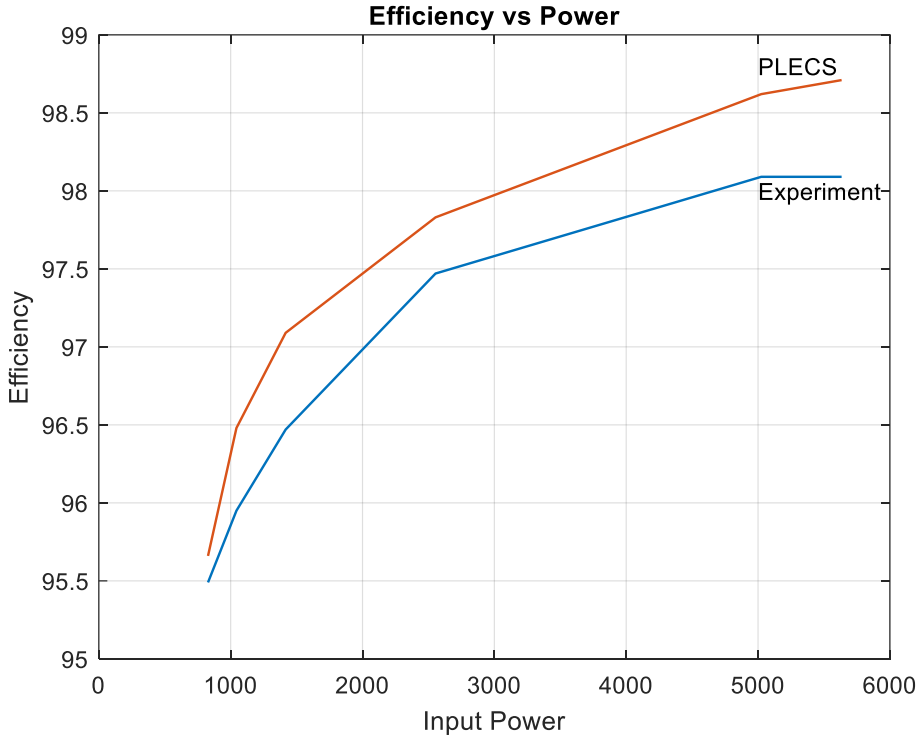


Figure 6.27 Efficiency comparison of B3LI DC/DC converter between the PLECS simulation and the experimental measurements.

6.4 Summary

This chapter presents the design and construction details of the 6kW/800V laboratory prototype power converter designed to validate the performance and functionality of the proposed Bidirectional Three-Level Interleaved DC/DC converter. The specifications of the prototype, including the control platform, are discussed. The experiments conducted included evaluating the converter's operation principles, verifying its ability to handle higher power and voltage, confirming the control dynamic performance and assessing the converter's efficiency which are all in line with the simulations and the expected performance from a PV powered EV charging system.

Chapter 7
Conclusions

7.1 Conclusions

Solar powered-EV charging station represents a promising and sustainable solution that can lead to a significant reduction in CO2 emissions in transportation. This innovative infrastructure reduces the dependency on the power grid and the traditional energy sources which currently are still dominated by fossil fuels and will minimize the carbon footprint associated with transportation. By integrating photovoltaic (PV) panels directly with EV charging facilities particularly in parking areas where renewable energy can be efficiently utilized to charge electric vehicles while they are parked.

This research investigated the potential of Bidirectional Three-Level Interleaved DC/DC Converter to be implemented in a charging station through mathematical modeling, simulation, and experimental validation. The results demonstrate that the combined advantages of the three-level structure and interleaving yield significant improvements in converter performance. The three-level configuration effectively halves the voltage stress on each semiconductor device, while interleaving increases the ripple frequency at both the input and output. This synergy leads to substantial reductions in switching losses, inductor current ripple, and the overall size and loss of passive components.

Based on the requirements of a PV-powered EV charging system, the Bidirectional Three-Level Interleaved DC/DC Converter is proposed due to the following key advantages:

1. Wide EV battery voltage compatibility, supporting charging up to 800 V, the emerging standard for high-power DC fast charging.
2. Compact and lightweight implementation, enabled by reduced switching voltage ripple and enhanced ripple cancellation in the interleaved

structure, further amplified through the use of coupled magnetics while maintaining high conversion efficiency (>98%).

3. Bidirectional power flow capability, essential for both battery charging and vehicle-to-vehicle (V2V) applications.

Finally, the theoretical analysis and simulation outcomes were validated using a laboratory-scale prototype. The experimental results confirm the practical feasibility and superior performance of the proposed converter and control strategy, reinforcing its suitability for PV-integrated EV charging systems.

7.2 Scientific Contributions

The various contributions of this thesis with regard to a PV-Powered EV charging station study are outlined below:

1. Deriving a procedure for optimizing the solar charging by finding the best match algorithm between the load EV charging profile and solar power generation profile to maximize direct charging of the EV battery. The target was achieved with a multi-orientation PV strings which improve the alignment between energy production and charging demand. An additional benefit of this method is the reduction of charge–discharge cycling in the energy storage system, thereby extending its operational lifespan.
2. Despite the widespread adoption of flying capacitor converters, no research has investigated their use in solar-powered EV fast-charging stations. This study proposed a three-level converter topology with interleaving operation and control method tailored specifically for PV powered-EV charging systems. This involves investigating the design, mathematical model, device parameters, and operating characteristics of the proposed converters to maximize conversion efficiency.
3. The viability of the topology to deliver higher current and voltage that match EV charging requirements is validated via simulations and building a full voltage rating experimental lab prototype. Comprehensive performance evaluations were conducted, including efficiency measurements, dynamic response analyses, and reliability assessments to validate the effectiveness of the proposed solutions.

7.3 Limitation

This work is focused on the development of an optimized solar charging station for electric vehicles. Several limitations of the work should be noted which can be put in some categories:

1. *Scope*: This study primarily focuses on the design and optimisation of solar charging stations which is also the most common and mostly suited to be widely integrated within car parks. However, it does not address other renewable energy sources such as wind power, limiting the generalizability of the findings to broader renewable energy systems.
2. *Scenario*: The scenario was designed with ideal considerations, for example, when modelling annual solar energy generation. This limits the ability to assess its performance in real-world scenarios with varying load demand and environmental factors that affect daily solar energy production, such as temperature and shading on solar panels.
3. *Simulation Assumptions*: The simulation models used to evaluate the performance of the proposed converter rely on certain assumptions regarding component characteristics and operating conditions. While efforts were made to ensure accuracy by referring to the datasheet, these assumptions may not fully capture the complexities of practical implementations.
4. *Experimental Setup*: Due to constraints in time and resources, the experimental validation of the proposed model was conducted under specific laboratory conditions which means that although the voltage range was the fully expected 800V, a reduced current rating of 8A was specified for the prototype. Secondly, the choice of components, such as power semiconductor devices and passive elements, was based on a scaled down design, availability, and cost considerations. This may have implications for the scalability and robustness of the system in commercial or industrial-scale applications.

5. *Regulatory Compliance*: Compliance with relevant power quality, EMC, safety and regulatory standards, comprehensive certification and validation processes were outside the scope of this study. Further regulatory assessments would be necessary for commercial deployment of the proposed system.

7.4 Future research

Future directions related to research on PV powered -EV charging station:

1. *Integration with other renewable energy sources and storage*: Relying on solar energy generation leads to unreliable energy generation particularly for location where the sunlight is limited during certain times/days/seasons such as in the Northern Hemisphere. Investigating the integration of PV with other renewable sources of energy such wind power and other energy storage technologies, such as supercapacitors will enhance energy availability, flexibility and stability. Future research could focus on optimizing the coordination between the different energy sources and energy storage units to improve response times and mitigate intermittency issues.
2. *Multi-Objective Optimization*: multi-objective optimization of PV-EV charging station should consider such factors cost, driving behaviour and efficiency. Future research could explore optimization algorithms and decision-making frameworks to find trade-offs between conflicting objectives, such as maximizing system efficiency while minimizing component costs, leading to more sustainable and economically viable solutions for renewable energy integration.
3. *Real-World Deployments*: Future research could involve collaboration with industry partners and utility companies to assess the practical feasibility and market acceptance of the proposed system. It is anticipated that the proposed converter would also be well suited to a range of other applications such as aerospace that is focused on weigh minimisation purpose. Utilizing advanced device such as wide-bandgap semiconductor could improve the overall charging performance.

4. *Topology extension*: Depend on the sizing, extension to more than 3 levels, more phase and as well as maximise coupling of inductors could be investigated to improve voltage/current/power sharing, waveform quality and reduced size.
5. Adding compliance investigations with power Quality, safety and EMC standards.

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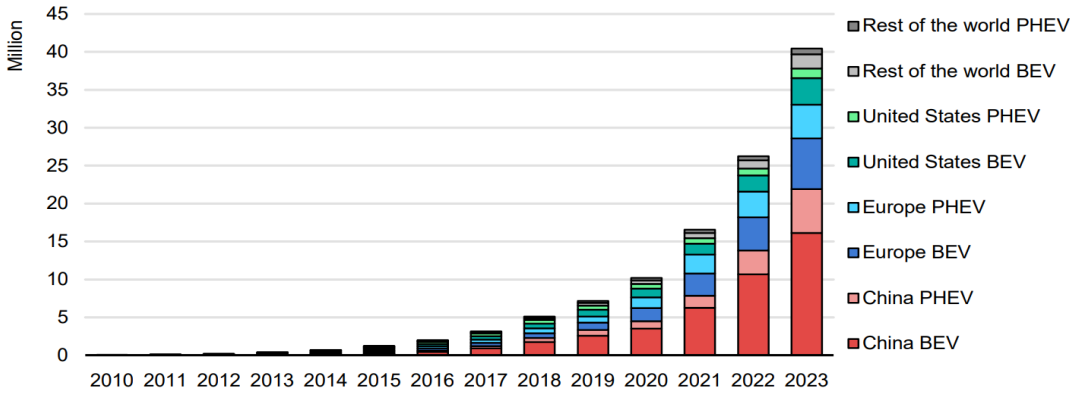
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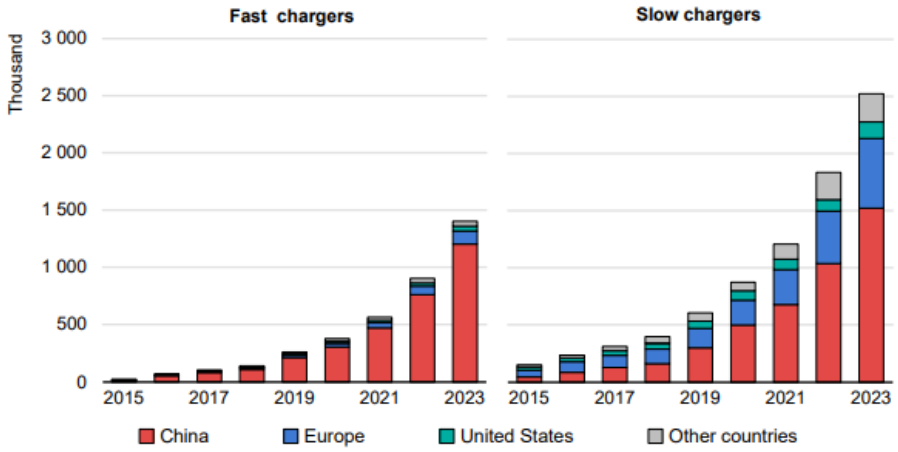
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Appendices

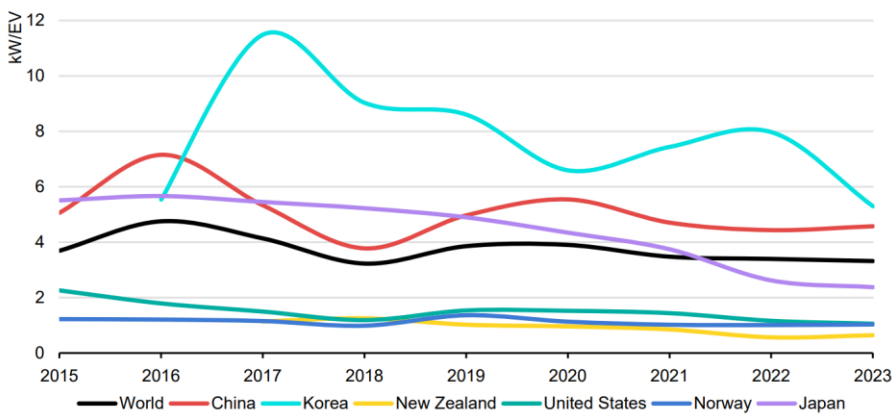
Appendix 1: Electric Vehicle data and solar charging potential



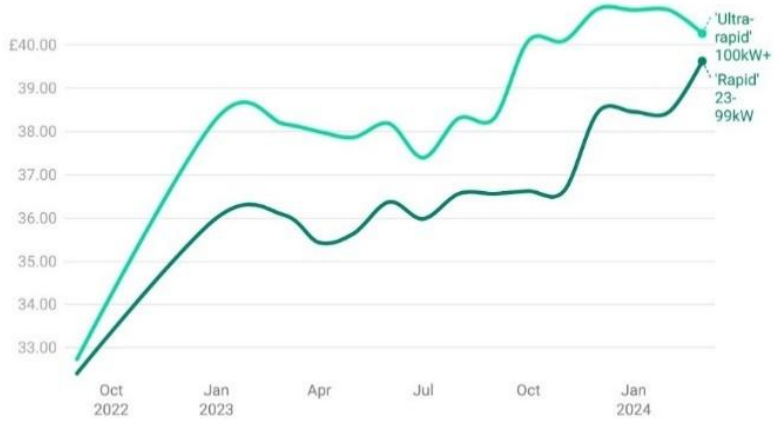
(a)



(b)

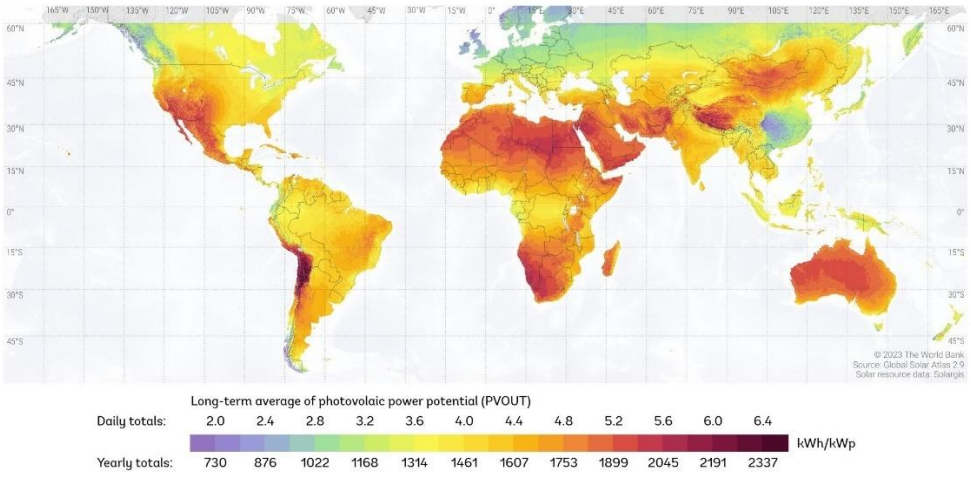


(c)



(d)

Appendix 1.1 (a) Electric cars stocks trends, (b) Installed publicly accessible light-duty vehicle charging points by power rating and region (c) Electric light-duty vehicle ratio per public charging point in kW/EV [14] (d) Average cost to charge a 64kWh electric car to 80% at a public charger [132]



Appendix 1.2 Solar resource maps of World[133]

Appendix 2: Charging specification for selected EV

Appendix 2.2 Charging specification for selected EV [25]

Car	Battery kWH	e Battery (	Architecture/ Nominal Voltage	Battery	Home charge power Max (AC)			Rapid charging (DC			Energy consumption wH/mi	Range (mi)	release	Bidirectional
						Power (kW)	time (H)		Power (kW)	time (m)				
Abarth 500e Hatchback	37.8	42.2	400 / 355	Li-ON	Type 2	11	4h15m	CCS	85	25	270	140	May-23	
Audi Q8 e-tron 55 quattro	106	114	400 / 397	Li-ON	Type 2	22	5h45m	CCS	168	33	337	315	Dec-22	
BMW iX xDrive 50	105.2	111.5	400 / 369	Li-ON	Type 2	11	11h15m	CCS	195	31	334	315	Nov-21	
BMW iX3	74	80	400 / 400	Li-ON	Type 2	11	8h	CCS	155	31	308	240	Sep-21	
BYD SEAL 82.5 kWh RWD Design	82.5	84	800 / 550	Li-ON	Type 2	11	9h	CCS	150	38	280	295	Sep-23	
Citroen e-Berlingo M 50 kWh	50	52	400 /	Li-ON	Type 2	7.4	8h	CCS	100	28	345	145	Mar-24	
CUPRA Born VZ	79	84	400 / 352	Li-ON	Type 2	11	8h30m	CCS	185	26	277	285	Aug-24	
Fiat 500e Hatchback 24 kWh	21.3	23.8	400 / 400	Li-ON	Type 2	11	2h30m	CCS	50	24	251	85	Apr-21	
Ford Mustang Mach-E Premium RWD	91	98.7	400 /	Li-ON	Type 2	11	9h45m	CCS	150	47	303	300	Dec-24	
Genesis G80 Electrified Luxury	82.5	87.2	800 /	Li-ON	Type 2	11	9h	CCS	230	21	300	275	Jun-22	
Hyundai IONIQ 5 N	80	84	800 / 697	Li-ON	Type 2	11	8h45m	CCS	263	17	333	240	Nov-23	V2L : 3.6 kW
Jaguar I-Pace EV400	84.7	90	400 / 400	Li-ON	Type 2	11	9h15m	CCS	104	44	360	235	Jan-23	
KGM Torres EVX	72	73.4	400 / 390	Li-ON	Type 2	11	7h45m	CCS	120	37	313	230	Apr-24	
Kia EV9 99.8 kWh RWD	96	99.8	800 / 552	Li-ON	Type 2	11	1030m	CCS	209	22	343	280	Sep-23	V2L : 3.6 kW, V2G: 11kW
Lotus Eletre	109	111.9	800 / 709	Li-ON	Type 2	22	6h	CCS	367	19	357	305	Nov-23	
Lotus Emeya	100	102	800 /	Li-ON	Type 2	22	5h30m	CCS	350	18	308	325	Mar-24	
Maserati Grecale Folgore	95	105	400 /	Li-ON	Type 2	22	5h15m	CCS	150	38	388	245	Mar-24	
Maxus MIFA 9	84	90	400 /	Li-ON	Type 2	11	9h	CCS	114	36	373	225	Jan-23	
Mazda MX-30	30	35.5	400 /	Li-ON	Type 2	6.6	5h30m	CCS	54	41	286	105	Jul-23	

Car	Battery kWH	e Battery (	Architecture/ Nominal Voltage	Battery	Home charge power Max (AC)			Rapid charging (DC			Energy consumption wH/mi	Range (mi)	release	Bidirectional
						Power (kW)	time (H)		Power (kW)	time (m)				
Mercedes-Benz EQS SUV Maybach 680	118	125	400 /	Li-ON	Type 2	: 22	6h30m	CCS	: 200	33	387	305	Apr-24	
MG MG4 EV Extended Range	74.4	77	400 /	Li-ON	Type 2	: 6.6	13h15m	CCS	: 144	30	281	265	Aug-23	
Mini Countryman E	64.6	66.5	400 / 286	Li-ON	Type 2	: 11	7h	CCS	: 128	30	275	235	Feb-24	
Nissan Ariya 87kWh	87	91	400 /	Li-ON	Type 2	: 22	4h45m	CCS	: 130	35	311	280	Aug-22	
Peugeot e-3008 98 kWh Long Range	98	103	400 /	Li-ON	Type 2	: 11	10h30m	CCS	: 160	32	311	315	Sep-24	
Polestar 3 Long Range Dual motor	107	111	400 /	Li-ON	Type 2	: 11	11h30m	CCS	: 250	32	357	300	Nov-22	
Porsche Macan 4 Electric	95	105	400 /	Li-ON	Type 2	: 22	5h15m	CCS	: 150	38	317	300	Mar-24	
Porsche Taycan Plus	97	105	800 /	Li-ON	Type 2	: 11	10h30m	CCS	: 320	18	277	350	Feb-24	
Renault Scenic E-Tech 220hp Long Range	87	92	400 /	Li-ON	Type 2	: 22	4h45m	CCS	: 150	40	285	305	Dec-23	
Skoda Enyaq 85	77	82	400 / 352	Li-ON	Type 2	: 11	8h30m	CCS	: 135	28	275	280	Oct-23	
Subaru Solterra AWD	64	71.4	400 / 355	Li-ON	Type 2	: 6.6	11h30m	CCS	: 147	28	320	200	Mar-23	
Tesla Model S Dual Motor	95	100	400 / 407	Li-ON	Type 2	: 11	10h15m	CCS	: 250	30	268	355	Sep-24	
Toyota bZ4X FWD	64	71.4	400 / 355	Li-ON	Type 2	: 6.6	11h30m	CCS	: 147	28	298	215	Aug-24	
Vauxhall Astra Electric	50.8	54	400 / 377	Li-ON	Type 2	: 11	5h30m	CCS	: 100	26	261	195	Jun-23	
Volkswagen ID.7 Pro S	86	91	400 / 383	Li-ON	Type 2	: 11	9h15m	CCS	: 200	26	269	320	Jul-24	
Volvo EX90 Twin Motor	107	111	400 /	Li-ON	Type 2	: 11	11h30m	CCS	: 250	32	369	290	Dec-22	

Appendix 3: Inductor voltage at different duty cycle

Appendix 3.1 . During buck operation

D<0.25

+State	Interval	v_A	v_B
1000	D	$V_H - V_{cfA} - V_L$	$-V_L$
0000	0.25-D	$-V_L$	$-V_L$
0010	D	$-V_L$	$V_H - V_{cfB} - V_L$
0000	0.25-D	$-V_L$	$-V_L$
0100	D	$V_{cfA} - V_L$	$-V_L$
0000	0.25-D	$-V_L$	$-V_L$
0001	D	$-V_L$	$V_{cfB} - V_L$
0000	0.25-D	$-V_L$	$-V_L$

D=0.25

+State	Interval	v_A	v_B
1000	D	$V_H - V_{cfA} - V_L$	$-V_L$
0010	D	$-V_L$	$V_H - V_{cfB} - V_L$
0100	D	$V_{cfA} - V_L$	$-V_L$
0001	D	$-V_L$	$V_{cfB} - V_L$

0.25 <D<0.5

+State	Interval	v_A	v_B
1001	D-0.25	$V_H - V_{cfA} - V_L$	$V_{cfB} - V_L$
1000	0.5-D	$V_H - V_{cfA} - V_L$	$-V_L$
1010	D-0.25	$V_H - V_{cfA} - V_L$	$V_H - V_{cfB} - V_L$
0010	0.5-D	$-V_L$	$V_H - V_{cfB} - V_L$
0110	D-0.25	$V_{cfA} - V_L$	$V_H - V_{cfB} - V_L$
0100	0.5-D	$V_{cfA} - V_L$	$-V_L$
0101	D-0.25	$V_{cfA} - V_L$	$V_{cfB} - V_L$
0001	0.5-D	$-V_L$	$V_{cfB} - V_L$

D=0.5

+State	Interval	v_A	v_B
1001	0.5D	$V_H - V_{cfA} - V_L$	$V_{cfB} - V_L$
1010	0.5D	$V_H - V_{cfA} - V_L$	$V_H - V_{cfB} - V_L$
0110	0.5D	$V_{cfA} - V_L$	$V_H - V_{cfB} - V_L$
0101	0.5D	$V_{cfA} - V_L$	$V_{cfB} - V_L$

0.5 <D<0.75

+State	Interval	v_A	v_B
1101	D-0.5	$V_H - V_L$	$V_{cfB} - V_L$
1001	0.75-D	$V_H - V_{cfA} - V_L$	$V_{cfB} - V_L$
1011	D-0.5	$V_H - V_{cfA} - V_L$	$V_H - V_L$
1010	0.75-D	$V_H - V_{cfA} - V_L$	$V_H - V_{cfB} - V_L$
1110	D-0.5	$V_H - V_L$	$V_H - V_{cfB} - V_L$
0110	0.75-D	$V_{cfA} - V_L$	$V_H - V_{cfB} - V_L$
0111	D-0.5	$V_{cfA} - V_L$	$V_H - V_L$
0101	0.75-D	$V_{fA} - V_L$	$V_{cfB} - V_L$

D=0.75

+State	Interval	v_A	v_B
1101	1-D	$V_H - V_L$	$V_{cfB} - V_L$
1011	1-D	$V_H - V_{cfA} - V_L$	$V_H - V_L$
1110	1-D	$V_H - V_L$	$V_H - V_{cfB} - V_L$
0111	1-D	$V_{cfA} - V_L$	$V_H - V_L$

D>0.75

+State	Interval	v_A	v_B
1111	D-0.75	$V_H - V_L$	$V_H - V_L$
1101	1-D	$V_H - V_L$	$V_{cfB} - V_L$
1111	D-0.75	$V_H - V_L$	$V_H - V_L$

1011	1-D	$V_H - V_{cfA} - V_L$	$V_H - V_L$
1111	D-0.75	$V_H - V_L$	$V_H - V_L$
1110	1-D	$V_H - V_L$	$V_H - V_{cfB} - V_L$
1111	D-0.75	$V_H - V_L$	$V_H - V_L$
0111	1-D	$V_{cfA} - V_L$	$V_H - V_L$

Appendix 3.2 Dcuring boost operation

D<0.25

+State	Interval	v_A	v_B
0111	D	$V_L - V_{cfA}$	$V_L - V_H$
1111	0.25-D	$V_L - V_H$	$V_L - V_H$
1101	D	$V_L - V_H$	$V_L - V_{cfB}$
1111	0.25-D	$V_L - V_H$	$V_L - V_H$
1011	D	$V_L + V_{cfA} - V_H$	$V_H - V_L$
1111	0.25-D	$V_L - V_H$	$V_L - V_H$
1110	D	$V_L - V_H$	$V_L + V_{cfB} - V_H$
1111	0.25-D	$V_L - V_H$	$V_L - V_H$

D=0.25

+State	Interval	v_A	v_B
0111	D	$V_L - V_{cfA}$	$V_L - V_H$
1101	D	$V_L - V_H$	$V_L - V_{cfB}$
1011	D	$V_L + V_{cfA} - V_H$	$V_L - V_H$
1110	D	$V_L - V_H$	$V_L + V_{cfB} - V_H$

0.25 <D<0.5

+State	Interval	v_A	v_B
0110	D-0.25	$V_L - V_{cfA}$	$V_L + V_{cfB} - V_H$
0111	0.5-D	$V_L - V_{cfA}$	$V_L - V_H$
0101	D-0.25	$V_L - V_{cfA}$	$V_L - V_{cfB}$
1101	0.5-D	$V_L - V_H$	$V_L - V_{cfB}$

1001	D-0.25	$V_L + V_{cfA} - V_H$	$V_L - V_{cfB}$
1011	0.5-D	$V_L + V_{cfA} - V_H$	$V_L - V_H$
1010	D-0.25	$V_L + V_{cfA} - V_H$	$V_L + V_{cfB} - V_H$
1110	0.5-D	$V_L - V_H$	$V_L + V_{cfB} - V_H$

D=0.5

+State	Interval	v_A	v_B
0110	0.5D	$V_L - V_{cfA}$	$V_L + V_{cfB} - V_H$
0101	0.5D	$V_L - V_{cfA}$	$V_L - V_{cfB}$
1001	0.5D	$V_L + V_{cfA} - V_H$	$V_L - V_{cfB}$
1010	0.5D	$V_L + V_{cfA} - V_H$	$V_L + V_{cfB} - V_H$

0.5 <D<0.75

+State	Interval	v_A	v_B
0010	D-0.5	V_L	$V_L + V_{cfB} - V_H$
0110	0.75-D	$V_L - V_{cfA}$	$V_L + V_{cfB} - V_H$
0100	D-0.5	$V_L - V_{cfA}$	V_L
0101	0.75-D	$V_L - V_{cfA}$	$V_L - V_{cfB}$
0001	D-0.5	V_L	$V_L - V_{cfB}$
1001	0.75-D	$V_L + V_{cfA} - V_H$	$V_L - V_{cfB}$
1000	D-0.5	$V_L + V_{cfA} - V_H$	V_L
1010	0.75-D	$V_L + V_{cfA} - V_H$	$V_L + V_{cfB} - V_H$

D=0.75

+State	Interval	v_A	v_B
0010	1-D	V_L	$V_L + V_{cfB} - V_H$
0100	1-D	$V_L - V_{cfA}$	V_L
0001	1-D	V_L	$V_L - V_{cfB}$
1000	1-D	$V_L + V_{cfA} - V_H$	V_L

0.75<D<1

+State	Interval	v_A	v_B
0000	D-0.75	V_L	V_L
0010	1-D	V_L	$V_L + V_{cfB} - V_H$
0000	D-0.75	V_L	V_L
0100	1-D	$V_L - V_{cfA}$	V_L
0000	D-0.75	V_L	V_L
0001	1-D	V_L	$-V_L$
0000	D-0.75	V_L	$V_L - V_{cfB}$
1000	1-D	$V_L + V_{cfA} - V_H$	V_L

Appendix 4. Small signal signal Modelling of B3LI Converter

Appendix 4.1 Small-signal Modelling of the converters during buck operation

To simplify state space equation later in this section the Equation (8.1) and (8.2) will be used.

$$\frac{1}{(1-\alpha^2)L} = \frac{1}{\Sigma L} \tag{8.1}$$

$$\frac{(1-\alpha)}{(1-\alpha^2)L} = \frac{1}{\Sigma L x} \tag{8.2}$$

To develop small-signal (linear) model of transfer function of the system, one operating point is taken, for instance is between 0< VTR< 0.25 in table Appendix 3.1

Where,

$$\frac{di_A}{dt} = \frac{v_A - \alpha\, v_B}{(1-\alpha^2)L} \tag{8.3}$$

$$\frac{di_B}{dt} = \frac{v_B - \alpha\, v_A}{(1-\alpha^2)L} \tag{8.4}$$

Interval 1: D (1000)

$$v_A = V_{dc} - V_{cfA} - V_{ld} \tag{8.5}$$

$$v_B = -V_{Ld} \tag{8.6}$$

$$\frac{di_A}{dt} = \frac{V_{dc} - V_{cfA} - (1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.7}$$

$$\frac{di_B}{dt} = \frac{-\alpha V_{dc} + \alpha V_{cfA} - (1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.8}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{ld}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{\mathrm{C}} & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{ld} \end{bmatrix} + \begin{bmatrix} -\frac{1}{\Sigma \mathrm{L}} & 0 & \frac{1}{\Sigma \mathrm{L}} \\ \frac{\alpha}{\Sigma \mathrm{L}} & 0 & -\frac{\alpha}{\Sigma \mathrm{L}} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} = A_1 X + B_1 Y \tag{8.9}$$

Interval 2 : 0.25-D

$$v_A = -V_{ld} \tag{8.10}$$

$$v_B = -V_{ld} \tag{8.11}$$

$$\frac{di_A}{dt} = \frac{di_B}{dt} = \frac{-(1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.12}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{ld}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{\mathrm{C}} & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{ld} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} = A_2 X + B_2 Y \tag{8.13}$$

Interval 3 : D

$$v_A = -V_{ld} \tag{8.14}$$

$$v_B = V_{dc} - V_{cfB} - V_{ld} \tag{8.15}$$

$$\frac{di_A}{dt} = \frac{-\alpha V_{dc} + \alpha V_{cfB} - (1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.16}$$

$$\frac{di_B}{dt} = \frac{V_{dc} - V_{cfB} - (1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.17}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{ld}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{ld} \end{bmatrix} + \begin{bmatrix} 0 & \frac{\alpha}{\Sigma L} & -\frac{\alpha}{\Sigma L} \\ 0 & -\frac{1}{\Sigma L} & \frac{1}{\Sigma L} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} = A_3X + B_3Y \quad (8.18)$$

Interval 4 : 0.25-D

$$v_A = -V_{ld} \quad (8.19)$$

$$v_B = -V_{ld} \quad (8.20)$$

$$\frac{di_A}{dt} = \frac{-(1-\alpha)V_{ld}}{(1-\alpha^2)L} \quad (8.21)$$

$$\frac{di_B}{dt} = \frac{-(1-\alpha)V_{ld}}{(1-\alpha^2)L} \quad (8.22)$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{ld}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{ld} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} = A_4X + B_4Y \quad (8.23)$$

Interval 5 : D

$$v_1 = v_{cf1} - V_{ld} \quad (8.24)$$

$$v_B = -V_{ld} \quad (8.25)$$

$$\frac{di_A}{dt} = \frac{v_{cfA} - (1-\alpha)V_{ld}}{(1-\alpha^2)L} \quad (8.26)$$

$$\frac{di_B}{dt} = \frac{-\alpha v_{cfA} - (1-\alpha)V_{ld}}{(1-\alpha^2)L} \quad (8.27)$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{ld}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{ld} \end{bmatrix} + \begin{bmatrix} \frac{1}{\Sigma L} & 0 & 0 \\ -\frac{\alpha}{\Sigma L} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} = A_5X + B_5Y \quad (8.28)$$

Interval 6 : 0.25-D

$$v_A = -V_{ld} \quad (8.29)$$

$$v_B = -V_{ld} \quad (8.30)$$

$$\frac{di_A}{dt} = \frac{di_B}{dt} = \frac{-(1-\alpha)V_{ld}}{(1-\alpha^2)L} \quad (8.31)$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{ld}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{\mathrm{C}} & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{ld} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} = A_6 X + B_6 \tag{8.32}$$

Interval 7 : D

$$v_A = -V_{ld} \tag{8.33}$$

$$v_B = v_{cfB} - V_{ld} \tag{8.34}$$

$$\frac{di_A}{dt} = \frac{di_B}{dt} = \frac{-\alpha v_{cfB} - (1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.35}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{ld}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{\mathrm{C}} & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{ld} \end{bmatrix} + \begin{bmatrix} 0 & -\frac{\alpha}{\Sigma \mathrm{L}} & 0 \\ 0 & \frac{1}{\Sigma \mathrm{L}} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} = A_7 X + B_7 Y \tag{8.36}$$

Interval 8: 0.25-D

$$v_A = -V_{ld} \tag{8.37}$$

$$v_B = -V_{ld} \tag{8.38}$$

$$\frac{di_A}{dt} = \frac{di_B}{dt} = \frac{-(1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.39}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{ld}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{\mathrm{C}} & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{ld} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{dc} \end{bmatrix} = A_8 X + B_8 Y \tag{8.40}$$

Combining the state input for one switching cycle operation (see Figure 4.17),

$$\mathrm{A} = aA_1 + bA_2 + c\,A_3 + dA_4 + eA_5 + fA_6 + g\,A_7 + hA_8 \tag{8.41}$$

$$\mathrm{B} = aB_1 d_1 + bB_2 + c\,B_3 + dB_4 + \mathrm{e}\,B_5 + fB_6 + g\,B_7 + hB_8 \tag{8.42}$$

The following is obtained,

$$A = (D)A_1 + (0.25 - D)A_2 + (D)A_3 + (0.25 - D)A_4 + (D)A_5 + (0.25 - D)A_6 + (D)A_7 + (0.25 - D)A_8 \quad (8.43)$$

$$B = (D)B_1 + (0.25 - D)B_2 + (D)B_3 + (0.25 - D)B_4 + (D)B_5 + (0.25 - D)B_6 + (D)B_7 + (0.25 - D)B_8 \quad (8.44)$$

Where,

$$A_1 = A_2 = A_3 = A_4 = A_5 = A_6 = A_7 = A_8 = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma Lx} \\ 0 & 0 & -\frac{1}{\Sigma Lx} \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} -\frac{1}{\Sigma L} & 0 & \frac{1}{\Sigma L} \\ \frac{\alpha}{\Sigma L} & 0 & -\frac{\alpha}{\Sigma L} \\ 0 & 0 & 0 \end{bmatrix} \quad B_3 = \begin{bmatrix} 0 & \frac{\alpha}{\Sigma L} & -\frac{\alpha}{\Sigma L} \\ 0 & -\frac{1}{\Sigma L} & \frac{1}{\Sigma L} \\ 0 & 0 & 0 \end{bmatrix} \quad B_5 = \begin{bmatrix} \frac{1}{\Sigma L} & 0 & 0 \\ -\frac{\alpha}{\Sigma L} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad B_7 = \begin{bmatrix} 0 & -\frac{\alpha}{\Sigma L} & 0 \\ 0 & \frac{1}{\Sigma L} & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$B_2 = B_4 = B_6 = B_8 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Substitution of the value A_1-A_8 and B_1-B_8 will obtain,

$$A = A_1 \quad (8.45)$$

$$B = (D)(B_1 + B_3 + B_5 + B_7) \quad (8.46)$$

The process of small signal modelling involves linearizing the non-linear elements within a converter with respect to the duty cycle, denoted by $\overline{D}$ .This method examines the effect of a small perturbation in the duty ratio, represented as d on the overall system. The ratio of the change in duty ratio, d to the original duty ratio, $\overline{D}$, is typically quite small [103], [104].

Consider the presence of a small signal variation d with respect to the duty ratio D, which will result in a corresponding small variation x of the state variable X. Therefore the variation of the small signal model can be represented as follows:

$$\dot{\bar{X}} + \dot{x} = A_1(\bar{X} + x) + ((D)(B_1 + B_3 + B_5 + B_7))Y \tag{8.47}$$

Expanding the equation (8.48),

$$\dot{\bar{X}} + \dot{x} = A_1\bar{X} + A_1x + (\bar{D}(B_1 + B_3 + B_5 + B_7) + d(B_1 + B_3 + B_5 + B_7))Y \tag{8.48}$$

Eliminating the large variable in the equation (8.48) gives:

$$\dot{x} = A_1x + (d(B_1 + B_3 + B_5 + B_7))Y \tag{8.49}$$

The equation above follows that

$$\dot{x} = Ax + Fd \tag{8.50}$$

Where,

$$A = \begin{bmatrix} 0 & 0 & -\frac{1}{\mathrm{SL}_1} \\ 0 & 0 & -\frac{1}{\mathrm{SL}_1} \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{8.51}$$

$$F = (B_1 + B_3 + B_5 + B_7)Y = = \begin{bmatrix} \frac{V_{dc}}{\Sigma Lx} \\ \frac{V_{dc}}{\Sigma Lx} \\ 0 \end{bmatrix} \tag{8.52}$$

A is the average of A for one cycle while F is the difference of Equations of the on-state and the off-state of X.

The equation can be solved in s-domain by Laplace Transform to convert it into a transfer function

$$\frac{\dot{x}}{d} = [sI - A]^{-1}F \tag{8.53}$$

Since,

$$adj(sI - A)\,F = \begin{bmatrix} s^2 + s\frac{1}{R\,C} + \frac{1}{\Sigma LxC} & -\frac{1}{\Sigma LxC} & -\frac{s}{\Sigma Lx} \\ -\frac{1}{\Sigma LxC} & s^2 + s\frac{1}{R\,C} + \frac{1}{\Sigma LxC} & \frac{s}{\Sigma Lx} \\ \frac{s}{C} & \frac{s}{C} & s^2 \end{bmatrix} \begin{bmatrix} \frac{V_{dc}}{\Sigma Lx} \\ \frac{V_{dc}}{\Sigma Lx} \\ 0 \end{bmatrix} \tag{8.54}$$

$$det(sI - A) = s^3 + s^2\frac{1}{R\,C} + s\frac{2}{\Sigma LxC} \tag{8.55}$$

Therefore,

$$\frac{\dot{x}}{d} = [sI - A]^{-1}\,F = \frac{\begin{bmatrix} \frac{V_{dc}}{\Sigma Lx}(s + \frac{1}{R\,C}) \\ \frac{V_{dc}}{\Sigma Lx}\left(s + \frac{1}{R\,C}\right) \\ \frac{2V_H}{C\,\Sigma Lx} \end{bmatrix}}{s^2 + s\frac{1}{R\,C} + \frac{2}{\Sigma LxC}} \tag{8.56}$$

Finally, the voltage transfer function :

$$\frac{\dot{V}_{ld}}{d} = \frac{2V_{dc}}{C\,\Sigma Lx}\frac{1}{s^2 + s\frac{1}{R\,C} + \frac{2}{\Sigma LxC}} \tag{8.57}$$

If $\frac{\mathrm{d}i}{dt} = \frac{di_A}{dt} = \frac{di_B}{dt}$, the current transfer function :

$$\frac{i}{d} = \frac{V_{dc}}{\Sigma Lx}\frac{(s + \frac{1}{R\,C})}{s^2 + s\frac{1}{R\,C} + \frac{2}{\Sigma LxC}} \tag{8.58}$$

Similar steps for the operation of the converter when 0.25 <D <0.5, 0.5 <D< 0.75 and 0.75<D< can be seen in Appendix A1. They follow voltage balancing process, although they have different sequences during its operation.

In the case of discrete inductor instead of coupled being used, the inductor variable ΣL_1 is equal to inductor value because there is no magnetizing effect from the other inductor from another phase

The voltage and current transfer function of B3LI DC/DC Converter are second order transfer functions in the s-domain. The system possesses two left-half plane conjugate poles, indicating stability with an oscillatory response. Additionally, it features one left-half-plane zero in the current transfer function, necessitating further design considerations in the control system to maintain stability in the closed-loop control of current. While, the voltage transfer function does not have zeros, implying that the control loop is stable.

Appendix 4.2 Small-signal Modelling of the converters during boost operation

Assuming the operating point is around on 0.75< D< 1

Interval 1 : D-0.75 (1111)

$$v_A = V_{ld} \tag{8.59}$$

$$v_B = V_{ld} \tag{8.60}$$

$$\frac{di_A}{dt} = \frac{di_B}{dt} = \frac{(1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.61}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{dc} \end{bmatrix} + \begin{bmatrix} 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{ld} \end{bmatrix} = A_1 X + B_1 Y \tag{8.62}$$

Interval 2 : 1-D (1101)

$$v_A = V_{ld} \tag{8.63}$$

$$v_B = V_{ld} + V_{cfB} - V_{dc} \tag{8.64}$$

$$\frac{di_A}{dt} = \frac{(1-\alpha)V_L - \alpha V_{cfB} + \alpha V_{dc}}{(1-\alpha^2)L} \tag{8.65}$$

$$\frac{di_B}{dt} = \frac{(1-\alpha)V_L + V_{cfB} - V_{dc}}{(1-\alpha^2)L} \tag{8.66}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{\alpha}{\Sigma \mathrm{L}} \\ 0 & 0 & -\frac{1}{\Sigma L} \\ 0 & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{dc} \end{bmatrix} + \begin{bmatrix} 0 & -\frac{\alpha}{\Sigma \mathrm{L}} & \frac{1}{\Sigma Lx} \\ 0 & \frac{1}{\Sigma \mathrm{L}} & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{ld} \end{bmatrix} = A_2X + B_2Y$$

(8.67)

Interval 3 : D-0.75 (1111)

$$v_A = V_{ld} \tag{8.68}$$

$$v_B = V_{ld} \tag{8.69}$$

$$\frac{di_A}{dt} = \frac{di_B}{dt} = \frac{(1-\alpha)V_{ld}}{(1-\alpha^2)ld} \tag{8.70}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{dc} \end{bmatrix} + \begin{bmatrix} 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{ld} \end{bmatrix} = A_3X + B_3Y$$

(8.71)

Interval 4 : 1-D (1011)

$$v_A = V_{ld} - V_{cfA} \tag{8.72}$$

$$v_B = V_L \tag{8.73}$$

$$\frac{di_A}{dt} = \frac{(1-\alpha)V_{ld} - V_{cfA}}{(1-\alpha^2)L} \tag{8.74}$$

$$\frac{di_B}{dt} = \frac{(1-\alpha)V_{ld} + \alpha V_{cfA}}{(1-\alpha^2)L} \tag{8.75}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{1}{\Sigma L} & 0 & \frac{1}{\Sigma Lx} \\ \frac{\alpha}{\Sigma L} & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{ld} \end{bmatrix} = A_4X + B_4Y$$

(8.76)

Interval 5 : D-0.75 (1111)

$$v_A = V_{ld} \tag{8.77}$$

$$v_B = V_{ld} \tag{8.78}$$

$$\frac{di_A}{dt} = \frac{di_B}{dt} = \frac{(1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.79}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{dc} \end{bmatrix} + \begin{bmatrix} 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{ld} \end{bmatrix} = A_5X + B_5Y \tag{8.80}$$

Interval 6 : 1-D (1110)

$$v_A = V_{ld} \tag{8.81}$$

$$v_B = V_L - V_{cfB} \tag{8.82}$$

$$\frac{di_A}{dt} = \frac{(1-\alpha)V_{ld} + \alpha V_{cfB}}{(1-\alpha^2)L} \tag{8.83}$$

$$\frac{di_B}{dt} = \frac{V(1-\alpha)_{ld} - V_{cfB}}{(1-\alpha^2)L} \tag{8.84}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{dc} \end{bmatrix} + \begin{bmatrix} 0 & \frac{\alpha}{\Sigma \mathrm{L}} & \frac{1}{\Sigma Lx} \\ 0 & -\frac{1}{\Sigma \mathrm{L}} & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{ld} \end{bmatrix} = A_6X + B_6Y \tag{8.85}$$

Interval 7 : D-0.75 (1111)

$$v_A = V_{ld} \tag{8.86}$$

$$v_B = V_{ld} \tag{8.87}$$

$$\frac{di_A}{dt} = \frac{di_B}{dt} = \frac{(1-\alpha)V_{ld}}{(1-\alpha^2)L} \tag{8.88}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{dc} \end{bmatrix} + \begin{bmatrix} 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{ld} \end{bmatrix} = A_7X + B_7Y \tag{8.89}$$

Interval 8 : 1-D (0111)

$$v_A = V_{ld} + V_{cfA} - V_{dc} \tag{8.90}$$

$$v_B = V_L \tag{8.91}$$

$$\frac{di_A}{dt} = \frac{(1-\alpha)V_L + V_{cfA} - V_{dc}}{(1-\alpha^2)L} \tag{8.92}$$

$$\frac{di_B}{dt} = \frac{(1-\alpha)V_L - \alpha V_{cfA} + \alpha V_{dc}}{(1-\alpha^2)L} \tag{8.93}$$

$$\begin{bmatrix} \frac{di_A}{dt} \\ \frac{di_B}{dt} \\ \frac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma L} \\ 0 & 0 & \frac{\alpha}{\Sigma L} \\ \frac{1}{C} & 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ V_{dc} \end{bmatrix} + \begin{bmatrix} \frac{1}{\Sigma L} & 0 & \frac{1}{\Sigma Lx} \\ -\frac{\alpha}{\Sigma L} & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{cfA} \\ V_{cfB} \\ V_{ld} \end{bmatrix} = A_8 X + B_8 Y \tag{8.94}$$

For one cycle operation

$$A = (D-0.75)A_1 + (1-D)A_2 + (D-0.75)A_3 + (1-D)A_4 + (D-0.75)A_5 + (1-D)A_6 + (D-0.75)A_7 + (1-D)A_8 \tag{8.95}$$

$$B = (D-0.75)B_1 + (1-D)B_2 + (D-0.75)B_3 + (1-D)B_4 + (D-0.75)B_5 + (1-D)B_6 + (D-0.75)B_7 + (1-D)B_8 \tag{8.96}$$

$$A_1 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix} \quad A_2 = \begin{bmatrix} 0 & 0 & \frac{\alpha}{\Sigma L} \\ 0 & 0 & -\frac{1}{\Sigma L} \\ 0 & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad A_3 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix} \quad A_4 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix}$$

$$A_5 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{1}{RC} \end{bmatrix} \quad A_6 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix} \quad A_7 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix} \quad A_8 = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma L} \\ 0 & 0 & \frac{\alpha}{\Sigma L} \\ \frac{1}{C} & 0 & -\frac{1}{RC} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} 0 & -\frac{\alpha}{\Sigma L} & \frac{1}{\Sigma L_1} \\ 0 & \frac{1}{\Sigma L} & \frac{1}{\Sigma L_1} \\ 0 & 0 & 0 \end{bmatrix} \quad B_3 = \begin{bmatrix} 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \quad B_4 = \begin{bmatrix} -\frac{1}{\Sigma L} & 0 & \frac{1}{\Sigma Lx} \\ \frac{\alpha}{\Sigma L} & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix}$$

$$B_5 = \begin{bmatrix} 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \quad B_6 = \begin{bmatrix} 0 & \frac{\alpha}{\Sigma \mathrm{L}} & \frac{1}{\Sigma Lx} \\ 0 & -\frac{1}{\Sigma \mathrm{L}} & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \quad B_7 = \begin{bmatrix} 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & \frac{1}{\Sigma Lx} \\ 0 & 0 & 0 \end{bmatrix} \quad B_8 = \begin{bmatrix} \frac{1}{\Sigma \mathrm{L}} & 0 & \frac{1}{\Sigma \mathrm{L}1} \\ -\frac{\alpha}{\Sigma \mathrm{L}} & 0 & \frac{1}{\Sigma \mathrm{L}1} \\ 0 & 0 & 0 \end{bmatrix}$$

Substitution of the value A_1-A_8 and B_1-B_8 will obtain,

$$A = (2D - 1)A_1 + (1 - D)(A_2 + A_8) \tag{8.97}$$

$$B = (4D - 3)B_1 + (1 - D)(B_2 + B_4 + B_6 + B_8) \tag{8.98}$$

$$\dot{\bar{X}} + \dot{x} = ((2\bar{D} + 2d - 1)A_1 + (1 - \bar{D} - d)(A_2 + A_8))(\bar{X} + x)$$
$$+ ((4\bar{D} + 4d - 3)B_1 + (1 - \bar{D} - d)(B_2 + B_4 + B_6 + B_8))Y$$

A small perturbation in the duty ratio resulted small signal equation as follow

Expanding the equation,

$$\dot{\bar{X}} + \dot{x} = \big((2\bar{D} + 1)A_1 + (2d)A_1 + (1 - \bar{D})(A_2 + A_8) - (d)(A_2 + A_8)\big)\bar{X} +$$
$$\big((2\bar{D} + 1)A_1 + (2d)A_1 + (1 - \bar{D})(A_2 + A_8) - (d)(A_2 + A_8)\big)x +$$
$$((4\bar{D} - 3)B_1 + (4d)B_1 + (1 - \bar{D})(B_2 + B_4 + B_6 + B_8) - d(B_2 + B_4 + B_6 + B_8))Y$$

If the small-signal is zero,

$$\dot{\bar{X}} + \dot{x} = \big((2\bar{D} + 1)A_1 + (1 - \bar{D})(A_2 + A_8) + (d)(A_2 + A_8)\big)\bar{X} +$$
$$((4\bar{D} - 3)B_1 + (1 - \bar{D})(B_1 + B_3 + B_5 + B_7))Y$$

Eliminating the equation gives:

$$\dot{x} = (2d)A_1 - (d)(A_2 + A_8)\bar{X} +$$
$$\big((2\bar{D} + 1)A_1 + (2d)A_1 + (1 - \bar{D})(A_2 + A_8) - (d)(A_2 + A_8)\big)x +$$
$$((4d)B_1 - (d)(B_1 + B_3 + B_5 + B_7))\mathrm{Y}$$

Neglecting the high order small signal variation

$$\dot{x} = -(A_2 + A_4 + A_6 + A_8)d + 4d(A_1))\bar{X}$$
$$+ \big((1 - \bar{D})(A_2 + A_4 + A_6 + A_8) + (4\bar{D} - 3)A_1\big)x$$
$$+ (-(B_2 + B_4 + B_6 + B_8)d + 4d(B_1))Y) \tag{8.99}$$

The average of A for one cycle and the difference of equations of the on-state and the off-state of X are :

$$\dot{x} = (2d)A_1 - (d)(A_2 + A_8)\bar{X} + \big((2\bar{D} + 1)A_1 + (1 - \bar{D})(A_2 + A_8)\big)x + ((4d)B_1 - (d)(B_2 + B_4 + B_6 + B_8))\mathrm{Y} \tag{8.100}$$

$$A = (2\bar{D} + 1)A_1 + (1 - \bar{D})(A_2 + A_8)$$
$$F = \big(2A_1 - (A_2 + A_8)\big)\bar{X} + (4B_1 - (B_2 + B_4 + B_6 + B_8))\mathrm{Y} \tag{8.101}$$

Therefore,

$$\mathrm{A} = \begin{bmatrix} 0 & 0 & -\frac{1-D}{\Sigma Lx} \\ 0 & 0 & -\frac{1-D}{\Sigma Lx} \\ \frac{1-D}{\mathrm{C}} & \frac{1-D}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix}, \text{ and } \mathrm{F} = \begin{bmatrix} \frac{V_{dc}}{\Sigma Lx} \\ \frac{V_{dc}}{\Sigma Lx} \\ \frac{i_A + i_B}{\mathrm{C}} \end{bmatrix} if \ i_A = i_B = i_L \text{ then } \mathrm{F} = \begin{bmatrix} \frac{V_{dc}}{\Sigma Lx} \\ \frac{V_{dc}}{\Sigma Lx} \\ -\frac{2i_L}{\mathrm{C}} \end{bmatrix} \tag{8.102}$$

Solving the Equation using Laplace Transform to gives:

$$\frac{\dot{x}}{d} = [sI - A]^{-1} F = \frac{\begin{bmatrix} \frac{V_{dc}}{\Sigma Lx} s + \frac{1}{\Sigma Lx\mathrm{C}}\left(\frac{V_{dc}}{\mathrm{R}} + 2i_L(1-D)\right) \\ \frac{V_{dc}}{\Sigma Lx} s + \frac{1}{\Sigma Lx\mathrm{C}}\left(\frac{V_{dc}}{\mathrm{R}} + 2\, i_L(1-D)\right) \\ 2\left(V_{dc}\frac{1-D}{\Sigma Lx} - s\,\frac{i_L}{\mathrm{C}}\right) \end{bmatrix}}{s^2 + \frac{1}{\mathrm{RC}}\mathrm{s} + \frac{(1-D)^2}{\Sigma Lx\, C}} \tag{8.103}$$

The above voltage transfer function can be represented in term of V_L and I_L laced using the relationship as follow:

$$2I_L = \frac{I_{dc}}{1-D} = \frac{V_{dc}}{R\,(1-D)} \tag{8.104}$$

$$V_{dc} = \frac{V_{ld}}{1-D} \tag{8.105}$$

Therefore the voltage transfer function is :

$$\frac{\dot{V}_{dc}}{d} = 2\frac{V_{ld}}{RC\ (1-D)^2}\ \ \frac{\left(\frac{R(1-D)}{\Sigma Lx} - s\right)}{s^2 + \frac{s}{\mathrm{RC}} + \frac{(1-D)^2}{\Sigma Lx\ C}} \tag{8.106}$$

And the current transfer function is:

$$\frac{i}{d} = \frac{V_{ld}}{\Sigma Lx(1-D)}\ \frac{s + \frac{2}{\mathrm{RC}}}{s^2 + \frac{s}{\mathrm{RC}} + \frac{(1-D)^2}{\Sigma Lx\ C}} \tag{8.107}$$

Appendix 5. PV Panel model and MPPT Control

Appendix 5.1 : PV Panel model

The PV panel presented in simulation based on manufacturers datasheets of LG365Q1C-A5 PV panel, this pv panel type is Monocrystalline / N-type with parameter as in table B.1

Table B.1 LG365Q1C-A5 parameter

Parameter	Value	Unit
Maximum power	365	W
Open circuit voltage (Voc)	42.8	V
Short circuit current (Isc)	10.8	A
MPP voltage (Vmpp)	36.7	V
MPP current (Impp)	9.95	A
Efficiency	21.1	%
Dimension (LxWxH)	1,700 x 1,016 x 40	mm

Source: datasheet LG365Q1C-A5

PV panel model follow reference [6] to find maximum power point which expressed in Equation A1-A3where The coefficients C_1 and C_2 depend on short circuit current (I_{SC}), open circuit voltage (V_{OC}), maximum power point voltage (V_{MPP}) and maximum power point current (I_{MPP}.) which is expressed in Equation

$$I_{PV} = I_{SC}.\left[1 - C_1\left(e^{\left(\frac{V_P}{C_2 V_{oc}}\right)} - 1\right)\right] \tag{8.108}$$

Where,

$$C_1 = \left(1 - \frac{I_{MPP}}{I_{SC}}\right).e^{\left(\frac{-V_{MPP}}{C_2 V_{oc}}\right)} \tag{8.109}$$

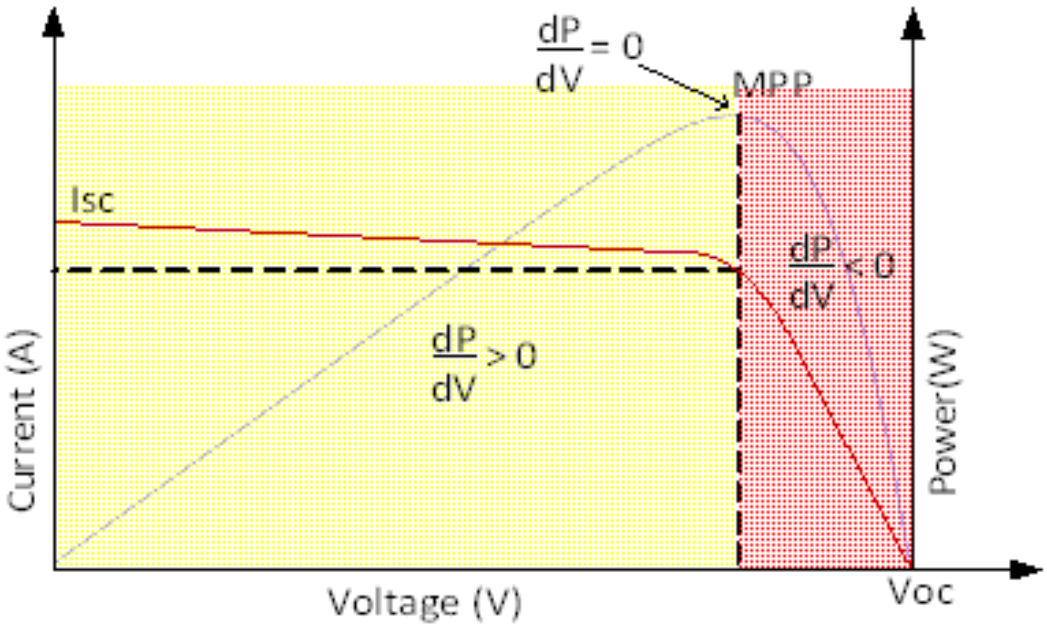
$$\mathrm{C_2} = \frac{\left(\frac{\mathrm{V_{MPP}}}{\mathrm{V_{oc}}} - 1\right)}{\ln\left(1 - \frac{\mathrm{I_{MPP}}}{\mathrm{I_{SC}}}\right)} \tag{8.110}$$

Appendix 5.2 : MPPT algorithm

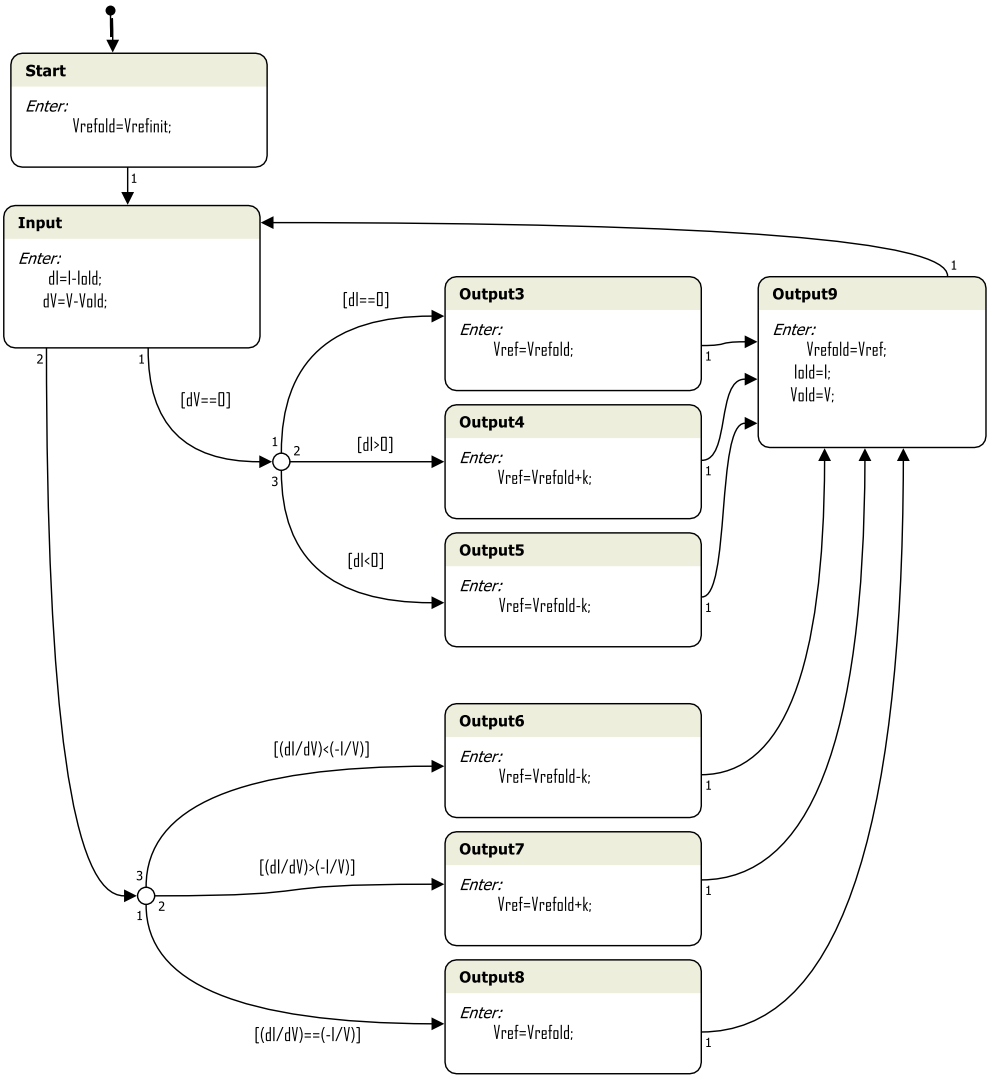
Incremental conductance is a mature method to find MPP. It tracks the MPP by comparing the instantaneous and incremental conductance of the PV array. The MPP achieved when dP/dV is equal to zero. If dP/dV less than 0 means that the voltage should be increased. Vice versa when dP/dV > 0, the voltage reference will be decreased.

$$\frac{dP}{dV} = I + V\frac{dI}{dV} = 0 \tag{8.111}$$

$$\frac{I}{V} = -\frac{dI}{dV} \tag{8.112}$$



(a)



(b)

Appendix 5.2 (a) incremental conductance method. (b) MPPT algorithm implementation in state machine in PLECS