Silent Switching

- EMI suppression without conventional EMI filters

Zhe Zhang

Thesis submitted to the University of Nottingham for

the degree of Doctor of Philosophy

Department of Electrical and Electronics Engineering

University of Nottingham

2018

Abstract

Electromagnetic Interference (EMI) has been a major concern when utilising Wide Band Gap (WBG) devices such as SiC (Silicon Carbide) and GaN (Gallium Nitride) for power conversion system. Electromagnetic interference arises from the rapid voltage and current transitions occurring during operation of the switching cell. Suppression of electromagnetic interference is typically achieved by a combination of filtering including differential and common mode filters, to attenuate conducted emissions and shielding to attenuate radiated emissions. The purpose of adding filters is to block the noise propagation (high impedance) and to bypass the noise (low impedance at high frequency for capacitors). On the top of understanding the source of EMI and impedance of noise propagation path, the attenuation from passive filters can be controlled to suppress EMI noise to acceptable levels that meet with various EMC (Electromagnetic compatibility) standards. Typically such features are added at converter and system levels but not integrated into the switching cell. At frequencies below several MHz, passive filters typically provide enough noise attenuation, however, at higher frequencies, filter performance is compromised by parasitic inductance and capacitance within the filter system and by mutual electromagnetic coupling between filter stages. In addition the bypass route for high frequency noise back to its noise source might not be effective due to the parasitic impedance in the noise current path. Therefore the realisation of wide-band noise filters becomes challenging with conventional filter configurations.

As the conventional approach of tackling EMI, passive EMI filters are used to attenuate noise outside the switching cell. The passive EMI filters normally include a combination of common mode and differential mode filters which are used at both input and output to attenuate conducted noise and shunt high frequency noise back to its noise source. Such filters may consist of two inductors are wound on a common core as a common

mode whose magnetic leakage is used as differential mode choke and several noise shunt capacitors across each line and the ground to return high frequency noise. Normally the EMI filter would occupy about 10% - 20% of the overall system size[1][2]. As the switching speed becomes faster, much larger EMI filter would be necessary for higher level of EMI noise attenuation [3].

In this thesis, in contrast to this conventional method, we propose an alternative approach to solve EMI problems within the switching cell. By applying partial or complete conductive partitions or by embedding an electrically conductive screen layer, internally generated switching noise is returned to the source via an internal screen layer. Common mode noise which would otherwise be capacitively coupled to ground is returned direct to the screen. Internally generated magnetic fields are attenuated in screen layer or in additional shielding layers whose thickness and extent are chosen to produce the desired degree of attenuation. On the top of screening and shielding techniques, differential mode noise is attenuated by low-pass filters that are applied in each of the electrical ports and whose high-freqeuncy return currents are directed back to the screen and hence to the noise source. This thesis also focuses on the achievement of high attenuation, across a wide bandwidth, for differential mode noise at the electrical ports. A new concept of suppressing electromagnetic interference by using multistage integrated filters within switching cells has been proposed to contain EMI noise. Furthermore, the techniques of partitioning each filter stage to improve noise attenuation at very high frequencies and feedthrough connection to decouple EMI field coupling have been proved to achieve attenuation levels of over -120dB up to 1GHz. In the end, a GaN power converter with 1MHz switching frequency is used as a test bed to confirm the effectiveness of EMI noise attenuation with each intervention. A silent switching environment has been confirmed on this GaN power converter when all interventions applied.

Acknowledgment

I would like to thank all people who helped me to complete this research. First my parents provide me with great metal and physical support during my PhD study at University of Nottingham. Second, special thanks to my supervisor Prof. Mark Johnson who offered me such a great opportunity of expending my knowledge on power electronics from power devices to system level integration, and who has been very kind an ultimately supportive during all stages of my research. Also many thanks to all the people from Mark`s research group Pearl Agyakwa, Marti Corfield, Li Yang, Bassen Mouawad, Jiangfeng Li, Ke Li, Amir Eleffendi and researchers from PEMC group, who have helped me throughout my PhD study.

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Chapter 1. Introduction

1.1 From EMI to EMC

Environmental Electromagnetic Interference (EMI) originates from the widespread use of electronic circuits / systems for communication, computing, power processing, automation, and other purposes. Electromagnetic interference is defined as an undesirable electromagnetic noise that corrupts, limits or interferes with performance of electronics or electrical systems[4]. This has been a serious problem for electrical and electronic equipment for years. Any electrical or electronic device is a potential noise source to its environment.[5] High-level electromagnetic disturbance may cause electrical and electronic devices and systems to malfunction in a common electromagnetic environment. EMI becomes even more critical with the constant size reduction of electronic circuits and the increased level of system integration.

It is common to categorise EMI studies into four groups: conducted susceptibility, radiated susceptibility, conducted emissions and radiated emissions. The susceptibility or immunity issues represent the ability of electrical equipment to reject the noise in the presence of external electromagnetic disturbance. The studies of conducted and radiated emissions deals with the undesirable generation of electromagnetic noise from a piece of equipment and the countermeasure that can be taken to reduce it [6]. These emissions are regulated and need to comply with the rule of electromagnetic compatibility (EMC), which is defined as the ability of a device, unit of equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment. This research is focused on conducted and radiated EMI emission which is generally defined as undesirable electromagnetic energy coupled out of an emitter or into a receptor via any of its respective connecting wires or cables.

1.2 EMI in Power Electronics

Over the past ten years, there has been increased integration of power electronic converters in “more electric” cars, ships, and airplanes to replace thermo-mechanical, mechanical, hydraulic, and pneumatic primary and secondary power systems [7][8]. Power electronic converters have been introduced with the goals of reducing the size, weight, and maintenance and operational costs of these power systems, while increasing efficiency, safety, reliability, and optimizing mission-specific objectives[9]. However, power converters based on power electronics are important sources of electromagnetic perturbations that can occasionally cause malfunctions in their local or distant electronic environments, such as avionics, navigation systems, reception antennae, etc.

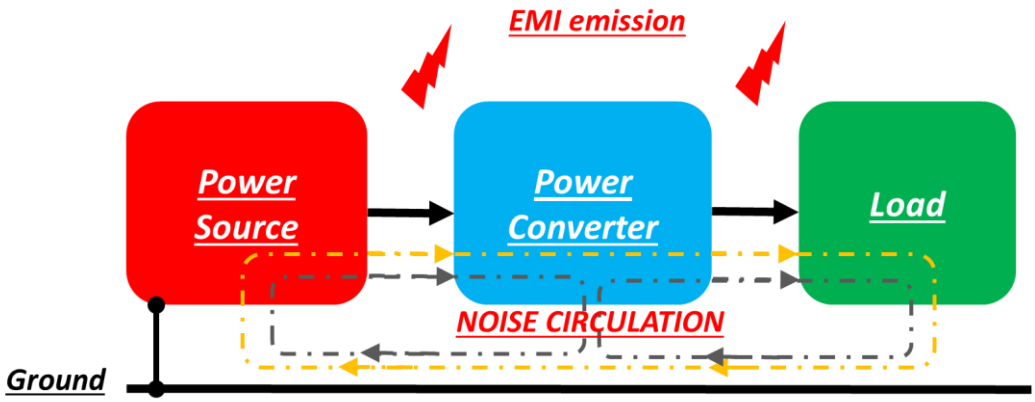


Figure 1-1 EMI noise circulation within power system

Converters carrying out the processing of electrical energy (conditioning, control) are based on the switching of semiconductors. This involves power components (Insulated Gate Bipolar Transistor (IGBT), Metal Oxide Silicon Field Effect Transistor (MOSFET), diodes, etc.) operating in a switching mode, which ensures a very high efficiency compared to operation in the linear mode. The consequences of the perturbation emitted by the switching power devices can be very serious in terms of the reliability and/or

security of systems. The switching of power semiconductors can cause conducted and radiated electromagnetic perturbations that cover a very large frequency range as shown in **Figure 1-2**.

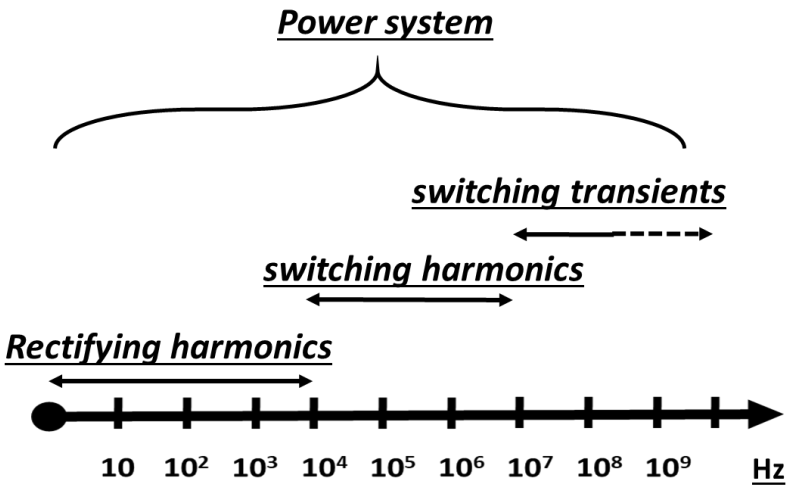


Figure 1-2 Frequency range of power electronic system 【7】

At low frequency from the network frequency of 50Hz the direct switching of silicon based diode or thyristor rectifiers, of triac dimmers in synchronization with the network frequency, generates perturbations observable up to a few tens of kilohertz. At medium frequency (ranging from 10 KHz to 10 MHz) the switching of controlled semiconductors (MOSFET, IGBT) in switched-mode power supplies, choppers and power inverters produces noise at the switching frequency and its harmonics [10]. At SiC applications, the commuted quantities show very quick temporal variations (of the order of a few 10kV/us and a few 100A/us) with extremely large spectral content during switching. The rapid transients produced in switching of semiconductors excite the normal modes of very low resistance electrical circuits (necessary for small losses). Thus, very high frequency resonances appear (10MHz-1GHz) during each switching between the parasitic inductances of connections (or of magnetic components) and the structural capacitances of the semiconductors.

1.3 New challenge on EMI (fast switching devices)

Power electronics has revolutionized the way we process power to meet the growing energy need of our society. The introduction of fast switching power semiconductor devices has greatly improved the dynamic response, efficiency and overall performance of the power converters. The fast switching power semiconductor devices provide the opportunity to reduce the size of the power converters and the energy storage components, in other words, reduce system weight/size and increase the power density of the system[11][12]. Recently increased availability of silicon carbide (SiC) and gallium nitride (GaN) devices has opened new opportunities for designing power converters that operate at increased switching frequencies with higher voltages and lower losses, to reduce the size/weight of the passive components for energy storage[13][14][15][16]. For example, the high electrical blocking capability of SiC power devices allows fabrication of much thinner and higher doped drift layers, significantly reducing the on-state resistance. The high thermal conductivity of SiC (4.9 W/cm·K) enhances heat dissipation and the wide bandgap energy (3.3 eV) allows high-temperature operation above 300 °C. Among the advantages SiC and GaN could bring, the characteristic of very fast switching speed has attracted much attention of researchers, since fast switching could reduce energy losses, and reduce size of passive electrical components (e.g. inductor). Several studies [17][18] have shown that using these advanced devices can push the switching frequency of the converters to several mega-hertz for kilowatt level converters. With improved module integration and packaging technologies that reduce parasitics, the power density of the power converters can be improved significantly.

However, faster switching devices bring additional electromagnetic interference (EMI) problems into the system. With the increase of the switching speed of the emerging advanced semiconductor devices, the dv/dt and di/dt transitions during the device switching become much higher than in traditional silicon (Si) devices[19][20]. The

switching energy is moved to higher frequencies, and both conducted and radiated noise emissions become much higher than in Si systems, which aggravates the EMI problems [21][22]. Therefore, it is a big challenge for modern power electronic systems to design and integrate the power converter and EMI filter together to minimize total weight/size and thus improve system power density.

1.4 Mechanism of EMI coupling and suppression solutions

The switching function is the major mechanism of electromagnetic noise generation, and both conducted and radiated EMI have become major problems which make EMC design essential.

The goal of studying conducted EMI is to understand how the noise is generated and to find the best solution to reduce or eliminate it in order to meet the EMC requirement for the device or system. **Figure 1-3** summarises the relationship between EMI noise source and different ways of EMI noise propagation.

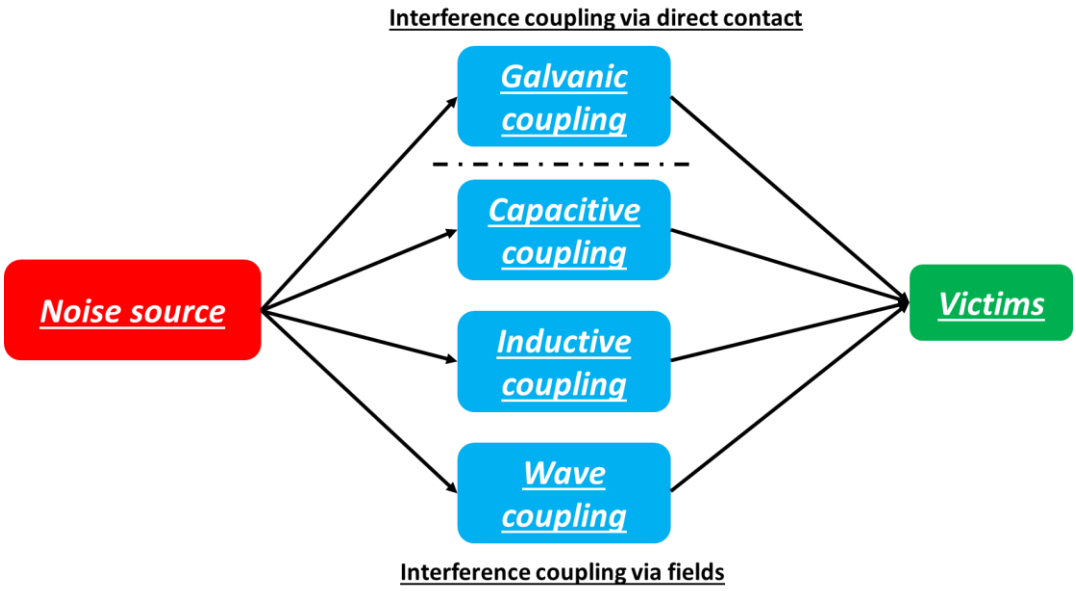


Figure 1-3 Interference coupling mechanism

The noise source:

The switching function at the basic operation of electronic power is the EMI noise source. There has been a lot of research on reducing EMI noise at source during switching transitions. Most have focused on improving circuit topologies by applying soft-switching technologies, and active or passive snubbers to suppress the HF EMI noise. However, the noise at switching frequency and its harmonics are inherent to the switching function, which cannot be alleviated completely by most soft-switching techniques or advanced semiconductor devices.

The noise coupling:

- **Galvanic coupling**:

EMI noise propagates through electrical connections at all frequencies.

- **Capacitive coupling**:

EMI noise propagates through electrical field coupling. This transmission path is quite common at the output traces or terminals, where very sharp edge of voltage pulses charge and discharge the parasitic capacitance between output trace and ground or another reference potential.

- **Inductive coupling**:

EMI noise propagates through magnetic field coupling. This transmission path is quite common in switched-mode power supplies since high frequency currents in the inductors can cause strong magnetic fields at higher frequencies, Or simply from high current tracks coupling with control circuits.

- **Wave coupling**:

EMI noise normally has very high frequency spectrum and is transmitted via an electromagnetic wave. Wave coupling characterised by generalised electromagnetic coupling and implies propagating EM waves i.e. far field radiated coupling vs. near field magnetic or electric coupling where the effects are generally dominated by one or the other.

This research will focus on galvanic, capacitive, and inductive coupling as they are the most important sources of EMI issues in power electronics applications. It is generally accepted industry practice to consider conducted EMI below 30MHz, radiated EMI above 30MHz, and in most cases up to 1GHz. In addition, at some avionics applications, EMI standard is defined as from 150kHz to 152MHz for conducted emission and from 100MHz to 6GHz for radiated emission (DO-160).

The most common and easiest way to avoid interference of the EMI noise emissions from the power electronics is to focus on galvanic coupling by inserting passive filter(s) to attenuate the noise[23]. These passive components form a significant portion of the total volume and weight of converters. In some applications, filters are needed for both the input and output of the converter, and the additional EMI filter weight may diminish the benefits power electronic converters have over traditional systems, and even make the total weight and size greater. Methods of active cancelling usually apply active devices and control to compensate for the dv/dt transients generated by PWM switching scheme, generally an extra winding is needed to form a coupled transformer which generates the opposite voltage to the other three inverter phases. The other techniques include: modification of PWM strategy, impedance balancing, modification of motor structure, etc. A detailed review of the principal EMC design strategies will be provided in the Chapter 2

1.5 Motivations

1.5.1 Problem descriptions

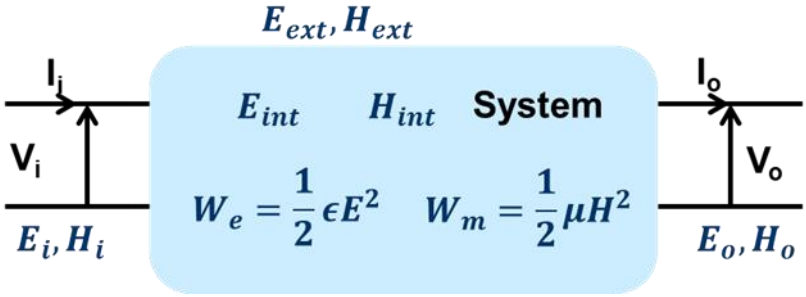


Figure 1-4 Electromagneitc interferece within power electronic system.

Most EMI solutions tend to tackle EMI issue from the perspective of galvanic coupling, and are very effective at "low" frequencies. However, at high frequency, electrical coupling and magnetic coupling modes cannot be treated separately since electric and magnetic field couple together, and electromagnetic coupling exists across the whole system. All electric circuit elements generate electromagnetic fields within the system, including intentional field such as electric and magnetic field stored in capacitors and inductors and unintentional stray field stored at parasitic inductance and capacitance. **Figure 1-4** indicates intentional and unintentional electric and magnetic field generated within a power electronic system. E_{int} and E_{ext} represent the internal and external electric field. H_{int} and E_{ext} represent internal and external magnetic field. Input side is on the left and output side is on the right. With the increase of switching speed, switching frequency and its harmonics are pushed into much higher frequency range. An awareness that power electronics with very fast switching devices has to be looked at as "high" frequency technology in order to control and prevent EMI issue is therefore necessary. However, as mentioned above, existing EMI techniques focus on either conducted EMI or radiated EMI problems separately and in each case different approaches are used to solve EMI problems. Every changing current flow (movement of charge) produces a changing magnetic field and changing magnetic field induce changing electric field. The parasitic capacitors and inductors are the enabler to spread the fast changing electric and magnetic

field, make it easy for EMI noise to propagate and contaminate electrical system. This point out the limitation of the conventional approach of separating conducted and radiated EMI noise and leads to the idea that they must be considered together. A new approach where unwanted electric and magnetic field coupling can be controlled over a wide frequency range (for example from 100s kHz to 1GHz is thus very important to realize effective EMI suppression for fast switching power electronics.

Common Mode (CM) noise current has been considered as a consequence of electric field coupling and CM noise attenuation is achieved by inserting high impedance in its propagation path, by connecting additional CM current filter next to the power converter or at load side such as next to the motor. However, a large proportion of CM current flows into the ground without being attenuated, which is due to a small yet finite capacitance existing between the power traces and the mounting baseplate. Very little effort has been put on how to attenuate CM current flow at the noise source, which is the switching cell other than, to prevent electric coupled noise current propagating outside but not to add some noise attenuation solutions afterwards.

Passive filters are widely used to supress the noise along the propagation path because the relatively low cost and high effectiveness. Numerous techniques, such as integration technology and parasitic cancellations. Integration technology is mostly realized by distributed inductance and capacitance, and behaves as an electromagnetically integrated LC structure. Parasitic cancellations is mostly realized by additional components added to cancel high influence parasitic components in inductor or capacitor. However, in practice, the filter components are not ideal and their characteristics deviate from those of the theoretical components. Parasitic component EPC (Equivalent Parasitic Capacitance) and ESL (Equivalent Series Inductance) cannot be eliminated completely and they determine filter performance and behaviour at very high

frequency. Also effects of electromagnetic coupling between each filter component and each filter stage dominate the effectiveness of filter performance at high frequency. Thus, for frequencies above 100MHz, it is very easy for noise to couple from the input side of filter directly to load side without going through each filter stage. Therefore careful electromagnetic field decoupling and containing are needed.

1.5.2 Thesis objectives

Based on the problems listed above, the objectives of this thesis are

To provide a new paradigm of considering EMI issue from the electromagnetic field perspective and suggest a guideline of conducted and radiated EMI noise attenuation step by step

To propose and demonstrate a new approach: the use of combination of screening and shielding to supress electromagnetic interference at the noise source which is the switching cell. (In this thesis, the phrase Screening is used at CM noise attenuation techniques and Shielding is used at radiated noise attenuation techniques)

To propose and demonstrate a broadband filter that can provide more than -100dB noise attenuation across 3-decade frequency range.

To demonstrate complete EMI suppression with new approach of EMI noise attenuation on a Wide Band Gap (WBG) converter switching at above 1MHz

1.5.3 Thesis layout

Chapter 2 reviews conventional EMI noise reduction from ① filter topology and optimization; ② switching cell layout optimization

Chapter 3 investigates the screening of common mode (CM) currents and the shielding of magnetic fields generated by a model switching cell using a combination of simulation tools and measurements.

Chapter 4 introduces the use of integrated filtering techniques to suppress EMI noise generated by a switching cell. Combinations of screening and shielding techniques are applied to multi-stage filters and evaluated over a broad frequency range

Chapter 5 demonstrate the effectiveness of EMI noise suppression with all techniques combined together at a GaN active device and prove achieving a silent switching environment

Chapter 6 concludes the achievements and recommends for future research of this thesis

1.5.4 Contributions to new knowledge

- ✓ UK patent: Broadband filter for suppression of electromagnetic interference (Processing)
- ✓ First Place award at Geoff Haynes Future Power Challenge 2018
- ✓ Publication:

  Suppression of Electromagnetic Interference Using Multi-Stage Integrated Filtering with Screening and Partitioning. Mar 2018 10th International Conference on Integrated Power Electronics.

  Suppression of Electromagnetic Interference Using Screening and Shielding Techniques Within The Switching Cells. Apr 2017 IEEE International Workshop on Integrated Power Packaging.

Chapter 2. Conventional EMI Suppressions in Power Electronics

2.1 Introduction

All power electronics must be designed so as not to interfere with other equipment in surroundings[24][25]. To ensure compliance with this requirement, numerous EMC standards are imposed by the authorized departments[6]. Conducted and radiated EMI emission is often defined as the undesirable electromagnetic energy emitting from an emitter and entering a receptor via any kind of connecting wires or cables and parasitic couplings[26][27]. The conventional EMC strategies for a power electronic system can be categorized into two basic ways[28]:

- Suppressing the EMI at the noise source
- Suppressing the EMI at the noise propagation paths

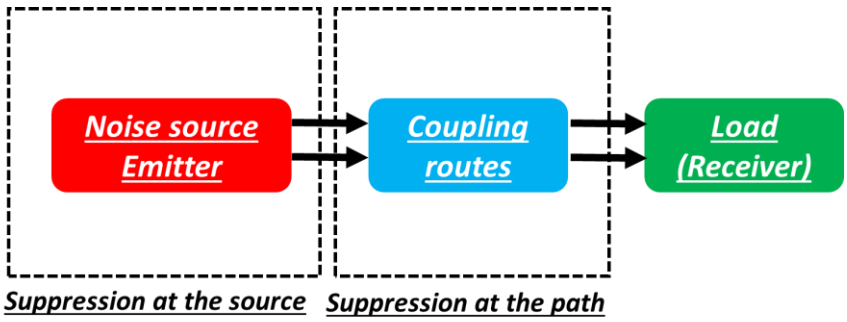


Figure 2-1 Illustration of EMI emission and EMC strategies

For the EMI suppression, normally passive suppression methods represent the use of a passive filter[29], due to their relevantly low cost, high efficiency and the fact that they are easy to implement. In order to meet the new requirement of high power density and high efficiency and better performance at power electronics, high speed switching capable wide Band Gap (WBG) devices such as GaN or SiC have been widely

investigated[30][31]. However, as shown in the work by Yuan and Walder [32][33], when the switching speed of transistor increases when utilising WBG devices, EMI level also increases significantly. As the switching speed increases, the current overshoot and ringings due to parasitic inductance and capacitance within the commutation loop become larger. The ringings can create more harmonic spikes in the EMI spectrum. This by-product of using WBG devices makes Electromagnetic Interference (EMI) become a major concern for inverter drives for instance, particularly when WBG-equipped converters are used in Electric Vehicles (EVs) or aircraft applications[34][35]. This is because the conducted and radiated EMI noise may cause malfunction of other electronic equipment within the system. In this chapter a common understanding of the mechanism of EMI generation and propagation is discussed and the recent research on EMI suppression techniques at both noise source and along the noise propagation path are compared.

2.2 Standards for conducted and radiated emission

Conducted emission

Standards of conducted EMI can be divided into civilian and military standards and further sub-divided into categories in accordance with different application environments[4]. There are four major standard imposing authorities[36]: the International Electromechanical Commission (IEC), the Federal Communications Commission (FCC) in the United States, and the European Committee for Electro-technical Standardization (CENELEC) and the European Telecommunications Standards Institute (ETSI) in European countries. IEC has the biggest number of committees and working groups that are active in more than 40 countries including the United States and most of the European countries. Nowadays, The Comité International Spécial des Perturbations

Radioélectriques (CISPR) has grown into a major authority issuing standards that are used worldwide. Examples of some main standards for conducted emission are[28][4][37]:

- CISPR 11: limits for industrial, scientific and medical radio frequency equipment
- IEC 61800-3: limits for variable speed electrical power drive systems
- EN 55011: limits and methods of measurement for industrial scientific and medical radio frequency equipment
- CISPR 16: measurement equipment and testing techniques

Some EMC standards stipulate the same limits, for example: IEC 60000 series, which define the safety characteristics of environments, measurement instructions, etc. and CISPR 11, which specifies the quality and interoperability requirements for specific equipment types or product families. For the harmonized standards, equipment is divided into two classes (class A and class B), according to the environment where the application of the equipment takes place, for example, residential, commercial, light industry and industry.

Radiated emission

On the other hand, for radiated emission the typical domestic/ commercial/industrial EN standards are over the frequency range of 30MHz to 1GHz[38][20]. In some specific case, the measurement range is over 1GHz, for instance for some types of radio-frequency (RF) equipment when applying EN 55011 (CISPR11). In some cases, the measurement is carried out below 30MHz, for example when measuring cable TV distribution systems. Military radiated emissions testing covers a much wider range that 30MHz to 1GHz. Most radiated EMC compliance mentioned above requires an antenna and anechoic chamber condition. For instance, a fully compliant test site includes a ground plane that stretches between the (Equipment Under Test) EUT's position and the measuring antenna and beyond them, a means of rotating the EUT and, for table top apparatus, of

positioning it 80cm above the plane, and a mast that allows the antenna to be scanned in height from 1 to 4m as well as giving both horizontal and vertical polarisation. The commercial standards allow three measurement distances, 3m, 10m and 30m, but the latter is very rarely used in practice and is not considered here.

2.3 Difficulties and limitation of the current EMC regulations

In power electronic applications, conventional Si based power devices have relatively slow switching speed and low switching frequency compared to WBG power devices. Their conducted noise spectrum starts from kHz range up to tens of MHz, due to ringing or resonant behaviour within system. Major efforts on EMI noise attenuation have therefore focussed around or below MHz range. However, with the increased use of wide band gap devices, the switching frequency has been pushed into hundreds of kHz or MHz range. It means that switching frequency and its harmonics are in the EMI regulation range. The frequency of switching harmonics and the noise originated from sharp edge of current and voltage transient which is less than 10ns might be able to reach the range above 30MHz. However, the existing conducted EMC regulation has no specific description about the noise level at the high frequency above 30MHz, and solutions of EMI suppression at that high frequency range has been overlooked at power electronic system design, only because it is not in the current EMC regulation range. Noise, generated at high frequencies (above 30MHz), could cause more problems through electromagnetic coupling than that at low frequency. Radiated EMI noise coupling in power electronics tends to occur through near-field or close-field radiation rather than far-field. Electromagnetic noise causes perturbation from the noise source through near-field electric or magnetic coupling. These couplings are proportional to the temporal derivative of the electrical quantities: M*di/dt and C*dv/dt (M is inductive coupling and C is capacitive coupling). Therefore, near-field electromagnetic couplings become very important, and how to control and manipulate the field coupling is the key to successful

EMI suppression. However, there is no specific radiated EMI standard with respect to near field/ close field radiation for power electronics.

In this research, in order to draw attention to the impact of noise spectrum at high frequency and to demonstrate the effectiveness of our proposed interventions on EMI noise attenuation, we extend the top end range of conducted EMI noise measurement from conventional 30MHz up to 200MHz and use relative value of EMI noise attenuation other than absolute value of EMC regulation to demonstrate the effectiveness of EMI noise suppression.

2.4 Mechanism of EMI noise source and its propagation path

2.4.1 EMI noise source

The high dv/dt voltage nodes and di/dt current loops are the well-known EMI noise sources of a switching cell[39]. The process of electrical energy conversion (switched-mode power supply, inverter, rectifier, etc.) is based on the principle of the switching cell and the switching cell is normally defined as a combination of one or more switching elements, typically semiconductor devices, and one or more electromagnetic energy storage elements, typically inductors and/or capacitors, that are operated to transfer electrical energy between two (or more) ports. The basic elements of the switching cell are combined with gate drives, sensors and associated control elements.

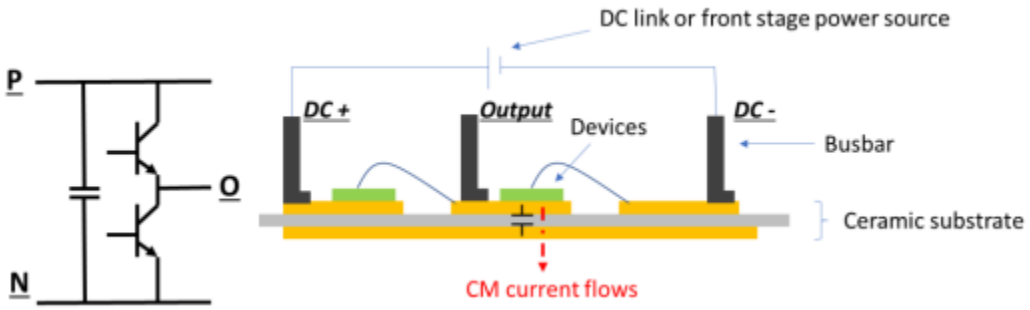


Figure 2-2 Switching cell

The connection of two switches in a “half-bridge”, which enables the management of energy between an input source of voltage and an output source of current, is shown in **Figure 2-2**. The switches are controlled by a periodic modulation function, with a binary value and a variable cycle ratio (duty ratio), regulating the transfer of electrical energy.

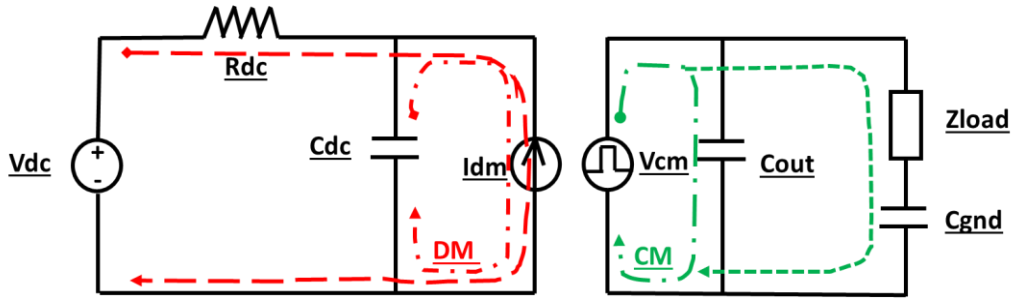


Figure 2-3 Equivalent circuit of a simplified switching cell

A switching cell and its noise source can be represented as a simple model shown in **Figure 2-3**[40]. The input current of the switching cell is presented as a current generator which creates the differential-mode (DM) current. The commutation current in the DC-link produces a voltage ripple in the DC-link capacitor. This produces mainly a DM noise current which spreads through the supply line into the power source side which can be a grid. Also fast changing circulated commutation current produces fast changing magnetic field which results in near field magnetic radiated noise.

The voltage of the switching cell is presented as a voltage generator which generates the common-mode (CM) current via capacitive couplings[41][42][43]. The voltage changes at the output node and charges and discharges all capacitances connected to the output. This produces mainly a CM noise which spreads via parasitic capacitances to power ground and back to the grid/source. Also, this pulsating voltage noise source causes differential noise current at the output side which propagates towards the load and circulates back to the noise source within the system. Such CM noise at output side could cause troubles to the load for instance damaging motor bearings and insulation. This

simple EMI model can be integrated with the other elements of the electric environment of the converter (network, control devices and connection to the earth) to determine and calculate the common and differential-mode currents at the input and output side.

In order to help to understand the basic features of an EMI noise source, the EMI effects of idealized pulse current and voltage waveform without finite slew rate are analysed first. The waveform of the current and voltage consist of pulses with different amplitudes and different durations. A simplified waveform is shown below in **Figure 2-4**.[44]

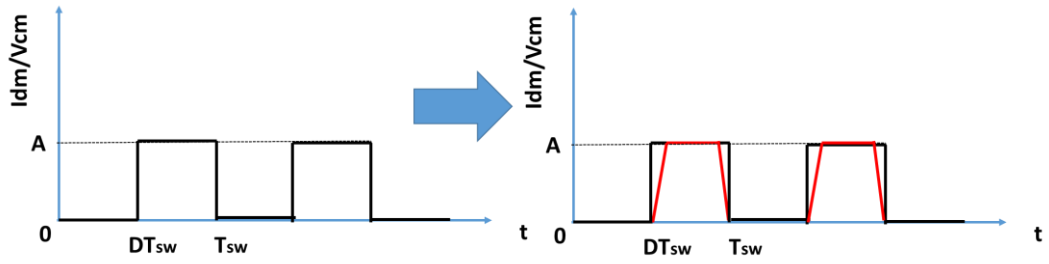


Figure 2-4 Simplified noise waveform with/without finite turn on and off times

The amplitude of the waveform is A, period is Tsw, and duty cycle is D. The frequency

$$x(t) = A * D + \sum C_n * \cos(n * \omega t + \varphi_n) \quad (1)$$

$$\varphi_n = \pm n\pi D \quad (2)$$

spectrum of the waveform can be represented in **Figure 2-5 [41]**

The envelope of noise source in the frequency domain includes two slopes: one is$0\ dB/dec$; the other is $-20\ dB/dec$. For practical cases, semiconductor devices cannot be turned on or off immediately. The trapezoidal waveform, shown in **Figure 2-4** is very close to the real current or voltage waveform. To simplify the analysis, it is assumed that the rising time T_r and falling time T_f are equal. The envelope of the frequency domain spectrum is the curves shown in the **Figure 2-5** below. **Figure 2-5** shows the comparison of noise spectrum envelope of a noise waveform of **Figure 2-4** at the frequency domain. The left noise spectrum envelope is without finite turn on/off time; and the right one is

with the finite turn on/off time. The first turning point at both spectrum envelope is inherent to the switching frequency ($f_{sw} = 1/\pi DT_{sw}$).

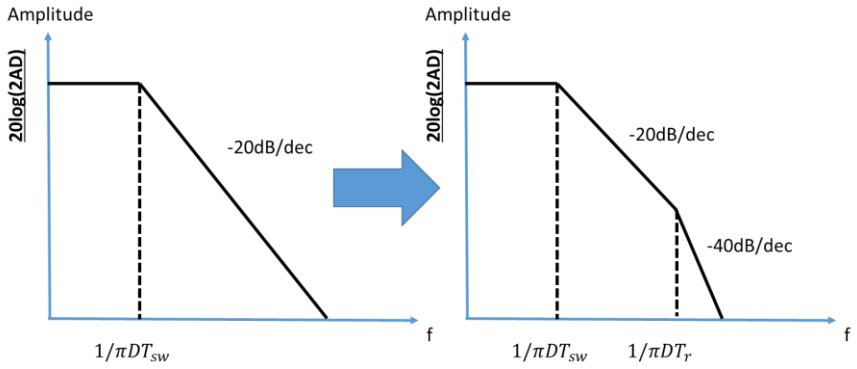


Figure 2-5 Noise spectrum envelope at freuqency domain of with/without finite turn on and off (turn on time is equal to turn off time) [41]

In contrast with the spectrum of a square waveform, the spectrum of a trapezoidal waveform has three traces: the first one is $0dB/dec$, the second is $-20dB/dec$ and the third one is $-40dB/dec$, which is caused by the finite rising and falling time. From the analysis above, it is seen that the maximum level of the noise envelope is related to waveform amplitude A. Much higher power rates results in higher noise level with a fixed duty ratio. The low switching frequency and longer rising and falling time lead to a lower corner frequency, hence much lower noise level at high frequency. Some passive techniques such as increasing gate resistor and snubber capacitors are used to slow down the slew of transit current and voltage[45][46]. Active gate control techniques use such feather to reshape the sharp edge and very steep slew rates of dv/dt or di/dt to reduce noise source. However, some of techniques will invariably increase switching losses and lose the advantage of using fast switching capable WBG devices. At higher powers and with very fast switching modulation, the noise envelope will shift to higher level and high frequency range.

2.4.2 Conducted EMI and its measurements Common-mode (CM) and Differential-mode (DM) noise characterization

The conducted EMI noise is usually decoupled and characterized as common-mode (CM) and differential-mode (DM) noise. CM noise is defined as the noise flowing between the power circuit and the ground, while DM noise is defined as the current following in the same path as the power delivery, as shown in **Figure 2-6**[47]. It is common to separate the CM and DM noise from the measured noise with a noise separator[48][49]. Many benefits are gained from this method, including simplicity of the filter design, each mode could be designed independently; and troubleshooting with the possibility to know directly which mode is not meeting the standard and therefore reducing the number of iterations required during the design stage.

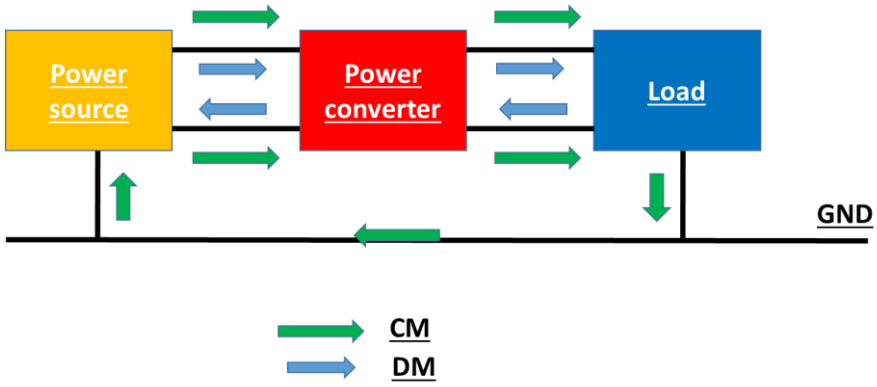


Figure 2-6 CM and DM noise propagation path

For measuring the conducted EMI noise, two Line Impedance Stabilization Networks (LISNs) are inserted between power source and equipment under test (EUT). The equivalent circuit for a LISN (one phase) is shown in **Figure 2-7**. The LISNs are used to stabilize the impedance of the input line and thus make sure that the measuring results are only related the EUT without any influence from the impedance of different AC line.

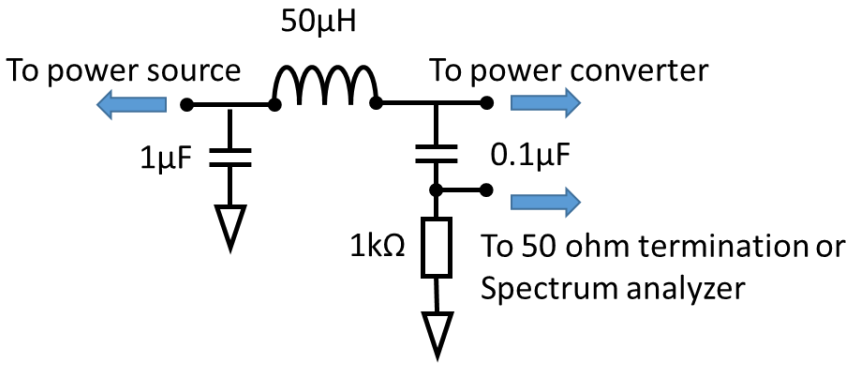


Figure 2-7 Equivalent circuit of the one-phase LISN

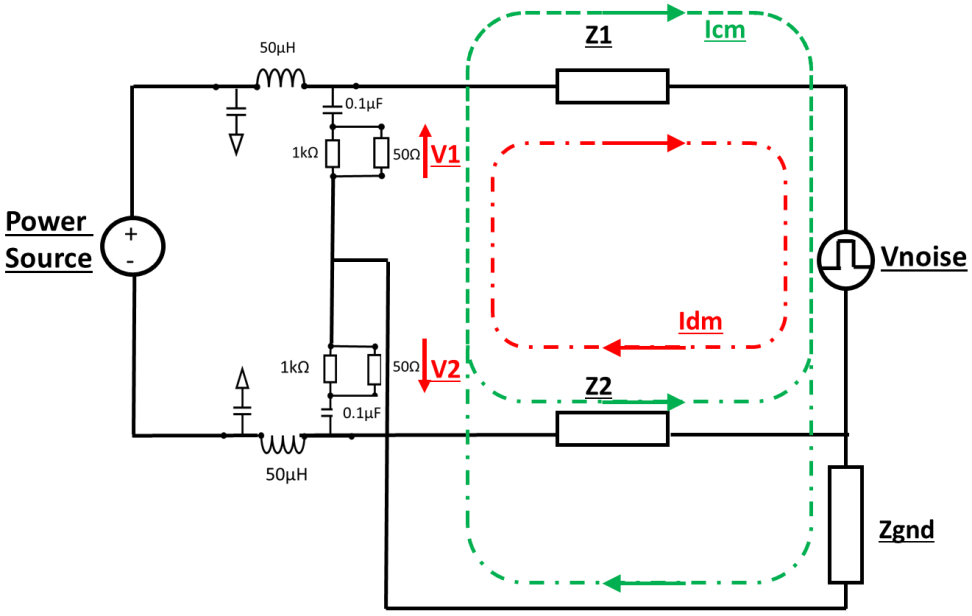


Figure 2-8 DM and CM nosie path with two-phase LISN

Since each LISN will either be connected to a 50Ω termination or the spectrum analyser whose input impedance is also 50Ω, the equivalent circuit for the measurement setup is shown in **Figure 2-8** which has two-phase LISN. The noise voltage developed across the LISN is given by

$$V_1 = 50 * (I_{cm} + I_{dm}) \quad (3)$$

$$V_2 = 50 * (I_{cm} - I_{dm}) \quad (4)$$

Thus the measured noise voltage across the LISN (V_1 andV_2) will have both CM and DM noise components. From the equation above, the CM and DM noise can be calculated by

$$V_{dm} = 50 * I_{dm} = \frac{V_1 - V_2}{2} \quad (5)$$

$$V_{cm} = 50 * I_{cm} = \frac{V_1 + V_2}{2} \quad (6)$$

Many papers have discussed and proposed noise separator using power combiner/splitter. The noise separator for measuring the DM noise is essentially a CM rejection network. A 180 degree power combiner can cancel two voltages with the same phase while combining two voltage out of phase. Since the voltage across one LISN resistor is $V_{cm} + V_{dm}$ and the other is $V_{cm} - V_{dm}$, theV_{cm} noise will be cancelled out, leaving V_{dm}. An alternative approach to measure DM and CM noise is using current probes as shown in **Figure 2-9**

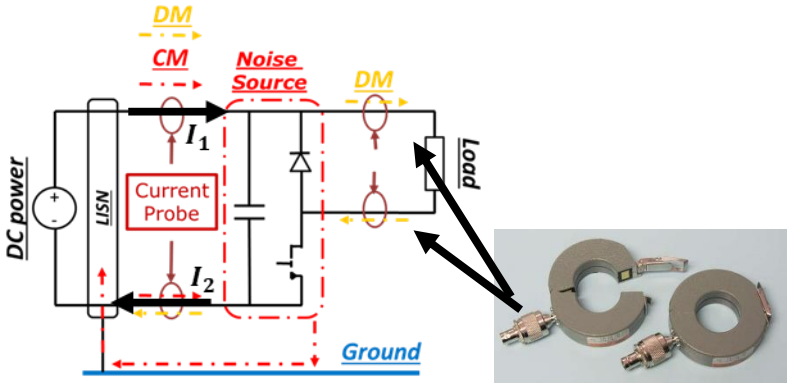


Figure 2-9 Conducted EMI measurement with current probe

The noise current in the wires I_1 , I_2can be given by

$$I_1 = I_{dm+}I_{cm} \quad (7)$$

$$I_2 = I_{dm} - I_{cm} \quad (8)$$

The measured positive and negative side currents can be used to calculate the CM and DM noise by

$$I_{dm} = \frac{I_1 - I_2}{2} \quad (9)$$

$$I_{cm} = \frac{I_1 + I_2}{2} \quad (10)$$

CM and DM voltage can be measured at 50 ohm terminated measurement receiver, a spectrum analyser for instance. The difference between using a current probe and the noise separator is minimum at the precious papers. Some small deviation between each method can be attributed to the approximation when reading the LISN impedance, or probe transfer impedance. For the sake of simple installation, in this research the current probe is used for EMI measurement.

2.4.3 Radiated EMI and its measurement

Radiated EMI from switching cells is usually treated as near field or close field radiation rather than far-field. In switching cell, noise current generates an extended electromagnetic field along the current path as the EM fields will propagate outside, as well as inside, the conductors. Changing current and voltage on the conductors results in high dv/dt and di/dt, and causes changing magnetic and electric fluxes that can generate unintended EM coupling via parasitic elements across relatively large distances. The magnetic radiated noise is due to the current commutation loop between DC-link and switching stage at the input side and between the load and switching stage at the output side. The oscillations generated in the loop between the inductive and capacitive parasitic components for instance at the DC-link capacitors and at the output stage can add further radiated noise.

The DM radiated noise is less severe and easily to be reduced by realizing a smaller commutation loop by twisting line cables together and shielding them. CM radiated noise includes both E-field mode originating from voltage changes at output node and H-field mode originating from coupled displacement current (changing electric flux) flowing through multiple low impedance ground paths. Through parasitic capacitive elements, coupled electric charges easily find relatively low impedance ground return paths, but these are often difficult-to-identify and may return back to the noise source through loops

with a large circulation loop area. All noise propagation paths become loop antennas, causing more radiated noise, and this case becomes worse when increasing power density where more parasitic couplings would be introduced to the system owing to the closer physical proximity of components. Reduction of CM radiated noise cannot be easily achieved because the CM circulation loop is often large and difficult to precisely identify. Moreover, it is difficult to separate H or E field noise behaviour at high frequencies (MHz), since mixed mode of both fields is dominant within switching cell. Every current flow (movement of charge) produces a varying magnetic field and this changing magnetic field induces electric fields: this continuous electromagnetic interaction and coupling increases the complexity of EMI generation within the switching cell. Common solutions include reducing loop CM current itself, coupling current back to the noise source through a much shorter route or by attenuating CM current, for example by inserting high impedance in the return path.

Near field probe or simple unshielded loop probes are used for measuring electric field and magnetic field separately from longwave to shortwave. H-field probes use a conductive loop to detect magnetic fields produced by switching power supplies. The probes produce a voltage proportional to the component of magnetic field that's perpendicular to the loop. The larger the loop, the more energy it will capture and the higher the voltage output. E-field probe is also called a pin probe. The E field probe is a voltage probe which makes contact to the target via 10pF capacitor, and it picks up the electric coupled noise. Unshielded loop probes can also be used to detect radiated emissions that are caused by both electric and magnetic field. They are sensitive to both types of field and their output is not as calculable or predictable, but they can save time when all that is needed is a quick check to see where an emission is coming from.

On the other hand, Full-compliance tests for radiated emissions use antennas designed for use in the far field, and EMC standards only give emissions limits in the far field. The far field is generally defined as greater than one-sixth of a wavelength, which for 30MHz is 1.7 metres. When measuring radiated emission between 30MHz and 1GHz a high performance ultra-wideband bi-logarithmic antenna is commonly used and the tests are performed in a large anechoic or semi-anechoic chamber where ambient RF noise is shielded. When performing an EMI test, the equipment under test (EUT) is placed in the anechoic chamber on a rotating carousel. The EUT is then powered up and the antenna moved 3m and 10m away which depends on what the standard calls for.

2.5 Review of EMI suppression at the noise source

Within a switching cell, switching devices are always denoted as the noise source. By switching at a certain voltage or current level through PWM techniques, these devices create a very high dv/dt and di/dt that have multiple harmonics in the EMI range. The noise source level is determined by the switched voltage/current level, device switching behaviour (switching speed and ringing after switching that is related with parasitic parameters of the devices) and modulation methods. The higher switching dv/dt and di/dt, the higher EMI emission.

2.5.1 Soft-switching and active gate controls

Soft-switching techniques are used to significantly reduce the switching dv/dt and di/dt. Less EMI noise is generated by improving the current and voltage waveforms associated with the switching of the power devices. Snubbers, gate-drive modification, and soft-switching techniques are common solutions for EMI suppression at the noise source strategy[50][51][52]. Snubbers are placed across switching power devices to soften the switch transitions and to damp the high frequency waveform oscillations during switching with small resistor. Another simple way to slow down the switching transitions would be

by increasing the gate resistance[53][33]. However, one downside of using snubbers and large gate resistor to reduce EMI is a slight increase in overall power loss. Alternative way to reduce EMI generation is to slow down the switching transitions by active gate control which modify the turn on and turn off trace and reduce voltage and current spikes. As mentioned in the research[54], instead of square and trapezoidal waveform with sharp corners and linear edges, the switching wave can be reshaped to more smoothed traces such as a "S" shape or "4^{th} derivative control". With this improvement, high frequency components in the waveform would be reduced, resulting in reduced current overshoot, ringings and EMI noise level. More smoothed switching waveform and longer switching time can lead to reduce further overshoots, oscillation and losses. This type of approach is effective to reduce high frequency EMI problems due to ringing effect at power device level, and to reduce resonance within current commutation loop. The level of EMI noise originated from the sharp transit of voltage and current at turn on and off has not been suppressed significantly, which is the main source for EMI noise production[55][56][57]. In addition, active gate drive are used to slow down the fast voltage and current transit, which contradict with the original purpose of using WBG devices to realize fast switching speed. On the top of that using auxiliary circuit of active gate drive will add complexity to the switching cell and introduce more EM coupling between electronic components and using active gate drive may also increase switching losses where dv/dt and/or di/dt are deliberately limited.

2.5.2 Improved switching cell layout

High dv/dt and di/dt are the noise source and inductive and capacitive parasitic elements within switching cell are the enabler for EMI propagation of both conducted and radiated noise. Furthermore, resonance between these parasitic elements and switching stage will inevitably add more EMI noise to the whole system. Reducing EMI noise at the switching cell and containing EMI noise from propagating or coupling to the

surrounding environment are also important from the perspective of system level EMI strategy.

In order to achieve small current commutation loop and lower parasitic inductance within a switching cell, recently, advanced planar interconnection techniques have been investigated, replacing bond wires interconnection, including deposit metallization, soldered copper plate, soldered copper lead, and silver sintered flex circuit[58][59][60]. These techniques successfully reduce parasitic inductance from several tens of nH to sub nH and improve electrical interconnection and thermal management configuration as well. Apart from physical reduction on loop length, some groups have focused on strip-line design on conventional planar power module[61][62][63], shown in **Figure 2-10** and **Figure 2-11**.

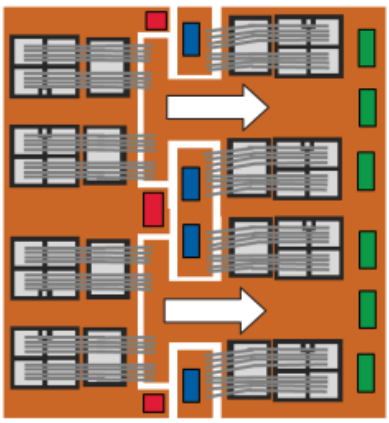


Figure 2-10 Half bridge layout with strip line layout (DC+/DC- terminals) [60]

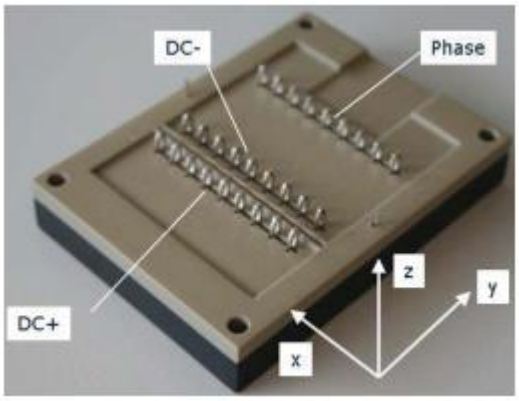


Figure 2-11 Strip line layout press fit pins for power module [60]

They can achieve similar parasitic reduction to several nH level by close placement of positive and negative terminals or arranging switching device and diode in a pattern that has very small current commutation loop[64]. Positive and negative terminals are arranged closely to each other in order to compensate for the magnetic field generated by the current flow in individual terminals. Normally the pin rows for positive and negative are situated in the middle of the substrate and the distance between each other is minimized by a laminated structure. The direction of substrate current, which flows under the emitter bond wires, is designed to be opposite to the direction of current flow in bonding wire. Consequently a smaller current commutation loop area produces a low-inductance packaging arrangement. This pattern is repeated for all devices yielding a symmetric current distribution within the power module, ensuring better controllability.

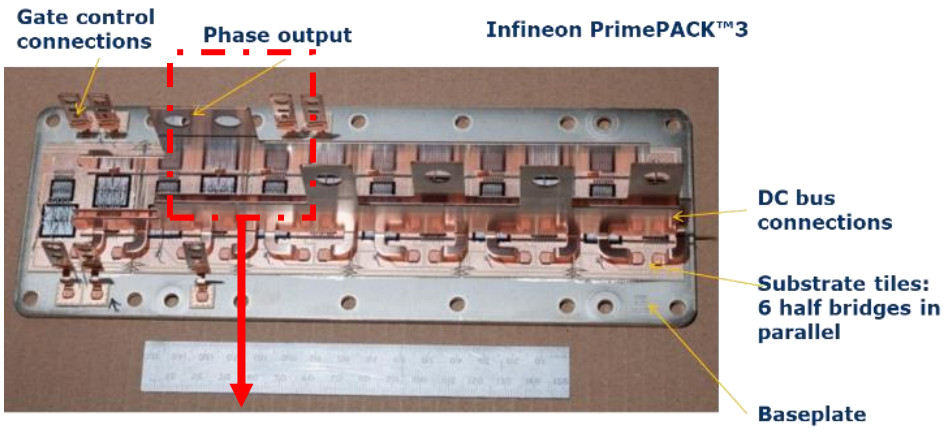


Figure 2-12 Infineon PrimePACK™3

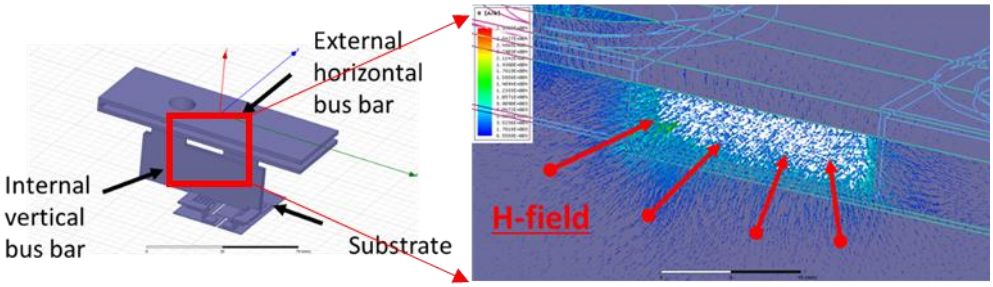


Figure 2-13 EM simulation model in Maxwell 3D (Left), H-field plot between bus bars (Right)

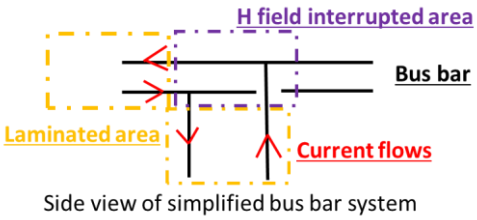


Figure 2-14 Simplified diagram of stripe line bus bar

However, these strip lines have breaks at interfaces inside modules, at terminals of modules, within the bus bars and at capacitor terminals. These breaks at physical interconnections fails to create a compact path for the magnetic flux, resulting in magnetic field leakage and additional parasitic inductance. Infineon PrimPACK power module as an example shown in **Figure 2-12**, and electromagnetic field distribution was studied with EM simulation tool Maxwell 3D. One half-bridge substrate and its internal and external bus bar connection was built in the software shown in **Figure 2-13**. On the top of vertical bus bar, there is break at between paralleled bus and H-field leakage is shown in the simulation result in **Figure 2-13** (right). On the top of that, screw structure on the horizontal bus and changing current flow direction from vertical to horizontal directly interrupt H field confinement, shown in **Figure 2-14**. Hence, a consequent strip line design without breaks, and wide; short conductors and the principal current vector kept within one plane for each segment, results in minimum inductance. In order to eliminate the breaks caused by screw connection, further search on external bus bar connection have been carried out, aiming to replace screw structure. A phase leg configuration can be implemented with the aid of a specially designed blade connectors[65][66][67][68]. All these techniques contribute to less parasitic inductance at current commutation loop, less voltage overshoot at turn off, less radiated noise on EMI property at input and output. Compact and balanced circuit layout is good to eliminate undesirable behaviour such as unbalanced current distribution and conversion between DM and CM noise current

Another problem is varying voltage potential at the output node driving CM noise currents through the stray capacitance of the output to the ground[69][70][71]. In order to reduce electric field coupling from output node to the ground, some researchers proposed flip-chip techniques where the high side chip is placed on the DC+ trace with source and gate contacts on the top, whereas the low side switch devices are turned upside down and DC- land needs a patterning for the gate control[72][55] in **Figure 2-15**. Or in an alternative way, some group have proposed stacked sandwich structure, where high side is positioned at the bottom and low side is on the top and output trace is the middle[73][74] in **Figure 2-16**.

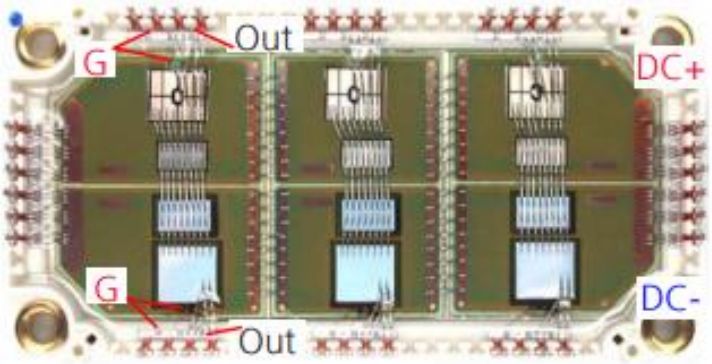


Figure 2-15 Flip-chip version power module from Fraunhofer (Top) [52]

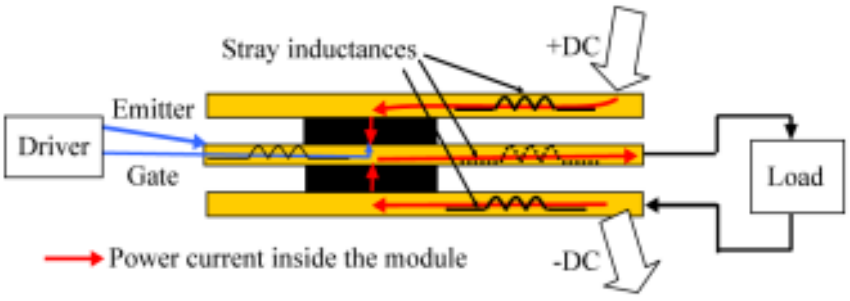


Figure 2-16 Three-Dimensional Power-Chip-on-Chip integration (Bottom) [70]

All switch devices are laminated between each conductive layer. These design increase electric field couple between DC- and DC+ and output node while reducing electric field

coupling with respect to the heatsink which is connected to the ground – therefore there is less electrical coupling path available for CM current to circulate. More electrically coupled noise current can be turned back to the noise source through DC-/DC+ rather flow into the ground. This phenomenon can be easily understand through a simplified model for the switching node to ground capacitance: $C = \frac{S*\varepsilon}{d}$ where reduced chip interconnection area (s) and increased distance (d) to ground result in reduction of unintended parasitic capacitive coupling. However, it also raise the question about an increase of thermal impedance and thermal-mechanical reliability to the power module. Also capacitive parasitics cannot be eliminated completely and there is fringing effecting and coupling to the ground. In contrast to capacitive parasitics reduction technique, [75]some other group focus on taking "advantage" from large capacitive effects and consider the capacitive coupling as an integrated capacitive filter to mitigate the CM emission directly within the switching cell, which contributes to direct "recycling" of the common mode current. However, recycling capacitive elements are small, and cannot provide enough low impedance for CM noise current as a return path at low frequency since the parasitic impedance at the CM current recycling path is relatively high compared to the ground path, and this technique has small improvement on CM reduction at high frequency due to skin effect on conductive ground layer and increased parasitic impedance. This type of "if you cannot beat them, join them" ideology[75][76][77] is not to solve the problem but to adapt to the problem, even sacrificing overall system performance. Although capacitive coupling can be reduced through the techniques above at power module and switching cell level, when the switching cell is connected to the external bus bar, changing electric field can still couple to low impedance paths such as ground, causing significant CM noise current. In other words, these methods just move the problematic dV/dt node from the output trace of power module to the external

connection such as bus bar, hence they change the route of electric field coupling, but do not break this field coupling and prevent it from propagating outside the switching cell.

2.5.3 Summary of EMI suppression at noise source

To summarise all techniques mentioned above, planar design for compact power module and strip line layout for small current commutation loop area can achieve sub-nH levels of low parasitic inductance between dc-link and switching stage. Also laminated bus bar design significantly reduces parasitic inductance. Flip-chip power module and laminated bus bar design can reduce parasitic electric field coupling between output node and the ground. However, current commutation loop cannot be reduced infinitely and capacitive coupling cannot be eliminated completely. On the other hand, ultra-compact power design can bring us new problems such as low thermal performance and thermal-mechanical reliability problem.

2.6 Review of EMI suppression along the noise propagation path

2.6.1 Filtering techniques

As suppression strategies along noise coupling path, passive filters are the most widely used because of the relative low cost and high effectiveness. Their general function are blocking the noise current propagating to the load by providing high impedance in the direction to the load and/or by providing high frequency paths with low impedance around the switching cell which is responsible for the generation of the noise sources. Thus the noise currents are circulated back internally. [23][78] The passive filter is typically a combination of inductors and capacitors and its design is based on the required level of attenuation which is the differential amplitude between the noise magnitude and the standard to be complied with. Previous research has developed many filter design procedures to determine the filter topology and component values[1][79][80][81]. The

effectiveness of passive filter basically relies on impedance mismatching networks and thus require an accurate estimation of the impedances that are expected to be seen at the input and output side of filter. Not only filter impedance but also source, line and load impedance are on the CM noise propagation path[82][83]. It is critical to model each element precisely and determine the impedance valleys at correct frequency for high noise attenuation. Over the past few decades, several modelling methodologies[84][85] have been published for extracting EMI models of power converters. They can be classified into two broad categories: detailed lumped-circuit and behavioural modelling[86][87][88]. Also some methods target on characterizing the filter itself have been investigated.[89][90][91].

However, the filter design method shown above only gives the optimised value for inductance and capacitance in the filter. To get the real value and size of filter, the physical implementation of each component needs to be considered. The main issue is the parasitic parameters of filter. Component parasitic parameters are also very important for filter high frequency performance[92][93]. Due to the parasitic parameters, the filter transfer gain slope cannot be made constant for the entire frequency range[94][95]. Many researcher have presented methods to either estimate the parasitic parameters of inductors and capacitors or to cancel them using circuit theories[96][97][98]. A technique has been introduced to improve the high frequency performance by cancelling out the effects of the parasitic capacitances of the filter inductors. Some group has shown that arranging capacitors in a lattice network with additional resistors and inductors[99][100], whose values are same as the equivalent series resistance (ESR) and equivalent series inductance (ESL) of the capacitors, would give an equivalent T-filter behaving as a capacitor without parasitic ESL and ESR, and thus, result in superior filter performance. Therefore, parasitic component must be designed and controlled during the implementation of filter to ensure adequate high frequency performance.

2.6.2 EMI filter

To reduce the EMI noise and meet EMI standard requirements of power electronic system, EMI filers are used to attenuate DM and CM noise at power converter system, in most cases applied at input side, between power source and power converter[79]. For many applications, the load is a standard equipment such as a motor, a resistor or an inductor which has a high noise immunity. For this type of application, EMI standard is enforced only at the noise source input side to make sure the converter would not influence the working condition of the power source[101]. Thus EMI filter helps preventing from polluting the main power line and interacting with other electronic system. One or two stages of EMI filters are usually used for DM and CM noise attenuation in the power electronics area[93]. The basic principle of filtering is to bypass noise using shunt capacitors and block noise using series inductors. The commonly used EMI filter topologies include LC pass filters to attenuate HF noise, and sometimes, band reject filters to attenuate a certain frequency, which is usually the switching frequency and its harmonics[102].

As an example, a DM filter used to attenuate DM noise shown in **Figure 2-17**. The right DM capacitor C_{dm} bypasses most of the DM current because of the high impedance of Ldm. The left DM capacitor C_{dm} bypasses most of the remained DM current because of high impedance of LISNs.

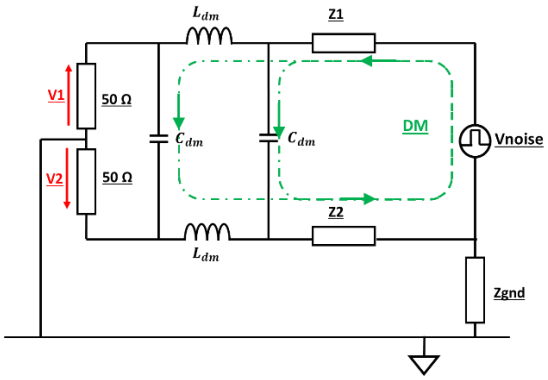


Figure 2-17 DM filter topology

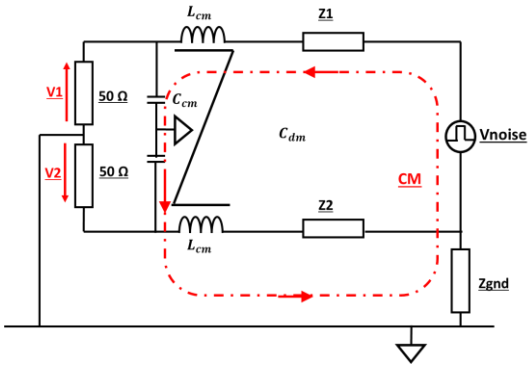


Figure 2-18 CM filter topology

A CM filter used to attenuate CM noise is shown in **Figure 2-18**. Cm capacitors have same capacitance and thus the same impedance to CM noise. The CM inductance L_{cm} is the same on two lines and at the same time, two inductors are closely coupled. Because of this, the CM currents in two lines are evenly bypassed by the two CM capacitors. CM and DM filter are usually built together in power electronics using a single inductive element. The leakage inductance of the inductor is the DM inductance of DM filter. The coupled inductance of the inductor is the CM inductance of CM filter[103].

2.6.3 Output filter

High dv/dt at output side causes malfunction [104][105]at load side for instance the stress on the motor, winding failures and bearing currents[106][107]. Research[108] has revealed the severe effect of the interaction between the converter and the load with

very high dv/dt transient. With an order of of magnitude higher switching speed of SiC converter, these phenomenon would be worse. Also when long cables are connected between the converter and the load, larger current spike would occur that the case without cables, due to the cable capacitance. Moreover, for many applications, when the connection cable between power converter and load is long, the cable behaves like an antenna and the conducted noise also generates radiated noise[109][110]. Thus output low-pass filter may be needed for high dv/dt reduction at the output terminals. Output filters suppress the noise in the first place before propagation to the load side. In the past few years, various output filter topologies have been developed to suppress the high DM or CM voltage at output. For instance, the simple output reactor reduces dv/dt of the inverter output, which in turn reduces the over voltage transient on the motor terminal[105], shown in **Figure 2-19**. Another method to suppress the over voltage is to use an RLC output filter. LC or RLC output filtering at the inverter terminal decrease the voltage transition rates below a critical value,[111][112][113] as shown in **Figure 2-20**.

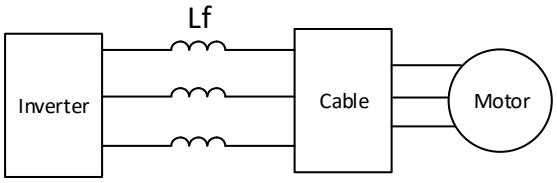


Figure 2-19 Output reactor at the power inverter terminal

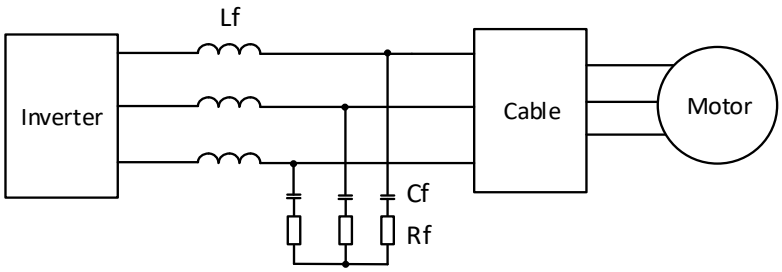


Figure 2-20 RLC output filter at the motor terminal

Using a resistance, inductance, capacitance (RLC) network, the magnitude of the voltage harmonics at any particular frequency depends on the cut-off frequency and amount of

damping achieved by the resistor. The design of this kind of filter is complicated by the fact that overvoltage can occur due to the filter resonance. For this reason, filters are often designed with a resonant frequency significantly below the switching frequency, and above the output fundamental frequency to avoid resonance with the load, as expressed in

$$f_{res} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{11}$$

$$f_f < f_{res} < f_{sw} \tag{12}$$

Here, f_{res}, f_{sw} and f_f, are the filter resonance frequency, switching frequency, and fundamental frequency of the drive's output voltage, respectively. However these topologies can only filter the line-to-line voltages, blocking and attenuating DM noise but have no impact on CM voltage at load side. CM noise current can flow into the ground either through parasitic capacitance between the output phase cable and the ground; or through the parasitic capacitance between load (for example, the neutral point of the motor windings) and the ground. In an improved output filter topology, a return path to the DC link from connecting the LC filter has been investigated,[114][115] shown in **Figure 2-21**. Connecting the neutral point of the CM filter to the DC bus can divert the CM noise current back to the dc bus and the noise source. This method is analogous to the previously mentioned CM filter which use the ground to block and return CM noise current back to the noise source. The solution of this topology has an important advantage over the classical output filter and it can reduce both CM and DM components, eliminating DM over-voltages, and suppressing CM noise.

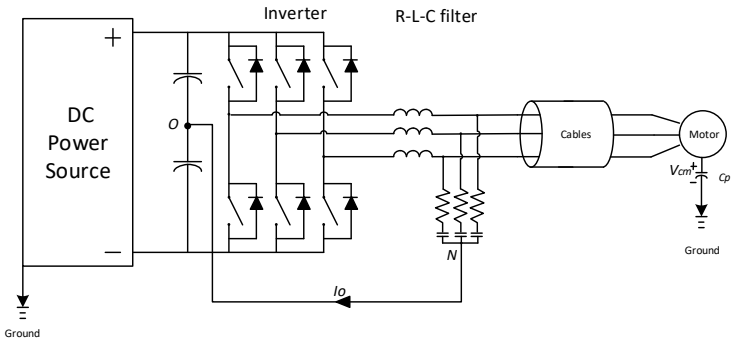


Figure 2-21 Output RLC filter with a return path to the DC link

Similar to the topology in which the neutral point of capacitor is connected to the middle point of DC link, in an alternative topology, the LC filter operates in differential mode, reducing the dv/dt, as shown in **Figure 2-22**[116][117]. The diode clamp operates whenever a voltage ringing overshoot occurs. During the ringing, the voltage has instantaneous values bigger than + or – $Vdc/2$ When the voltage in the star point of the capacitors from the LC filter becomes bigger than + or – $Vdc/2$, the corresponding diode starts conducing therefore clamping the overshoot voltage to the dc link. Other variation of similar topologies are introduced in [118][119][120][121][122][123].

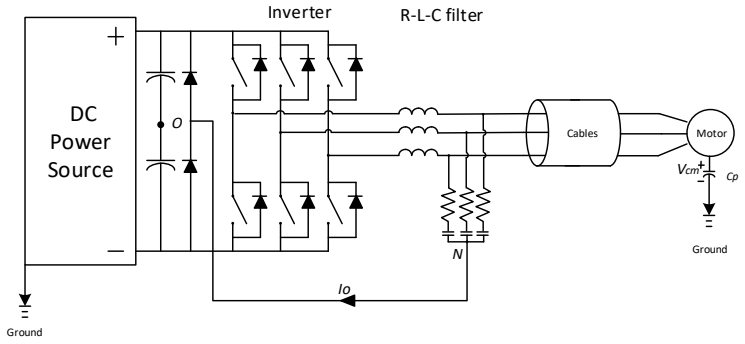


Figure 2-22 Output RLC fitler with a return path and diode clamp to the DC link

2.6.4 Summary of EMI suppression at noise propagation path

To summarize solutions of noise suppression at propagation path, at low frequency up to tens of MHz, switching noise and EMI noise can be effectively attenuated with proper system level modelling, following impedance mismatch philosophy and application of selected filter topologies. However, at frequency above 10 MHz, some stray inductance and capacitance within filters and power converter will dominate and limit the effectiveness of filters. Both discrete and integrated filter performance become significantly worse after 50MHz[124][100]. A filter featuring both high attenuation and broad stop band is necessary for dealing with WBG based power converter, where careful electromagnetic field design for filter arrangement is preferred. On the other hand, CM noise current is normally assumed to flow in the ground path and indeed this is how CM current is measured and how EMC performance is validated. A conventional solution can be achieved by CM filter including choke inductor and Y capacitor to block and shunt CM noise. However, the justification of grounding and the grounding position of the filter for CM return path has been a common sense that directing undesired CM noise to the ground would help with CM noise suppression. Many works have reported the improvement on ground connection to achieve lower parasitic impedance at ground path. With better connection and position, more CM noise can be shunted into the ground. However, this type of solution contradicts the principle of controlling and containing EMI noise, since CM noise flows into the difficult-to-identify ground path and returns back to the noise source in an inherently unpredictable way. Again, at high frequency parasitic inductance within CM capacitor (Y capacitor) or the ground connection will be present to hinder the high frequency CM noise being shunted. The remainder of the electrically coupled CM noise current flows in the main ground, resulting in additional conducted EMI. Moreover, some works have investigated the interaction between input and output CM filter and revealed that adding CM filter could alter and even worsen the other side of CM EMI performance. This result well illustrates that adding more diverting ground path for

CM attenuation cannot improve overall EMI performance but encourage more coupled noise current to flow into the ground, getting worse EMI performance. The most effective way to mitigate this issue is to provide a definite local return path, essentially breaking the loop of coupling to the ground for the electrically coupled displacement currents.

Taken together, the interventions described above together with their limitations leads to a significant conclusion, namely that in order to provide an effective means for EMI containment: 1) low-pass filters should be employed at both input and output side to attenuate and return noise as close as possible to the noise source, 2) stray electromagnetic fields should be contained so that they cannot propagate outside the switching cell enclosure. In this way, the electromagnetically coupled currents produced by rapidly changing voltages and currents in the main switching circuit are circulated back to the local DC-link rather than being coupled to ground. In addition, magnetic field coupling can also be attenuated by this containment by using a conductive enclosure of sufficient thickness (i.e. greater than the skin-depth at the lowest interference frequency).

2.7 Summary

In this chapter, the mechanisms of conducted and radiated EMI noise generation and the propagation path of common mode and differential mode conducted EMI noise have been introduced. The high dv/dt output voltage node and high di/dt current commutation loop are the primary EMI noise sources. Parasitic inductive elements at current commutation loop and parasitic capacitive elements between pulsating voltage node and the ground are the enabler to spread conducted and radiated EMI noise. To suppress the EMI noise at the noise source, a compact switching cell layout, featuring smaller parasitic inductance and small current commutation loop has been proved to have benefits but only on DM noise that originates from current and voltage oscillation and ripples resulting from switching. Indeed, low inductance power module design encourage much faster switching speed with WBG devices, resulting in higher dv/dt slopes and increased noise levels in the high frequency (>10 MHz) range.

Flip-chip and laminated (stacked-chip) module designs have some effect on reducing electric field coupling from the output node to the ground and suppressing CM noise from leaking to ground. However, this cannot completely eliminate stray electrical field coupling from the output to ground due to field fringing effects. In addition, unfiltered output and dc-link terminals provide another source of CM noise coupling to ground. Also this flip-chip and laminated module has no impact on DM suppression without low-pass filters. Furthermore, high dv/dt at output side may cause unnecessary over voltage and damage the load, for example by degrading insulation. Thus, optimisation of the switching cell itself has little impact on EMI performance, being limited to reductions in parasitic inductance and capacitance. Additional interventions are required to successfully attenuate noise at the noise source and prevent EM fields from leaking outside the switching cell

EMI filters and output filters are widely used for attenuating noise and blocking it from propagating to either the load or the source and with careful modelling and design, each filter topology can achieve good attenuation at low frequency. However, at higher frequencies, stray inductance and capacitance, together with mutual coupling between filter elements, dominate filtering performance. Both conventional discrete and integrated filters are typically not able to provide significant noise attenuation at frequencies above 50MHz which may limit their application in high-speed WBG enabled switching circuits.

Upon understanding conventional EMI noise suppression and its limitation, new approach for CM noise suppression is introduced in the chapter 3; new filter design feathered with high noise attenuation and wide stop band is introduced in the chapter 4. CM noise should be electrically isolated, returned through a low impedance path and attenuated to less pulsating waveform or a sinusoidal waveform within a conductive EM confinement before it reaches outside.

Chapter 3. Electromagnetic screening and shielding techniques

3.1 Introduction

Electromagnetic interference arises from the rapid voltage and current transitions occurring during operation of the switching cell. High dv/dt , where V_1 and V_2 represent voltages at the output terminals of inverters, causes massive Differential Mode (DM) noise to circulate between the inverter and load, leading to motor winding stresses due to capacitively coupled currents and voltage reflections. At the same time, rapidly changing voltages can cause massive Common Mode (CM) noise to circulate through the ground path back to the power module. This CM noise may introduce power losses and system malfunctions, such as deterioration of the motor winding insulation and high ground leakage currents from the motor windings. In addition, the power converter together with its associated connections to the power source and load can become a strong source of radiated EMI, which can then couple with nearby electrical systems.

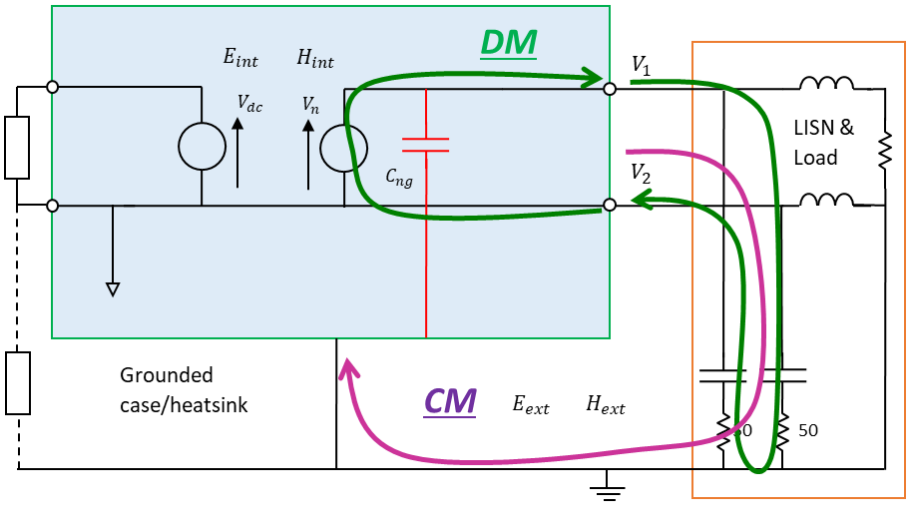


Figure 3-1 Simplified equivalent circuit EMI model for a switching cell without filters

A simplified model of the sources of EMI, the propagation path and a typical measurement arrangement for conducted EMI is showed in **Figure 3-1**. Noise sources within a switching cell are represented by voltage source V_n. The input voltage of the switching cell is represented as V_{dc}. Variations in Vdc occur as a result of the differential mode current produced by the switching action of the converter e.g. charging and discharging of the dc-link. This current produces a DM noise current which spreads through the supply line to the power source. On the other hand, the noise source $V_n$at output terminals which generate the common mode current via capacitive couplings. The voltage changes at the output node and charges and discharges all capacitance connected to the ground. This produces a CM noise which spreads via parasitic capacitances to the power ground and back to the power source. $C_{ng}$is the parasitic capacitance between the switching node and ground. Also this pulsating voltage noise source causes differential noise current at the output side which propagate towards the load and circulates back to the noise source within the system. The circulation paths for differential-mode and common-mode EMI are shown respectively by the green and magenta lines.

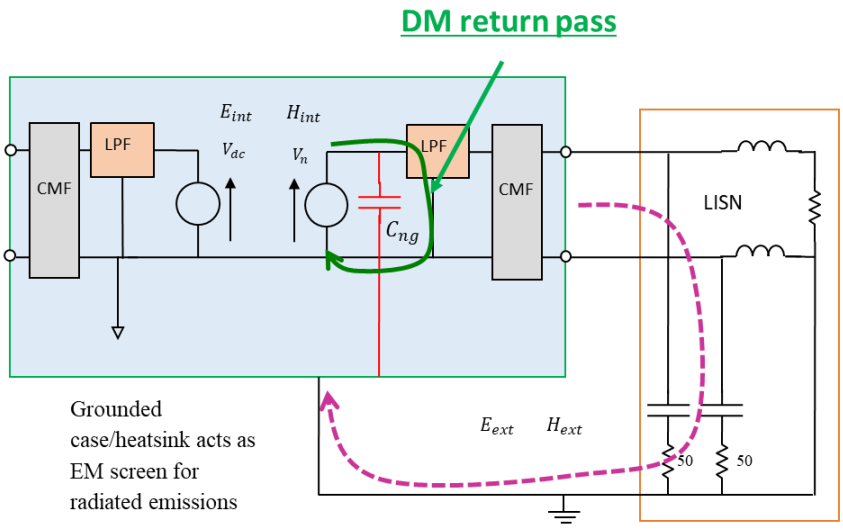


Figure 3-2 Simplified equivalent circuit of converter with EMI filters

So far, some researchers have tackled EMI problems inside power modules by reducing either parasitic inductance [68][74] on interconnections, or parasitic capacitance to "ground" through heatsink [72]. **Figure 3-2** expresses the conventional solution for EMI suppression, where a combination of common mode (CMF) and differential mode (LPF) filters are used at both input and output to attenuate conducted noise and shunt high frequency noise back to its noise source. In addition, conductive shield layer is applied outside the switching cell to attenuate radiated noise. However, this type of solution may not be able to contain and attenuate EMI noise locally within the switching cell: conducted and radiated noise may be coupled to the outside of power converter due to ineffective filtering layout and the ground connection for returning CM noise may exhibit a relatively high impedance.

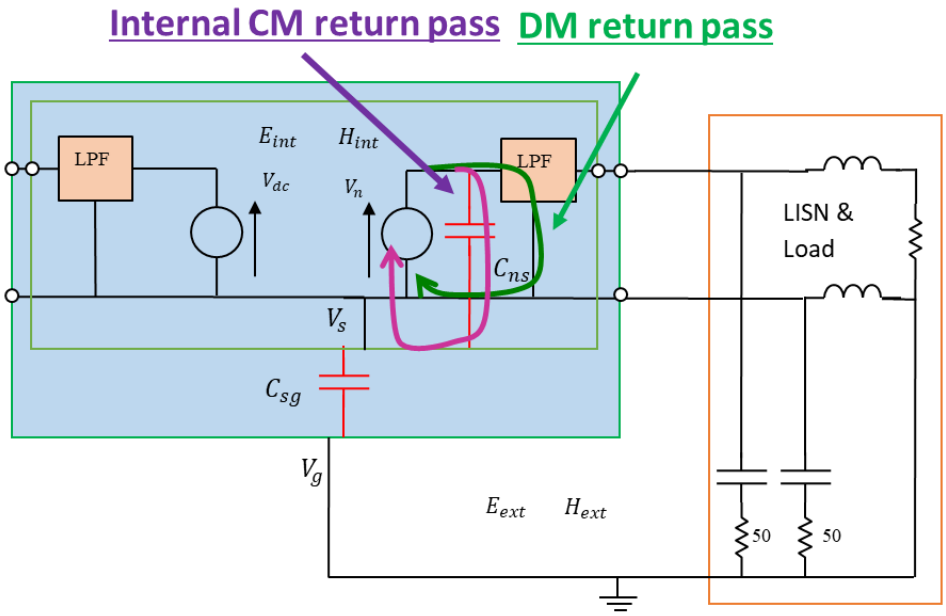


Figure 3-3 Simplified equivalent circuit of integrated swtiching cell with screening and shielding techniques

In contrast to the conventional approach of tackling EMI problems, we propose an alternative approach, utilizing a combination of screening and shielding techniques to solve EMI problems within the switching cell. The schematic of **Figure 3-3** illustrates the

function of screen structure in suppression of the common mode current that would otherwise circulate in the ground path, by recirculating CM current through internal screen/shield layer, shown by magenta line. (**Figure 3-5** shows a 3D model of CM screen layer beneath the noise source and return coupled CM noise current back to the noise source. **Figure 5-34** shows the actual layout of Buck converter including a half bridge). The screen is shown as an inner green rectangular area and it is electrically connected to the switching cell DC-link decoupling capacitance, providing a low-impedance path for local recirculation of common mode currents which are coupled electromagnetically into the screen, for example through the dielectric layers of the substrate. This arrangement successfully avoids returning CM noise through a common capacitor ("Y" capacitor) and avoids using ground as the return path. This is important because once CM noise flows into what is often a difficult-to-identify ground path, it cannot easily be controlled and confined within a specific arrangement and the level of attenuation attainable by such CM filtering techniques can therefore be difficult to predict.

On the top of that differential mode noise can be suppressed by incorporating a low-pass filter, which is integrated within the switching cell. In this case, the screen can provide a convenient means for returning the high-frequency noise to the source as a part of low pass filter configuration. The screen will also attenuate radiated electromagnetic fields, as long as it is significantly thicker than the electromagnetic skin-depth at the converter switching frequency.

This chapter will introduce the modelling and behaviour of shielding and screening layers, while the next chapter will focus on the achievement of high attenuation, across a wide bandwidth, for differential mode noise at the electrical ports.

3.2 Electromagnetic screening

3.1.1 Theories of screening CM current

When applying an internal screen as illustrated in **Figure 3-3,** effective suppression of common mode currents will be achieved by: ①ensuring the impedance of the internal loop connecting the screen to the switching cell DC link decoupling capacitance is much lower than that of the external ground loop; ②providing a layout which features maximum capacitive coupling between the noise source and the screen layer and minimum capacitive coupling between the noise source and the external ground. From this specific screening arrangement, electrically coupled noise current originated from pulsating voltage at the output node would be encouraged to flow on the inside of the screen and be return to the noise source, rather than flow into the ground. The screen layer may form a complete enclosure around the switching cell or may be a partial screen, for instance a conducting plane layer embedded in a substrate. In order to better illustrate the relationship between internal return path and external ground path on effective suppression of common mode currents, an approximate, small-signal, ac-equivalent circuit for the switching cell is proposed and shown in **Figure 3-4.**

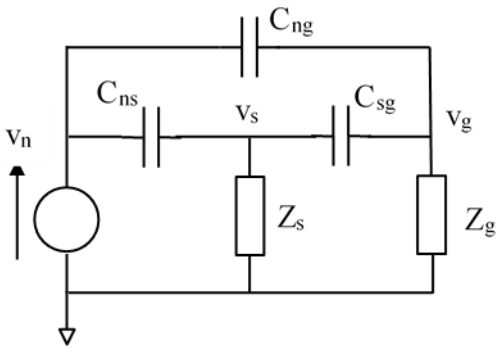


Figure 3-4 Approximate equivalent circuit for common mode current analysis

V_n is the switching noise source, V_s is the screen voltage andV_g is the ground voltage. The Voltage definitions for the screen layer and ground are not intended to correspond to any particular geometrical arrangement and are included solely to aid the analysis. Voltages and impedance for this arrangement will in general be distributed with variations expected across the bus connection, screen layer and ground planes. C_{ns} represents the capacitance from noise source to screen layer, C_{sg} represents the capacitance from screen to ground and C_{ng} represents the capacitance from noise source to ground. Z_s (Y_s) is the screen layer return path impedance (admittance), Z_g $\left(Y_g\right)$ is the ground return path impedance (admittance).

Nodal analysis defines:

$$V_g\left(Y_{ng}+Y_{sg}+Y_g\right)=V_nY_{ng}+V_sY_{sg} \tag{13}$$

$$V_s\left(Y_{ns}+Y_{sg}+Y_s\right)=V_nY_{ns}+V_gY_{sg} \tag{14}$$

Eliminating V_s:

$$V_g\left(\left(Y_{ng}+Y_g\right)\left(Y_{ns}+Y_{sg}+Y_s\right)+Y_{sg}(Y_{ns}+Y_s)\right)= \tag{15}$$

$$V_n\left(Y_{ng}\left(Y_{ns}+Y_{sg}+Y_s\right)+Y_{ns}Y_{sg}\right)$$

From which the common mode current can be obtained:

$$I_g=V_nY_g\times\frac{Y_{ng}\left(Y_{ns}+Y_{sg}+Y_s\right)+Y_{ns}Y_{sg}}{\left(Y_{ng}+Y_g\right)\left(Y_{ns}+Y_{sg}+Y_s\right)+Y_{sg}(Y_{ns}+Y_s)} \tag{16}$$

Some specific cases:

Case ① No screen:

$$Y_{ns}=Y_{sg}=0 \tag{17}$$

$$I_g = V_n Y_g \times \frac{Y_{ng}}{Y_{ng} + Y_g} \tag{18}$$

This result indicates that Y_{ng} and Y_g dominate common mode current. Increasing ground impedance by inserting high impedance choke filters at the ground path, and/or increasing impedance Z_{ng} by reducing parasitic capacitance between noise source and ground would realize common mode current suppression as per conventional solutions.

Case ② applying Screen and no direct coupling from source to ground:

$$Y_{ng} = 0 \tag{19}$$

$$I_g = V_n Y_g \times \frac{Y_{ns} Y_{sg}}{Y_g(Y_{ns} + Y_{sg} + Y_s) + Y_{sg}(Y_{ns} + Y_s)} \tag{20}$$

In the case of $Y_s \gg Y_{ns}, Y_{sg}$,

$$I_g = V_n Y_g \times \frac{Y_{ns}}{Y_s\left(\frac{Y_g}{Y_{sg}} + 1\right)} \tag{21}$$

At high frequencies the common mode current is determined by the ratio of Y_{ns}/Y_s (assuming Y_g is small).

In the case of $Y_s \ll Y_{ns}, Y_{sg}$

$$I_g = V_n Y_g \times \frac{Y_{ns} Y_{sg}}{Y_g(Y_{ns} + Y_{sg}) + Y_{ns} Y_{sg}} \tag{22}$$

This case is similar to the unscreened case but with the series combination of capacitorsY_{ns}, Y_{sg}.

From the case ②, we can understand that in the case when the screen layer can completely decouple noise source from ground, common mode current is greatly determined by the impedance of return path. As illustrated by equation (21), with careful

design of return path and screen layer, the impedance at internal screen path can be kept to minimum and the common mode current can be significantly attenuated by being returned internally. However, if at high frequency the return path becomes high impedance due to parasitic inductance along the return path and skin effect, and the path of Y_{ns}; Y_{sg} becomes low impedance, the common mode current would couple to ground through the screen layer and parasitic capacitance between screen and ground (Y_{sg}) as described in equation (22).

Case ③ Both screen configuration and the direct coupling from noise source to ground exist, $Y_s \gg Y_{ns}, Y_{sg}$:

$$I_g = V_n Y_g \times \frac{Y_{ng}}{(Y_{ng} + Y_{sg} + Y_g)} \tag{23}$$

In this case the leakage of electric flux around the screen layer limits common current screening performance and Y_{ng} should therefore be kept to a minimum level. A complete screen layer enveloping the noise source will minimise Y_{ng} and decouple the noise source from the ground more effectively compared with partial screen layer beneath noise source.

Common mode noise either couples to the ground directly due to the leaked flux (fringing effect) or couples to the ground via two capacitive couplings $C_{ns}C_{sg}$ or is locally returned through screen layer, depending on proportional parasitic impedance at each path. In all cases Z_s (Y_s) is a critical element impacting screening effectiveness. A small Z_s ensures the electromagnetically coupled current can be recirculated back to the noise source, and minimizes the component of current flowing in the ground return path. Another critical element is the relationship between C_{ns} and C_{sg}. Different shape and arrangement of screen layer will result in different combination of these parasitic capacitance. A good design with larger C_{ns} and smaller C_{sg} will intentionally couple more common mode

noise onto the screen layer and encourage it to be recycled back to the noise source internally and locally.

3.1.2 Characterization of CM screening using Impedance Analyser

3.1.2.1 Simulations

In order to relate the common mode current screening concept to a practical case and to illustrate the behaviour of the screen layer, we use a simplified model within ANSYS MAXWELL Q3D electromagnetic field simulation tool, shown in **Figure 3-5** and **Figure 3-6**, which includes the major noise source, screen layer, ground and return point. This simple model can well represent most cases of switching cell such as a half bridge.

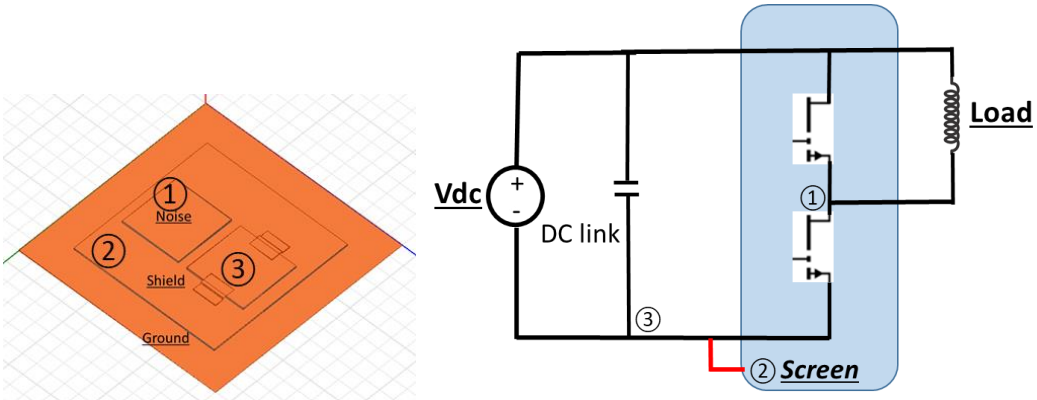


Figure 3-5 Model of CM returning system within ANSYS MAXWELL simulation (Left); relative position at simple half bridge circuit (Right)

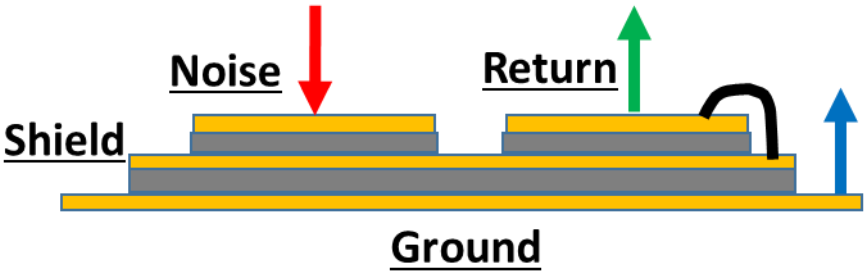


Figure 3-6 side view of CM returning system

In **Figure 3-5** number labels indicate relative position between CM screening model and a half bridge circuit. ① is the noise source in the CM model and the midpoint/ output of half bridge circuit. ② is the screen layer beneath the noise source and extend to the whole half bridge area. ③ is the noise return point and connected back to the DC link terminals. A copper sheet of size 20mm*20mm*0.1mm represents a noise source such as the output (switching node) trace inside the switching cell, constantly generating impulse voltage waves. A larger copper sheet of size 65mm*55mm*0.1mm represents the screen layer between circuitry and ground. In the end, a copper sheet of size 85mm*70mm*0.1mm represents the grounded baseplate/heatsink. A return point of the same size as the noise source which represents the position where coupled current is returned, for example either potential of the DC-link. In this model the return point is electrically connected to the screen layer by a set of bus bars whose properties are chosen to represent interconnections such as a wire.

Polyimide layers with thickness of 0.05mm are inserted between each of the copper layers to represent the required electrical isolation, shown in **Figure 3-6**. By creating an excitation point on the noise source and two sink points on the return point and on the ground layer respectively, a complete screening system can be realized by this model and CM current returning function of screen layer can be investigated through the following simulations and measurements.

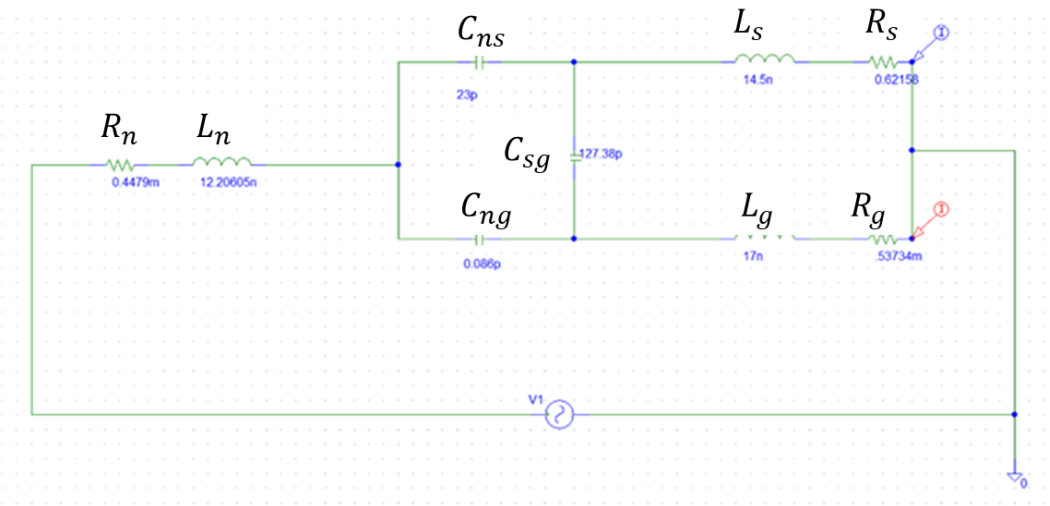


Figure 3-7 : Equivalent circuit of screen and return paths within Pspice simulation.

All parasitic capacitance, inductance and resistance of this model are extracted by ANSYS MAXWELL Q3D, and an equivalent circuit built within PSPICE simulation software, as shown in **Figure 3-7**. Vn is noise source; C_{ng} is capacitance between noise source and ground; C_{ns} is capacitance between noise source and screen layer; C_{sg} is capacitance between screen and ground; L_s and L_g are inductance of the current path on screen layer and ground layer. R_s and R_g are resistance of current path on screen layer and ground layer respectively. By measuring the currents flowing on the screen and ground layer represented by measurement point ① (blue) and ② (red) respectively, the impedance of both current paths can be obtained. The extracted parasitic parameters R, C and L are shown in the **Table 3-1** below.

C_{ns}	C_{sg}	C_{ng}	L_s	L_g	L_n	R_s	R_g	R_n
23pF	127.38pF	0.086pF	14.5nH	17nH	12.2nH	0.62mΩ	0.537mΩ	0.4479mΩ

Table 3-1 Extracted parameters from CM screening model

From the extracted data, the capacitive coupling between noise source and the ground is negligibly small, being only 0.086pF compared with the capacitive coupling between noise source and the screen layer which is 23pF. The screen layer would easily couple and

collect the electric field and return the noise current. Also large C_{sg} coupling is due to large overlapped area between screen layer and the ground, and this points out a concern that a bad design of return path would cause high parasitic impedance (L_s & R_s) at high frequencies and encourage noise current to couple to the ground through the screen layer. In this case screening function would be compromised and noise current would flow in the ground through screen layer as described in the case ② mentioned above.

Impedance comparison between current paths on both screen layer and ground are shown in **Figure 3-8**, with simulation frequency from 10 kHz to 100MHz. From the initial frequency to 10MHz, the impedance on screen layer is 100 times less (-40 dB) than that on ground, and after then two traces tend to converge together. From this result we can understand, capacitance C_{ng} and C_{ns} mainly affect the impedance and dominate the impedance ratio at low frequency. A larger Cns and smaller C_{ng} will increase difference of the impedance at screen layer and ground at low frequency and improve common mode current returning function hence increase noise current attenuation.

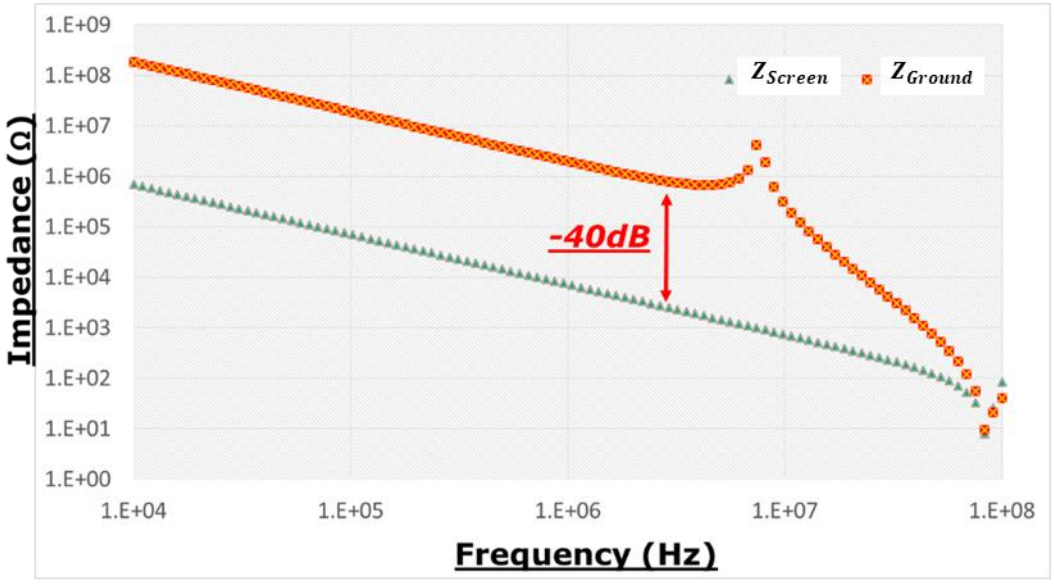


Figure 3-8 Impedance comparison between current paths of screen and ground.

The inductances Ls and Lg begin to dominate current balance between these two paths at higher frequencies, crosstalk (C_{sg}) between the two current paths becomes low impedance and starts to affect the current ratio. Eventually, impedance difference is proportional to the ratio of parasitic inductance L_s andL_g. This result agrees with the theory: Y_s and the ratio of coupled capacitance C_{ng} and C_{ns} dominate the current returning effect and CM screening effectiveness.

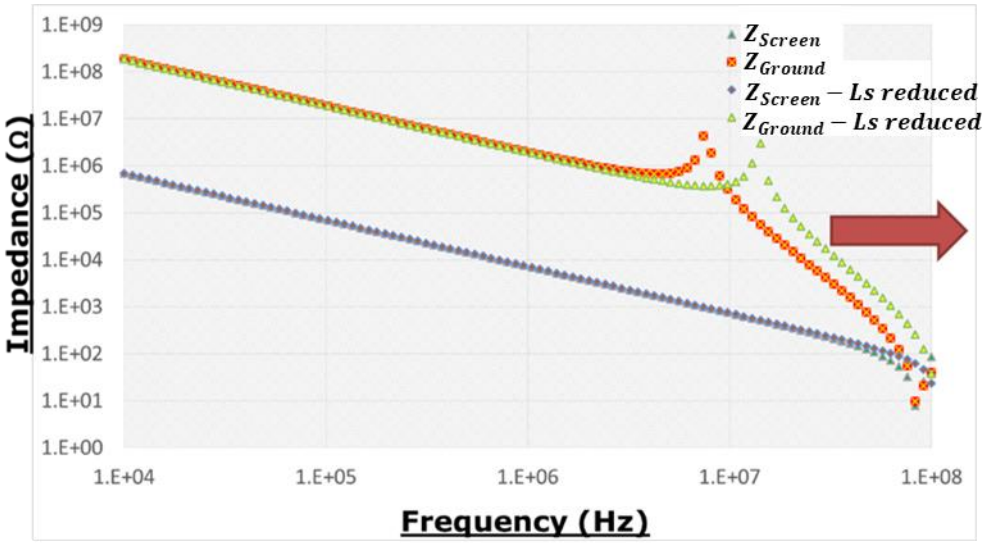


Figure 3-9 Impedance comparison between current paths of screen and ground when L_s is reduced

Figure 3-9 shows that a reduced value of L_s.(increased Y_s) would improve common mode noise screening results by pushing the resonant points to higher frequency and maintain difference of the impedance between $Z\ screen$ and $Z\ ground$, which means the impedance of internal current returning loop to DC-link is small compared with that of the external ground path.

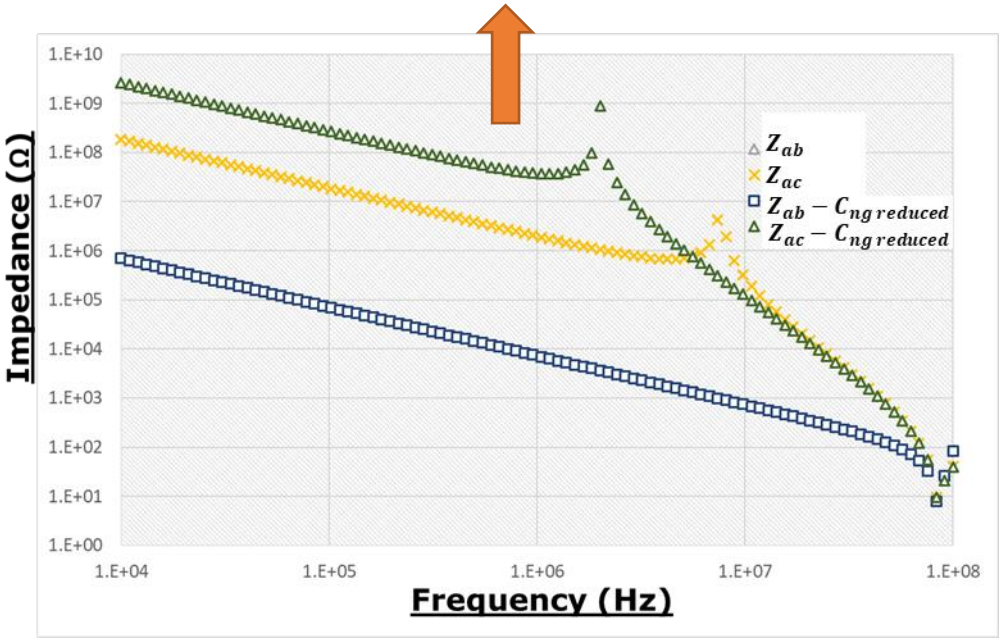


Figure 3-10 Impedance comparison between current paths of screen and ground when C_{ng} is reduced

Figure 3-10 indicates a larger C_{ns} and/or smaller C_{ng} will increase difference of the impedance at screen layer and ground at low frequency and greatly improve common mode current returning function hence increase noise current attenuation. This result can be achieved by applying extended or full screening arrangement rather than partial screen layer just beneath the noise source, which would increase electric field coupling from noise source to screen whilst decrease coupling from noise source to ground. Also simply increasing the distance between noise and ground by inserting a thick electrical isolation layer can achieve same level of decoupling function, however, it would increase thermal resistance and cause heat spreading problem for switching cell[125][126]. Oppositely, isolation layer between source and screen should be kept as thin as possible without causing partial discharge or breakdown[127][128]. In addition, at high frequency, impedance at screen return path and the ground converge together and align with previous discussion which is independent of capacitive coupling and dependent on parasitic inductance L_s and L_g. Low L_s at noise current return path can be realized by

thick and short bus bar connection or multiple direct vias through the isolation connecting the screen layer and return path.

3.1.2.2 Measurements

We used impedance analyzer KEYSIGHT E4990A with test fixture 16047E (DC to 120MHz) to measure impedance of internal and external current path Z_s and Z_g respectively, indicated in **Figure 3-11**, which shows the screen return current and ground return current. The fabricated sample and the connection points to the impedance analyser are also shown in **Figure 3-11** (Bottom). At the measurement, one port of the impedance analyser is connected to a plane in the module representing the typical location of the midpoint of a half-bridge circuit (the source of common mode noise), the other port of impedance analyser is then connected to the screen and baseplate (ground) layers in turn to measure the impedance from the noise source to both. When measuringZ_s, the noise source and noise return point are connected to the High and the Low ports of impedance analyser respectively and connect the ground to the Guarding port of impedance analyser simultaneously. The guarding function of impedance analyzer was used for the measurement, when one current path measurement is being performed $Z_s$or Z_g), the effects of paralleled impedance can be reduced[129].

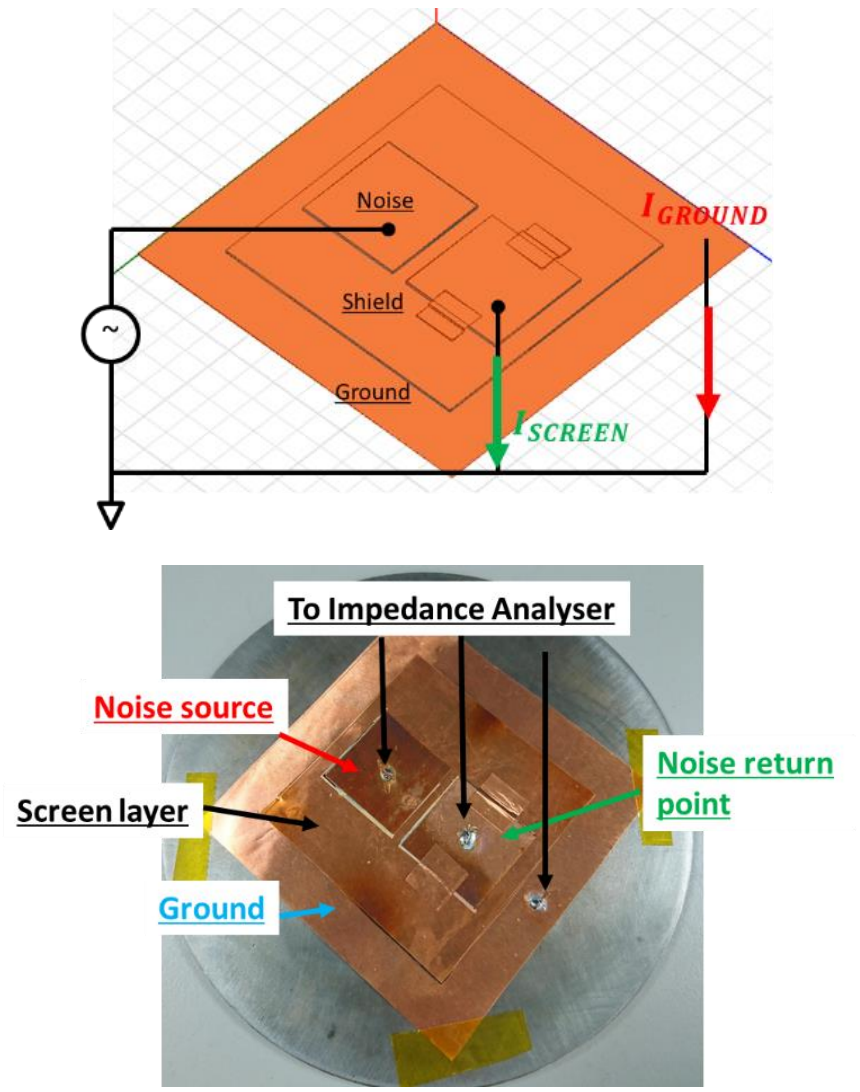


Figure 3-11 Schematic circuit of impedance measurement of Z_s and Z_g with a screen layer

The results from simulation and measurement align with each other very well, as shown in **Figure 3-12**. It demonstrates that the equivalent circuit can well represent CM screen layer and can be used to investigate impact on current returning path with different screen arrangements.

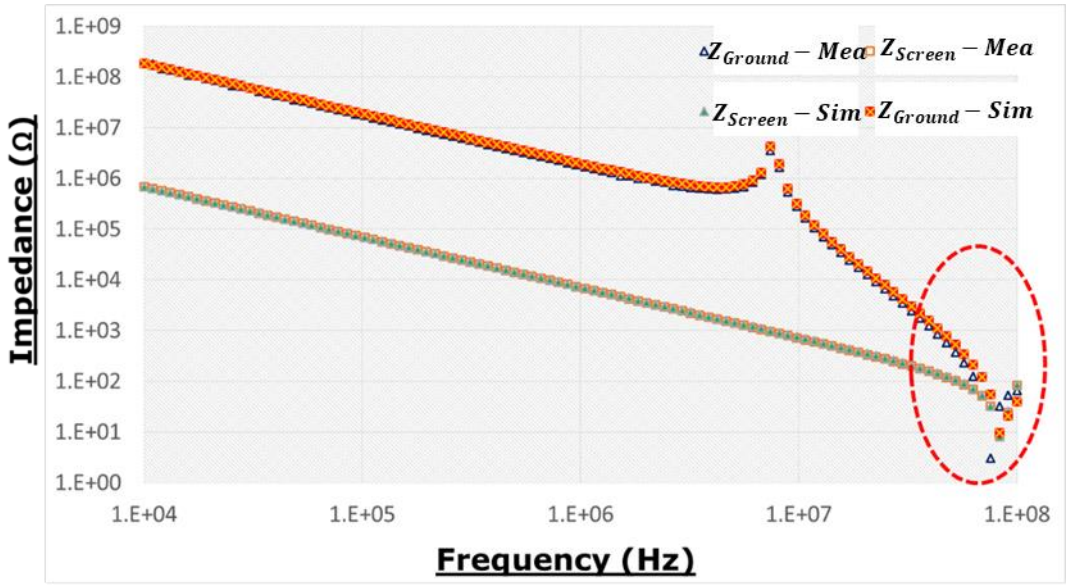


Figure 3-12 Impedance comparison between simulation and impedance analyzer measurement.

However at high frequency (above 50MHz) a small deviation is visible. That is because at high frequency, lumped equivalent circuit might lose accuracy. Instead, a distributed circuit with multiple elements might be desirable to obtain better accuracy on characterizing screen layer at very high frequency, see for example those based on RLC transmission line elements[130][131][132].

3.1.3 Characterization of CM screening using s-parameters and Vector Network Analyzer (VNA)

3.1.3.1 Characterization with Voltage insertion loss

In the previous section, we demonstrated the relationship between different layout and impedance at internal CM circulation path and external ground path by Pspice simulation and impedance analyser. On the top of that, In order to provide an intuitive impression about common mode current screening performance on noise reduction from the noise source to the ground, we also use network analyser to measure signal losses between noise source port 1 and ground port 2 to investigate how much excited noise can spread

to ground side. Common mode noise screening technique was also characterized by measuring the insertion loss using a VNA with 50Ω source (Z_S) and load (Z_L) impedances, which is included in VNA equipment. Scattering parameters (s-parameters) are chosen to characterize the screening arrangement. By measuring the s-parameters of a screen layer and different screen layer arrangements, the performance of the screening technique can be validated. The dominant elements within the screening layout are the parasitic capacitance and small parasitic inductance along the noise current path. Thus, it is reasonable to characterize a screen layer as a linear passive two port network under small signal excitation condition. The test setup for a screen layer is shown in **Figure 3-13**, where the CM screening layout is characterized in term of power waves, a_1, a_2, b_1, b_2.

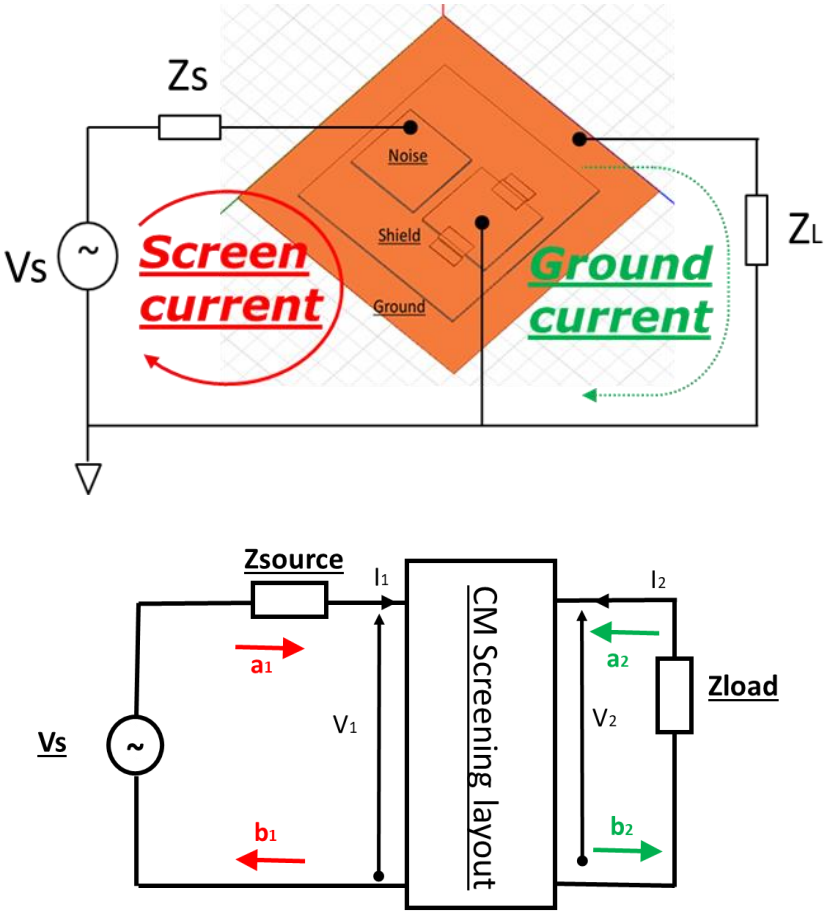


Figure 3-13 Schematic circuit of CM nosie attenuation with a screen layer

There are four waves in **Figure 3-13**, including wave $a_1$and its reflected wave b_1 at the port 1. The incident wave a_1 and its reflected wave b_1 at the port 2. From these four parameters, the voltage V_1 and current I_1 at the port 1; the voltage V_2 and current I_2 at the port 2 can be gained by the equations as follows:

$$V_1 = \sqrt{Z_0}(a_1 + b_1) \tag{24}$$

$$V_2 = \sqrt{Z_0}(a_2 + b_2) \tag{25}$$

$$I_1 = \frac{1}{\sqrt{Z_0}}(a_1 - b_1) \tag{26}$$

$$I_2 = \frac{1}{\sqrt{Z_0}}(a_2 - b_2) \tag{27}$$

Where Z_0 is the reference impedance and is usually 50Ω; V_s is voltage source; Z_s is source impedance which is usually 50Ω; Z_L is load; a_1& $a_2$are normalized incident wave on the source side and the load side; b_1& b_2 are normalized reflected wave on the source side and the load side; I_1&I_2 are input currents o the port 1 and port 2;V_1&$V_2$are voltages of the port 1 and port 2.

To fully characterize a two-port linear passive network, two linear equations are required from the four wave variables. The four s-parameters:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{28}$$

S_{11}, S_{22}, S_{12}, S_{21} are used to relate a_1, a_2, b_1 and b_2. S_{11} and S_{22} are reflection coefficients. S_{21} and S_{12} are transmission coefficients. According to the transmission line theory, when reflected wave b_1 or b_2 reaches the source or load side, it would also be reflected due to the mismatched impedance. The reflection coefficients Γ_s at the source and Γ_L at the load side can be gained:

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{29}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{30}$$

For CM screening, insertion voltage gain $A_v$is defined as the ratio of the port voltage at load side without the screen layer to that with the screen layer.

$$A_v = -20\log(\frac{V_{wo}screen}{V_w screen}) \tag{31}$$

This insertion voltage gain is further developed by the following equations:

$$A_v = \frac{V_2}{V_0} = \frac{V_2}{V_s}\left(1 + \frac{Z_s}{Z_L}\right) \tag{32}$$

$$= \frac{V_2}{(V_1 + I_1 Z_s)}(1 + \frac{Z_s}{Z_L}) \tag{33}$$

Substituting equations (24)-(27) into (33) generates

$$A_v = \frac{\frac{a_2}{b_s} + \frac{b_2}{b_s}}{\frac{a_1}{b_s}\left(1 + \frac{Z_s}{Z_0}\right) + \frac{b_1}{b_s}\left(1 - \frac{Z_s}{Z_0}\right)}(1 + \frac{Z_s}{Z_L}) \tag{34}$$

b_s is the normalized wave emanating from the source. For a given noise voltage source V_s with impedanceZ_s, b_s is given by

$$b_s = \frac{\sqrt{Z_0}V_s}{Z_s + Z_0} \tag{35}$$

From Mason`s rules:

$$\frac{a_2}{b_s} = \frac{S_{21}\Gamma_L}{\Delta} \tag{36}$$

$$\frac{b_2}{b_s} = \frac{S_{21}}{\Delta} \tag{37}$$

$$\frac{a_1}{b_s} = \frac{(1 - S_{22}\Gamma_L)}{\Delta} \tag{38}$$

$$\frac{b_1}{b_s} = \frac{S_{11}(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L}{\Delta} \tag{39}$$

Substituting equations (29), (30) and (36)-(39) into (34), Δ is cancelled, and the insertion voltage gain is:

$$A_v = \frac{S_{21}(1-\Gamma_L\Gamma_S)}{(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)-S_{21}\Gamma_L S_{12}\Gamma_S} \quad (40)$$

S_{11}, S_{12}, S_{21}, and S_{22} of the CM screening are obtained by the measurement of s-parameters. From equation (40), it is clear that the source and load impedance affect the insertion voltage gain of CM screening performance through reflection coefficients Γ_L and Γ_S. For the VNA measurement setup, Z_s and Z_L are standard 50Ω, and $\Gamma_L = \Gamma_S = 0$ is obtained from equations (29) and (30). Therefore,

$$A_v = S_{21} \quad (41)$$

can be used to describe voltage insertion gain and effectiveness of CM attenuation function of the screening technique.

3.1.3.2 Simulations

As discussed above, the voltage insertion gain can be discribed by s-parameter S_{21} in equation (40) with standardized 50Ω source impedance and load and S_{21} also is tansmission coefficient from input port 1 to output port 2. Thus s-parameter S_{21} can be calculated from the relationship between the source voltage and output voltage as discribed in (28)

$$s_{21} = \frac{2V_{out}}{V_{gen}} \quad (42)$$

With circuitry simulation tool Pspice, this voltage insertion gain can be obtained with known variables. Based on the previous schematic equivalent circuit, additional source impedance and load, which are 50Ω respectively, are added to the new simulation circuit, shown in the **Figure 3-14** and its simulation results are shown in the **Figure 3-15**

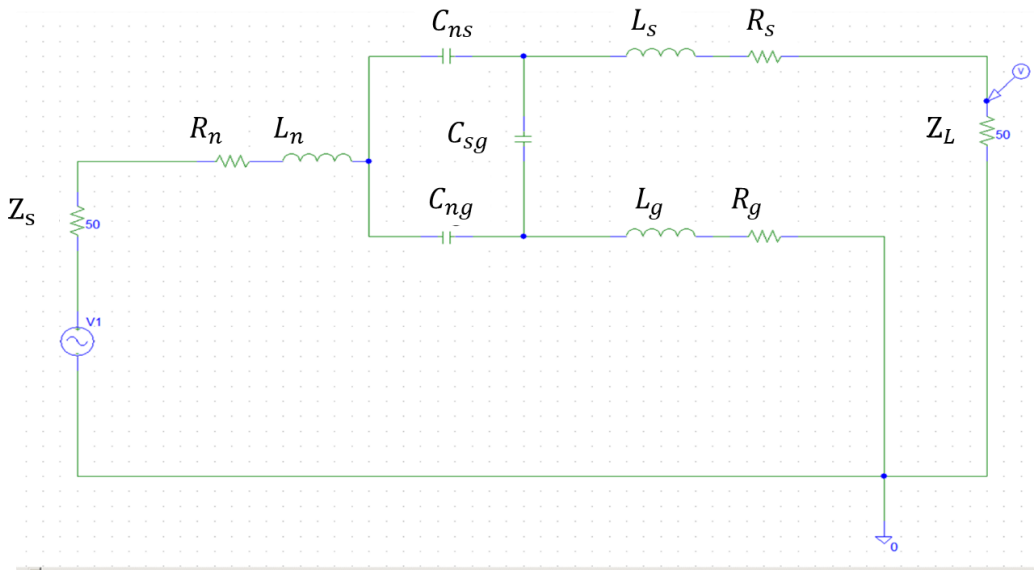


Figure 3-14 Equivalent circuit of voltage insertion gain within Pspice simulation.

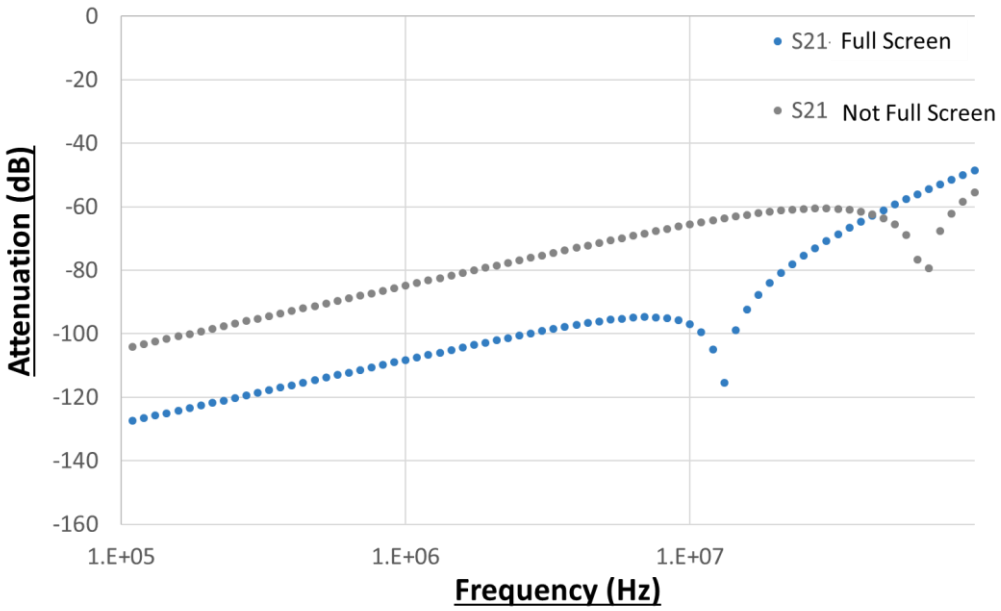


Figure 3-15 Simulation results of voltage insertion gain within Pspice simulation

From the initial frequency 100kHz, the voltage insertion gain or CM screening performance can achieve over -100dB and the effectiveness of screening function gradually becomes worse as the frequency goes higher. This CM screening effectiveness eventually reaches about -60dB attenuation above 50MHz due parasitic inductance at noise current return path and leaked electromagnetic field from noise source to ground. In contrast to the standard layout, an improved layout was proposed and simulated. This

features a full screening arrangement, shown in **Figure 3-16**, where a conductive copper sheet envelopes the noise source and its return point inside and it electrically connected to the screen layer beneath noise source to achieve a close and continuous EM field containment. A practical arrangement of full screening layout is shown in **Figure 3-18**. This full screening arrangement would change the electric field coupling between noise source and screen layer, and between noise source and ground. The change of capacitive coupling is shown in the **Table 3-2.**

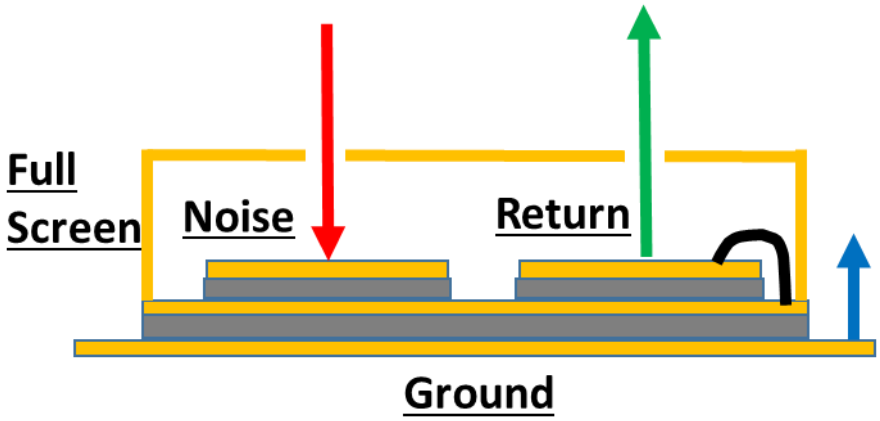


Figure 3-16 Side view of full CM screening arrangement

	Standard arrangment	Full screening arrangment
C_{ns}	23pF	26.6pF
C_{ng}	0.086pF	0.026pF
C_{sg}	127pF	130.1pF

Table 3-2 Comparision of extracted parasitic capacitance between standard arrangement and full screening arrangment

From the extracted parasitic capacitance with and without full screen layer, it is clear that full screening arrangement further improves the electric field decoupling between noise source and ground (4 times smaller from 0.086pF to 0.026pF). It also enhances capacitance coupling between noise source and screen layer. All these changes would work in favour to intentionally couple noise current and collect electromagnetic field onto

the inside of screen layer and return the coupled charges back to the noise source. On the other hand, this layer inevitably increases the stray coupling between screen layer and ground. As discussed above, to avoid coupled charges flowing through the screen layer and reaching the ground, the internal return path should be kept as short as possible to achieve the minimum level of parasitic inductance. The insertion voltage gain of proposed full screen layout simulation result is shown in **Figure 3-15** as the blue dotted line. The full screening arrangement improves the voltage insertion gain by more than -20 dB from the initial frequency up to 10MHz. Above this frequency, the two traces tend to converge together. These results agree well with the previous simulation results of **Figure 3-10:** capacitances C_{ng} and C_{ns} mainly affect the impedance and dominate the impedance ratio at low frequency. A larger Cns and smaller Cng will increase difference of the impedance at screen layer and ground at low frequency and improve common mode current returning function hence increase noise current attenuation. Comparison of two different arrangement well illustrates the impact of full screening arrangement as a complete electromagnetic field containment solution for common mode noise attenuation. It also illustrates that different CM screening arrangement results in different level of electric field coupling among noise source, screen layer and ground, thus resulting in different screening performance.

3.1.3.3 Measurements

We use KEYSIGHT ENA Network Analyser E5080A to measure signal losses between noise source (port 1) and ground (port 2) to investigate the voltage insertion gain, which means how much excited noise can spread to ground side and how much noise current signals can be attenuated through applied screen layer.

In the experimental setup, exactly same size and thickness of copper sheet as the Maxwell simulation model was used to fabricate the test sample shown in **Figure 3-17**. They are

20mm*20mm*0.1mm for the noise source and return paths; 65mm*55mm*0.1mm for the screen layer; 85mm*70mm*0.1mm for the emulated ground layer respectively. The connection between the screen layer and return pad is realized by short and wide copper sheet through soldering process. Between the noise source and screen layer and ground layer, $50\ \mu m$ thickness of polyimide layer was inserted to achieve electrical isolation. Also adhesive layers Pyralus RF1500 ($13\ \mu m$ thickness) was used to laminate polyimide layer and copper foil through an assembling process carried out at a temperature of 199°C, pressure of 2.7MPa and dwell time of 60 mins. The whole test sample was positioned on a nonconductive shelf to avoid any electromagnetic coupling with surroundings.

Excited noise is generated within VNA and delivered onto the noise source pat from port one through a coaxial BNC cable to emulate a noise source within a switching cell where normally active switching devices are located. As the noise receiver, the port two is connected to the bottom ground layer to emulate the case that common mode noise flows into the ground. System ground of both port one and two are connected to the return pad which is next to the noise source. As the CM noise returning function, most electrically coupled noise is circulated back to the return pad and flows into VNA system ground rather than couple to the port 2 which is emulated as the CM ground**. The Figure 3-18** shows the improved full CM current screening arrangement, where additional closed screen layer is positioned on the top to envelope the noise source and return pad. To achieve a near gap-free, complete, closed containment, the four corners of screen box are joined together by soldering process. At the bottom, screen layer is also electrically connected to the laminated screen layer beneath the noise source.

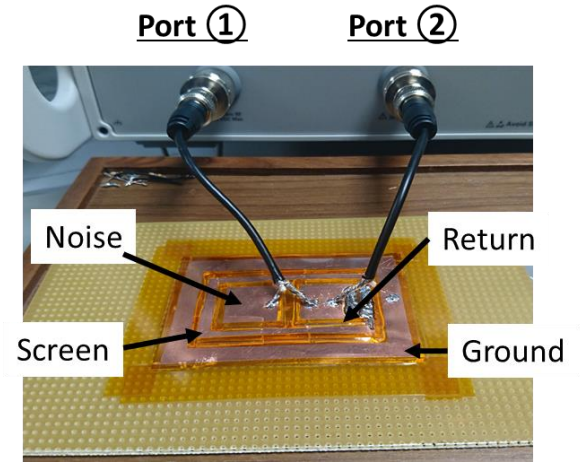


Figure 3-17 Measurement setup of CM noise attenuation with a screen layer



Figure 3-18 Measurement setup of full CM screening arrangement

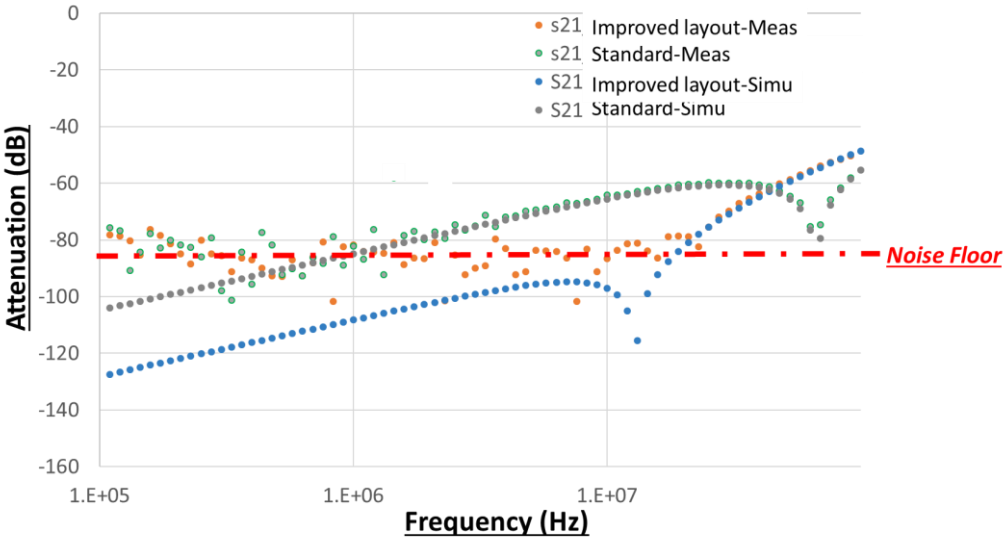


Figure 3-19 simulation and measurement results of standard screening and full screening arrangement.

Compared with simulation results from Pspice, we can see the measurement results from VNA align with each other very well for both standard screening and full CM screening arrangement for levels of attenuation below 80dB (the noise floor of the measurements). There is very small deviation at high frequencies, due to a simplified lumped simulation circuit, which is similar situation to the previous comparison between impedance analyser measurement and simulation results. **In Figure 3-19**, for full CM screening layout, the noise floor (about -85dB~-90dB) extends from 100kHz to 20MHz and then insertion voltage gain goes up to -50dB at 100MHz because of the increase of parasitic impedance in the noise current return path and electromagnetic field leakage from the clearance between screen layer and the BNC cables. Despite reduced CM noise attenuation performance at high frequency, it extends the noise floor of standard screen layout from 5MHz to 20MHz, illustrating the high effectiveness of CM noise decoupling and attenuation of proposed full screening arrangement.

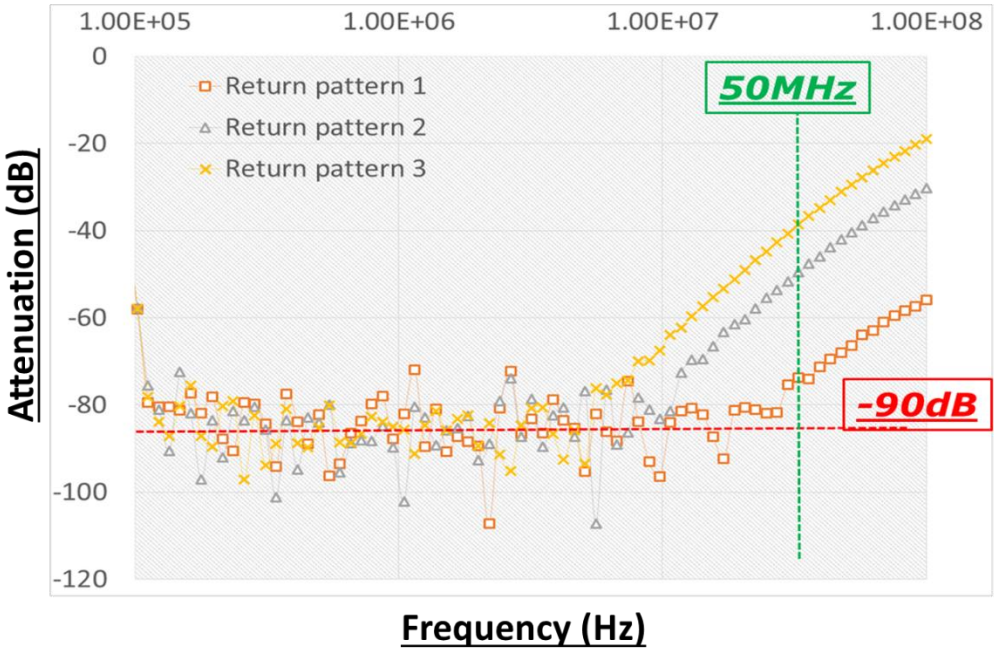


Figure 3-20 Noise attenuation through screen layer with different return patterns

Measurements of noise attenuation with different return pattern were also conducted, and the results are shown in **Figure 3-20**. Orange trace represents the lowest impedance at the connection between the screen layer and returns pad. It used short and wide bus bar and the connecting location on the surface of the screen layer is as close as possible to the return pad. Another two traces represent higher impedance where grey trace used thin wire instead of wide bus bar with the same length and yellow trace used a long wire to emulate longer return path from screen layer to the return pad. Different return patterns produce different Y_S and result in different signal attenuation from noise source to ground. These trends in insertion voltage gain correspond to the previous results measured by impedance analyser. Lower impedance ratio of internal current path compared with the external path always results in better screening effectiveness. These simulation and measurement results again well illustrate that the low impedance of internal noise current return path and maximum decoupling of noise source from ground from full screening arrangement are very critical to common mode noise attenuation.

3.2 Electromagnetic shielding

3.2.1 Introduction

Previous section explained the CM screening and noise current returning function of partial or full conductive layer surrounding the noise source. This conductive metal layer has two-fold effects, and the second function is magnetic field shielding. It helps to attenuate and contain varying magnetic field within continued shield layer. This section begins with mechanism of magnetic shielding function, followed by magnetic field simulations and H-field measurement.

Current flow (movement of charge) produces a magnetic field according to Ampere`s law: $\nabla \times \mathrm{H} = \mathrm{J} + \mathrm{dD}/\mathrm{dt}$. All circuit elements generate electromagnetic fields, intentional ones such as inductors; unintentional ones such as stray inductance inside power module. Additional energy is stored in these stray electromagnetic fields. Very fast changing currents circulating inside power module, for example around the switch commutation loop(s), will generate strong electromagnetic fields, leading to unintentional EMI. Reducing the size of the circulating current loops will reduce the generated EM fields and reduce radiative EMI noise. Alternatively, metal shield layers can be employed to effectively stop electromagnetic waves from propagating outside power converter. Eddy currents generated on the surface of the metal shield layer produce counter-effect electromagnetic fields which cancel the original field. This shielding concept is shown in **Figure 3-21**. The shielding effectiveness is decided by the skin depth, distance from noise to shield layer, size and thickness of shield layer. A thicker shield layer with continuous design can provide massive magnetic field attenuation.

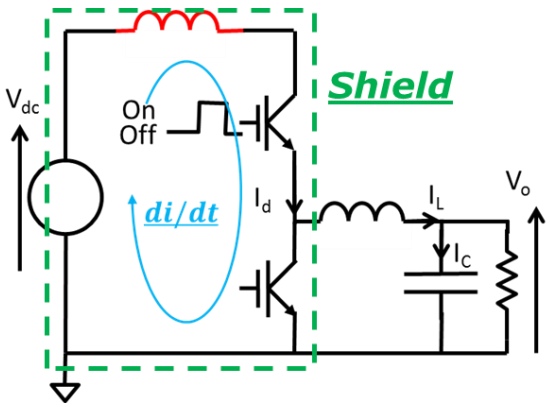


Figure 3-21 shielding swtiching cell to attenuate radiated EMI noise

3.2.2 Theories of shielding radiated EM noise

From the outset, it is important to understand whether electromagnetic analysis and shield design should be undertaken in terms of near field or far field perspective. Typically, field analysis should be undertaken within a distance of one sixth of wavelength in the near field perspective. The distance of the boundary separating the near field from the far field region, is expressed by $\lambda/2\pi$, the boundary distance being calculated based on field propagation through a medium with unity relative permeability and relative permittivity. In the near field region, the electromagnetic fields are complex and the properties of the field are primarily characterized by the source characteristics. Importantly, the ratio of electric field and magnetic field is not constant. The physical scale of most power electronic equipment means that the near field behaviour is most relevant and thus the shield design and shielding effectiveness must be based on this assumption.

Shielding at higher frequency is based on the eddy current effects through utilization of conductive shield materials. Incident magnetic fields induce current in a shorted conductive loop and the current in turn generates counter fields that attempt to cancel the incident fields. The magnetic flux due to eddy currents has components 180 degree out of phase with incident flux, as shown in **Figure 3-22**. (**Figure 3-22** shows an ideal case

of interaction between incident magnetic field and induced magnetic field. The practical case would be very complicated, and in this research Ansys Maxwell 3D simulation tool is used to well analyse magnetic field distribution and attenuation with different arrangements). The induced magnetic flux will cause an electromagnetic force (EMF) opposite to that of the original current excitation, resulting in increase of resistance and decrease of self-inductance. The shield thickness required in order to generate ample amount of eddy currents for proper field cancellation is directly proportional to the skin depth δ, which decreases with increasing frequency, shown in **Figure 3-23**. When a magnetic field generated by a current-carrying conductor comes in contact with a material of infinite conductivity, then skin depth will become infinitely small, and we can consider it approaches $\delta \approx 0$. In this case eddy current only flows at the surface of shield layer. Magnetic field strength inside shield layer is infinitely small, no magnetic field can penetrate through metal shield layer and all magnetic fields near shield layer are repelled (or diverted) away from shield layer, tangential along the surface of shield layer.

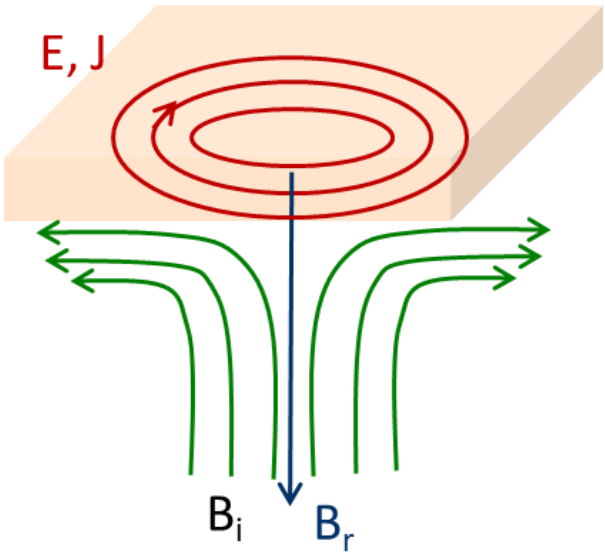


Figure 3-22 Flux due to eddy currents Br has components out of phase with flux Bi: induces voltage in-phase with original current.

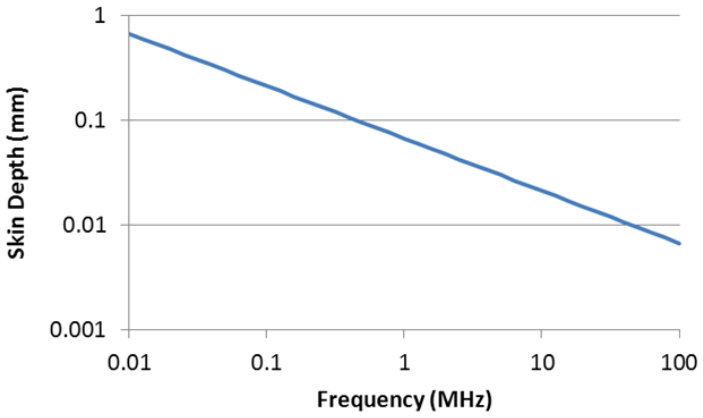


Figure 3-23 Skin depth along with different frequency

In order to better apply this theory to shield design, and investigate impact on shielding effectiveness of various different parameters, the method of Images[133][134][135][136] is used to visualize how eddy currents cancel out original magnetic field to achieve better shielding result. A mirror image of original current excitation is used to replace metal shield with the same boundary condition ($B = 0$). Metal shield layer (with infinite conductivity or a good conductor such as Copper) acts as another excitation with same distance, size, current excitation, but 180 degrees out of phase. Based on this method, it's easier for us to understand which parameters will affect magnetic field cancellation.

On the other hand, more fundamental field theory approach can be undertaken for EM field analysis, which is very similar to the traditional plane wave method. Although shielding target should be considered under near field condition rather than far field plane wave condition, some of the concepts are still valid, and similar discussion can be found in [137], [138]. Generally total shielding effectiveness of a conductive shield is equal to the sum of the absorption loss (A) and the reflection loss (R), and correction factor (B) [1-3]

$$S = 20log\frac{H_0}{H_t} = A + R + B \tag{43}$$

Where:

H_0 =Incident field strength

H_t =Field strength of transmitted wave out of the shield

Absorption Loss

When an electromagnetic wave passes through a shield, its amplitude decreases exponentially. This decay occurs because eddy currents induced in the medium produce ohmic losses and heating of the material. Therefore the absorption losses can be written by

$$E_1 = E_0 e^{-t/\delta} \tag{44}$$

$$H_1 = H_0 e^{-t/\delta} \tag{45}$$

Where E1 and H1 are the wave intensity at a distance t within the shield layer.

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{46}$$

$$A = 20(\frac{t}{\delta})log_{10}(e) \tag{47}$$

μ , σ are the material permeability and conductivity

From this equation, we understand that absorption loss is closely related to material property (permeability and conductivity), frequency of electromagnetic wave and thickness of shield layer no matter the condition is under far field or near field.

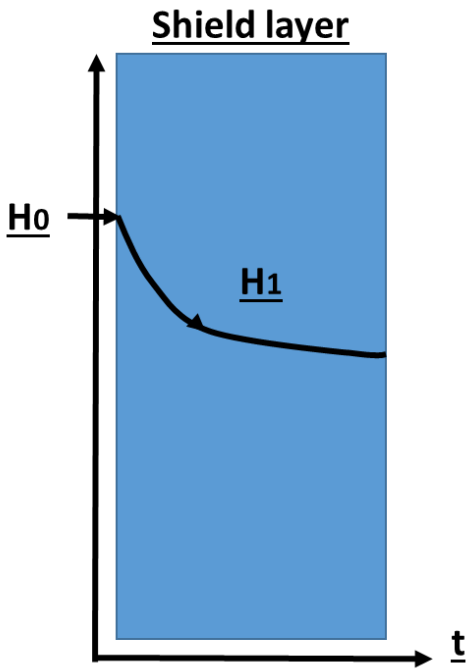


Figure 3-24 Magnetic field decays through shield layer

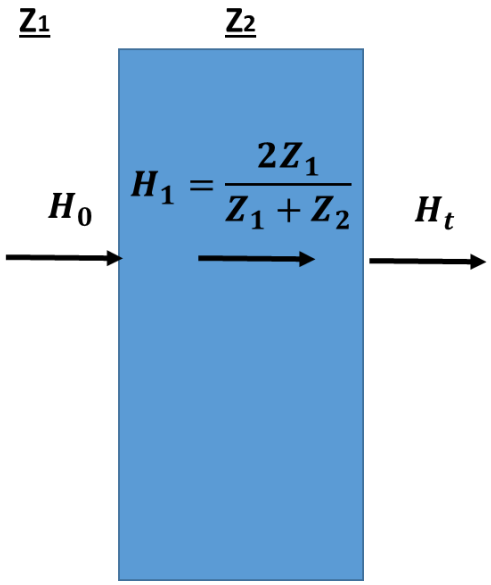


Figure 3-25 Magnetic field reflects at the interface of different medium

Reflection Loss

Reflection of electromagnetic field occurs at the interface of two different medium, such as the air to shield or shield to air boundary. A wave impedance and characteristic medium/shield impedance are defined by

$$Z_w = \frac{E}{H} \tag{48}$$

$$Z_s = \sqrt{\frac{j\varpi\mu}{\sigma + j\varpi\epsilon}} \tag{49}$$

Based on these two impedances, reflection loss is defined by

$$R = 20log\frac{|Z_w|}{4|Z_s|} \tag{50}$$

Reflection loss quantifies how much of the electromagnetic fields are attenuated through reflections occurring at the interfaces of the media. The intensity of the magnetic field inside the medium, H_1, and intensity of the field that has been transmitted through the medium, H_t, are a function of characteristic medium impedances, Z_1 and Z_2. For the near field assumption, $r < \lambda/2\pi$, the wave impedance due to a point source of the magnetic field may be approximated as

$$|Z_w| \approx 2\pi f\mu r \tag{51}$$

Where r=distance from source to shield

With (38), the reflection loss at the specific distance from a point source producing only a magnetic field can be obtained. Different from absorption losses, reflection losses are significantly affected by wave impedance of propagating medium which vary very much based on far field or near field condition. If the source has high voltage and low current, the wave impedance is greater than 377Ω, and the field will be dominated by the electric field. If the source has low voltage and high current, the wave impedance will be less that 377Ω, and the field will be dominated by a magnetic field. However, in practice, when shielding EM field at switching cell, the source will include a combination of both electric and magnetic field due to high dv/dt node and di/dt current loop.

3.2.3 Simulations

Analytical analysis can only provide a physical understanding about electromagnetic field shielding and the important factors which impact on shielding effectiveness. And these analyses are based on very simple geometry mainly 1-dimensional or infinite shield layer and simple excitation. Most of the actual problems are very complicated and 3-dimensional, where 1-dimentional analytical approaches cannot be applied. Therefore, computer aided tools have been more and more involved in the magnetic component design. FEM method is one of the most popular numerical techniques. With the help of high performance computers, the simulation tools have greatly widened the range of the problems amenable to numerical analysis. Maxwell software developed by Ansoft is used to solve Maxwell`s differential equations for quasi-static electromagnetic fields using FEM [5][139]. The basic principle behind FEA analysis is to break up a larger simulation into many smaller, solvable tetrahedral elements. In each tetrahedral element, the simulation solves Maxwell`s differential equations to evaluate the magnetic fields in the system. The Maxwell 3D package, using eddy current solver method takes into account the eddy current effects, skin depth effect, cornering effect, and proximity effect encountered in high frequency. Eddy current solver uses an AC current input and computes the magnetic field in the system and stores them in magnitude and phase vectors by using Maxwell equation

$$\nabla \times \left(\frac{1}{\sigma + j\omega\varepsilon} \nabla \times H \right) = j\omega\mu H \tag{52}$$

Where σ represents conductivity, ω represents radian frequency, and H represents magnetic field intensity.

At the same time, energy stored in a magnetic field is given by

$$W = \frac{1}{2} L I^2 \tag{53}$$

This energy is equal to the energy stored in the leakage inductance produced by an external AC current source. From these equations we can understand that magnetic energy stored in system where current paths exist. If a good conductive shield is placed nearby, magnetic fields induced by eddy currents cancel the original magnetic field, reduce stored magnetic energy in the system and result in reduction of leakage inductance.

From previous analytical methods, we can see absorption loss is inversely proportional to the skin depth, thus closely related to permeability and conductivity [140]. Potential shielding materials are Copper, Aluminium, Nickel and Iron, etc. among these materials, Iron seems to be the ideal choice for achieving the highest absorption loss. On the other hand, copper has the highest reflection loss. Choosing shielding material needs to balance the absorption loss and reflection loss. This thesis does not discuss the shielding effectiveness in terms of different material, but focuses more on shielding arrangement.

Magnetic field shielding effectiveness was investigated through the Maxwell 3D package. Utilizing eddy current solver method takes into account the eddy current effects, skin depth effect, and proximity effect encountered at high frequency. By considering current commutation within switching cell as a noise source, constantly generating radiative EMI noise, a simple model can be built within Maxwell 3D as illustrated in **Figure 3-26**. This model well emulates the case of half bridge switching cell. Simulation results illustrate magnetic field generated from current commutation loop and shield effectiveness of the external shield layer. In the simulation model the top copper layer is built to emulate the current commutation loop between top arm and bottom arm of half bridge having a size of 40mm*31mm* 0.1mm. In the middle, a polyimide layer having a size of

40mm*31mm*0.25mm is inserted. At the bottom, a 52mm*43mm*0.1mm copper shield layer is built. Noise excitation is created on the surface of boundary and coupled onto one side of the current loop through a thin wire and returned on the other side of loop. Excitation frequency is 1MHz. In this loop all wire bounds and bus bar are omitted for simplicity.

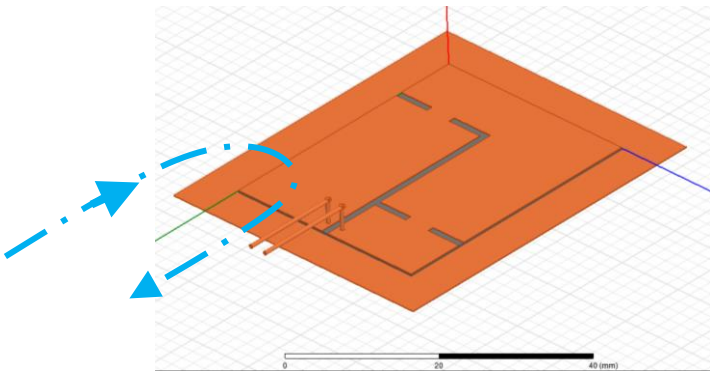


Figure 3-26 Model in Maxwell 3D (Current loop is indicated as a blue dash line)

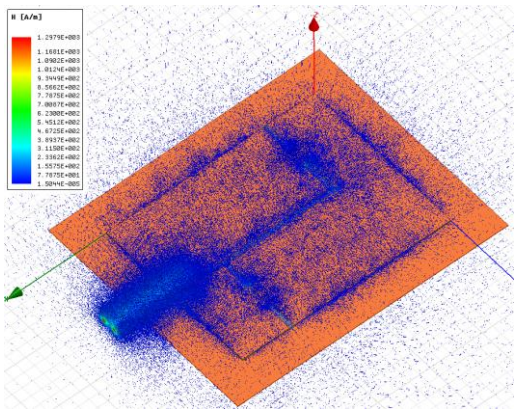


Figure 3-27 3D Magnetic field distribution

Figure 3-27 shows the magnetic field plot under high a 1MHz noise excitation condition. It is clear that the intensity of magnetic field is highest near the connection between each pad and near the wires due to high current density.

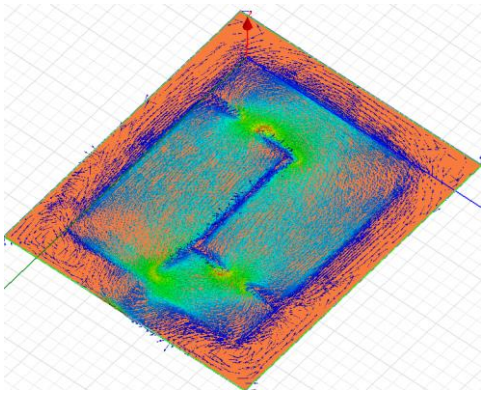


Figure 3-28 Induced eddy current on the bottom shield layer

Figure 3-28 shows the induced eddy current on the shield layer. Its circulation direction is opposite to the excited current on the top (source) layer and its intensity reflects the intensity of the source magnetic field. When the shield layer at the bottom is very close to the source layer, the induced eddy current distribution resembles the top layer current. In this case the induced current in the shield layer increases and counteracts the commutation loop and greater amounts of field cancellation are achieved. **Figure 3-29** shows the side view of magnetic field plot. High intensity of magnetic field can be found at the edge and within the current loop while the Copper shield layer stops magnetic field propagation below the shield.

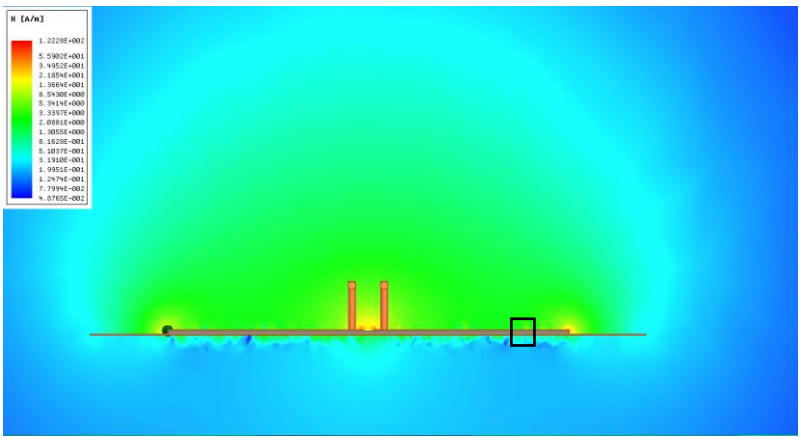


Figure 3-29 Side view of magnetic field distribution

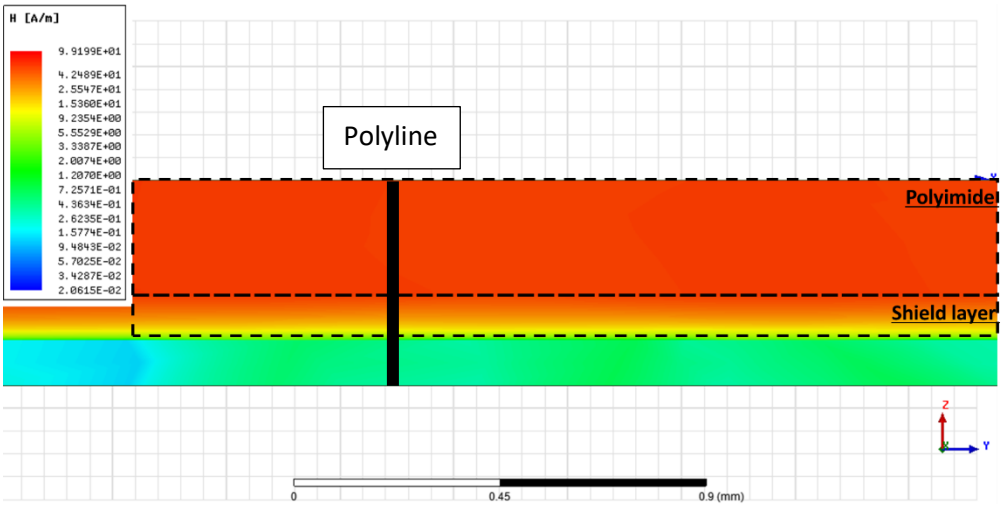


Figure 3-30 detailed H field distribution on selected cross-section

Figure 3-30 shows the detailed H field distribution from top side of polyimide through the whole shield layer. It is clear that the strength of H field within polyimide is constant and is greatly reduced within shield layer. As an example, one polyline was selected for the plot of H field intensity as shown in **Figure 3-31**. X-axis is the distance (µm) from polyimide layer to the bottom side of shield layer, Y-axis is H field strength (A/m). Shield layer attenuates most magnetic field and on the other side of shield layer is there much less intensive magetic field. Converting linear plot of H-field strength to absorption loss, **Figure 3-29** gives radiated noise attenutaion through the shield layer with the thickness of 0.1mm. Simulation result aligns well with analytical calculation: $Absorption\ loss = \exp(-\frac{thickness}{skin\ depth})$: this 0.1mm thick shield layer can provide about -30 dB radiated noise attenuation. Therefore thickness of shield is one importance factor for radiated noise attenuation.

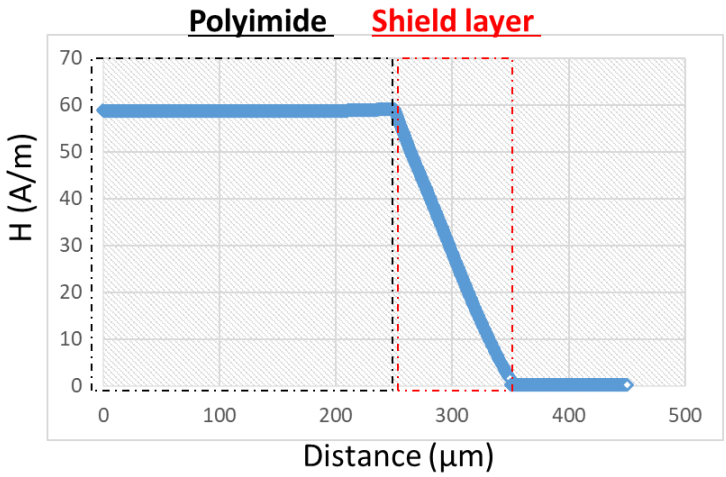


Figure 3-31 H field strength plot along a polyline from polyimide layer to shield layer

From these results, we can see thickness of shield layer is one of essential factors for radiated noise attenuation. However, some magnetic field can go around the edge of shield layer and reach the backside. For the shield layer to be effective, it must be a complete and closed arrangement. Partial shielding arrangement shown above cannot provide overall good shielding effectiveness. To illustrate this idea, another model is built in Maxwell, shown in **Figure 3-32**, which has a second shield layer positioned 5mm above existing layout. The resulting magnetic field plot is shown in **Figure 3-33**. It is very clear that top shield layer contributes to magnetic field containment. Compared with **Figure 3-29**, more magnetic field is contained between two shield layers rather than propagating upwards. Induced eddy current both on the top and bottom helps to cancel the original radiated noise. Close distance between noise source and shield layer ensure high coupling between induced and original magnetic field, improving field cancellation, and a significant reduction. However, four sides of noise source are still open and magnetic field can leak from there. For a complete shielding arrangement, the last model was built with complete and closed shield layer, shown in **Figure 3-34**. It has only one small opening on the shield layer for the signal connections, and this opening should be kept as small as possible to avoid field leakage. The width and the size of opening are also the key factor

of electromagnetic field leakage. As the aperture becomes shorter, the radiation efficiency will decrease at a rate of 20dB per decade, hence the shielding effectiveness will increase at the same rate.

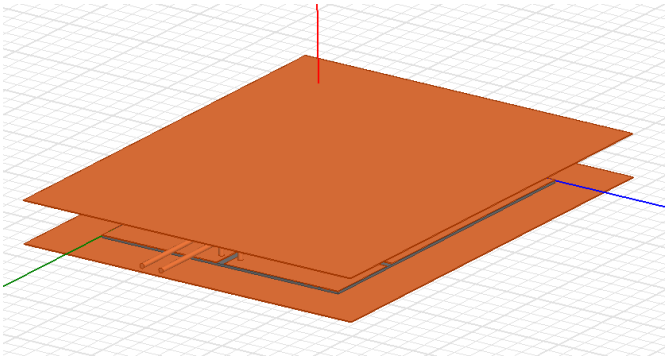


Figure 3-32 3D model with two shield layers in Maxwell

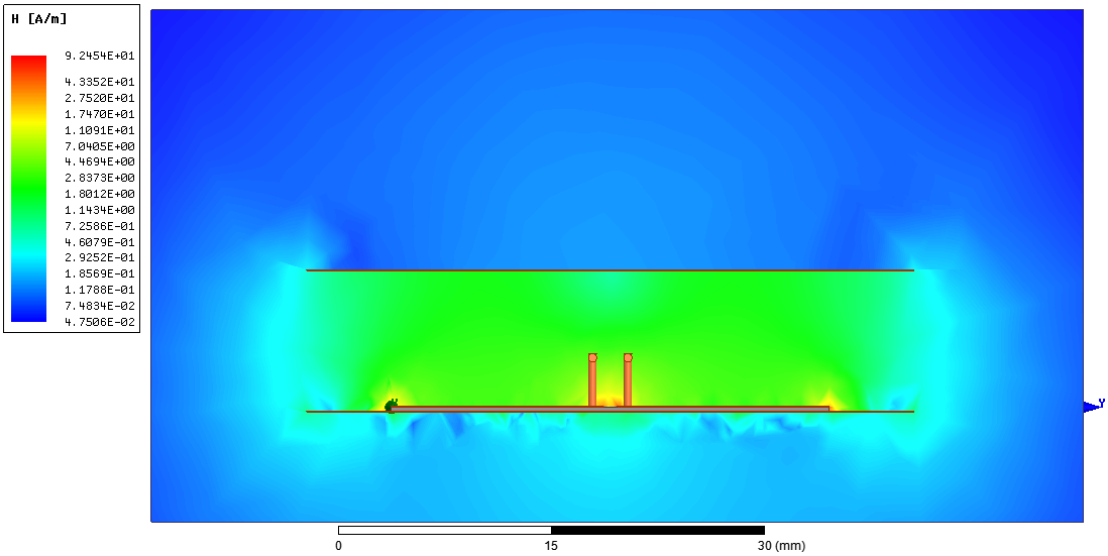


Figure 3-33 Magnetic field plot with two shield layer arrangement

From the magnetic field plot of **Figure 3-34**, complete and closed shielding arrangement can confine radiated noise within specific shield layer and all magnetic field passing through would be significantly attenuated. This result illustrates that a closed shield layer with thickness of several times of skin depth would be able to decouple radiated noise from the external and provide enough radiated noise attenuation and contain nosie within switching cell.

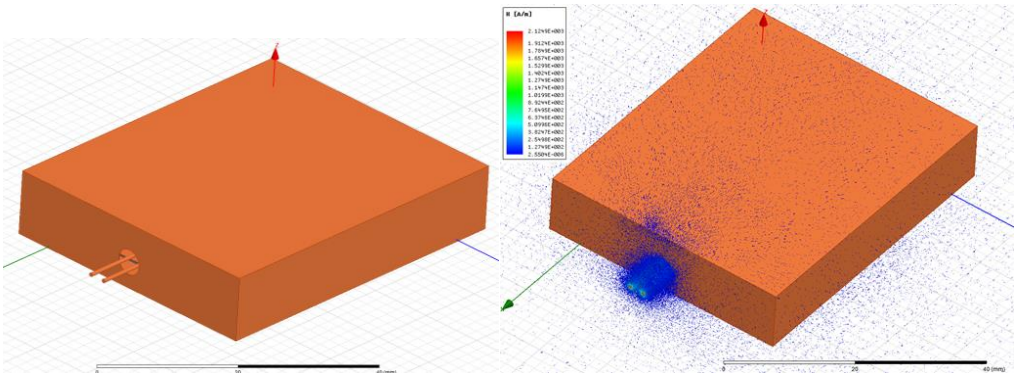


Figure 3-34 3D model with complete and closed shield in Maxwell

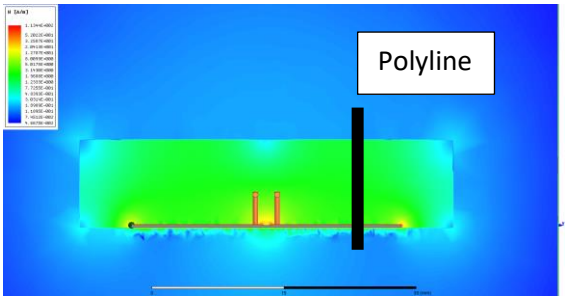


Figure 3-35 Magnetic field plot with complete and closed shield layer arrangement

To confirm the magnetic field shielding effectiveness around the radiated noise source with and without shield layer. Magnetic field strength is plotted along a polyline which goes through the whole shielding arrangement near the centre from the top side to the bottom side shown in **Figure 3-35**. **Figure 3-36** shows the magnetic field comparison between no shield, partial shield, and full shield from **Figure 3-28, 3-33**, and **3-35**, and their plots are blue line, orange line and grey line respectively. X- axis is distance in mm from the bottom, and Y- axis is magnetic field intensity in log scale. Two red dot lines indicate the top and bottom side the shield layer. The peak on the left side indicates very high concentration of magnetic field between current loop pattern and bottom shield layer, which originates from the noise source and its induced eddy current in the shield layer. Gradually reduced magnetic field intensity in blue line shows the radiated magnetic field strength is inversely proportional to the distance from the noise source with no shield arrangement. On the other hand, from the partial and full shield plot is it clear that

a very obvious step change of magnetic field intensity happens across the shield layer. The step change of the field intensity is about -27dB and this result is aligned with the previous simulation result of radiated noise attenuation through a copper shield layer with 0.1mm thickness. Magnetic field intensities between shield layers are nearly constant. It is interesting to see the difference of magnetic field strength outside shield layer between partial and full shield layout. This result is because with a partial shield layer some radiated H field leaks from four sides and reaches the external environment. Thus full shield layer can provide better shield effectiveness over other arrangements. All results above demonstrates shield layers provide good radiated noise attenuation and closed shield layer with minimum opening on it could provide the best overall shielding effectiveness.

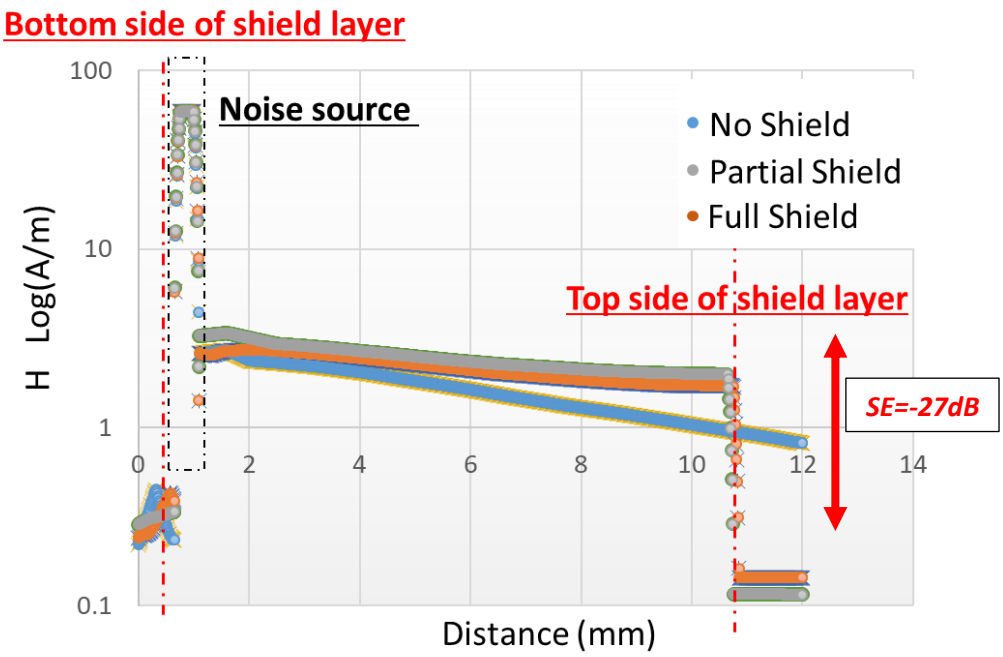


Figure 3-36 Magnetic field plot and comparison between no shield, partial shield and full shield arrangement.

3.2.4 Measurements

Experiments were carried out in order to validate the shielding effectiveness and confirm the impact of a complete and closed shield layer on radiated noise attenuation. A near

field probe was used to measure the magnetic field radiation and confirm the impact of different shielding arrangement. Near field probe used in this research is LF-R-400 from LANGER EMV-Technik and its effective frequency range is from 100kHz to 50MHz. The LF-R 400 H-field probe has a large diameter (25 mm), which makes it highly sensitive and suitable for measurements within ranges up to 10 cm around assemblies and devices. With its large tip diameter (25 mm), it is more sensitive and thus is able to detect a greater area of the magnetic field. Measured probe voltage (V_{prob}) at spectrum analyser is proportional to the magnetic field that's perpendicular to the loop. The final magnetic field strength H_{noise} going through the near field probe can be calculated (by Equation 54) from the voltage output signal of the V_{prob} and characterized correction factor of this probe, shown in **Figure 3-37**. The correction factor of the magnetic field probe compensates the variable coupling factor as a function of frequency.

$$H_{noise}\left[dB\mu\frac{A}{m}\right] = V_{prob}[dB\mu V] + K_H\left[dB\frac{\mu A}{\mu V m}\right] \quad (54)$$

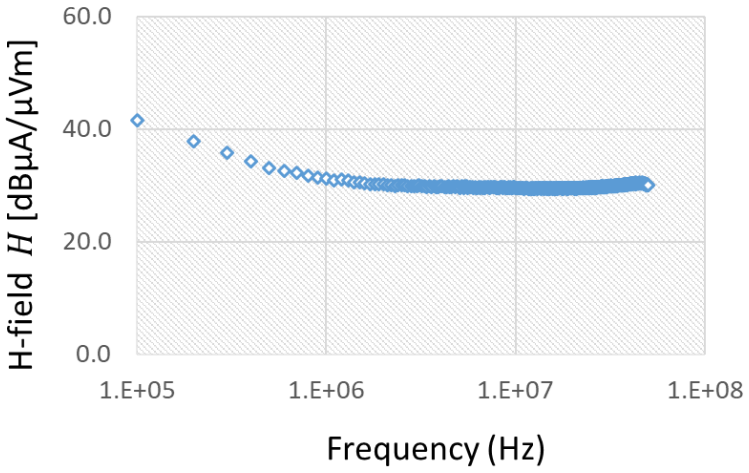


Figure 3-37 Characterized magnetic field correction factor of near field probe LF-R-400

In this experiment, a sample consists of current commutation loop on the top as a radiated noise source, a copper layer with the thickness of 0.1mm at the bottom, and a polyimide isolation layer in the middle, shown in the **Figure 3-38**. Another sample is based

on the first layout and in addition, is covered with a complete shielding layer. In full shielding arrangement, top and side of the shield layer is electrically connected to the bottom shield layer, and edges are completely sealed through soldering process to achieve a complete and closed shielding layout. There is one opening with 5mm diameter for the BNC cable passing through. These samples have the same size as the models simulated in Maxwell 3D. A noise excitation is created by a function generator and this noise is coupled to the current loop through a coaxial BNC cable, where the signal line of BNC cable is soldered on the one side of current loop and the ground line was solder on the other side. Excited noise is 1MHz sinusoidal signal with 5V peak-to-peak voltage to emulate current circulation within a switching cell and its radiated noise. Near field probe is positioned on the top of the noise source at 11mm height and is connected to a spectrum analyser with a 50 Ω input.

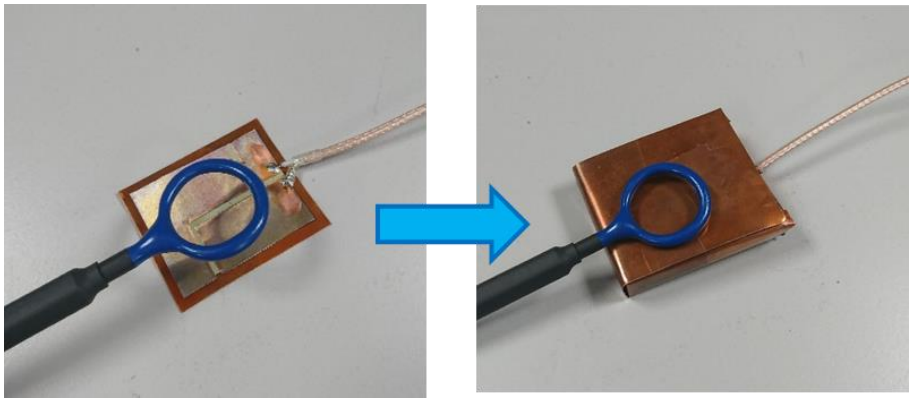


Figure 3-38 Radiated noise measurement with near field probe

By comparing detected radiated noise level between no shield and full shield layout, the shielding effectiveness of shield layer can be validated. Also by comparing results from the same full shield layer but with different thickness, the impact of thickness on shielding effectiveness can be studied. **Figure 3-39** shows measured radiated noise H_{noise} $\left[dB\mu\frac{A}{m}\right]$ with different measurement position. In the first position, H field probe is positioned on the top of tested sample with the probe head parallel with its surface to measure vertical

radiated noise. Its measurement results are shown on the left of the **Figure 3-39**. In the second position, the probe is positioned to the side with the probe head perpendicular to the sample surface to measure horizontal radiated noise. Its results are shown on the right of the **Figure 3-39**. Measuring position and direction would result in different H-field coupling from radiated noise to the probe. From the results, there is more vertical radiated noise at the centre than horizontal noise at the side of noise source. In addition, we can see the significant radiated noise reduction with and without full shield layer. This trend is aligned with the previous H-field distribution and H-field plot along the polyline, which shows about -27dB radiated noise attenuation through 0.1mm thick full shield layer. Thus the measurement with near field probe can be used to validate shielding effectiveness with different shield arrangement effectively and efficiently.

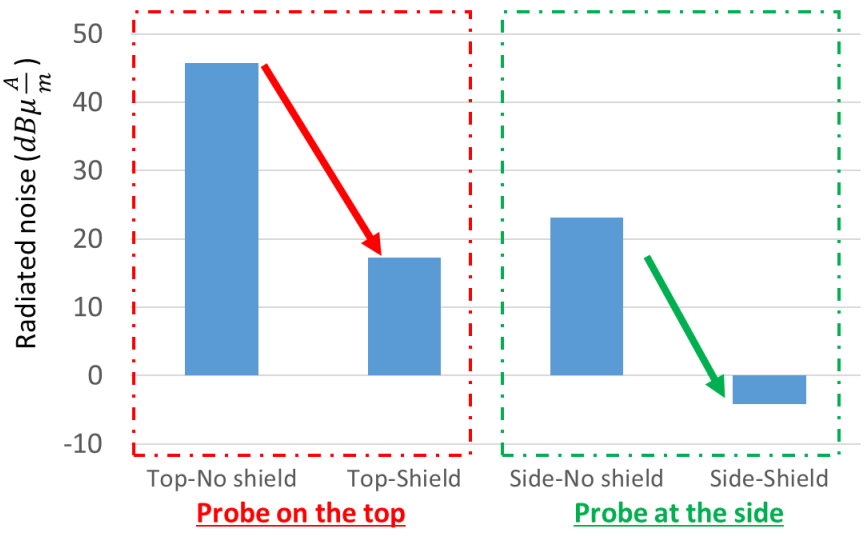


Figure 3-39 Shielding effectiveness comparison W/O shield layer

Figure 3-40 shows the shielding effectiveness of full shield layout with different shield layer thickness from 50um, 100um to 250um. Aligned with the analytical calculation: $Absorption\ loss = \exp(-\frac{thickness}{skin\ depth})$, a thicker shield layer would provide more noise attenuation. A full shield layer with 250um thickness, which is 4 times of skin depth at excited noise frequency 1MHz, could give about -75dB radiated noise

attenuation. Therefore, thick enough shield layer is necessary for better shielding effectiveness, however it would add extra weight to the switching cell and worsen cost performance.

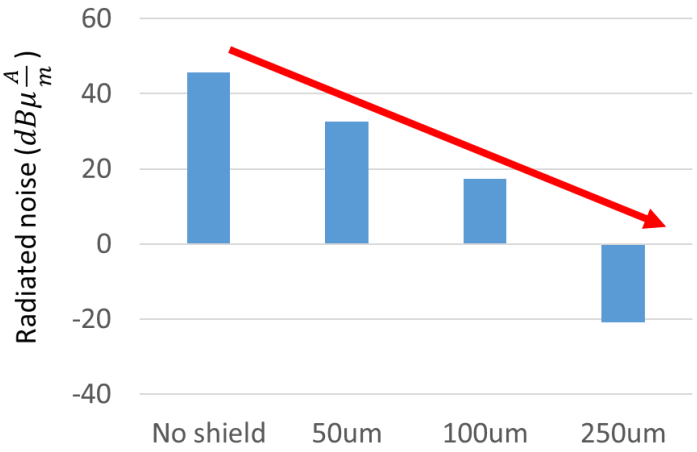


Figure 3-40 Shielding effectiveness comparison between different thicknesses of shield layer

3.3 Conclusions

In this chapter, we have proposed and analyzed a CM current and magnetic field attenuation technique employing screening and shielding layers within a power switching cell. We used the simulation tool ANSYS Maxwell Q3D and circuit simulator PSpice for prediction and an impedance analyzer to verify the high frequency performance of the screen layer. Good agreement between a simple equivalent circuit model and measurements were obtained. A Network Analyzer was used to investigate screening effectiveness for different screen layer arrangements. Our results show that screening effeteness is closely related to the screen geometry and associated electrical return path within the switching cell. A low-impedance current return path is critical to minimizing noise transmission to ground over a wide frequency range.

For magnetic field attenuation, we used the simulation tool Maxwell 3D for analysis and prediction and a near field probe to validate the shielding effectiveness of different shield arrangement. Measurement results show that magnetic field effectiveness is closely

related to the shield layer thickness and shield arrangement with same material. A complete and thick enough shield layer would give the best shielding performance.

In general, electromagnetic screening and shielding techniques provide very good EM noise containment and provide an attractive method to achieve low EM emission levels in both conducted and radiated noise. A complete and closed conductive layer can provide these two function shielding and screening simultaneously and may eliminate the need for a separate common mode filter for some configurations.

However, a complete shield layer is not very easy to achieve. The opening for signals passing through the screen/shield layer would allow electromagnetic flux to leak to the external environment, generating common mode noise current and radiated noise. On the top of that, all signals coming out of the EM containment should be filtered to an acceptable level which has less $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$. Otherwise, unfiltered connection would allow additional coupling routes through the screen layer to the external environment, compromising the overall shielding and screening performance. Therefore, integrated filtering techniques and EM field blocking techniques around openings in the screen layer are very critical to this concept and will be discussed in the chapter 4.

Chapter 4. Broad band integrated filtering technique

4.1 Introduction

Electromagnetic interference arises from the rapid voltage and current transitions occurring during operation of the switching cell. Suppression of EMI is typically achieved by a combination of ① filtering (differential and common mode), to attenuate conducted emissions and ② shielding to attenuate radiated emissions. The general function of passive filters is to prevent noise current propagation from the source to the load by providing a high attenuation forward path between the noise source and the load coupled with an effective means to either return unwanted noise to the source or dissipate the associated noise energy in the filter. On the top of understanding the noise source of electrical system and the impedance of noise propagation path, the attenuation from passive filters is determined to suppress EMI noise to acceptable levels that meet with various EMC standards. Typically, such filtering functions are added at converter and system level but not integrated into the switching cell. At the frequencies below several MHz, passive filters typically provide enough noise attenuation, however, at higher frequencies, filter performance is compromised by parasitic inductance and capacitance within the filter system and by mutual electromagnetic coupling between filter components and filter stages. In addition, the return path for high frequency noise back to its noise source might not be effective due to the parasitic impedance at the noise current path. Therefore, the realisation of broad stop band noise filters becomes challenging with conventional filter configurations.

In contrast to the conventional approach of tackling EMI by applying passive filters to attenuate noise outside the switching cell, we propose an alternative approach to solve EMI problems within the switching cell, illustrated in **Figure 4-1**. By applying partial or complete conductive partitions or by embedding an electrically-conductive screen layer,

internally generated switching noise may be returned to the source. Common mode noise which would otherwise be capacitively coupled to ground is returned direct to the screen. Internally generated magnetic fields are attenuated in the screen layer or in additional shielding layers whose thickness and extent are chosen to produce the desired degree of attenuation. On the top of screening and shielding techniques, differential mode noise is attenuated by low-pass filters that are applied at each of the electrical ports and whose high-frequency return currents are directed back to the screen and hence to the noise source.

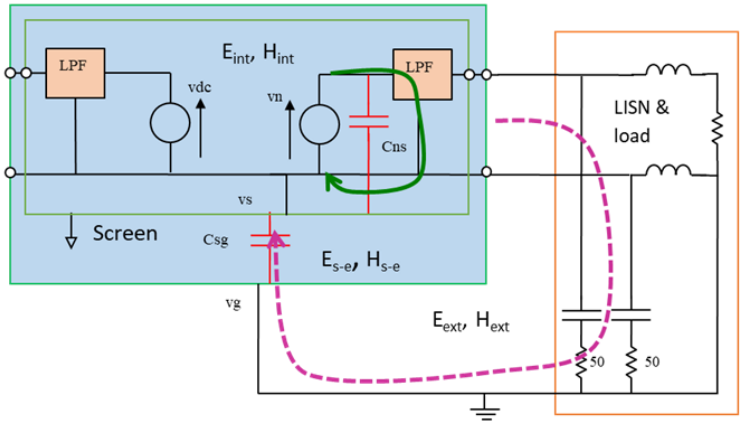


Figure 4-1 Simplified equivalent circuit of integrated swtiching cell with screening and shielding techniques

However, in practice, the filter components are not ideal and their characteristics deviate from those of the theoretical components[95]. Parasitic elements within the filter include both self-parasitics and mutual-parasitics. They are critical to filtering performance in the high frequency range. The self-parasitics include the equivalent series inductance (ESL) and equivalent series resistance (ESR) in capacitors, and equivalent parallel capacitance (EPC) and equivalent parallel resistance (EPR) in inductors. ESL is generated by the capacitor`s leads as well as within the capacitor structure itself. In the case of an inductor, EPC is generated due to the electric field distributed between the winding turns and the core. The ideal inductor impedance is proportional to the frequency. However, in practice

it is decreased by the EPC effect after the first self-resonance. This effect results in the inductor's high frequency blocking capability being reduced. Similarly, capacitor performance is degraded due to the ESL and ESR effects at high frequency. Other ESL and EPC cancellation methods have been mentioned by [141][97][142].

Mutual coupling can also occur between different components and gives rise to additional parasitic effects in the filter. In a circuit there are various mutual coupling points because each component can act as both a source and receiver of electromagnetic fields. Much better filtering performance can be achieved through the proper layout of components. Generally, reducing mutual coupling is realized by changing magnetic coupling direction to perpendicular position[142], by shielding to decouple electromagnetic field linking[95], or by increasing the distance between components. However this final approach may not be desirable as it will significantly increase the overall volume of the filter.

Apart from effects of self-and mutual-parasitics, another importance factor is the presence of parasitic impedance in the current return path. [143] describes the impact of the layout of multistage filters and its return path arrangement on filtering performance from simulation and measurement results. By improving filter layout to a compact arrangement, the presence of parasitic impedance in the current return path can be minimised.

As an alternative to conventional filters, integrated filter strategies have been investigated, where inductive and capacitive elements are integrated together in the same component, for example two windings, separated by a dielectric material. The resultant structure has distributed inductance and capacitance, and behaves as an electromagnetically integrated LC structure[144][145]. In [145], despite the decreased parasitics within the filter system, filter attenuation decreases significantly above 10MHz and reduces to only -20dB or -30dB at 30MHz. This is because the parasitic EPC and ESL

cannot be eliminated completely and they determine filter performance and behaviour at very high frequency. Indeed, irrespective of the method of construction, all passive components display a mixed L-C-R behaviour. In addition, the effects of electromagnetic coupling between each filter component and each filter stage dominate the effectiveness of filter performance at high frequency. As a consequence, for frequencies above, say, 100MHz, it is very easy for noise to couple from the source side of filter directly to load side without passing through each filter stage. Therefore careful electromagnetic field decoupling and containment are needed.

This chapter focusses on the achievement of high attenuation wide stop band differential mode noise filters at the electrical ports. Firstly, it introduces the concept of suppressing electromagnetic interfere by using multi-stage integrated filters within switching cells and investigates component-level modelling and characterization. Secondly, this chapter discusses shielding and partitioning each filter stage to improve noise attenuation at very high frequency. In the end, advanced electromagnetic field blocking connection is introduced, achieving attenuation levels of over -120dB up to 1GHz.

4.2 Filter configuration, simulation and characterization

4.2.1 Component-level characterization

To achieve high noise attenuation and wide stop-band filter characteristics, broadband filters typically consist of a cascaded series of low-pass filters whose configuration and cut-off frequency is chosen to achieve the required level of attenuation over the stop-band. The cut-off frequency of low frequency stage is chosen to be lower than switching frequency to achieve enough noise attenuation at switching frequency. The multiple stop

bands from the different filter stages merge into each other to provide continuous noise attenuation from the first cut off frequency, shown in **Figure 4-2**.

For this purpose, the primary stage filter inductors are of the order of 100µH to limit the current ripple to acceptable levels and the filter capacitors are of the order of 1µF to achieve a cut-off frequency substantially below the switching frequency (e.g. cut-off of several kHz for switching at several 100s kHz). A second filter stage consists of ~10µH inductor and ~0.1µF capacitor to achieve broad-band noise attenuation. Two or more stop bands from different filter stages merge into each other to provide continued noise attenuation from the first cut off frequency.

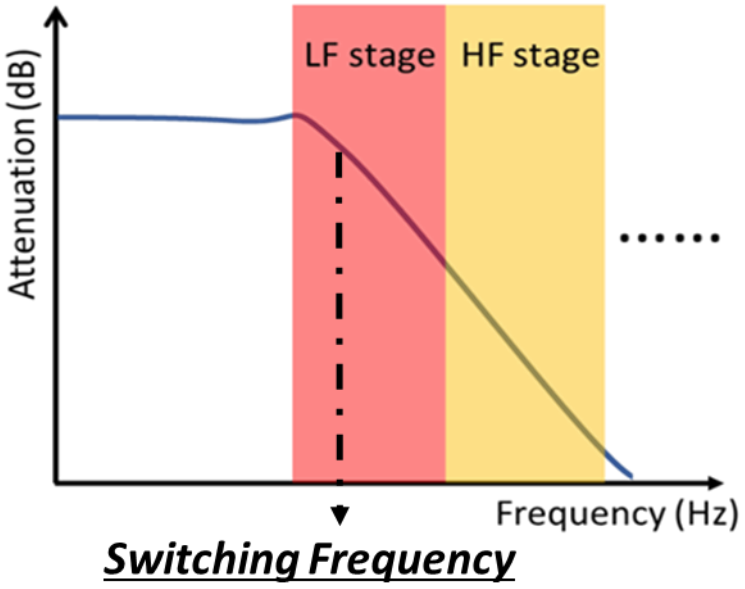


Figure 4-2 Noise attenuation with multi-stage filters

The 100µH inductor used in this study is AGP4233-104ME, provide by Coilcraft®, shown in **Figure 4-3**. Core material is ferrite and ambient temperature is -40 °C to +125°C with max Irms=34A. This type of inductor is features shield tabs which provides some level of shielding of the emitted electromagenetic field. The film capacitor used for 1uF capacitance is B32672P5105K000, provided by EPCOS®, which has maximum operating

temperature of 125 °C and voltage capability of 520 V Vdc. This type of capacitor features very compact design and short leads, which can contribute to low self parasitic inductance, hence high self resonant frequency and high level of nosie attenaution at high frequency.

A vector network analyser (VNA) E5080A and impedance analyser (IA) KEYSIGHT E4990A were used to measure s-parameters and to investigate the parasitic effects from the inductors and capacitors on filtering performance. Measurement range is from 10kHz to 100MHz. voltage insertion gain measurement result from vector network analyser and impedance measurement result from impedance analyser are shown in **Figure 4-4**. The frequency of resonant valley in the voltage insertion gain agrees with that of resonant peak in impedance level, which is about 5.59MHz. After the self-resonant frequency, this 100μH inductor behaves more like a capacitor due to the EPC effect, impdeance value derease significantly.

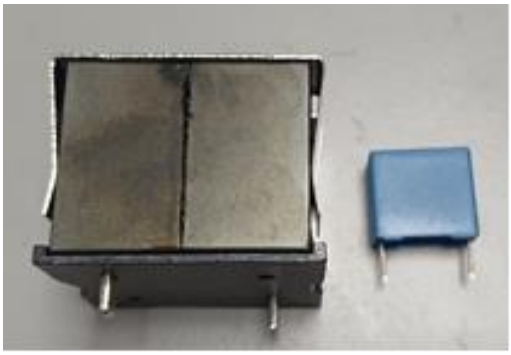


Figure 4-3 Inductor and capacitor used in this research (Left)

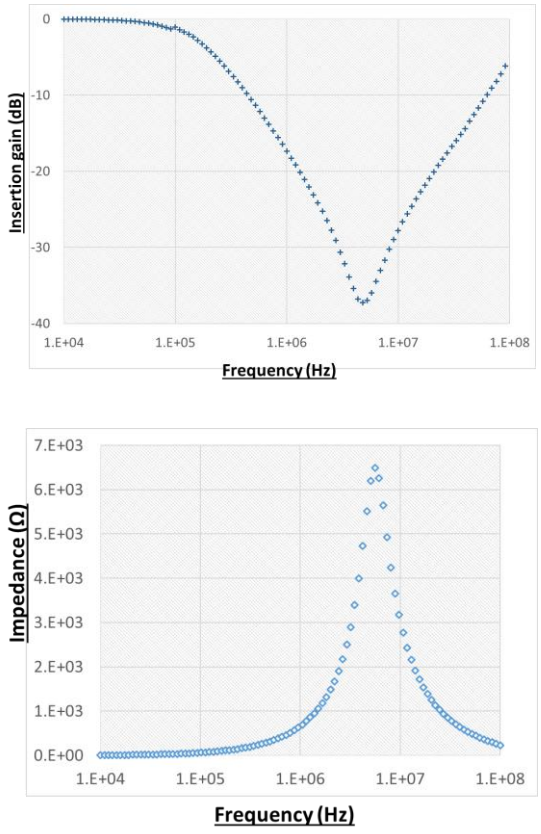


Figure 4-4 voltage insertion gain (top) and impedance level (bottom) of 100μH inductor

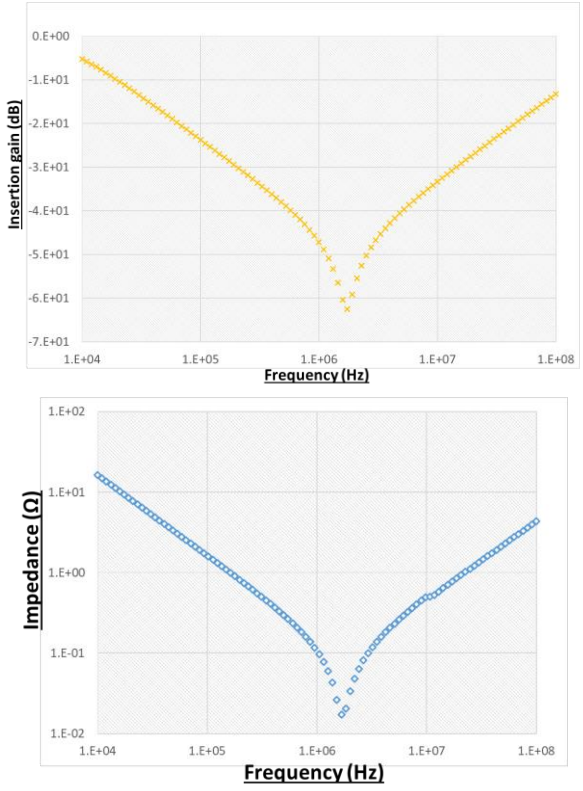


Figure 4-5 voltage insertion gain (top) and impedance level (bottom) of 1uF capacitor

Figure 4-5 shows the voltage insertion gain and impedance level against frequency of the 1μF capacitor. Its self-resonant freqeuncy is about 1.67MHz and beyond this the capacitor behaves more like an inductor due to ESL, as illustratead by the increasing impedance. From the previous measurement from impedance analyser and network analyser, value and parasitic elements of inductor and capacitor are summarized in **Table 4-1**

100μH Inductor	1μF Capacitor
L =100.68μH at 1kHz	C=975.69nF at 1kHz
EPR=6.48kohm	ESR=17.43mohm
EPC=8.02pF	ESL=9.31nH

Table 4-1 Measured value and parasitics of 100uH and 1uF

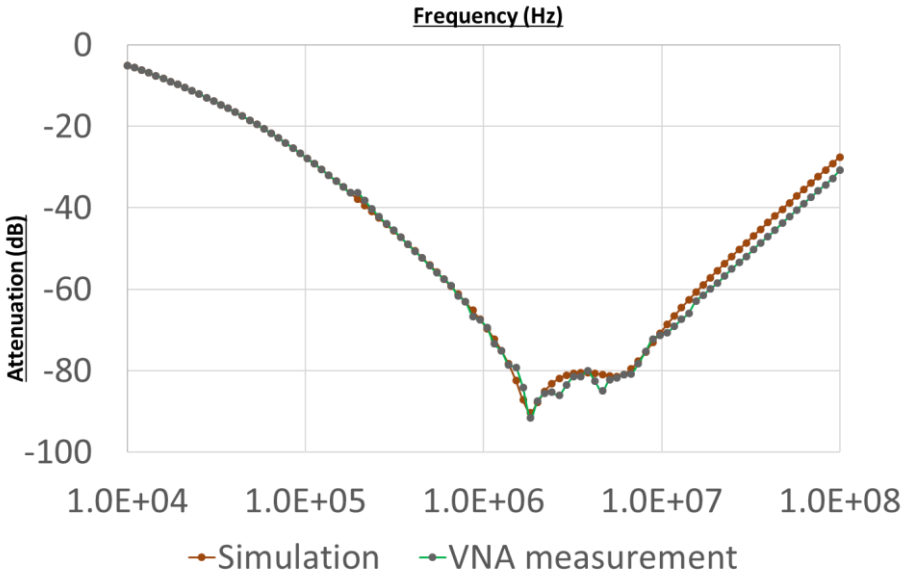


Figure 4-6 Simulation and measurement results of first stage

The measurement and simulation include the 50 ohm source impedance of the VNA. Measurement and simulation results of the combined noise attenuation of the first stage L-C filter are shown in **Figure 4-6**. The simulation result aligns with measurement result

very well. A noise attenuation of -40dB/dec continues from low frequency 10kHz to the first self-resonance frequency, caused by ESL and capacitor, followed by the second resonance, caused by EPC and inductor. The stop band of the LC low pass filter remains below -70dB from 1MHz to 10MHz. Noise attenuation at high frequency typically weakens due to non-ideal components and unintended interstage coupling. Simple models with ESL and EPC factors can well represent and describe filters at low frequency, but some deviation is expected at high frequency due to the simplified lumped parameter models considered in this research. For higher accuracy of simulation at high frequency, a distributed model should be used. Also, the cut off frequency and noise attenuation at low frequency can be modified by selecting different values of inductance and capacitance for the filter components. However, the bigger the values, the greater the parasitic components ESL and EPC are associated with capacitor and inductor, and the greater the electromagnetic field coupling between each component. This will in turn tend to deteriorate the high frequency performance. Careful layout for filter stages and parasitic cancellation arrangements may improve this situation as described below.

4.2.2 Self-parasitic elements cancellation techniques

As discussed above, the filter self-parasitics are very critical to filtering performance especially in the high frequency range. Equivalent Series Inductance (ESL), which is from the capacitors leads and internal current distribution path, defines its noise shunting performance at high frequencies. Similarly, for inductors the high frequency performance is limited by the Equivalent Parallel Capacitance (EPC), which arises from the electric field distribution between the winding turns and between the windings and the core. Apart from using low ESL surface mount ceramic capacitor or low EPC inductor to improve filtering performance at high frequency, parasitics cancellation techniques are an

alternative option to improve noise attenuation capability. In this section, self-parasitic elements cancellation techniques and its validation are discussed.

The principle of ESL cancellation techniques is to create an inductance which is equal to and has negative polarity of the ESL in the capacitor. This can be carried out based on the use of coupled magnetic windings to cancel the parasitic inductance in discrete capacitors [5] or by using a PCB layout design which is optimised to cancel the ESL of two capacitors in parallel connection [6]. In this research, we applied ESL cancellation by creating additional inductance that has negative magnetic coupling with ESL. This can be achieved by primary and secondary winding connected to the capacitor lead shown in **Figure 4-7**. In the T circuit, two windings L_1, L_2 have the opposite polarity and the equivalent mutual inductance M_{12} can cancel the ESL in capacitor. For the network on the left in **Figure 4-7**, the relationship between the input port (Left) output port (right) voltages and currents can be written as

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = s * \begin{pmatrix} L_1 & M_{12} \\ M_{12} & L_2 \end{pmatrix} * \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} + Z_c * \begin{pmatrix} I_1 + I_2 \\ I_1 + I_2 \end{pmatrix} \quad (55)$$

Z_c is the impedance of capacitor. It is the summation of ESL, ESR and C.

Using the T-equivalent circuit for a pair of coupled coils, the network can also be represented as shown on the right in **Figure 4-7**:

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = s * \begin{pmatrix} L_1 + M_{12} & 0 \\ 0 & L_2 + M_{12} \end{pmatrix} * \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} + (Z_c - s * M_{12}) * \begin{pmatrix} I_1 + I_2 \\ I_1 + I_2 \end{pmatrix} \quad (56)$$

Comparing these two networks, the impedance Z_c in the first network is replaced by the equivalent $Z_c - s * M_{12}$. From this comparison, ESL can be cancelled. The most effective cancellation is achieved when the additional mutual inductance is completely equal to the expected capacitor ESL.

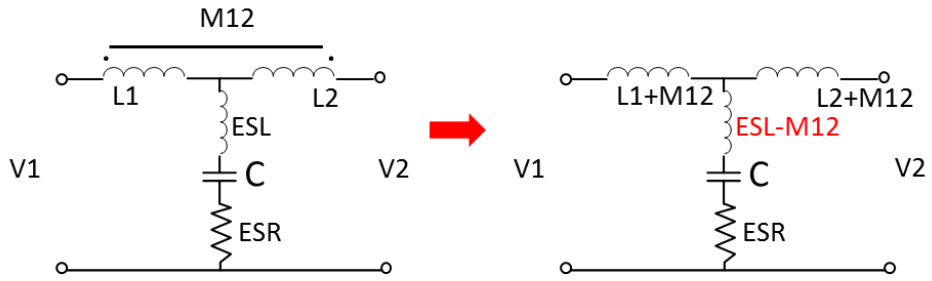


Figure 4-7 Equivalent circuit model of ESL cancellation

Figure 4-8 illustrates the design and implementation of two-coil layer structure of the cancellation windings. The winding is constructed out of a 0.78mm diameter common copper coil, which can be adjusted according to the current rating. The width of the winding is designed as 10mm to comply with the film capacitor used for filters. For different types of capacitors, the winding widths are modified optimally according to the calculated mutual inductance and the resulted rectangular winding cross window area. The mutual inductance M_{12} of the two single turn coils is approximated by

$$L = \frac{\mu_0}{2\pi} * \left[2x * In\left(\frac{2x + 2ac}{2x + 2bz}\right) + 2y * In\left(\frac{2y + 2ac}{2y + 2bz}\right) - 4(a - b + c - z)\right] \quad (57)$$

$$a = \sqrt{x^2 + z^2} \quad (58)$$

$$b = \sqrt{x^2 + y^2 + z^2} \quad (59)$$

$$c = \sqrt{y^2 + z^2} \quad (60)$$

μ_0 is air permeability, z is distance between the two coils for ESL cancellation, and x and y are width and height of the coil window respectively, shown in **Figure 4-8**. Two coils are assumed to have the same height and width. Accuracy of the calculation is also

determined by the magnetic field coupling coefficient between the primary and secondary coils.

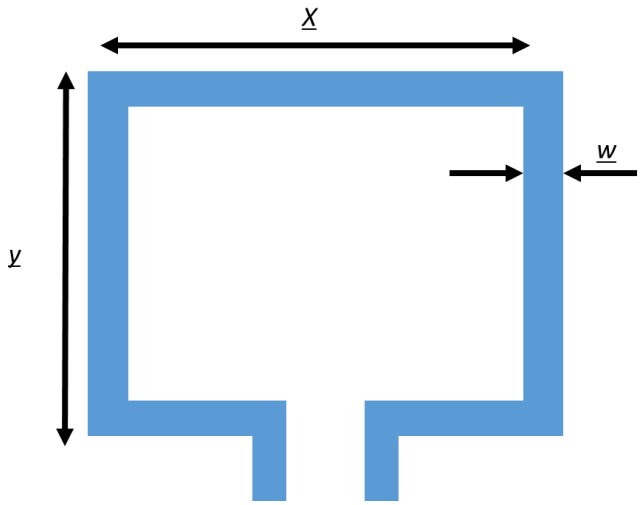


Figure 4-8 ESL cancelling coil design

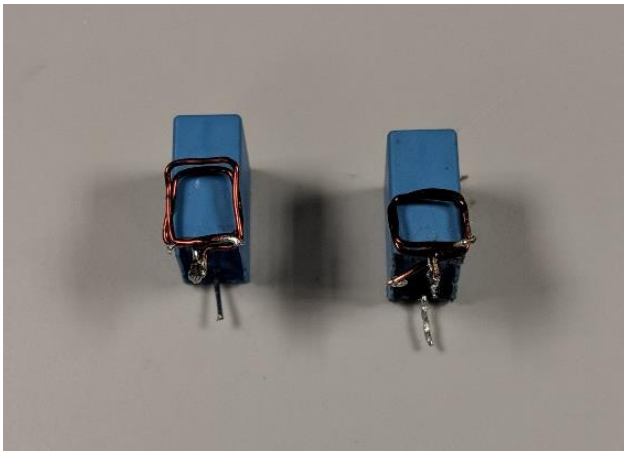


Figure 4-9 Different ESL cancelling coil design and integration with 1uF capacitor

A 1uF capacitor was used as an example to investigate the effectiveness of ESL cancellation, which has about 9.81nH measured from impedance. ESL cancellation coil is made out of coated copper wire with diameter of 0.78mm with about 10mm width and 10mm height on the left side in **Figure 4-9**, and another pair of coils have 10mm width and 6.5mm height on the right. At each ESL cancellation arrangement, two coils are aligned to each other, having the largest coupling area and the direction of negative magnetic coupling. One common lead from both coils is electrically connected with one

lead of capacitor, leaving another lead of the coils to become input and output ports of the network and its equivalent circuit shown in **Figure 4-7**.

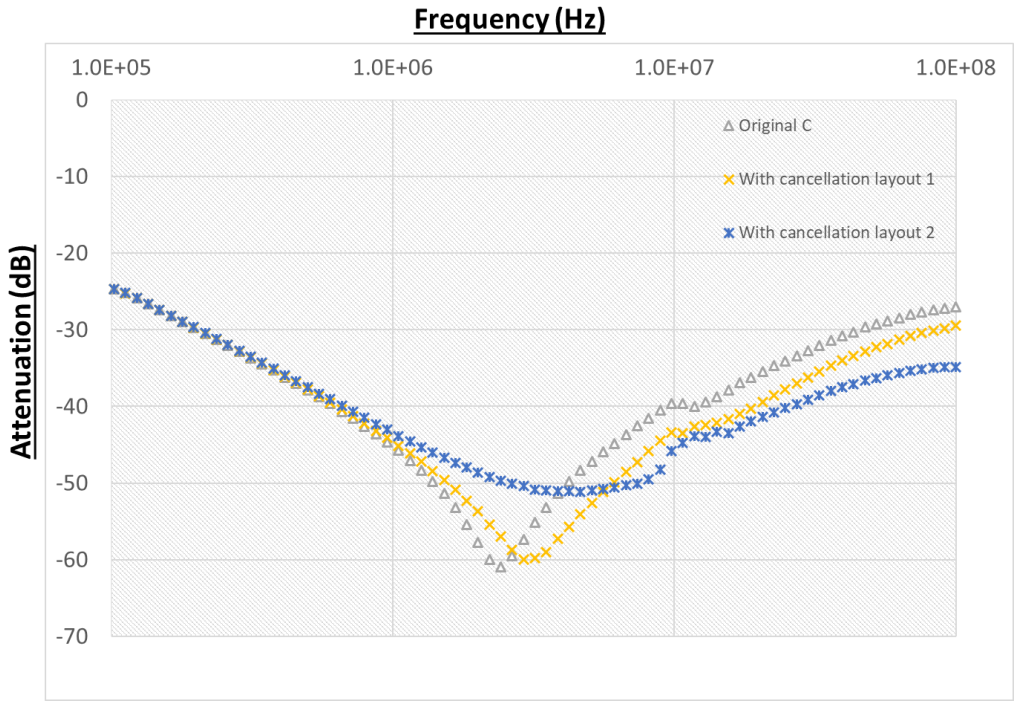


Figure 4-10 comparison of measured noise attenuation with different integrated cancellation windings

Figure 4-10 shows measured noise attenuation with different ESL cancellation arrangements. The grey line shows the voltage insertion gain of 1uF capacitor without any ESL cancellation, yellow line is that with 5.3nH ESL cancellation and blue line is that of with 9nH ESL cancellation. With increase of ESL cancellation, self-resonant frequency has moved to a higher frequency range, which mean the ESL cancellation is in effect. Integrated cancellation windings can provide an additional 10dB attenuation in the high frequency range. ESL cancellation value should not exceed the ESL of capacitor, otherwise it would give negative impact on noise attenuation.

On the other hand, parasitic capacitance (EPC) cancellation techniques are generally applied to cancel EPC of a wound inductor. Two additional capacitors are used to cancel the EPC of inductors based on the theory of balanced condition in the Wheatstone Bridge.

As discussed in paper[146], in order to achieve EPC cancellation layout, two paralleled inductor L1 and L2 are needed, which can be the differential mode filter or common mode filter. Two additional capacitors C1 and C2 are paralleled with L1 and L2 across the inductor`s two ends. Most EPC cancellation arrangement needs two or more inductors to be parallel to achieve an equivalent Wheatstone network for the EPC cancellation. This type of cancellation needs additional capacitors and make cancellation arrangement more complicated. However, ESL cancellation on capacitor is more simple and practical, which is easily realized through a couple of thin wire positioned in a T network and negative magnetic coupling to reduce ESL.

4.2.3 Mutual-parasitic elements cancellation

Mutual coupling, including inductive and capacitive coupling, occurs between nearby filter components. It appears as additional parasitic components in or between the filter components. Mutual coupling becomes more dominant than self-parasitics in high frequency range due to parasitic electromagnetic field couplings especially in high density power electronic system where component spacing are small. Among these couplings, inductive couplings are more critical. Previous papers [93][147] reveal that reduced mutual coupling can be realized by carefully orientating the filter components to reduce mutual coupling, for example orthogonal orientation of inductor windings. As an alternative, a cancellation inductor is integrated with the capacitor to cancel the mutual coupling between two capacitors. Better filtering performance can also be achieved by shielding to decouple electromagnetic field linking [92], or by increasing the distance between components. However, this final approach may not be desirable as it will significantly increase the overall volume of the filter. In addition, since increased scale of filter layout would inevitably introduce more self-parasitic elements, which can decrease noise attenuation performance of filters. Therefore orientation of field coupling, shielding

and distance between elements are the key to decrease mutual coupling in [148] by E.Hoene et Al .

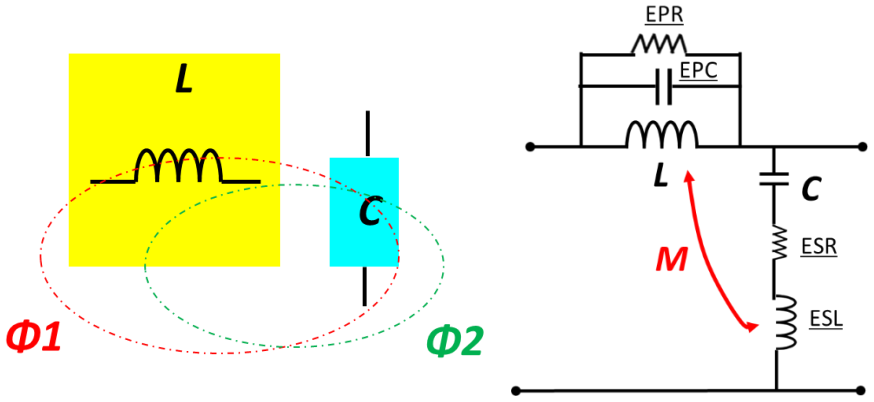


Figure 4-11 Mechanism of mutual coupling between inductor and capacitor

Considering the case of a L-C low pass filter configuration with 100uH capacitor and 1uF inductor, the mutual coupling between them can be described by **Figure 4-11**. Φ1 originates from inductor flux leakage. Using ferrite E core can confine most of magnetic flux within the core, however some flux may leak from the gap of parts of E core, and this leakage will couple with nearby filter components such as capacitor. On the other hand, the film capacitor is composed of thousands of displaced parallel metalized films and its internal equivalent current flowing path is formed from one tab/lead to the other one. These current loops causes Φ2 external magnetic flux and links with Φ1 becoming mutual coupling between inductor and capacitor. The equivalent circuit of this mutual magnetic coupling between inductor and capacitor is shown in **Figure 4-11**. The current flows in the inductor and generates magnetic flux which couples with the magnetic flux produced by the capacitor, giving rise to further unwanted parasitic effects in the filter. Similar to ESL cancellation technique, the mutual coupling M will be added into capacitor branch and this impact would alter the noise shunting performance of this capacitor. However, this coupling would not impact much on inductor`s performance, since the magnetic leakage M is considerably smaller than filter`s inductance. If the magnetic coupling M is positive between capacitor and inductor, it would hinder noise current shunting performance and

left shift self-resonant frequency. The resonant frequency f_1 of this capacitor branch is therefore lower than the original.

$$f_1 = \frac{1}{2\pi\sqrt{(ESL + M)} * C} \tag{61}$$

And the capacitor branch impedance of the positive coupling is

$$Z_1 = ESR + j * \left[\omega(ESL + M) - \frac{1}{\omega C}\right] \tag{62}$$

Oppositely, if the magnetic coupling is negative, it may work in favour to cancel out ESL, then the resonant frequency f_2 of the capacitor branch is higher than that of the capacitor, giving

$$f_2 = \frac{1}{2\pi\sqrt{(ESL - M) * C}} \tag{63}$$

And the capacitor branch impedance of negative coupling is:

$$Z_2 = ESR + j\left[\omega(ESL - M) - \frac{1}{\omega C}\right] \tag{64}$$

However, if negative coupling in bigger than ESL, a minimum impedance rather than resonance would appear at the frequency f_3 and no phase polarity change occurs.

$$f_3 = \frac{1}{2\pi\sqrt{(M - ESL) * C}} \tag{65}$$

And associated impedance Z_3 is

$$Z_3 = ESR + \frac{1 + \omega^2 C(M - ESL)}{j\omega C} \tag{66}$$

The second term is the function of frequency and Z_3 will increase again after the frequency f_3. After the frequency f_1, f_2 or f_3, the impedance of the capacitor branch becomes higher with frequency. Because a small impedance of capacitor branch benefits the filter performance, it would become worse after such frequencies. Thus, any mutual

couplings affecting the impedance of the capacitor branch would affect the performance of the filter.

In order to understand the magnetic flux linkage between inductor and capacitor and the impact of each layout with different flux linking on filtering performance, the following factors have been investigated. The factors include orientation of filter components, distance between them and shielding effect. Through the change of noise attenuation and the series resonant frequency, the impact of each factor can be observed. In the first case, the magnetic field coupling between inductor and capacitor with different layout and orientation is investigated. Shown in **Figure 4-12**.

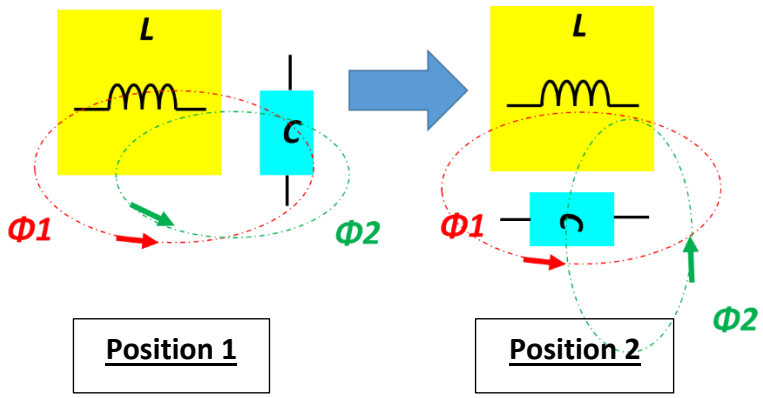


Figure 4-12 Magnetic field coupling between inductor and capacitor with different layout

In the first layout shown in **Figure 4-12** (left side), inductor and capacitor are positioned next to each other closely, and electrically connected to form a LC low pass filter. Capacitor current loop direction is perpendicular to inductor toroid direction. Magnetic flux Φ1 originated from inductor leakage flux is aligned with the magnetic flux Φ2 generated by the current loop flowing through capacitor, and these flux have a maximum coupling. In the second layout shown on the right side, capacitor is moved to the other side of inductor and keep the same distance from the inductor. However, since magnetic flux from inductor is paralleled with capacitor current loop, these magnetic fields are perpendicular to each other and the flux linking between Φ1 and Φ2 has the minimum

coupling. The noise attenuation level comparison of these different layout is shown in **Figure 4-13**

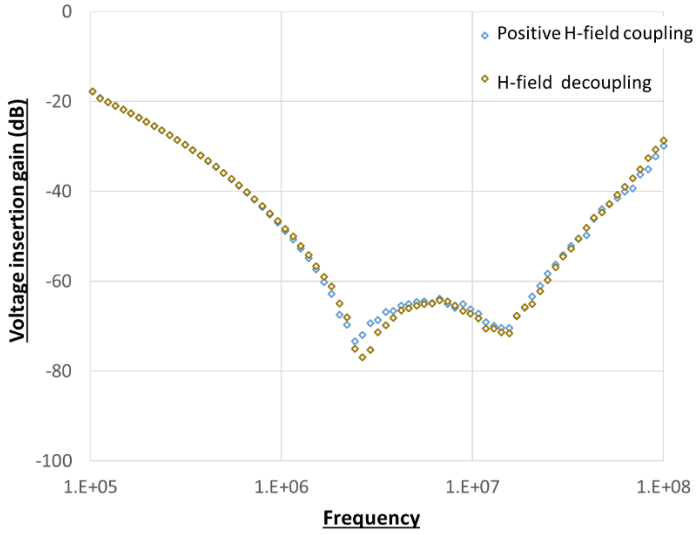


Figure 4-13 Voltage insertion gain between different layout of LC filter. Note yellow dot line is position 2 and blue line position 1 respectively shown in Figure 4-12

The blue dot line has the maximum magnetic field coupling between inductor and capacitor, where magnetic fluxes from inductor and capacitor are aligned. The orange dot line is the minimum magnetic field coupling where two magnetic fluxes are perpendicular to each other. The first frequency valley is due to self-resonant between ESL and the capacitor. Due to the positive coupling between these two magnetic flux Φ1 and Φ2, the additional mutual inductance M is added to ESL and alters voltage insertion gain and current shunting effect. The self-resonant frequency is pushed down to 2.42MHz from 2.65MHz and from this frequency shift mutual inductance can be calculated to be about 2.8nH, which is added to original 7.3nH ESL. This result shows that unintended magnetic field linkage from a bad EM design gives 30% additional parasitics ESL to capacitor, which would further deteriorate filtering performance. Apart from the self-resonant frequency valley, the voltage insertion gains of the two different layout remains identical. It reflects that this magnetic field coupling impact capacitor behaviour most and has much less

impact on inductor which at 100uH is comparably larger than several nH mutual inductance. Position 2 is used as the benchmark at all the following experiments to validate magnetic field coupling effect.

Next experiment is to vary the impact of changing distance between capacitor and inductor on magnetic field coupling, while keeping the relative orientation the same. The magnetic field strength and field linkage is generally inversely proportional to the distance. **Figure 4-14** shows the measurement results for different component separation distances. Blue dot line is the original distance, and the brown dot line is that capacitor is moved 10mm away from inductor, where it would have less magnetic field coupling. The result does not show much difference because of the fact that the capacitor is positioned at minimum magnetic field coupling with inductor and distance does not alter the capacitor behaviour very much. Increasing distance between interference and receiver to reduce unintended magnetic field linkage is not practical for high density power electronic system, also increased distance would add more parasitic inductance and would impact noise current shunting effect at its return path and worse overall filtering performance, which will be discussed in the next section. Another experiment is shielding effect on decoupling magnetic field linkage, where the capacitor was completely shielded to block off all magnetic field coupling from outside. The whole capacitor is covered by the thickness of 100um copper shield layer. The comparison of measurement results are shown in **Figure 4-15**. The yellow dot line is the original setup, and the blue line is the result of shielded capacitor.

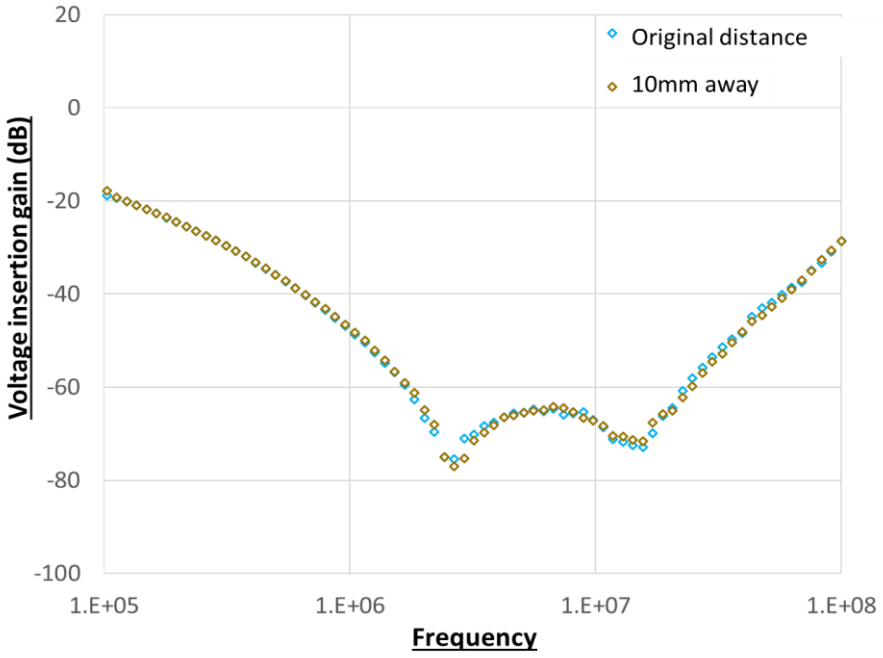


Figure 4-14 Noise attenuation comparison between different distances

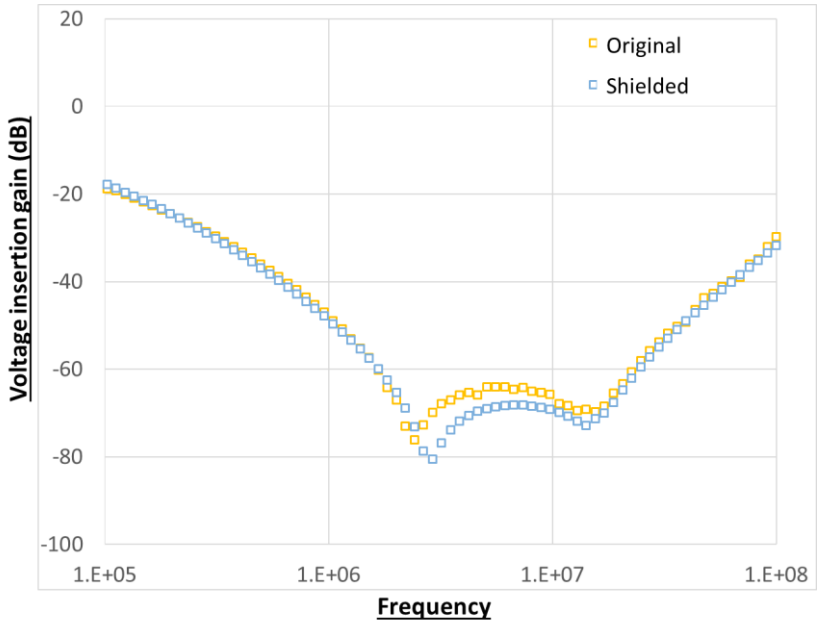


Figure 4-15 Noise attenuation comparison between shielded and no shielded capacitor

Due to shielding arrangement on capacitor, the first frequency response valley is pushed to a higher frequency from 2.65MHz to 2.91MHz and the noise attenuate is further improved by about -8dB right after then. ESL would be reduced by about 2.9nH,

calculated from the self-resonant frequency. 100um shield layer can both decouple magnetic field from inductor flux leakage and it can also cancel some level of ESL by generating counteracting magnetic field, because current loop within the capacitor induces eddy currents within the shield layer. Therefore shield layer works in favour of enhancing noise attenuation by reducing ESL of capacitor and would add parasitic capacitance paralleled across the capacitor. However, adding shield layer to inductor would give negative effect on filtering performance by introducing more parasitic coupling between input and output, which has equivalent effect of adding EPC to the inductor. This effect is also discussed in the next section.

Together, these results illustrate the mutual magnetic field coupling between filtering components and impact of factors including orientation, distance and shielding arrangement on filtering performance. Better noise attenuation of filters can be achieved through proper electromagnetic field design and filter component placement.

4.2.4 Cascading multi-stage filters and noise current return path

Based on the previous magnetic field decoupling techniques, multi-stage filtering arrangement was employed to realize a broad stop band filter for noise suppression. The proposed broad band filter consists of a cascaded series of low-pass filters whose configuration and cut-off frequency is chosen to achieve significant attenuation of switching harmonics. Upon this aim, the primary stage is for low frequency noise attenuation and secondary stage and above are for high frequency noise attenuation. The primary stage filter inductors are of the order of 100µH to limit the current ripple to acceptable levels and the filter capacitors are of the order of 1µF to achieve a cut-off frequency substantially below the switching frequency (e.g. cut-off of several kHz for switching at several 100s kHz). A second filter stage consists of 10µH inductor and 0.1µF capacitor to achieve broad-band noise attenuation. A third filter stage consists of 1uH

inductor and 0.01uF capacitor, aiming to extend the stop band to much higher frequency range. As an example, merged multi-stage filtering configuration which can cover weakened attenuation and spread the stop-band from low frequency range to over 100MHz is shown in the simulation results **Figure 4-16**. In this simulation, all parasitic elements such as EPC, EPR, ESL and ESR were included and they are extracted through the measurement results with impedance analyser. Also simulation adopts 50Ω input and output impedance as same arrangement as VNA measurement. The blue dot line is the first stage, a combination of 100uH inductor and 1uF capacitor. The orange line is the second stage filter, a combination of 10uH and 0.1uF, and the grey line is the third stage filter, a combination of 1uH and 0.01uF respectively. The first filter stage produces the noise attenuation -40dB/dec from the first stage cut-off frequency to the second stage cut-off frequency which is around 24 kHz. After then the second filter stage becomes in effect and produce further noise attenuation achieves -80dB/dec. The third filter stage takes over from the second stage at around 25MHz, where the second filter stage noise attenuation begins to reduce due to parasitics.

From the simulation results, it is clear that the cascaded three filter stages could achieve overall very good filtering performance, providing a high level of noise attention of over -100dB from 1MHz up to 85MHz. in addition, the resonant peak of the first filter stage is not visible due to overdamped pole of transfer function ($\zeta = \frac{1}{2} * R * \sqrt{\frac{C_1}{L_1}} = 2.5 \rightarrow Q = 0.4$), where R=50Ω, C1 is 1uF and L1 is 100uH. Conversely, the resonant peak of the second filter stage is visible due to underdamped pole $\zeta = \frac{1}{2} * \frac{1}{R} * \sqrt{\frac{L_2}{C_2}} = 0.1 \rightarrow Q = 10$, where R=50Ω, C2=0.1$\boldsymbol{\mu}$F, L2=10$\boldsymbol{\mu}$H

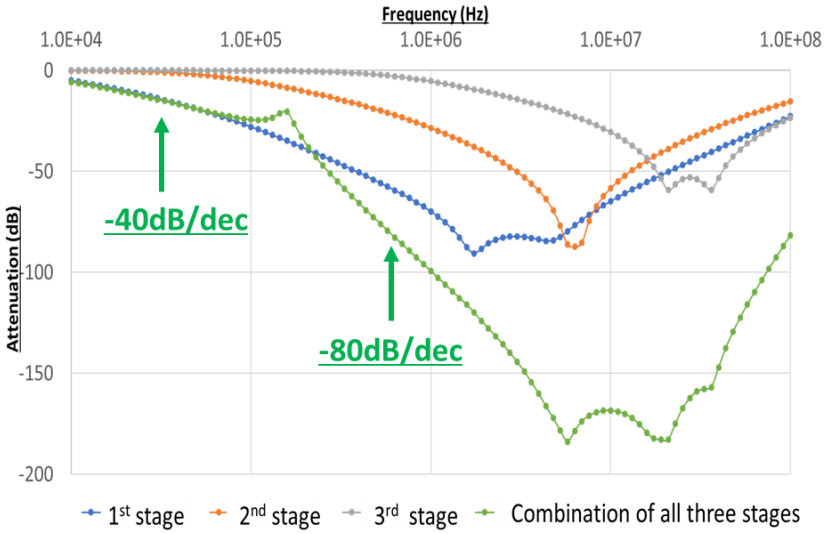


Figure 4-16 simulation results of noise attenuation for each stage and combination of all three stages

Therefore, in each filter stage, noise attenuation is degraded after the anti-resonant frequency due to parasitic elements (ESL, EPC). The next highest cut-off filter stage (higher frequency stage) needs to take over the attenuating role from the previous stage (lower frequency stage) to achieve the fastest roll-off rate and to yield an extended stop-band. **Figure 4-17** illustrates the impact of changing the cut-off (resonant) frequency of the high frequency stage relative to the anti-resonant frequency of the low frequency stage in a 2-stage low-pass filter. The blue line shows a case where the anti-resonant frequency of the LF stage is aligned with the resonant frequency of the HF stage. If the anti-resonant point of the LF filter stage is well below the cut-off point of the HF stage, the overall noise attenuation would get worse right after the first anti-resonant point (orange line in **Figure 4-17**). Conversely, if the HF cut-off is well below the LF anti-resonant frequency and very close to LF cut-off (green line in **Figure 4-17**), it could cause the faster and steep roll-off frequency response after HF cut-off, however, high value L and C result in high ESL and EPC involved, and HF noise attenuation becomes worse.

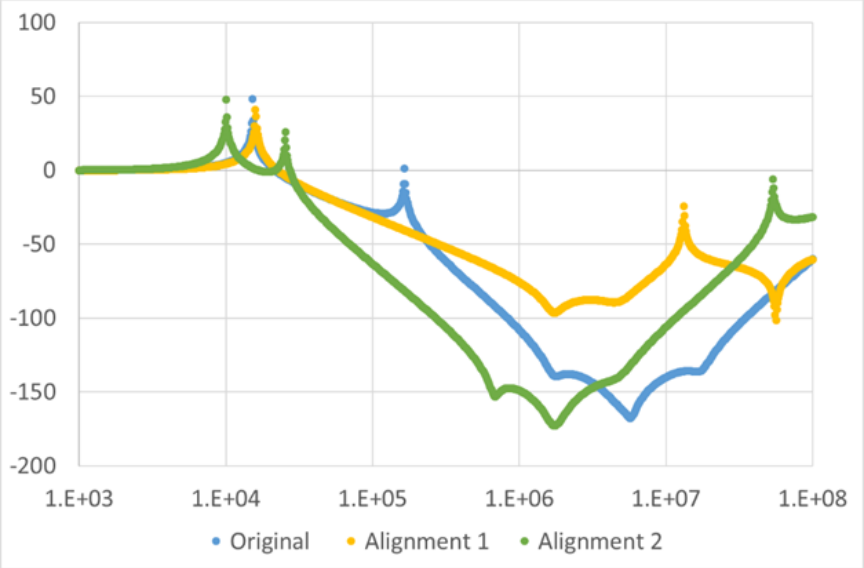


Figure 4-17 Simulation results of different cut-off frequency alignment

4.2.5 Cascaded filter layout optimisation

Besides the selection of cut-off frequencies and alignment of filter resonance/antiresonance, another importance factor is the presence of parasitic impedance in the current return path. Bad layout associated with unintended parasitics could hinder high level of noise attenuation for cascaded filter stages. Optimizing multi-stage filter to achieve reduced parasitics in the return path is investigated as follows.

A typical configuration for multistage filters is to position them in line and in this case it's important to take into consideration of presence of parasitic impedance in the high frequency noise current return path. In general, the greater the number of filter stages, the higher the parasitic impedance of the high frequency noise return path. Poor grounding and/or filter layout will inevitably result in greater parasitic impedance reducing the proportion of high frequency noise being shunted back to the source and increasing the proportion of noise propagating to the load.

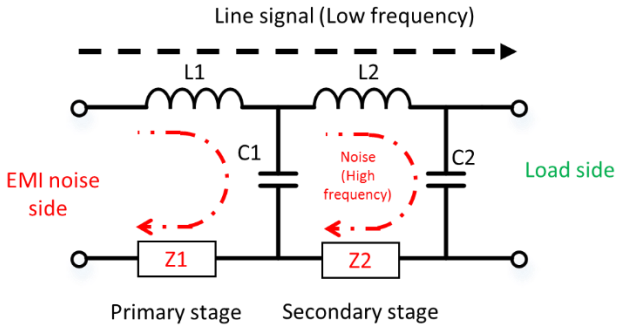


Figure 4-18 Schematic of first two filter stages

Figure 4-18 shows a schematic of a 2-stage filter in which L1, C1, L2 and C2 are the filter components of primary and secondary stages. Z1 and Z2 represent the parasitic impedance of the noise return path which is directly connected to the noise source (e.g. DC link). Inductors and capacitors L1 and C1; L1 and L2; L2 and C2 are positioned in the direction where the fluxes from inductor and capacitor are perpendicular so as to have low level of parasitic coupling between each other.

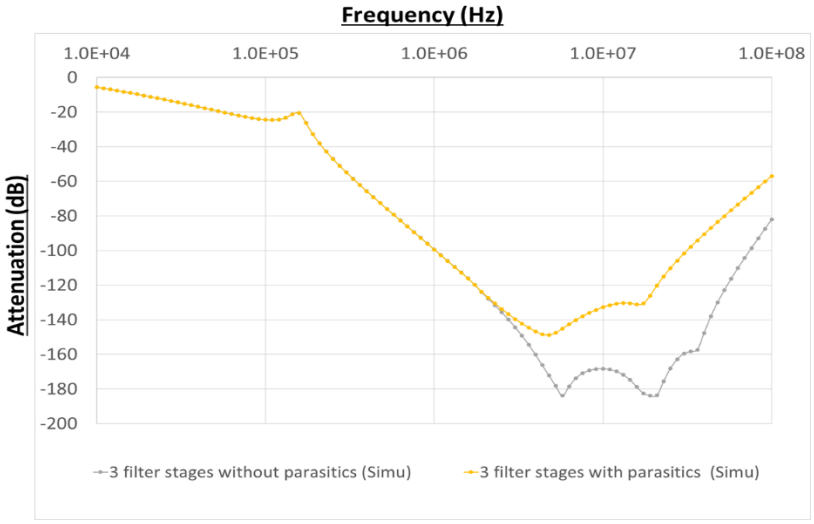


Figure 4-19 Pspice simulation results for a 3-stage filter with and without return-path parasitics.

Figure 4-19 shows PSpice simulation results of a case where 3nH parasitic inductance is inserted between the 1st, 2nd and 3rd filter stages to emulate presence of parasitics in the return path. Clear differences are visible in the simulated response with and without

return path parasitics at frequencies above 3MHz and are greater than 25dB between 10MHz and 100MHz. To illustrate this case in practice, 3-stage filters are positioned in line with same separation distance, and a 100um thin copper sheet is used as the ground path for noise current return. Its width and length is modified to fit with cascaded filter layout and its parasitic components are extracted by Maxwell Q3D to achieve about 3nH between each filter stage. Experimental results for the 3-stage filter are presented in **Figure 4-20** superimposed on the simulation results. There is good agreement between the experimental and the simulated results for the case with parasitic inductance in the return path above the noise floor, which is about -100dB. The results illustrate how even small levels of return path impedance can significantly compromise the high frequency performance of multi-stage filters.

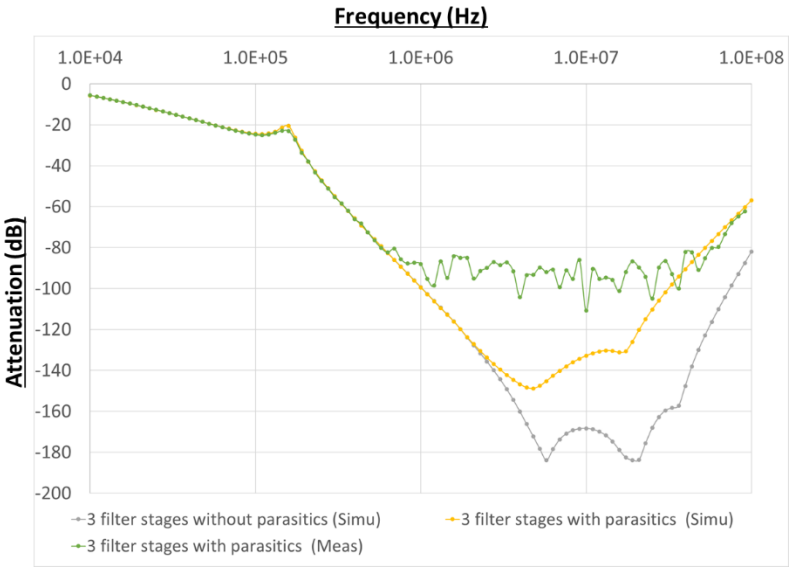


Figure 4-20 Comparison of measured and simulated results for a 3-stage filter. Note that the noise floor for the experimental results is around -90dB.

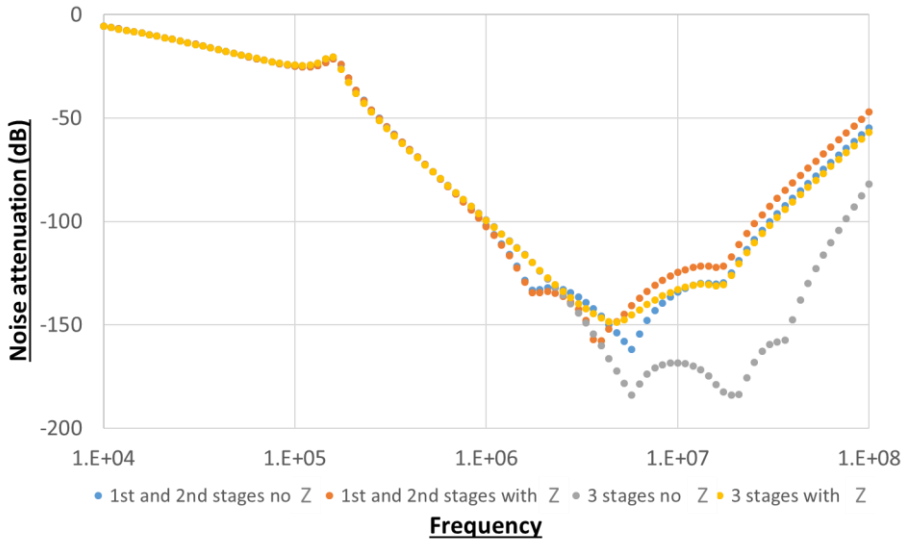


Figure 4-21 Comparison of simulation for 3-stage and 2-stage filter with and without parasitic impedance at return path

Furthermore, the impact of parasitic impedance at return path due to non-optimised layout on 3-stage filter is much bigger than that on 2-stage filter. The more filter stages, the more presence of parasitic impedance impacts on the current path. The return current from the last filter stage would encounter the highest parasitic impedance. In this case, noise current would be encouraged to flow to the load side instead of being returned to the noise source and the last filter stage would lose its noise attenuating function. **Figure 4-21** shows the simulation results comparing the noise attenuation between 2-and 3-stage filters with and without parasitic impedance. The grey dot line and yellow dot line are the same results from the previous simulation in **Figure 4-20**, and on the top of that, orange dot line representing 2-stage with Z and blue dot line representing 2-stage without Z are added. The differential noise attenuation of 3-stage filters w/wo parasitics is about 27dB at 100MHz and that of 2-stage filter w/wo parasitic is only 6dB. Furthermore, the result of 3-stage with parasitics is very close to that of 2-stage with or without parasitic. It reflects the parasitics in the return path can completely compromise the function of 3rd filter stage by preventing noise current from being circulating back due to a bad filter layout. Experimental measurements for the cases

above are shown in **Figure 4-22**. In addition to **Figure 4-21**, the blue dot line representing 2-stage filter layout agrees with the simulation result of 2-stage filter with parasitics at return path. There is only 7dB differential noise attenuation between the 2- and 3-stage filters, which compares poorly with the ideal case with no parasitics, where there is a difference of about 27dB. From this comparison, it is clear to see that presence of parasitic impedance in the return path can have a dramatic impact on noise attenuation. These results also illustrate that adding more filter stages would not necessarily improve noise attenuation.

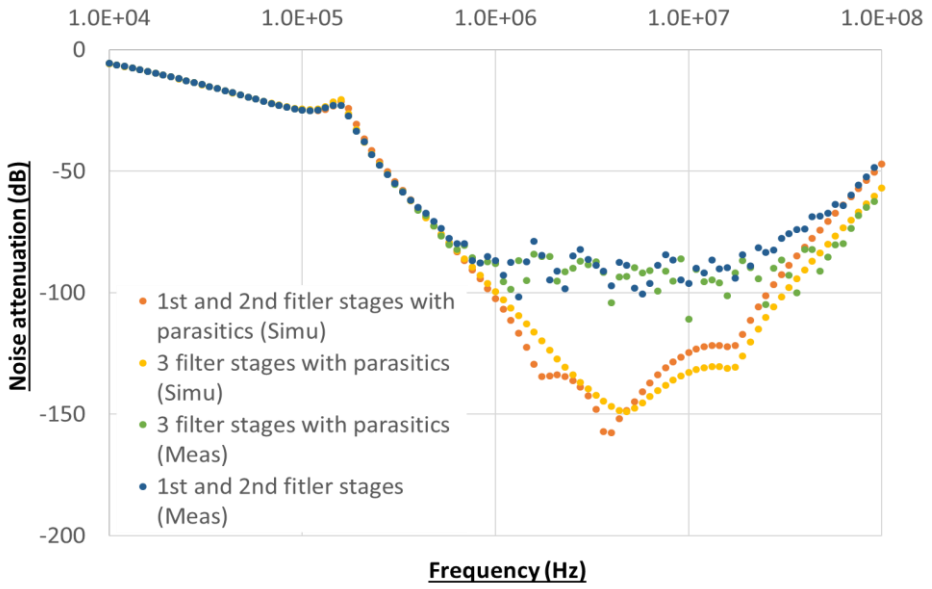


Figure 4-22 Comparison of simulation and measurement for 3-stage and 2-stage filter with parasitic impedance at return path

Therefore, improvement of filter layout has been investigated by to minimise parasitics in the noise current return path. Firstly, as shown in **Figure 4-23**, instead of positioning all filter stages in a line, which results in additional parasitic impedance, filters are arranged in a circular pattern to minimise the distance between all shunt capacitors and noise source and to achieve balanced parasitic impedance from all filter stages. In this case, the impedance from each shunt capacitor to the ground return point is well balanced and minimised. From the measurement results shown in **Figure 4-24**, filtering performance of

the new layout (dark green dot line) at a frequency of 100MHz is improved by 15dB. It indicates that a compact filter layout and minimised current return path can shunt high frequency noise current effectively and increase noise attenuation of cascaded filter stages.

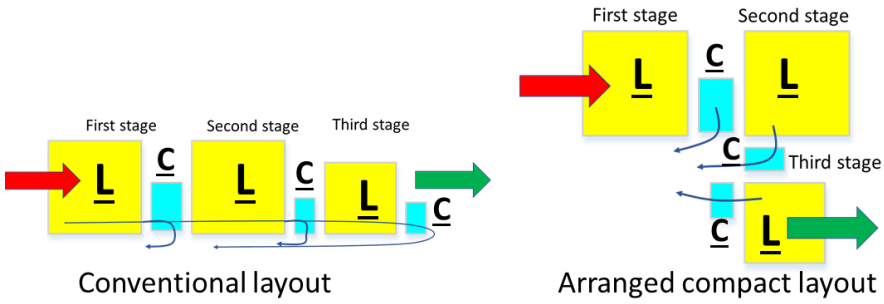


Figure 4-23 Alternative filter arrangements: left series string, right circular.

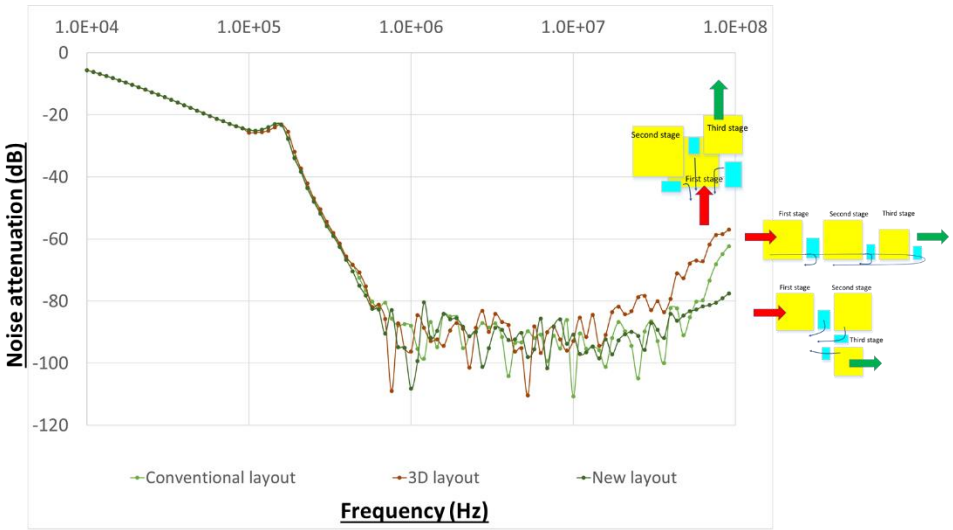


Figure 4-24 Comparison of cascaded filter response for three arrangements.

To further minimise the distance and parasitic inductance on the return path, a 3D layout has been investigated, where the first stage is positioned on one side of PCB and second and third stage filters are integrated on the other side of PCB, as shown in **Figure 4-24**. Dark red line is the 3D layout measurement result. However, this compact design does not realise further noise attenuation and noise attenuation capability is reduced after 50MHz compared with the results from previous two layouts. The filtering performance is even reduced by about 20dB at 100MHz. This result can be explained by the reduced

distance between input of 1st stage and output of 3rd stage filter which results in electromagnetic field coupling at high frequency, allowing noise current to be bypassed through the parasitic mutual couplings without being attenuated through the filter stages. This case can be improved if a whole metal shield layer is inserted between the top and bottom side of the PCB to reduce coupling. Thus, for low and mid-range noise attenuation, reducing parasitic inductance between each filter stage and the noise source is an effective way to improve filtering performance. However, for frequencies above 50MHz, self and mutual parasitics within and between the filter stages become dominant and it is very easy for noise to couple from the input of primary stage filter directly to load side without going through each filter stage. Here careful electromagnetic field decoupling and control are needed.

4.3 Shielding techniques: Containing EM noise

High frequency noise generates an extended electromagnetic field along the current path, an effect that is enhanced due to the skin effect which prevents the fields from propagating inside the conductors. When noise current flows through filter stages, the changing magnetic and electric fluxes can generate unintended coupling across relatively large distances, compromising filter performance and interfering with control circuitry. The electromagnetic interference coming from the switching cell, filters and output terminals must be suppressed and contained within an effective metal shield layer and this shielding and integrating filter stages concept is associated with the previous shielding and screening concept to achieve an overall EMI suppression solution. Therefore, after the discussion about element level characterization of filter components, mutual magnetic field coupling between filter stages and the optimization of filter layout, the next step is to discuss how to achieve a clean switching environment and mitigate both conducted and radiated EMI together.

However, when shield layers are applied to filter components, the contained electromagnetic field may alter filtering behaviour due to altered coupling characteristics and eddy currents induced in the shield itself. For example induced eddy currents can generate partial cancellation of the original magnetic field, leading to a reduction in the parasitic inductance. **Figure 4-25** shows the effect of a shield on the performance of a 1μF capacitor. With the shield, the resonant frequency shifts from 2.6637MHz to 3.203MHz. This shift indicates that parasitic inductance of the filter loop is reduced by eddy currents induced within copper shield layer, in this case from 7.55nH to 5.22nH. Meanwhile, the shielding structure may also affect the parasitic capacitance associated with the inductance. This trend can be verified from the measurement shown in **Figure 4-26**,

where resonant frequency shift, although very small, indicates an increase in parasitic capacitance from 4.76pF to 5.24pF.

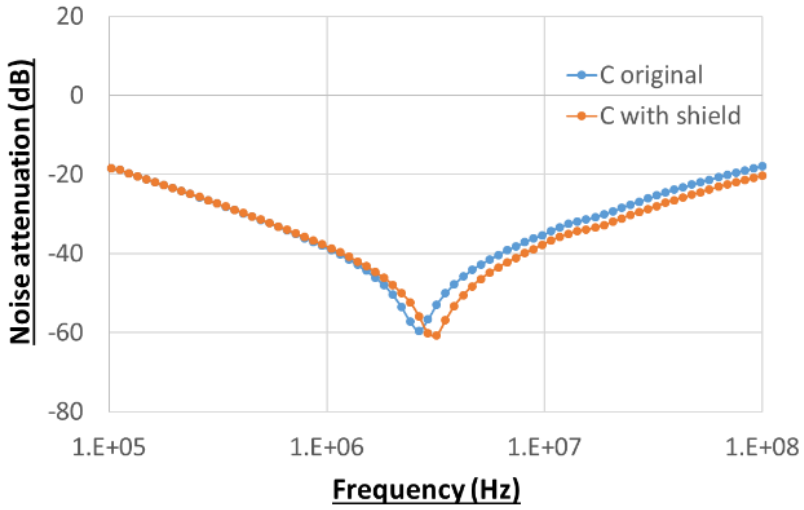


Figure 4-25 shielding effect on 1uF capacitor

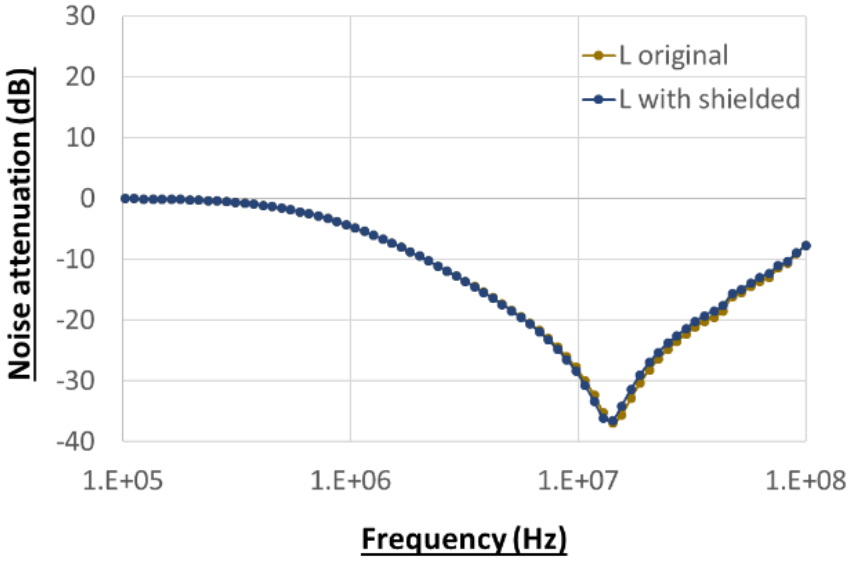


Figure 4-26 shielding effect on 100uH inductor

Electric flux that is coupled into the shield will generate currents that should be typically returned to the noise source (e.g. dc-link). If this current is not returned effectively, the shield itself will act as a radiator, coupling to the external environment (outside the

shield), to other parts of the filter (inside the shield) and to the input and output ports. To illustrate this matter, experimental measurements were made to compare the noise attenuation of a 2-stage filter with and without shield layer, where shield layer itself is electrically isolated from both the true ground and the noise source. **Figures 4-27** and **4-28** show the shielding arrangement outside of filter stages. The thickness of copper sheet layer is 100um. It is 5 times thickness of the skin depth of copper at 10MHz and is assumed to have enough attenuation on radiated high frequency noise. 1st stage and 2nd stage are positioned inside of the shield box and electrically isolated from the shield layer. VNA measurement ports are connected to the Input port and output of the filter stage via BNC coaxial cables which go through the shield layer. The openings/slots for passing BNC cables are kept as small as possible. The top cover of shield box is solder-jointed with the bottom part to achieve a complete and closed shielding configuration when measurement is conducted.

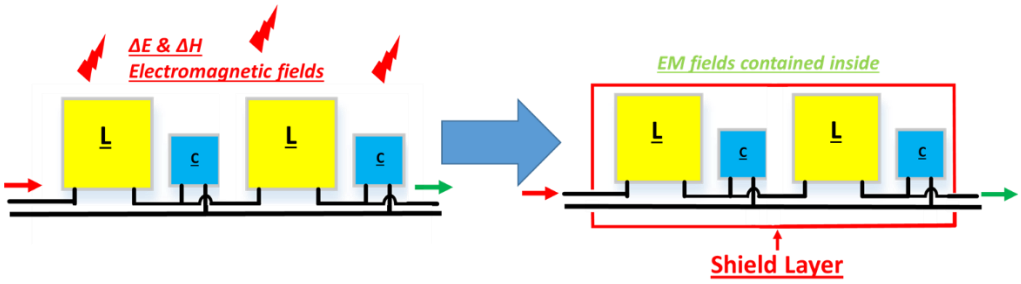


Figure 4-27 Schematic of two-stage filter with and without shield layer

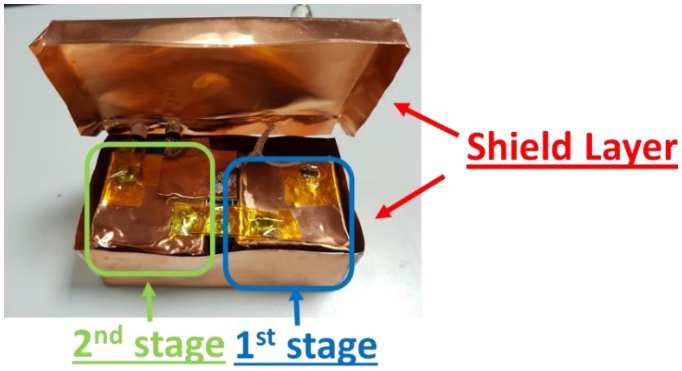


Figure 4-28 Practical shielding arrangement outside filter stages

Figure 4-29 compares the noise attenuation with and without shielding configuration, where shield layer is not grounded and completely floated from all potentials. The green dot line represents components only 2-stage filters and brown dot line represents the same filter configuration with closed shielding arrangement. It is notable that the shielded configuration results in diminished filter performance at frequencies above 10MHz. After then the differential noise attenuation becomes larger when the frequency goes up, reaching 26dB at 85MHz. As discussed above, a floating shield layer allows radiated noise to be reflected inside shield layer and coupled to load side, resulting in reduced attenuation. Changing electric flux which is coupled into the shield layer generates a noise current, and this noise current tends to find a lower impedance path to flow to the ground. Some noise current would couple to the load through parasitic capacitive coupling within the shielding containment or directly couple to the ground through the shield layer, when the shield layer is not grounded.

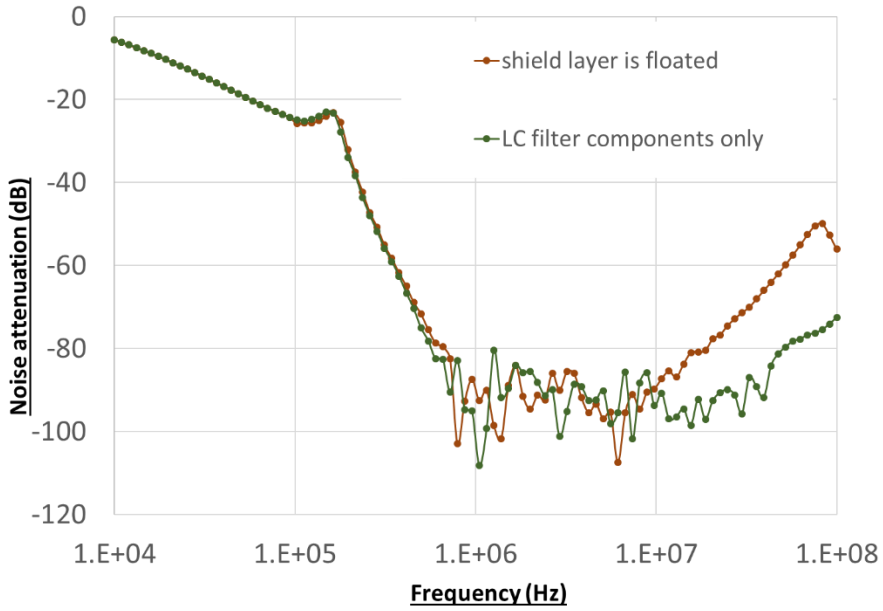


Figure 4-29 Effect of different grounding conditions on filter response

This experiment results is analogous to the shielding and screening arrangement described in chapter 2, and in both cases, the conductive shield layer must be grounded

and the connection impedance between this shield layer and the noise source must be kept to a low level to ensure noise current could be returned rather than being coupling to the ground. When taking the connection of shield layer around filters to the return point which is the ground of VNA analyser in this setup, a totally different noise attenuation outcome is observed, as shown in the comparison results of **Figure 4-30**.

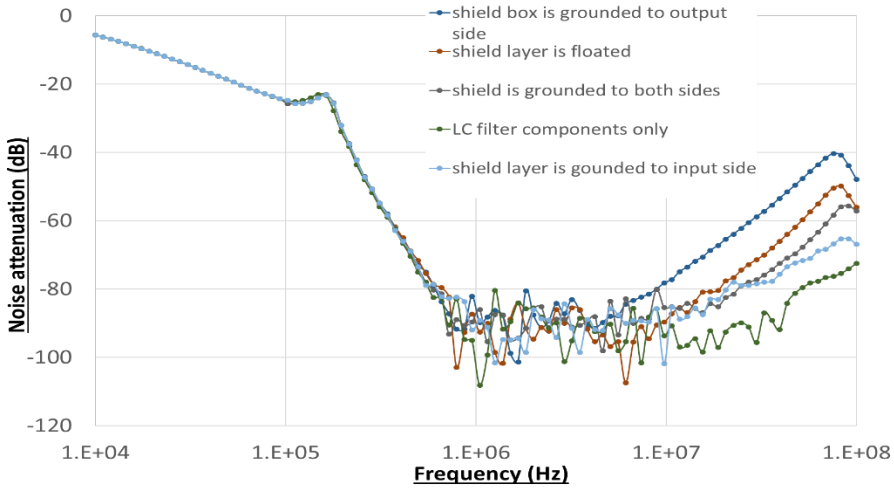


Figure 4-30 Effect of different grounding conditions on filter response

For these shielded cases, the filter current return path to the noise source is made separately from the shield connection. Current induced in the shield layer flows to the point(s) of ground connection. It includes the output and input port of VNA analyser. In addition to the previous results, three new measurement results are added to the comparison. They are the cases of the shield connected solely to the input (Light blue, **Figure 4-31**) or output port (Blue line), and the shield connected to both ports at the same time (Dark green line). It is notable that the worst case is when the shield is connected solely to the output port and the noise reducing performance is even worse than that of shield-floated case. The best performance is achieved when the shield is connected solely to the input port (noise source) and under this condition the performance is similar to the un-shielded case. With the same shielding arrangement, only different grounding scheme can generate up to 40dB differential noise attenuation. The performance of connecting

shield layer to both input and output is between the previous two cases. From this comparison of the noise attenuation with different shield-layer grounding conditions and with the case of no shield, it is clear that grounding shield layer and grounding point close to the noise source side would intentionally create low impedance for the coupled shield current and reduce the chance of noise coupling to the external through parasitic capacitive coupling . And it also encourage shield noise current to be returned to the noise source and reduce fraction of the shield return current diverted to the output port rather than the noise source. Nevertheless, all of the shielded configurations result in reduced filter performance compared to the unshielded case at the frequency above 10MHz and these results are expected to become worse at much higher frequencies, due to increased parasitic impedance and due to increased mutual coupling either between the filter stages or to the output port. By these two mechanisms noise coupled into a shield can degrade filter performance, and this is a side product of using a shield layer to contain all electromagnetic fields inside the switching cell.

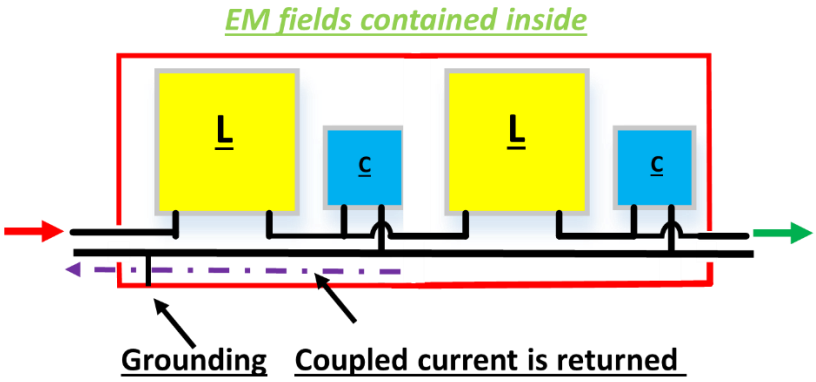


Figure 4-31 schematic diagram of grounding shield layer at input port

Improved method of creating a lower parasitic impedance in the return path to the noise source is to utilise the shield layer itself as the return path instead of using a separate return path connected to the shield layer. In this case, noise current flows at the inside of shield layer and the extended surface area of the shield layer can minimise the parasitic

impedance for the return path. In addition, using the shield as the only return path avoids the possibility of mutual coupling between a separate return path and the shield.

In the practical arrangement, the separate current return path is replaced by the bottom side of shield layer. One lead of shunt capacitor is directly connected to the inside of shield layer by soldering process. The diagram of this arrangement and actual layout are shown in **Figure 4-32.** The measurement comparison is shown in **Figure 4-33**, where the yellow dot line represents the improved return path. The noise attenuation of it has been further improved from the previous results by about 10dB, which is very close to the filter component only arrangement. Due to the lower parasitic impedance at current path while utilising the extended internal shield layer as return path, more noise current would be encouraged to shunt to the noise source and less noise current could couple to the load side.

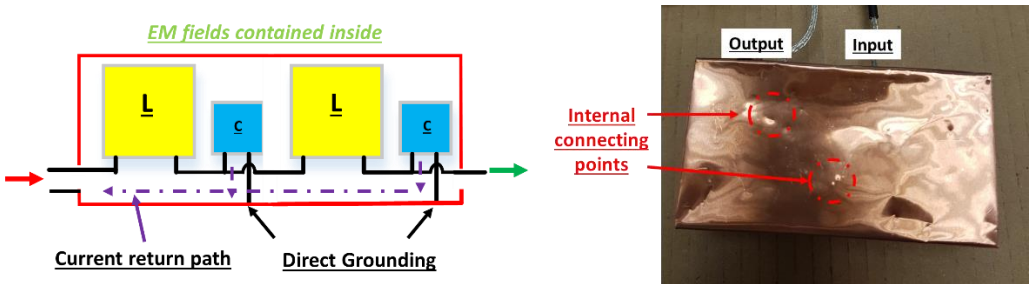


Figure 4-32 Schematic diagram of using shield layer as the current return path (Left) Top view of fully shielded filter stage and two internal connecting points of shunt capacitor

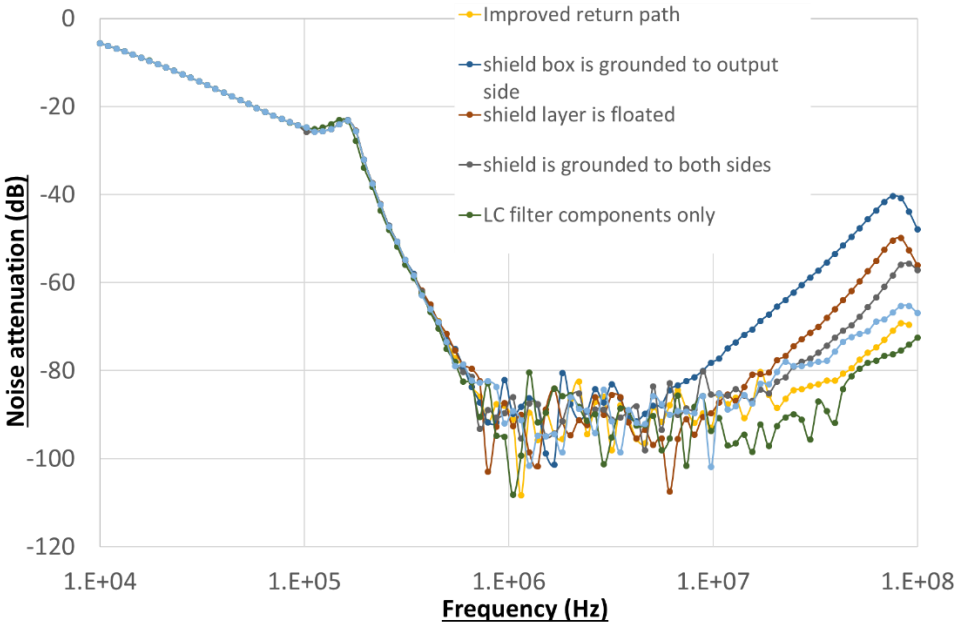


Figure 4-33 Noise attenuation of the improved current return path

4.4 Partitioning techniques: Decoupling EM noise

High frequency noise generates an extended electromagnetic field along the current path, with EM fields propagating outside the conductors, a feature that becomes more severe at high frequencies by the skin effect. The changing magnetic and electric fluxes from different conducting paths will interact and can generate unintended (parasitic) coupling over relatively large distances. This can compromise filter performance and cause interference e.g. with sensitive measurement and control circuitry. Thus for HF noise, it is typical to find a relatively low-impedance, parasitic path coupling the source to the load. Specific mechanisms are needed to block the HF noise and return it to the source. The forward path for EM waves thus needs to be suppressed whilst the reverse (reflected) path needs to have a very low impedance. Providing a low parasitic impedance in the return path by using the shield layer and connecting the shield layer to the noise source is an effective method of shunting noise back to the source. However, the filter stages can still be coupled by stray electromagnetic fields inside the shield, so an effective means of blocking these fields is needed. As a typical solution, a conductive mesh or shield layer is inserted between each filter stage to reduce EM field coupling, as shown in **Figure 4-34**.

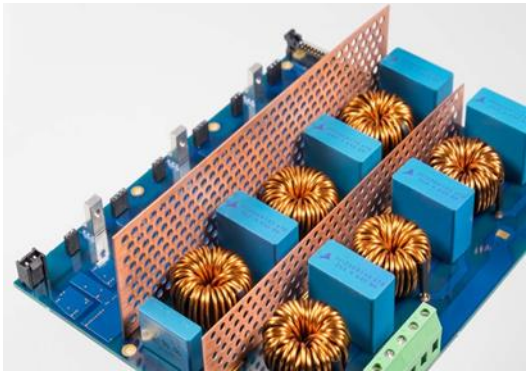


Figure 4-34 conventional EM fielding configuration

Because the shield layer has a semi-open arrangement rather than being closed like a Faraday cage, parasitics still exist between each filter stage and between source and load.

At high frequencies, leaking electric and magnetic fields from the source can easily couple to the load without being properly attenuated.

To overcome the limitations of semi-closed shielding, separate closed volumes with continuous conducting partitions may be used to shield each stage and return the filtered noise current, as shown in **Figure 4-35** and **4-36**. Note that by using the shield layer within each closed volume to return the filter current, HF noise can be more easily confined within each partition thereby reducing coupling to subsequent stages and the load. Therefore, noise from the source cannot easily couple to the load because they are separated by a number of closed, separately shielded regions. In addition, any component of noise current that is coupled from one partitioned region into the next will be preferentially returned back to the source rather than being propagated to the load.

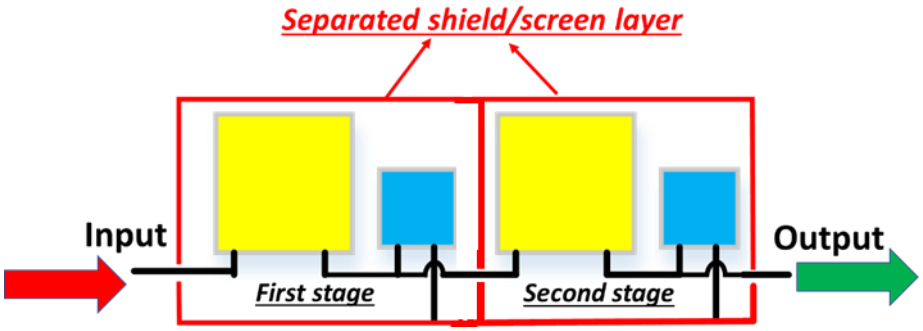


Figure 4-35 Schematic of complete closed partitioning arrangement.

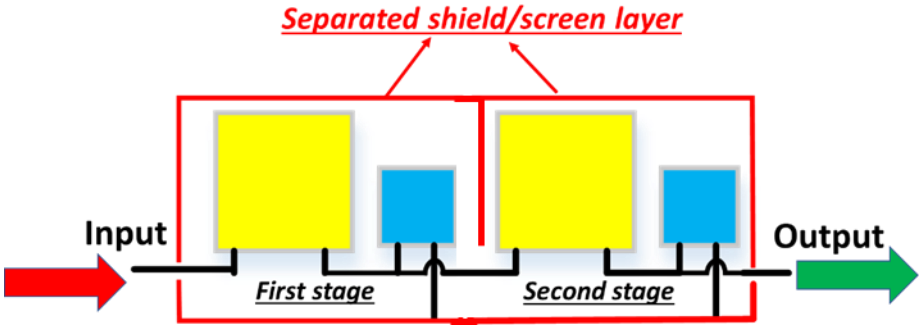


Figure 4-36 Schematic of partially partitioned arrangement

To illustrate the effects of different partitioning arrangements, s-parameter measurements were made on a 2-stage low pass filter using a Vector Network Analyser (Keysight model E5080A). **Figure 4-37** compares the forward transfer gains of a non-partitioned arrangement, a partially partitioned arrangement and a completely closed partitioned arrangement. It is clear that partitioned arrangements can achieve greater noise attenuation, extending the -120dB noise floor to 70MHz. Partial partitioning can provide an attenuation of -100dB at 70MHz. In the case of using partial partition, a significant amount of the HF noise current can still be coupled to load side through the shield layer instead of being shunted back to the noise source. Complete partitioning involves minimising the openings in the individual shields between the filter sections. In this case, HF noise is encouraged to flow on the inside of shield layer and be returned to the noise source, instead of flowing to the load side. It should be noted, however, that a simple opening between two partitioned regions is unable to block all EM fields because gaps will inevitably exist between the interconnecting conductor(s) and the shield.

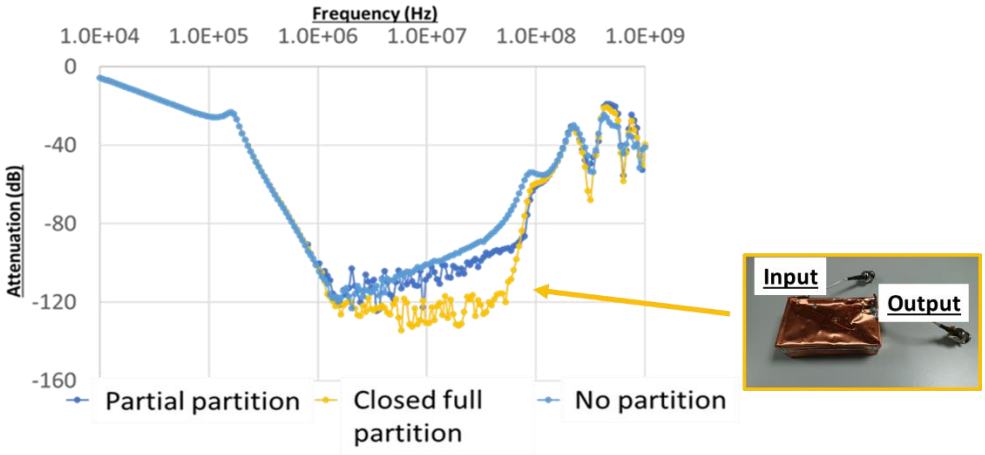


Figure 4-37 Comparison of different partitioning arrangements

4.5 Feedthrough connection techniques: Realizing GHz high frequency EM containment.

4.5.1 Conventional feedthrough capacitors for EM decoupling and the limitations for power electronic application

Even with careful arrangement of filter stages, shields and partitions there are unavoidable apertures in the partitions and shield where the connections are made. RF electromagnetic noise/fields can “leak” through the slots and make the partitioning and shielding structure less effective. The solution adopted is to cover the apertures between the signal conductors and partitions/shields using capacitors, whose layout around the aperture and internal structure is chosen to provide a low-impedance, high-frequency EM path from signal conductor to partition/shield, shown in **Figure 4-38**

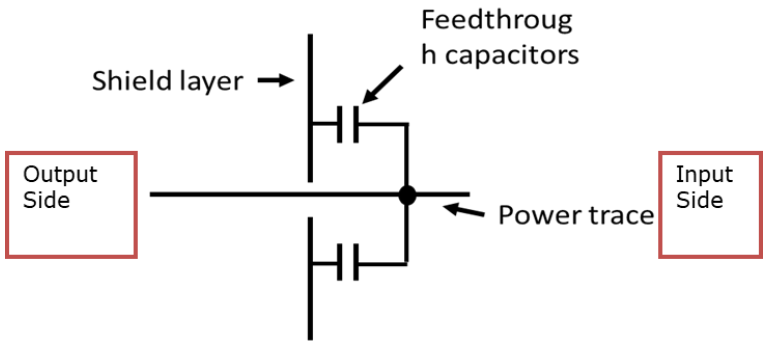


Figure 4-38 Schematic circuit of Feedthrough connection

The effect is two-fold. Firstly, the capacitors form part of the filter stage capacitance, bypassing high frequency currents from the signal trace to the partition/screen (other capacitors may be added remote from the aperture to achieve specific values of capacitance and the correct filtering function in combination with the filter stage inductance). Secondly, the construction of typical capacitors includes multiple layers of metal in the capacitor structure together with metal end-caps, which act to reflect and absorb incident electromagnetic fields. RF noise is thus reflected back into the filter stage rather than being allowed to propagate. With the combination of partition layer and

integrated capacitor, all radiated noise and high frequency noise can be blocked and confined, only letting low frequency noise and the intended signals to pass though.

Conventional feedthrough capacitors perform this function, where the conductor carrying the current or signal is connected concentrically to one electrode and is run centrally through the capacitor. The other electrode is contacted concentrically to the capacitor case. An example is shown in **Figure 4-39** and cross-section of a multi-terminal feedthrough connector is shown in **Figure 4-40**. A feedthrough capacitor typically has a small value of shunt capacitance built into it and is used for bypass purposes in ultra-high-frequency applications. In order to realize the EM decoupling, the feedthrough components must be mounted directly into a closed shielding arrangement and the case must be contacted seamlessly to the shielding wall. With this arrangement, high frequency EM fields will be reflected from the shield and feedthrough rather than being allowed to propagate.



Figure 4-39 Commercialised feedthrough connector from TUSONIX

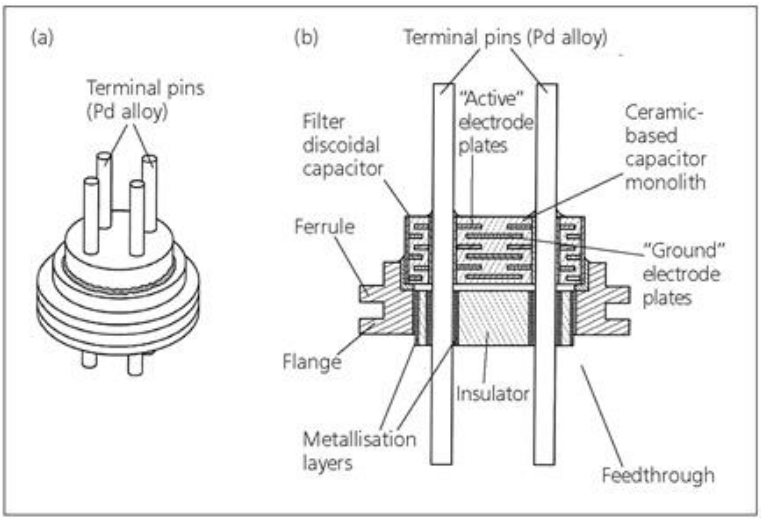


Figure 4-40 3D view and cross-section of a four-pin feedthrough capacitor [149]

Application of feedthrough capacitors provides a very good solution for decoupling EM fields on either side of a shield since their integrated capacitive components provide a low-impedance, reflecting structure. However conventional feedthroughs are only available for use at low current (up to tens of Amperes) and with low isolation voltages (up to 100 Volts). They are not suitable for many power electronics where hundreds or thousands amperes flow through filter stages or where voltages may be as high as several kV. Another drawback of conventional feedthrough connectors is the relatively small, fixed value of shunt capacitance, which is typically of the order of 1 nF. This feature is restrictive where the capacitor is also intended to be applied as part of a filter whose capacitance thus needs to be selected as part of the filter design. Finally, feedthrough capacitors are invariably cylindrical in shape with round conductors. Interfacing such capacitors to the flat rectangular bus-bar structures, or printed wiring traces found in many power electronic applications, is made difficult and will result in additional series impedances in the interconnections.

4.5.2 Proposed new design of feedthrough connections

To mitigate the HF EM field leakage, apertures in shields and partitions may be surrounded by capacitive components connected between the power trace and the shield/partition layers. They provide an EM field reflecting capability and in addition bypass lower frequency current components to the shield so they can be returned to the source. A minimum clearance between shield/partition layers and the power traces must be kept to avoid insulation breakdown and partial discharge (PD). This is particularly important where the voltage potential of shield and power trace differ by hundreds (or even thousands) of volts, for example in power electronic filtering applications. On the other hand, unnecessary clearance could leak RF and HF noise from partition layer and compromise shielding effectiveness.

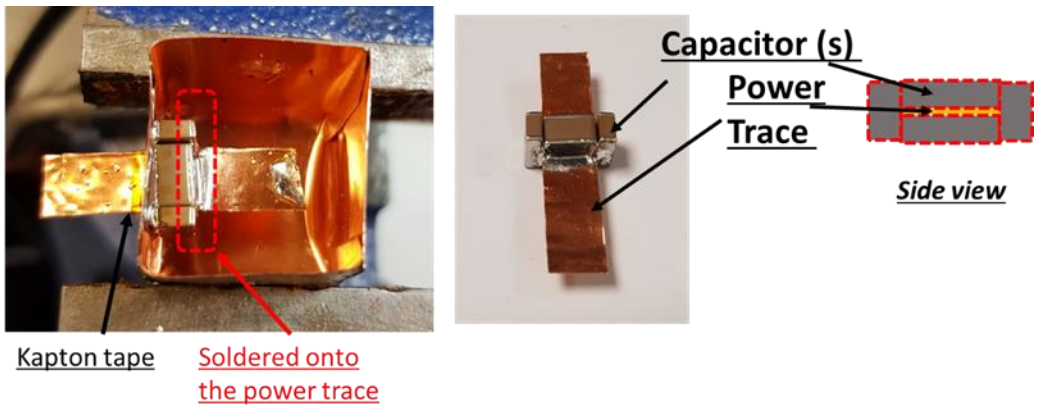


Figure 4-41 Arrangement of 4 feedthrough capacitors

To provide an effective reflecting and blocking structure, thin capacitor(s) may be embedded into the insulation layer to form a layout where power trace is surrounded by capacitors on all sides. **Figure 4-41** shows a practical arrangement of a combination of shield layer and feed through capacitors. A rectangular bus bar is surrounded by 4 chip capacitors, one side of capacitors is soldered onto the bus bar whilst the other side of the capacitors is soldered to the inside of the shield. In this experiment setup, kapton tape is

used to realise electrical isolation between capacitors and the bus bar. Measurements of forward transfer gain were made using a vector network analyser with a 50 ohm source impedance. The result shown in **Figure 4-42** indicates that the configuration of combination of integrated capacitors and shield layer acts as a low pass filter. At frequencies below ~10MHz the response follows that of a classic single-pole low-pass filter with a cut-off rate of -20dB/decade. Above 10MHz frequency range, the shield and integrated feedthrough capacitor can effectively reflect and contain both conducted and radiate EM noise, electromagnetically decoupling the noise source from the load. An attenuation level of over 100dB is maintained from 100MHz till 1GHz.

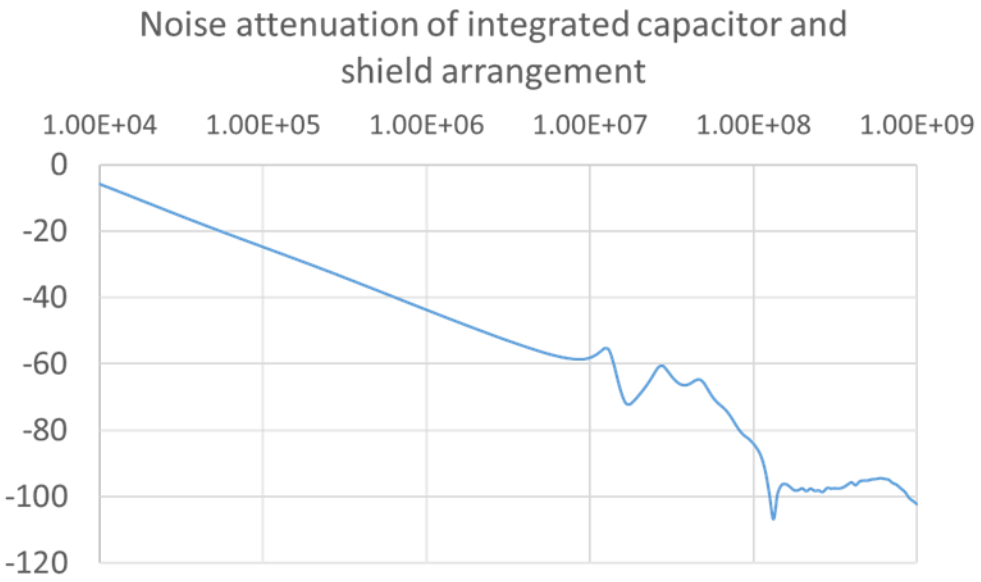


Figure 4-42 Measurement of noise attenuation of a single FT connection

In the arrangement shown in **Figure 4-41** the aim is to completely surround the bus-bar with capacitors. However, small gaps will inevitably be present between each capacitor and these can provide a path for electromagnetic leakage through the bus-bar slot insulation. This effect will become much more noticeable if the feedthrough arrangements does not encircle the bus-bar, for example using a capacitor on just one or two faces of the bus-bar. One such realization of a feed through structure is shown in **Figure 4-43** where only two capacitors are integrated on the top and bottom of the bus

bar, whilst the left and right side is left open. Due to the connection of capacitors, only the top and bottom of bus-bar are electrically connected to shield/capacitor whilst the sides of bus bar are left open, allowing EM field leakage through the sides of the slot insulating layer. The impact of this arrangement is indicated in the measurement comparison shown in **Figure 4-44**. From 10 KHz to 10MHz, there is only a small difference in noise attenuation indicating that EM leakage through the sides of the slot has relatively little impact. However, above 10MHz, the sample with only two capacitors shows an inferior noise attenuation characteristic, resulting in more than 40 dB difference above 100MHz. In conclusion, we can see that an incomplete feed-through structure cannot completely prevent high frequency EM leakage and thus a feed-through solution in which the blocking capacitors completely surround the bus-bar is preferred.

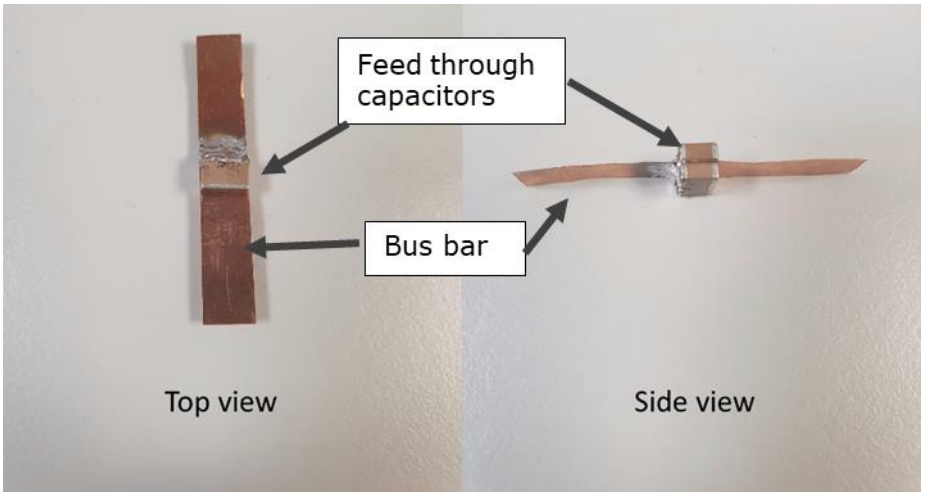


Figure 4-43 Arrangement of 2 feedthrough capacitors

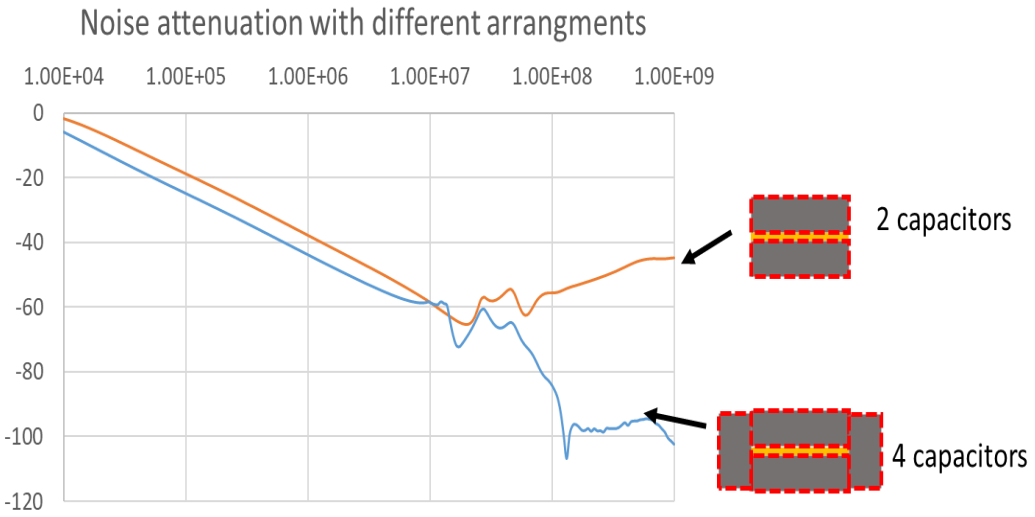


Figure 4-44 Noise attenuation comparison between different feedthrough capacitor arrangements.

4.5.3 Overall performance of filtering, shielding and partitioning

Combined with previous techniques such as multi filter stages, shielding, partition, the overall performance of the proposed broad band filter is shown in **Figure 4-45**. The attenuation characteristic initially displays a -40dB/decade slope above the low-frequency stage cut-off frequency which increases to -80dB/decade above the high-frequency stage cut-off frequency. With partitions and reflecting structures, the response falls below the noise floor (~-120dB) and remains at this level to beyond 1 GHz. This results clearly demonstrates that the feedthrough/ EM field blocking structure successfully confines EM noise inside the shield. By way of contrast, the response of a more conventional arrangement, without inter-stage partitions and reflecting structure shows significant deterioration in attenuation above 1MHz.

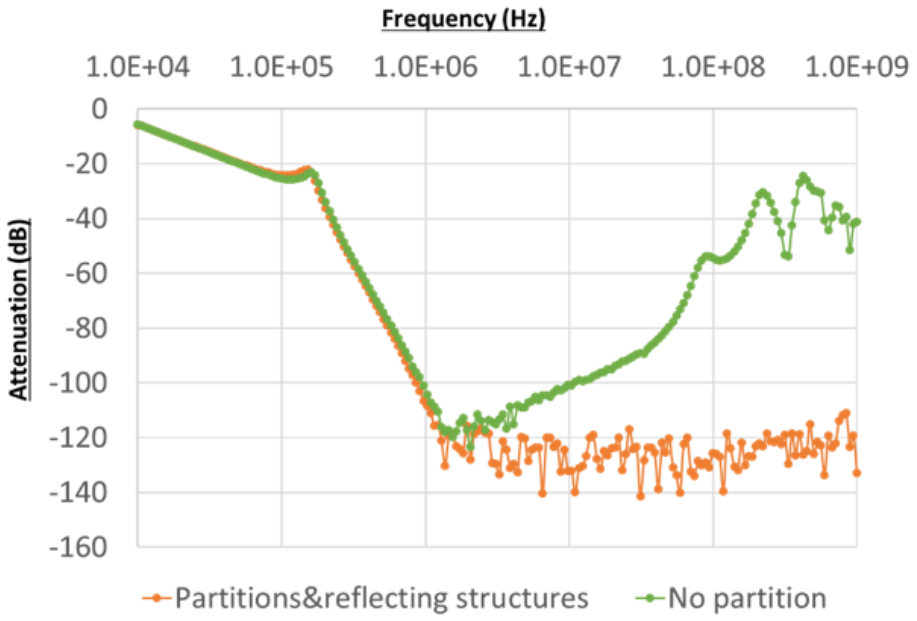


Figure 4-45 noise attenuation comparison between conventional filter arrangement and this invention

This newly proposed arrangement differs from that of a conventional coaxial feedthrough capacitor in that: 1) it is integrated with the partition/shield and filter inductor to provide a specific filtering function rather than simply being a physically separate high-frequency bypass; 2) it can be designed to accommodate arbitrary signal conductor geometries, for example flat bus-bars or circuit traces, rather than being limited to round wires.

4.6 Conclusion

This chapter began with component level simulation and characterization of filter components and each filter stage. Self-parasitic components such as EPC and ESL are the main factors influencing filter behaviour. Introduced ESL and EPC cancellation techniques may be applied to improve stand-alone filter performance. On the other hand, mutual parasitic coupling is another key factor to decide the filtering performance of multistage filter configurations. It is typically dominated by inductive coupling between different components and gives rise to further unwanted parasitic effects in the filter. Much better filtering performance can be achieved through the proper layout of components, which is realized by changing magnetic coupling direction to perpendicular position and by shielding to decouple electromagnetic field linking. The effective confinement of high frequency electromagnetic fields requires the filtered noise currents to be returned to the source from each filter stage. To achieve the best high frequency performance, the impedance of the return path must be minimised and this becomes progressively more important at higher frequencies. It is thus desirable to minimise the length and thus the impedance of all return paths and particularly those associated with the higher frequency components. By applying shielding and partitioning techniques to cascaded filter stages, high frequency noise can be more easily confined within each partition thereby reducing coupling to subsequent stages and the load, thereby realizing a high level of EM decoupling from the source to the load. In this case, any component of noise current that is coupled from one partitioned region into the next will be preferentially returned back to the noise source rather than propagated to the load. Finally, specific feedthrough connections are adopted to cover the apertures between the signal conductors and partitions/shields using capacitors. Firstly, the capacitors form part of the filter stage capacitance, bypassing high frequency currents from the signal trace to the partition/screen. Secondly, the construction of typical capacitors includes multiple layers of metal in the capacitor structure together with metal

end-caps, which act to reflect and absorb incident electromagnetic fields. Combined with previous techniques such as multi filter stages, shielding, partition, the overall performance of the proposed broad band filter realizes the highest level of -120dB noise attenuation up to 1GHz. This new EM suppression solution demonstrates that the feedthrough/ EM field blocking structures can successfully confine EM noise inside the shield.

Chapter5. Electromagnetic interference suppression techniques applied on fast switching GaN converter

5.1 Introduction

In the previous chapters we introduced the use of combination of screening, shielding, integrated filtering, partitioning, and feedthrough connection to suppression electromagnetic interference. Simulation tool ANSYS Maxwell and circuit simulator PSpice were used for the effectiveness prediction of EMI suppression comparing different layouts and arrangements. A Network Analyzer (VNA) was used to generate a passive noise source (sinusoidal excitation) and this was fed into the EMI noise suppression system to emulate ac active noise source such as a switching cell. The resulting frequency response was used to investigate screening effectiveness for different screen layer arrangements and broad band filtering effectiveness for different layout. In general, electromagnetic shielding and screening provide an attractive method to achieve low levels of EM emission and may eliminate the need for separate common mode filters in some configurations. Integrated filters are employed to remove noise at output terminals to achieve a clean switching environment, mitigating both conducted and radiated EMI together. All above investigation were based on small signal circuit, which has low voltage and low current.

In this chapter, to illustrate that the various techniques described in the previous chapters may also applied to large signal (high current & high voltage) practical power electronic switching cells, we employ a GaN (Gallium Nitride) half-bridge power module, configured as a step-down or buck converter, as a source of switching noise. RF current probes (Fisher Custom Communications F-33-3 Bandwidth: 1kHz-200MHz), with a bandwidth of 200MHz, are used to measure CM and DM noise at both input and output, whilst a near

field probe is used for radiated noise measurement. The effectiveness of the range of interventions including shielding, screening, integrated filtering, partitioning and feedthrough connection are determined by comparing the differential mode, common mode and radiated noise spectra over a frequency range from 1MHz to 200MHz using a Rhode & Schwarz spectrum analyser (ESL EMI Test Receiver ESL3 9kHz to 3GHz).

5.2 GaN power module characterization and initial EMI measurement

5.2.1 GaN power module description

We have employed a GaN (Gallium Nitride) half-bridge power module, configured as a step-down or buck converter, as a source of switching noise. **Figure 5-1** shows the compact GaN half-bridge, obtained as a commercial product from EPCOS & Fraunhofer. This GaN power module has an integrated DC link 1uF, 500V Ceralink capacitor and it also features integrated isolation to the heatsink using an Insulated Metal (IMS) substrate. The gate driver is a Texas Instruments LM 5114 driver. 2 GaN system GS66508T 650V, 55mΩ GaN HEMTs are position between the bottom IMS substrate and top IC gate drive PCB board to form a half-bridge layout. **Figure 5-2** is the SEM image of side view and shows the detailed layout of this power module. The DC link capacitor is positioned right above the two GaN HEMTs to realize ultra-low parasitic inductance between DC link and switching stage and to reduce unwanted voltage overshoot during switching. Measured loop inductance is about 2.8nH. Similarly, Gate deriver TI LM5114 is also placed as close to the GaN devices as possible to diminish unintended inductance at gate input terminal to improve switching speed and prevent gate signal ringing. The equivalent circuit of gate driver and turn on and turn off resistor is shown in **Figure 5-3.** Ron is 20Ω and Roff is 2Ω. V supp+ is driver positive supply voltage, V supp- is driver negative supply voltage, In is driver signal input, and Vref is driver reference potential connection. In this experiment, the Vref to Vsupp+ is 7V and Vsupp- to Vref is -

10. IMS substrate consists of 1mm thickness of copper layer on the top, 70um thickness of isolation layer in the middle and 140um thickness of copper layer at the bottom, which yields 148.73pF parasitic capacitance from the output port to the backside of IMS substrate, measured by impedance analyser. In general, this parasitic capacitance becomes very low impedance at MHz high frequency, and is the main path for common mode current flow when the potential of output port changes during switching.

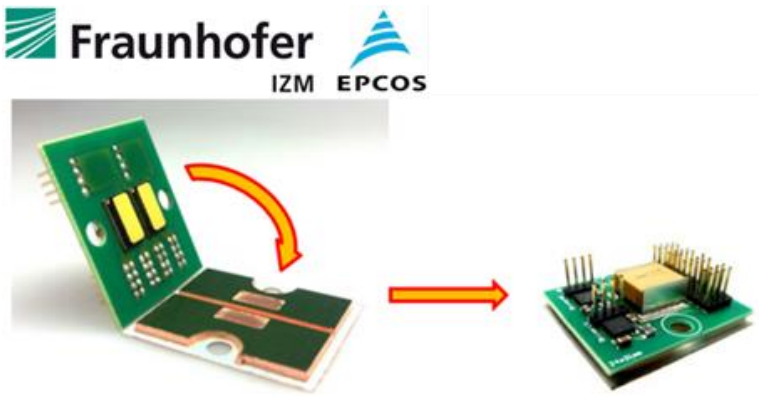


Figure 5-1 GaN power module

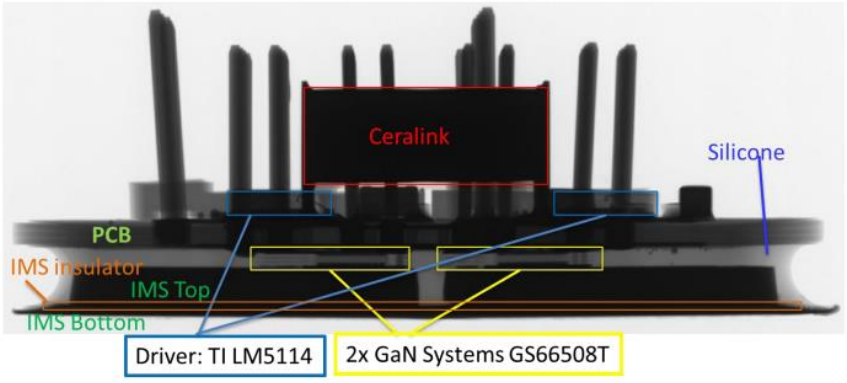


Figure 5-2 SEM image of GaN power module (side view)

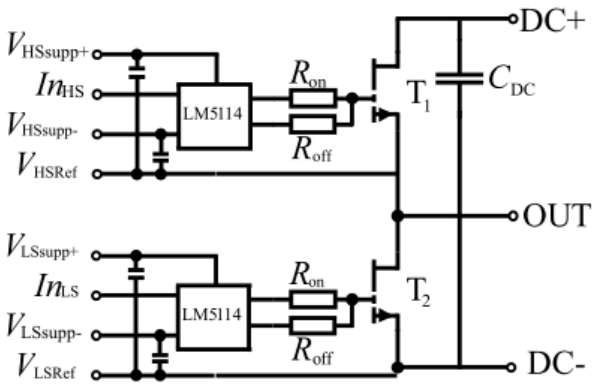


Figure 5-3 Equvilant circuit of gate driver and turn on and off resistor

5.2.2 Double pulse test

Before continuous operation of GaN half-bridge power module, we used a double pulse test to confirm the switching behaviour under very fast switching condition. **Figure 5-4** shows the schematic diagram of the double pulse test circuit used in the experiment. DC link capacitors consists of two 50uF metallized Polypropylene Film Capacitors (VISHAY 50u 500V MKP 1848-c), and two 4.7uF metallized Polypropylene Film Capacitors (VISHAY 4.7u 400V MKP 1840-M). A 250uH air-cored inductor is used as the load inductor. The GaN half bridge power module has one high-side switch and one low-side switch but the double pulse test are conducted on the low side switch only. The high side switch is kept off by shorting gate and source to avoid unintended turn-on of high-side switch, by direct connection between V_{HSRef} and the GaN device gate input pad.

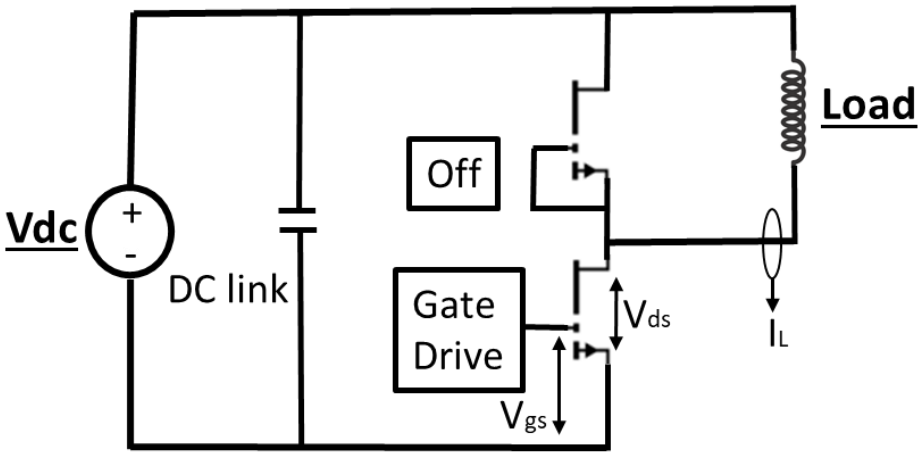


Figure 5-4 Schmatic of the double pulse test circuit used in this experiment

Figure 5-5 shows the close-up of double pulse test setup and connection arrangements around GaN power module. To drive the low side switch, 6V is supplied to VLsupp+ to power the gate driver LM5114 from a DC power supply HY3003-3 digimess®, whilst VHsupp- and VHSRef are connected to the reference port of the power supply instead of feeding negative voltage to VHSupp- port, which are shown on the right side of **Figure 5-5**. Pulse signal is supplied to InHS port from a function generator AFG3022C Tektronix. Also the reference potential of function generator is connected to that of DC power supply. DC- ,DC+ and output cables are soldered onto 8-pin sockets which are directly connected to the terminals of GaN power module on the left side in **Figure 5-5**. Passive voltage probes are used to measure Vgs and Vds, which are Tek P6139A 300V 500MHz and 8.0pF PVP. The termination resistance of the oscilloscope is chosen to be 1MΩ. Bringing the ground potential of oscilloscope into the measurement is the downside of using passive voltage probe. This may cause EMI noise to couple to the ground during measurement and alter the measurement results out of passive voltage probe. Despite of this drawback, the broad bandwidth and high voltage measurement rating make it adaptable to measure fast switching devices. In the measurement of Vgs and Vds, the contact across the drain-source and gate-source has been made as close as possible to interference from parasitic inductance in the measurement loop.

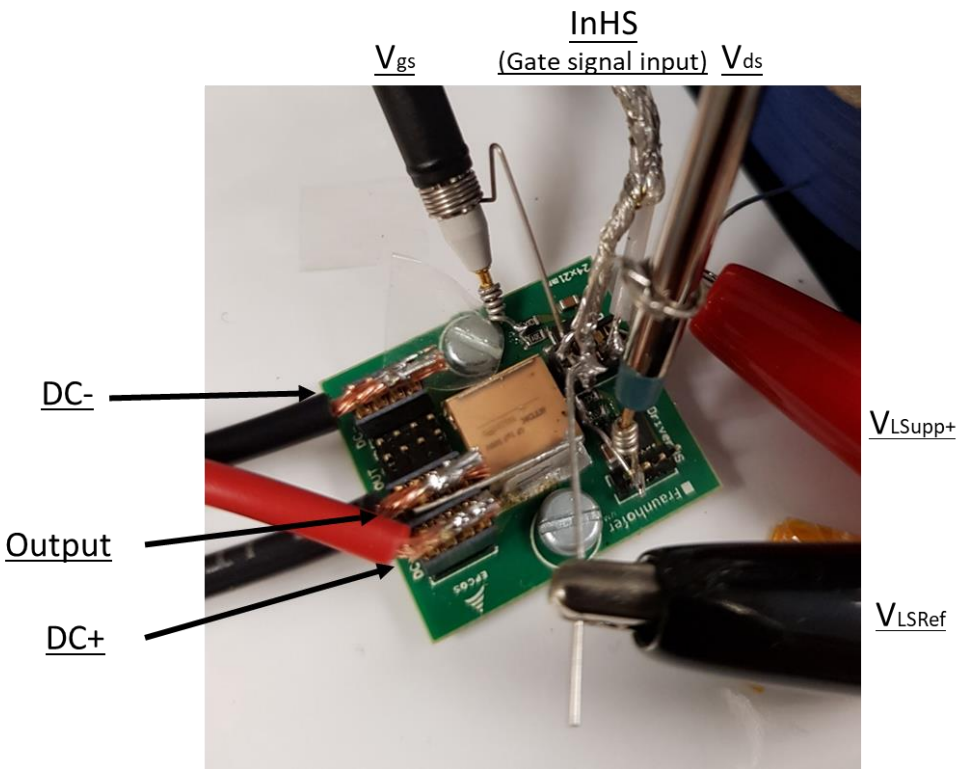


Figure 5-5 Double pulse test setup of GaN half-bridge power module

In the double pulse test, firstly a turn-on pulse of 10us time span is applied to the low-side GaN device. Positive voltage +Vdc is applied across the inductor during this time internal and therefore the load current rises up to 4.0A. The duration of this pulse is adjusted according to the target test current. The device is turned off at the end of the first pulse. The inductor current free-wheels through the high-side always-off GaN device. After a short while the low-side device is turned on again, and the inductor current commutates from the high-side to low-side device. The device turn-off time between two pulses is kept short so that the current change in inductor is small. At the end of second pulse, the load current reaches 9.1A. The device is turned off again after a small time interval, and the inductor current flows through the high-side device until it gradually reduces to zero. The device turn-off characteristics is obtained at the falling edge of the first pulse and the turn-on characteristics is obtained at the rising edge of the second pulse. The turn-on and turn-off transitions of the GaN power module voltage and current are recorded by digital phosphor oscilloscope DPO7104 Tektronix.

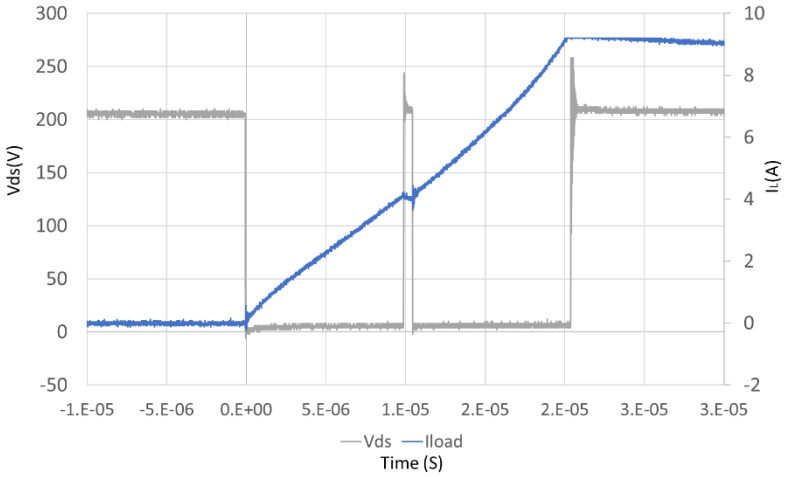


Figure 5-6 Double test results at 200V-9A Vds-IL

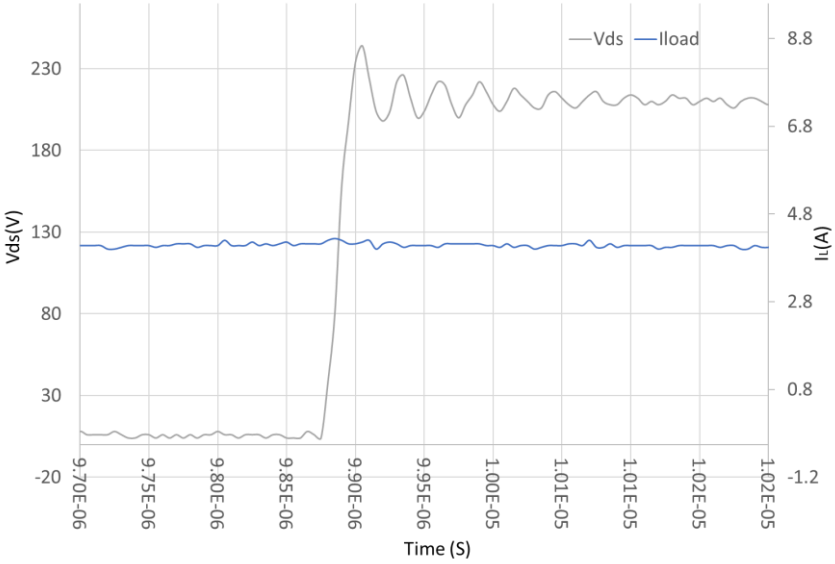


Figure 5-7 Double pulse turn-off transient

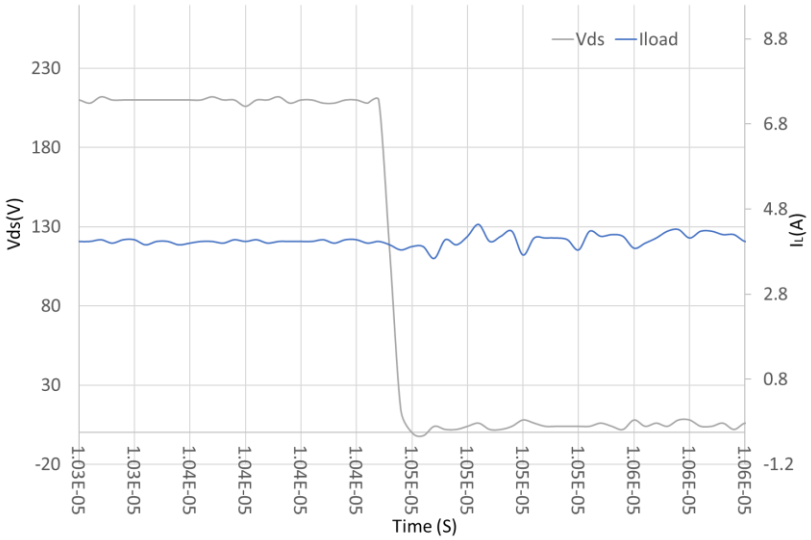


Figure 5-8 Double pulse turn-on transient

The double pulse test waveform for 200V and 9A are shown in **Figure 5-6, 5-7 and 5-8.** In **Figure 5-6** the overall record during the double pulse test is shown, and **Figure 5-7** shows the turn-off transition, **Figure 5-8** presnts the turn-on transition. During turn-off transient, voltage rises at a rate of 13.3V/ns, and during turn-on transient, voltage falls at the rate of 20V/ns. In this experiment, since the GaN HEMT devices are embedded into the Power module, between top gate driver circuit and bottom IMS substrate, the device current I_{source} cannot be measured easily through conventional solution such as Rogowski coil. Instead, the load current is measured by current probe and shown in the **Figure 5-6, 7 and 8**. It is noted that the voltage overshoot is 30V against Vdc= 211V at turn-off transient, which is only 15% of Vdc, and this relatively small overshoot voltage results from the usage of compact and low ESL ceramic capacitor and integrated DC-link layout with low parasitic inductance current commutation loop. Less overshoot and voltage ringing contributes to a cleaner switching environment. From this double pulse test, switching behaviour under very fast switching condition has been confirmed.

5.2.3 Gate power circuit design

In the double pulse test, the gate driver is power by external DC power supply and gate control signals are provided by external function generator. All these signals and power have to be fed through coaxial BNC cable or twisted power cable. These cables or interconnecting structures are the most critical for the overall effectiveness of EMI suppression when a closed and complete shield and screen arrangement is applied to this GaN power converter. When cables go through the shield layer, a slot or opening cannot be avoided. The electromagnetic wave length becomes shorter and electromagnetic fields can more easily leak from the slots/opening between the filter stages and where external connections are made. It is noted that the greater the number of interconnection passing through the shield layer, the more routes are available for EM fields to leak to the external

environment. On the top of that, all connections that penetrate the shield have to be filtered and high frequency noise has to be completely attenuated inside the shielding containment, otherwise high frequency noise would be able to couple to the external environment, compromising the overall effectiveness of combined EMI suppression techniques. Low frequency connection, for example a DC power supply would not be affected by the filtered termination arrangement, however, the gate control signal cannot pass through the shield without being affected. The gate signals must therefore be generated within the shield.

In order to avoid the concern about openings for the signal and power cables passing through and to persuasively demonstrate EM field confinement with a simple design and arrangement, we use an internal battery to power the gate driver and the pulse generator IC that is used to generate the gate control signals. **Figure 5-9** shows the schematic diagram of IC circuit of powering gate driver of GaN power module.

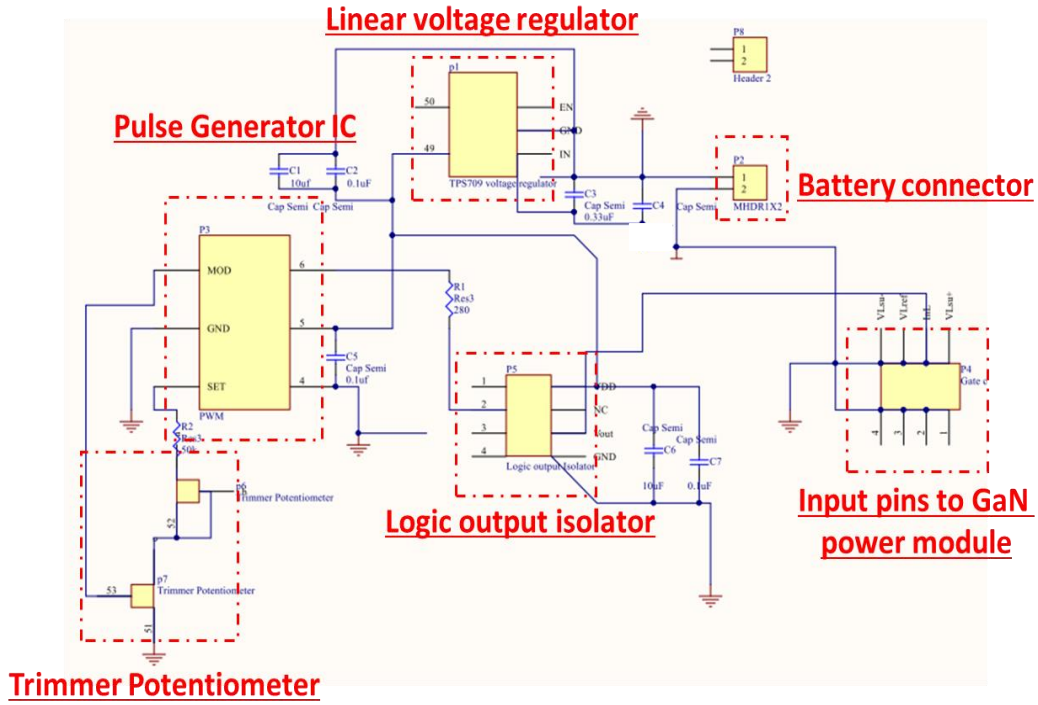
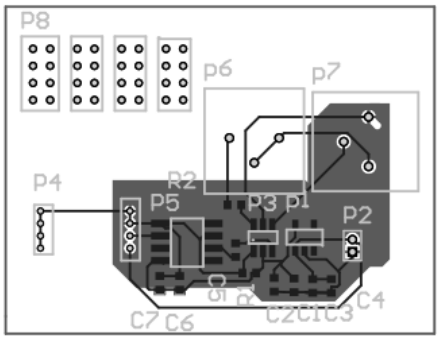


Figure 5-9 schematic of IC circuit for gate driver of GaN module.

The designed circuit mainly consists of 4 components: first, is the linear voltage regulator, TPS709 150mA, 30V, 1uA with Enable, which is ultralow quiescent current device designed for power sensitive applications. Quiescent current of only 1uA makes it ideal solution for the a battery-powered and always-on system. This linear voltage regulator transforms Vdc=6V to acceptable level of 5V to power pulse generator IC. Second, is the pulse generator IC, LTC6992 Linear Technology, which can generate pulse width modulation (PWM) with variable duty ratio from 0% to 100%, and has frequency range up to several MHz. This pulse generator is used to create pulsating waves as gate control signal to feed InHS GaN device gate input. Because it has analogue voltage-controlled pulse width modulation capability, it provides the capability to produce different switching frequencies and different duty ratios to investigate the cases with high and low load current. Output frequency is determined by $f_{out} = \frac{1MHz*50K}{N_{DIV}*R_{SET}}$ and $D = \frac{V_{MOD}}{0.8*V_{SET}} - \frac{1}{8}$. The Rset and ratio of Vmod and Vset are determined by two trimmer potentiometers, and in this experimental setup Ndiv (an internal frequency divider) is set to 1. Third, is the digital Isolator SI8715BC-A-IS, a 5kV LED emulator input Logic Output CMOS Isolator for popular optocouplers with data rates up to 15Mbps. It isolates high-speed pulse generator from switching stage. Forth, is the Trimmer Potentiometer, single turn and 3/8inch square potentiometer, and resistance value ranges from 10 Ω to 2 MΩ. The 6V power supply is provided by 5 AA rechargeable batteries in series. **Figure 5-10** shows the PCB design layout and **Figure 5-11** shows that the PCB connected to the GaN power module alongside the 6V battery.



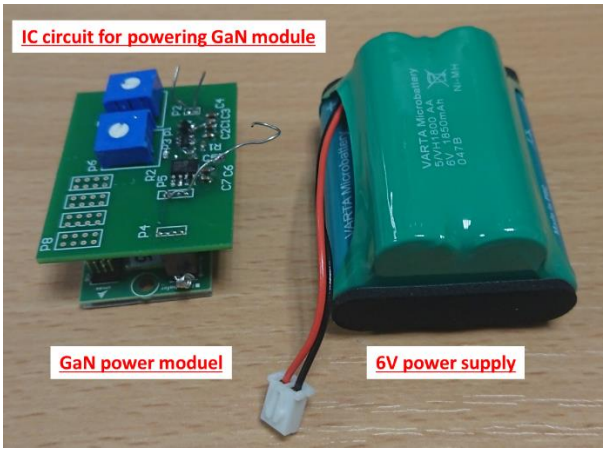


Figure 5-10 IC circuit layout (Left)

Figure 5-11 IC circuit and powering GaN power module

5.2.4 EMI measurement setup & Initial conducted and radiated EMI measurement results

Figure 5-12 shows an outline schematic of the experimental arrangement, including switching cell, DC power source, LISN (Line Impedance Stabilization Network), and load. Differential Mode (DM) noise, indicated by the green dashed lines is circulated between the DC-link and switching stage/LISN at the input side and between the load and switching stage at the output side. Coupled Common Mode (CM) noise is circulated between the converter system and the ground, indicated by the dashed red line.

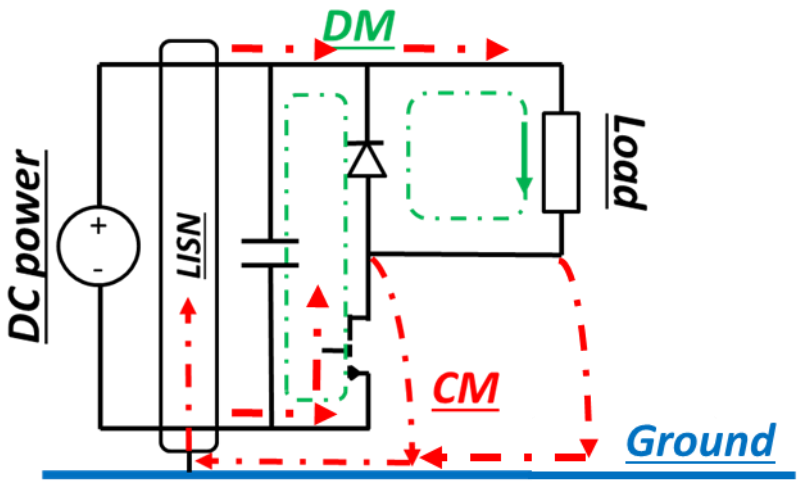


Figure 5-12 Schematic of GaN power converter

RF current probes (Fisher Custom Communications F-33-3 Bandwidth: 1kHz-200MHz), with a bandwidth of 200MHz, are used to measure common mode and differential mode noise at both input and output, whilst a near field probe is used for radiated noise measurement. A schematic of the instrumentation and an image of the experimental set-up are shown in **Figure 5-13**. The effectiveness of the range of interventions described in the previous chapters were determined by comparing the common mode, differential mode and radiated noise spectra over a frequency range from 1MHz to 200MHz using a Rhode & Schwarz spectrum analyser (ESL EMI Test Receiver ESL3 9kHz to 3GHz).

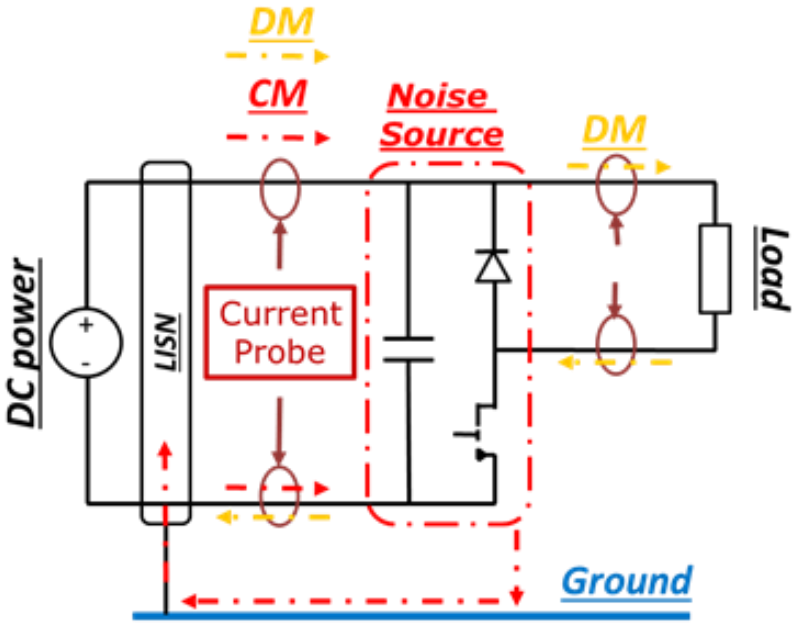


Figure 5-13 Schematic of EMI measurement

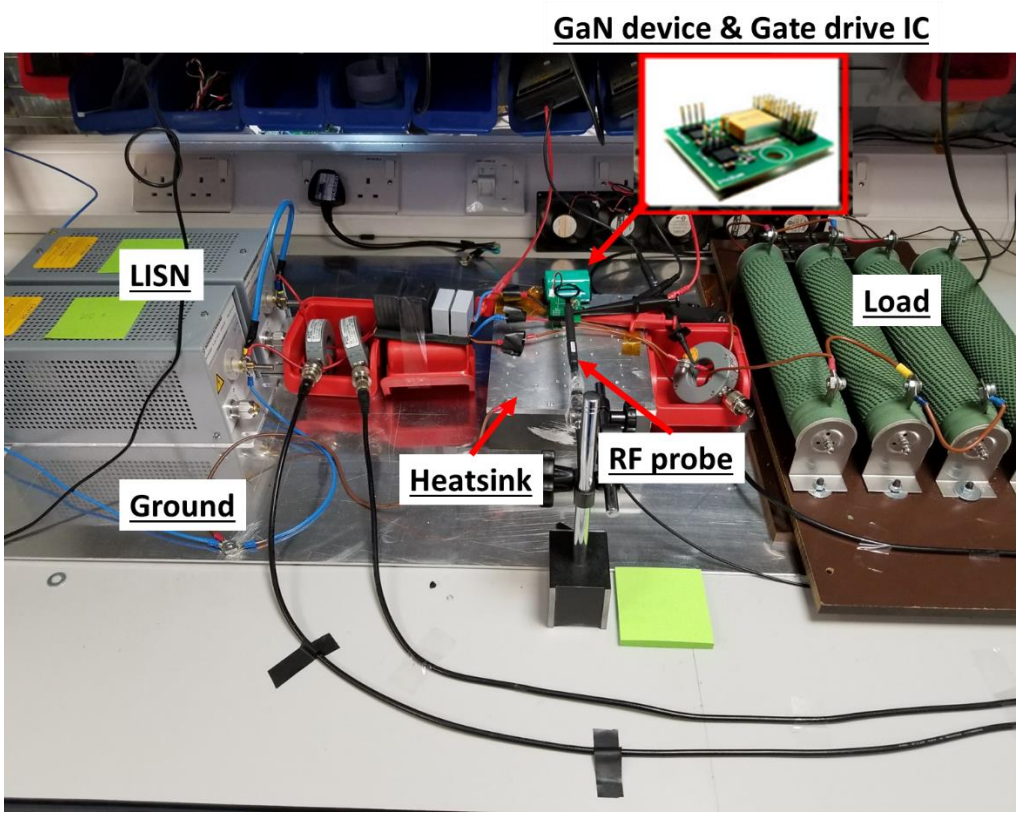


Figure 5-14 EMI measurement setup

Figure 5-14 shows the EMI measurement setup. From left hand side in the **Figure 5-14** is Line Impedance Stabilization Network (LISN) ESH3-Z6 supplied by Rohde&Schwarz. The

R&S®ESH3-Z6 single-phase V-network with an equivalent circuit of (5 µH + 1 Ω) || 50 Ω meets the requirements of EN55016-1-2/CISPR16-1-2 (low-impedance power supplies), EN55025/CISPR25 as well as MIL-STD-461, DEF-STAN59-411 and DO-160 in the frequency range from 100 kHz to 200 MHz. The R&S®ESH3-Z6 is rated for a continuous current of up to 100 A and can handle surges of up to 500 A for a maximum of 30 s. Both sides of the LISN are grounded to an artificial ground, a conductive metal layer. XDC 600-20 DC power supply is connected to the LISN on the left (outside the **Figure 5-14**). On the right side of LISN, 50Ω termination and DC + and – line to the DC link capacitor are connected. DC link capacitors consist of two 50uF metallized Polypropylene Film Capacitors (VISHAY 50u 500V MKP 1848-c), and two 4.7uF metallized Polypropylene Film Capacitors (VISHAY 4.7u 400V MKP 1840-M). Next to the DC link is the GaN power module mounted onto an Aluminium heatsink with a size of 40cm*40cm*20cm, whose thermal resistance is 3°C/W. This heatsink is connected to the artificial ground through a short and thick cable to ensure low parasitic impedance in the common mode current path. On the right hand side is the load which consists of three 47Ω resistors (TE500B47RJ Power rating: 500W) in parallel and three 100uH ferrite cored inductors (AGP4233-104ME, -40 °C to +125°C with max Irms=34A). Current probes for common mode and differential mode noise measurement are inserted between LISN and DC link at input side and between switching stage and load at output side. The load is positioned above the artificial ground and electrically isolated by a 2cm thickness wood fixture. RF probe RF-R-400 for high frequency range (50MHz-1GHz) and LF-R-400 for middle frequency range (1MHz-50MHz) is used to measure radiated noise and is positioned above GaN power module at a distance of 10mm. the centre of the probe head is aligned with the centre of GaN module to reach the maximum radiated magnetic field coupling. It should be noted that the orientation and distance of RF probe head impacts the measurement results very much.

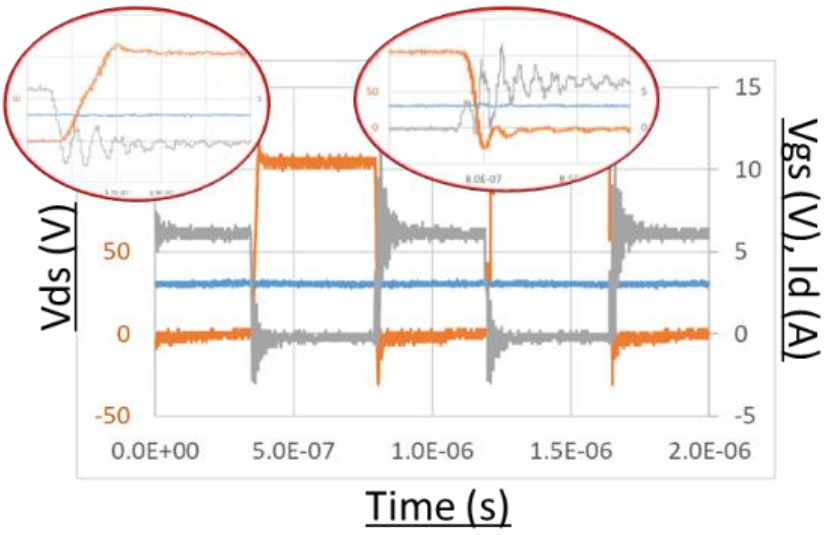


Figure 5-15 switching wave form

In the experimental setup, the GaN device is switched at a frequency of around 1.1 MHz with a DC input voltage of 100V and output current of 3.1A. Voltage rise and fall times of 9ns and 3ns respectively ensure that a broad-spectrum of EM noise is generated, extending from the switching frequency to over 100MHz. Typical switching voltage wave forms are shown in **Figure 5-15**. From the initial EMI measurement results of **Figure 5-16**, a high level of noise is visible in both conducted and radiated measurements. The first noise peak is at the 1.1MHz switching frequency with its harmonics and high frequency noise showing a significant level up to at least 200MHz (limited by the current probe bandwidth). The input CM and output DM results show a conducted noise level of more than 100dB compared to background noise (noise floor). Background noise is measured at the condition where the switching stage keeps off and the DC main power source remains on. On the other hand, the input DM does not have high level of noise across the whole range compare with the output side DM. This is because the DC link capacitor is integrated next to the GaN HEMT device in a very compact arrangement, and this capacitor returns and attenuates most of DM noise from the half bridge. In the following

EMI investigations, the input CM and output DM are the main targets because these are dominant.

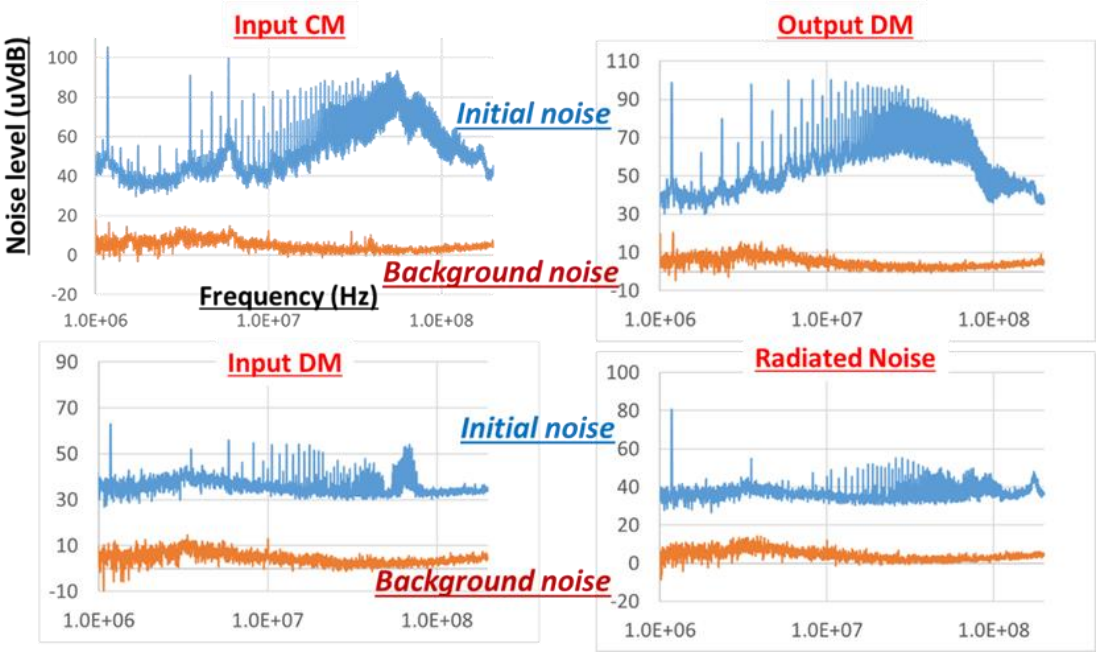


Figure 5-16 Conducted and radiated noise measurement results of initial setup

5.3 Interventions of EMI suppression techniques

5.3.1 Screening and shielding techniques (changing distance / full or semi-full shield arrangement)

The first intervention is to create a screen layer between GaN power module and heatsink to intentionally couple varying electrical field generated from output node of GaN power module to the screen, decouple the parasitic coupling between the node and the ground and to return the coupled noise current back to the noise source. The return path consists of a short and thick busbar to the DC-link negative with very low parasitic impedance, as shown in **Figure 5-17**.

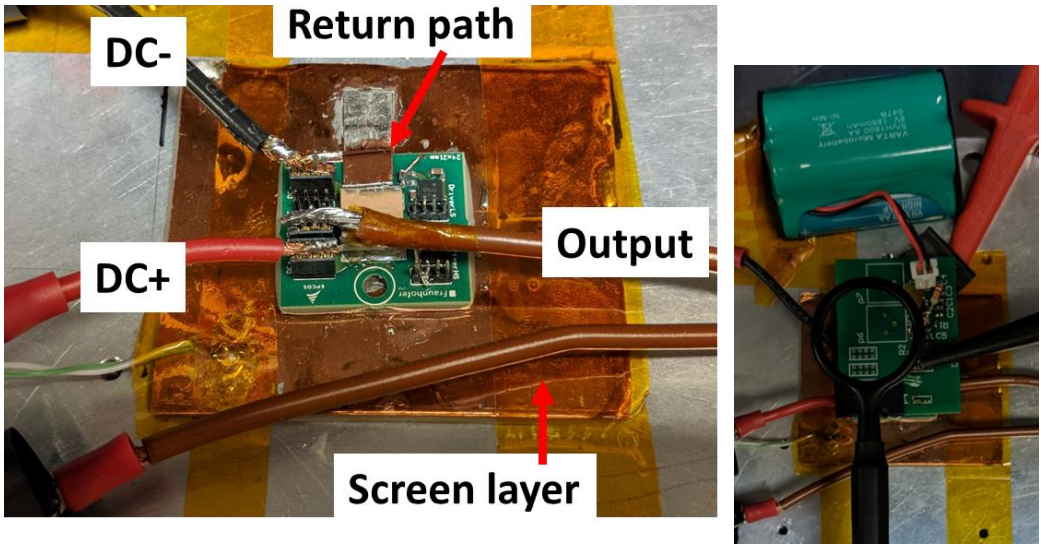


Figure 5-17 EMI setup with screen layer (Left), finalised setup with battery and gate powering IC circuit (Right)

Due to the metallization on the back side of GaN power module, it is possible to directly solder this GaN module onto a wide copper screen layer, which in this case has a size of 100mm*100mm*0.2mm. Backside of IMS substrate and screen layer becomes a unified potential. Electrical isolation between the screen box and heatsink is achieved by inserting an AlN (Aluminium Nitride) ceramic substrate.

As discussed in the chapter 3, different return patterns produce different return path impedance and result in different signal attenuation from noise source to ground. Lower impedance ratio of internal current path compared with the external path always results in better screening effectiveness. Therefore, 8mm wide 0.2mm thick copper sheet is used as a bus bar, where one side is directly soldered on the DC link capacitor rather than to the DC- terminal, which would add parasitic impedance from the terminal to DC link along the internal path of GaN module. The other side of the bus bar is soldered onto the screen layer to make sure that the screen layer and DC- have a unified potential. The total length bus bar is kept to a minimum to minimise the parasitic impedance of the return path. Kapton tape and fixture are used to eliminate air gap between screen layer and ceramic

layer and heatsink. DC + & - cables are connected to the terminals on the left side and output cable is connected across the whole power module from the right side. The finalized EMI measurement setup is shown in Figure **5-17**, where battery and gate powering circuit are inserted during measurement.

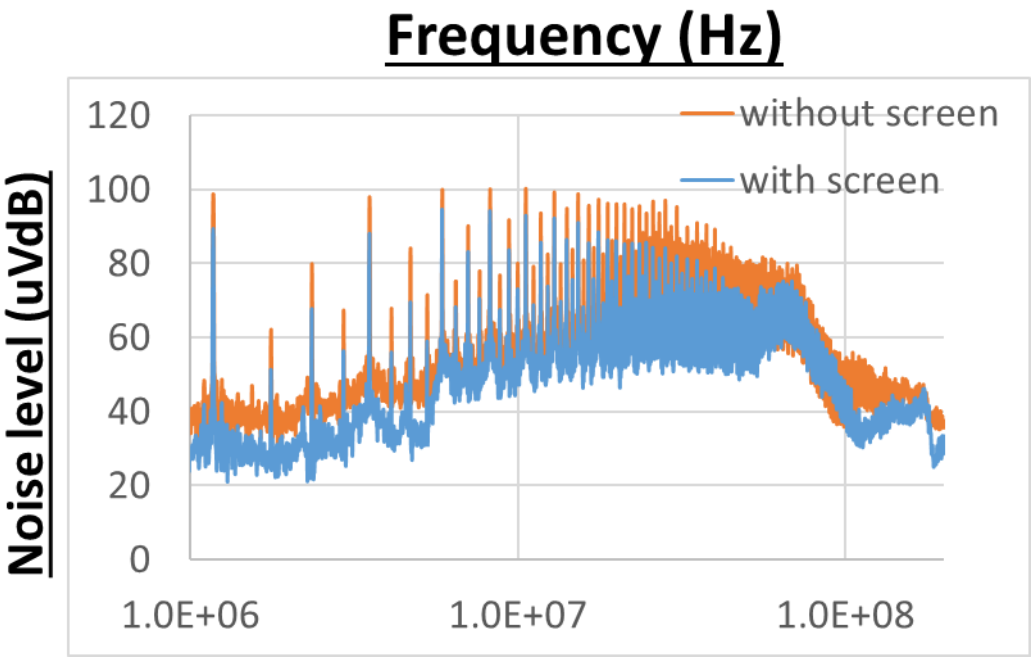


Figure 5-18 Input side CM noise comparison between with and without a screen layer

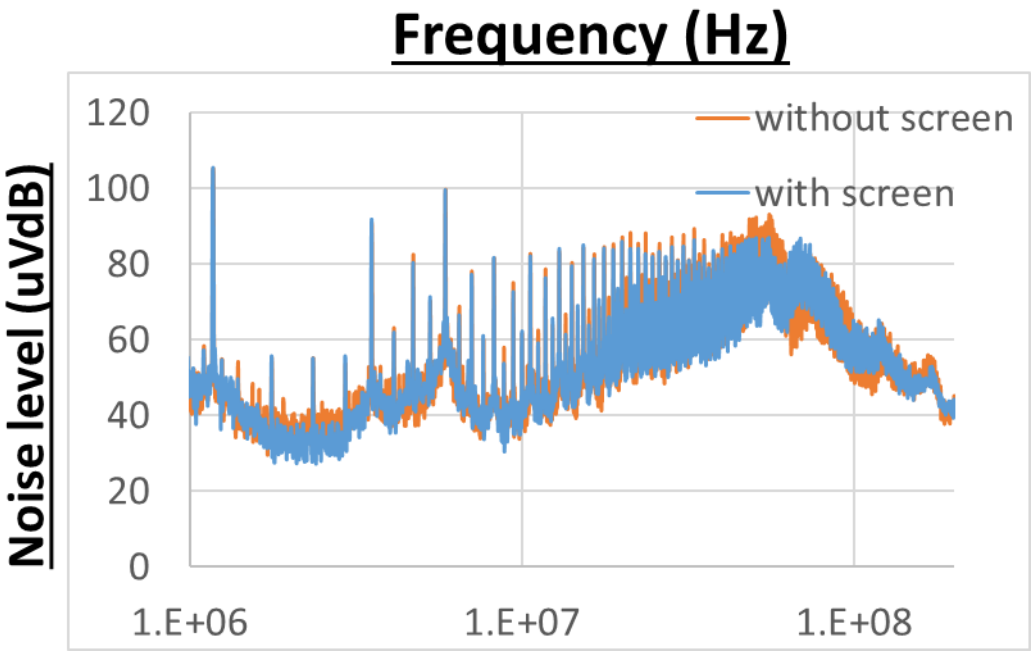


Figure 5-19 Output side DM noise comparison with and without a screen layer

Figure 5-18 and 19 show the measurement results of input side CM and output side DM of the comparison between with and without a screen layer. The blue spectrum is with and the orange spectrum is without the screen layer. From **Figure 5-18**, we can see a screen layer has some effect on common mode noise, yielding a reduction by -10dB at the switching frequency and by about -5dB to -8dB at the harmonics and higher frequencies. This result explains the screen layer and the low impedance return path are effective on CM reduction. On the other hand, output DM results show no difference between with and without screen layer. This is because the screen layer has no impact on DM noise attenuation owing to the totally different circulation path for DM noise.

As noted in chapter 3 more capacitive coupling Cns between the output node and the screen, and less coupling Cng between output and the ground can improve CM attenuation effectiveness. It can be realized by a complete and closed screen arrangement around the noise source, as shown in **Figure 5-20 and 21**. In order to achieve the maximum coupling of the noise source with screen layer and minimum coupling with the ground, the full screening arrangement with the size of 70mm*120mm*45mm is adopted. With this size, both GaN power module and battery can be accommodated within the screen box. The screen box is made of 0.1mm thickness copper sheet. Similar to the previous arrangement, the GaN power module is directly soldered on the bottom of the box. The same size of bus bar is made to return CM noise current and it is also soldered on the bottom of the screen box. AlN ceramic substrate is used to isolate the screen box from the heatsink. Openings with the size of 5mm diameter are made in the screen layer for passing DC+& DC- on the left side and output cable on the right side. The finalised setup is shown in **Figure 5-20**. In order to realize a closed and complete screen layer and achieve the maximum parasitic coupling between the noise source and the

screen layer, top side screen cover is made and solder-jointed with the existing screen box.

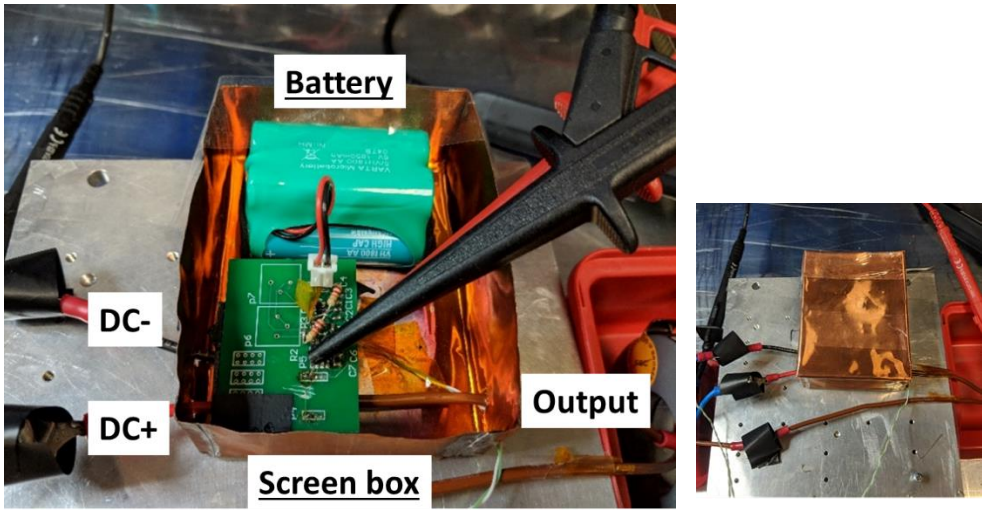


Figure 5-20 EMI setup with screen box (left), final setup of screen box with the top cover (right)

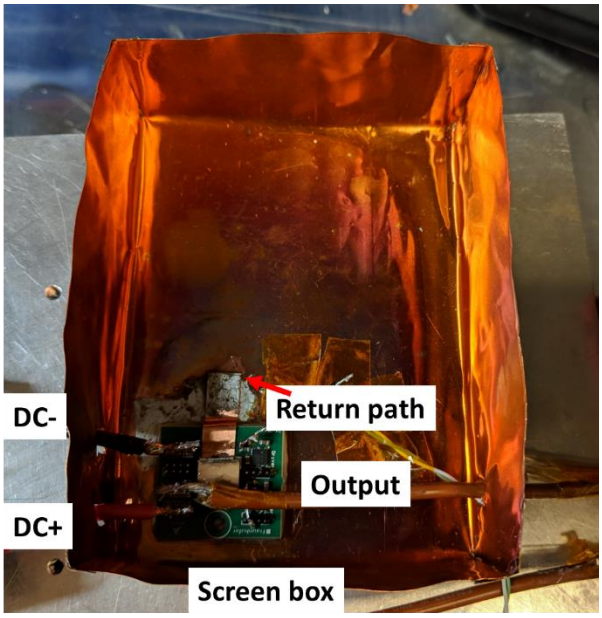


Figure 5-21 EMI setup with screen layer and noise returning bus bar

Input CM and output DM noise comparison are shown in **Figure 5-22 and 23** respectively. In spite of the closed and continuous screen box which envelopes the whole noise source GaN power module, very small improvement of CM noise attenuation can be observed.

There is only -2dB or -3dB additional attenuation at switching harmonic frequencies and at MHz frequency range. Similar trend can also be seen in output DM noise attenuation. Compared to the significant (more than -90dB) noise attenuation described in chapter 3, that obtained from this active GaN power module is very different and much worse than might be expected. This stunning difference on screening effectiveness between two setups can be explained as follows. In the chapter 3 setup, excited noise is fed into the closed and complete screen box by a coaxial BNC cable, and there is no parasitic coupling path for the noise current to reach the external ground. However, in the case of GaN power module, the “screen box“ cannot remain complete and closed as the previous one, as long as there are openings in the screen layer for power input and output cables passing through. More electromagnetic field would leak to the external environment from the gap between the power cables and screen layer. On the top of that, unfiltered power cables introduce more parasitic coupling into the system, where internally generated noise could couple to the external environment. It is safe to say that without being filtered, the power cables act as antenna radiating noise to surrounding components and the ground. In other words, unfiltered connections at the interface of screen layer compromise the function of screening technique, and leads to the limited

impact on CM suppression.

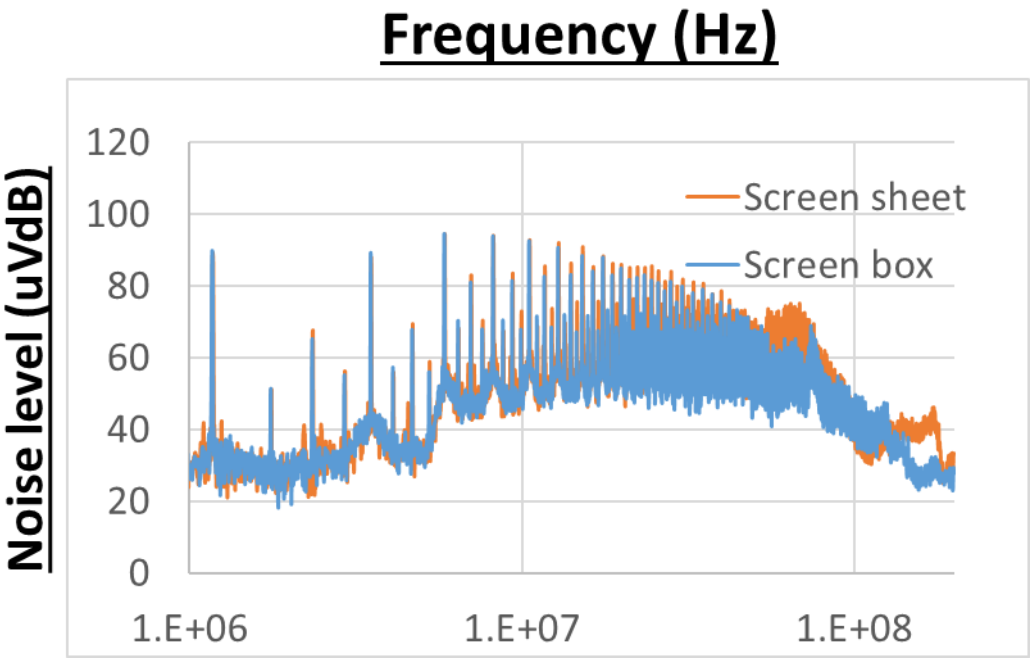


Figure 5-22 Input side CM noise comparison between a screen box and a screen sheet

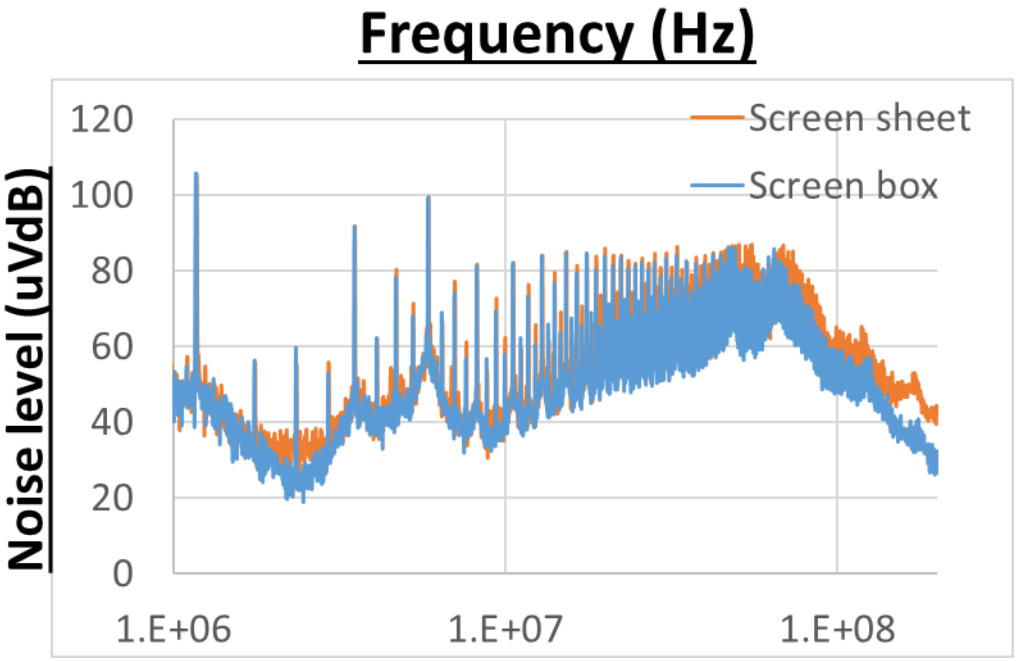


Figure 5-23 Output side DM noise comparison between a screen box and a screen sheet

5.3.2 Integrated filtering techniques

Integrated filtering arrangement within the screen box is necessary to stop high frequency propagation to the external environment. It can help confine and attenuate the electromagnetic interference within a screen box, otherwise the EMI noise would impact on surrounding components. On the top of the first intervention of screening technique, the next intervention is to add single- or multi-stage low pass filters to attenuate noise at both the output and input of the GaN converter. **Figure 5-24** shows the applied filter assemble comprising a single-stage low pass filter at the input and a two-stage low pass filer at output. A conductive copper screen layer is used to confine and attenuate radiated electromagnetic noise and to return coupled electric flux (charge) back to the switching cell. The filters used at the input side combines a 100uH inductor and 1nF capacitor to provide more than -70dB noise attenuation from 1MHz to 10MHz. An identical filter is applied at the output side combine with a second-stage low pass filter which includes 10uH inductor and 0.1uF capacitor to extend the stop band to higher frequency range. The 2-stage filter on the output side reflects the need to attenuate much higher levels of high frequency noise when compared to the input inside, because on the output side there is more high frequency noise components included in pulsating wave form. On the other hand, the input side mainly includes the DC components and some electromagnetic coupled noise through the conductive screen layer, which has much lower level of noise compared to that of the output side.

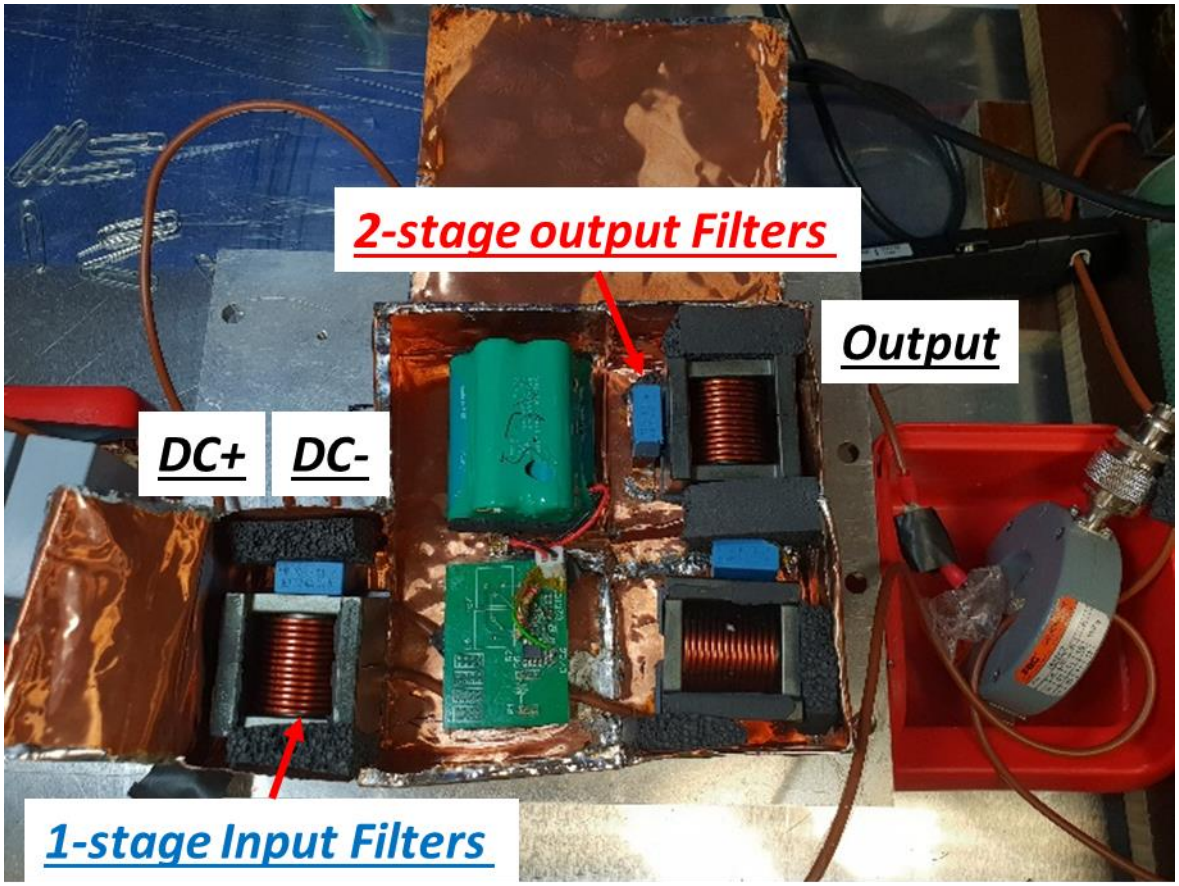


Figure 5-24 EMI measurement setup with integrated filters and screen box

In order to improve the noise attenuation at each filter stage by reducing mutual coupling between each filter stage, the 2-stage inductor components are positioned perpendicular to one another, resulting in the lowest magnetic field coupling between these two inductors. The presence of parasitic impedance in noise current return path is critical to the effectiveness of filtering techniques. Not putting noise shunting capacitors in line but positioning them in a circle surrounding the noise source ensures a short return path and low parasitic impedance. Apart from optimized filter layout, using the bottom screen layer as the noise current return path could achieve further low impedance compared to the additional current path, as described in chapter 4. Therefore, one leg of filter capacitors is directly soldered down to the bottom of screen box, then all high frequency

noise can be cycled back to the noise source through the bottom of the screen box and the bus bar connected to DC link.

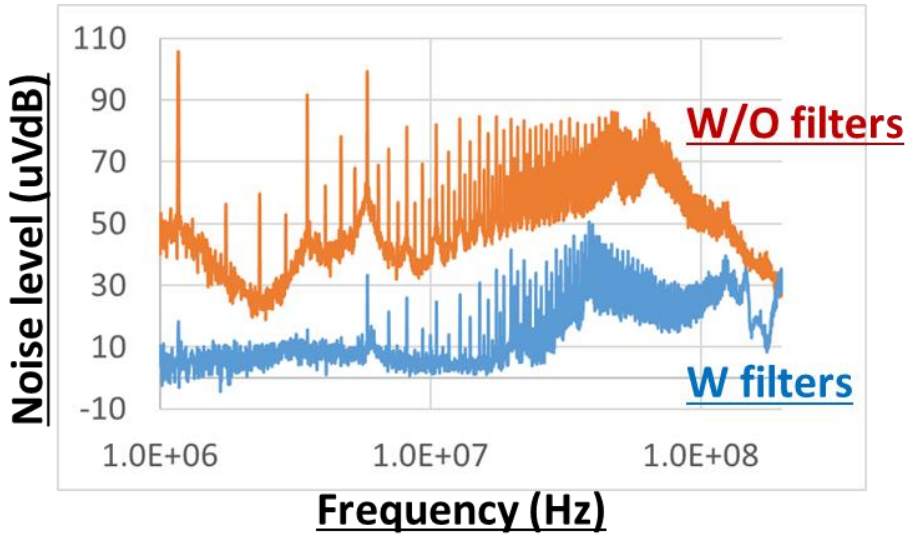


Figure 5-25 Output side DM noise comparison between with and without integrated filters

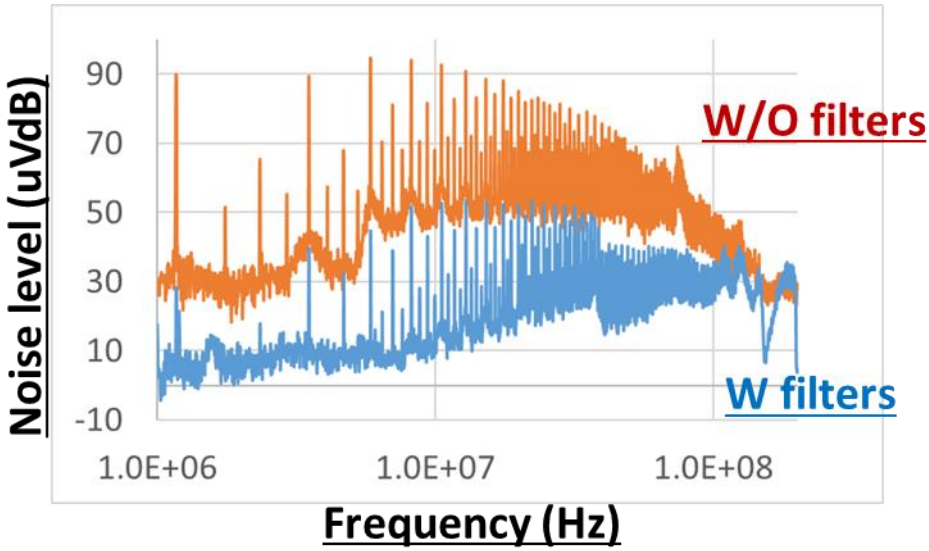


Figure 5-26 Input side CM noise comparison between with and without integrated filters

From the EMI measurement results shown in **Figure 5-25 and 26**, the combined input and output filters can achieve about 70dB noise attenuation of input side CM and 80dB suppression of output side DM at the switching frequency 1.1MHz and at the power switching harmonics. However, it has more limited impact at frequency above 10MHz due

to parasitic inductance and capacitance within the filter stages. Unintended electromagnetic coupling between filter stages and the shield layer can reduce the effectiveness of EMI suppression and let the noise couple to the load without be attenuated through the filter stages as expected at high frequencies. This result aligns well with the previous simulation and measurement of standalone filter components, described in chapter 4.

5.3.3 Partitioning techniques

To meet the requirements for higher attenuation at higher frequencies, closed conducting partitions are needed to ensure effective electromagnetic field decoupling between each filter stage. In contrast to the partial partitions, closed partition containment can stop most of electromagnetic coupling between individually screened regions.

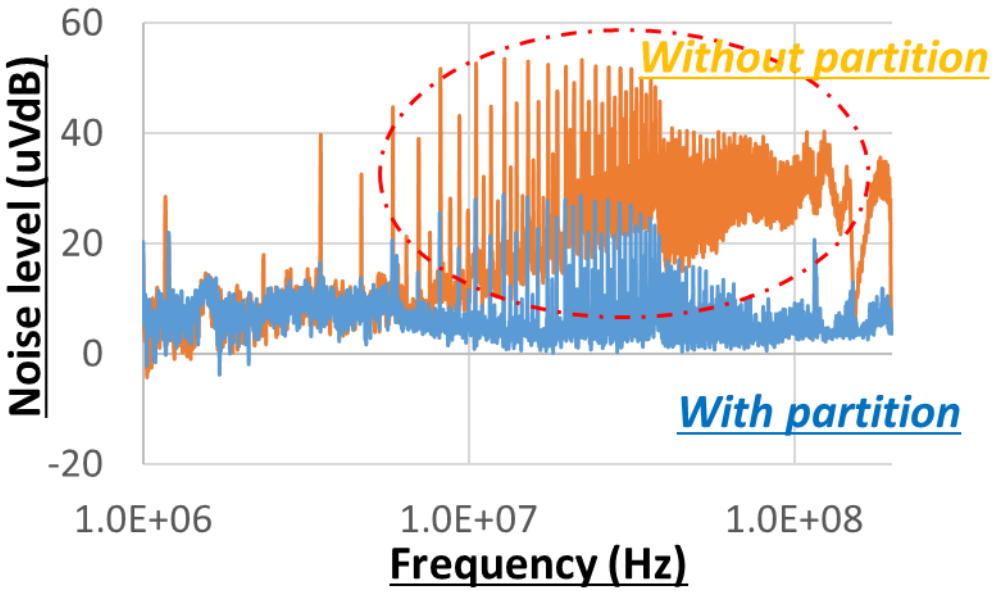


Figure 5-27 Input side CM noise attenuation comparison between with and without partition

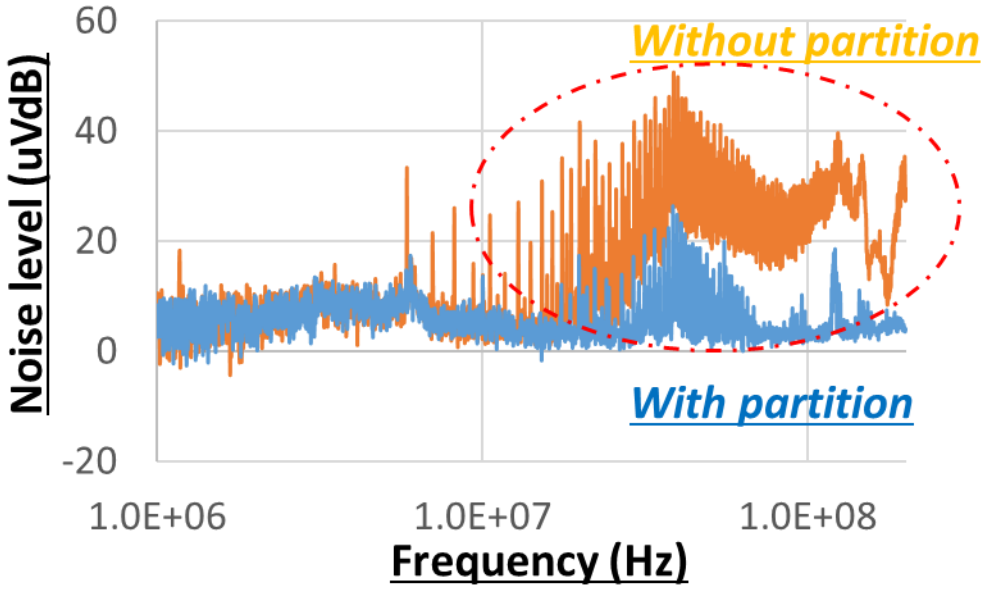


Figure 5-28 Output side DM noise attenuation between with and without partition

Figure 5-27 and 28 compare the EMI attenuation results with and without a closed partition layout. The closed partition arrangement can achieve additional 30dB improvement in conducted noise attenuation at frequencies from 10MHz to 50MHz. the level of additional noise attenuation aligns closely with the previous results obtained from the VNA frequency response and proves that a closed partition containment can very effectively limit electromagnetic coupling from the noise source to the external environment. However, as discussed above, the gaps and slots between partition layers and power traces still allow high frequency electromagnetic fields to pass through, compromising the overall filtering performance. This leaked electromagnetic field propagates along the power traces and eventually reaches the external environment. Evidence of this effect can be seen in **Figure 5-27 and 28** for frequencies in excess of 20MHz.

On the other hand, the **Figure 5-29** presents the input side DM noise attenuation comparison between with and without partition. We can see the combination of integrated filtering and screening techniques without partition already can achieve a very

low level of DM noise at the input side across the wide frequency span. There is some residual noise at high frequencies around 55MHz and above 100MHz. With the closed partitioning technique, the remaining high frequency noise is wiped out, extending the 5dBuV noise floor from 1.1MHz to 200MHz.

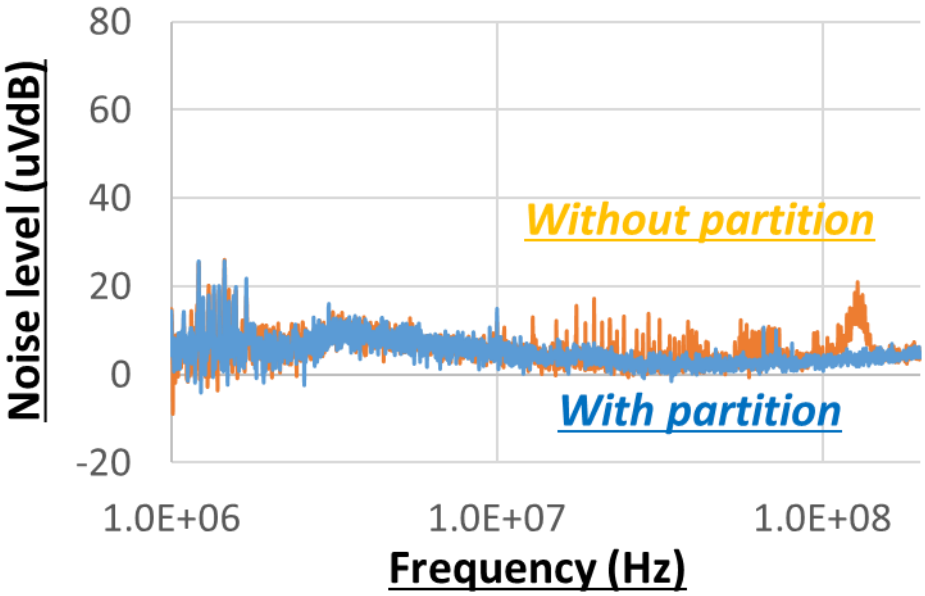


Figure 5-29 Input side DM noise attenuation between with and without partition

5.3.4 Feedthrough connection techniques

To overcome the limitations of a simple closed partition with the existing gaps and slots between the power traces and partition or shield layers, integrated feedthrough capacitors are used to fill the gaps and block electromagnetic field propagation. Feedthrough capacitors should be integrated around the power trace(s) to realise a continuous electromagnetic field blocking configuration in combination with the partition and shield layers. In this experimental setup, feedthrough capacitors are integrated around the power trace as shown in **Figure 5-30 and 31**.

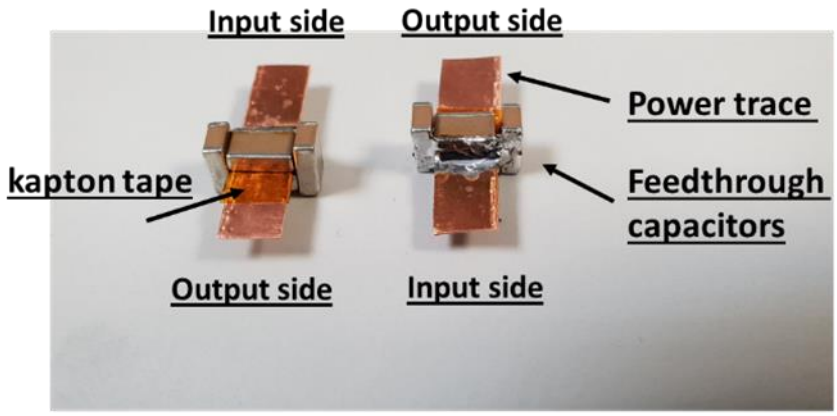


Figure 5-30 Side view of feedthrough capacitors configuration

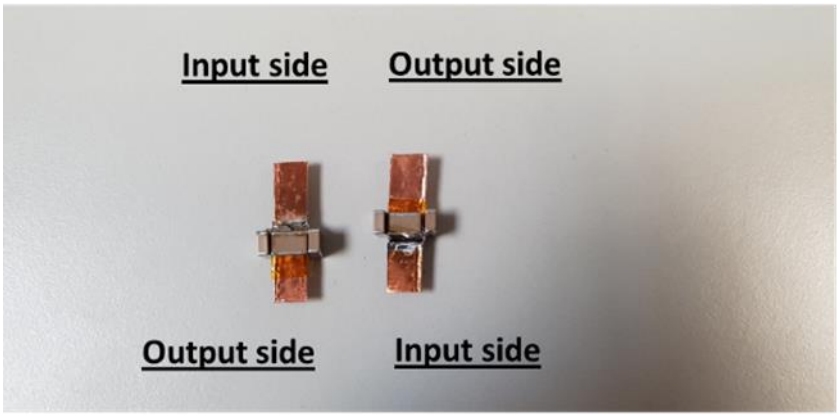


Figure 5-31 Top view of feedthrough capacitors configuration

On the output or load side, the capacitors are connected to the screen or partition layer. Kapton tape is used to provide electrical isolation between feedthrough capacitors and the power trace. On the input or source side, all capacitors are electrically connected to the power trace, such as by soldering process. **Figure 5-32** shows how integrated feedthrough capacitors and power trace arrangement is connected to partition or shield layer. The slot opened in the shield or partition layer is to accommodate the power trace. It is noted that the aperture in the shield or partition layer that carries the power trace should have the minimum possible gap around the trace to minimise the electromagnetic flux leakage from the noise source side whilst respecting electrical isolation requirements, which allow the minimum clearance to avoid partial discharge (PD). In this experiment

setup the kepton tape thickness is 65um and has more than 250kV/mm breakdown strength, which is suitable for the voltage rating in this experiment.

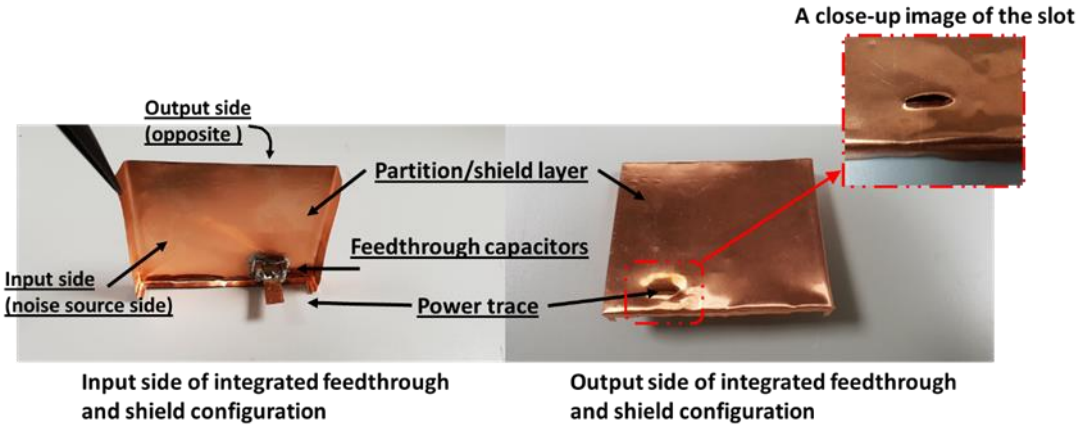


Figure 5-32 Configuration of integrated feedthrough capacitors with shield/partition layer

Figure 5-33 shows the connection of feedthrough capacitors with partition or shield layer between the first and second stage filters. On the right side is the first stage low-pass filter which is connected to the output power trace of GaN half bridge, and on the left side is the second stage filter, which is connected to the load or external terminals. Two-stage low pass filter components are used to attenuate and return unwanted low frequency noise and the combination of partition or shield layer and integrated feedthrough capacitors is used to return high frequency noise and reflect electromagnetic fields. The feedthrough capacitor configuration is a part of filtering function and shunts high frequency noise through the shield or partition layer back to the noise source. The inter-stage partition with integrated feedthrough capacitors helps to confine high frequency conducted noise and electromagnetic fields within the first stage section. Therefore, noise current is preferentially returned to the noise source (DC link), rather than able to couple to the next filter stage via parasitic couplings.

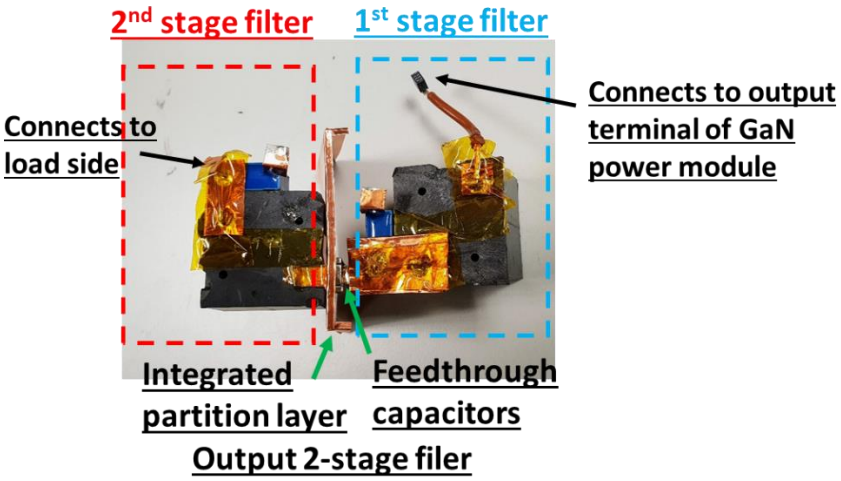


Figure 5-33 Configuration of feedthrough capactiors with patition layer and 1st stage and 2nd stage output filter

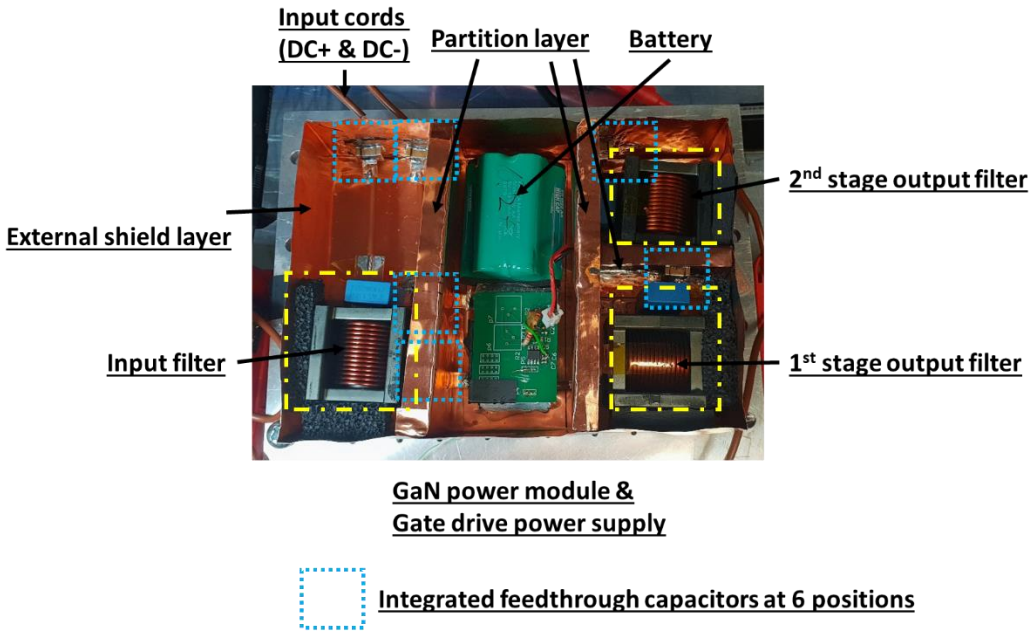


Figure 5-34 Proposed GaN power converter configuration

Figure 5-34 shows a complete arrangement including feedthrough capacitors, partitions and shield layers. The basic layout of GaN switching cell, gate derive power supply, input and output filters remains the same layout of **Figure 5-24**, but with the addition of partition layers. Partition layers are added between the input filter and the switching stage and between the output filters and switching stage. A further partition layer is

inserted between the first filter stage and second filter stage of the output filter. These internal partition layers are effective at decoupling high frequency electromagnetic fields between individual screened compartments. Where the power traces pass through external shield layers and partitions, integrated feedthrough capacitors (at 6 position, indicated by blue dot lines in **Figure 5-34**) are used to return high frequency noise and block electromagnetic field leakage between the partition or shield layer and the power trace.

Figure 5-35 shows the finished GaN power converter with all EMI interventions applied. It is noted that the top shield layer (missing in **Figure 5-34**) is connected to the remainder of the external shield layer by an electrically connection to the top shield layer to provide a continuous shielding configuration. Details of the input and output terminals, where the insulated power traces pass through the external shield layer, are shown in Figure 35.

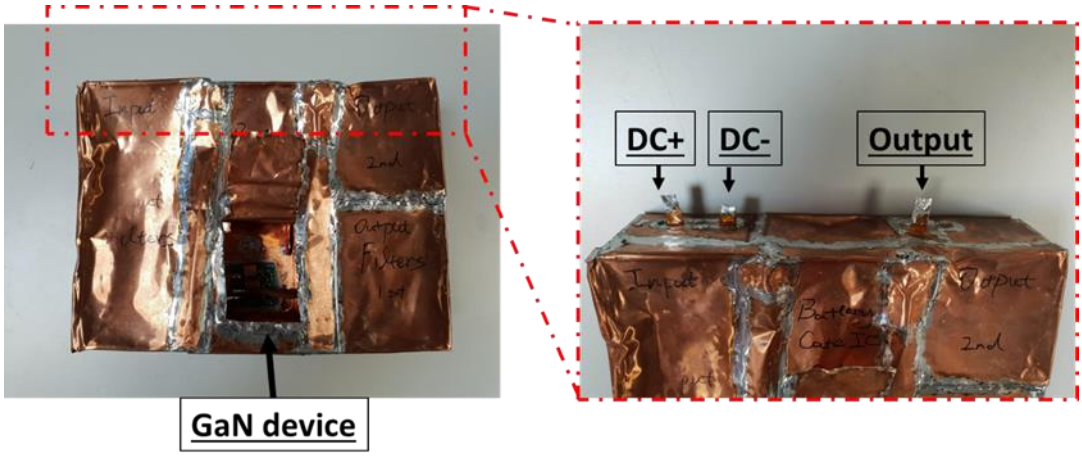


Figure 5-35 final finishing with solder top shield layer

Figure 5-36 shows a functional schematic diagram of the finished GaN converter. Red, yellow and blue areas indicated the relative intensity of high frequency electromagnetic interference from high (red) level to low (blue) level. With the partition or shield layers and feedthrough capacitors, high frequency electromagnetic interference is confined and contained within the compartment where the GaN switching cell is located. When the

power trace passes through an electromagnetic-field containment barrier, which is partition or external shield layer, the electromagnetic noise level is reduced. The closed and continuous external shield layer contains all high frequency electromagnetic fields within this converter whilst allowing DC and low-frequency power to pass through freely.

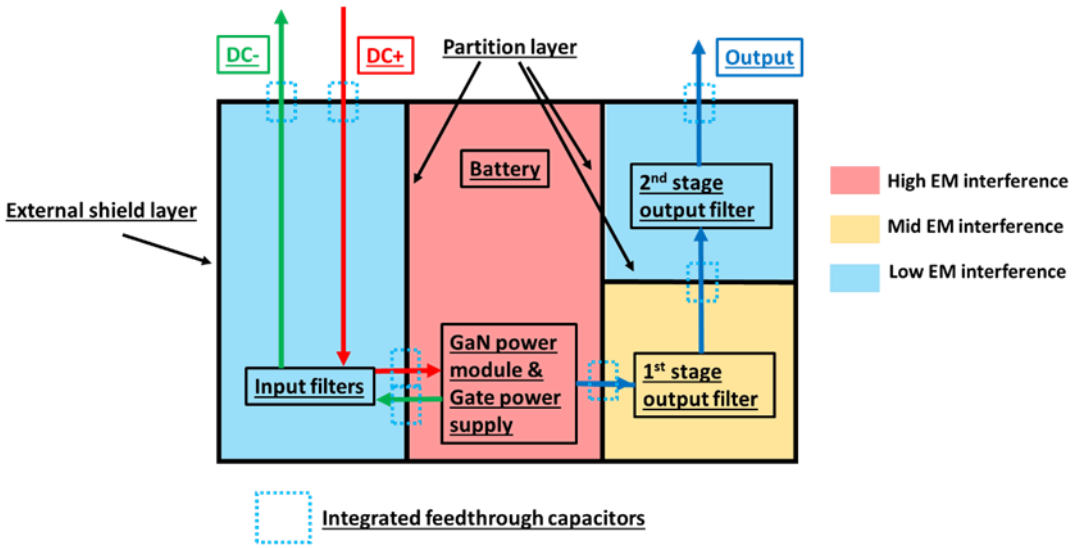


Figure 5-36 Diagram of EMI interference strength at different section within GaN power converter

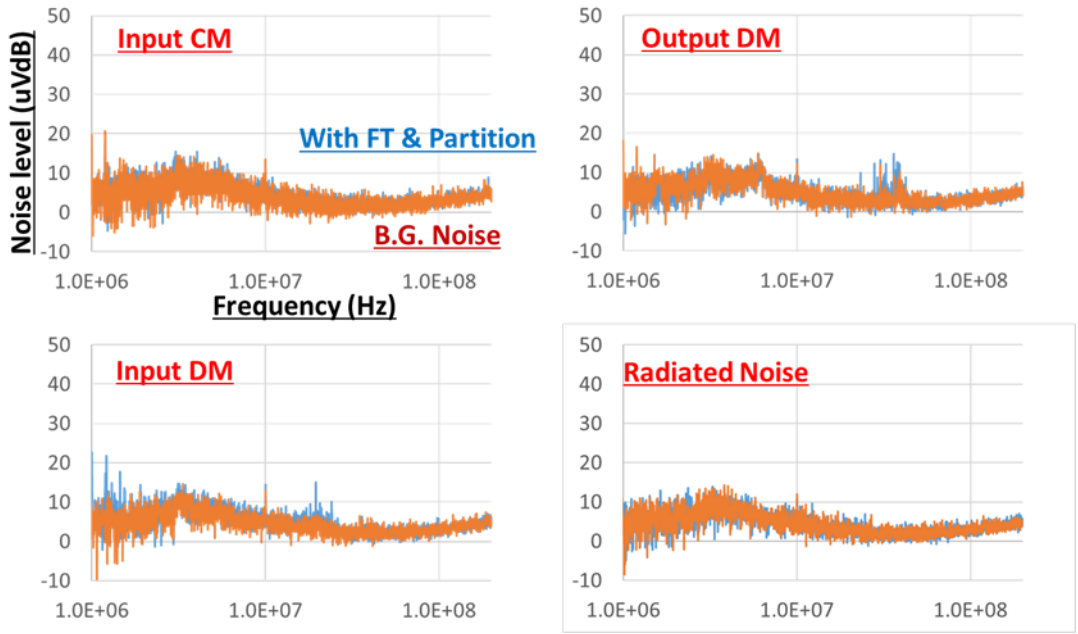


Figure 5-37 EMI measurement results of proposed configuraion

Figure 5-37 compares the results obtained from the converter with all EMI interventions applied and the background noise level. Both the conducted and radiated noise components are reduced close to or below the background noise level. These results align closely with the previous frequency response result of proposed high attenuation broad band filter and demonstrate that more than 100dB of the noise attenuation is possible across a 3-decade frequency range.

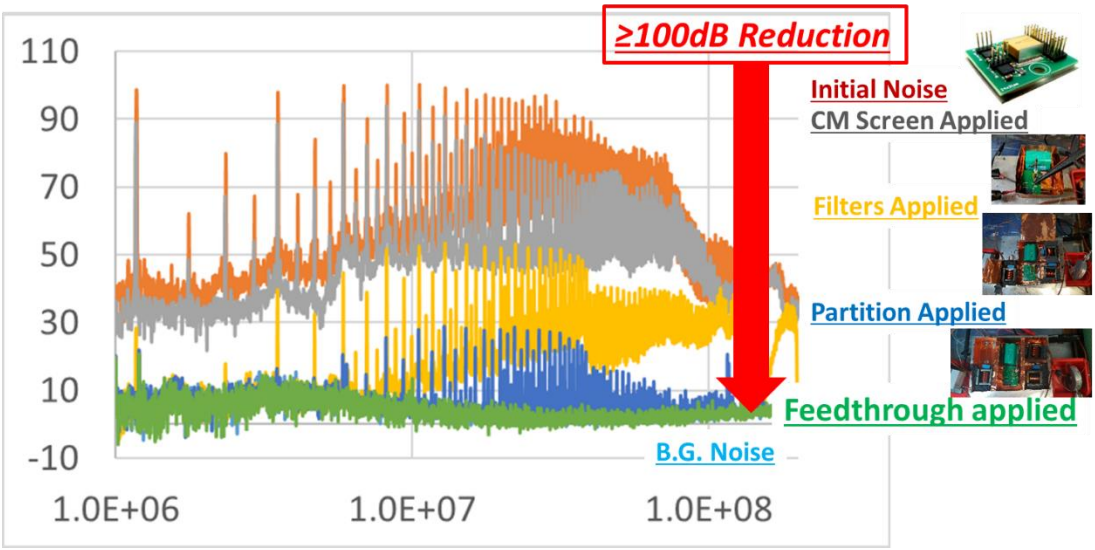


Figure 5-38 Input CM nosie reduction improvement

In the end, input CM noise reduction improvement with different electromagnetic interference interventions is shown in **Figure 5-38** as a representative example to illustrate how much impact each EM suppression technique has on the noise reduction. The closed screen box can only provide limited CM noise reduction, because internally generated noise is not contained and the screen box is only providing additional circulation path for coupled electric flux or CM current. After integrated low pass filter is applied, most low frequency noise is wiped out (yellow noise spectrum), however, it has very limited noise suppressing performance for high frequencies due to parasitic elements and mutual couplings. Feedthough and parition together help to complete the

high frequency noise containment and confinement. Eventually with all EM interventions, the noise level can be reduced significantly down to the background noise level.

5.4 Conclusion

In conclusion, by the combination of filtering, conductive shield/partition layers and EM field-blocking/reflecting capacitors, the overall performance of this EM suppression techniques can be realised with an attenuation capability of over 120dB across more than 3-decades and a stop-band extending to over 1GHz. In a GaN power electronic converter application, all conducted and radiated noise generated by switching is contained and only the intended, low-frequency power signals are present outside the converter enclosure. In addition, this same combination of interventions can act to prevent external conductive and radiative noise from penetrating the converter enclosure.

Chapter6. Summary: Silent switching

– EMI suppression without EMI filters

Electromagnetic Interference (EMI) is one major problem people have to encounter when using the fast voltage and current switching transients in power electronic applications and in addition, compliance with all relevant Electromagnetic Compatibility (EMC) standards has to be achieved before power electronic products can enter the market. In recent years, the newly emerged Wide Band Gap (WBG) device technologies such as Silicon Carbide (SiC) and Gallium Nitride (GaN), have shown a great potential to replace Silicon (Si) as the dominant technology because of their superior capabilities such as fast switching, low on-resistance, high operating temperature and high blocking voltage. In order to take full advantage of these features, advanced packaging technologies have been investigated, such as 3D packaging or laminated design to replace traditional 2D packaging design; conductive pillar connection to replace wire-bond connection; silver sintering material to replace conventional solder paste. Taken together, these technologies enable WBG devices to switch much faster, leading to higher dv/dt at switched nodes and higher di/di in current commutation loops. However, these advances come at the cost of increased EMI resulting from the transistor's faster switching speed and higher switching frequencies.

Suppression of EMI is typically achieved by a series of filters (differential and common mode) to attenuate conducted emissions and shielding to attenuate radiated emissions. Techniques involved with filtering such as modelling, layout optimization and filter integration technologies have been intensively researched, resulting in established methods for solving EMI suppression problems in conventional Si power device (e.g. IGBT) based power electronic system. However, at high frequencies, noise generates an

extended electromagnetic field along the current path, with EM fields propagating outside the conductors, a feature that is enhanced at high frequencies by the skin effect. The changing magnetic and electric fluxes from different conducting paths will interact and can generate unintended (parasitic) coupling over relatively large distances. This can compromise filter performance and cause interference. In addition, conventional EMI solutions treat the whole power electronic system as an EMI black box with suppression measures being applied retrospectively in order to meet a given standard. Techniques to contain and attenuate EMI noise at the noise source i.e. within the switching cell, have received relatively little attention.

In this research we have investigated techniques to suppress EMI at the noise source and to control EMI propagation by deliberately confining any unwanted EM fields inside a specific closed containment. Containment of EM fields is achieved by applying partial or complete conductive partitions and by embedding an electrically conductive screen layer. Common mode noise which would otherwise be capacitively-coupled to ground is returned direct to the screen. Internally generated magnetic fields are attenuated in the screen layer or in additional shielding layers whose thickness and extent are chosen to produce the desired degree of attenuation. In addition to screening and shielding techniques, differential mode filters, which feature a very broad stop band and significant level of noise attenuation are required to attenuate EMI which would otherwise propagate along the conduction paths in and out of the power electronic system.

Through a combination of simulations and measurements performed on test structures and on an active device GaN power switching module, it has been shown that a combination of filtering, conductive shield/partition layers and EM field-blocking/reflecting capacitors, can be employed to realise a broad-band filter with an attenuation capability of over 120dB across more than 3-decades and a stop-band extending to over 1 GHz. In a power electronic converter application, all conducted and radiated noise generated by switching is contained

and only the intended, low-frequency power signals are present outside the converter enclosure. In addition, this same combination of interventions can act to prevent external conductive and radiative noise from penetrating the converter enclosure.

The research has contributed new knowledge and understanding in the following specific ways:

- Introduced a new paradigm of considering and tackling EMI problems in terms of electro-magnetic field propagation and management rather than through conventional circuitry treatment.
- Introduced a new concept of EMI common-mode noise suppression by deliberately manipulating electromagnetic field couplings. Including a low impedance conductive screen layer to return capacitively-coupled CM noise directly to the noise source eliminates the need for a separate CM filter.
- Developed techniques to support the design and realisation of a broad band filter for DM noise suppression, which can provide more than 120 dB attenuation across three decades. This broad band filter can be used for various applications to effectively wipe out high frequency noise. A combination of shielding, screening, partitioning, and attenuation at feedthrough connections has been shown essential to this task.
- Demonstrated the practicality of these techniques when applied to a fast switching GaN power module, ultimately resulting in suppression of all EMI to a level below the measurement noise floor at frequencies up to 200MHz.
- Illustrated the effectiveness of the noise suppression of each intervention and provided guidelines for EMC engineers on which interventions to use to achieve the desired level of EMI suppression.

Chapter 7. Future work

- Cost-effective integration and assembly techniques: in this research, electromagnetic interference containments and partitions are made of copper sheet and its manufacture process is hand-made soldering assembly. To achieve high efficiency and cost effective process, advanced integration process need to be investigated, where vertical partition layer and feedthrough connection can be built easily in the process. 3D laminated layout would be a good option for this achievement. All power electronic components including power devices, input and output filters, partition, feedthrough connectors and gate control circuits are constrained within laminated substrates. An external closed and continuous conductive layer works as the shield and/or screen layer to attenuate conducted and radiated EMI noise.
- Further measurement on power losses: a portion of EMI noise energy is dissipated in the shield layer where the shield layer is used to reflect and absorb near-field radiated noise; in the screen layer due to the skin effect, where the screen is used to return CM noise current back to the noise source. Also there is some power lose within magnetic filter components. In other words, EMI confinement and suppression performance comes with some compensation of power losses within the system. All these power loses need to be confirmed and validated through EM software Maxwell 3D, and physical measurements.

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