

University of Nottingham

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

SiC-Based Power Electronics for Wind Energy Applications

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Abstract

The aim of the thesis is to investigate and assess the benefits of SiC power devices on wind inverter topologies for low and medium voltage grid connections in terms of power losses and efficiency under different conditions, i.e. various power loading, different switching frequencies and different heat-sink temperatures. The thesis also proposes and develops solutions for maximum exploitation of the potential benefits of SiC technology in wind energy applications.

The comparison between Si and SiC devices is established for a particular case of wind applications; the compared efficiency versus the wind distribution allows to determine the advantages of SiC-based solution. The static and dynamic characterizations of the 1.2 kV SiC MOSFET power module are carried out to allow determining the impact of different operating parameters over the device performance. The evaluated module is used for the design of a three-phase inverter for wind application referring to some behavioural features of SiC devices and specific operating conditions of wind turbines. A bespoke design for the three-phase inverter is presented to inverter performance and power density by joint electro-thermal and electro-magnetic design optimization of the wind inverter. Finally, the knowledge gained in low voltage SiC devices is transferred to the high voltage ones, especially 3.3 kV SiC MOSFET; these devices not yet commercially available at the time of writing, but promising to become a key SiC component in the near future.

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Lastly, but definitely not the least, I like to express all of my sincere and appreciated thanks to my parents, my brothers and my sisters for encouraging me during my doctoral period. Besides, I like to express my greatest gratitude to my wife Aisha, my daughters Omaima, Sarah and Raghed, and my sons Ibrahim and Muhammad for their invaluable encouragement and support during my study.

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Preface

This preface describes the main contributions of the thesis and a list of publications of the author is reported.

Main contribution of the thesis

Emerging innovative SiC power semiconductor devices bring more efficient and reliable power electronics conversion systems for renewable energy. This thesis aims to assess the benefits of SiC MOSFETs at 1.2 and 3.3 kV blocking voltage classes and to develop solutions for maximum exploitation of the potential benefits of SiC technology in this application. In addition, this thesis delivers a proof-of-concept demonstration of the proposed solutions with best-in-class performance (efficiency and power density).

The first contribution of this thesis is the evaluation of the benefits of 1.2kV/20A SiC MOSFET six-back power module (CCS020M12CM2 from Wolfspeed [1]) to a 12 kW wind inverter in small-scale wind turbines connected to low voltage (LV) distribution grid. In particular, the assessment of power losses and efficiency under different conditions, i.e. various power loading, different switching frequencies and different heat-sink temperatures was performed. The results show that SiC devices can be used to enable higher switching frequencies and operational temperatures, yielding in a significant reduction in magnetic and heat-sink volume and weight, without penalty on efficiency.

One important result that was found was that the maximum value up to which it makes sense to increase the heat-sink temperature is limited at about 250-255^oC; beyond this value, the increase in semiconductor losses becomes a limiting factor and no further heat-sink volume shrinkage is viable. This result based on a physical semiconductor device model validated up to a representative high temperature values.

The second contribution presents joint electro-magnetic and electro-thermal design optimization of the inverter, referring to some behavioural features of SiC MOSFETs and specific

operating conditions of wind power conversion applications. With the aim of maximizing the power density of the inverter, a trade-off between the efficiency and power density are taken into account. The inverter efficiency is maximized by varying the switching frequency as a function of the wind speed distribution, given an increase in annual energy delivery to the grid results, without compromise on the maximum achievable power density.

The final contribution of this work is the assessment of state-of-the-art 3.3 kV SiC MOSFET to be used in medium voltage (MV) wind energy application; the assessment includes the static and dynamic characterization. It is shown clearly that the 3.3 kV SiC MOSFET with the availability of body-diode has the capability to replace existing counterpart Si IGBTs that come with an external diode to achieve a higher power density and a superior performance multi-chip module. The dynamic performance of a 3.3kV SiC MOSFET and body-diode with parallel chips indicates the devices can be used well in parallel operation and achieve power sharing even during fast transient events.

List of publications

- **A. Hussein**, A. Castellazzi, P. Wheeler and C. Klumpner,"*Performance benchmark of Si IGBTs vs. SiC MOSFETs in small-scale wind energy conversion systems*". Power Electronics and Motion Control Conference (PEMC), 2016 IEEE.

- **A. Hussein** and A. Castellazzi,"*Optimization of thermal management and power density of small-scale wind turbine applications using SiC-MOSFETs*". Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia).

- B. Mouawad, **A. Hussein** and A. Castellazzi,"*A 3.3 kV SiC MOSFET Half-Bridge Power Module*". Proc. CIPS2018, Stuttgart, Germany.

- **A. Hussein**, B. Mouawad and A. Castellazzi,"*Dynamic performance analysis of a 3.3 kV SiC MOSFET half-bridge module with parallel chips and body-diode freewheeling*". 2018 IEEE 30th International Symposium on Power Semiconductor Devices.

- Y. Zeng, E. Gurpinar, **A. Hussein** and A. Castellazzi,"*Experimental demonstration of an optimised PWM scheme for more even device electro-thermal stress in a 3-Level ANPC GaN inverter*". PEMD2018, Liverpool, UK.

- Y. Zeng, **A. Hussein** and A. Castellazzi,"*Individual device active cooling for enhanced system-level power density and more uniform temperature distribution*". 2018 IEEE 30th International Symposium on Power Semiconductor Devices.

- **A. Hussein** and A. Castellazzi,"*Variable frequency control and filter design for optimum energy extraction from a SiC wind inverter*". IPEC2018, Niigata, Japan.

- A. Castellazzi, A. Fayyaz, E. Gurpinar, **A. Hussein**, J. Li and B. Mouawad,"*Multi-Chip SiC MOSFET Power Modules for Standard Manufacturing, Mounting and Cooling*". IPEC2018, Niigata, Japan.

- A. Cheraghinezhad, **A. Hussein** and A. Castellazzi,"*Parametric study of optimum gate-resistance for performance and short-circuit robustness of novel half-bridge IGBT modules*". ESARS-ITEC Europe 2018, Nottingham, UK (In Press).

- **A. Hussein** and A. Castellazzi,"*Comprehensive design optimization of a wind power converter using SiC technology*". icSG2018, Japan.

Chapter 1

Introduction

This chapter reviews the global developments and markets of the wind energy sector, and then introduces SiC power electronics technology in wind energy applications. Finally, the thesis outlines and the content of each chapter are presented.

1.1. Wind energy and power electronics developments

Due to the increased awareness for the need for reduced carbon emission energy resources, the demand for renewable energy has been increasing. Due to an increase in energy demand and the limited amount of fossil fuels, there has been an increased demand on wind based electricity generation around the world, competing with fossil and nuclear fuels [2]. The amount of global installed wind energy has been increasing rapidly, with total installed capacity jumping from 23.9 GW in 2001 to 539.123 GW by 2017, as Fig. 1.1 presents. The reasons for the increase of wind energy penetration for electricity generation are the maturing of the industry and the reduction in wind turbine price [3].

Power electronics have become widely used for wind energy conversion systems to improve the overall system performance in terms of efficiency, reliability and reduced cost. Wind turbines equipped with a squirrel cage induction generator (SCIG), connected directly to the grid, were very common in the 1980's with a maximum capacity of 50 kW. By developing power converter technology in the 1990's and 2000's, the rating and size of wind turbines have been grown fast to reach 7.5 MW capacity in 2011 and 10 MW wind turbine by the year 2018, as Fig. 1.2 shows [4].

In the past few decades, there have been significant advances in power semiconductor device fabrication. While silicon (Si) is still the most widespread material for the main substrate, the development of Si semiconductor technology has almost achieved its limit for the current and future market demands. The reasons for this are that Si power electronics suffer from slow

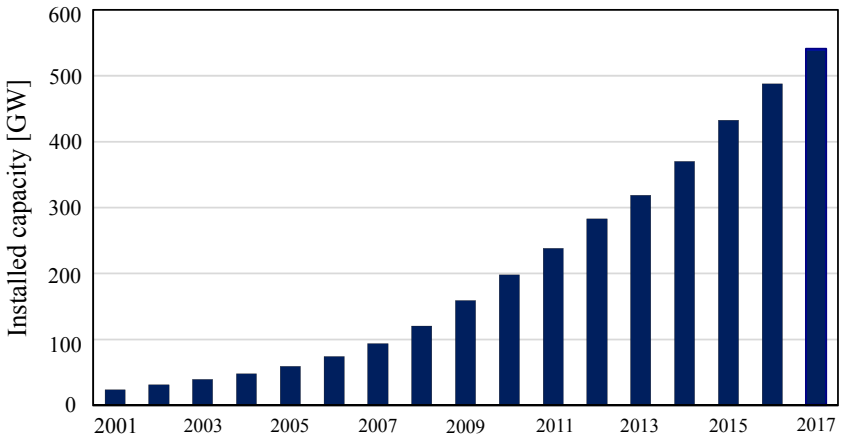


Figure 1.1: Global cumulative installed wind capacity 2001-2017 [3].

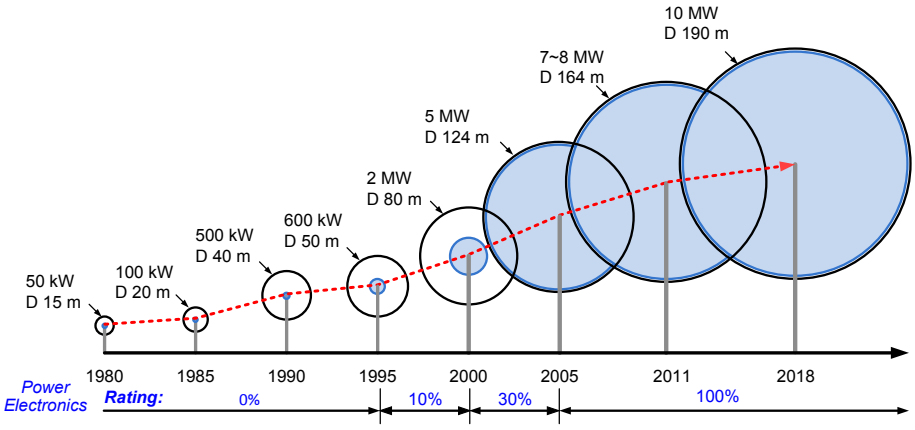


Figure 1.2: Wind turbines development and the main trend of power electronic conversion system [4].

switching transitions, relatively high on-state resistance and conduction losses at high voltage blocking classes and temperature dependency characteristics [5–7].

Silicon carbide (SiC) technology is favoured beyond the capabilities offered by Si devices for use in power conversion applications. From Fig. 1.3, the main advantages of SiC power devices compared with Si are as follows: [5–7]

- Very fast switching speeds (factor of 10 over Si IGBTs); this feature enables a straightforward increase of the switching frequency, and thus reduces the size and cost of the passive components and improves the system dynamics.
- Availability of built-in diode with possible synchronous rectification, which leads to reducing the semiconductor area and the cost of the external diode.
- Smaller thermal resistance (nearly three-fold value compared to Si IGBTs); this contributes to increase the device power density or decrease the device operational temperature.

- Very good temperature stability, which results in reducing the converter cooling requirements and pushing the converter to operate in a harsh environment, where Si devices could not perform well.

- Excellent power scaling, thanks to its parallel-ability.

The production and long-term costs of wind inverters become less expensive by replacing Si IGBTs with SiC MOSFETs. SiC devices brought an improvement of the system efficiency up to η_{Euro}=2.36% in comparison with Si devices [8]. If the trend of wind energy growth is continues at the same rate as shown in Fig. 1.1, it is expected that the accumulated installed capacity will be about 860 GW by 2027. Replacing Si devices with SiC devices will lead to money saving up to 13 B£ (by considering feed-in tariff of 0.12 £/kWh and load factor of 38.9% for offshore wind turbines [3]). More financial benefits can be gained by reducing the production cost of inductive components and heat-sink by employing SiC devices [8].

If SiC devices are used in wind energy application, taking into consideration the benefit of increasing the overall system efficiency and power density rather than focusing only on individual device cost, SiC devices will definitely enable more efficient, reliable, high power density, low overall cost and thermally stable power converters. However, SiC technology still shows limitations to its maximum exploitation, particularly in terms of power density, high temperature, parasitic inductance and common mode noise at higher switching frequencies, due to lack of suitable packaging for SiC devices [5].

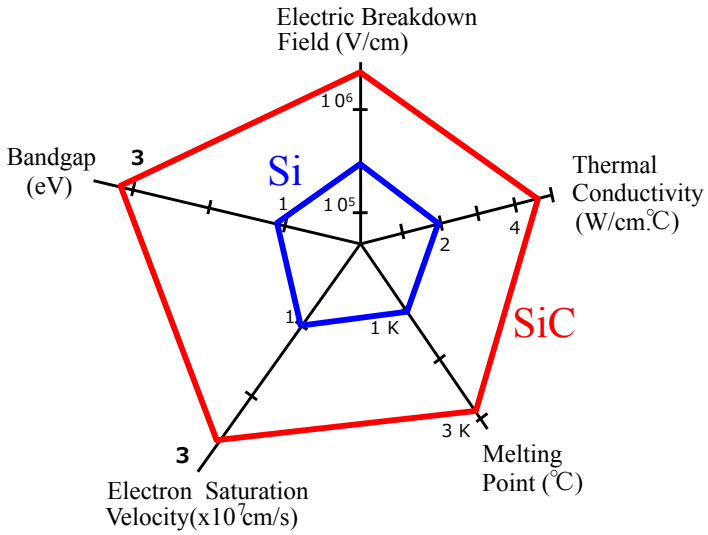


Figure 1.3: Material properties of SiC devices versus Si.

Applications of SiC devices in wind energy conversion systems have been already discussed in the literature. In [9], the performance of SiC MOSFET is evaluated for a 1.5MW

wind turbine two-level back-to-back converter topology. The converter is assumed to be composed of ten SiC-based converters that each use twenty 1.2kV/10A SiC MOSFETs for a power rating of 150 kW each in a simulation. The results show that replacing Si-IGBT with SiC-MOSFETs can bring up to 4.3% average efficiency gain over a range of wind speeds from 6 m/s to 11 m/s for the 3 kHz switching frequency, and a reduction in heat-sink size due to the low power losses achieved.

In [10], a SiC JFETs-based generator-side two-level power converter (less than 40 kW) for the small-scale wind turbine was investigated in an experimental setup with a three-phase squirrel cage induction generator (SCIG), in which the high switching frequency (greater than 100 kHz) reduces the generator-side passive filter size. In [11, 12], an efficiency improvement in NPC three-level inverter in 3.3 kV and 2.3 MW wind turbine was achieved by just replacing Si diode with SiC Schottky in the clamping diode location. A single phase NPC inverter with 4500V/1200A Si IGBT and 800 A Si diode (20×40 A SiC-Schottky) was investigated in simulation and experimental setup. An improvement of efficiency gains of 0.5% to 1.5% was observed. [13] designed qZS-derived push-pull DC/DC converter in the boost stage of small-scale wind conversion system based on SiC MOSFETs. Experimentally obtained results showed that the converter with SiC MOSFETs has superior efficiency over Si-IGBTs (2.5-5.2% higher) at all corresponding operating points of the case study.

However, in recent studies, some specific behavioural features of SiC MOSFETs and the intermittent nature of wind speed are taken into account for the design and evaluation of wind inverters, where in [14], a 12 kW 2L 3-phase inverter for small-scale wind turbines was evaluated; the efficiency and energy production study shows that SiC MOSFETs can solve the issue with the existing inverters based on Si IGBTs in terms of limited extracted power from wind turbine at partial loads in the region of high wind speed distribution. This results in saving in lost energy up-to 75% by replacing Si with SiC devices.

Moreover, in [15], focusing on the very stable performance of SiC MOSFETs over a broad temperature range: designing the cooling system for nominal operational conditions, typically corresponding to a much lower than maximum power rating in the region of highly probable wind conditions results in a significant increase of the converter power density without destroying the efficiency. In [16], the authors propose to maximize the energy yields of SiC wind inverter by optimising the low-load efficiency, which corresponds to the most frequent operational condition in time, by varying the switching frequency; about 51% saving in the lost energy was achieved. In addition, [17] proposes the joint electro-magnetic and electro-thermal design optimization of a three-phase two-level voltage-source inverter, referring to the specific operational conditions of wind power conversion applications. the paper focuses on the salient features of SiC and discusses their impact on system performance, elaborating on the associated bespoke design needs to yield optimum results in terms of inverter performance and power density. More advanced, in [18, 19], the knowledge of SiC devices at low voltage

was transferred to high voltage ones, especially 3.3 kV SiC MOSFETs for wind applications.

1.2. Research objectives

The objective of this work is to investigate and assess the potential utilization of using SiC devices technology on the design and performance of highly efficient and power dense wind power inverters.

In this thesis the following aspects are considered:

- Performance benchmarking of SiC MOSFETs and Si IGBTs at 1.2 kV blocking voltage class for 2L 3-phase wind inverter. The comparison includes efficiency and energy production, switching frequency performance, temperature stability and thermal stress.
- Parametric characterization of 1.2 kV six-pack SiC MOSFET power module; the characterization includes the conduction and the switching characteristics of the MOSFET and its parallel Schottky diodes under a wide range of operating conditions (i.e. baseplate temperature, load current and gate drive resistors).
- Evaluation of the performance of wind inverter topology based on SiC MOSFETs at 1.2 kV blocking class in terms of power losses, efficiency, thermal capability and non-unity power factor operation.
- Optimized inverter design based on some specific behavioural features of SiC MOSFETs and the intermittent nature of wind speed, with the aim of maximizing the inverter performance and power density.
- Transfer of knowledge gained about low voltage SiC devices to higher voltage levels, especially 3.3 kV MOSFET in wind energy applications.

1.3. Outline of the thesis

Hereafter, the contents of each chapter of the thesis are briefly described:

Chapter 2 reviews wind turbine systems and their wind inverter topologies. It also covers the international standards for integrating power electronics inverters into the AC grid. This chapter ends with SiC versus Si simulation based benchmarking in a 2L 3-phase wind inverter topology.

Chapter 3 discusses the properties of SiC material and state-of-the-art diodes and controlled devices. After that, the conduction and switching characterization of a 1.2 kV six-pack SiC MOSFET power module under different operating conditions are presented.

Chapter 4 presents an evaluation of SiC MOSFETs in the wind inverter. The overall analysis under different conditions, i.e. various power loading, different switching frequencies and heat-sink temperatures are detailed. In addition to this, the reactive power handling feasibility was demonstrated as well at non-unity power factor inverter operation.

Chapter 5 highlights the optimized design for a wind inverter. This chapter starts with the bespoke design of the wind inverter cooling system, and then the concept of variable switching frequency is applied. Finally, a proof-of-concept demonstration of the designed wind inverter with best-in-class performance (efficiency and power density) was delivered.

Chapter 6 explores the potential benefits of SiC power devices at higher voltage levels, especially 3.3 kV MOSFET. This chapter starts with a review of HV SiC MOSFET power devices, and the review is followed by a detailed parametric characterization of a 3.3 kV SiC MOSFET half-bridge module with parallel chips and body-diode freewheeling. Lastly, the performance of 3.3 kV based wind inverter in high power wind application was analysed and presented.

Chapter 7 has conclusions and recommendations for future work.

Chapter 2

Wind Turbines and Grid-Connected Inverters

This chapter gives an overview of wind turbine systems; a comparison of different wind turbine speed control concepts; and discusses different converter topologies for low and medium voltage grid connections. It also covers the international standards for integrating power electronics inverters into the AC grid. State-of-the-art two-level three-phase wind inverters have been presented and simulated with SiC-MOSFET and Si-IGBT devices; the results show that SiC inverter can achieve higher performance at low loads in the region of high wind speed distribution, and hence can maximize the energy extraction from wind turbines. The comparison also shows that SiC-MOSFETs exhibit superior switching performance, stable temperature performance and less thermal stress over Si-IGBTs.

2.1. Wind power system

The power content of the wind in form of kinetic, P_w, described as per (2.1) is proportional to the air density, ρ, the cube of wind speed, v, and the blade sweep area πr^2, where r is the blade radius. The turbine power coefficient, C_p is defined by the efficiency of the turbine in converting the power available in the wind to the turbine power, P_{out} as shown in (2.2), and typically has a maximum value of 59% known as Betz limit. C_p is a function of the tip speed ratio, λ, which relates the turbine blade speed to wind speed as expressed by (2.3) and (2.4), where ω is the turbine angular velocity [20].

$$P_w = \frac{1}{2}\rho\pi r^2 v^3 \tag{2.1}$$

$$P_{out} = C_p \times P_w \tag{2.2}$$

$$C_p = f(\lambda) \tag{2.3}$$

$$\lambda = \frac{\omega r}{v} \tag{2.4}$$

The optimum tip speed ratio, λ_{opt}, is one of the important parameters for assessing the performance of wind turbines. The optimum tip speed ratio is a function of the turbine blade speed; too slow a rotation of wind turbine rotor means that the tip speed ratio is low and the wind will pass through the space between turbine blades. As a consequence, the turbine generates very low power. However, if the tip speed is high due to the too fast rotor, the turbine blades act as a solid wall to the wind. Therefore the optimum tip speed ratio should be designed well in correspond to the maximum extraction of wind power. At the optimum tip speed ratio, the wind turbine has the maximum power coefficient, $C_{p,m}$ [21, 22].

Fixed speed wind turbines use the maximum power coefficient, $C_{p,m}$ at one particular wind speed and lower values of the power coefficients are observed at other wind speeds; therefore they yield poor wind energy extraction from the turbine. On the other hand, if the wind turbine speed can be adjusted with reference to the wind speed, the $C_{p,m}$ can be achieved at different wind speeds which means the turbine works under maximum power point tracking (MPPT), and therefore, maximum wind turbine energy can be extracted from the source, especially at low wind speeds, as Fig. 2.1 shows [20].

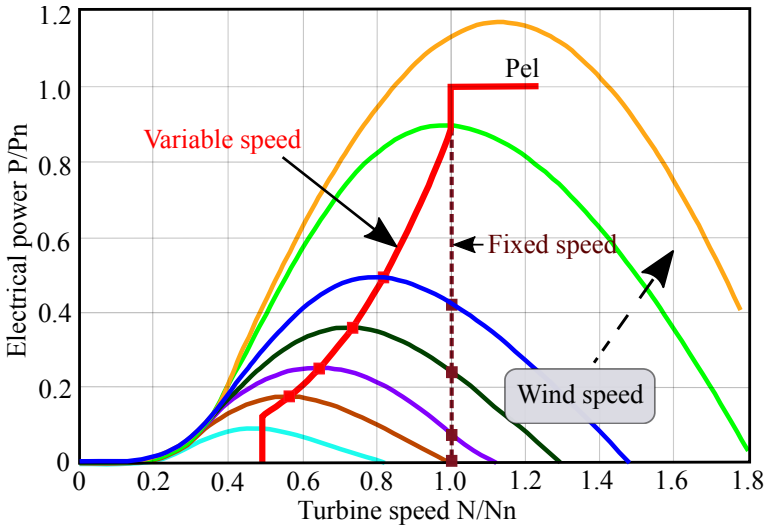


Figure 2.1: Wind power capture: fixed vs variable speed wind turbine.

2.2. Wind turbine speed control concepts

According to speed control ability, wind turbines can be subdivided into the following categories.

2.2.1. Constant speed wind turbine

This configuration was developed and used in 80s and referred to as the Danish concept. As shown in Fig. 2.2, the wind turbine is equipped with a squirrel cage induction generator (SCIG) operated at a constant speed determined by the frequency of the grid regardless of the wind speed. This structure is suited to direct grid connection since the SCIG is supplied by grid reactive power. The power converter in this configuration is a soft starter, and the capacitor bank is to compensate reactive power demand by the asynchronous generator in case of voltage fluctuations at the point of grid connection. This configuration is very cheap and easy to build. However, the main disadvantages of this configuration are: no speed control; requires a strong grid to avoid unstable output voltage due to wind speed fluctuations; and needs high mechanical construction to overcome the problem of torque pulsations due to wind gusts. An improvement of this concept is made by introducing an adjustable soft starter based on a resistor fitted on the rotor. However, power losses in the rotor resistance are clearly a drawback [4, 23, 24].

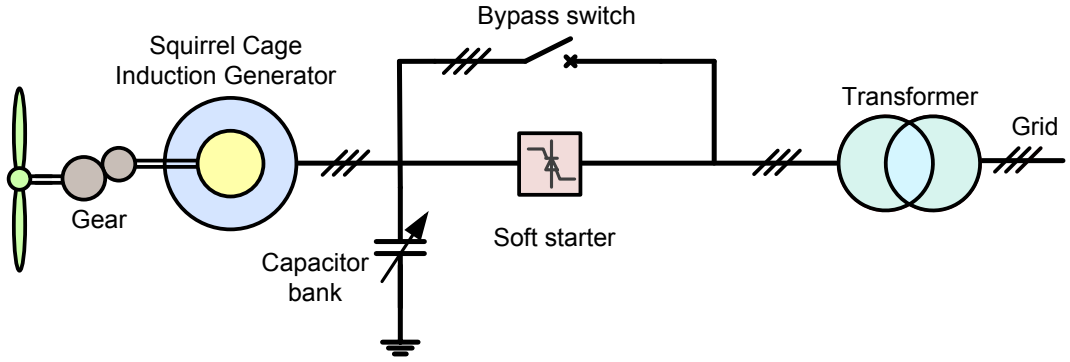


Figure 2.2: Fixed speed wind turbine system.

2.2.2. Variable speed wind turbine with slip power converter

This technique is known as the doubly fed induction generator (DFIG) concept. As shown in Fig. 2.3, the stator winding is connected directly to the grid to deliver the bulk power to the grid, while the rotor winding is connected through a small-scale frequency converter with a typical rating of around 30% of wind turbine capacity. The small converter controls the frequency and the rotor current, and thus variable speed operation can be satisfied. In this type of configuration, a step-up transformer is required between the converter and grid to match the voltage ratio between the stator and rotor of the generator. The advantages are that this

configuration is more economical due to smaller converter rating, and the converter acts as a reactive power compensator and soft starter. However, the use of slip rings and insufficient power controllability in case of grid faults are the main disadvantages [4, 23, 24].

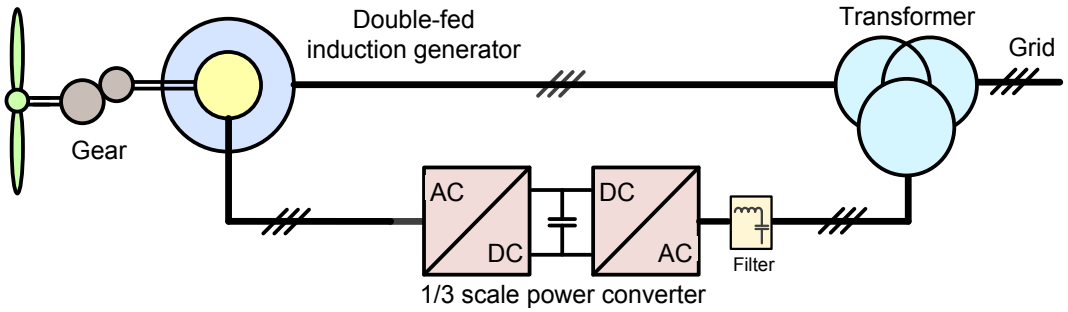


Figure 2.3: Variable speed WT with slip power converter [4].

2.2.3. Variable speed wind turbine with full-scale power converter

In this configuration as shown in Fig. 2.4, all the generated power is delivered to the grid through a full-scale frequency converter. This structure uses the wound rotor synchronous generator (WRSG) or permanent magnet synchronous generator (PMSG). The full-scale converter solution offers some advantages over DFIG structure: full speed and power control, elimination of slip rings and possible elimination of the gearbox by using synchronous generators. In addition, the use of a full scale converter allows eliminating the bulky step-up transformer by increasing the converter output voltage levels, which is an attractive solution for future Mega-Watt (MW) wind turbines. As for disadvantages: more stress upon power electronics devices in the full-scale power converter and the use of the permanent magnet (PM) adds extra cost to the system [4, 23, 24].

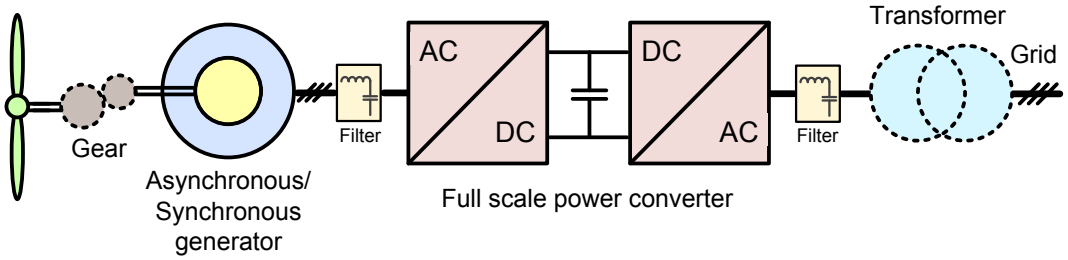


Figure 2.4: Variable Speed WT with full scale frequency converter [4].

2.3. Grid converters for wind energy

The AC-AC power electronics conversion system in wind turbine systems can be direct or indirect. Indirect conversion, in which there is a DC-link capacitor connecting two converters performing AC-DC and DC-AC conversion, is more popular than the direct conversion. The indirect conversion provides decoupling between grid and generator, and thus compensates the non-symmetry and power quality issues and supports the grid during the low-voltage ride-through transient. On the other hand, direct conversion such as matrix converters performs AC-AC conversion without intermediate energy storage. This conversion system offers some advantages, such as less thermal loading stresses and better power quality in comparison with two-level back-to-back VSC topology. However, it needs a higher number of components, more complex control and more complex grid filter design [25]. So that, here reference is made to the indirect conversion topologies.

2.3.1. Two-level unidirectional voltage source converter (2L-UNI)

This topology is a full-rated power converter topology used for wind turbines with permanent magnet synchronous generator (PMSG) which has high torque density, overload capability, low maintenance and there is no need for reactive power supplying the machine [4, 26]. The power flows in one direction from PMSG to grid through power converters. The advantage is a low-cost solution because a simple diode rectifier can be used on the side of generator [4]. However, diode rectifiers generate low-frequency pulsation that may cause shaft resonance [27].

As shown in Fig. 2.5, a boost dc-dc converter is used to boost the DC-link voltage at low wind speeds [25]. The dc-dc converter is used to control the wind turbine speed in a way that the peak of power coefficient C_p and consequently the maximum output power of the wind turbine is obtained. The boost converter allows the maximum power extraction from the source even at low wind speeds, and thus they operate at MPPT conditions.

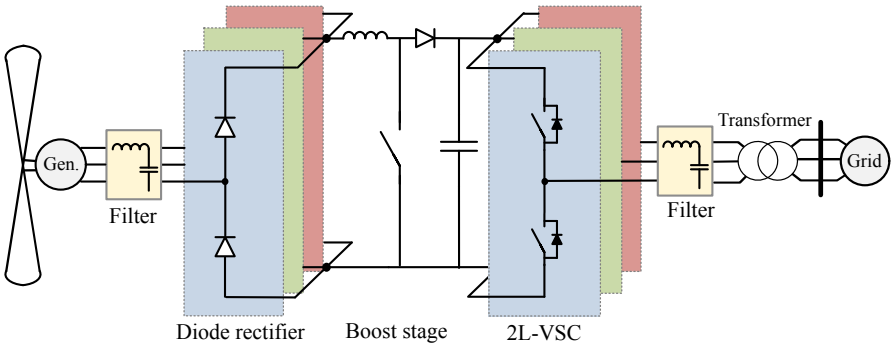


Figure 2.5: Two level unidirectional voltage source converter for wind turbine [4].

2.3.2. Two-level back-to-back voltage source power converter (2L-BB)

The two-level back-to-back structure (2L-BB) shown in Fig. 2.6 is the most widely used three-phase converter topology so far as the interface between generator and grid in wind turbine systems up to 2 MW. This topology can be a full-scale power converter topology for wind turbines with squirrel-cage induction generator or partial-scale power converters in the case of DFIG. This structure offers four quadrant operation capability with a simple structure and few components [4, 25].

However, the 2L-BB topology suffers from high power losses and thus lower efficiency when used with MW wind turbines. It uses semiconductors with full DC-link blocking voltage, so that, the available semiconductor might need a series connection, yielding to a complex control and issues with voltage imbalance. Another disadvantage is the only two voltage levels at the converter output which causes a high dv/dt stress to the magnetic elements, and thus bulky filter is required to limit the voltage gradient and to reduce the harmonic distortion [4].

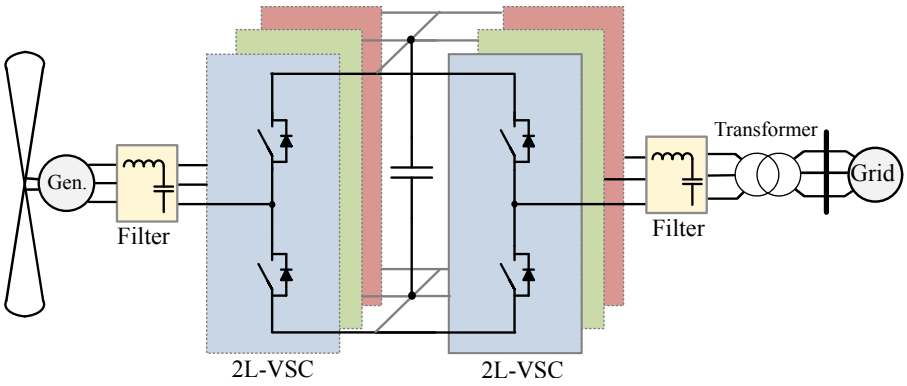


Figure 2.6: Two level back-to-back voltage source converter for wind turbine [4].

2.3.3. Three-level neutral point diode clamped topology (3L-NPC)

This topology is one of the most commercialised converters in case of power level over 2 MW. It has back-to-back configuration similar to the 2L-BB as shown in Fig. 2.7. This structure enables the use of semiconductor devices with a lower blocking voltage - potentially only half the rated DC-link voltage. In addition, this is one more output voltage level and consequently less dv/dt stress, thereby smaller filter size is required compared with two level converters for the same power and voltage levels [4,28,29]. For the same harmonic requirement, the switching frequency of a multi-level converter can be reduced up to 25% in comparison with two-level converter, and thus a reduction of the switching losses can be achieved [29].

However, it has higher conduction losses due to the number of devices in series and more complex control is required to balance the DC-link due to the mid-point voltage fluctuation [4, 28, 29]. Non-uniform power dissipation between the inner and outer switches on the same

switching arm might lead to uneven electro-thermal stress among four switches which mean different devices lifetime [28, 30].

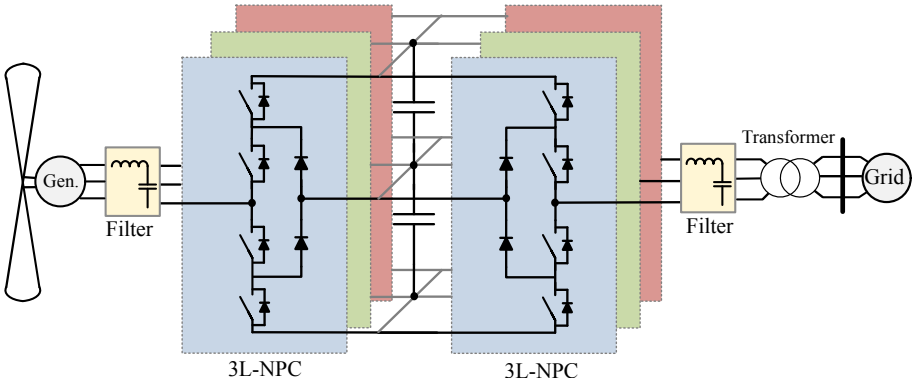


Figure 2.7: Three level neutral point clamped back to back converter for wind turbine [4].

2.3.4. Multi-cell interleaved converter

Fig. 2.8 shows a single line diagram of a multi-cell topology used for Multi-Megawatt (MW) variable speed wind turbines to use identical power converter modules in parallel and interleaved on the grid side to increase the power handling capability of the system. Each converter module is formed by its own 3-phase 2-Level VSC, filters, measurements and control system [4, 29, 31]. This converter configuration was adopted by Siemens and Gamesa in their MW wind turbines [31, 32].

The main advantages of the multi-cell topology: it uses the 2L-VSCs standard topology, the design is modular and redundant; it provides a back-up if one of the cells fails; the power losses can be decreased by reducing the number of parallel cells in operation in case of low wind power conditions. Moreover, the topology structure is scalable by paralleling converter modules for the target of wind turbine rating, the interleaving operation allows the reduction of the filter size on the grid side by implementing PWM interleaving modulation to reduce the harmonic content in current and voltage waveforms [31, 32].

2.3.5. Modular multilevel converter (MMC)

Fig. 2.9 shows the topology of MMC in wind energy application. The MMC configuration is formed by back-to-back three-phase units with cascaded sub-modules of 2L-VSC. One of the advantages is to eliminate the line step-up transformer and to minimize the output filter on the grid and generator sides by increased the voltage levels. Another advantage is to achieve a modular system with one power converter design to adapt different voltage and power levels to the range of wind turbine power ratings. Moreover, the converter modularity allows a good redundancy if one of the modules fails [4, 33].

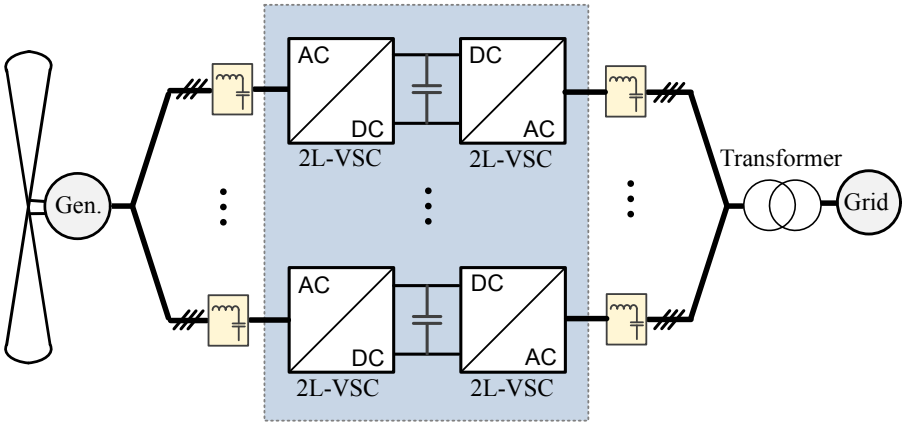


Figure 2.8: Multi-cell converter with paralleled modules [4].

On the other hand, MMC in wind energy applications requires higher rating voltage levels and more voltage insulation for the stator winding [4, 33]. For example, if the wind turbine conversion system is designed to be connected directly to the medium voltage level, i.e. 13.8 kV, thereby, a generator with a rated voltage equal to or slightly more than the grid voltage is required. However, such a generator is difficult to design and not commercially available [33].

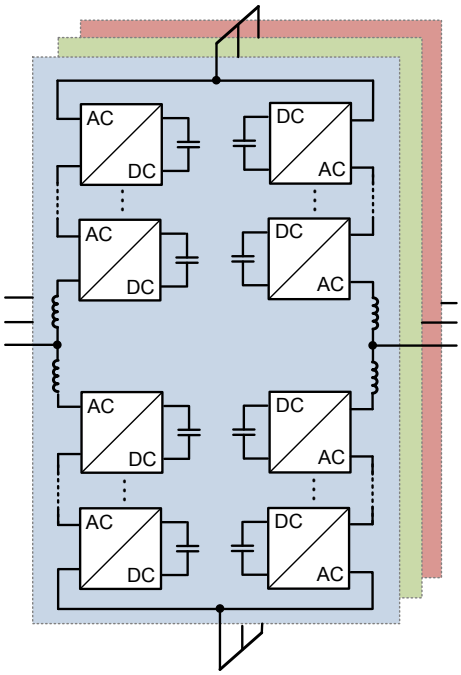


Figure 2.9: Modular multilevel converter for wind turbines (MMC) [4].

2.4. Harmonic standards for grid-connected inverters

Due to advances in power electronics development over the past few decades, the application of power electronics has been widely used in wind turbine conversion systems [4]. The output voltage and current of wind inverters should be restricted to the grid power quality requirements in order to minimise the impact of the inverter harmonics on other equipment.

Some power quality standards such as IEEE Std 519 [34] and IEC 61727 [35] have been introduced to comply with the grid requirements. These standards deal with the total harmonic distortion (THD) and the first 40 current harmonics, which must be within specified limits. A summary of standards for interconnection of power electronic converters to the grid is presented in Table 2.1.

Table 2.1: Power quality requirements for system interconnections to the grid

Issue	**Standard**
Harmonic currents (order -h) limits	(3-9) 4% (11-15) 2% (17-21) 1.5% (23-33) 0.6%
Maximum THD	5%
Power factor at 50% rated power	0.90
DC current injection	Less than 1.0% of rated output current
Voltage range for nominal operation	85% - 110% (196 V - 253 V)
Frequency range for nominal operation	50± 1 Hz

The current harmonic distortion can be quantified by the total harmonic distortion, THD, and the total demand distortion, TDD. The total harmonic distortion can be defined by [34]:

$$THD_I = \frac{\sqrt{I_2^2 + I_3^2 + ... + I_n^2}}{I_1} \tag{2.5}$$

where I_n is the RMS value of the n^{th} harmonic and I_1 is the RMS value of the fundamental current.

The definition of TDD includes the RMS value of the maximum load current, I_L. TDD gives an indication to how much THD impacts the system, for example, very high THD at low power loading has a low impact on the grid. At full load TDD=THD [34].

$$TDD_I = \frac{\sqrt{I_2^2 + I_3^2 + ... + I_n^2}}{I_L} \tag{2.6}$$

2.5. Wind turbine modelling and wind condition

For a small-scale wind conversion system in the power ranges up to hundred kW, it is a trend to use a PMSG in industry applications especially for a directly driven wind turbine with benefits of size and weight reduction. As there is no reactive power needed, the conversion system is a simple 3-phase diode rectifier with a dc-dc boost converter connected to 2L 3-phase PWM inverter as shown in Fig. 2.5 [4, 36]. Among various topologies for wind power applications, 2L 3-phase VSI is a good candidate for small-scale wind turbine applications. The main advantages of the 2L-topology compared to 3L-topologies, i.e. 3L-NPC, are simpler hardware and control complexity, fewer switches and circuits for switch-driving and protection, and even thermal stress among the switches [4].

The focus is on the inverter stage in this work, so that, the wind turbine model under MPPT is simplified by a current source connected in parallel with the DC-link capacitor of the grid-side inverter as shown in Fig. 2.10 [37].

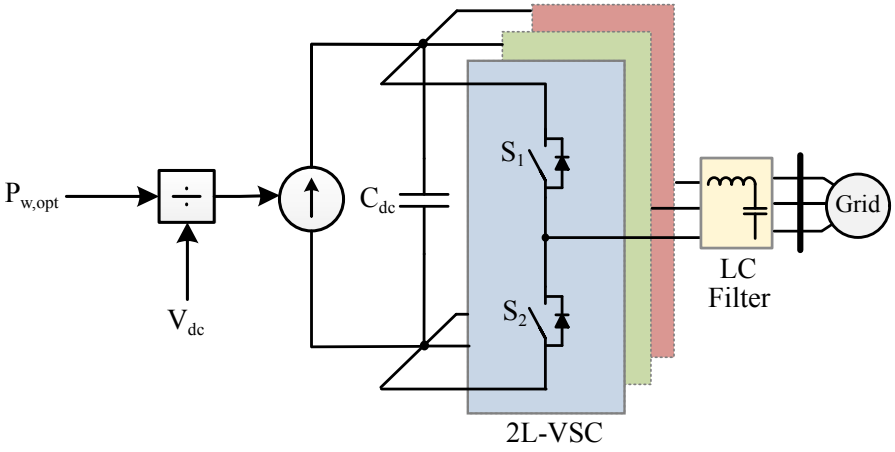


Figure 2.10: Simplified model of small scale wind turbine under MPPT.

The input signal of the current source is given by [37]:

$$I_w = \frac{P_{w,opt}}{V_{dc}} \tag{2.7}$$

where, $P_{w,opt}$ is the optimal wind turbine output power and V_{dc} is the DC-link voltage of the converter.

A typical wind turbine system and wind condition have to be chosen as a case study. The output power curve of a 10 kW commercial small-scale wind turbine is shown in Fig. 2.11: it is characterized by a small overshoot around the generator rated output and a lower power output for higher wind speed, because the blades are bolted onto the hub at a fixed angle. The output power curve is used an input to the inverter, and the rated power of the wind turbine is

achieved at the wind speed of 11 m/s, where the wind turbine starts at the wind speed of 3 m/s and shuts down at 25 m/s [38].

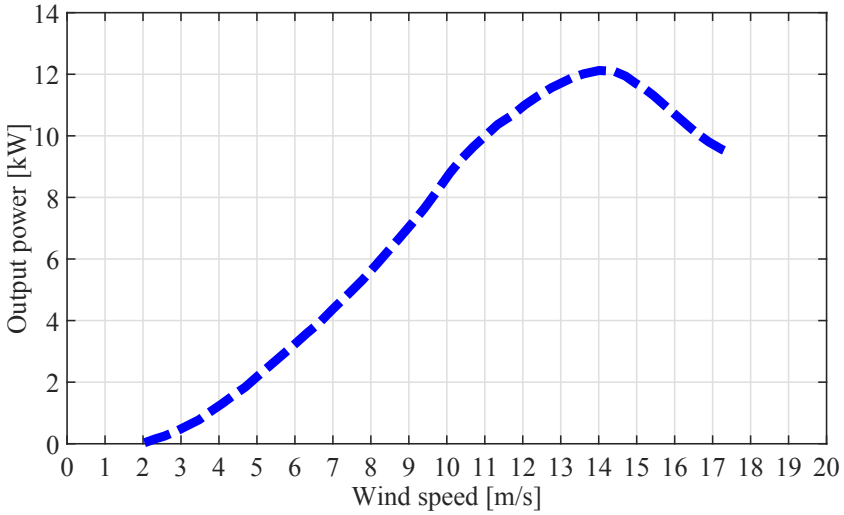


Figure 2.11: 10 kW wind turbine maximum output power [38].

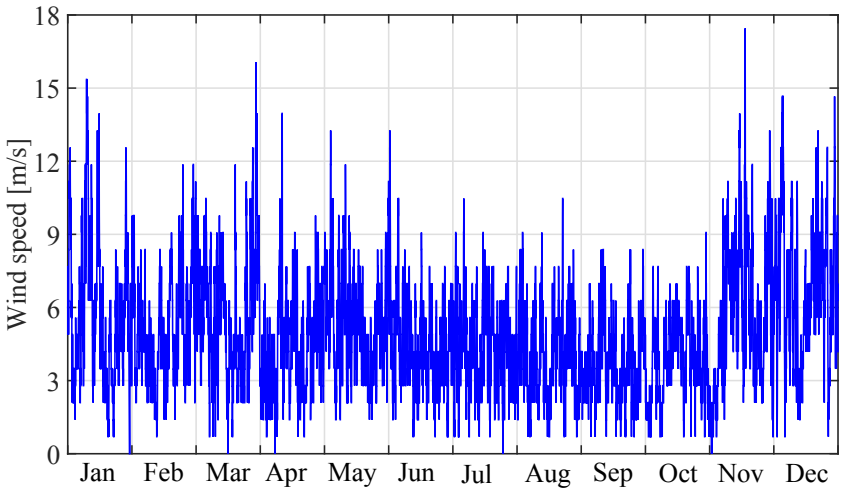
As shown in Fig. 2.12, a real-field annual mission profile data (i.e., wind speed and ambient temperature) provided by Watnall weather forecast (in Nottingham) is used with one hour averaged at 15 m hub height [39].

The wind mission profile in Fig. 2.12-a is converted to a wind speed distribution as presented in Fig. 2.13, which represents the wind speed frequency values in one year (% in 8760 hour). It is noticed that wind turbines consume most of their operational time at low wind speeds and they actually work at their maximum rated power for only a small fraction of time.

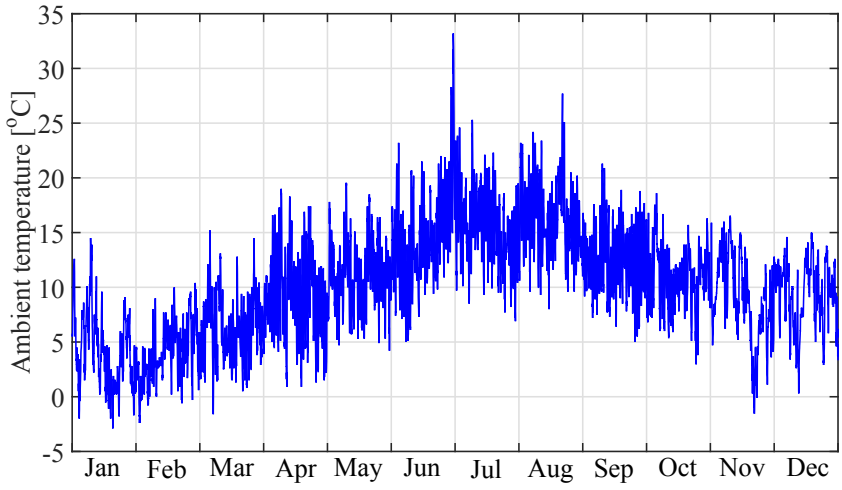
2.6. Description of the two-level three-phase inverter

Fig. 2.14 shows the power circuit for grid-connected applications, where V_{dc} represents the DC source, i.e. the output of the boost converter. A DC-link voltage V_{dc}=720 V (which is typically between 700 to 800 V) is introduced here to eliminate the need for a step-up transformer for low voltage grid connections. The DC-link of the inverter includes two identical capacitors to ensure an equal share of DC-link voltage and to introduce the mid-point for a grid neutral wire connection. A LC output filter is required to smooth the load current ripple. The low voltage grid uses an AC power system with the line-to-line voltage of 400 V and line frequency of 50 Hz.

The different methods for PWM generation can be classified into Sinusoidal based PWM (SPWM) and Space Vector based PWM (SVPWM). SPWM is favoured due to its simplicity. However, SVPWM has advantages over SPWM due to its harmonic reduction, better utilization of the DC-bus voltage [40,41], and the switching pattern can be modified to create a more even



(a) Wind speed



(b) Ambient temperature

Figure 2.12: One year mission profile of wind speed and ambient temperature in Nottinghma (1-hour averaged). (a) Wind speed profile and (b) Ambient temperature profile [39].

distribution of the conduction losses, and to reduce the switching losses [42]. In this work, the switches are driven by the modulation scheme based on SPWM control. The modulation strategy for one phase-leg, i.e. phase A with transistors M1, M2 and freewheeling diodes D1, D2, are presented in Fig. 2.15. The carrier signal is compared with the reference signal to generate the switching pulses for phase A switches, M1 and M2. The reference voltage signal and the output current at the fundamental frequency, f_0 is given by (2.8) and (2.9) respectively. θ is equal to $2\pi f_0 t$, V_r is the peak of the reference voltage, I_P is the peak of the load current and φ is the phase shift between voltage and current waveforms.

$$v_r = V_r sin(\theta) \tag{2.8}$$

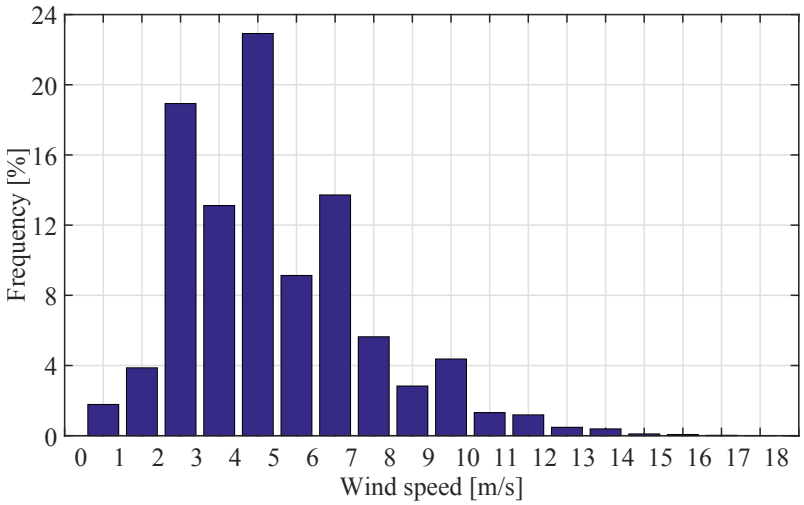


Figure 2.13: Wind speed distribution in Nottingham [39].

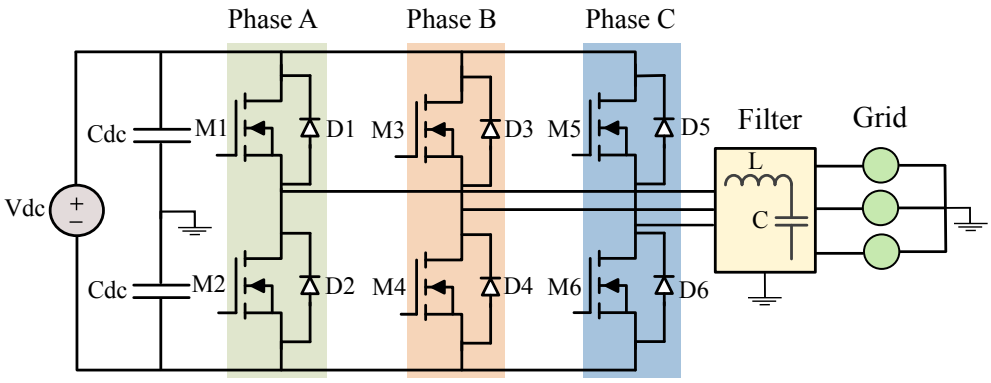


Figure 2.14: Schematic of three-phase two-level voltage source inverter.

$$i_o = I_P sin(\theta - \varphi) \tag{2.9}$$

According to [9], the switch RMS current I_{rms} is given by:

$$I_{rms} = I_P \sqrt{\left(\frac{1}{8} + \frac{1}{3\pi} m_a cos\varphi\right)} \tag{2.10}$$

The freewheeling diode average current I_{avg} and RMS current I_{rms} are given by (2.11) and (2.12), respectively [9].

$$I_{avg} = I_P \left(\frac{1}{2\pi} - \frac{1}{8} m_a cos\varphi\right) \tag{2.11}$$

$$I_{rms} = I_P \sqrt{\left(\frac{1}{8} - \frac{1}{3\pi} m_a cos\varphi\right)} \tag{2.12}$$

where m_a is the amplitude of modulation index and given by $m_a = V_r/V_c$.

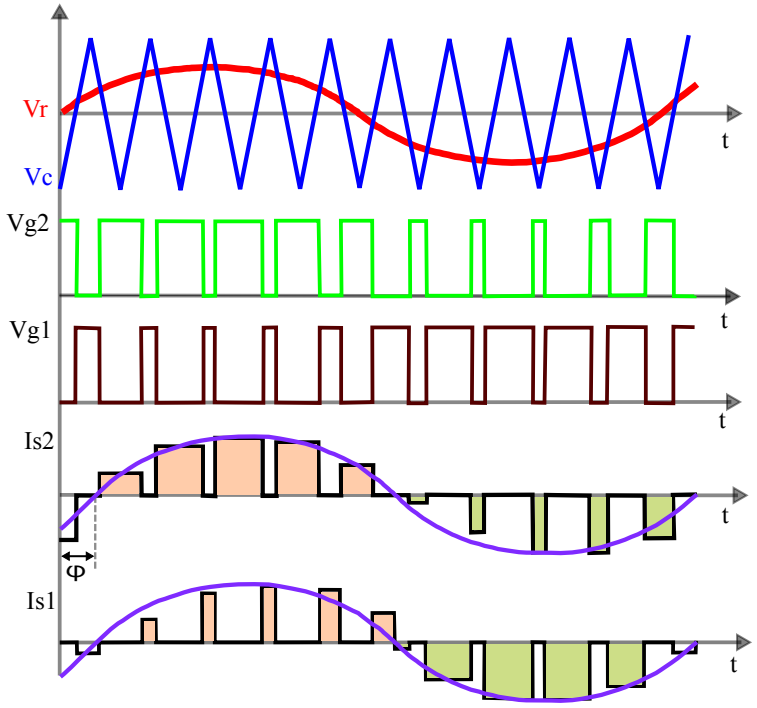
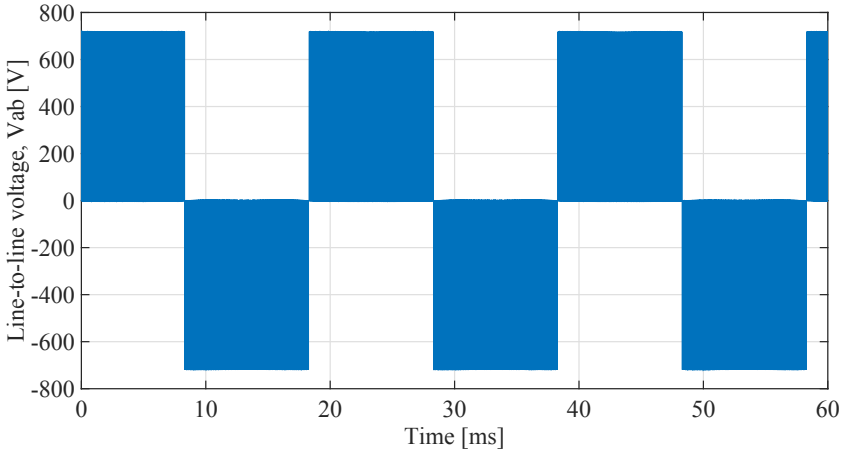


Figure 2.15: Switching waveforms for complete fundamental cycle.

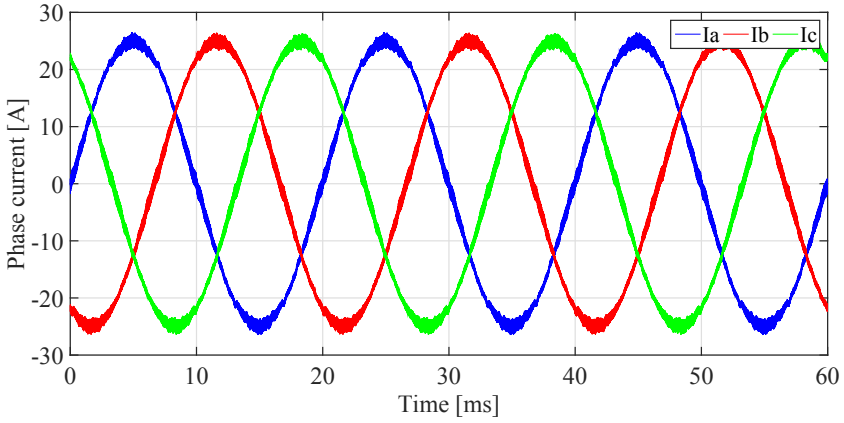
Fig. 2.16 shows the simulation results of phase voltage with respect to the line-to-line voltage generated by the transistor bridge and the corresponding line currents through line side inductor injected into the grid for a switching frequency of 32 kHz.

2.7. SiC MOSFET vs. Si IGBT performance benchmarking

In this section, a detailed description of the power losses analysis procedure for Si and SiC devices in order to benchmark their performance in the device level and in the corresponding inverter operation. The comparison was performed between 1.2kV/20A six-pack SiC MOSFET power module (CCS020M12CM2 from CREE) and 1.2kV/25A six-pack Si IGBT power module (FS25R12W1T4 from Infineon) based on the available information from device datasheets [1, 43]. Devices characteristics, efficiency at different wind speeds, a wide range of switching frequencies and heat-sink temperatures, and thermal stress based on a real mission profile (wind and temperature) were presented in order to fully evaluate of SiC and Si in wind energy applications.



(a) Line-to-line voltage



(b) Line currents

Figure 2.16: Simulation results of 2L-VSI. (a) Line-to-line voltage, and (b) Line currents, at 32kHz.

2.7.1. Electro-thermal model

The aim of the electro-thermal model is to deliver the device model, the power loss model and the thermal model. The device model estimates the device on-state voltage drop (switch voltage V_S and diode forward voltage V_D), and device energies (E_{on} and E_{off}) for the switch and diode taking into account the device current (switch current I_S and diode current I_D), the ambient temperature (T_a) and the junction temperature (T_j). Then, these parameters and the switching frequency (f_{sw}) are fed into the power loss model to estimate the device losses, where the contribution of conduction and switching losses of the device (switch and diode) are determined. The device conduction losses (switch conduction loss $P_{S,cond}$ and diode conduction loss $P_{D,cond}$) are produced by the product of the on-state voltage drop (switch voltage V_S and diode forward voltage V_D) across the power device and the device current (switch current I_S, diode current I_D) which is flowing through it, while the device switching losses (switch power losses $P_{S,sw}$ and diode switching losses $P_{D,sw}$) are determined at different device voltages,

current levels and junction temperatures based on the device switching losses data provided in the device datasheet.

After that, the thermal model estimates the device junction temperature and case temperature by considering the device total power loss and ambient temperature. The device junction temperature can be calculated by (2.13) and (2.14) based on the thermal circuit for devices in the 2L 3-phase converter topology shown in Fig. 2.17. Since, in practice, the junction temperature varies with the variable power availability from the source, this affects the losses in the device. Therefore, the junction temperature and the corresponding loss calculations have to be repeated in the simulation until the junction temperature deviation becomes lower than a preset error.

$$T_{j,S} = P_S.R_{th,jc,S} + 6 \times (P_S + P_D).R_{th,ch} + T_h \tag{2.13}$$

$$T_{j,D} = P_D.R_{th,jc,D} + 6 \times (P_S + P_D).R_{th,ch} + T_h \tag{2.14}$$

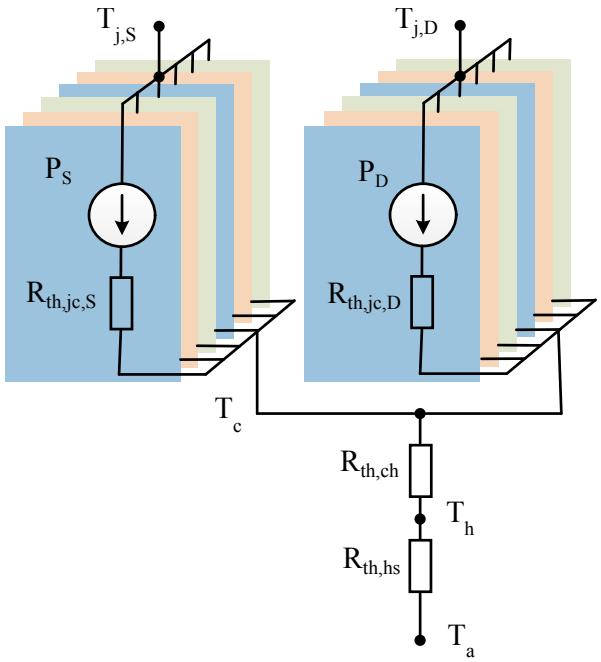


Figure 2.17: Thermal circuit of six pack power module for the 2L VSC protoype.

The thermal circuit parameters for Si IGBT , Si diode, SiC MOSFET, SiC Schottky diode are shown in Table 2.2 [43].

Table 2.2: Thermal circuit parameters

Item	$R_{th}[^oC/W]$
Si IGBT	0.66
Si diode	0.95
SiC MOSFET	0.7
SiC Schottky diode	0.8
Thermal grease	0.02

Si IGBT power loss model

The on-state voltage of Si-based IGBT and power diode are calculated as follows:

$$V_S = V_{S,on} + I_S R_{S,on} \tag{2.15}$$

$$V_D = V_{D,on} + I_D R_{D,on} \tag{2.16}$$

where I_S and I_D are the conduction current through Si IGBT and power diode, respectively; $R_{S,on}$ and $R_{D,on}$ are on-state resistance for Si IGBT and power diode, respectively; and $V_{S,on}$ and $V_{D,on}$ are the Si IGBT and power diode on-state on-state voltage when I_S=0 and I_D=0, respectively.

The on-state voltage and resistance in $[m\Omega]$ for Si IGBT switch depend on the semiconductor junction temperature as follows:

$$V_{S,on} = \gamma T_j + V_{S0} \tag{2.17}$$

$$R_{S,on} = a_2 T_j^2 + a_1 T_j + a_0 \tag{2.18}$$

Where γ, V_{S0}, a_2, a_1 and a_0 are coefficients extracted from IGBT output characteristics information offered in the datasheet [43].

Table 2.3: IGBT on-state voltage and resistance parameters

Parameter	Value
γ	-0.0012
a_2	0.0009
a_1	0.0402
a_0	31.656

The temperature dependency of on-state voltage and resistance of Si power diode are as follows:

$$V_{D,on} = \alpha T_j + V_{D0} \tag{2.19}$$

$$R_{D,on} = \beta T_j + R_{D0} \tag{2.20}$$

where α, β, V_{D0} and R_{D0} are extrapolated from Si diode forward characteristic data provided by the manufacturer [43].

Table 2.4: Si diode on-state voltage and resistance parameters

Parameter	Value
α	-1.5×10^{-3}
β	0.360×10^{-4}
V_{D0}	1.1481
R_{D0}	0.0243

The conduction losses for Si IGBT and power diode are calculated as follows:

$$P_{S,con} = I_P \left(\frac{1}{2\pi} + \frac{m_a cos\phi}{8} \right) V_{S,on} + I_P^2 \left(\frac{1}{8} + \frac{m_a cos\phi}{3\pi} \right) R_{S,on} \tag{2.21}$$

$$P_{D,con} = I_P \left(\frac{1}{2\pi} + \frac{m_a cos\phi}{8} \right) V_{D,on} + I_P^2 \left(\frac{1}{8} + \frac{m_a cos\phi}{3\pi} \right) R_{D,on} \tag{2.22}$$

where I_P is the peak value of phase current, m_a is the amplitude modulation ratio and ϕ is the current phase shift.

The switching losses for Si IGBT switch and power diode in [mW] are given as follows:

$$P_{S,sw} = f_{sw} \left(\frac{2b_3 I_P^3}{3\pi} + \frac{b_2 I_P^2}{4} + \frac{b_1 I_P}{\pi} + \frac{b_0}{2} \right) \times (1 + TC_{sw}(T_j - T_{jref})) \tag{2.23}$$

$$P_{D,sw} = f_{sw} \left(\frac{2b_3 I_P^3}{3\pi} + \frac{c_2 I_P^2}{4} + \frac{c_1 I_P}{\pi} + \frac{c_0}{2} \right) \times (1 + TC_{sw}(T_j - T_{jref})) \tag{2.24}$$

Where b_0, b_1, b_2, and b_3 are constants derived from IGBT switching losses data provided in the device datasheet; c_0, c_1, c_2, and c_3 are coefficients extracted from Si diode switching losses [43]; TC_{sw} is the temperature coefficient of switching losses (IGBT=0.004 and Diode=0.006 [44]); and T_{jref} is the reference temperature for switching energy measurements given by the

manufacturer.

Table 2.5: Si IGBT switching losses parameters

Parameter	Value
b_3	0.00003
b_2	0.00004
b_1	0.16804
b_0	0.43989

Table 2.6: Si diode switching losses parameters

Parameter	Value
c_3	0.00002
c_2	-0.00208
c_1	0.98824
c_0	0.28285

SiC MOSFET power loss model

The on-state voltage of SiC-based MOSFET and Schottky diode are calculated as follows:

$$V_S = I_S R_{S,on} \tag{2.25}$$

$$V_D = V_{D,on} + I_D R_{D,on} \tag{2.26}$$

where I_S and I_D are the conduction current through SiC MOSFET and Schottky diode, respectively; $R_{S,on}$ and $R_{D,on}$ are on-state resistance for SiC MOSFET and Schottky diode, respectively; and $V_{D,on}$ is the Schottky diode on-state voltage when I_D=0.

The on-state resistances for SiC MOSFET switch in $[m\Omega]$ as a function of the semiconductor junction temperature is given by [1]:

$$R_{S,on} = a_2 T_j^2 + a_1 T_j + a_0 \tag{2.27}$$

Where a_2, a_1 and a_0 are coefficients derived from MOSFET on-state resistance information provided in the datasheet [1].

The on-state voltage and resistance of Schottky diode depend on the junction temperature as follows:

$$V_{D,on} = \alpha T_j + V_{D0} \tag{2.28}$$

Table 2.7: MOSFET on-state resistance parameters

Parameter	Value
a_2	0.0020
a_1	0.1658
a_0	74.9056

$$R_{D,on} = \beta T_j + R_{D0} \tag{2.29}$$

where α, β, V_{D0} and R_{D0} are extrapolated from the Schottky diode forward characteristic data provided by the manufacturer [45].

Table 2.8: Schottky diode on-state voltage and resistance parameters

Parameter	Value
α	-1.40×10^{-3}
β	2.71×10^{-4}
V_{D0}	0.97
R_{D0}	0.023

The values of conduction losses for SiC MOSFET and Schottky diode are calculated as follows:

$$P_{S,con} = I_P^2 \left(\frac{1}{8} + \frac{m_a cos\phi}{3\pi} \right) R_{S,on} \tag{2.30}$$

$$P_{D,con} = I_P \left(\frac{1}{2\pi} + \frac{m_a cos\phi}{8} \right) V_{D,on} + I_P^2 \left(\frac{1}{8} + \frac{m_a cos\phi}{3\pi} \right) R_{D,on} \tag{2.31}$$

where I_P is the peak value of the phase current, m_a is the amplitude modulation ratio and ϕ is the current phase shift. The switching losses for SiC MOSFET in [mW] and the Schottky diode is given as follows:

$$P_{S,sw} = f_{sw} \left(\frac{2b_3 I_P^3}{3\pi} + \frac{b_2 I_P^2}{4} + \frac{b_1 I_P}{\pi} + \frac{b_0}{2} \right) \times (1 + TC_{sw}(T_j - T_{jref})) \tag{2.32}$$

Where b_0, b_1, b_2, and b_3 are constants derived from SiC MOSFET switching losses data provided in the device datasheet; c_0, c_1, c_2, and c_3 are coefficients extracted from Si diode switching losses [45]; TC_{sw} is the temperature coefficient of switching losses (MOSFET=0, because SiC MOSFET has a negligible temperature dependency); and T_{jref} is the reference temperature for switching energy measurements given by the manufacturer [44].

Table 2.9: SiC MOSFET switching losses parameters

Parameter	Value
b_3	0.2938
b_2	0.3329
b_1	0.4244
b_0	0.5219

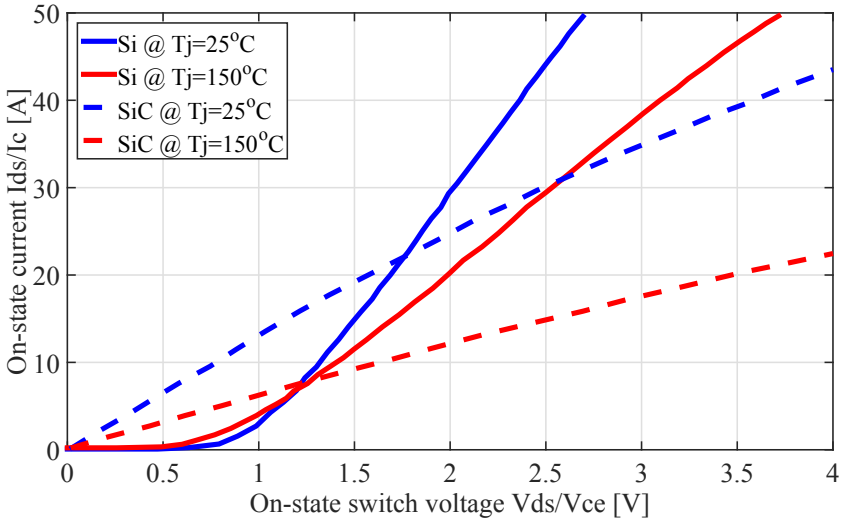
The Schottky diode has zero reverse recovery ($P_{D,sw}$ is equal to zero) [45].

2.7.2. Device characteristics

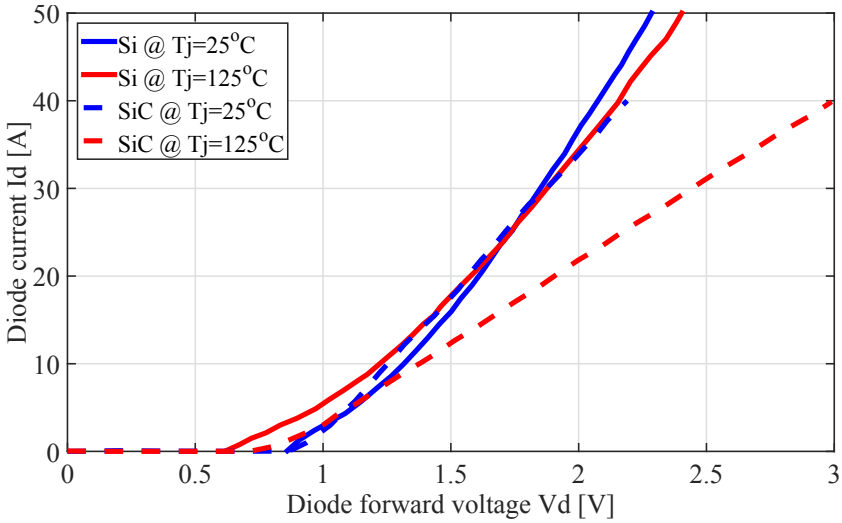
In terms of conduction performance, Fig. 2.18-a shows that SiC MOSFETs offer the best on-state conduction voltage at currents less than 22 A at $T_j = 25^oC$ and less than 8A at $T_j = 150^oC$, because they have no offset voltage during turn-on like Si IGBTs. Fig. 2.18-b shows the conduction characteristics comparison between Si P-i-N diode and SiC Schottky diode, and it is clear that the conduction performance of Si and SiC diodes are comparable at currents less than 10 A. However, at higher currents and junction temperatures, Si diode has lower conduction voltage than that of SiC Schottky diode.

Moreover, SiC MOSFETs have significant lower turn-on and turn-off switching losses than that of IGBTs. This property allows SiC converter to operate at much higher switching frequencies. In addition, SiC Schottky diode has excellent reverse recovery characteristics due to almost zero reverse recovery losses compared with the reverse recovery energy of $0.9 - 1.7$ mJ for Si diode.

With regard to the inverter operation, the analysis were carried out on a three-phase 2L VSI based on the available information from datasheets. Inverter efficiency and cumulative energy production, switching frequency and volume, and temperature stability and thermal stress comparison for MOSFET and IGBT-based technologies are included. The switching frequency was set at 10 kHz for comparison, for two reasons. First, 10 kHz is the edge of the switching frequency range (8 kHz to 10 kHz) for IGBTs based on this topology and at this power level. Second, 10 kHz is chosen as a trade-off between IGBT losses and passive components size.



(a) Si IGBT vs SiC MOSFET



(b) Si PiN diode vs SiC Schottky diode

Figure 2.18: Conduction loss characteristics benchmarking. (a) Si and SiC switches. (b) Si and SiC diodes [1, 43].

2.7.3. Efficiency and energy production

The analysis was carried out on a 12 kW 2L VSI. The switching frequency was set at 10 kHz for comparison, where 10 kHz is the reference switching frequency for Si IGBTs based on this topology at this power level. A DC-link voltage of 720 V, grid phase voltage of 230 V and a line frequency of 50 Hz were used.

The power cell efficiency of a wind grid-connected inverter with Si IGBTs and SiC MOSFETs in the presence of wind speed distribution is shown in Fig. 2.20. Over the whole range of operation, SiC devices show higher efficiencies than that of Si, especially in the region of

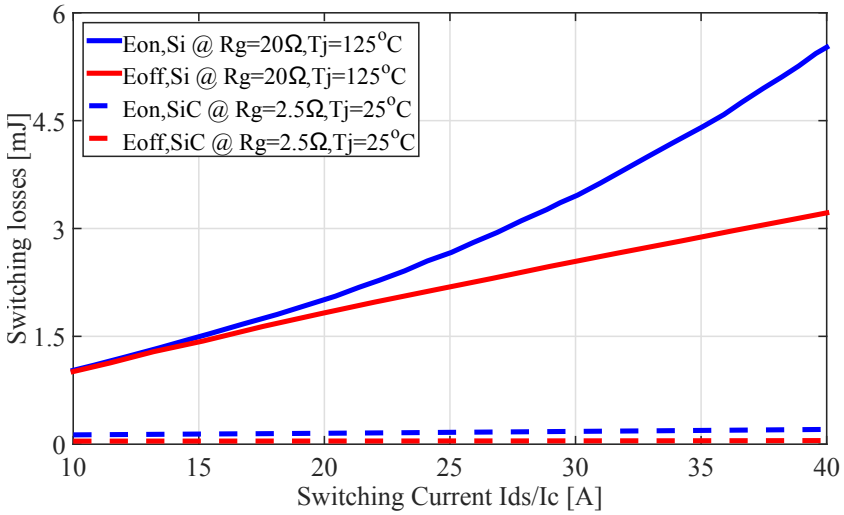


Figure 2.19: Switching loss characteristics of the Si and SiC switches [1,43].

interest where wind turbines actually work for most of their operational time (about 78% of the time). The major issue with the existing grid-connected inverter based on Si IGBTs is very low efficiencies at partial loads of low input power levels as the converter losses become dominant. SiC MOSFETs, however, show better performance at light-load conditions, and therefore have better efficiencies in the region of high wind speed distribution; this subsequently reduces the overall system size and cost.

Moreover, at the minimum wind speed operation range of 3 m/s which has a highly probable working chance, SiC devices present higher efficiency by a value of 2.5% than that of Si devices. In addition, at the rated wind speed of 11 m/s, the efficiency of SiC is about 99.4% compared to 98.6% for Si inverter.

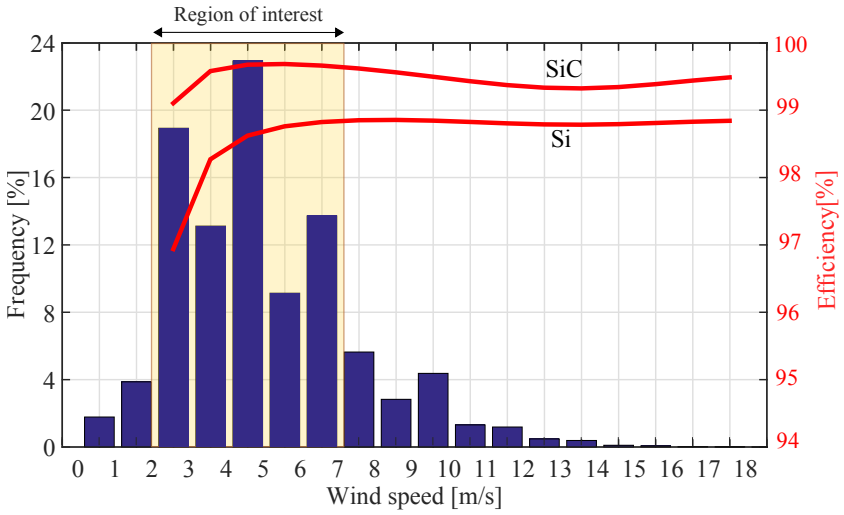


Figure 2.20: The wind speed distribution (blue data) and inverter efficiency (red data) versus wind speed for heat sink temperature of 60 ^oC and switching frequency of 10 kHz.

The annual cumulative energy loss was estimated based on the power loss model (conduction and switching) considering the mission profile of wind speed and ambient temperature with 1-hour averaged samples. First, wind turbine output power is obtained at different individual operating points and then the corresponding power losses and device junction temperature are calculated. After that, the resulting junction temperatures are curve-fitted with respect to wind speed and ambient temperature in a way to link the mission profile with the power device. Finally, the inverter power losses and the accumulated energy throughout the whole year are calculated.

As a result of using a mission profile with 1-hour averaged samples, some simplifications were made: the power device and heat-sink thermal capacitance can be neglected and only a static model based on thermal resistances can be used in the analysis. However, wind turbines are highly dynamic (wind speed and heat-sink ambient temperature change in minutes rather than hours). Therefore the annual energy loss calculation as carried out are inevitably characterized by some degree of inaccuracy, but as the inaccuracy is the same for all devices, it is expected that the error should always be in the same direction and should not affect the comparative analysis.

For grid-connected applications, the resulting annual energy for the Si-based inverter is about 322.1 kWh, and in contrast, 101.8 kWh for SiC inverter as shown in Fig. 2.21. This results in a total energy losses saving up-to 68.4% by replacing Si with SiC devices solution. Based on UK infeed tariff for small-scale wind turbines of 0.12 £/kWh, it can be seen that the SiC inverter will bring £ 26.44 to the investors in comparison with Si inverter.

The increased efficiency of SiC inverter can lead to reducing the heat-sink volume requirements. In particular, the required heat-sink thermal resistance attained by natural convection is 0.37 ^{o}C/W with a volume of 2.36 dm^3 for SiC-based inverter, and in contrast, 0.21 ^{o}C/W with a volume of 4.95 dm^3 for Si inverter; this leads to a reduction in heat-sink volume by more than 52% and still ensuring the designed heat-sink reference temperature of 60^{o}C even at a smaller system volume.

2.7.4. Temperature capability and thermal stability

Fig. 2.22 presents the inverter efficiency over a range of heat sink temperatures from 50 ^{o}C to 100 ^{o}C, where it is seen that SiC devices show higher temperature capability compared with Si devices. SiC devices show 0.16% drop in efficiency which is smaller than that of Si devices which show 0.27% drop in efficiency in the tested temperature range.

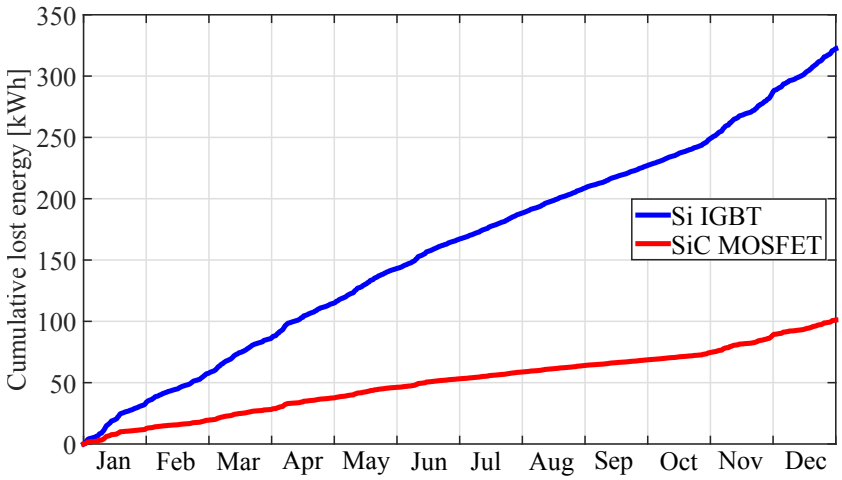


Figure 2.21: Cumulative energy loss of two-level grid-connected inverter based on Si and SiC technologies.

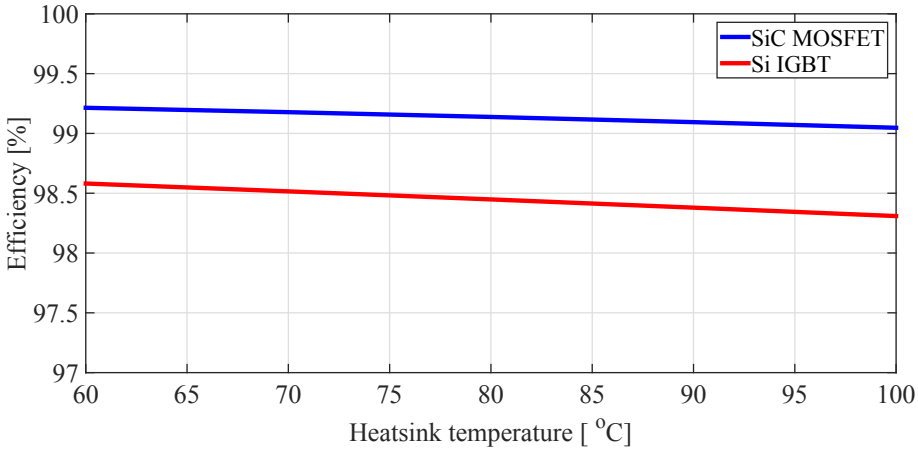


Figure 2.22: Efficiency of SiC and Si inverter versus heat sink temperature at 12 kW output power and switching frequency of 10 kHz.

2.7.5. Switching frequency performance

Fig. 2.23 presents the inverter efficiency over a range of switching frequencies, where it is clearly seen that Si devices can operate just on a narrow range of switching frequencies due to a higher switching loss. In contrast, SiC works on a wider range of switching frequencies without a significant loss of efficiency. Moreover, by increasing the switching frequency from 10 kHz to 20 kHz, the efficiency is dropped more quickly at the rate of 0.93% for Si and by a slower rate of 0.05% for SiC. This merit of SiC devices can lead to reducing the size of bulky passive elements in 2-level converters without losing a significant amount of efficiency. However, increasing the switching frequency leads to a larger heat-sink volume as a result of increasing the converter power losses.

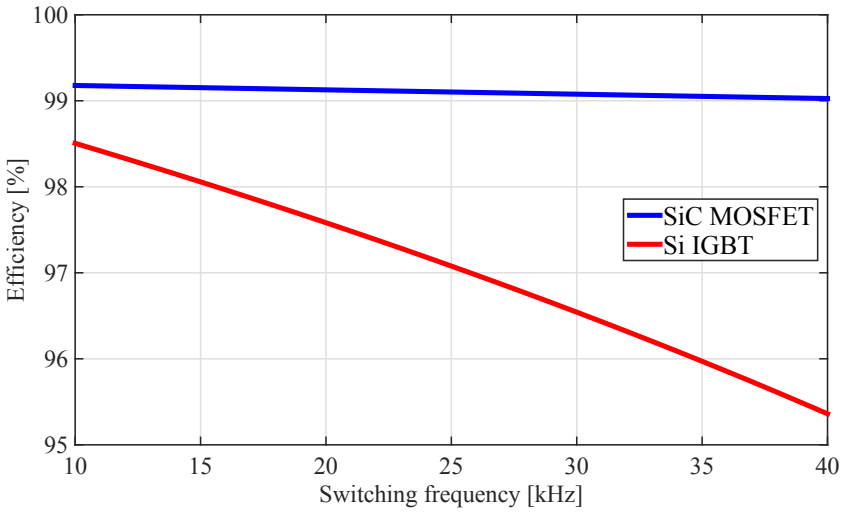


Figure 2.23: Efficiency of SiC and Si inverter versus switching frequency at 12kW output power and heatsink temperature of 60^oC.

2.7.6. Thermal stress comparison

The 2L-VSI topology shown in Fig. 2.14 provides an even loss distribution among each phase leg, and therefore, the thermal stresses in all devices are identical. In this section, the thermal loading of power electronics devices are conducted based on the annual mission profile in Nottingham presented in Fig. 2.12. The junction temperature, T_j, for Si and SiC devices under the thermal loading profiles is shown in Fig. 2.24 with junction temperatures up to 74.5^{o}C for Si-IGBT and 61^{o}C for SiC MOSFET during warm times in summer. It is shown that SiC devices bring reduced mean and amplitude junction temperature variations in comparison with Si devices.

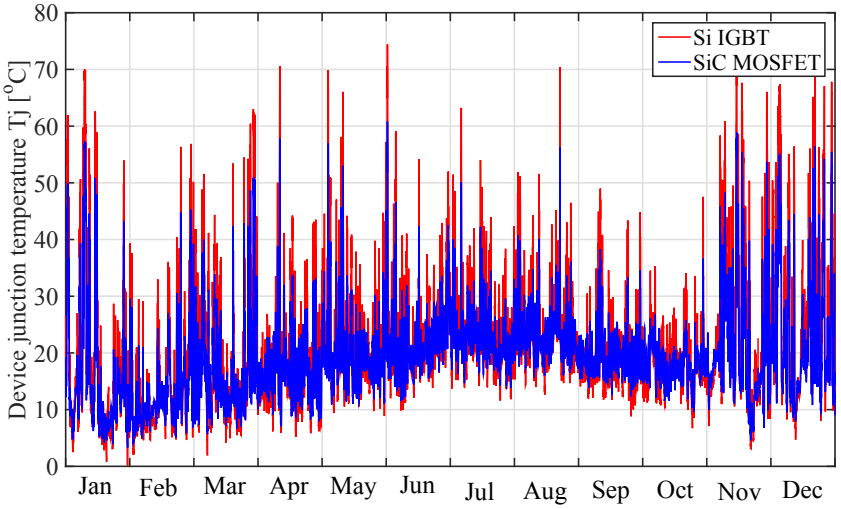


Figure 2.24: Junction temperature variation of stressed devices in 2L-VSI through a whole year.

2.8. Conclusion

In this chapter, a historical overview of wind turbine inverters topologies has been presented, and a comparison of wind turbine systems with different conversion stages has been discussed. State-of-the-art two-level three-phase inverter topologies for wind turbine systems have been designed. The inverters presented have been analysed with SiC and Si based power devices in order to assess their performance under different conditions. The results comparing efficiency against the wind speed distribution enable the advantages of SiC technology to be determined: reduced power losses and heat-sink requirements. When this capability is added to the decrease in the size of passive filter elements, which can be gained by exploiting the higher switching frequency capability of SiC MOSFETs, the result is a significant increase in the converter power density. The economic impact of SiC solution has been described, the replacement of Si IGBT with SiC in the system brought significant operational income due to higher energy production throughout the year.

Chapter 3

Wide-Bandgap Power Devices

This chapter discusses power electronic devices: diodes and transistors, with a focus on the semiconductor material properties and the fundamentals of power devices. The discussion of fundamental properties of silicon carbide (SiC) material is presented as an overview of its superior properties over the current standard semiconductor material, silicon. A brief overview of SiC and Si devices including P-i-N diode, SBD, IGBT and MOSFET was introduced; their structures and the benefits of emerging SiC material on the device characteristics were discussed. In addition, the static and dynamic performance of SiC power module with a blocking voltage of 1.2 kV under different current loading, different temperatures and different gate driver resistors were presented.

3.1. Wide-bandgap material properties

In most power electronics, for optimum efficiency, the power switches should entail as much as possible currents without voltage drop during on-state; high voltage blocking without leakage current during off state; and zero switching losses. In practice, therefore, due to the growing number of industrial applications, the material used in power semiconductor devices fabrication have to satisfy the above requirements as much as possible [46]. Silicon is a state-of-the-art material for power semiconductor devices manufacturing since the first introduction of bipolar and unipolar devices. The intrinsic characteristics of Si material, however, limits the performance of power converters to satisfy the future power electronics converter requirements. However, WBG material such as silicon carbide (SiC) and gallium nitride (GaN) have been introduced to deliver semiconductor devices that may merge the potential of low on-state resistance, high blocking voltage, high operating temperature and high switching frequency capability [5,6,46].

Table 3.1 shows the material properties of Si and WBG materials. The bonds between silicon and carbon atoms in SiC are stronger than that between silicon atoms in silicon, which

enables bandgap energy in SiC to be about three times larger than that of Si, which can be realized by looking into bandgap energy for different materials Si (1.12 eV) and SiC (3.2 eV) [47]. This has the consequence of enabling the design of devices with higher voltage capability, stable thermal operation which may withstand a number of out of safe operating area (SOA) stress conditions [5, 46].

The energy gaps for metal, semiconductor and insulator are illustrated in Fig. 3.1. The interaction between the valence and the conduction bands in solids are described by a bandgap energy E_g. The E_g represents the required energy for electrons in the valence band to break the atom bonds and generate electrons in conduction band. For semiconductor material which have a moderate conductive proprieties between metal and insulator, the conduction band is almost empty and valence band is almost full with electrons. At the thermal equilibrium, the thermal energy in the intrinsic semiconductor is sufficient to generate electrons in the conduction band (n_0), and the empty states in the valence band leave positively charged holes (p_0). The intrinsic carrier concentration n_i, i.e. the number of electrons and holes per unit volume in the semiconductor, is dependent on material properties and temperature and given by (3.1) [48]. The intrinsic carrier concentration in SiC is about 20 times lower than in Si at room temperature; for reference, the intrinsic carrier concentration in Si reduces from nearly $1.45 \times 10^{10} cm^{-3}$ to nearly $8.2 \times 10^{9} cm^{-3}$ at 300 K [5]. This enables SiC material to become intrinsic at high temperature, i.e. 1000 ^{o}C [47], which leads to design of devices which may operate at high temperatures in excess the maximum operating temperature for Si devices [5, 47].

$$n_0.p_0 = n_i^2 \tag{3.1}$$

Table 3.1: Material properties for series of semiconductor fabrication materials [47]

Property	Si	4H-SiC	GaN	Diamond
Bandgap, $E_g[eV]$	1.12	3.26	3.39	5.47
Dielectric constant, ϵ_r	11.8	9.7	9	5.7
Electric breakdown field, $E_{crit}[MV/cm]$	0.23	2.2	3.3	5.6
Electron mobility, $\mu_n[cm^2/V.s]$	1400	950	1500	1800
Saturated electron drift velocity, $v_{sat}[\times 10^7 cm/s]$	1	2	2.5	2.7
Thermal conductivity, $\lambda[W/cm.K]$	1.5	3.8	1.3	1.3

The critical electrical field of SiC is almost a factor of ten times higher than that of Si (2.2 MV/cm for SiC and 0.23 MV/cm for Si). This feature leads to design of devices with low-loss high-voltage characteristics by increasing the doping level for a given target blocking voltage. Device requirements for voltage withstand capability are dictated by the crystal thickness and the doping level; higher blocking voltage requires the thicker lower-doped region to support the reverse bias voltage.

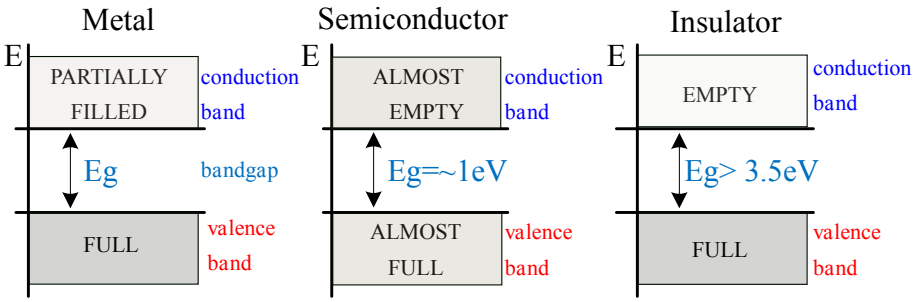


Figure 3.1: Energy diagram of metal semiconductor and insulators.

By considering the p-n junction structure at a reverse bias presented in Fig. 3.2, for a given target break down voltage V_{BD}, the relation between the depletion layer width, W, the critical electrical field, E_C, and V_{BD} are given by (3.2). The limit of minimum thickness is maintained by the depletion region width, W, which is possibly made thinner by about ten times as the maximum electric field of SiC material is almost higher ten times than that of Si.

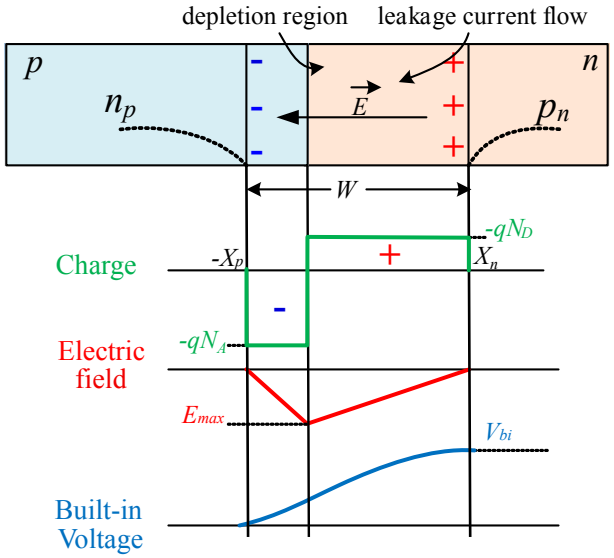


Figure 3.2: p-n junction under reverse bias voltage.

$$W = \frac{2V_{BD}}{E_C} \tag{3.2}$$

The required doping level to achieve this electrical field is given by (3.3), which is proportional to the square of E_c, so that around 100 times higher doping level for a given target voltage blocking is possible in SiC devices compared with Si.

$$N_D = \frac{2\varepsilon V_{BD}}{qW^2} = \frac{\varepsilon E_c^2}{2qV_{BD}} \tag{3.3}$$

where, ε is the dielectric constant, q is the electron charge.

The relation between R_{on}, V_{BD}, and E_C is given by (3.4). It is obvious that the on-state resistance is proportional to the square of V_{BD}, which means that the R_{on} is mainly dominated by the low-doped blocking region for high breakdown voltage power devices. R_{on} also inversely proportional to cube of E_C, and its value theoretically becomes 400 times lower than that of Si at the same target blocking voltage level [47]. Practically, this does not mean that for the same power dissipation, a reduction by a factor of 400 in a chip size can be achieved due to some thermal restrictions [49]. However, SiC devices with smaller cross-section and lower on-state resistance than their Si counterpart can be achieved; this in spite of a lower value of the carrier's mobility in SiC as compared with Si ($950cm^2/V.s$ for SiC, and $1400cm^2/V.s$ for Si) [5, 47]. The denominator of (3.4) is defined as Baliga's figure of merit $BFoM$, which represents the measure of on-state resistance of the drift region with respect to the material properties.

$$R_{on} = \frac{W}{q\mu_n N_D} = \frac{4V_{BD}^2}{\varepsilon\mu_n E_C^3} \tag{3.4}$$

$$BFoM = \varepsilon\mu_n E_C^3 \tag{3.5}$$

where, R_{on} is the on-state resistance and μ_n is the electron mobility.

The leakage current in a reverse biased P-N junction is formed mainly by electrons and holes swept across the depletion region. It is ideal to have as low as possible leakage currents during the voltage blocking mode. The leakage current in power devices is a function of blocking voltage and intrinsic carrier concentration according to (3.6), and the latter is proportional to the bandgap energy and temperature as presented in (3.7). SiC enables the design of devices with lower off-state leakage current at higher temperatures than that of Si due to lower intrinsic carrier concentration and higher bandgap energy of SiC [5, 50]. In high voltage devices, i.e 6.5 kV Si IGBT modules employed in railway traction applications, the off-state losses due to the leakage current becomes significant which enhance a risk of failure as a result of thermal runaway phenomena [51].

$$J_{leak} \propto \sqrt{V_{BD}}.n_i \tag{3.6}$$

$$n_i^2(T_j) = C.T_j^3.e^{\frac{E_g(T_j}{kT_j)}} \tag{3.7}$$

where, J_{leak} is the leakage current amplitude, and k is Boltzmann constant.

The thermal conductivity of SiC material is higher nearly 3 times than that of Si, in principle, the thermal conductivity of SiC is about 3.8 W/cm.K compared with 1.5 W/cm.K for Si. This means that a possible design of SiC devices with a significant reduction in the thermal

resistance of the die, which will consequently, as shown in (3.8), lead to increase the device power density for a given change in device operational temperature, ΔT, or reduce ΔT for a given power density [5]. ΔT is responsible for the power device reliability and lifetime, where the temperature cycles with large ΔT have the main contribution to the device damage and failure [52]. However, the extent of the benefit of reduced die thermal resistant R_θ depends on the overall thermal resistance of the device package [5].

$$\Delta T = P_D.R_\theta \tag{3.8}$$

$$R_\theta = \frac{1}{\lambda_\theta}.\frac{d}{S} \tag{3.9}$$

where P_D is the power density, d is the device thickness, S is the device area, λ_θ is the thermal conductivity and R_θ is the thermal resistance.

The electron saturation velocity in SiC is two times higher than that of Si, which takes advantage of faster switching. However, this benefit is limited by lower carrier mobility of SiC devices, for reference, the electron mobility of silicon is nearly 1400 cm^2/V.s in Si reduced to 950 cm^2/V.s in SiC. The lower channel mobility in SiC can be avoided by applying a higher gate voltage to increase the channel charge (reducing channel resistance). By applying a higher gate voltage, the electric field in the oxide is increased to the detriment of reliability. It is recommended to keep the electric field across the gate oxide lower than 3 MV/cm to avoid oxide reliability issues [47].

One of the challenges associated with the wider band gap is the higher built-in voltage, V_{bi}. The relation between V_{bi} with the intrinsic carrier concentration n_i, and the doping level which are dependent on the wideband energy is given by (3.10). This results in higher V_{bi} for SiC, about 2.8 V versus 0.7 V for Si [47].

$$V_{bi} = \frac{kT}{q}.ln(\frac{N_A N_D}{n_i^2}) \tag{3.10}$$

3.2. State-of-the-art SiC power device

3.2.1. P-i-N Diodes

Power rectifiers are one of the most important semiconductor devices developed for power electronics conversion systems. They are characterized by blocking high voltage during reverse bias and conducting high currents during forwarding bias. For optimum efficiency, they block high voltages with minimum leakage currents in one direction and permit as high as possible currents with low voltage drop in the other. The structure of a P-i-N power diode is shown in

Fig. 3.3, where it is formed by three layers: p^+ is the highly doped p-type layer; n^+ is the highly doped n-type layer; and n^- is the low doped n-type middle region in between causes two junctions: one is the n^-n^+, and the other is p^+n^- junction with wider depletion region and which dominates the performance of the diode [53, 54].

It should be noted that the n^- region is designed to minimize the on-state resistance within the limits of the avalanche breakdown voltage of the diode. The design of high blocking voltage P-i-N power diodes requires wider depletion width and lower doped drift layer to minimize the electric field at the junction below the critical electric field. However, the penalty is high drift region resistance. Based on the blocking voltage level, the low doped n-type layer n^- is designed in two ways: non-punch through (NPT) and punch through (PT) types. In NPT structure, the device is characterized by a triangle shape of the electric field and the depletion region is contained in the drift region formed by low doped region n^-. On the other hand, in PT type the electric field has a trapezoidal form and the depletion region reaches the borders of the drift region. Therefore, more even distribution of the electric field across the drift region is attained which consequently reduces the thickness of the drift region in PT devices; shorter drift region associated with PT devices yields smaller on-state resistance [53, 54].

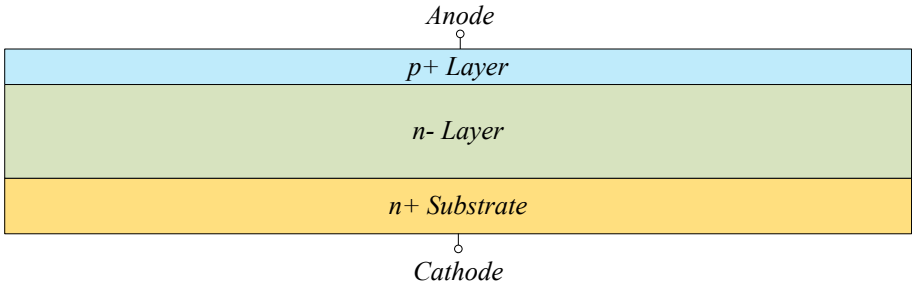


Figure 3.3: The cross section of a typical power PiN diode.

The on-state of a P-i-N power diode is dominated by the ohmic voltage drop due to the injection of the minority carrier in the lightly doped drift region, V_{Drift}, while the other part of voltage drop is the built-voltage on the device junctions, $V_{bip^+n^-}$ and $V_{bin^-n^+}$. Therefore, the voltage drop of P-i-N diode can be expressed as follows [53, 54]:

$$V_{Drop} = V_{bip^+n^-} + V_{Drift} + V_{bin^-n^+} \tag{3.11}$$

It should be noted that Si is the preferred material for P-i-N power diode fabrication, it has lower built-in voltage than that of SiC material which has higher bandgap energy.

The voltage drop across the drift region is given by [54]:

$$V_{Drift} = \frac{I_F W^2}{(\mu_n + \mu_p).Q_F} \tag{3.12}$$

where I_F is the diode forward current and Q_F is the stored charge in the drift region.

The drift region voltage drop is proportional to the carrier mobility, where an increase in carrier mobility leads to a lower forward voltage drop across the drift region. Therefore Si is favoured material for P-i-N power diode as SiC has lower carrier mobility value.

The stored charge in the drift region can be expressed as [54]:

$$Q_F = \frac{W^2 I_F}{V_{Drift}(\mu_n + \mu_p)} \tag{3.13}$$

An optimization between the conduction losses associated with the drift region drop voltage and the switching losses determined by accumulated charges is essential during diode design.

During the conduction period of P-i-N diodes, the drift region is flooded with excess minority carrier charges as the current density increases. Therefore, a low on-state voltage drop with high density currents is achieved. However, when the P-i-N diode is switched from on-state to off-state, the stored charge in the drift region should be removed first before extending the depletion region for blocking the reverse voltage. After removing the accumulated charges from the drift region, the voltage will increase rapidly to the blocking voltage determined by the value of DC-link voltage. Therefore, this reverse recovery charge causes losses in the diode at turn-off and also additional turn-on losses in the complementary device in hard switching topologies. The reverse recovery energy E_{rr} based on the area of the power losses triangle during the reverse recovery time, t_{rr}, is described in the reverse recovery current I_{rr} or in reverse recovery charge Q_{rr} expressed as follows [54].

$$Err = \frac{1}{2} I_{rr} V_{DC} t_{rr} = \frac{1}{2} Q_{rr} V_{DC} \tag{3.14}$$

It can be noted that the reverse recovery energy E_{rr} in P-i-N diodes is linearly proportional to accumulated charges in the drift region due to the need of large diffusion currents to achieve good on-state performance. Therefore, in high frequency applications, P-i-N diodes are not favourable due to their high switching losses.

3.2.2. Schottky Barrier Diode (SBD)

SBD is a unipolar device, where carrier transport relies on only the majority carrier. The structure of the Schottky diode with the indication of the contact metal, the drift region and the substrate is shown in Fig. 3.4. SBD is different from P-i-N diodes, where the SBD structure is formed by the connection of the Schottky metal to low doped semiconductor $n-$. Like P-i-N diodes, SBD uses the $n-$ layer for the drift region to support a high voltage withstanding capability and higher doped $n+$ layer. In SBD, when the forward bias voltage is applied, electrons are transferred from $n-$ semiconductor over the potential barrier into the Schottky metal; this creates a negative charge and a depletion region at the semiconductor surface. However,

SBD blocks the flow of carriers in the other direction due to the presence of Schottky barrier height [53, 54].

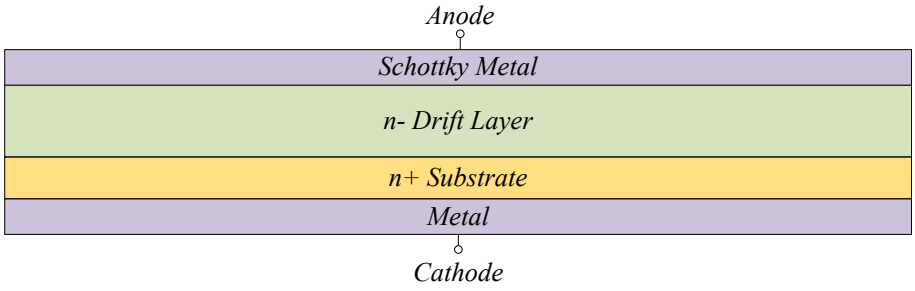


Figure 3.4: The cross-section of a typical power Schottky diode.

The on-state resistance presented in (3.4) is proportional to the square of V_{BD}, which means that the R_{on} in SBD is mainly dominated by the drift region for high breakdown voltages. The SBD on-state voltage drop is dominated by the threshold voltage and the voltage drop across the on-resistance of drift region during the forward conduction. Even the on-state threshold voltage in SBD is lower than that in P-i-N, and the ohmic resistance of drift region still higher. In addition, the leakage current under blocking voltage is inversely proportional to the on-state threshold voltage, which is proportional to Schottky barrier height. In order to maintain low on-state threshold voltage, the low Schottky barrier height is required which will increase the leakage current. Therefore, Si SBD is not feasible at high blocking voltages [53, 54].

However, employing SiC material in SBD enables design of devices with a thinner drift layer due to higher electrical field E_c and possible higher doping levels due to smaller intrinsic carrier concentration n_i for the same target blocking voltage capability. Therefore, SiC-SBD is superior to that Si P-i-N diode for high blocking voltage capability with reasonable on-state drift region resistance. These diodes have almost zero reverse recovery during turn-off state and low reverse bias leakage current even at high operating temperature [55].

3.2.3. Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET)

The MOSFET structure shown in Fig. 3.5 is formed by four layers, the highly doped n-type layer $n+$ at the drain which is used for other layers growth, low doped layer $n-$ which is grown epitaxially after the formation of $n+$ substrate, and the channel is formed by the diffusion cycles of p and $n+$ source regions. The gate is isolated from the MOSFET body by means of oxide SiO_2, and therefore, no possible minor carrier injection contributes to the current transport. Some parasitic elements presented in the structure of power MOSFET play a role in device reliability and switching performance. There are three parasitic capacitances; gate-to-source capacitance C_{GS}; gate-to-drain capacitance C_{GD} which is also called Miller capacitance; and drain-to-source capacitance C_{DS}. These capacitors are always described in

terms of input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss} as follows:

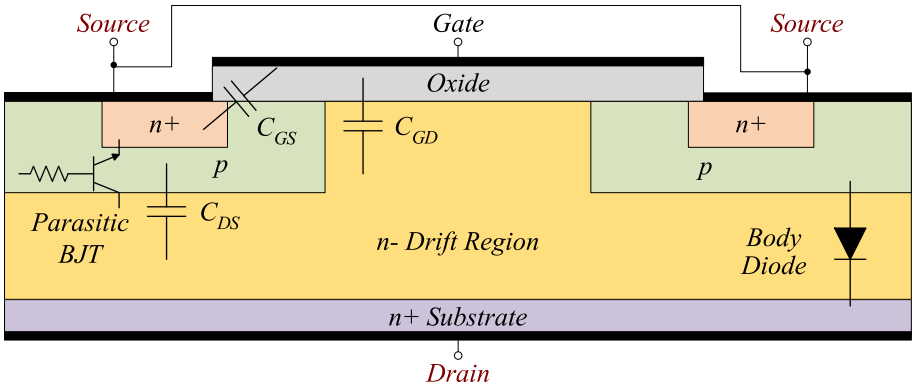


Figure 3.5: Typical cross-section of power MOSFET.

$$C_{iss} = C_{GD} + C_{GS} \tag{3.15}$$

$$C_{oss} = C_{GD} + C_{DS} \tag{3.16}$$

$$C_{rss} = C_{GD} \tag{3.17}$$

The C_{GS} arises from the overlapping of the gate electrode over $n+$ source region, p region and source metal. This capacitance is the highest among the three capacitances and almost independent of drain voltage V_{DS}. The Miller capacitance C_{GD} is due to the overlapping between the gate electrode over the drift region, and C_{DS} which is formed due to the overlapping of doped semiconductor layer p and the $n-$ drift region. C_{GD} and C_{DS} are dependent on drain voltage V_{DS} due to widening the depletion layer to support drain high voltages [53, 55].

A parasitic BJT is formed across $n+/p/n-$ regions in which the emitter is placed in the $n+$ layer, the base in the p region and the collector in the $n-$ drift region. If the base resistance of BJT is not sufficiently low, a significant voltage drop across the base resistance may activate the bipolar transistor and consequently lead to the device destruction as the device continues conducting through the BJT route. The risk of parasitic BJT turn-on can be eliminated by the inherent connection of p layer to the source metallisation. At the connection, a heavy $p+$ is added to reduce the BJT base resistance without changing the threshold voltage. However, this will initiate another parasitic element in the MOSFET which is the intrinsic body-diode. The parasitic power diode is formed across $p/n-/n+$ regions and behaves like P-i-N diode. This P-i-N body-diode is attractive in some applications require reverse current flow through the active power switch; it reduces the complexity and cost of using an external diode. However, the

essential problem with using a body-diode is a significant reverse recovery charge. Although the body-diode has a poor performance in comparison to P-i-N or Schottky power diodes at the same blocking voltage, it can be used in synchronous rectification to conduct only during the dead times between the complementary switches, hence, a reduction in conduction losses during the freewheeling is achieved [53].

The voltage drop during the on-state operation of power MOSFETs is given by:

$$V_{on} = R_{on}.I_{DS} \tag{3.18}$$

R_{on} is the total on-state resistance of the MOSFET between the drain and source, and its value at high voltage levels is dominated by the drift region resistance. The resistance of low doped n-type region is given by (3.4) which is function of square V_{BD} [55]. At high blocking voltages above 600V, Si MOSFET is not feasible due to the increase of on-state resistance during forward conduction [53, 56]. However, SiC MOSFET offers reasonable on-state resistance values even at higher blocking voltage, thanks to the higher electrical field and possible higher doping levels of WBG material [55]. The on-state voltage drop for the same current value does not change significantly with change in temperature; this is due to their higher bandgap energy [53, 54].

However, employing SiC material in SBD enables design of devices with a thinner drift layer due to higher electrical field E_c and possible higher doping levels due to smaller intrinsic carrier concentration n_i for the same target blocking voltage capability. Therefore, SiC-SBD is superior to Si P-i-N diode for high blocking voltage capability with reasonable on-state drift region resistance. These diodes have almost zero reverse recovery during turn-off state and low reverse bias leakage current even at high operating temperature [55].

Due to the absence of minority carrier transport in power MOSFETs, the operation of these devices is only limited by the rate of charge and discharge of the input capacitance C_{ISS} by the gate driver. In SiC power MOSFETs, the relatively smaller input capacitance is due to smaller chip area and there is no need for charge extraction from the drift region, making them superior at high switching frequencies. The switching energy of power MOSFETs can be given by the following [54]:

$$E_{sw} = E_{on} + E_{off} \tag{3.19}$$

$$E_{on} = \frac{1}{2}.V_{DS}.(I_{DS} + I_{RRM}).t_{ri} + \frac{1}{2}.V_{DS}.(I_{DS} + \frac{2}{3}.I_{RRM}).t_{fv} \tag{3.20}$$

$$E_{off} = \frac{1}{2}.V_{DS}.I_{DS}.t_{rv} + \frac{1}{2}.(V_{DS} + V_{pk}).I_{DS}.t_{fi} \tag{3.21}$$

3.2.4. Insulated-Gate Bipolar Transistor (IGBT)

The basic structure of an IGBT is shown in Fig. 3.6; it is similar to that of MOSFET except adding a layer of highly doped P-type down the MOSFET structure. It is seen that the IGBT is a voltage controlled device with a gate structure identical to the MOSFET. When the positive gate bias voltage is applied and exceeds the threshold voltage, the inversion layer in the $p-$region is formed and the electrons start to flow from $n+$ emitter to the n- drift region. The channel provides the drift current similar to that in MOSFET to supply the base drive current for the BJT transistor in IGBT structure. Since the BJT transistor is in forward bias, the $p+$ region injects holes into the n- drift region; hence a diffusion current based on minority carriers from the $p+$ at the collector side is flowing towards the p-layer. These minority carriers are involved in the current conduction to achieve IGBT devices with low on-state resistance at very high current densities. The presence of $n+$ buffer layer between the $p+$ and $n-$ drift region in the punch-through (PT) IGBT devices is essential for blocking higher voltages. This layer makes the electrical field distribution in a horizontal form and causes a narrow depletion region; hence thinner drift region is achieved for the same blocking voltage target compared to the non-punch-through (NPT) IGBTs [53, 55].

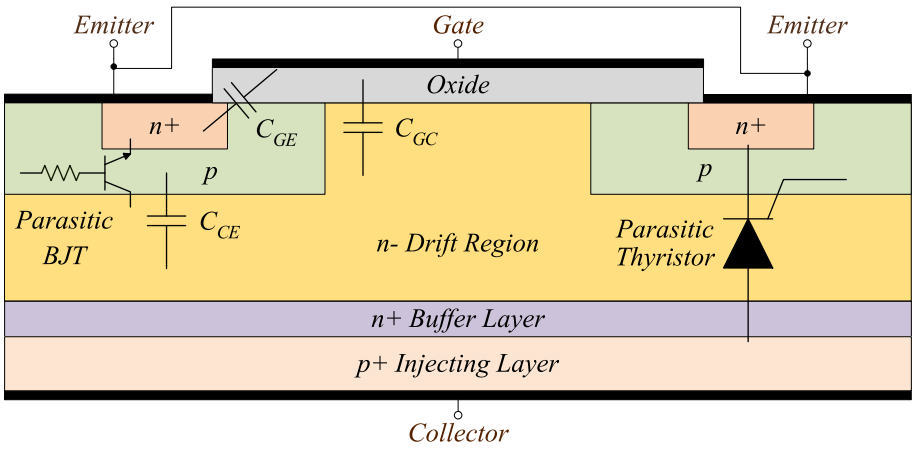


Figure 3.6: Typical cross-section of punch-through (PT) IGBT.

The maximum operating current of IGBT is limited by the presence of the parasitic thyristor in the IGBT structure. As shown in Fig. 3.6, the parasitic thyristor is formed between the $n+$ source region of MOSFET acting as the cathode of the thyristor, the p base region, the $n-$ drift region and the p collector region; this parasitic thyristor can be false activated and the IGBT current is no longer controlled by gate bias. This process is called the "latch-up" of the parasitic thyristor. During the conduction phase, the holes injected from $p+$ into $n-$ drift region flow into the p layer. This current produces a voltage drop across p layer resistance which is made much smaller than the diode built-in voltage (V_{bi}) at normal operating current levels. If the voltage drop is large enough, then parasitic thyristor latch-up will be initiated and the collector current will continue without gate control until the device fails [53, 55].

The on-state voltage drop across the IGBT is given by:

$$V = V_{on} + R_{on}.I_{CE} \tag{3.22}$$

Where V_{on} is the threshold voltage across the P-i-N diode in IGBT structure and R_{on} is the drift region resistance. At low collector current, the voltage drop across the IGBT is dominated by the voltage drop across the P-i-N diode, while at a larger collector current the voltage drop across the drift region is significant [53, 54].

During on-state, high minority carriers concentration is stored in the drift region, and to initiate the turn-off transition, these accumulated charges have to be removed from the device so that the device fully turn-off, which results in a gradual reduction in the collector current "tail current". This tail current causes large switching power losses because of high blocking voltage across the IGBT during this period. The turn-on and turn-off losses for IGBT is simplified by the following equations [54].

$$E_{on} = \frac{1}{2}.V_{CE}.(I_{CE} + I_{RR}).t_{ri} + \frac{1}{2}.V_{CE}.(I_{CE} + \frac{2}{3}.I_{RR}).t_{fv} \tag{3.23}$$

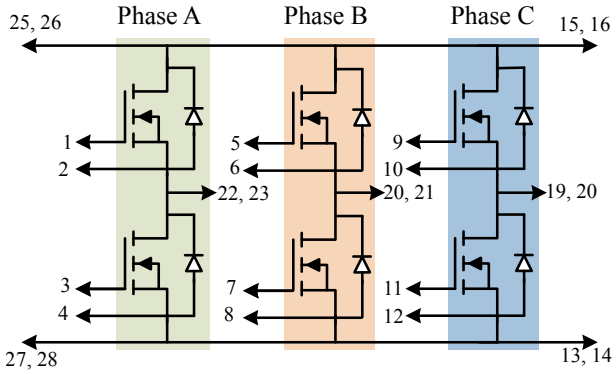
$$E_{off} = \frac{1}{2}.V_{CE}.I_C.t_{rv} + \frac{1}{2}.(V_{CE} + V_{pk}).I_C.t_{fi} + \frac{1}{2}.I_{tail}.V_{CE}.t_{tail} \tag{3.24}$$

The semiconductor characterization made thus far is important for this application. The comprehensive review of the available semiconductor materials and power devices shows that the SiC Schottky diode has a low on-state voltage drop and almost zero reverse recovery current. This feature of SiC diode can be seen as a great advantage in the inverter performance, especially if the inverter is required to operate at non-unity power factor, where the total loss increase is only due to the conduction losses through the Schottky diode as the power factor decreases. Further reduction in diode conduction losses can be achieved using synchronous rectification, where the load current freewheel through the SiC MOSFET as well; this benefit leads to a decrease the losses at high power loading where the conduction losses are dominant. In addition, power MOSFET can operate with low on-state resistance values even at higher blocking voltage and very fast switching speeds. These characteristics lead to a minimising of the inverter losses, especially under light-load conditions corresponding to higher wind speed distribution regions. Moreover, the higher operating temperature of the SiC MOSFET yields a smaller design of the inverter cooling system, and thus increases the converter power density. In addition, this section sets some power device physics background to build an electro-thermal model for SiC MOSFET necessary for device operation, system design, and power converter evaluation. The on-state voltage of the SiC-based MOSFET and the Schottky diode, and their switching energy are described here to be used in the device electro-thermal model.

3.3. Characterization of 1.2 kV SiC MOSFET three-phase module

3.3.1. 1.2 kV SiC MOSFET module

The 1.2 kV, 20A SiC six-pack three-phase module (CCS020M12CM2 from Wolfspeed) was inspected for static and dynamic characterization. Each switch in the module is formed by a single 1.2 kV, 80 mΩ SiC MOSFET (C2M0080120D), and a single 1.2 kV Schottky diode (C4D20120A). The power module has an internal gate drive resistance equal to 3.8 Ω connected in series to each module MOSFETs [1]. The schematic and the hardware of a 1.2kV/20A SiC MOSFET three-phase module are shown in Fig. 3.7.



(a) Schematic.



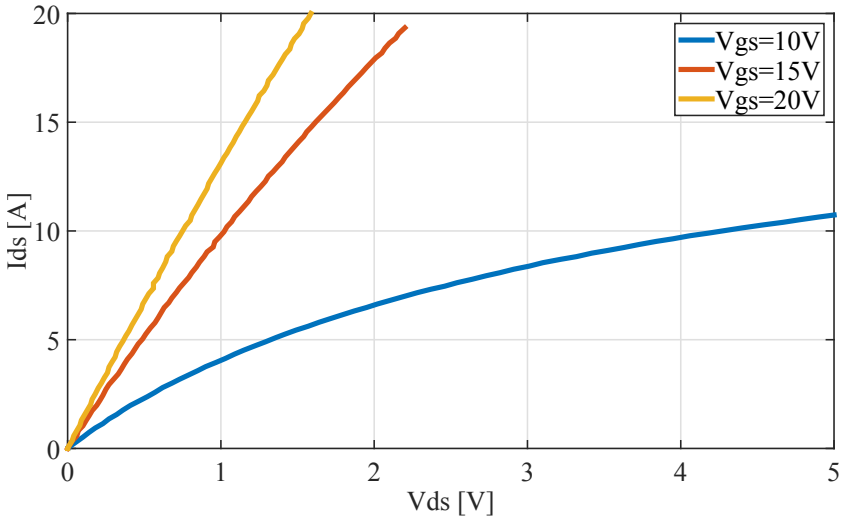
(b) hardware.

Figure 3.7: 1.2kV/20A three-phase module (a) Schematic with indications of module terminals, and (b) Power module hardware [1].

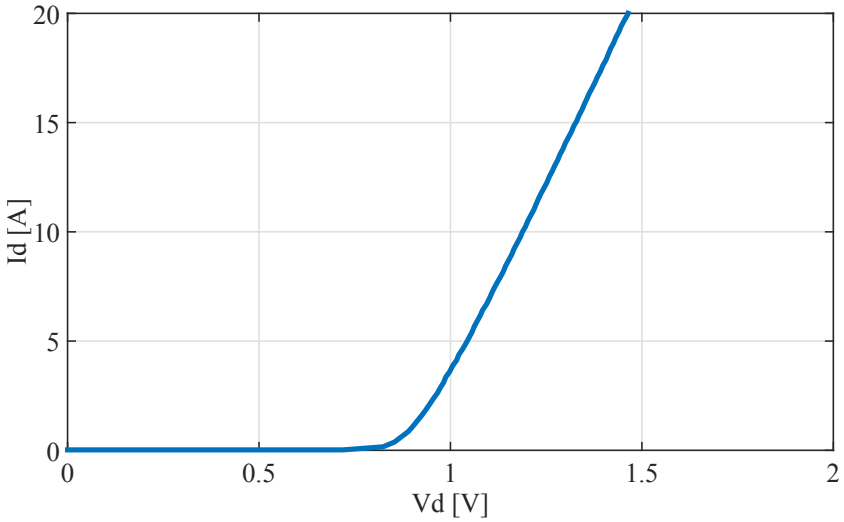
The device output and forward characteristics of SiC MOSFET and Schottky diode were measured by curve tracer, and four-wires (Kelvin connection) were used to guarantee accurate measurements. A hotplate was also utilized for the measurements at different baseplate temperatures, i.e. 25 ^oC and 90 ^oC. Once the required baseplate temperature was reached, the measurements were performed as quickly as possible to mitigate the device self-heating.

Fig. 3.8 reports the measured MOSFET output and Schottky diode forward characteristics. Based on these curves, it can be observed that SiC MOSFET exhibit good on-state performance even at a gate-source voltage of only +15 V which is the reference voltage level for driving IGBT devices. However, for a better performance, a gate-source voltage of +20 V is chosen

for driving SiC MOSFETs gate driver in inverter operation. In addition, Schottky diode is well designed to have a low forward-voltage drop, and thereby, it has a comparable conduction performance to the Si diodes in the same voltage class.



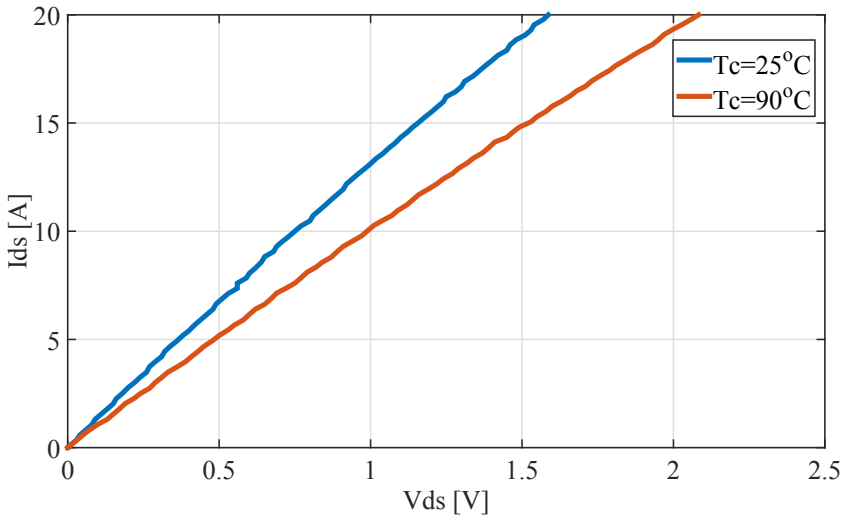
(a) MOSFET.



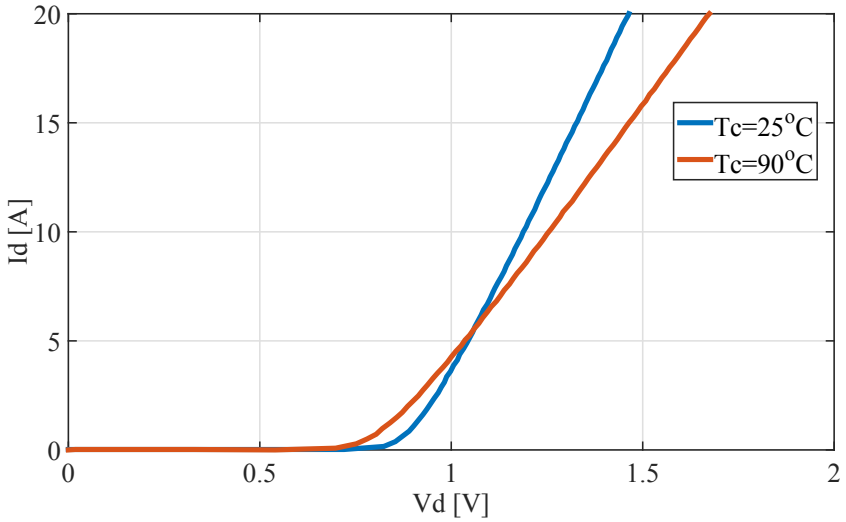
(b) Schottky diode.

Figure 3.8: Measured output characteristics and forward characteristics of (a) MOSFET , and (b) Schottky diode ($V_{gs} = -5V$), at ambient temperature.

Fig. 3.9 show the MOSFET and diode output characteristics, respectively, measured at two different baseplate temperatures, 25 and 90 ^oC. As can be seen, the effect of temperature on the on-state performance becomes more pronounced at higher current levels; however, diode conduction starts already at current levels between 5 and 10 A and can help contain current and temperature related decrease of performance compared to reliance on the MOSFET body-diode and synchronous rectification.



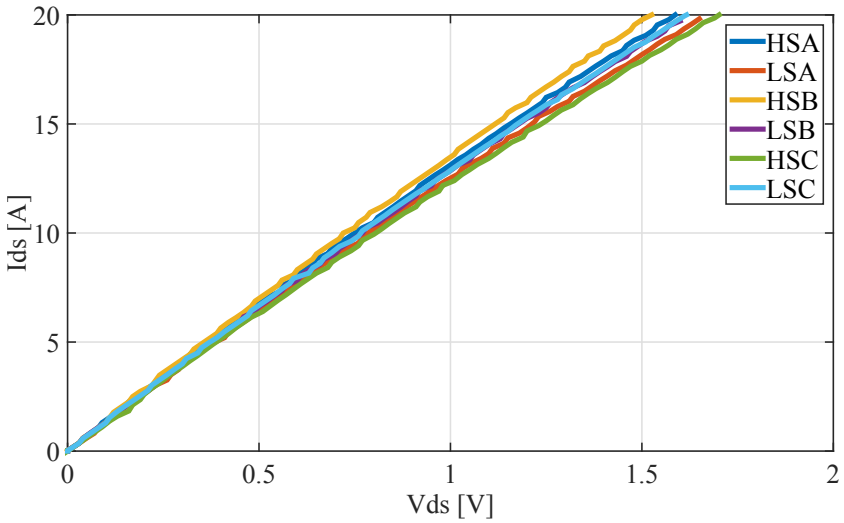
(a) MOSFET.



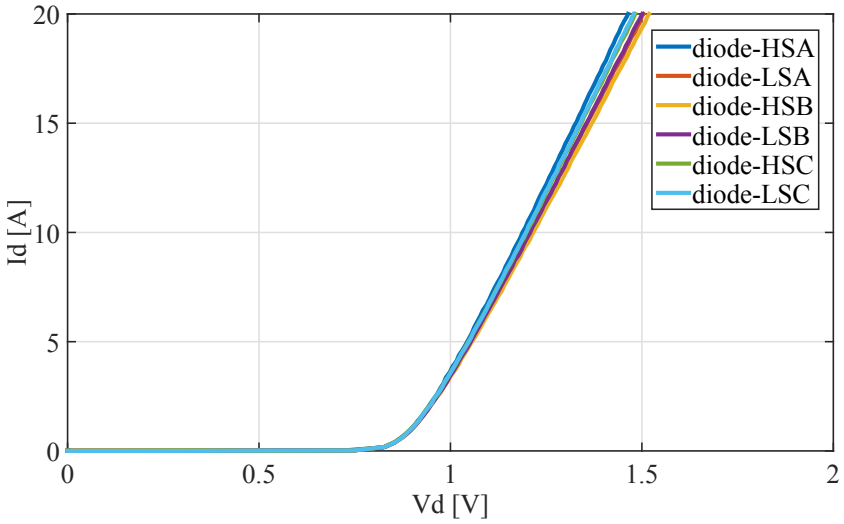
(b) body-diode.

Figure 3.9: Temperature dependency of (a) MOSFET output characteristics, and (b) Schottky diode forward characteristics.

Fig. 3.10 shows the measured spread over six devices; the reported differences in the MOSFETs output characteristics are mainly due to a slight difference in threshold voltage. In addition, the spread in the Schottky diode forward characteristics was satisfied at this voltage level.



(a) MOSFET.



(b) Schottky diode.

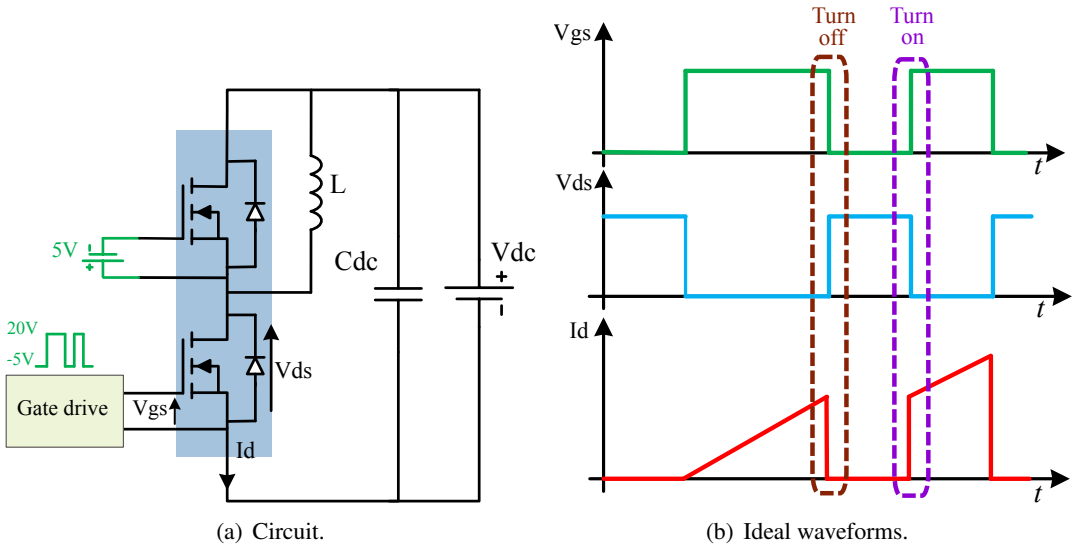
Figure 3.10: Measured spread in (a) MOSFET output characteristics, (b) Schottky forward characteristics, for six devices at $V_{gs} = 20V$.

3.3.2. Switching characteristics of 1.2kV/20A SiC MOSFET module

The parametric switching characterization of SiC MOSFET over load current, baseplate temperature and different gate driver resistors are performed experimentally using the double pulse test (DPT). Two pulses with variable widths are generated and then applied to the gate drive input of the lower MOSFET (device under test, DUT) as shown in Fig. 3.11-a. The MOSFET is driven by double pulse signal with +20 V level for turn-on and -5 V for turn-off, while the upper MOSFET is always kept off by applying -5 V between gate and source. The first pulse controls the current rise in the inductor as shown in Fig. 3.11-b, and the pulse width Δt can be adjusted to set the desired current level as seen in (3.25). Once the current reaches the target

level, the MOSFET (DUT) is switched off and the corresponding MOSFET switching transient event can be observed. During the short off period, the inductor current can be taken as a constant current. By this way, the MOSFET turns on at the same current and voltage levels during switching off, and consequently, the turn-on switching waveforms can be monitored. Finally, when the smaller pulse finishes, the inductor current decays slowly through the Schottky diode of the complementary switch.

$$I_L = \frac{V_{dc}}{L} \times \Delta t \tag{3.25}$$



(a) Circuit. (b) Ideal waveforms.

Figure 3.11: DPT (a) Circuit schematic diagram, and (b) Ideal circuit waveforms.

The corresponding hardware setup is shown in Fig. 3.12, where film capacitors are the only technology used to implement the input bulk capacitor with a total value of 56μF, distributed into two groups to have a symmetrical parasitic inductance between the three half-bridge legs. Moreover, the DC-link was designed in a way to minimize the stray inductance based on magnetic field cancellation [57]. The MOSFET (DUT) was mounted on a hotplate and the temperature was controlled to maintain the desired case temperature. An air core inductor with a value of 400 μH was designed to ensure higher test currents without saturation and to guarantee smaller equivalent parallel capacitance.

The circuit components and the details of instruments are given in Table 3.2 and Table 3.3, respectively, the voltage probe was deskewed with reference to the current probe to avoid any errors in power loss measurements due to delayed signal.

The voltage rise or current rise time is the time interval for the drain voltage/current to rise from 10% to 90% of the final value. Similarly, the voltage drop or current drop time is the time interval for the drain voltage/current to drop from 90% to 10% of its final value [1]. The

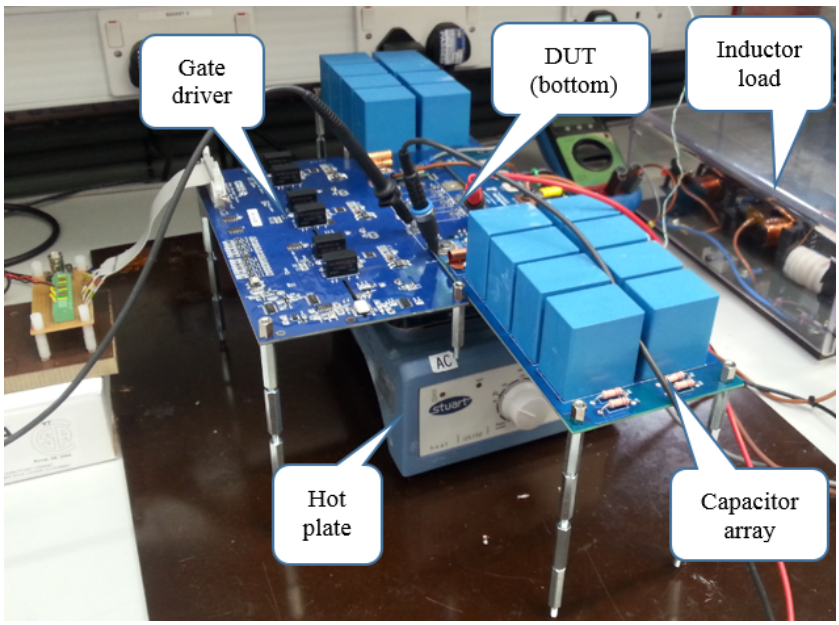


Figure 3.12: DPT circuit hardware setup, with detail of capacitor bank, inductive load, gate drivers and device under test (DUT) mounted on hotplate.

Table 3.2: Components details.

Component	Model	Value
Load inductor	Air core	400μH
Input bulk capacitor	B32676G	14μF$\times$16

di/dt is the slope of the drain current measured at 50% of the final current, while the dv/dt is the slope of the drain voltage measured at 50% of the final drain voltage. The switching energy is measured by integrating the product of device voltage (V_{ds}) and device current(I_d). The interval of integration time is taken from zero current to zero voltage during the turn-on and from zero voltage to zero current during the turn-off [58].

The turn-on and turn-off switching transient waveforms of SiC MOSFET power module at DC-bus voltage of 700 V, maximum switch current of 20 A, gate drive resistance of 10 Ω and at room temperature are shown in Fig. 3.13, where these results are obtained consistently for repeated switching cycles when considering particular operating conditions such as the same load current, DC-link voltage, gate drive resistance, gate drive voltage level, junction temperature, the type of freewheeling diode and the dc-link and PCB configuration. The current overshoot was referred to the Schottky diode reverse recovery current of the opposite switch which assumed equal to zero by the manufacturer [1]. Indeed, it is mainly due to the MOSFET stray capacitance in the presence of high dv/dt, i.e dv/dt=28 V/ns here. The turn-on transient has a current overshoot of 11 A, di/dt of 4.9 A/ns and oscillations with frequency around 42 MHz due to the stray inductance of the switching loop (PCB, DC capacitors and module

Table 3.3: Instruments details.

Component	Model	Bandwidth	Deskew
Current shunt resistor	SDN	400 Mhz	0 ns
Differential Voltage probe	701926	50 Mhz	12 ns
Oscilloscope	Lecroy	600 Mhz	with deskew
Hotplate	US150	–	–

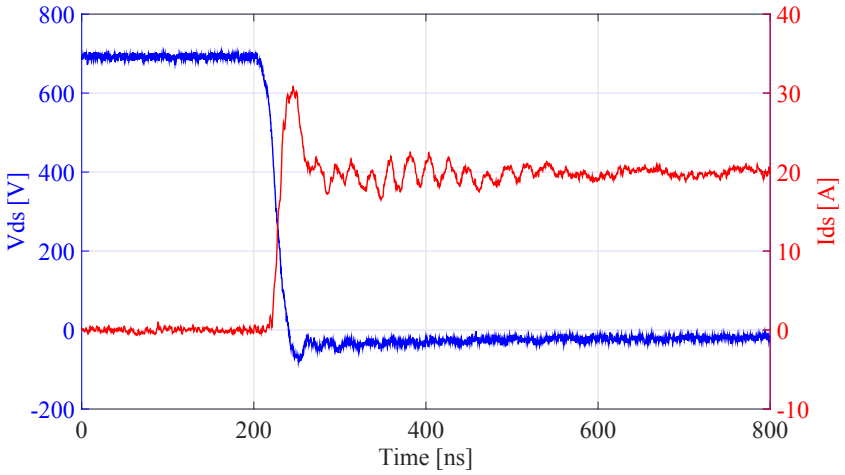
itself). During the turn-off, the drain voltage transition has an overshoot of 77.6 V, and di/dt of 0.7 A/ns. From this, the switching loop inductance is estimated equal to $77.6/0.7 = 110.8$ nH. The module stray inductance is 30 nH [1], the equivalent series inductance (ESL) of the capacitor array is 3.5 nH. Therefore, the PCB trace inductance can be estimated by subtracting the module and capacitor array inductances from the total stray inductance, resulting in 77.4 nH.

The switching loop inductance is mainly controlled by the module package and PCB layout and becomes a major contributor to voltage overshoot. In this case, the module package shares about 27% of the total stray inductance. If the reduction in the package stray inductance provided by future SiC modules reduces by up-to e.g. 50% of the existing module package, the expected overshoot will decrease by just 13.5%. As a result, the PCB layout and the type of DC-link capacitors are still the limiting factor on the high switching frequency performance of the converter, while the module package impacts the gate drive performance.

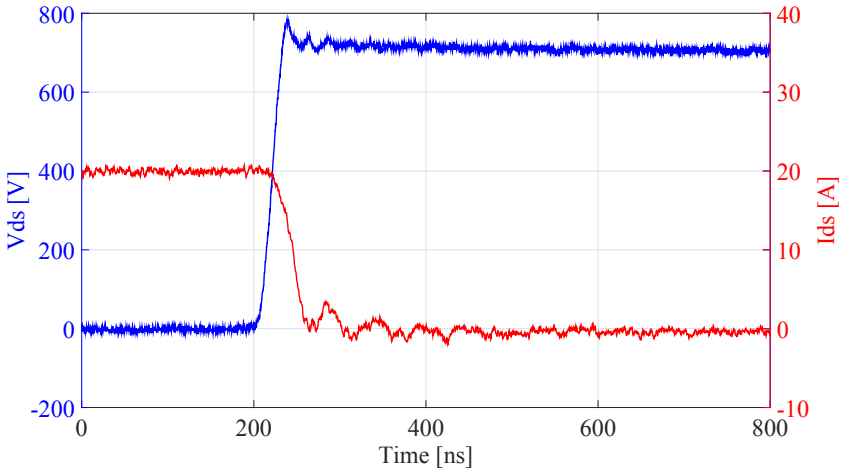
The variation of switching energy loss with different baseplate temperature at different load currents is shown in Fig. 3.14. It is clear that the junction temperature has a minor effect on both turn-on and turn-off energy losses of SiC MOSFET devices. With higher baseplate temperature, the turn-on switching losses slightly decrease. This is due to the decrease in device threshold resulting in faster turn-on transition. However, the turn-off energy loss increases slightly with the increase of baseplate temperature, but with a smaller rate than the decrease in turn-on switching losses. This feature can help to increase the system level power density by joining the optimization of the heat-sink and switching frequency.

Fig. 3.15 depicts the turn-on and turn-off switching energy loss by varying the gate drive resistance at different load currents. The measured results show that the gate driver resistance has a significant effect in both turn-on and turn-off switching losses; the switching energy loss increases by the increase of the gate driver resistance because the switching transient time of the switch reduces. On the other hand, lower gate drive resistance yields lower switching losses but increases the oscillations in the device current and voltage waveforms. The gate resistances at turn-on and turn-off are intentionally chosen differently, so as to optimise each transition independently.

The gate drive resistance was chosen as a trade-off between the power losses and di/dt



(a) Turn-on.



(b) Turn-off.

Figure 3.13: Switching characteristics of SiC MOSFET: (a) Turn-on, $R_{g,on}$=10 Ω and (b) Turn-off, $R_{g,off}$=10 Ω, at room temperature

during the transient. Higher values of di/dt resulted in high transient over-voltage across semiconductors, while lower values excessively slow down the switching process, thus increasing the power dissipation, as demonstrated in Fig. 3.15 and Fig. 3.16. Therefore, a gate driver with separate gate resistors of 10 Ω and 5 Ω for turn-on and turn-off, respectively was selected.

Fig. 3.17 shows a plot of the turn-on and turn-off times as a function of the load current, for a bias voltage of 700 V and at a baseplate temperature of 25^oC, where a longer turn-off switching time is observed as the current decreases. This behavioural feature needs to be duly taken into account in setting system level design parameters, such as, for instance, the dead-time used in-between commutations, which, if constant, needs to be chosen for the worst case. In this design, 200 ns was kept for the turn-off time dependency and 300 ns to ensure fully damped switching oscillations. Therefore, 500 ns dead-time was chosen for optimising the system operation.

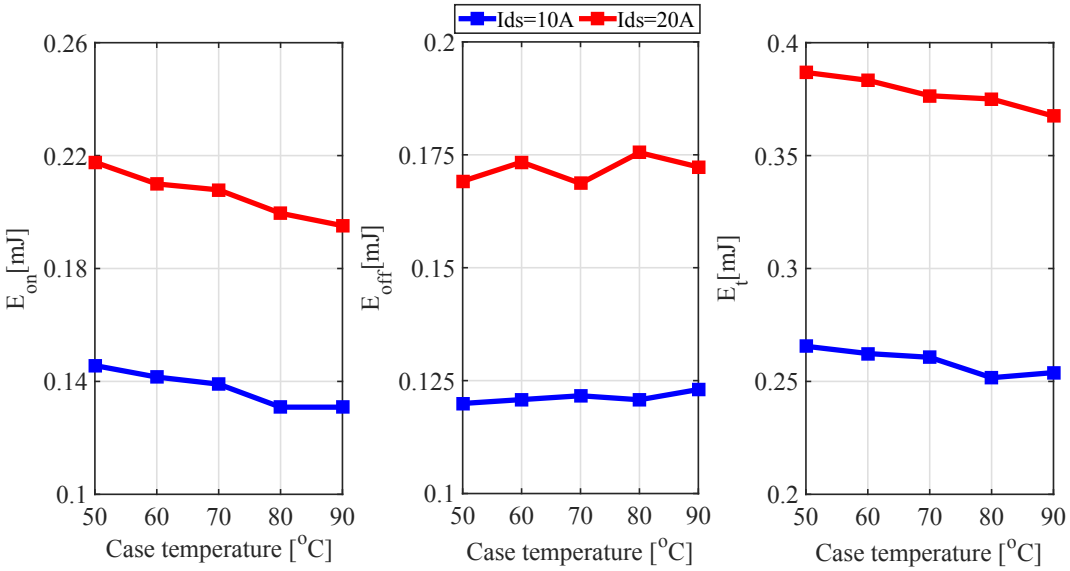


Figure 3.14: Measured switching energy versus baseplate temperature at different currents, $V_{ds} = 700V$ and Rg=10 Ω.

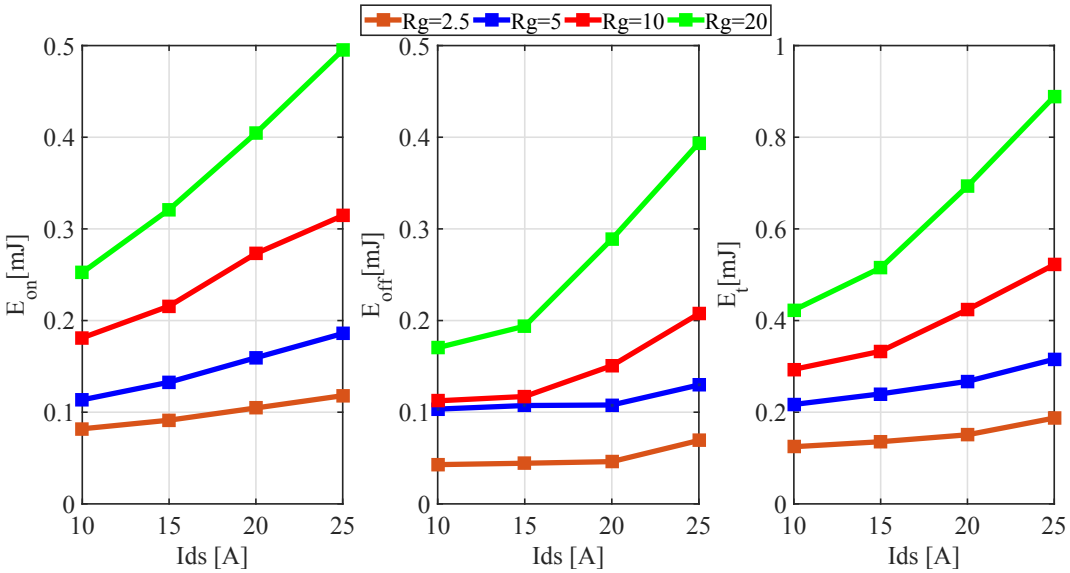


Figure 3.15: Measured switching energy versus drain currents at different gate resistance values, $V_{ds} = 700V$ and $T_c = 25^oC$.

In order to prevent shoot through, the dead-time between complementary switches in a half-bridge configuration is required. However, the dead-time introduces additional losses when its value becomes significant in a switching period. Although negative gate-source is required for SiC MOSFET due to its low threshold voltage, it will cause a significant voltage drop across the MOSFET during dead-time instants. Therefore, dead time should be kept as small as possible to avoid additional conduction losses, especially at high switching frequencies where the dead-time becomes a significant part of the switching period.

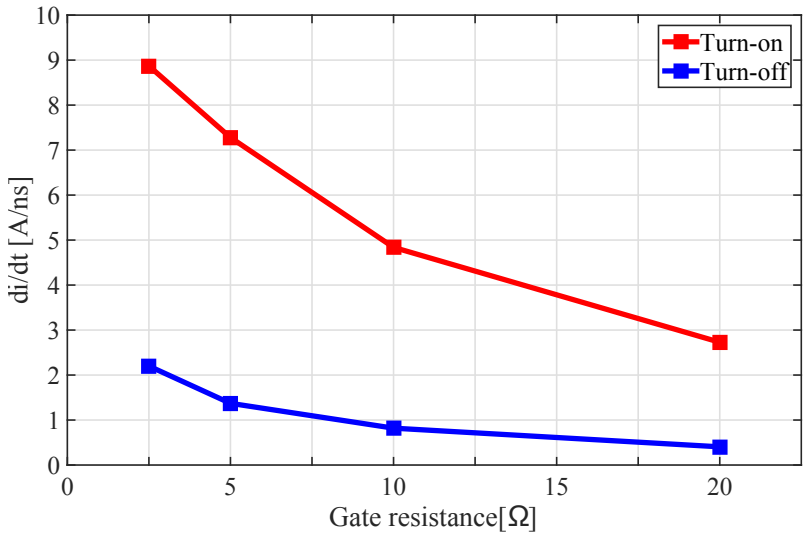


Figure 3.16: di/dt values with different external gate resistors, $V_{ds} = 700V$, $I_d = 20A$ and $T_c = 25^oC$.

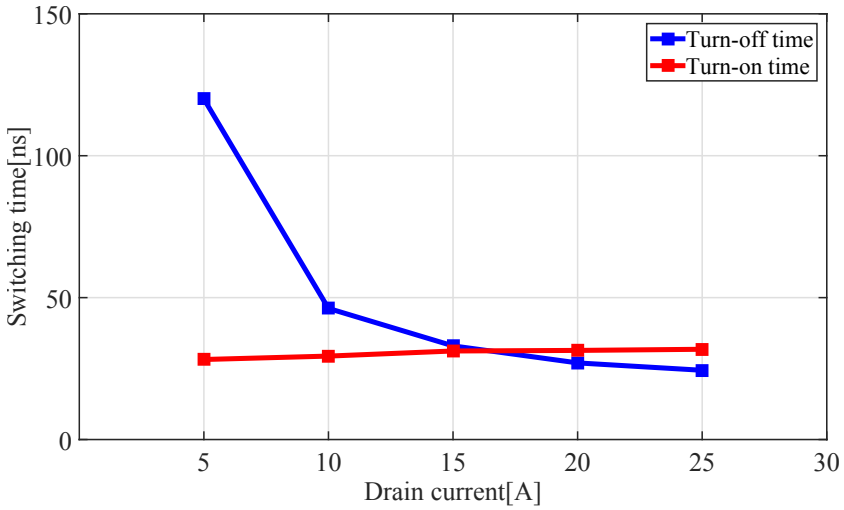


Figure 3.17: Measured turn-on and turn-off switching time over device current at Vds = 700V , Rg,on =10 Ω, Rg,off=5 Ω, Tc= 60^oC.

3.4. Conclusion

In this chapter, the fundamental properties of wide-bandgap materials were discussed compared to the state-of-the-art Si material, which is still the most widespread material for the main substrate in power semiconductor devices. The operating principles of power semiconductor devices including P-i-N diode, SBD, IGBT, MOSFET have been presented, with aim to show the superior device characteristics of WBG devices over Si. It is clear that SiC is the promising material for WBG power device development. The static and dynamic characterization of the six-pack power module CCS020M12CM2 including a power MOSFET with anti-parallel Schottky diode was presented. As can be seen, the effect of temperature on the

on-state performance becomes more pronounced at higher current levels; however, a diode can help contain current and temperature related decrease of performance compared to reliance on the MOSFET body-diode and synchronous rectification. As far as the switching performance is concerned, the measured turn-on, turn-off and total switching energy as a function of power module case temperature show a certain dependence of the switching efficiency on the load conditions; however, the extremely contained dependence on temperature is also of note: this is an important characteristic of SiC devices compared to their silicon equivalents (e.g., IGBTs), which can be exploited in the system design optimization. In particular, it has been shown the switching energy is independent of baseplate temperature over a wide range of temperature, which means a stable operation of wind inverter even at higher temperature values. The power loss is dependent on the gate resistor, so that, the gate resistances at turn-on and turn-off are intentionally chosen different, so as to optimise each transition independently.

Chapter 4

Preliminary Evaluation of SiC Wind Inverter

This chapter presents the design of SiC based three-phase wind inverter to deliver an evaluation of SiC MOSFET devices in terms of power losses and efficiency under different conditions, i.e. various power loading, different switching frequencies and different heat-sink temperatures. In addition, the reactive power handling feasibility was demonstrated as well at non-unity power factor inverter operation resulting in a very small dependency of SiC inverter power losses on the power factor.

4.1. Test setup

In this section, a SiC-based three-phase inverter has been designed and built in the lab to deliver a through characterization performance of 1.2kV/20A SiC MOSFET power module (CCS020M12CM2 from Wolfspeed [1]). The inverter is a 12 kW 2L 3-phase used for small-scale wind turbines, and its parameters are shown in Table 4.1. To deliver a demonstration of the inverter characterization, a series of measurements of power losses and efficiency are performed for different power loading up to 12 kW input power at different heat sink temperature of 60 ^{o}C to 90 ^{o}C, and different switching frequency from 16 kHz to 32 kHz. A dead-time of 500 ns and DC-link voltage of 720 V are considered. The test was made with a variable three-phase resistive load to emulate the grid connection at different power loading.

The test setup schematic is shown in Fig. 4.1, the converter is powered by a DC power supply, and the power losses are measured by Yokogawa WT3000E precision power analyzer. In this stage to assess the performance of the inverter power cell based on six-pack SiC power module, the voltage measurements are set before the filter inductor L_f to exclude the inductor losses from the assessment. The input current for the power analyzer was measured before

Table 4.1: Converter parameters and test conditions

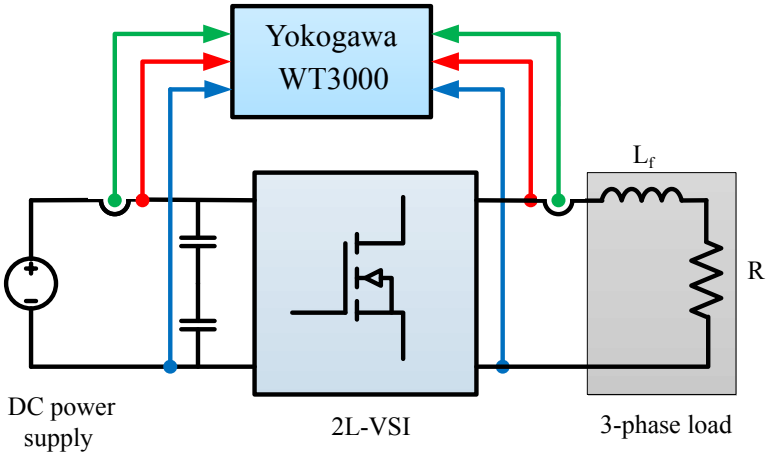
Parameter	Value
Input power rating, P_{in}	12 kW
DC-link voltage, V_{DC}	720 V
DC-link capacitor C_{DC}	56 μF
Filter inductance L_f	3 mH tap
Grid phase voltage, V_g	230 V
Switching frequency, f_{sw}	16-32 kHz
Dead-time	500 ns
Devices	CREE CCS020M12CM2

the DC-link bank due to the implementation of DC-link capacitors close to the power module in the PCB design to minimize the parasitic inductance in the switching loop. Therefore the losses of the DC-link are included in the power cell measurements. However, the losses of the DC-link based on film capacitor are too small even at higher switching frequencies and can be ignored.

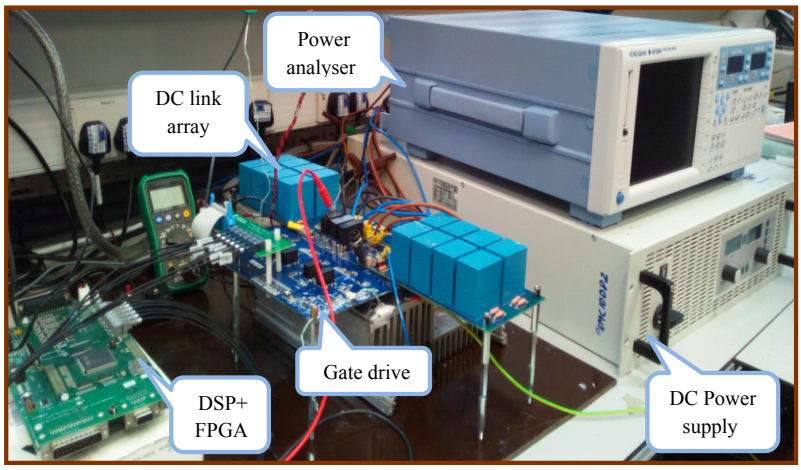
The DC-link PCB was designed based on a planar structure to minimize parasitic inductance in the commutation loop at high switching speed, and two sets of DC link is to have an asymmetric parasitic inductance between the individual half-bridge sections. High-frequency film capacitors are fixed very close to inverter legs used to provide minimum voltage overshoots. The output inductor in this section is formed by off-the-shelf 3-phase inductor for the purpose to provide current filtering for a range of switching frequencies, i.e from 16 kHz to 32 kHz. The carrier and modulating signals are performed using a control platform based on Texas Instrument TMS320C6713 floating point digital signal processor (DSP) and Actel ProAsic3 field programmable gate array (FPGA), and then processed to the gate driver to generate the required switching sequence. The gate driver board is kept very close and directly connected to the power cell in order to minimize the driving loop and reduce the noise pick-up at the gate signals.

4.1.1. DC-link capacitor design

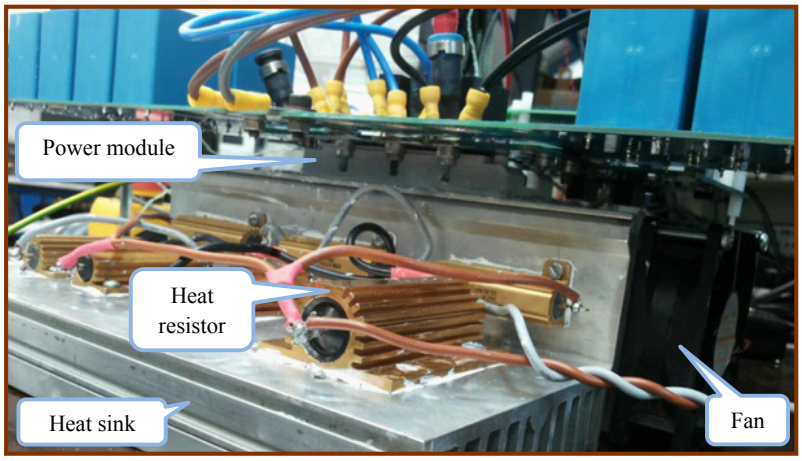
The DC-link capacitor in the three-phase system is used to minimize the high switching frequency components of the PWM converter current, as well as required for energy storage [59]. The DC-link capacitance by imposing a maximum current ripple to be carried by the capacitor and a peak-peak DC-link voltage ripple which is limited to say 2% of the DC-link voltage (or smaller), otherwise an oscillation in the extracted power due to the voltage ripple will occur.



(a) Schematic



(b) Hardware



(c) Temperature control

Figure 4.1: Three-phase Inverter test setup.(a)Schematic (a) Hardware, and (b) Heat sink temperature control technique.

The minimum DC-link capacitor value is given by [60]:

$$C_{dc,min} = \frac{I_C}{2\pi \times f_s \times V_{ripple}} \tag{4.1}$$

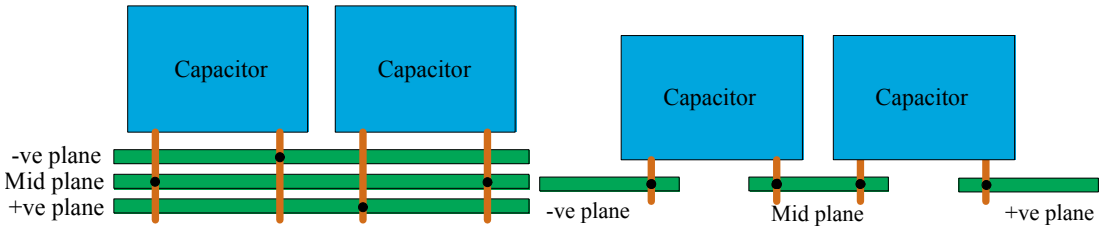
The RMS capacitor ripple current is given by [59]:

$$I_C = I\sqrt{\frac{20\sqrt{3}}{9Mpi} - 1} \tag{4.2}$$

where M is the modulation index, I is ripple free DC output current.

For capacitor current in three-phase systems, such a six-switch PWM converter, no low-frequency current will present and the current stress is due to high switching frequency components calculated by (4.2) [59]. Therefore, metalized polypropylene film capacitors is a good choice for the DC-link to guarantee low equivalent series resistance (ESR) and low equivalent series inductance (ESL) which means low loss characteristics and low parasitic inductance at high switching frequencies.

The DC-link is designed to minimize the stray inductance based on magnetic field cancellation provided by the planar structure as shown in Fig. 4.2-a. Planar traces offer a significantly lower stray inductance based on magnetic field cancellation in comparison with coplanar traces depicted in Fig. 4.2-b. Planar traces layout is recommended in designing the power circuit for SiC MOSFET module based inverters; on the other hand, the coplanar structure is popular in Si IGBT module applications. Both configurations allow series connection of parallel capacitor sets to offer the required test voltage and to provide a midpoint connection.



(a) Planar structure (b) Coplanar structure

Figure 4.2: DC-link structure.(a) planar, and (b) coplanar.

The DC-link capacitors were shared into two sets to have a symmetrical parasitic inductance between the three half-bridge legs, as Fig. 4.3 shows. The concept of magnetic field cancellation is also applied between each parallel rows of capacitors. Moreover, as shown in Fig. 4.4, the PCB is designed in a way that the inner polarity of each pair of series capacitors connected to $-$ve plane and the $+$ve plane is switched while the outer capacitor terminals are connected to GND. This leads the current to flow in opposite directions through the parallel capacitor rows as indicated by black arrows and helps in magnetic field cancellation.

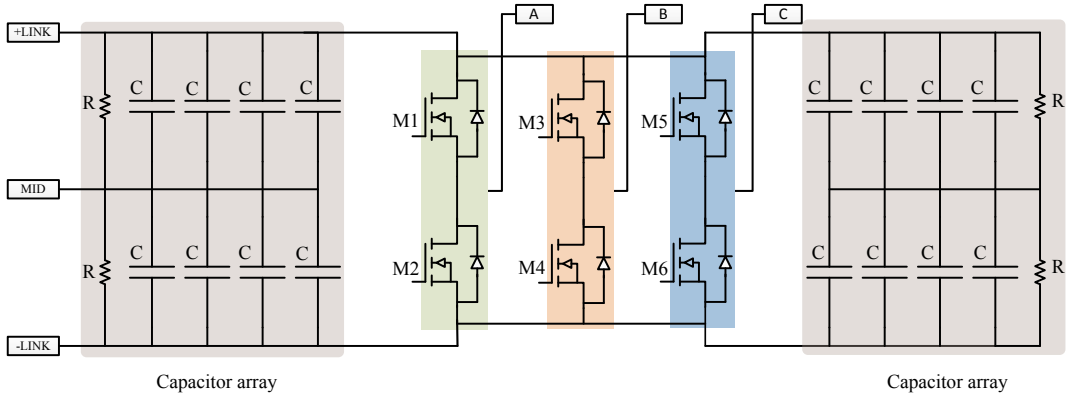


Figure 4.3: Simplified schematic of the DC-link capacitor.



Figure 4.4: DC link PCB for SiC 3-phase inverter.

The DC-link capacitors consists of 16 film capacitors each with 14 μF, 630 V rating, two sets of eight parallel capacitors connected in series, giving a total capacitance of 56 μF with total voltage withstand capability of 1260 V. Each capacitor has a contribution of 14 nH equivalent series inductance (ESL) [61], and the total parasitic inductance of the capacitor array is 3.5 nH. In addition to the first stage of DC-link film capacitors, high-frequency decoupling capacitors are mounted directly between DC+ and DC- close to each phase leg switch pair with a value of 15 nF to provide a low impedance, high-frequency current loop. Practically, this can help to prevent destructive voltage at turn-off.

The equivalent series resistance (ESR) of the DC-link capacitor bank over the range of frequencies is shown in Fig. 4.5, which contributes to the power losses of the system. In the experimental setup, the DC-link power losses cannot be measured directly due to the integration of the DC-link capacitors in the PCB that is designed to accommodate the SiC power module. Therefore, the DC-link power loss using the ESR in Fig. 4.5 is calculated over the relevant range of frequencies (16 kHz to 32 kHz) and the result is shown in Fig. 4.6. The effect of the DC-link power loss is insignificant at the rated output power over the operation range of switching frequencies (about 0.14W power loss), and therefore can be ignored in the inverter power cell efficiency measurements.

Power electronics conversion systems for the wind turbine are mainly based on a DC-link capacitor which occupies a significant part of the converter volume. The volume of the DC-link capacitor at different switching frequencies is derived by a curve fitting of the actual design

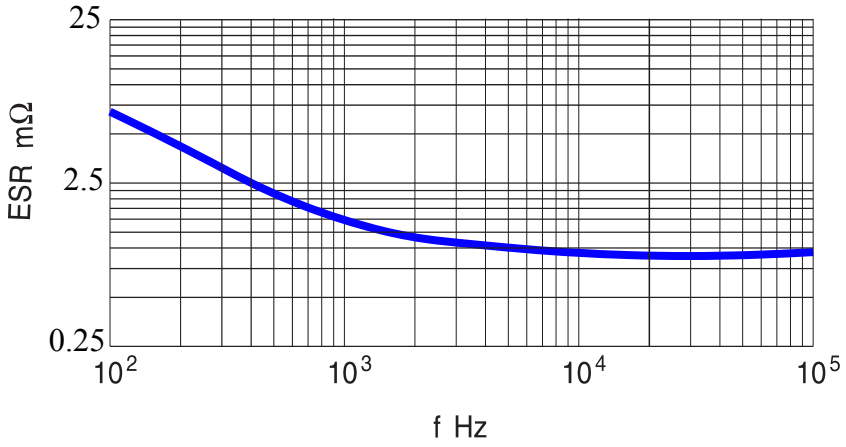


Figure 4.5: The resistance-frequency profile of the DC-link capacitor bank.

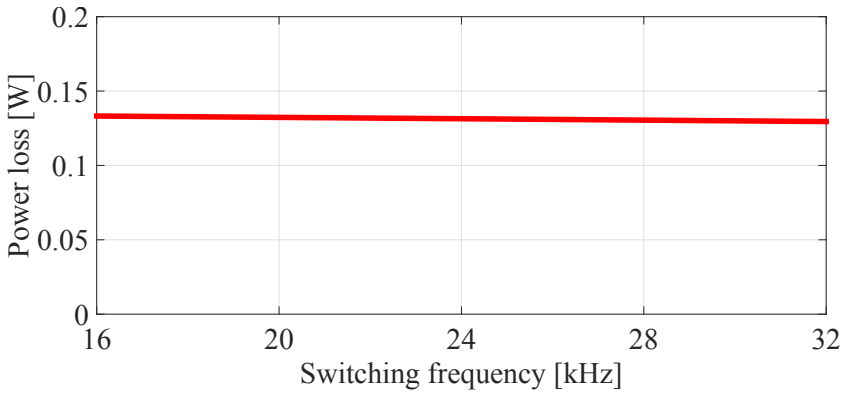


Figure 4.6: The DC-link capacitor bank power loss versus the switching frequency at full power level.

based on MKP film capacitor series as shown in Fig. 4.7 and given by:

$$V_{cap} = 5.962 \times f_{sw}^{-0.8929} \tag{4.3}$$

4.1.2. R-L load

To assess the performance of a 2L-VSI in a 3-phase grid-connected configuration, the grid connection at different power loading was emulated by a variable 3-phase resistive load with values shown in Table 4.2 to keep the grid phase voltage constant at 230 V at different power loading. The corresponding resistive load setup is shown in Fig. 4.8, with power dissipation capability up to 6.75 kW/ph.

The minimum inductance of a 2L inverter topology is given by (4.4) [62]. The inductor must be designed to ensure the maximum output ripple current within 20% of the peak output

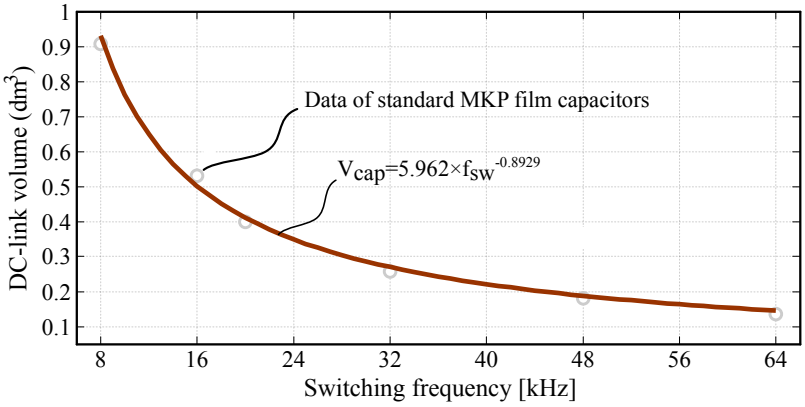


Figure 4.7: DC link volume at different switching frequency.

Table 4.2: Load resistors at different power loading values

Load resistors, $R_L[\Omega]$	Power loading, $P_L[\%]$
13.33	99.21
15	88.86
45	29.62
75	17.77
135	9.87
440	3.03

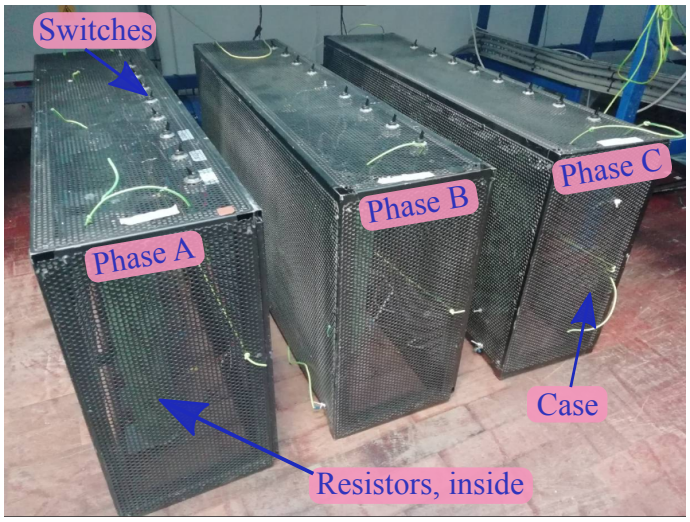


Figure 4.8: Picture of three-phase variable resistive load.

current I, in which the wind turbine feeds the maximum output current.

$$L_{min} = \frac{V_{dc}}{4 f_{sw} \triangle I_{PP}} \tag{4.4}$$

where V_{dc} is the DC-link voltage, f_{sw} is the switching frequency and I_{PP} is the peak to peak switching ripple in the filter output current.

The off-the-shelve 3-phase inductor shown in Fig. 4.9 has been used to provide current filtering in compliance with power quality standards in the range of switching frequencies, i.e. 16 kHz to 32 kHz. The 3-phase inductor specifications are listed in Table. 4.3, where the inductor uses a laminated iron core and a foil winding with a current rating of 32 A. The 3-phase inductor offers four different taps (0.5, 1, 3 and 5 mH per phase), and here the tap of 3 mH was used. The corresponding small signal analysis of the inductance of 3 mH was performed using impedance analyser, and the resulting inductance characteristics are shown in Fig. 4.10, where all the inductance values at the test switching frequencies are presented.

The minimum required inductances and the test inductance values at different switching frequencies are listed in Table 4.4, where all the test values are within the specified limit.

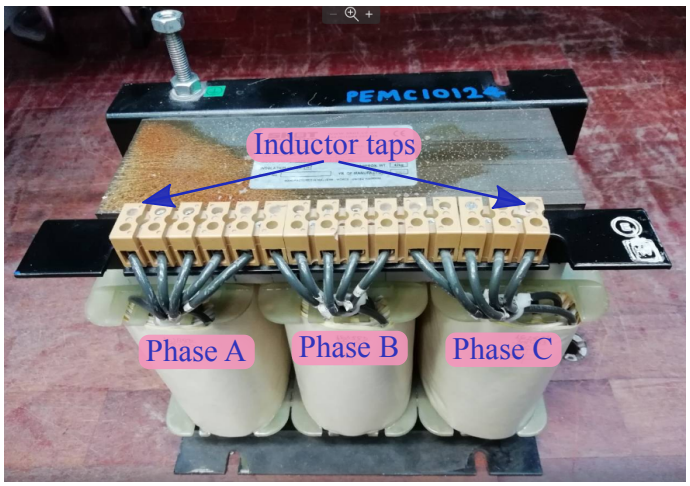


Figure 4.9: Picture of three-phase inductor.

Table 4.3: Specifications of the 3-phase inductor

Item	Value
Inductance	taps at 0.5/1/3/5 mH/ph
Rating current	32 A RMS
Line frequency	50 Hz
Core	laminated iron
Winding	foil

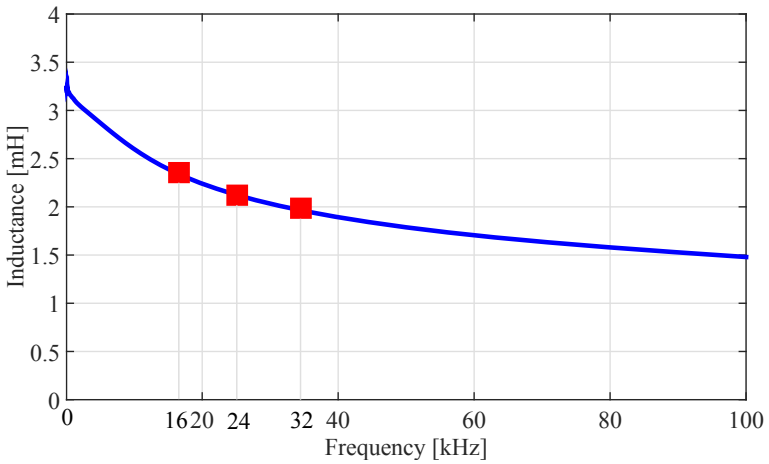


Figure 4.10: Small signal analysis of the inductance characteristic.

Table 4.4: Minimum and test inductance values at different switching frequencies

$f_s(kHz)$	$L_{min}(mH)$	$L_{test}(mH)$
16	2.3	2.4
24	1.5	2.1
32	1.1	1.9

4.1.3. Power analyser

In this work, the Yokogawa WT3000E precision power analyser as shown in Fig. 4.11 was used to extract power losses in the system. It is used to perform power measurements based on voltage, current and power factor data at the input and the output of the converter, and thus performs overall efficiency measurements. The WT3000E power analyser has four measuring elements which enable the measurement of efficiency of the DC-input three-phase inverter with one unit, and therefore highly accurate efficiency measurements can be attained. In addition, it can display 104 data and waveforms of input and output signals which can be combined by the user settings. The WT3000E is a digital power analyser, it takes the instantaneous values in the measured section, then it samples the instantaneous values of the measured waveforms and provides arithmetic multiplication and averaging to obtain the power measurements. The power analyser accuracy is given as a sum of the reading uncertainty and the measurement range uncertainty. The WT3000E precision power analyser has $\pm$(2% of reading + 0.4% of measurement range) power accuracy in the case of the fundamental frequency less than 400 Hz and switching frequency in the range of (10 kHz $<$ f $\leq$ 55 kHz) [63, 64].



Figure 4.11: Picture of the Yokogawa WT3000E precision power analyzer. [63]

4.1.4. Control platform

The control platform that has been used in this work to generate the modulation scheme is based on the Texas Instrument TMS320C6713 digital signal processor (DSP) along with the Microsemi ProAsic3 A3P400 field programmable gate array (FPGA) as shown in Fig. 4.12. This control platform has been designed and developed within the Power Electronics, Machines and Control Group (PEMC)at the University of Nottingham.

The DSP board is clocked at 225 MHz to perform floating point calculations for the modulation and control algorithms, while all the time-constrained functions - i.e. PWM generation and analogue to digital conversion (ADC) - are performed by FPGA which is operating at 50 MHz clock signal. The output of the modulation and control algorithm performed by DSP is stored in memory registers to be accessed by FPGA. The functions of the FPGA are to pick-up the duty cycles from DSP, generate the PWM signals and deliver them to the gate drivers. The host PC is used to program the DSP and to set different parameters such as switching frequency, dead time, measurement and control gains. The HPI daughter board designed by Educational DSP can provide a real-time interface between DSP and the host PC via a graphics user interface (GUI) in MATLAB. Moreover, the HPI allows the host PC to have an access to the internal memory locations without interfering the DSP operation.

Fig. 4.13 shows the simple structure of the control platform: in each switching cycle a set of pre-defined parameters, for example, switching frequency, dead-time and the modulation index are processed in the DSP, after which the DSP stores the demanded switching times in a first-in-first-out (FIFO) memory to be used in the next switching cycles. At the start of each switching cycle, the FPGA accesses the stored switching times to perform the required gate pulses for switch gate driver.

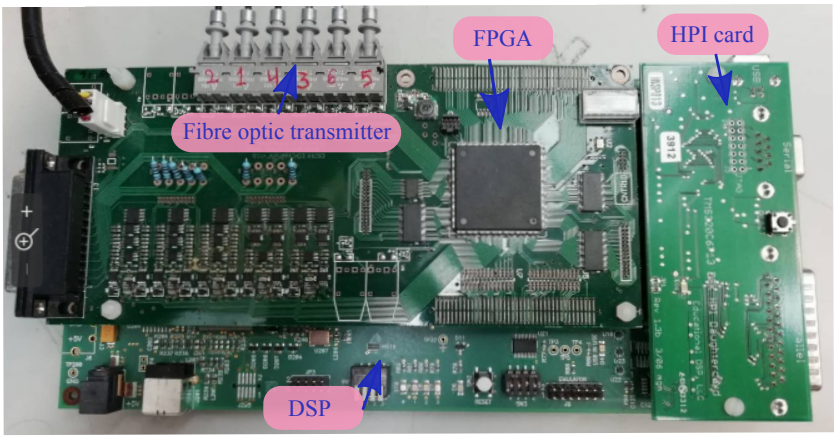


Figure 4.12: Picture of control platform utilising FPGA board and HPI daughte-rcard mounted on the DSP board.

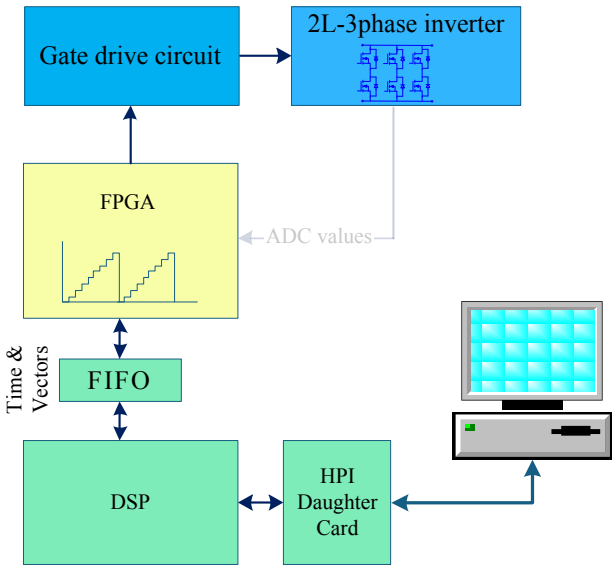
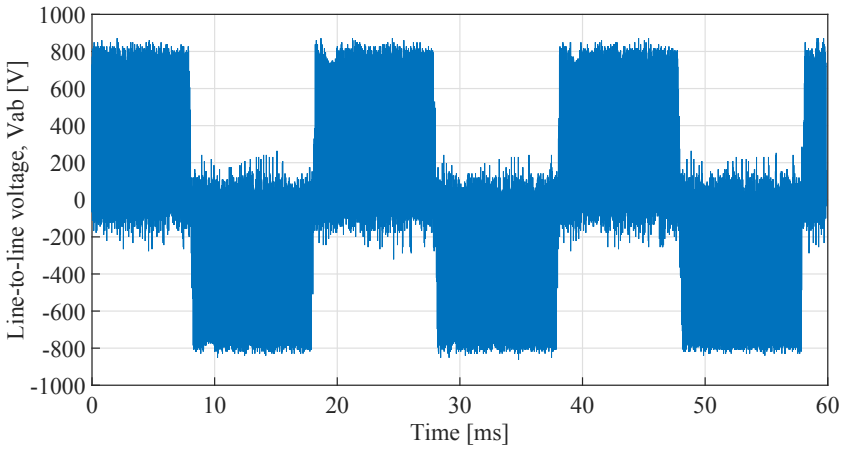


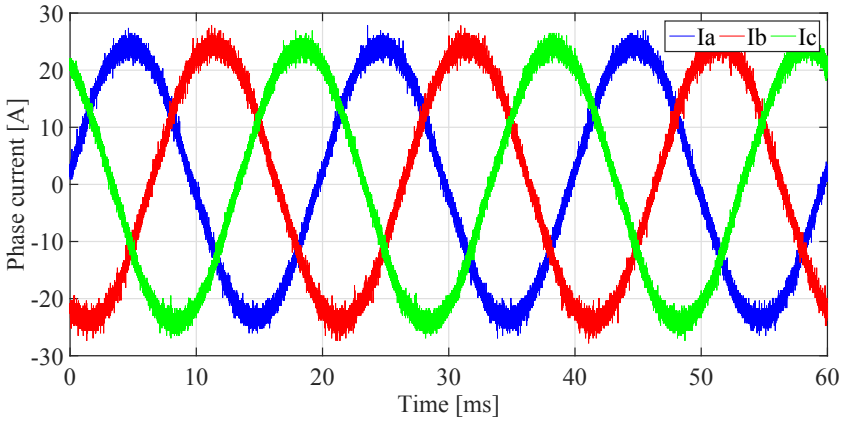
Figure 4.13: Control platform simple block diagram.

4.2. Experimental results and loss analysis

The experimental waveforms of the inverter line-to-line voltage and load currents at full output power and 32 kHz switching frequency are presented in Fig. 4.14. The load current THD estimation includes up to the 50000^{th} harmonic order with a total value less than 5% and complies with grid power quality requirements for different switching frequencies, as Fig. 4.15 shows.



(a) Line-to-line voltage



(b) Line currents

Figure 4.14: Measured waveforms of 2-level VSI.(a) Phase to mid DC-link voltage (b) Line-to-line voltage, and (b) Line currents, at 32kHz.

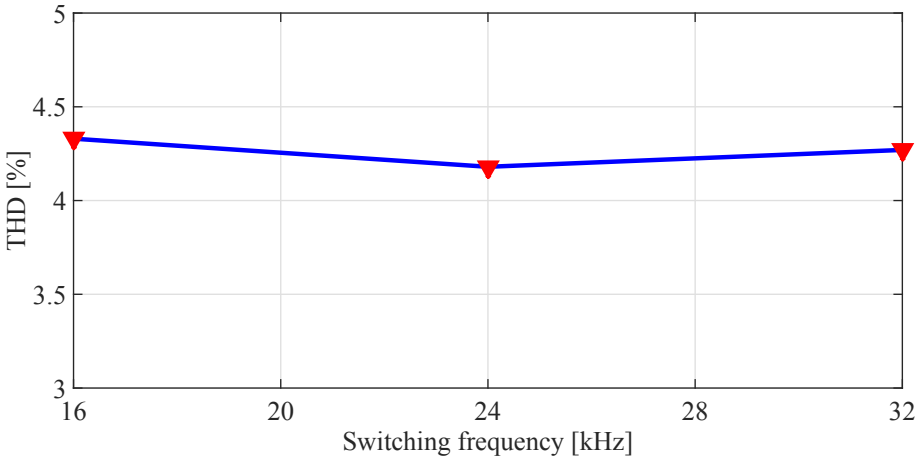


Figure 4.15: Total harmonic distortion (THD) versus switching frequency at full loading.

4.2.1. Efficiency performance and energy production

The power cell measured efficiency against the output power at different switching frequencies and at 60 ^{o}C heat-sink temperature is shown in Fig. 4.16. At higher output powers, the performance difference between different switching frequencies is insignificant, it is clear by increasing the switching frequency by a factor 2 implies a reduction in efficiency of less than 0.35% when working at 11.5 kW output power and 60 ^{o}C heat-sink temperature (less than 40 W difference in total power dissipation with about ± 1 W measurement error). This interesting feature enables a significant reduction of filter elements by increasing the switching frequency.

At light loads (the region of interest), in which the wind turbines spend most of their operational time; however the efficiency is reduced gradually by increasing the switching frequency. The reason for the efficiency reduction is due to the domination of switching losses instead of conduction losses at light loads. At 400 W output power which represents the starting wind turbine power, about 5% efficiency drop in the performance curve is observed when moving from 16kHz to 32kHz switching frequency.

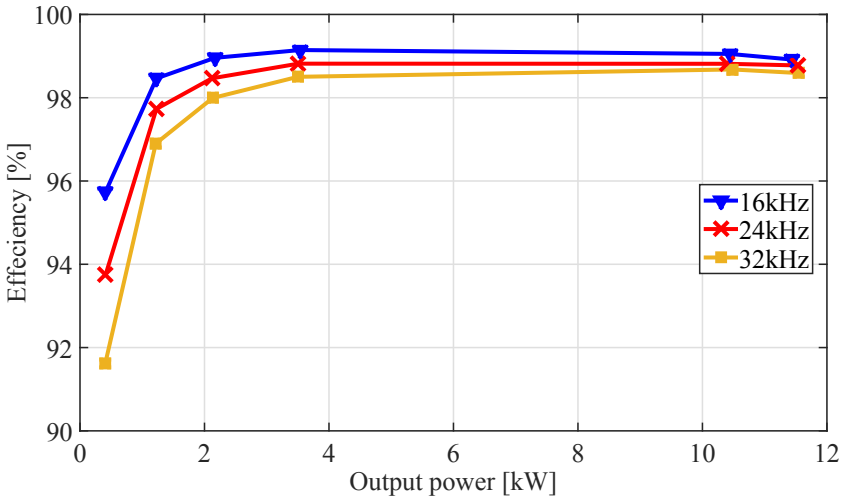


Figure 4.16: Efficiency vs. output power at T_h=60^{o}C.

Fig. 4.17 presents the annual lost energy calculated based on the measured power losses at different power loading and the hourly wind speed distribution throughout the year in Nottingham. It is clear that lost energy difference at high wind speeds which has a chance of small fraction of wind turbine operational time is almost negligible. The significant reduction of efficiency at lighter loads in the region of highly probable wind speed distribution, on the other hand, leads to a significant difference in the lost energy throughout the whole year. By considering the operation of the wind turbine in the wind speed range from 3m/s to 7m/s which has a highly probable working chance, this subsequently leads to about 53% difference in the lost energy by increasing the switching frequency from 16 kHz to 32 kHz.

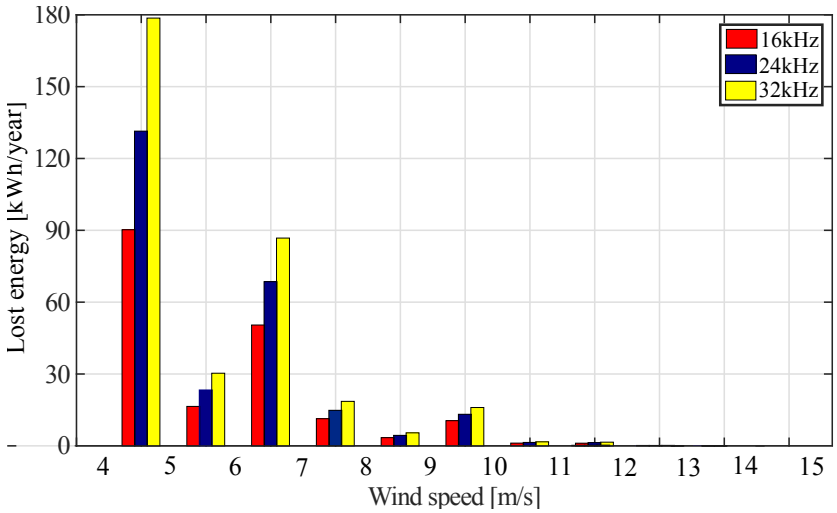


Figure 4.17: Annual lost energy vs. wind speeds at different switching frequencies.

4.2.2. Temperature stability

Fig. 4.18 presents the temperature dependency of wind inverter efficiency at full power loading for a given 32 kHz switching frequency. It is seen from the results that the performance of the inverter has a negligible dependency on heat-sink temperature within a representative range of heat-sink temperature; the efficiency drop was 0.19% (less than 22W) over a whole range of heat-sink temperatures (from 50 ^{o}C to 90 ^{o}). The increase of heat-sink temperature without compromising the efficiency allows the design of the cooling system for nominal operational conditions, typically corresponding to lower than maximum power rating in the region of high probable wind speed distribution, which will result in a significant decrease in heat-sink volume.

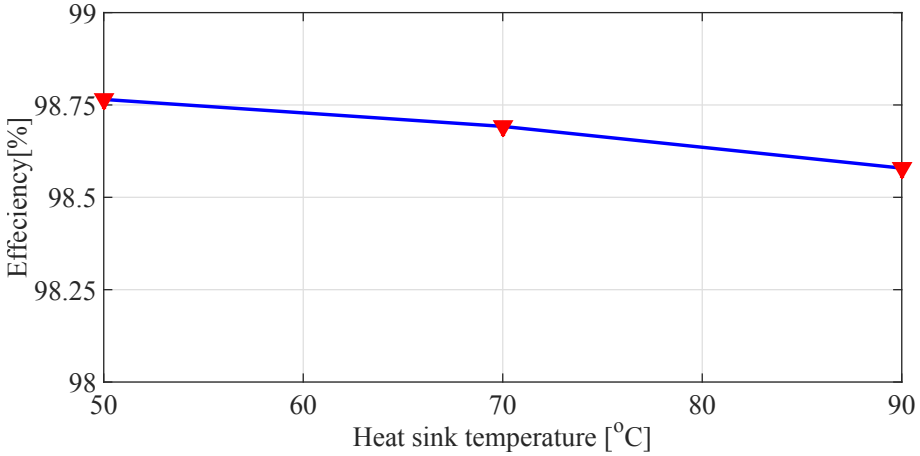


Figure 4.18: Efficiency vs. different heat sink temperature at full loading and 32 kHz switching frequency.

4.2.3. Power losses breakdown

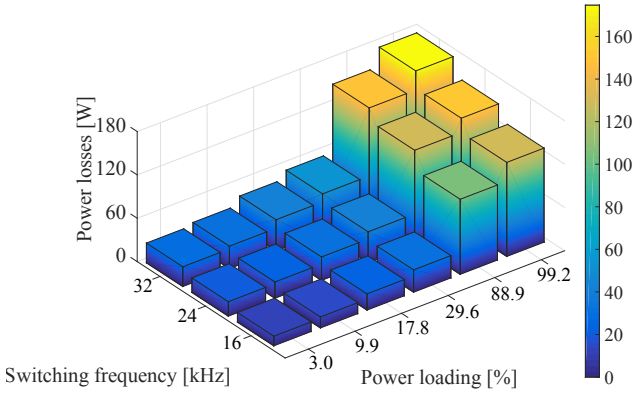
To evaluate the dominant loss component at a different switching frequency and under different loading, a breakdown of overall power cell loss in terms of conduction and switching loss was performed. Particularly, this evaluation can help to understand the behaviour of the losses at different operational conditions of wind turbines, and thus enables the optimisation of wind inverter design for maximum exploitation of the potential benefits of SiC technology in wind energy applications. In order to separate the conduction and switching losses for each operating point, the switching energies are measured directly by double pulse test (DPT) prototype presented in chapter 3, and the total switching losses are calculated by assuming identical devices within the three-phase module. Then the total conduction loss was obtained by subtracting the total switching loss from the measured total power cell loss.

Fig. 4.19-a, Fig. 4.19-b and Fig. 4.19-c show, respectively, the converter total loss, conduction loss and switching loss as a function of switching frequency and power loading at a reference heat sink temperature of 60^oC. Fig. 4.19-a shows that the increased power loading becomes the dominant factor in the total losses. According to Fig. 4.19-b with respect to three different switching frequencies, i.e. 16 kHz, 24 kHz and 32 kHz, the conduction loss is the main contributor to the total power cell loss due to the increase of on-state voltage drop of SiC MOSFET at higher currents. Meanwhile, the conduction loss is seen to be increased with respect to the switching frequency increase due to the increase in dead time losses in a switching period by increasing the switching frequency. However, at light loads where the wind turbines spend most of their operational time, the total losses are dominated by the switching frequency as shown in Fig. 4.19-c. The switching losses increase as the switching frequency increases from 16 kHz to 32 kHz resulting in a high lost energy per year at low wind turbine power. One can consider the reduction of switching losses by varying the switching frequency at the region of interest of highly probable wind speed distribution.

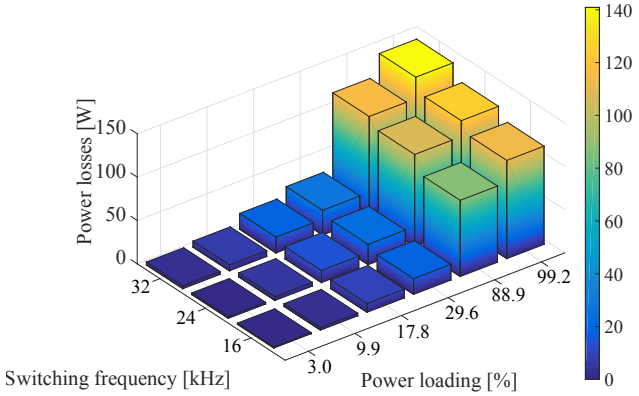
4.3. Converter power losses model validation

In this section, both calculations and experimental tests are provided to validate the power loss model. The experimental results of the SiC-based prototype (i.e., 2L-VSI) at different power loading are presented to deliver proof-of-concept demonstration of the power loss analytical model.

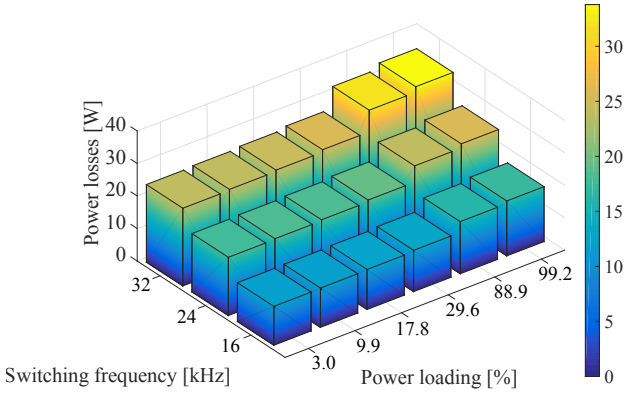
For calculation of conduction losses, it is enough to use the manufacturer information in the datasheet, which provide detailed performance data for the MOSFET $R_{S,on}$, and the Schottky diode $R_{D,on}$ and $V_{D,on}$ [1,45]. However, it is difficult to determine the devices switching losses from datasheets information, particularly when the test conditions are different from those available in the datasheets. Typically, to further improve model accuracy, the switching loss should be obtained for particular operating conditions such as gate drive resistances, gate drive



(a) Total losses



(b) Conduction losses



(c) Switching losses

Figure 4.19: Loss breakdown for SiC MOSFET based 2-L 3-phase inverter at 60^oC heat sink temperature: (a) total power device loss, (b) conduction loss, (c) switching loss.

voltage level, junction temperature, the type of freewheeling diode and the DC-link and PCB configuration. In this work, in order to have an adequate accuracy, the switching characteristics and hence the device switching losses are measured using a laboratory prototype for DPT with the same switching conditions for inverter, i.e. +20 V for turn-on and -5 V for turn-of, gate resistors of 10Ω for turn-on and 5Ω for turn-on, Schottky diode is used for freewheeling, the same heat sink temperature, and the exact power plan configuration.

The switching energy loss of the SiC MOSFET in (mJ) as a function of the output current can be expressed by a second-order polynomial function:

$$E(i) = b_2 i^2 + b_1 i + b_0 \tag{4.5}$$

where, b_2, b_1 and b_0 are constants derived from the curve fitting of DPT switching characterization.

Table 4.5: Switching losses parameters

Parameter	Value
b_2	0.0002
b_1	0.0022
b_0	0.2374

Fig. 4.20 presents a comparison between the analysed power cell efficiency of SiC 3-phase VSI, and the efficiency measured throughout the experiment. To understand if the error in the efficiency curves comes from switching losses or conduction losses, the analysed and measured total losses were separated into switching and conduction losses. The device switching losses from double pulse test (DPT) with the same switching conditions for inverter operation were used to estimate the power losses in the analytical model and to breakdown the measured total losses. As shown in Fig. 4.21, the calculated conduction losses over the output power is slightly different from the measured one. The losses of the DC-link and the copper losses of the PCB tracks were included in the experimental measurements and this is probably the source of the major difference. In addition, the theoretical analysis was made with some assumptions, i.e. zero dead time and zero leakage current.

Fig. 4.22 presents a comparison between the analysed and measured efficiencies over a wide range of heat sink temperature; the analytical model results are in a good agreement with measurements whereas the efficiency over the whole temperature range is dropped by 0.19% in analysis and 0.14% in measurement.

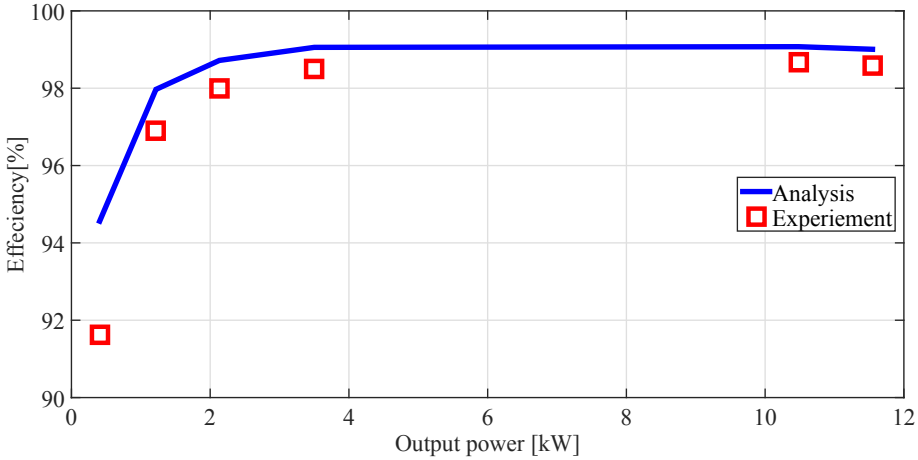
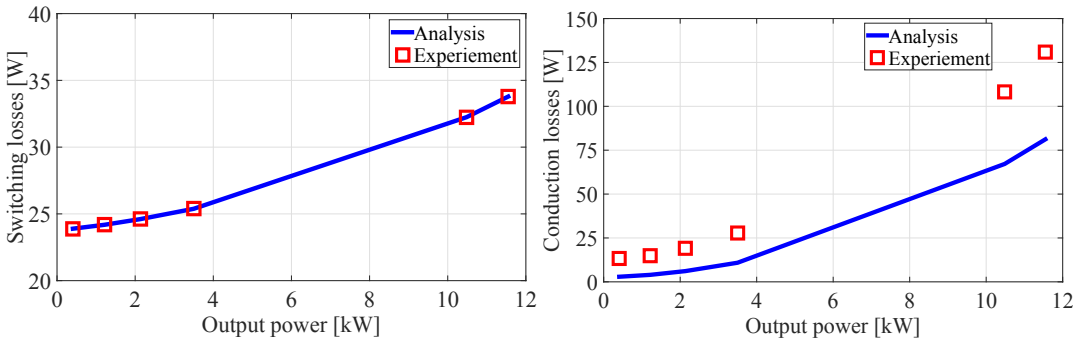


Figure 4.20: Comparison between simulated and experimental efficiency for 2L-VSI with SiC MOSFETs working at 32kHz and different loading, at heat-sink temperature of 60^oC.



(a) Switching losses (b) Conduction losses

Figure 4.21: Converter power losses versus power loading at switching frequency of 32kHz and heat-sink temperature of 60^oC with simulation and experimental results: (a) Switching losses (b) Conduction losses.

4.4. Non-unity power factor inverter operation

For grid-connected wind turbines, the inverter must comply with the power grid requirements; this means it should have the ability to handle active and reactive power to support the grid, for example, it contributes to voltage recovery, when the grid voltage sags [65]. Since the tested inverter can only operate in an open loop, it cannot supply reactive power to the grid. To create a current with a phase shift, a set of inductors were added to the resistive load. The peak current and grid voltage were kept at the same value at different power factors to ensure valid comparison.

In this experiment, the inverter power cell efficiency which is of interest for a comparison between different power factor values was measured using the power analyser. The DC-link voltage of 720 V and the modulation index were set to generate the sinusoidal output voltage of 230V. The switching frequency was 32 kHz and the apparent power was 10.5 kVA. The

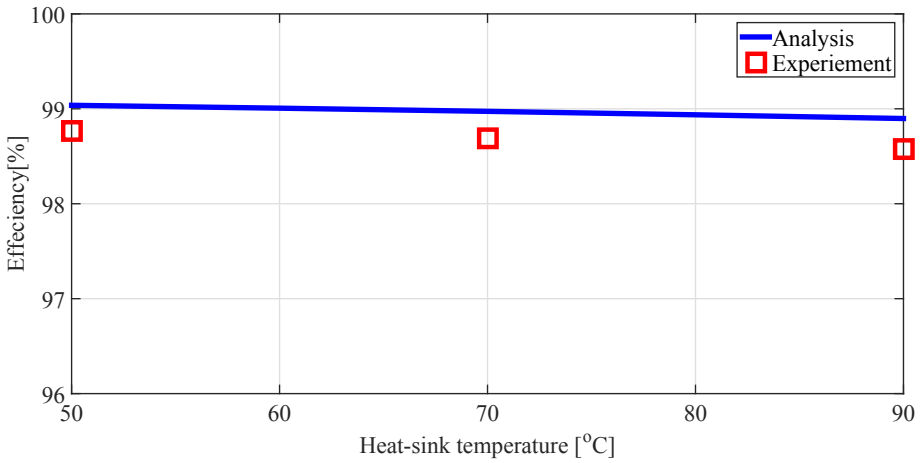


Figure 4.22: Comparison between simulated and experimental efficiency for 2L-VSI with SiC MOSFETs working at 32kHz and different heat-sink temperature, at full loading.

efficiency at different power factors (i.e. 1 and 0.92) was measured, Table 4.6 shows the measured efficiency for the given SiC wind inverter at S=10.5 kVA. It can be seen that there is no significant drop in efficiency in case of reactive power generation at 0.92 power factor, the efficiency drop was 0.055% (less than 6 W). In a full SiC system, the reason for the power loss increase is only due to the increase of conduction losses through the Schottky diodes with decreasing power factor. However, the Si configuration dominates the switching losses when the power factor decreases which leads to higher power losses than SiC counterpart. Therefore, the capability of the reactive power handling to the grid is overall guaranteed by using SiC wind inverter with very small dependency on the power factor.

Table 4.6: Measured efficiency as a function of power factor at S = 10.5 kVA

UPF	non-UPF (0.92)
98.679%	98.624%

4.5. Conclusion

In this chapter, the evaluation of SiC devices in a 2L 3-phase wind inverter was presented in terms of power losses and efficiency under different conditions, i.e. various power loading, different switching frequencies and different heat-sink temperatures. The results show that SiC MOSFET devices can be used to design wind inverters with high efficiency and high power density. Moreover, SiC devices exhibit good thermal behaviour over a wide range of heat-sink temperatures; this enables the design of the wind inverter cooling system to increase the power density for natural convection cooling without compromising the efficiency. In addition to this, the wind inverter loss breakdown shows that the switching losses dominate the total

power cell losses at light loads; this leads to maximize the low-load efficiency by varying the switching frequency as a function of the wind speed distribution. The capability of the reactive power handling to the grid is overall guaranteed by using SiC wind inverter with very small dependency on the power factor.

Chapter 5

Inverter Optimized Design

In this chapter, a bespoke design has been presented to inverter performance and power density by joint electro-thermal and electro-magnetic design optimization of a 2L 3-phase voltage source inverter, referring to the salient features of SiC MOSFET and some specific operating conditions of wind turbines. The inverter power cell efficiency is not significantly dependent on heat-sink temperature indicating the possibility to reduce the heat-sink size without the penalty of decreased system efficiency. With the aim of maximizing the power density of the inverter, the overall volume was reduced by increasing the heat-sink temperature and choosing the optimum switching frequency for the minimum inverter volume. To enable optimum efficiency versus power density trade-off, the inverter was redesigned with variable switching frequency as the load changes.

5.1. Bespoke design of wind inverter cooling system

5.1.1. Heat-sink design

The heat-sink thermal resistance can be calculated by the maximum power to be dissipated at a specific heat-sink temperature as follow [66]:

$$R_{th,hs} = \frac{(T_{hs} - T_a)}{P_{semi,tot}} \tag{5.1}$$

T_{hs} is the reference heat-sink temperature (equal to 60^oC for some industrial applications, i.e. PV inverters), T_a is the ambient temperature (chosen as 25^oC), and $P_{semi,tot}$ is the total semiconductor losses.

The thermal circuit for devices in 2L 3-phase prototype converter is shown in Fig. 5.1, the losses of each semiconductor device is dissipated via the device internal thermal resistance $R_{th,jc}$. The total semiconductor power losses are transferred to the ambient via the series

connection of thermal resistance of the thermal paste applied between the power module and heat-sink $R_{th,ch}$, and heat-sink thermal resistance $R_{th,hs}$ [15].

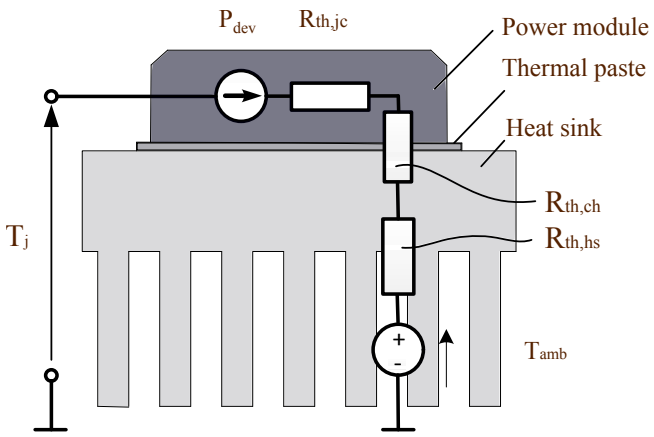


Figure 5.1: Thermal network of power semiconductor devices.

In order to have heat transfer to the environment, natural and forced convection air cooled are commonly used. For stationary installations (i.e. wind turbines, PV systems and EV charging stations) and for high efficient power electronics systems that require a relatively higher thermal resistance (i.e. converters utilizing SiC power semiconductors), the natural convection is much more attractive than forced air convection in terms of efficiency and volume since no fan is needed [67].

This work focuses on natural heat-sinks, whereas first the heat-sink thermal resistance ($R_{th,hs}$) is calculated, then can be used to calculate the heat-sink volume. The dependency of heat-sink thermal resistance based on natural cooling on volume and temperature difference between the heat-sink and ambient temperature ($\Delta T = T_{hs} - T_{amb}$) is shown in Fig. 5.2. The heat-sink thermal resistance as a function of volume is derived by curve fitting of $R_{th,hs}$ at a given volume (gray dots) for commercially available heat-sinks (i.e. Aavid Thermalloy) as shown in Fig. 5.2-a and presented in (5.2) in which the ambient and the heat-sink temperatures of $T_{amb} = 25^oC$ and $T_{hs} = 60^oC$ are considered. Dependency of the heat-sink thermal resistance ($R_{th,hs}$) on temperature difference (ΔT) is shown in Fig. 5.2-b and is achieved by multiplying the heat-sinks nominal thermal resistance ($R_{th,hs,n}$) which is defined at 75^oC temperature difference by the adjustable factor (AF) as presented in (5.3) and (5.4) [68].

$$R_{th,hs} = 0.7232 \times V_{hs}^{-0.7784} \tag{5.2}$$

$$R_{th,hs} = AF \times R_{th,hs,n} \tag{5.3}$$

$$AF = 1.243 \times 10^{-4}\Delta T^2 - 2.143 \times 10^{-2}\Delta T + 1.910 \tag{5.4}$$

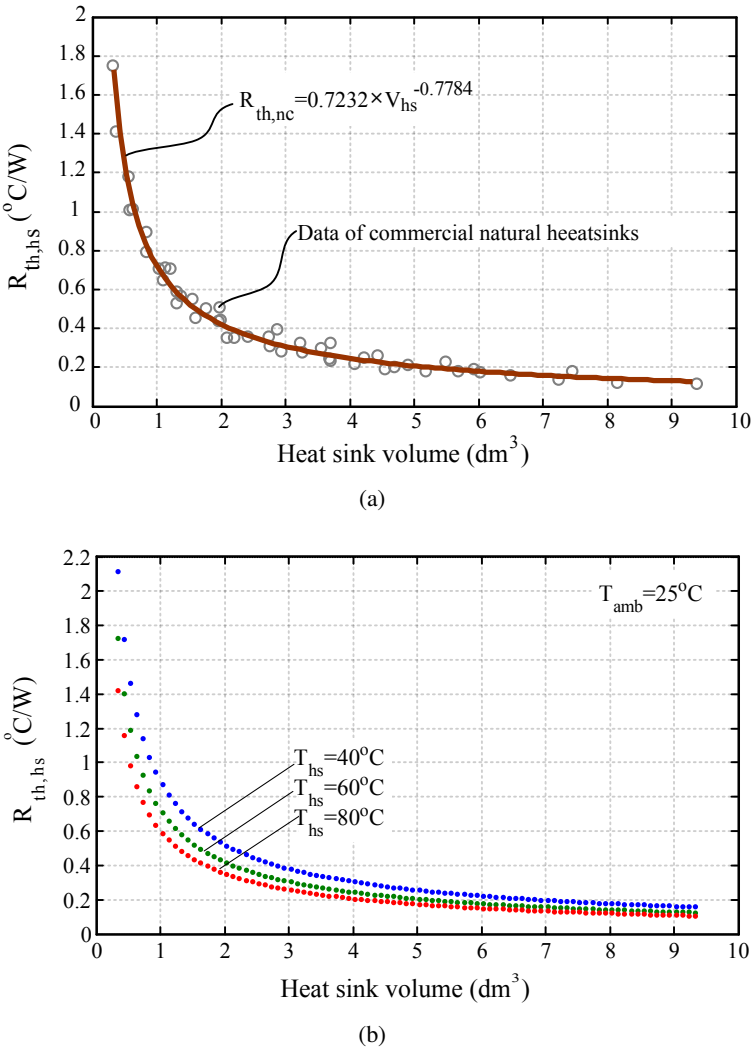


Figure 5.2: Dependency of natural convection cooled heat-sinks on (a) the volume and (b) the temperature difference.

5.1.2. Basic idea

This section deals with the thermal management design of 12 kW three-phase inverter for a small-scale wind turbine, taking into account some specific behavioural features of SiC power MOSFETs. Power converters used in renewable energy conversion have to deal with intermittent and variable power availability from the source, which implies that they actually work at their maximum rated power for only a small fraction of their operational time. Still, traditional thermal management design of power modules has to refer to maximum load conditions. SiC-MOSFETs exhibit a very stable performance over a broad temperature range; this feature

enables the design the cooling devices for nominal operational conditions, typically corresponding to a much lower than maximum power rating. When this capability is added to the decrease in the size of passive filter elements, which can be gained by the higher switching frequency capability of SiC MOSFETs, the result is a significant increase in the converter power density.

The basic idea is illustrated on the basis of Fig. 5.3. Still, the traditional heat-sink design has to refer the maximum rated power, i.e 12 kW in this work, the heat sink was designed to give a steady-state temperature of 60 ^oC (a reference value for some industrial applications, i.e. PV and wind turbines). Alternatively, designing for a maximum full load temperature of 90^oC corresponds to 60 ^oC heat-sink temperature at 8.5 kW in the region of interest, which although not the most probable working condition, is however, a more highly probable working condition. If the peak of wind speed histogram shown in Fig. 5.3 increases randomly or it shifts slightly towards a higher power region, this change does not affect the design point and the operating temperature range. However, in this case, the design point offers a wider margin against variations in wind speed distribution.

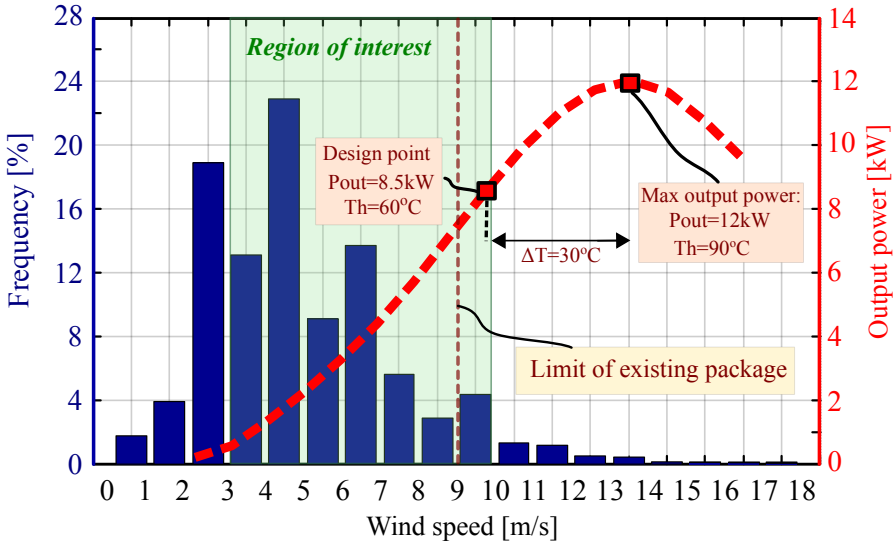


Figure 5.3: The wind speed distribution (blue data) and wind output power (red data) versus wind speed.

To achieve lower output power for heat-sink design corresponding to higher wind speed distribution, the junction temperature must be increased accordingly in case of a given heat-sink. The heat-sink temperature also rises over the temperature which significantly improves the convective heat transfer and allows smaller heat sink volume. However, the fact that the heat-sink volume decreases with the increase of the heat-sink temperature is true in a limited range of heat-sink temperatures. Fig. 5.4 shows a very important result: the maximum value up to which it makes sense to increase the heat-sink temperature is limited at about 250-255^oC; beyond this value, the increase in semiconductor losses becomes a limiting factor and no further

heat-sink volume shrinkage is viable.

SiC devices offer the capability for higher temperature operation over their Si counterparts, which has been demonstrated at temperatures up to 600^oC. However, the limiting factor for these devices to operate at higher temperatures, more than 200^oC, is the limitations imposed by currently available packages. The maximum temperature of 250^oC and beyond which corresponds to the minimum heat-sink volume is not so far from the temperature limit of the present packages, which typically have the maximum temperature of 150^oC-200^oC. Innovative packaging designs and materials are required, especially around the temperature of 250^oC, to satisfy more efficient and high power density power converters (i.e. 2L-VSI topology at 12 kW power level).

In this work, the reference temperature for the heat-sink design was increased from 60 ^oC to 90 ^oC; this decreased the heat-sink size and weight significantly. However, higher heat-sink temperatures greater than 125 ^oC may lead to exceeding the recommended maximum junction temperature which is between 150 ^oC and 175 ^oC for SiC devices with conventional packaging.

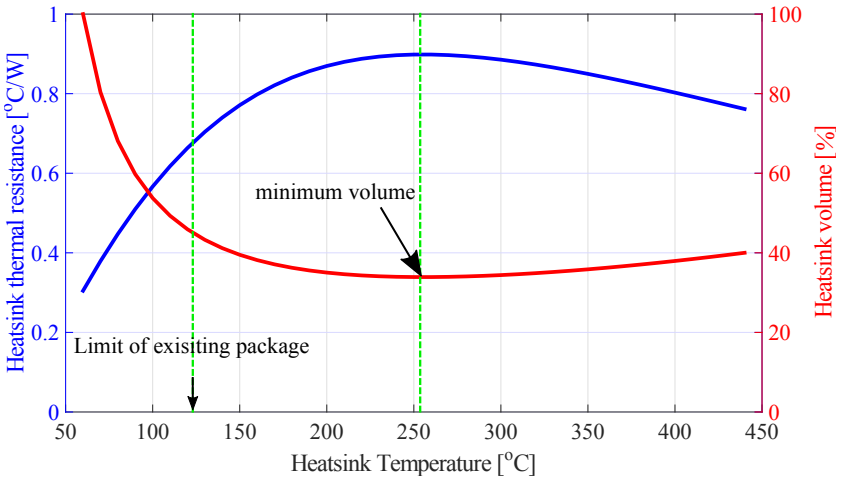


Figure 5.4: Analytical estimate of passive heat-sink volume reduction with increasing temperature.

To deliver a proof-of-concept demonstration of heat-sink reduction model with respect to the increase of heat-sink temperature, air forced convection heat sink was used where the-heat sink thermal resistance at different heat-sink temperatures was determined by varying the applied bias voltage (i.e. the rotation speed) of the cooling fan.

To simplify the concept validation, a set of power resistors with a total value of 3.3 Ω were mounted on the heat-sink with a cooling fan; total power cell losses of 170 W which is the measured power losses at full power loading was supplied to the power resistors from external power supply without the need of inverter operation. The power resistors dissipate the power cell losses and generate a heat in the assembly causing a heat-sink temperature rise, while the cooling fan is to control the heat-sink temperature.

Fig. 5.5-a shows the characteristics of the measured heat-sink temperature, T_h, to the fan

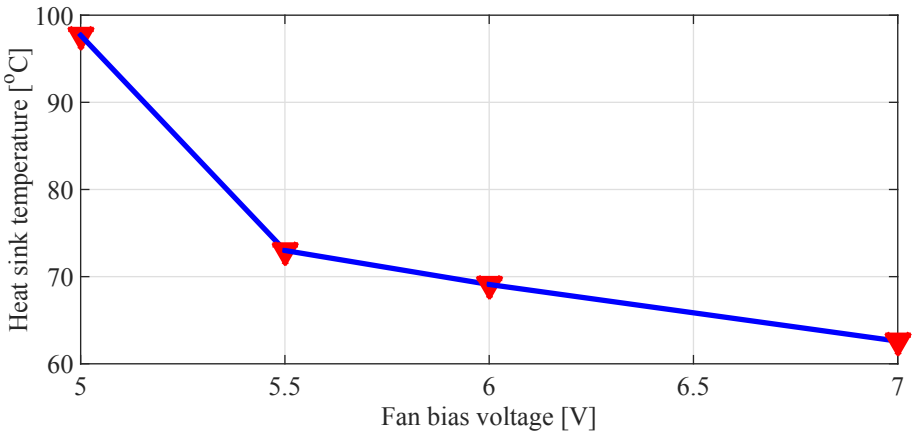
bias voltage, V_{bias}. This relation is transformed to the heat-sink thermal resistance, $R_{th,hs}$, as a function of fan voltage bias as shown in Fig. 5.5-b by using (5.1), where $Ta = 25^oC$ and $P_{semi,total}$=170 W. After that, the passive heat-sink volume is determined based on a curve fitted derived equation for commercially available heat-sinks, i.e. Aavid Thermalloy. Fig. 5.6 shows the estimated heat-sink volume as a function of heat-sink temperature; the heat-sink volume from the measurement is characterized by some degree of deviation from simulation values, especially at low heat-sink temperatures. However, it should be noted that the heat-sink volume from measurement and analysis show the same trend over the whole test range. In addition, it is clear that the mismatch is always reduced with the increase of heat-sink temperature in the same direction as analysis. The error between analysis and measurement is due to the deviation of the estimated power loss between the theoretical analysis and the measured one. This is probably due to including the losses of the DC-link and the copper losses of the PCB tracks in the experimental measurements, and the theoretical analysis was made with some assumptions, i.e. zero dead time and zero leakage current.

5.2. Design of inductor-filter

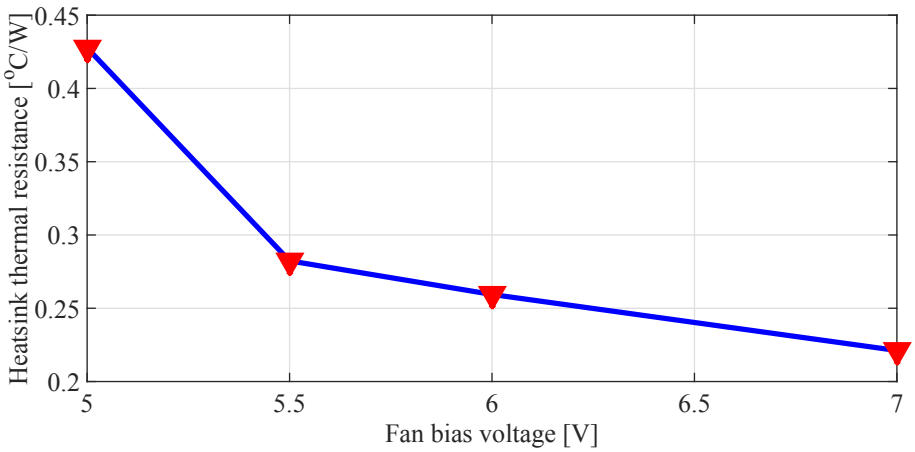
The output filter for the grid-connected inverter is to attenuate high-frequency harmonics injected into the grid. Typically the choice of the output filter in this work is LC filter, because this configuration is simple to design, stable, and the possibility of using a relatively high switching frequency and low dead-times for WBG-devices can lead to achieving reduced levels of harmonic distortions in compliance with grid quality requirements.

5.2.1. Cores magnetic material selection

The purpose of the magnetic material core is to generate higher magnetic flux than that produced by the air core for a given applied electric field and to create a path for the magnetic flux. The important properties of the core material are the relative permeability, μ_r, maximum flux density,B_{max}, coercivity, H_c, and resistivity, ρ. With high relative permeability, the material's capability to conduct the magnetic flux will increase. The maximum flux density determines the core size; high maximum flux density decreases the core cross section. Small coercivity reduces hysteresis losses while a high resistivity reduces eddy currents. The magnetic materials used in industry can be classified as hard magnetic materials and soft magnetic materials. Hard magnetic materials which have a wider hysteresis loop and higher coercive forces are commonly used in permanent magnets in motors and generators. Soft magnetic material, on the other hand, are used in high frequency transformers, filter inductors and EMI filters. Soft magnetic materials are classified into laminated iron alloy, ferrite material, powder iron alloy, amorphous alloy, and nanocrystalline material [69, 70].



(a) Heat sink temperature



(b) Heat-sink thermal resistance

Figure 5.5: The characteristics of heat-sink temperature and thermal resistance to bias voltage of the fan: (a) Heat sink temperature, (b) Thermal resistance.

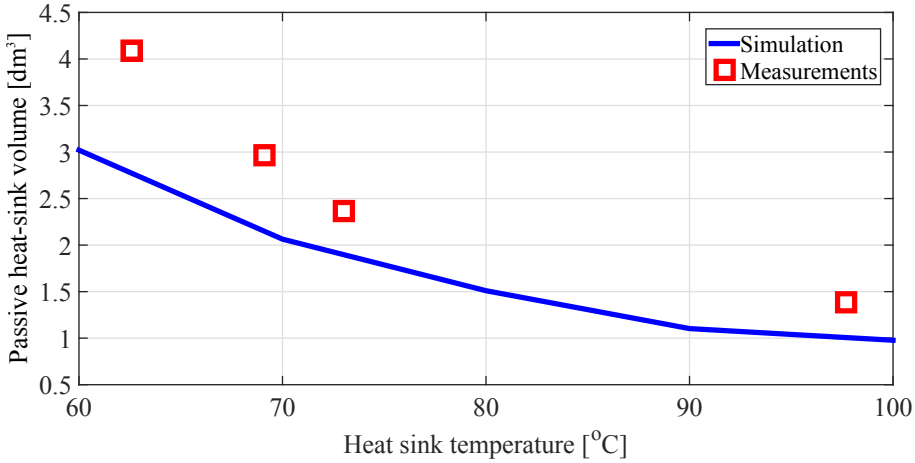


Figure 5.6: Heat sink volume versus heat-sink temperature at 32kHz with analysis and experimental results.

The choice of magnetic material to ensure low losses, minimum size and low cost is the most necessary step for the inductor design. In laminated iron alloy, a small amount of silicon (typically 3%) often is added to iron to increase the core electrical resistivity which gives a significant reduction in eddy current losses. The iron alloy is characterized by high flux density (up to 2.0 T) and high permeability (up to 40 000). Addition to thin laminations of silicon-iron cores but still have high eddy currents due to their low core resistivity and high coercive forces. Therefore, these cores are only suitable for low frequency applications in the range of few kHz [69, 71].

Ferrite is a ceramic material; they mainly contain iron oxide (Fe_2O_3) mixed with other materials such as manganese (Mn), nickel (Ni) and zinc (Zn). The most commonly used types of this material are Ni-Zn and Mn-Zn. Ni-Zn ferrite can achieve low losses at high switching frequencies,$>$1MHz, due to their higher resistivity (up to 10 000 mΩm). Mn-Zn ferrite type, on the other hand, can provide higher permeability and maximum flux density with the penalty of lower electrical resistivity (about 1mΩm), makes the ferrite suitable for applications with frequencies lower than 1MHz [69, 71].

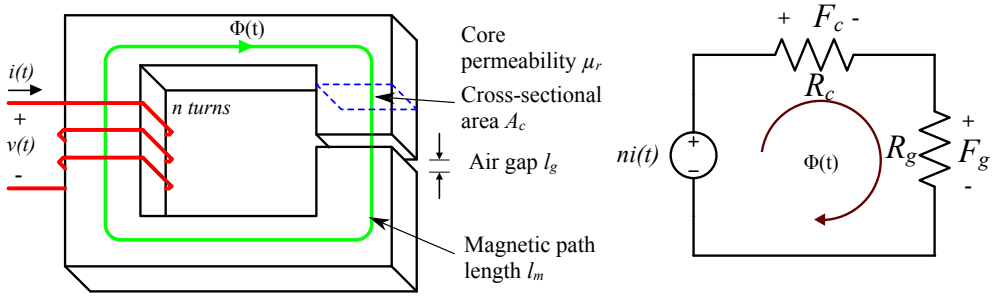
Iron powder cores are metal particles, about 100μm, bonded in epoxy and pressed into a bulk material at high pressure. The epoxy bonding material acts as a small distributed air gaps between the particles along the core instead of the large air gap in the magnetic circuit. The distributed air gaps between each particle have fewer issues, i.e. fringing, EMI and mechanical assembly problems. The insulating bonding of each particle provides a small eddy current paths throughout the particles and higher electrical resistivity of the bulk core. Typical magnetic powder material offers cores with a relative permeability in the range from 15 to 550, electrical resistivity around 1mΩm and saturation flux density between 1-1.5T. The resulting inductance of iron powder cores is very stable over a wide range of temperatures and switching frequencies [69, 70].

The tap-wound amorphous/nanocrystalline materials are an alternative to the laminated steel with typically tape thicknesses (less than 0.003mm). The amorphous alloy contains iron-based non-crystalline, and it is often called metallic glass because of its glass-similar structure. Amorphous cores provide shorter eddy current paths due to the lamination of tape-wound cores (the thin ribbon), high core resistivity, typically can reach 1.6 $\mu\Omega$m, which is three times higher than that of silicon steel and low coercive forces resulting in lower core losses. This material can offer cores with relative permeability up to 100 000 and maximum flux density around 1.6T, which is four times higher than that of ferrites. However, amorphous alloy shows a significant drop in the saturation flux density with temperature [69, 72, 73].

The nanocrystalline alloy is established in iron-based ultra-fine crystals below 20nm in size. This material combines the advantages of high saturation flux of laminated iron steel cores with an improved high frequency of ferrite cores. The relative permeability of nanocrystalline reaches 20 000 and its maximum flux density is about 1.5T. This material is characterized

by reduced eddy currents losses because the core is supplied with a thin ribbon of 15-25μm thickness and electrical resistivity of about 0.012$\mu\Omega$m. The nanocrystalline material has a very good temperature stability over a wide range of temperature operation with thermal properties better than that of amorphous material [69, 72, 73].

The discrete air gap is mandatory for magnetic cores, utilising materials of laminated iron, ferrite, amorphous and nanocrystalline to avoid the core saturation. However, iron powder cores can provide distributed air gaps due to small gaps between particles instead of large air gap; this subsequently leads to lower fringing issues and thus lower core and winding losses. Fig. 5.7 shows a simple magnetic circuit model with inductive components enables the calculation of the inductance. The inductance with N winding turns, a magnetic core reluctance R_c and an air gap reluctance R_g is calculated as:



(a) Physical geometry (b) Magnetic circuit

Figure 5.7: Illustration of a simple magnetic core: (a) Physical geometry and (b) Magnetic circuit.

$$L = \frac{N^2}{R_c + R_g} \tag{5.5}$$

The calculation of the magnetic core and air gap reluctance is given by:

$$R_c = \frac{l_c}{\mu_r \mu_0 A_c} \tag{5.6}$$

$$R_g = \frac{l_g}{\mu_0 A_c} \tag{5.7}$$

Where lc and lg are the core and air gap length, respectively, Ac and Ag are the cross-section area of the magnetic core and air gap, respectively, μ_0 is the permeability of free space and μ_r is the relative permeability.

It is worth mentioning that the air gap reluctance R_g is dominant for the inductance value in applications using cores with laminated iron, ferrite, amorphous and nanocrystalline materials in which they provide low reluctance paths due to their higher relative permeability values, and thus exhibit fixed inductance value over the applied magnetic field range. However, the pow-

dered iron material can achieve the effective permeability without any large air gap; instead, very small gaps distributed over the core, so that the core inductance linearly reduces with the increase of magnetic field.

Fig. 5.8 shows the relative permeability of ferrite and powdered iron (Kool mu) cores. When using ferrite cores, the core shows constant permeability over the operating range and a sudden drop in permeability occurs when the iron saturates. The permeability of Kool mu cores, on the other hand, varies linearly with the increase of the magnetic field strength [74,75].

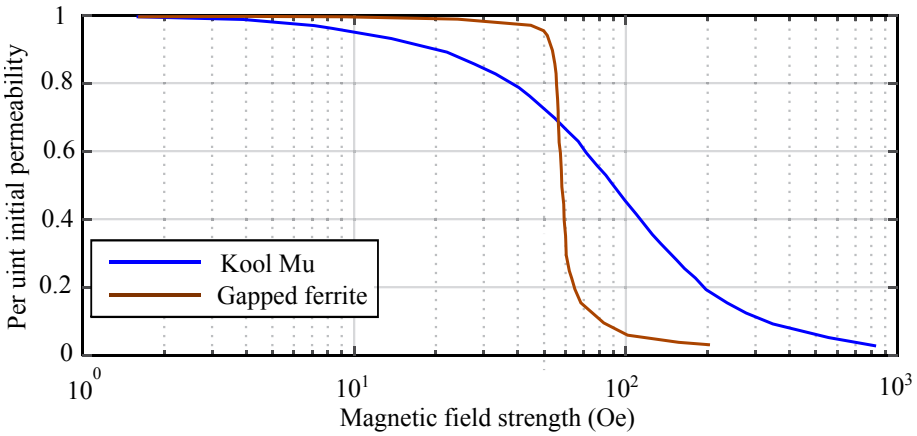


Figure 5.8: Permeability of ferrite and powdered iron (Kool Mu) cores as a function of magnetic field strength [74].

Fig. 5.9 shows the magnetic flux baths for powdered iron and ferrite E-cores. The design of powdered iron cores often provides low effective permeability without any large air gaps in the magnetic circuit. The distributed air gaps along the core result in lower air losses due to the absence of fringing flux around the air gap. However, when designing inductors with ferrite cores; the low effective permeability to avoid the iron saturation at high DC bias currents can be only attained by creating a large air gap in the magnetic circuit which results in high fringing flux, thereby increasing the core and copper losses due to the intersection of the fringing flux with the copper winding [75,76].

There have been many different materials for powder cores: Molybdenum permalloy (MPP); High flux; Kool Mu, etc. Molybdenum permalloy, MPP (2% Molybdenum, 81% Ni, 17% Fe) has the lowest power losses among powder materials at high saturation flux density. However, it is high cost material and has limited geometry to toroidal shape. High flux (50% Ni, 50% Fe) has the highest magnetic flux density (about 1.5 T), makes the material suitable for high power applications. High flux cores, on the other hand, has the only available toroidal core shape like the MPP cores. Kool Mu material (6% Al, 9% Si, 85% Fe): it saturates around 1 T and its permeability between 26-125 μ. Kool Mu material properties fit between the characteristics of MPP and High flux combining the power losses and maximum flux density. The advantage of

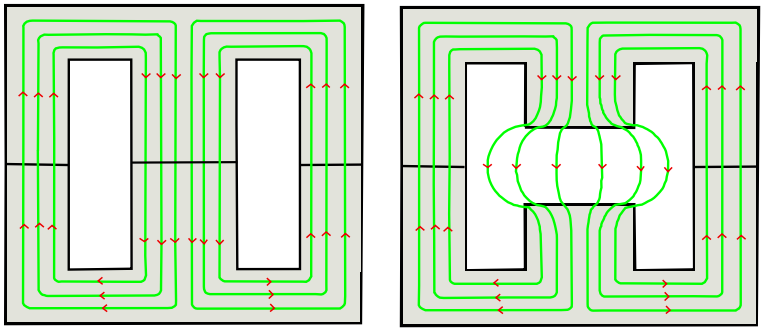


Figure 5.9: Magnetic flux through ferrite cores (right) and iron powder cores (left) [76].

Kool Mu is cheaper than MPP and high flux because it is a nickel-free alloy, and it is available in different shapes, i.e. toroid, C and E core shapes [70, 74, 75].

5.2.2. Inductor design using Kool Mu core

The filter inductance of 2-Level three-phase inverter is given by (4.4) [62]. The inductor must be designed to ensure the maximum output ripple current within 20% of the peak output current I in which the wind turbine feeds the maximum output current. The core size can be determined by computing the product LI^2, and then locating the value on the core selector table; the first core size located above the calculated value is the smallest core size that can be used in the design [77].

The design of Kool Mu inductor is different from other inductor designs, i.e. cores based on ferrite and amorphous; the core has no air gap; and the soft saturation property where the core inductance varies with the of DC bias current should be compensated. The permeance of the core AL reduces linearly with the increase in inductor current i_L as given by (5.8), where AL_0 is the permeance at zero ampere-turns, and M is the slop of the permeance variation as a function of amper-turns. Usually, the manufacturer provides the information of the permeance variation with the ampere-turns, i.e as shown in Fig. 5.10 for Kool Mu 60μ LE114 core. As a result, the inductance L decreases linearly by the increase of inductor current i_L and presented by (5.9), where L_0 is the inductance at zero current and K is the slop of the inductance reduction with the increase of the current through the inductor and related to M by the factor of N^3 [75].

$$AL(t) = AL_0 - M(Ni_L(t)) \tag{5.8}$$

$$L(t) = L_0 - Ki_L(t) \tag{5.9}$$

$$K = N^3 M \tag{5.10}$$

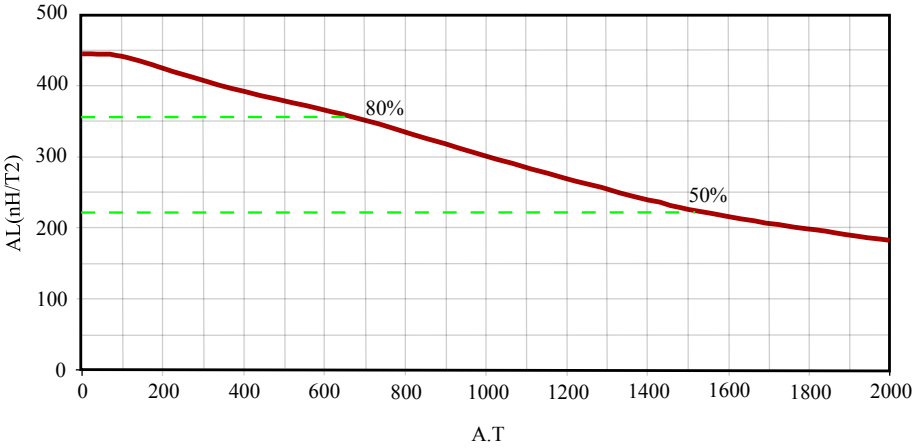


Figure 5.10: Permeance vs amber-turn for Kool Mu 60μ E-core [78].

The permeance A_L at the maximum inductor current is determined by using the inductor permeance as a function of amber-turns, (NI). After that, the number of turns N for a given core permeance A_L is determined using (5.11).

$$L = A_L N^2 \tag{5.11}$$

In this design, Kool Mu 60μ E-core with litz wire is used. Once the core dimensions are selected, the number of winding and the winding area are calculated, and then the inductor volume can be estimated. The volume of three single-phase inductors is derived based on curve fitting of the actual design of Kool Mu 60μ E-core with litz winding at different switching frequency as shown in Fig. 5.11 and given by:

$$V_L = 8.53 \times f_{sw}^{-0.6148} \tag{5.12}$$

In Fig. 5.12, the volume of the main components that contribute to the system volume, i.e. cooling system, DC-link capacitor and filter inductor for different switching frequency were plotted at different heat-sink temperature values. In order to include the heat-sink temperature and power cell loss impact to the total volume reduction, the increase of the reference temperature for heat-sink from 60 ^oC to 90 ^oC can bring significant reduction in overall volume up to 37.8% at switching frequency beyond 32 kHz.

After the switching frequency at full load was chosen at 32 kHz, the Kool Mu LE114 60μ core was selected. The material properties of the Kool Mu LE114 60μ core are mentioned in [77, 78]. The permeance A_L of the core as a function of the ampere-turns is shown in Fig. 5.10. The permeance and inductance of the core linearly reduce with the increase in the inductor current; it has a permeance of 445 nH/T^2 and a relative permeability of 60 at no load, with lower permeability values at higher currents.

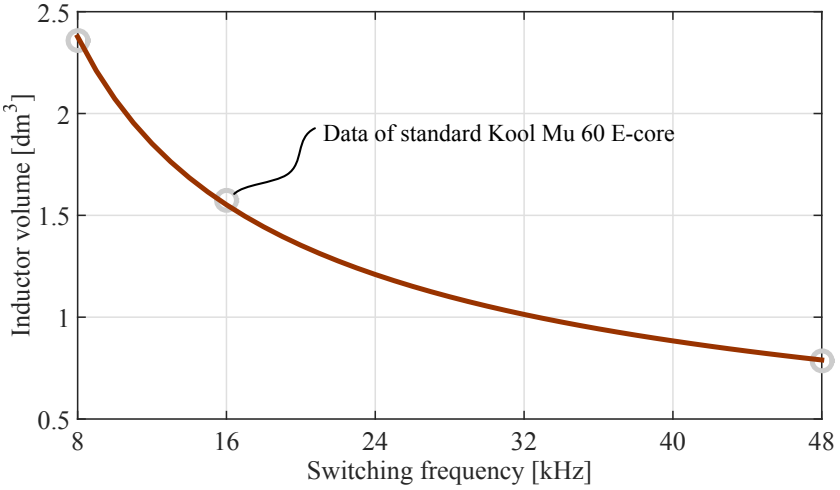
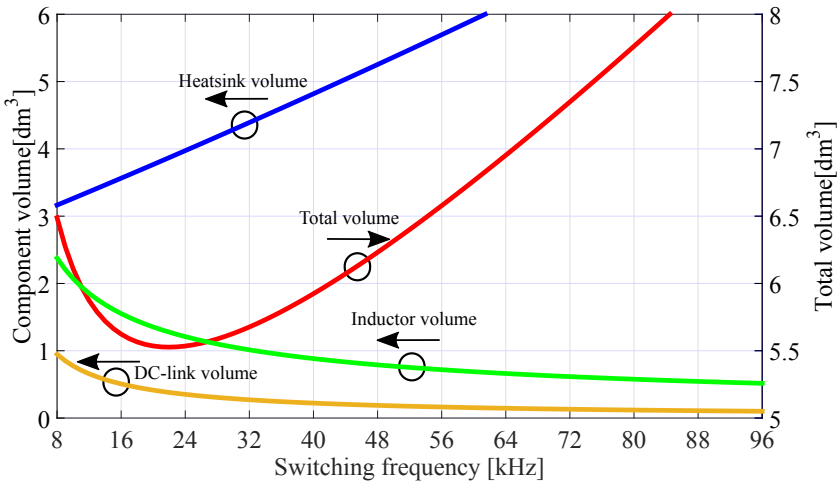


Figure 5.11: Inductor volume at different switching frequency.

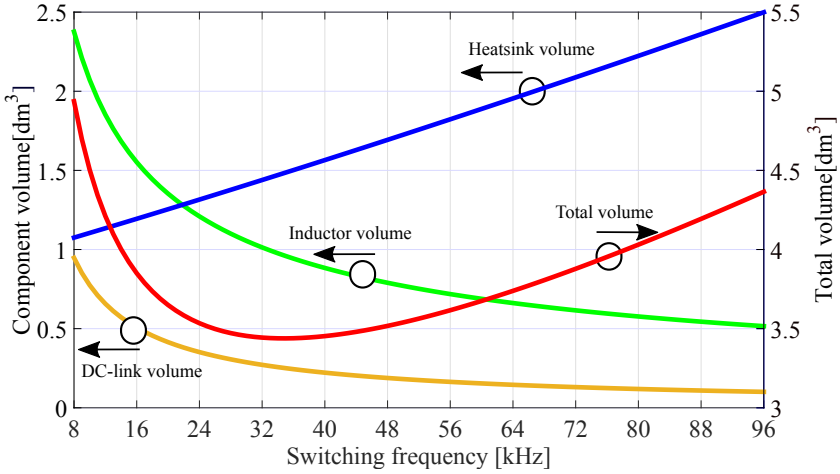
Three single phase Kool Mμ LE114 E-core were designed with 85 turns with the target to provide inductance with a minimum value of 1.1 mH corresponds to 32 kHz switching frequency at the maximum output current of 24.6 A. To achieve low AC resistance at a given switching frequency, i.e. 32 kHz, litz wires with a thickness less than the skin depth is calculated to be 11$\times$0.63 mm.

To improve the converter efficiency at low power loading in the region of interest which has highly probable wind conditions, one important parameter to change is the switching frequency. The switching frequency is varied by tracking the load current based on the relation shown in Fig. 5.13, which is extracted from combining the inverter cell power losses and the nature of wind speed distribution. The nominal switching frequency is 32 kHz, while DC-link capacitors put a limit on the minimum switching frequency at 16 kHz. In between 32 kHz and 16 kHz, the switching frequency decreases in steps as the load reduces. The combination between the inverter power losses and the wind speed distribution as a function of the load current is shown in Fig. 5.14; where the switching frequency is kept at 32 kHz in the region-III which has higher output currents and poor wind speed distribution. In the region-II, the switching frequency decreases in steps as the wind speed distribution becomes more significant, while in the region-I which has highly probable wind speed conditions, the switching frequency is set at 16 kHz to satisfy minimum inverter power losses.

$$f_{sw}[kHz] = \begin{cases} 16, & 0.72A \leq I \leq 5.66A \\ 0.078I^2 - 0.338I + 15.91, & 5.66A < I \leq 12.37A \\ 32, & 12.37A < I \leq 17.68A \end{cases}$$



(a) 60 ^oC heat-sink temperature



(b) 90 ^oC heat-sink temperature

Figure 5.12: Filter inductor, DC-link capacitor, heat-sink and total volume versus switching frequency: (a) at 60 ^oC heat-sink temperature and (b) 90 ^oC heat-sink temperature.

5.3. Proof-of-concept demonstration

To deliver proof-of-concept demonstration of design optimization of a three-phase two-level voltage-source inverter, the inverter was re-designed with variable switching frequency (f_{sw}) modulation: the nominal value is 32 kHz, decreasing in steps to 16 kHz as the load decreases. The heat-sink temperature was kept at 90 ^oC at full load by controlling the heat-sink fan. The output filter inductors were used to ensure compliance with the maximum admissible harmonics generation profiles even at the lower frequencies. The final design of the inverter together with the inductor-filter are shown in Fig. 5.15.

Fig 5.16 shows the obtained experimental phase current waveform at full load. To assess the effectiveness of the inductor-filter to achieve the power quality requirements at different

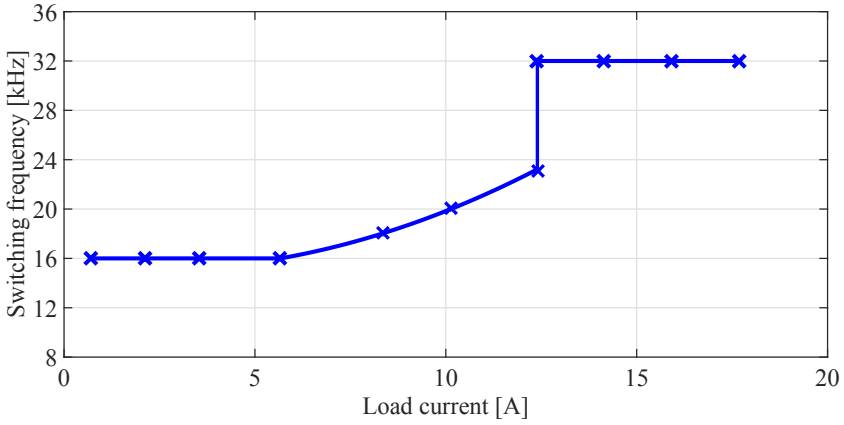


Figure 5.13: Switching frequency and output current relationship.

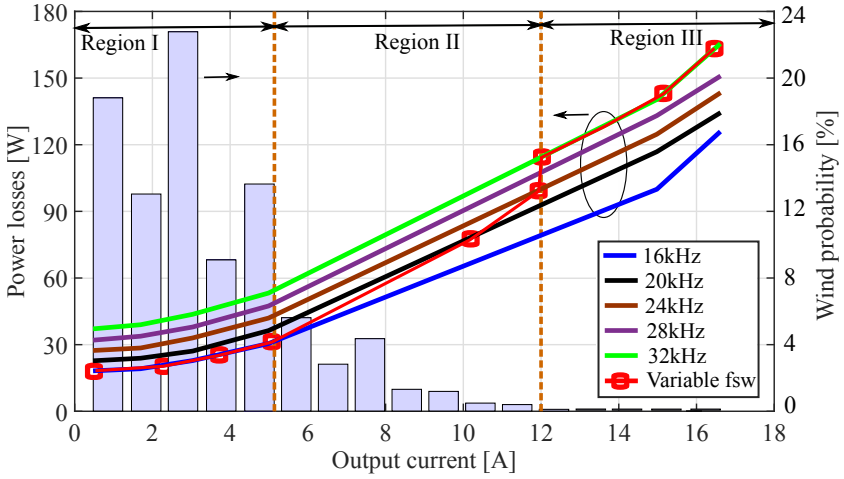


Figure 5.14: Wind speed distribution and inverter cell power losses versus output current at different switching frequencies.

power loading which correspond to different switching frequencies, the output phase current is processed through fast fourier transform (FFT) and its spectrum is shown in Fig. 5.17 and Fig. 5.18. The results indicate that the total harmonic distortion (THD) at full load is equal to 3.78%, which is less than 5%, and the first 40^{th} current harmonics orders meet the standard requirements as a percentage of the fundamental component. The results also indicate that the switching frequency harmonics and the multiple order of switching frequency harmonics are suppressed by using the output filter.

The design also ensures that the power quality requirements are maintained over the whole range of wind turbine power loading. The total demand distortion (TDD) gives better insight about the impact of harmonic distortion at different loads, i.e the THD could be very high at low loads, but its impact on the system is low. Fig 5.19 shows the TDD is complying with the grid requirements, which is less than 5% [34] over the whole range of loading even at high THD at low power demands. Hence, the designed inductor is effective to meet the grid power

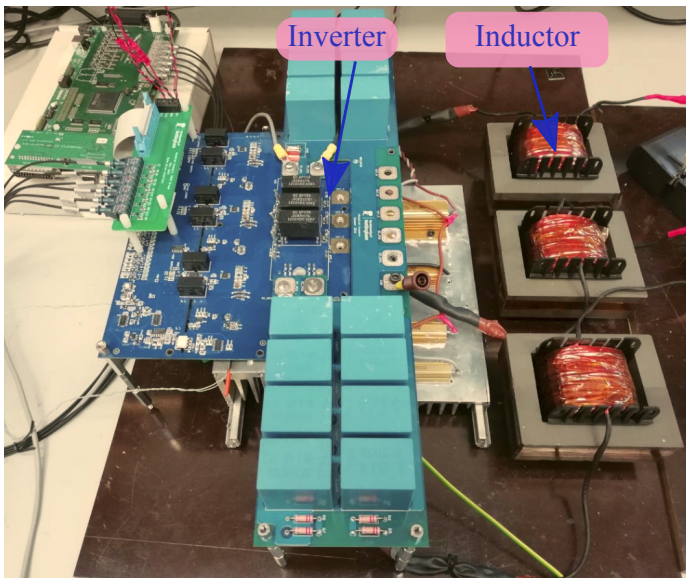


Figure 5.15: Hardware of inductor-filter with 3-phase 2-level inverter.

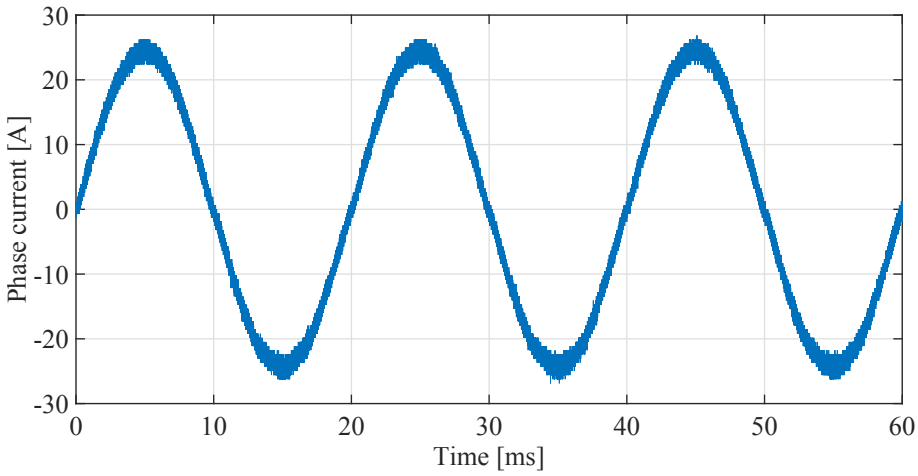


Figure 5.16: Experimental current waveform of the inverter at full power.

quality requirements throughout the whole power loading range.

A Yokogawa WT3000E precision power analyser is used to measure the overall efficiency. The voltage output is measured after the filter-inductor to include the inductor losses together with the power cell losses. The gate driver and the control signal losses are excluded from the measurements. The overall efficiency with fixed switching frequency (32kHz) and variable switching frequency (16 kHz-32 kHz) is presented in Fig. 5.20. The performance difference between fixed and variable switching frequency becomes clearer at low power demand, which corresponds to the most frequent operational time of the wind turbine. The converter achieved the peak efficiency of 98.8% with variable switching frequency.

For grid-connected applications, the annual cumulative lost energy for SiC inverter with

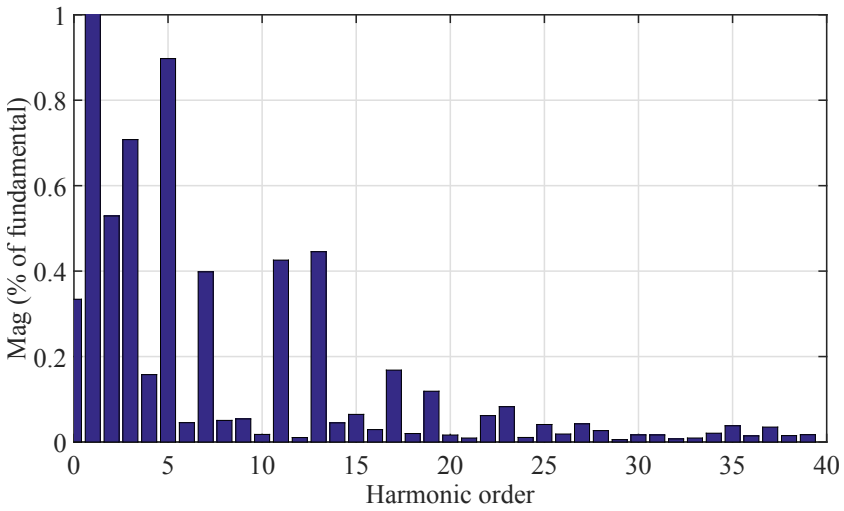


Figure 5.17: Current harmonic limits for the first 40^{th} harmonics at full power.

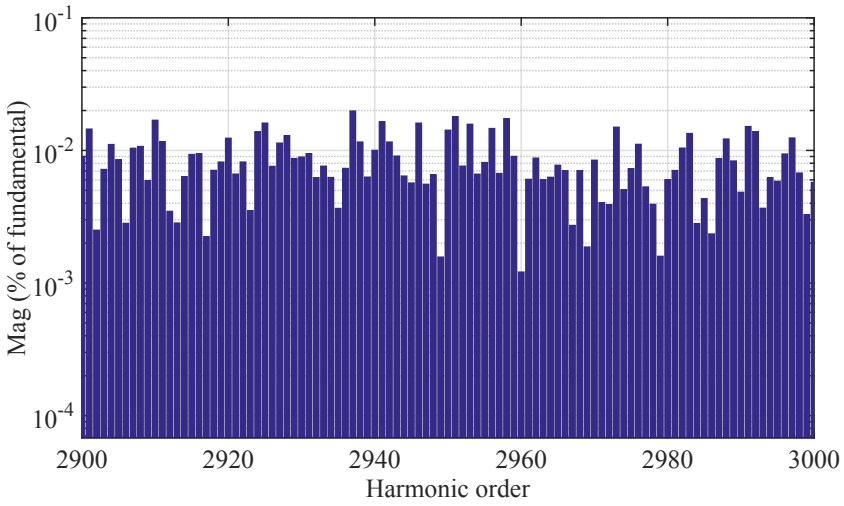


Figure 5.18: Current spectrum at full power (high frequency range).

fixing switching frequency is about 224.6 kWh, and in contrast, 128.7 kWh for the inverter with variable switching frequency as shown in Fig 5.21. This results in a total lost energy saving up-to 42.69% by adopting a variable switching frequency technique.

To validate the thermal performance of the inductor-filter, the temperature at full load power is recorded by the thermocouple data logger (TC-08) and the thermal image is captured using the Fluke IR camera (Ti400) and presented in Fig. 5.22 and Fig. 5.23, respectively. The temperature rise with natural air convection has stabilized at a temperature around 146^oC after 150 minutes of continuous operation and the temperature is less than the maximum allowable temperature of 180 ^oC which is the limit of H-insulation class winding. The hot spot occurs at the area of the winding, as the winding has higher power losses, comparing to other parts of the core and the bobbin. In reality, the temperature rise should not reach the hot spot, i.e. 146^oC

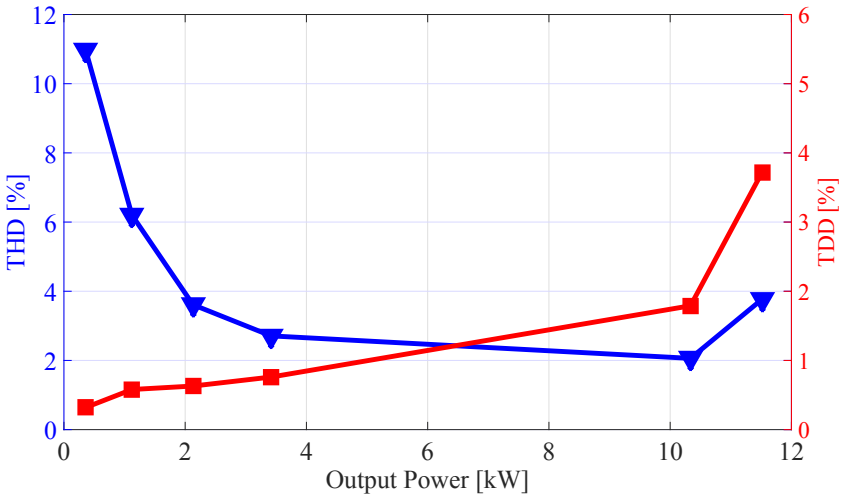


Figure 5.19: Measured current THD and TDD for various output power.

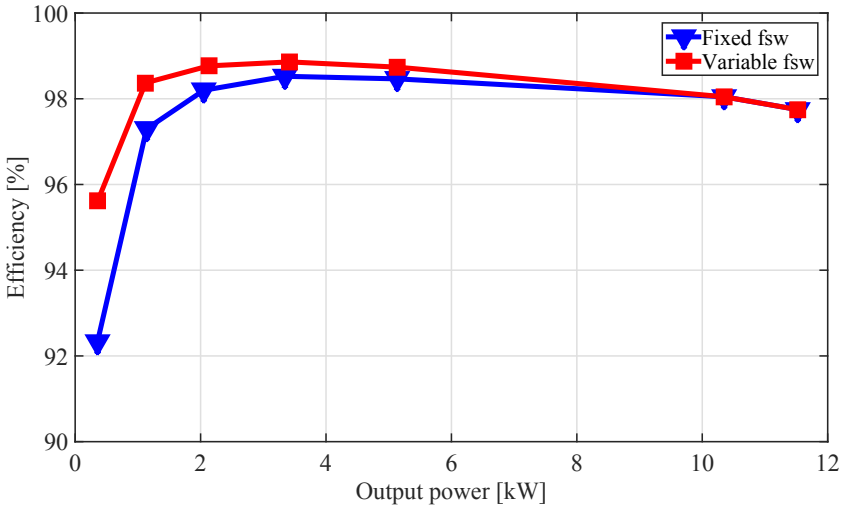


Figure 5.20: Measured overall efficiency vs. load operating at fixed and variable switching frequency.

in this design, because wind turbines spend a small fraction of time working at their maximum power with the intermittent behaviour from the source. In addition, the inductor cooling system based on natural convection can be further improved by inserting a spacer in the middle of the inductor winding to increase the cooling surface area of the winding.

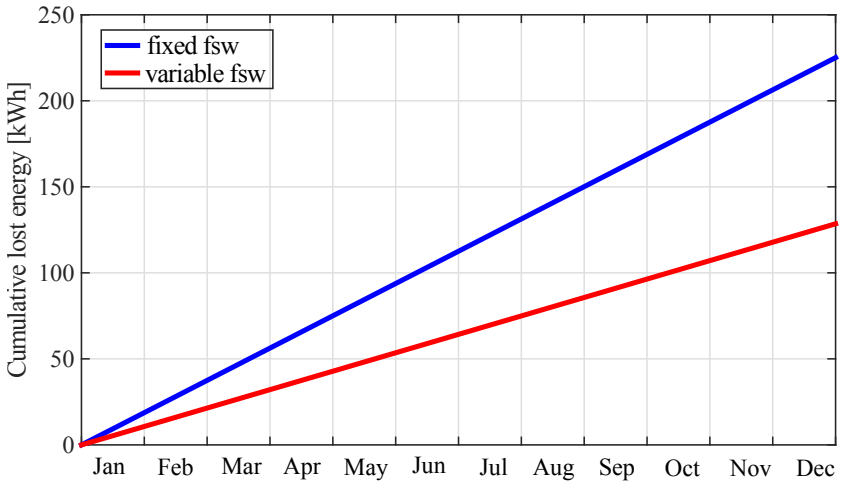


Figure 5.21: Cumulative energy loss of the two-level grid-connected inverter based on fixed and variable switching frequency.

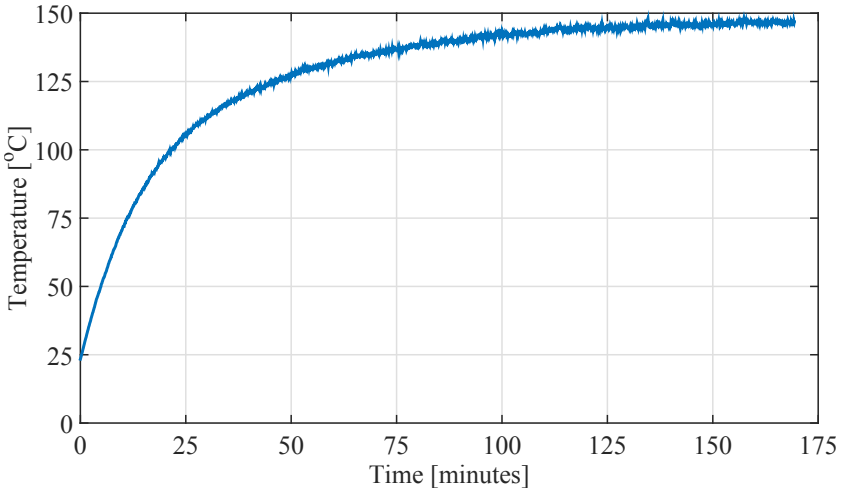


Figure 5.22: Temperature rise versus time of the inverter inductor-filter.

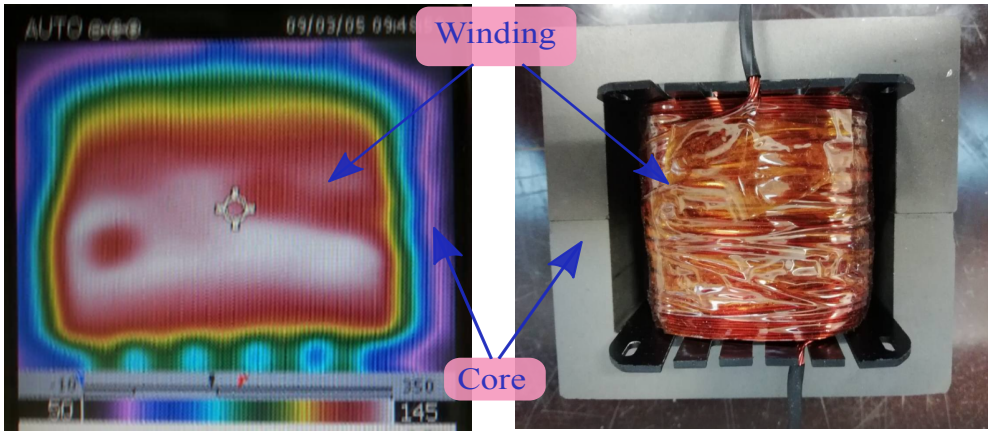


Figure 5.23: The measured inverter inductor-filter thermal image operating at full output power.

5.4. Conclusion

With the aim of maximizing the power density of the inverter, a combined heat-sink and output inductor-filter volume were reduced by increasing the heat-sink temperature from 60^oC to 90^oC, and choosing the optimum switching frequency at 32 kHz for minimum converter volume. To enable optimum trade-off between efficiency versus power density, the inverter was redesigned with variable switching frequency, the nominal value is 32 kHz, decreasing in steps to 16 kHz as the load decreases. The output filter inductors were used to ensure compliance with the maximum admissible harmonics generation profiles even at the lower frequencies. This enables an increase of 37.8% in the inverter power density and saving up to 42.7% of the lost energy per year.

Chapter 6

Transfer of SiC Technology to Medium Voltage Wind Inverter

In this chapter, the knowledge gained in LV SiC devices is transferred to the HV SiC devices, especially 3.3 kV SiC MOSFETs. These devices are not yet commercially available at the time of writing, but are promising to become a key SiC component in the near future. This chapter starts by reviewing the specific characteristics of HV SiC MOSFETs. A detailed parametric characterization of a 3.3 kV SiC MOSFET half-bridge module with parallel chips and body-diode freewheeling is then presented. After that, the performance of the 3.3 kV SiC devices are analysed in a medium voltage wind inverter at different wind speeds, temperatures, and switching frequencies. Finally, the results presented for 3.3 kV SiC devices in a half-bride module were used to simulate the efficiency performance of wind inverter in high power wind application.

6.1. High voltage SiC MOSFET devices

Recently, 3.3 and 6.5 kV power MOSFETs with characteristics superior to counterpart Si IGBTs have been introduced [79]. Fig. 6.1 shows the 3.3 kV SiC MOSFET chip from ROHM Semiconductors Ltd, Japan, with nominal continuous current of 50 A (on-state resistance of 52 $m\Omega$ at 125^oC), and die area of 7.2 $mm\times$7.2 mm, with maximum operating temperature of 175 ^oC. It is a vertical power MOSFET with the indication of gate and source terminals on the top of the chip while the drain, not shown, is on the bottom of the chip. As can be seen, the devices, with a nominal rating of 50 A, exhibit nearly a 4 to 5 times bigger cross-section than counterpart lower voltage rated SiC MOSFETs.

Fig. 6.2-a shows a comparison between Si and SiC devices at 3.3 kV blocking voltage level in terms of on-state voltage characteristics. 3.3 kV SiC MOSFET devices offer the best

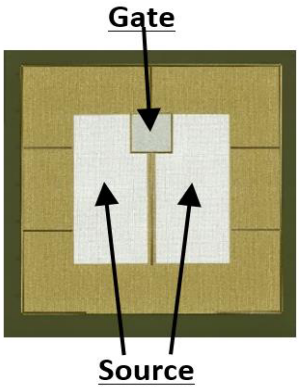
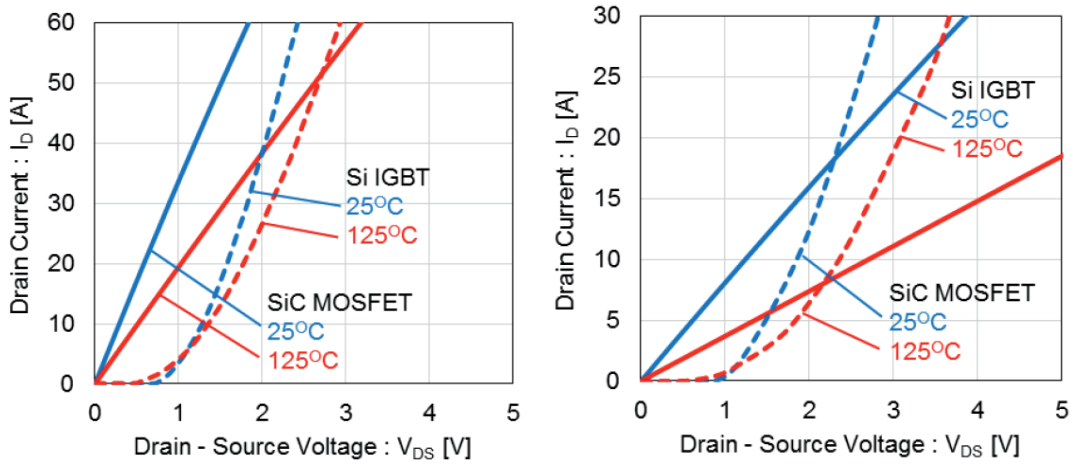


Figure 6.1: 3.3 kV 50 A SiC MOSFET chip with the indication of the gate and source at the top and the drain on the bottom of the chip (not shown) [18].

on-state voltage performance up to 50 A at $T_j = 125^oC$. The 6.5 kV SiC MOSFET devices shown in Fig. 6.2-b provide better on-state voltage at lower currents, i.e. less than 18 A at $T_j = 25^oC$ and less than 8 A at $T_j = 125^oC$ [79]. The good on-state performance of SiC MOSFET devices at low currents are still important in wind turbine applications if high wind speed distribution at light loading is taken into account.

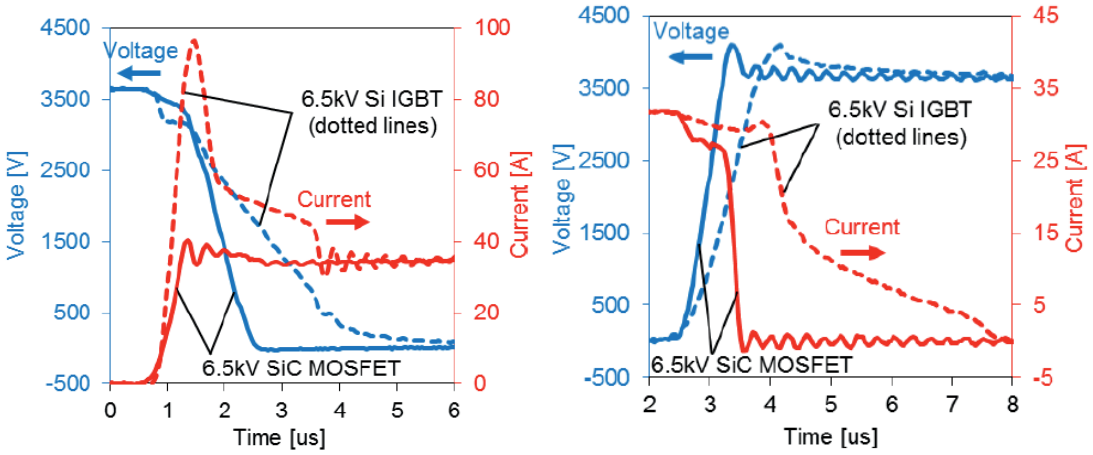


(a) 3.3kV (b) 6.5kV

Figure 6.2: Conduction loss characteristics of Si and SiC switches: (a) 3.3 kV power device and (b) 6.5 kV power device [79].

The switching waveforms of 6.5 kV SiC MOSFET and Si IGBT are shown in Fig. 6.3. They indicate that HV SiC devices have faster-switching speed than that of Si, and thus a significant reduction in switching losses was maintained. For example, the total switching loss (turn-on plus turn-off) of 6.5 kV SiC MOSFET (155 mJ tested at 3.6 kV dc and 32A), is much less than that of 6.5 kV Si IGBT (563 mJ at the same test conditions) [79]. During turn-on, HV Si IGBT shows overshooting of current due to the P-i-N diode reverse recovery, which

is mainly due to the reverse recovery charge of junction capacitance. Due to the absence of minority carriers, the only reverse current in SiC MOSFET is due to the junction capacitance even the body diode is a P-N junction. In addition, the tail currents associated with Si IGBT devices during turn-off transition causes additional significant power losses to the device.



(a) Turn-On transition

(b) Turn-Off transition

Figure 6.3: Switching loss characteristics comparison for 6.5 kV Si and SiC power devices at 3.2 kV and 32 A: (a) Switching-On waveforms and (b) Switching-Off waveforms [79].

Replacing HV Si IGBT devices with HV SiC MOSFET devices enables high frequency operation (in the range of 5 kHz-10 kHz for HV SiC devices compared to 500 Hz-1 kHz for HV Si devices), and reduced power losses which are significantly decrease the size and weight of the power converters which is required in offshore wind turbines where a limited space is available in the Nacelle. Moreover, the high switching capability of SiC MOSFET devices at medium voltage (MV) high power grid connection can benefit higher bandwidth operation, and thus better transient performance can be maintained. For example, for MV grid-connected wind inverters, the use of SiC devices with higher bandwidth controller enables the operation of active power filters to improve the grid power quality [80].

In addition, SiC devices allow a reduction of $1/3$ of the switching device area for a given current by the use of a built-in body-diode for freewheeling the inductive currents to replace the existing IGBT with an external diode solution. Moreover, the possible implementation of synchronous rectification in inverter operation enables the reduction of conduction losses [18, 81].

Due to the better performance of SiC power semiconductors compared to Si, SiC MOSFET power devices in VSI-topology have to achieve a dominant position in the field of low as well as of medium voltage wind turbines. For low voltage wind conversion systems, the 2L-VSI is a good candidate, but this simple inverter topology can also be used for medium voltage applications. However, power semiconductor devices with higher blocking voltage are required, since

the series connection of power devices yields a complex control issue of voltage balancing and additional snubber circuits are required.

However, with the appearance of HV SiC-MOSFETs, thanks to WBG material with a high critical electrical field, it is getting possible to return to a simple 2L topology in MV wind energy systems with a comparable efficiency and reduced system complexity and overall cost including the running cost and energy saving over time. If MMC is assumed to be used in MV wind inverter, the application of HV SiC devices will help to reduce the number of sub-modules or the number of devices in series connection in each module, and then a simpler circuit is achieved. Therefore, HV SiC power devices are an enabling technology for power converters with advantages of simple, reliable, and low-cost power converters to be used in medium voltage wind turbines for modern power distribution systems.

In a 2L VSI topology, each semiconductor should withstand the total DC-voltage (V_{DC}). The required DC-link voltage, V_{DC}, as a function of line grid voltage ($V_{G,RMS}$) can be calculated by [82]:

$$V_{DC} = \sqrt{2} \times V_{G,RMS} \times \left(1 + \frac{x}{100}\right) \tag{6.1}$$

the over voltage factor, x, typically equal to 15% for medium voltage systems.

The required semiconductor blocking voltage can be calculated by [82]:

$$V_B = V_{DC} \times \left(1 + \frac{y}{100}\right) \tag{6.2}$$

where y is the safety factor which is selected about 50% for low stray inductance circuits and 60% for medium stray inductances. Then the preferred device voltage rating is selected as the next highest standard device voltage rating.

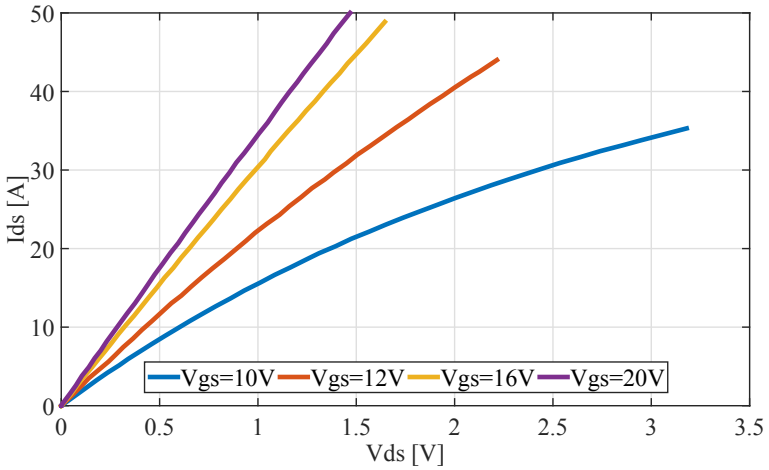
Some standard semiconductor blocking voltage ratings for various ac line voltages are shown in Table 6.1. As shown, future semiconductor devices with higher voltage capability can lead to elimination of the line frequency ac transformer in modern power systems.

Table 6.1: Required blocking voltage in 2-L VSI.

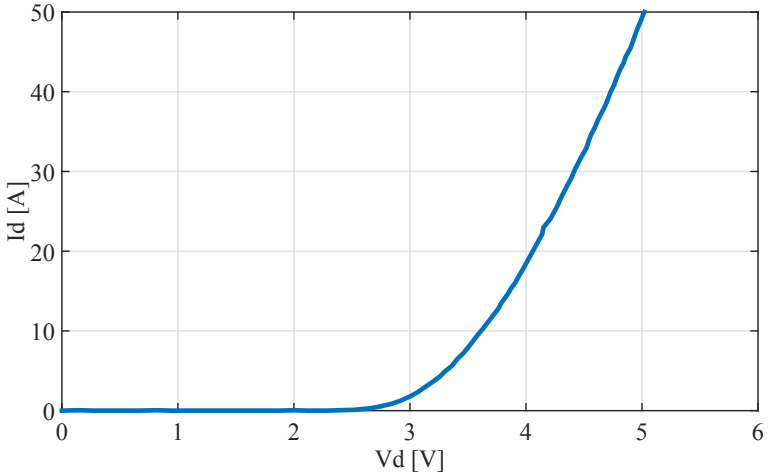
Nominal line voltage (V)	Nominal DC-link voltage (V)	Required semiconductor blocking voltage (V)
1100	1800	3300
2700	4500	6500
4100	6600	10000
6700	11000	15000

6.2. 3.3 kV SiC MOSFET chip characterization

Fig. 6.4 shows the measured output characteristics of a SiC MOSFET and the body-diode forward characteristics. The reported output characteristics in Fig. 6.4 -a shows that the device exhibits very good on-state performance at the gate-source voltage of 20 V which is the nominal driving voltage of reference for MOSFET devices with a value of on-state resistance equal to 30 $m\Omega$ at room-temperature. Moreover, Fig. 6.4 -b shows that the body-diode enables the use of synchronous rectification for optimum performance. During the freewheeling period, the MOSFET can provide a path with a smaller voltage drop compared with the body-diode which is only conducting during the dead times in a few hundreds of nanoseconds.



(a) MOSFET.



(b) Body-diode.

Figure 6.4: Measured device characteristics: (a) MOSFET output characteristics, and (b) Body-diode forward characteristics (V_{gs}=-3.3V), at ambient temperature.

Fig. 6.5 shows the measured temperature dependence of the MOSFET output and the body-diode forward characteristics, measured at two different baseplate temperatures, 25 ^{o}C

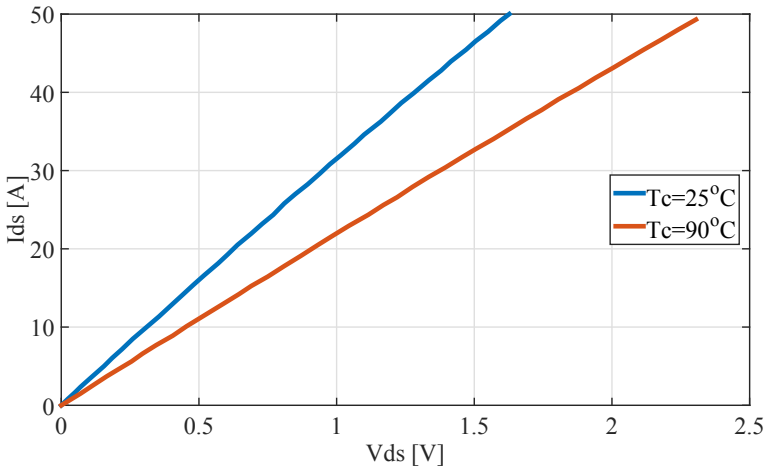
and 90 ^{o}C. Although as expected in low voltage SiC devices, the effect of temperature on the on-state characteristics of the SiC MOSFET is more pronounced than the temperature dependency of diode forward characteristics, the advantages of using synchronous rectification in HV SiC power devices for freewheeling are still visible up to considerable operational temperature values. For example, the MOSFET conduction voltage at a current level of 50 A and baseplate temperature of 90 ^{o}C is half the value of body-diode conduction voltage at the same test conditions. This can help to reduce the body-diode high on-state losses by using the MOSFET body-diode and synchronous rectification.

Moreover, adopting a body-diode solution leads to reduce the high cost of HV modules, and a straightforward reduction of the semiconductor area will be achieved by eliminating the external HV freewheeling diode. Some manufacturers prefer using Schottky diode in LV modules, i.e 1.2 kV six-pack power module used in this work, to provide better performance. However, using the body-diode will decrease the high cost and the size of HV SiC devices. In addition, due to the improvement at the technology level, the body-diode of low voltage SiC devices work reliably for current freewheeling in inverter operation [83]. The preliminary tests of 3.3 kV SiC MOSFET considered here show that the body-diode works reliably and no signs of ageing or any degradation have been detected.

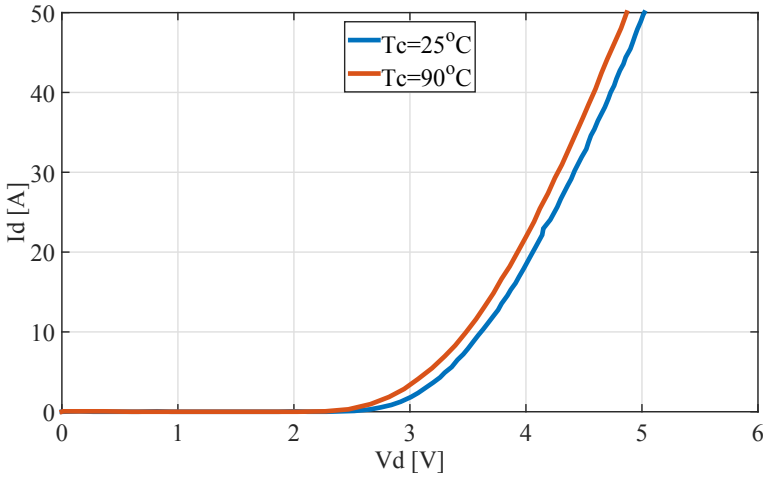
Fig. 6.6 shows the measured spread among 4 devices. It is observed that the difference in the output characteristics is mainly related to a small difference in threshold voltages, which is considered a very tight distribution in comparison with commercial products at a lower voltage. As shown in Fig. 6.7, the maximum deviation in the device threshold voltage is about 0.37 V which is less than the acceptable limit of 1 V for SiC devices. In addition, the four body-diodes have a satisfactory spread in the on-state performance in view of high voltage technology. Therefore, the gathered results are encouraging for the development of multi-chip modules based on HV SiC MOSFET power devices with a body-diode for freewheeling.

6.3. 3.3 kV SiC MOSFET half-bridge module

The 3.3 kV/100 A SiC MOSFET Half-Bridge Module has been recently developed by the PEMC group at the University of Nottingham [18]. The half-bridge module has two chips in parallel for each switch to achieve a total module current of 100 A. The hardware of the fabricated 3.3 kV/100 A SiC MOSFET is shown in Fig. 6.8, in the top, the open module can be seen, in the bottom, the module encapsulation to protect the dies and package from environmental conditions. The module assumes three power terminals; positive bias (DC+), the negative bias (DC-), and middle point (M), and two drive terminals; each consists of gate (G) and source (S) connections (G-HS/S-HS and G-LS/S-LS). The module enables full separation of drive and power loops by using Kelvin-source type connection, to avoid interference of switching load currents with gate-loop parasitic inductance, and therefore high switching



(a) MOSFET.



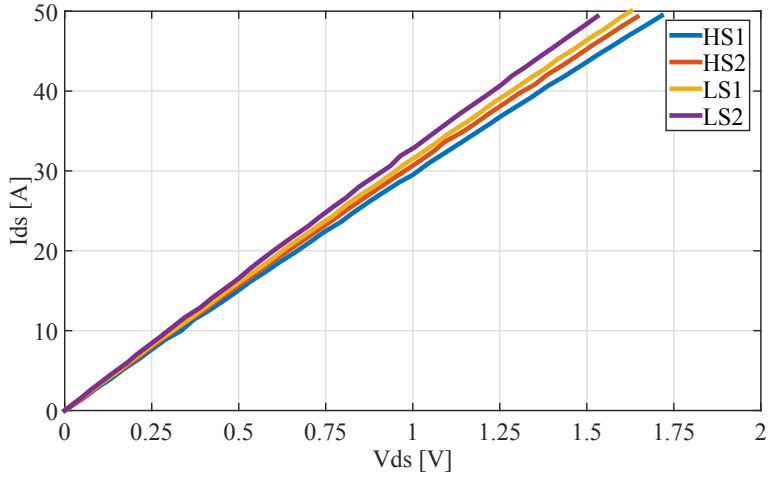
(b) Body-diode.

Figure 6.5: Temperature dependency of (a) MOSFET output characteristics, and (b) body-diode forward characteristics.

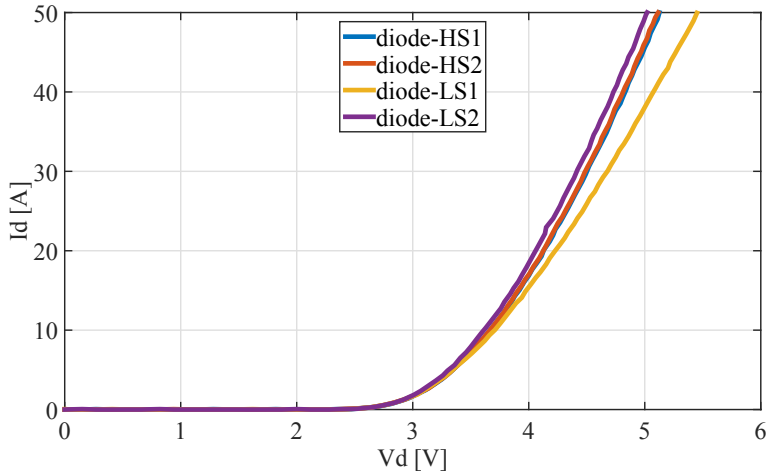
performance can be ensured.

6.4. Switching characteristics of 3.3kV/100A SiC MOSFET module

The parametric switching characterisation of 3.3 kV SiC MOSFETs and their body-diodes over temperature and load conditions are performed experimentally using the clamped inductive DPT circuit. The gate signal to the upper module MOSFET is kept low at -3.3 V to ensure a fully blocked MOSFET during freewheeling while the bottom MOSFET which represents the device under test (DUT) is driven by a double pulse signal with +20 V level for turn-on and -3.3 V for turn-off. The body-diode of upper MOSFET in the top module is used as a freewheeling diode for inductive currents. The DUT current rise is controlled by the width of pulses while the DC-link voltage and the inductor values are kept at 1.8 kV and 1.2 mH, respectively.



(a) MOSFET.



(b) body-diode.

Figure 6.6: Measured spread in (a) MOSFET output characteristics, (b) body-diode forward characteristics, for four devices at V_{gs}=18 V.

The corresponding hardware setup is shown in Fig. 6.9; film capacitor technology is only used with a total value in excess of 1 mF. The film capacitors were distributed into two groups, with different values, which are the input bulk capacitors and the first stage of high-frequency decoupling filters. In addition, a set of commutating capacitors based on CeraLink capacitors are mounted very close to the module switches to prevent destructive voltages at turn-off. However, preliminary test results show that ceramic capacitors - if properly mounted - can help to compensate the value of the parasitic inductance and to get cleaner switching waveforms, so that, more efforts should be taken to include higher value configurations of CeraLink capacitors in the PCB design. The device under test (DUT) is mounted on a hot plate where the temperature is controlled to maintain the junction temperature, since there are not enough power losses in the module during the DPT.

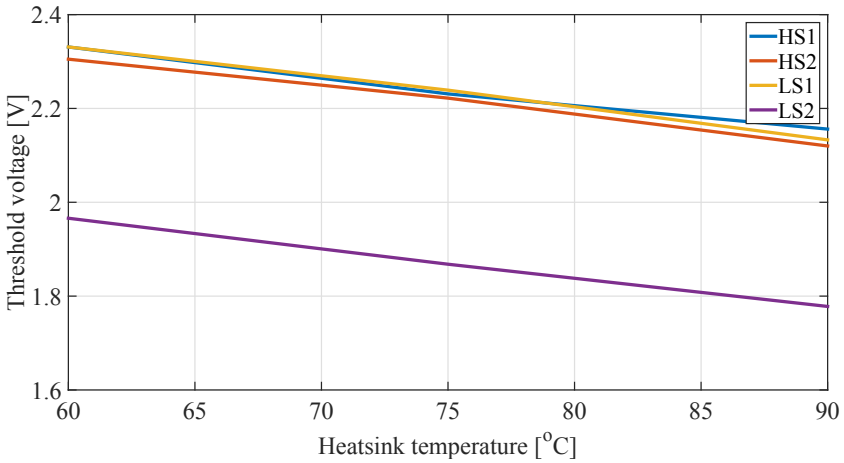
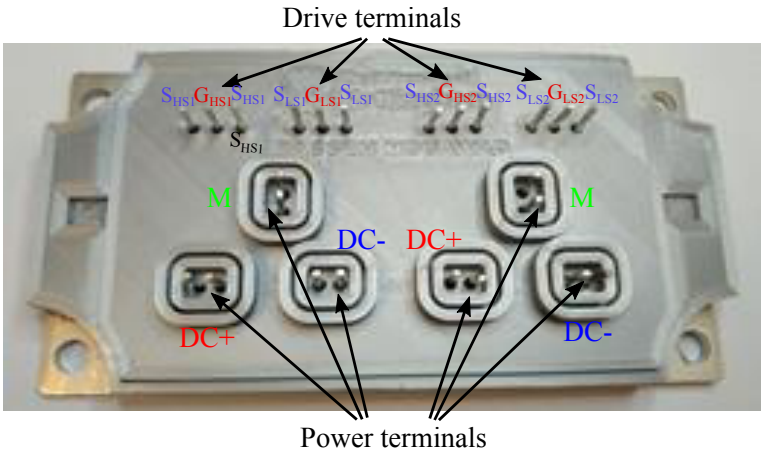


Figure 6.7: Measured threshold voltages for four devices at different heat-sink temperatures .



(a) Open module.



(b) Encapsulated module.

Figure 6.8: View of 3.3kV/100A module hardware: (a) Open module, including power and drive terminals, and (b) fully encapsulated module [18]

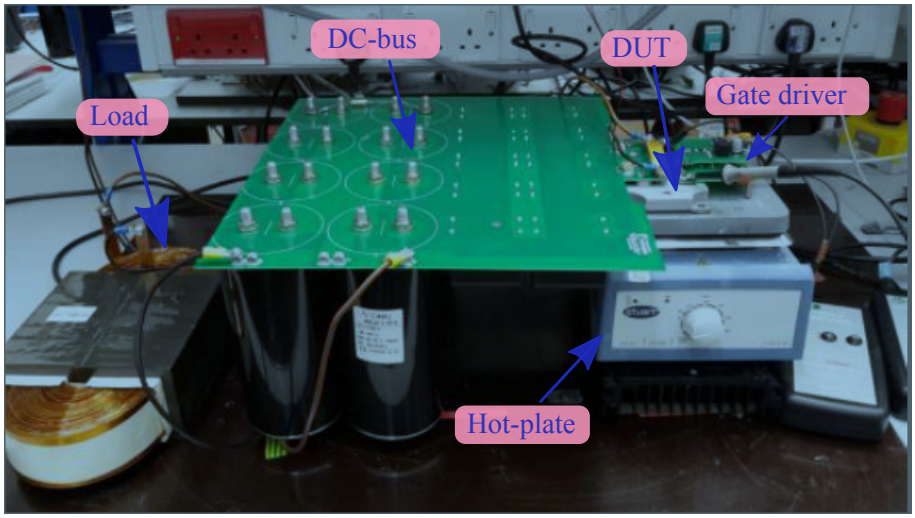


Figure 6.9: Test circuit hardware setup, with indication of dc-bus capacitors, inductive load, gate drivers and device under test (DUT).

The circuit components along with details of instruments are given in Table 6.2 and Table 6.3, respectively, where the current and voltage probes are deskewed to eliminate any delay in the measured current and voltage signals, and thus accurate power loss measurements are maintained.

Table 6.2: Components details.

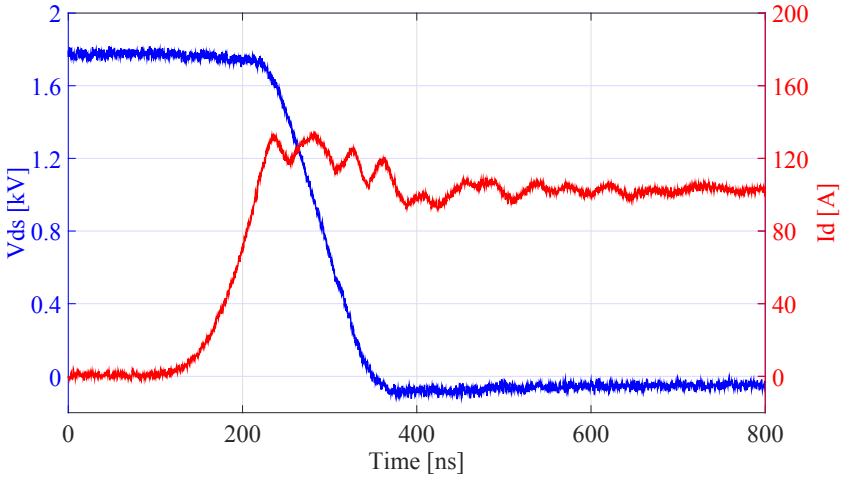
Component	Model	Value
Load inductor	Air core	1.2 mH
Bulk input capacitor	C44U	500 μF×8
Decoupling capacitor	MKP1848C	30 μF×10
Commutating capacitor	CeraLink	0.25 μF×10

Table 6.3: Instruments details.

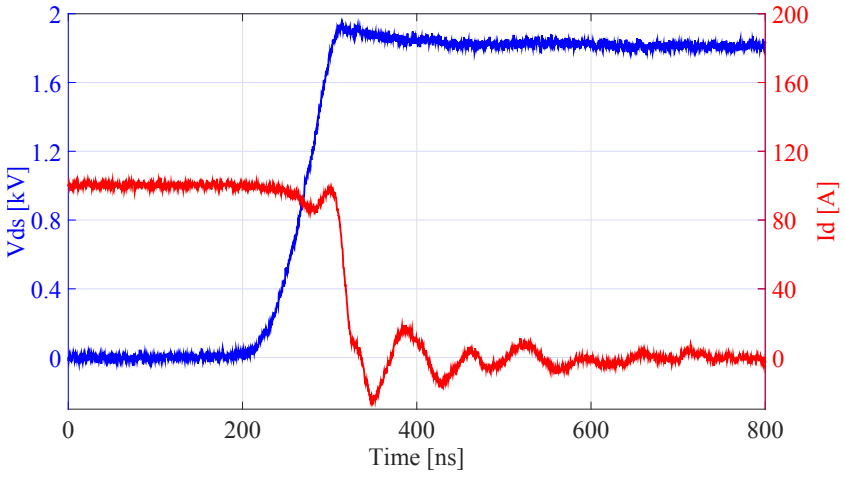
Component	Model	Bandwidth	Deskew
Rogowski current probe	CWT/UM	40 Mhz	15 ns
Voltage probe	701926 Diff	50 Mhz	12 ns
Oscilloscope	Lecroy	600 Mhz	with deskew
Hotplate	US150	–	–

Fig. 6.10 shows the turn-on and turn-off switching characteristics of the 3.3kV/100A SiC MOSFET module, at 1.8 kV, the current nominal rating of 100 A, and 75 ^{o}C case temperature. The turn-on and turn-off gate resistances used are chosen as 10 Ω and 5 Ω, respectively. The measured current waveforms refer to the total current of the two parallel chips. As seen in

Fig. 6.10-a, the current peak overshoot is due to the body-diode reverse recovery of the complementary switch, but mainly as a result of the MOSFET stray capacitance in the presence of high dv/dt (i.e.13V/ns). However, at low switching current, higher current overshoot with oscillations is observed. The turn-off transition presented in Fig. 6.10-b does not show any significant voltage overshoots which usually happen as a result of the parasitic inductance of the switching loop, i.e. the parasitic inductance of the power plan and module package. This means the circuit is designed well with the low degree of parasitic inductance.



(a) Turn-on.



(b) Turn-off.

Figure 6.10: Switching characteristics at T_c=75 ^{o}C (a) Turn-on, $R_{g,on} = 10\Omega$ and (b) Turn-off, $R_{g,off} = 5\Omega$.

In Fig. 6.11, switching energy losses (on, off and total) are reported over different device currents (from 10 A to the nominal module rating current of 100 A) at the drain-source voltage of 1.8 kV, and the hotplate temperature is kept controlled at 75 ^oC. It is seen that the contribution of turn-on switching losses is around two-thirds of the total losses. At high switching rates, the turn-on switching losses is dominated by the current overshoots, so that, more atten-

tion should be paid to minimize the current overshoots, i.e. by introducing suitable values of high-frequency filters closer to the device for more cleaner switching.

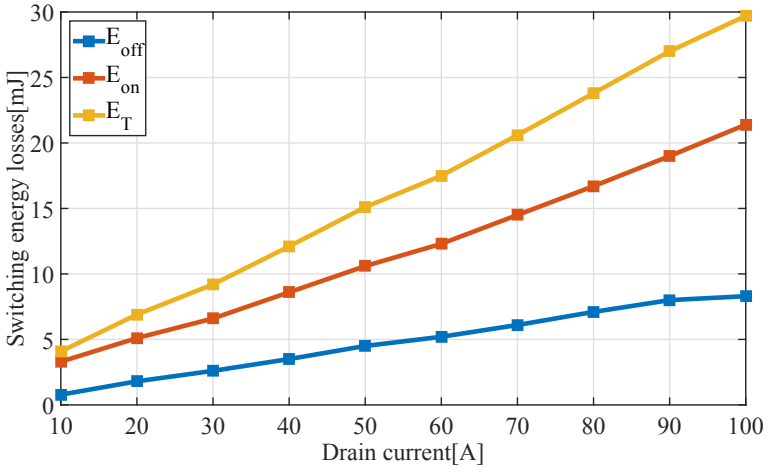
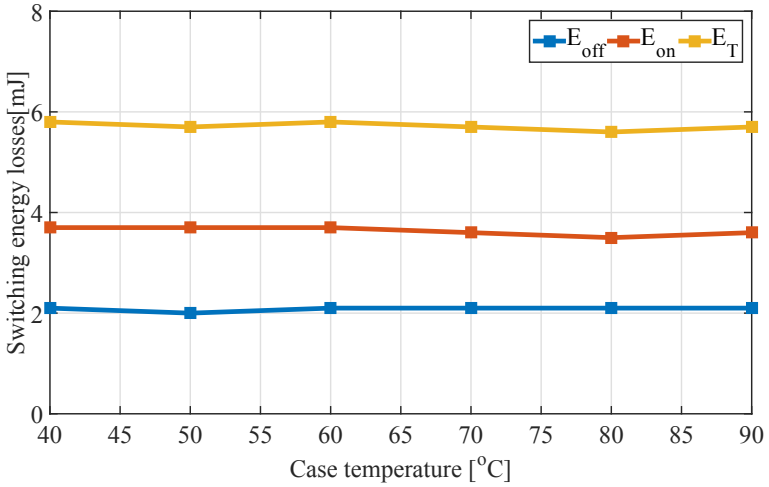


Figure 6.11: Measured energy losses over current at $V_{ds} = 1.8kV$ and $T_c = 75^oC$.

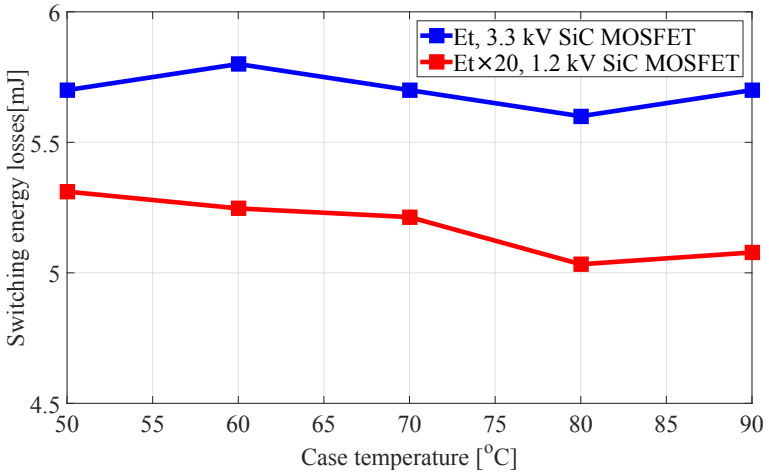
The switching loss variations with baseplate temperature are presented in Fig. 6.12-a. It is seen that the turn-on losses go down slightly with the increase in baseplate temperature; the reason for this is the decrease in device threshold voltage with higher junction temperatures. On the other hand, the turn-off loss increases somewhat at the higher temperature. As a result, the total switching loss is stable for a wide range of baseplate temperatures. This behaviour is in line with findings in lower voltage devices, i.e. 1.2 kV SiC MOSFETs, as presented in Fig. 6.12-b. This is a key feature of SiC which can help deliver new ways of designing power electronics conversion systems by joint optimization of high-frequency operation and high heat-sink temperature.

It is observed from Fig. 6.13 that with a lower drain current, longer switching times during the turn-off process are needed. This is the reason why the increase of E_{off} with the load current is less than E_{on}. In low voltage SiC devices, i.e. 1.2 kV blocking voltage class, the switching results shows that the switching time can be as small as 50 ns due to their high switching speed. Therefore, high switching performance can be attained without compromising the efficiency and power quality. However, the variation of turn-off switching times of 3.3 kV SiC MOSFET is much more pronounced than that in 1.2 kV devices due to more dependence of the drain-source capacitance at low voltage levels on the drain currents. This behaviour should be taken into account when setting the designing parameters of the inverter, for example, the dead time between commutationof complementary switches should be chosen for the worst case (longest switching time). Longer dead time for HV SiC devices may limit their operating switching frequency due to power quality concern in comparison to LV ones.

Fig. 6.14 shows turn-on and turn-off switching current sharing for two parallel transistors of the lower switch. The results show good current sharing of SiC MOSFETs even during fast



(a) 3.3 kV SiC MOSFET.



(b) Comparison between 3.3 kV and 1.2 kV SiC MOSFETs.

Figure 6.12: Measured energy losses over different baseplate temperature: (a) 3.3 kV MOSFET (3 curves, on, off and total) at $V_{ds} = 1.8kV$ and $I_{ds} = 15A$ and (b) Thermal behaviour comparison between 3.3 kV SiC MOSFET at $V_{ds} = 1.8kV$, $I_{ds} = 15A$ and 1.2 kV SiC MOSFET at $V_{ds} = 0.7kV$, $I_{ds} = 10A$.

transition events, thanks to the positive coefficient of SiC MOSFETs on-state resistance and well designed symmetry of the stray parameters in SiC power module. It is remarkable that the SiC MOSFET parallel chips have great power balance compared to Si IGBT modules, which show that some parallel chips are more stressed than others by the imbalanced power loss as a result of imbalanced current sharing between Si IGBT transistors [84, 85].

Fig. 6.15 shows the results of the body-diode transient switching operation for two parallel transistors in the higher switch; it is clear that the body-diode of parallel transistors also exhibit good reverse recovery current sharing during turn-off under extensive current stress up-to their rated current, and the body-diode also shows a good stable temperature operation over a representative range of baseplate temperatures. The results gathered so far show good reverse

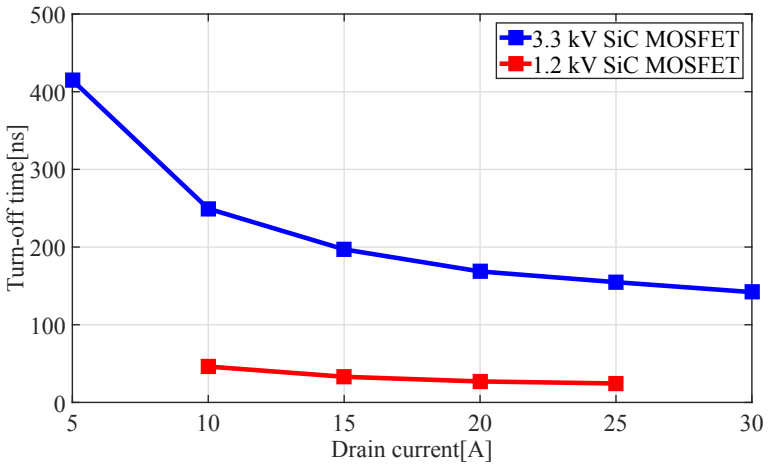


Figure 6.13: Measured turn-off switching time over device current at $V_{ds} = 1.8kV$, Rg=5Ω, Tc=75 ^oC for 3.3 kV SiC MOSFET (blue data) and at $V_{ds} = 0.7kV$, Rg=5Ω, Tc=25^oC for 1.2 kV SiC MOSFET (red data).

recovery performance of body diode, good power-sharing and stable temperature operation, enabling usage of synchronous rectification to replace the traditional freewheeling and increase the system efficiency at MV power converters.

6.5. Application to wind generation

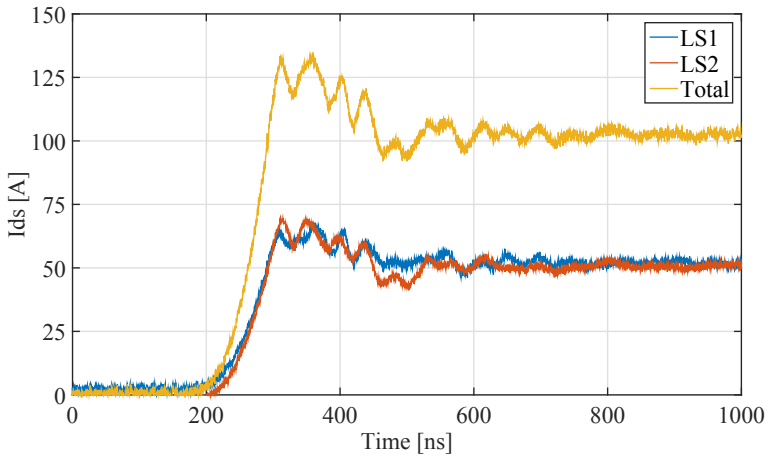
In addition to the promising applications of SiC devices in low voltage wind inverters, high power wind turbines at the medium voltage level is another attractive area for SiC devices. In this section the results presented for 3.3 kV SiC devices in a half-bride module will be used to simulate the efficiency performance of a wind inverter in a high power wind application. A 0.9 MW wind turbine system was chosen as a case study, the output power curve of the wind turbine is shown in Fig. 6.16; it is characterized by a flat output power around the generator rated power for higher wind speed, because stall and pitch control are implemented [86].

6.5.1. Power loss model

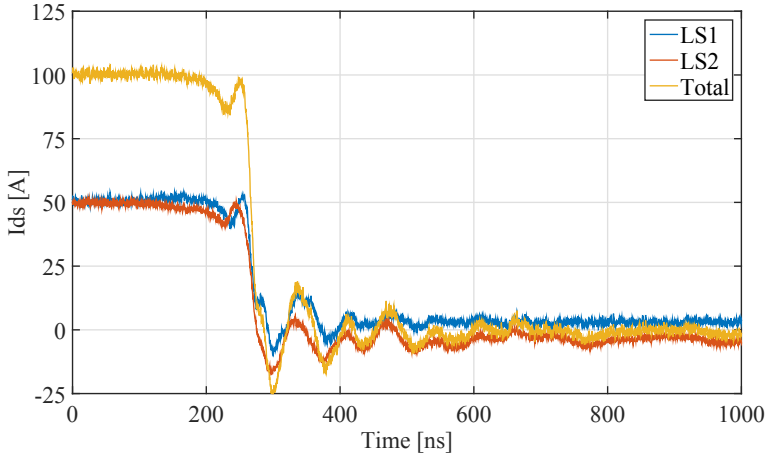
In this section, the power loss model is presented based on the data extracted from the extensive static and dynamic characterization of 3.3 kV SiC devices performed in the previous section. The values of on-state and switching parameters of the SiC MOSFET and its body-diode and their temperature dependency are listed and used by the power loss model of SiC-based prototype (i.e., 2L-VSI).

The on-state resistances for the 3.3 kV SiC MOSFET chip in [$m\Omega$] as a function of the device case temperature is given by:

$$R_{S,on} = a_1 T_c + a_0 \tag{6.3}$$



(a) Turn-on.



(b) Turn-off.

Figure 6.14: Transient switching drain current waveforms for two parallel devices (a) Turn-on and (b) Turn-off.

Where a_1 and a_0 are coefficients derived from the MOSFET on-state resistance information.

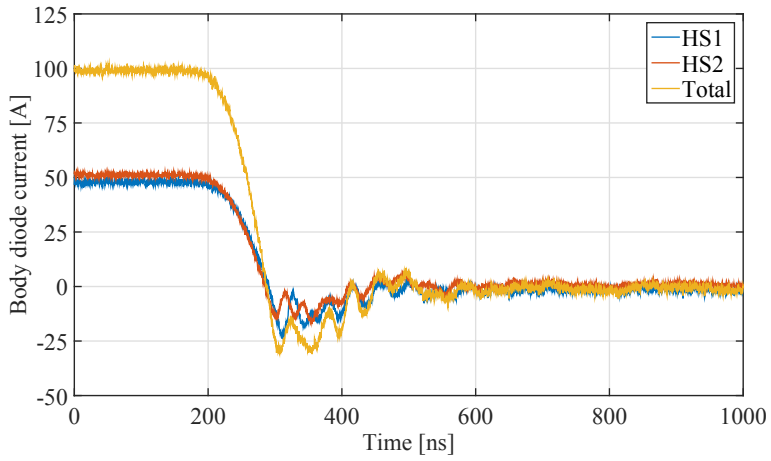
Table 6.4: MOSFET on-state resistance parameters

Parameter	Value
a_1	0.1
a_0	46.7

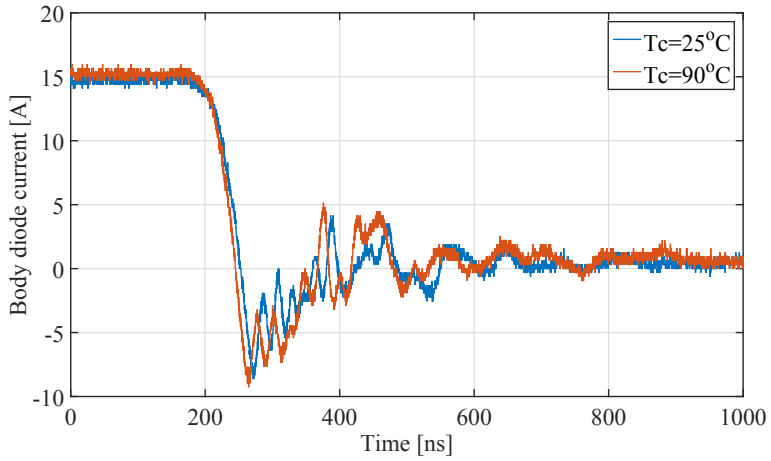
The on-state voltage and resistance of the MOSFET body-diode depend on the case temperature as follows:

$$V_{D,on} = \alpha T_c + V_{D0} \tag{6.4}$$

$$R_{D,on} = \beta T_c + R_{D0} \tag{6.5}$$



(a) Current sharing.



(b) Temperature stability.

Figure 6.15: Body-diode turn-off performance: (a) Transient switching body-diode turn-off current for two parallel devices in the high-side switch at $V_{ds} = 1.8kV$ and $I_{ds} = 100A$ and (b) Temperature stability of body-diode turn-off reverse recovery current at $V_{ds} = 1.8kV$ and $I_{ds} = 30A$.

where α, β, V_{D0} and R_{D0} are extrapolated from the body-diode forward characteristic data.

The switching energy loss of the SiC MOSFET in (mJ) as a function of the output current can be expressed by a second-order polynomial function:

$$E(i) = b_2 i^2 + b_1 i + b_0 \tag{6.6}$$

where b_2, b_1 and b_0 are constants derived from the curve fitting of the DPT switching characterization.

The switching losses assumed that SiC MOSFET and its body-diode have a negligible temperature dependency and the body diode has reverse recovery energy equal to 2.18 mJ.

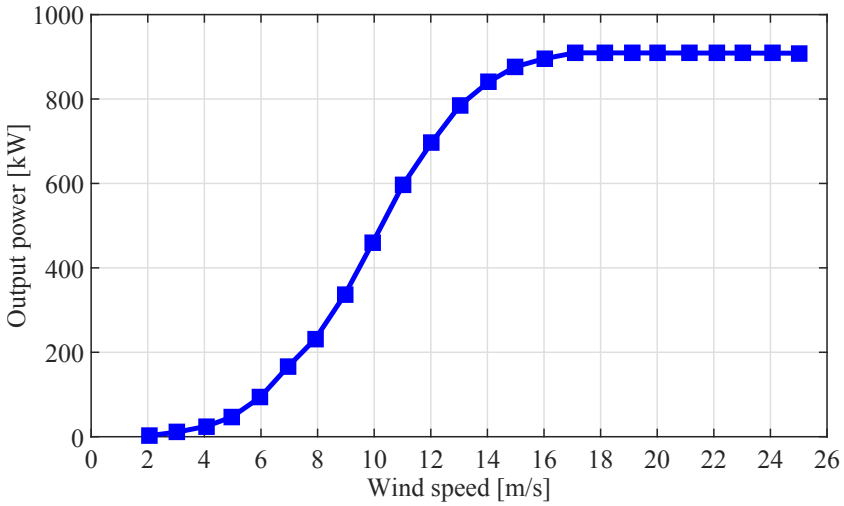


Figure 6.16: 900 kW wind turbine output power at hub hight 45m [86].

Table 6.5: Body-diode on-state voltage and resistance parameters

Parameter	Value
α	-3×10^{-3}
β	-6.2×10^{-3}
V_{D0}	2.77
R_{D0}	0.034

6.5.2. Simulation and discussion

The simulation was made on a 0.9 MW three-phase wind inverter for wind speeds ranging from 3 to 25 m/s. The converter is assumed to be composed of 10 chips of 3.3kV/50A SiC-MOSFETs in parallel per switch. The DC-link voltage of 1.8 kV, grid transformer primary side voltage of 1.1 kV and a line frequency of 50 Hz was used. The efficiency at different switching frequencies and heat-sink temperatures are studied.

Switching frequency performance

The inverter efficiency from 3 to 25 m/s based on a 3.3kV SiC MOSFET operating at different switching frequencies in the range of 1 kHz to 8 kHz is shown in Fig. 6.17. The power cell efficiency of the wind inverter with SiC MOSFETs shows very good performance over the whole range of operation at 1 kHz, which is the edge of the switching frequency range for HV Si IGBTs [80]. The inverter reaches 99.6% at wind speed of 7 m/s. Moreover, the inverter efficiency over a range of switching frequencies shows the possibility of increasing the switching frequency by a factor of 3 to 5. This merit of SiC devices can lead to reducing the size of bulky passive elements in a 2-level topology.

Table 6.6: Switching losses parameters

Parameter	Value
b_2	0.0002
b_1	0.1211
b_0	0.8771

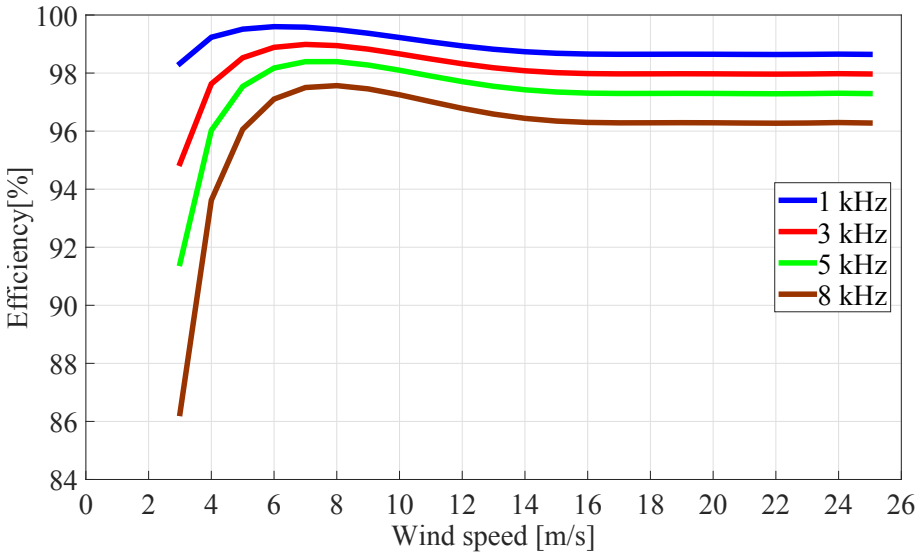


Figure 6.17: SiC inverter efficiency versus wind speed at different switching frequencies

Temperature performance

Fig. 6.18 shows that the inverter efficiency is virtually independent of the heat-sink temperature over a broad range of temperature values. SiC devices show a 0.48% drop in efficiency over the whole tested temperature range. This finding confirms previous observations on low voltage SiC inverters, for which this particular feature has already been proven to be associated with disruptive possibilities to optimize system level power densities by optimization of both the switching frequency and the heat-sink.

6.6. Conclusion

The results presented show clearly that the 3.3 kV SiC MOSFETs considered here are very advanced and technologically mature; they have the required characteristics to enable major impacts in replacing IGBT + Diode solutions with more power dense and higher performance multi-chip modules. The body-diode is reliable and operates virtually reverse-recovery free. Initial results on the device performance considering both single and parallel chip operation are very encouraging, even with conventional packaging solutions. The analysis of 3.3 Kv SiC

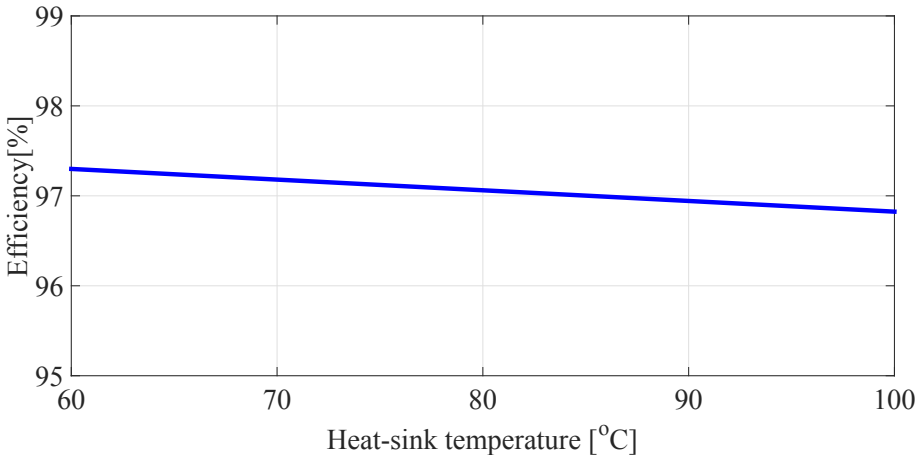


Figure 6.18: Efficiency of SiC inverter versus heat-sink temperature at 0.9 MW output power and switching frequency of 5 kHz

MOSFETs in the medium voltage wind inverter has led to a conclusion that the application of a SiC converter in the wind generation system will increase the switching frequency by up-to 3-5 times and improve the inverter temperature capability in comparison with HV Si IGBTs, which can lead to a reduction in system size and cost. These results are in line with the previous observations on low voltage SiC inverter.

Chapter 7

Conclusion and Future Work

In this chapter, the research finding drawn from this thesis and some recommendations for future work will be discussed.

7.1. Conclusion

This thesis has presented an investigation into wind turbines and their inverter topologies at low and medium voltage levels in Chapter 2. State-of-the-art 2L 3-phase wind inverter has been chosen and analysed with SiC-MOSFET and Si-IGBT devices at 1.2 kV blocking class for small-scale wind turbines. The benchmarking of devices include conduction, switching and inverter operation performance under various test conditions. SiC inverter provides better performance at low-loads correspond to the most probable wind speed distribution, and hence higher energy extraction from wind turbines can be achieved. In addition, it has been shown that using SiC power devices, the wind inverter has very good switching and thermal performance capability, and therefore higher inverter power density can be maintained by making use of SiC device solution, not only by reducing passive elements size but also by reducing the cooling system requirements. These results reasonably motivate the use of 2L 3-phase circuit topology with SiC MOSFETs to replace the existing Si IGBTs with more opportunity for higher performance and power density.

The discussion of WBG material properties and state-of-the-art semiconductor power devices were presented in Chapter 3. It also includes the conduction and switching characterization of SiC power module with 1.2 kV blocking voltage class under different test conditions. It has been shown that the power module, with a nominal rating of 20 A, exhibit very good MOSFET output and Schottky diode forward characteristics. The reduced dependence on switching frequency and baseplate temperature, and these key features of SiC can help deliver new ways of designing power electronics conversion systems, which can contribute to optimizing sys-

tem level power densities by joint optimization of the switching frequency and the heat-sink temperature.

The evaluation of wind inverter power cell in terms of power loss and efficiency at various power loading, different switching frequencies and different heat sink temperatures was discussed in Chapter 4, with the aim of proposing some design values for maximum exploitation of the potential benefits of SiC MOSFETs in wind energy applications. The experimental results show that SiC power MOSFETs have very good thermal behaviour over a wide range of heat sink temperatures and less dependence on switching frequency at heavy loads; this increases in the inverter power density without compromising the efficiency. In addition, the wind inverter losses breakdown shows that the switching losses dominate the total power cell loses at light loads; this leads to proposing an approach to maximize the low-load efficiency by varying the switching frequency as a function of the wind speed distribution. In addition, the capability of the reactive power handling to the grid is overall guaranteed by using SiC wind inverter with very small dependency on the power factor.

The joint electro-thermal and electro-magnetic design optimization of a 2L 3-phase voltage source inverter in terms of inverter performance and power density was discussed in Chapter 5. With the aim of maximizing the power density of the inverter, a combined heat-sink and output inductor-filter volume were reduced by increasing the heat-sink temperature from 60^oC to 90^oC, and choosing the optimum switching frequency at 32 kHz for minimum converter volume. To enable optimum efficiency versus power density trade-off, the inverter was redesigned with variable switching frequency, the nominal value is 32 kHz, decreasing in steps to 16 kHz as the load decreases. The output filter inductors were used to ensure compliance with the maximum admissible harmonics generation profiles even at the lower frequencies. This enables to a 37.8% increase in the inverter power density and saving up to 42.7% of the lost energy per year. This work is of relevance primarily to stationary systems, but also includes novel insight and results of straightforward spin-off transfer to a number of transport applications, including upcoming hybrid and fully electric naval and avionic applications.

In Chapter 6, the knowledge gained about LV SiC MOSFETs was transferred to HV ones, especially 3.3 kV. These devices not yet commercially available, but the results presented the 3.3 kV SiC MOSFETs considered here promising to become a key SiC component in the near future. They have superior requirements to replace the existing counterpart IGBTs with external diode solutions to achieve higher power density and higher performance multi-chip modules. The body-diode works reliably with almost zero reverse recovery current, balanced sharing current during the very high switching transient and good stable temperature operation over a representative range of baseplate temperatures. In addition, using the MOSFET body-diode and synchronous rectification can help to reduce the body-diode on-state losses up to considerable operational temperature values. Therefore, the 3.3 kV SiC devices are very advanced technology and may deliver potential benefits both in converter and system level on

a number of application domains. Also, the analysis of 3.3 kV SiC MOSFETs in the medium voltage wind inverter has lead to a conclusion that the application of a SiC converter in the wind generation system will increase the switching frequency up-to 3-5 times and improve the inverter temperature capability in comparison with HV Si IGBTs, which can lead to reduce the system's size and cost. These results are in line with the previous observations on low voltage SiC inverter. This study is of relevance primarily to wind energy systems, but also includes an insight to a number of other HV applications, including railway traction and solid state transformers.

7.2. Future work

The work that has been presented in this thesis has investigate the potential benefits of SiC MOSFETs in wind energy applications. However, the following points can be investigated further:

- This thesis has shown the superior SiC devices electro-thermal properties when compared to Si, makes the WBG-material be a good candidate for higher performance and power density applications. More intensive work on power cycling based on a mission profile (i.e renewable energy, hybrid and fully electric vehicles) is still necessary for SiC devices. Fig. 7.1 shows the thermal cycling stress in 12 kW 2L topology inverter due to wind speed and ambient temperature mission profiles stress; replacing Si IGBTs with SiC MOSFETs solution can reduce the number of thermal cycles with large amplitude of ΔTj which has the main contribution to the damage. However, at the moment of writing, there are no lifetime models available for SiC power module to demonstrate the impact of SiC reliability on the inverter design optimisation.

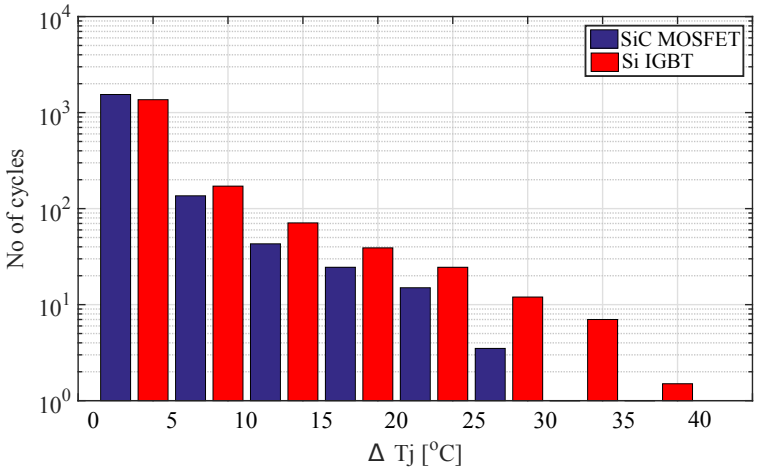


Figure 7.1: Rain-flow counting results of number of thermal cycles and cycle amplitude under a yearly mission profile of 1-hour averaged for the stressed devices in 2L-VSI.

- This study focuses on the grid-connected wind inverter, where the SiC MOSFET is considered more preferable since it provides valuable changes not only in the annual energy, but also in power density, thermal stress and, as a result, reliability of the system. Implementation of the generator-side rectifier and boost stage converter using SiC devices still requires more investigation. Despite the comparable on-state performance of SiC Schottky diode and Si P-i-N diode, the SiC diode in the rectifier stage features lower turn-off switching losses, which makes its implementation highly desirable. At the same time, the possibility of higher switching frequency operation in the dc/dc boost stage using SiC MOSFET devices can gain a massive decrease in the inductor-filter and dc-link capacitor sizes. In addition, it is recommended that future work looks at modularising and optimising the mission profile of the wind turbine converter system in order to determine the optimal distribution of the active and passive components for minimal losses and ensure high reliability in order to extend the lifetime of the system, and therefore reduce the cost of energy generation. This study is more relevant to wind energy applications, but also includes novel insights and results of straightforward spin-off transfer to other renewable energy systems, including photovoltaic application specially, to enable very high efficiency and very high power density by increased switching frequency.

- In this thesis, a detailed parametric characterization of a 3.3 kV SiC MOSFET half-bridge module with parallel chips and body-diode freewheeling is presented. The preliminary results show that the device performance with parallel-chip and body-diode are very encouraging. Further tests will include extended operation in an inverter and active rectifier modes; investigation of the synchronous rectification in inverter operation and comparison with a conventional operation using freewheeling diode are still needed. In addition, it is still necessary to assess is the out-of-SOA (Safe Operating Area) transient robustness and long-term stability of the MOSFET and body-diode under various operational conditions.

- Power converters used in renewable energy conversion have to deal with intermittent and variable power availability from the source. They actually work under light-load conditions for most of their operational time which result in worse harmonics performance. A variable filter-inductor which has higher inductance at low power compared to its inductance value at rated power is recommended for future work to reduce current harmonics in all converter operating conditions.

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